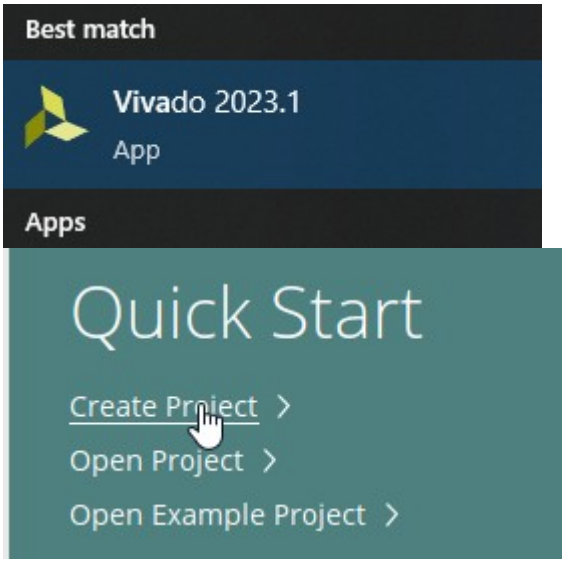
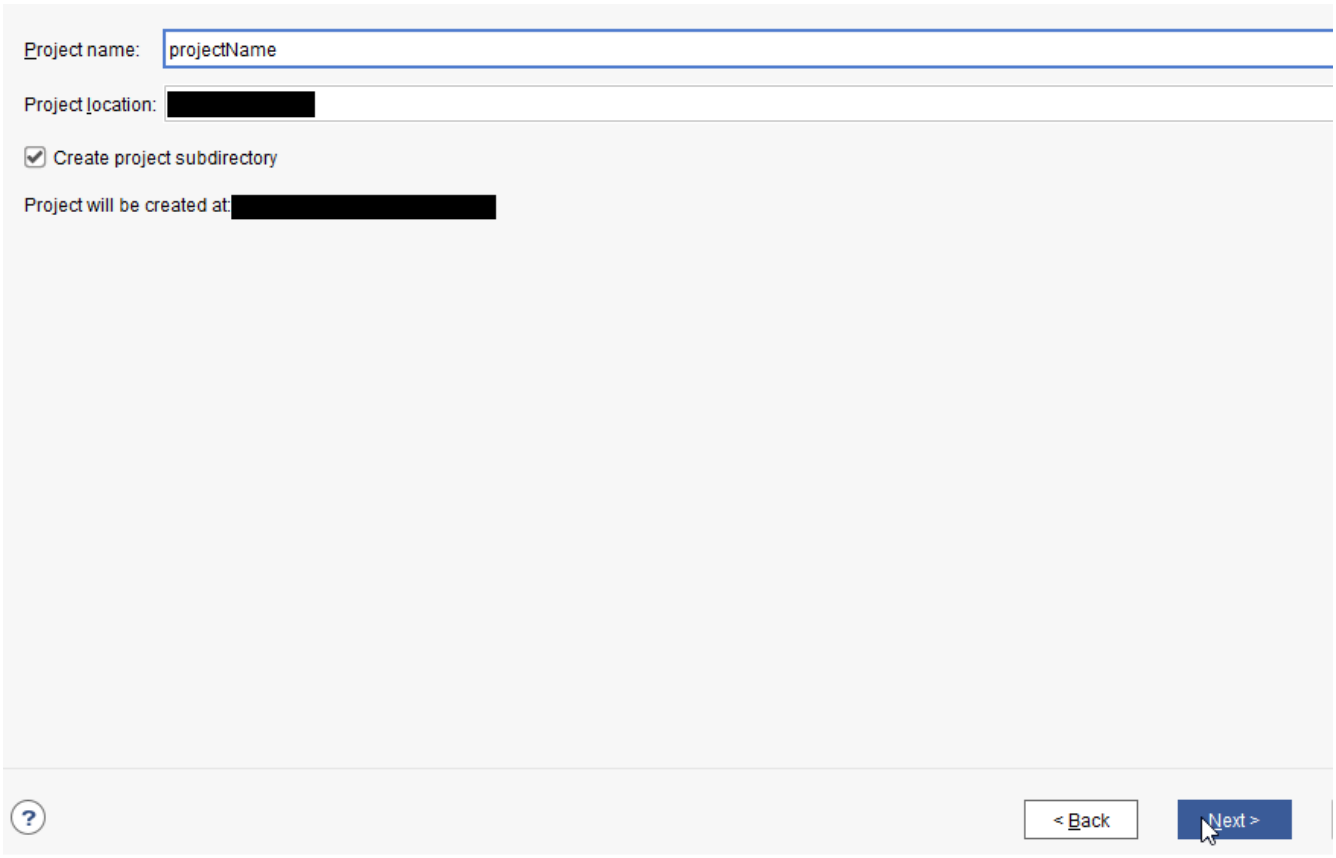
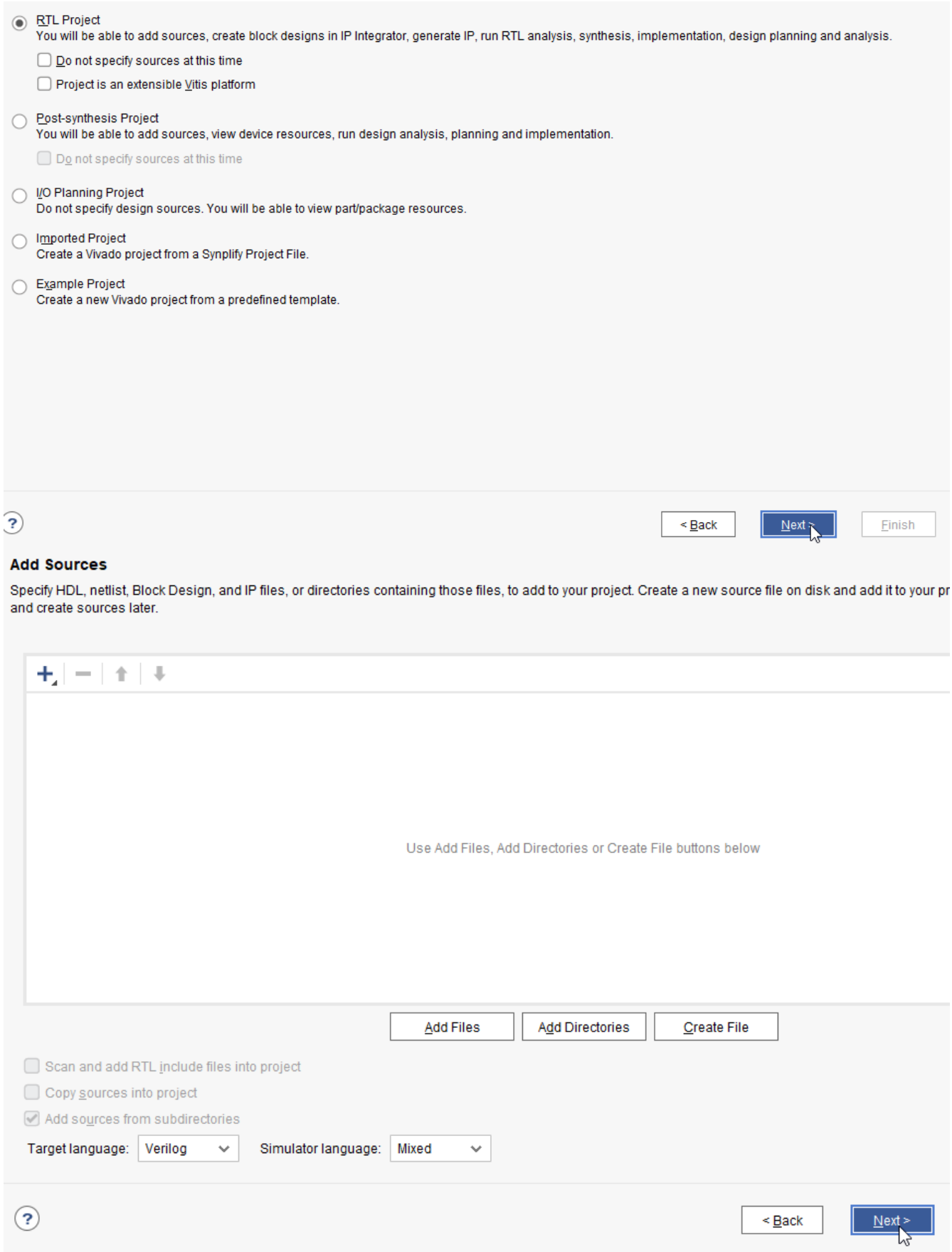
Mesh of following tutorials:
Getting started from scratch with Digilent Zybo Z7 Xilinx Zynq FPGA board using Vivado 2018.3: https://www.youtube.com/watch?v=12mnBk5SrIk
Vitis Beginner Tutorial- Creating GPIO project: https://www.youtube.com/watch?v=3D2-OPArCiA

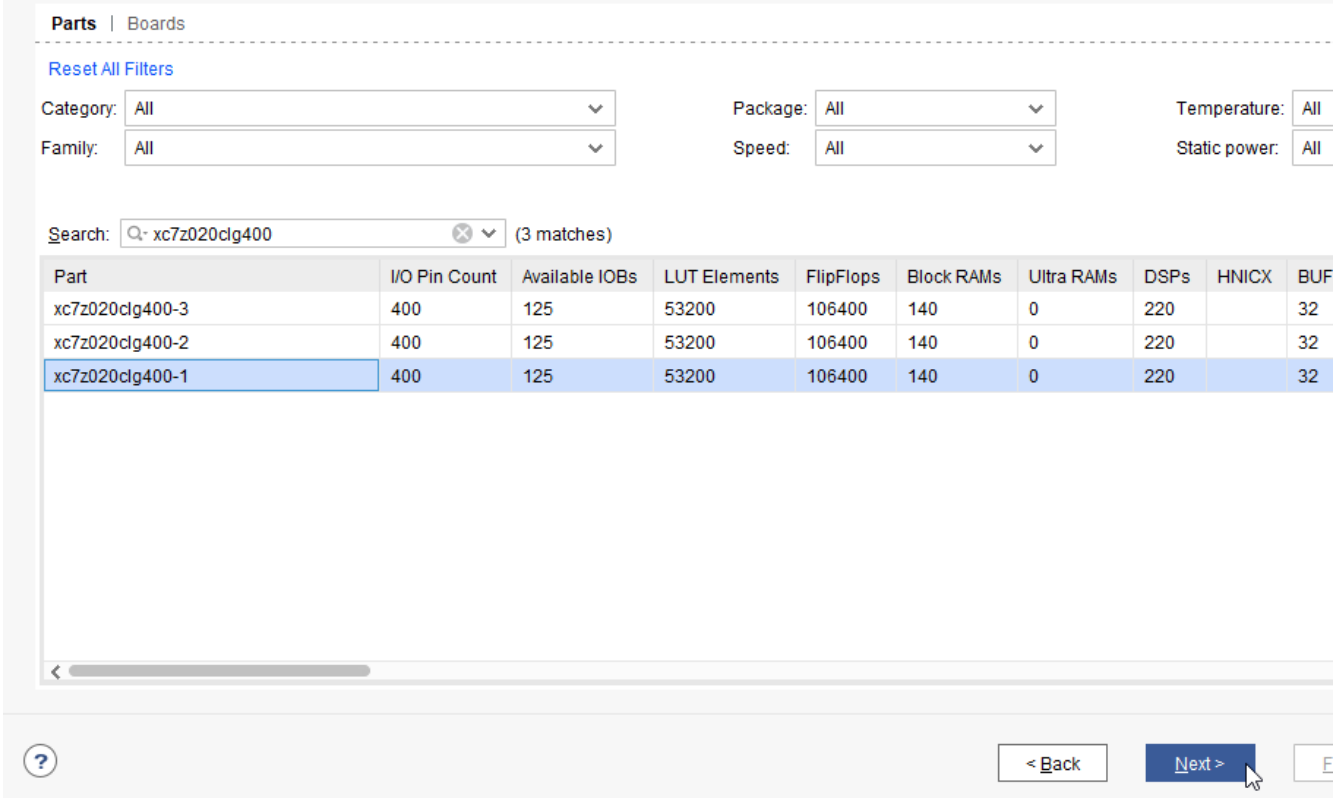




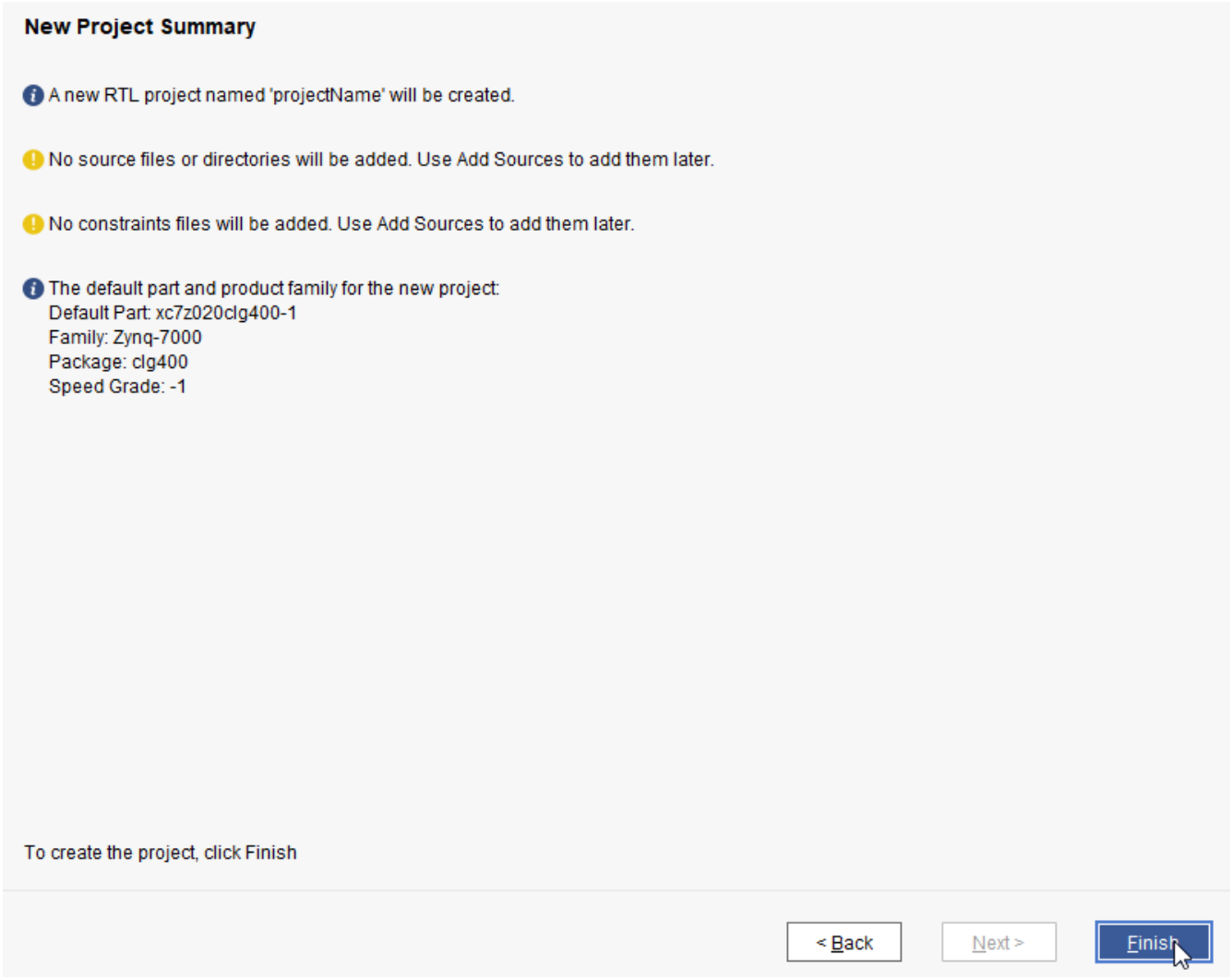

RTL Project
You will be able to add sources, create block designs in IP Integrator, generate IP, run RTL analysis, synthesis, implementation, design planning and analysis.
Do not specify sources at this time
Project is an extensible Vitis platform
Post-synthesis Project
You will be able to add sources, view device resources, run design analysis, planning and implementation.
Do not specify sources at this time
I/O Planning Project
Do not specify design sources. You will be able to view part/package resources.
Imported Project
Create a Vivado project from a Synplify Project File.
Example Project
Create a new Vivado project from a predefined template.
< Back
Next >
Finish
Add Sources
Specify HDL, netlist, Block Design, and IP files, or directories containing those files, to add to your project. Create a new source file on disk and add it to your pr
and create sources later.
Use Add Files, Add Directories or Create File buttons below
Add Files
Add Directories
Create File
Scan and add RTL include files into project
Copy sources into project
Add sources from subdirectories
Target language: Verilog
Simulator language: Mixed
< Back
Next >

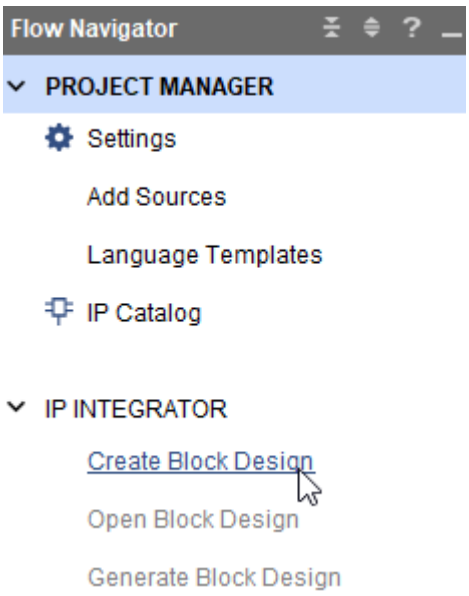
Default Part

Choose a default Xilinx part or board for your project.



< Back Next >


New Project Summary
A new RTL project named 'projectName' will be created.
No source files or directories will be added. Use Add Sources to add them later.
No constraints files will be added. Use Add Sources to add them later.
The default part and product family for the new project:
Default Part: xc7z020clg400-1
Family: Zynq-7000
Package: clg400
Speed Grade: -1
To create the project, click Finish
< Back
Next >
Finish


Flow Navigator
PROJECT MANAGER
Settings
Add Sources
Language Templates
IP Catalog
IP INTEGRATOR
Create Block Design
Open Block Design
Generate Block Design

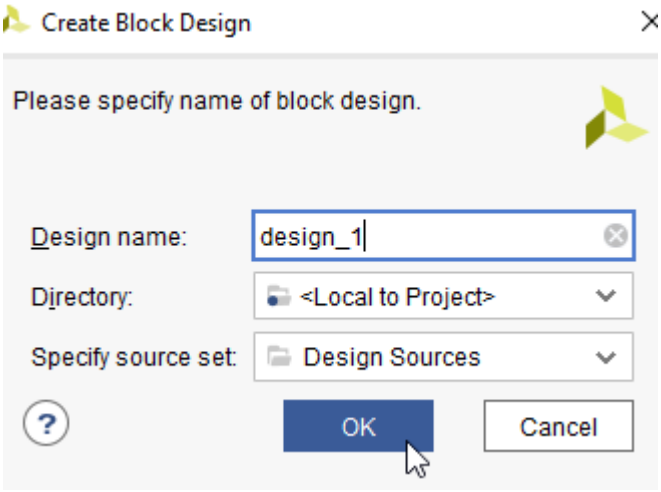
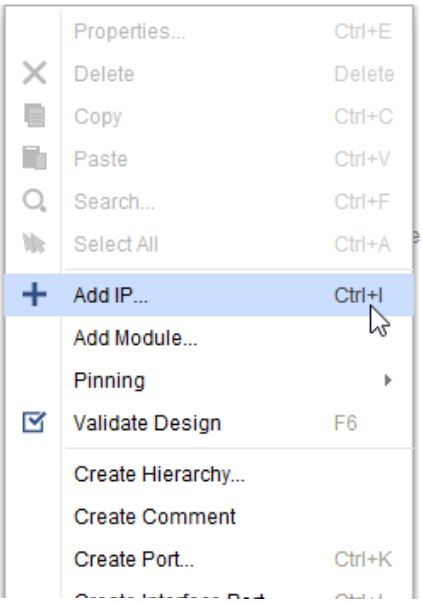
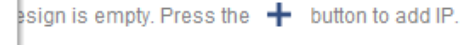
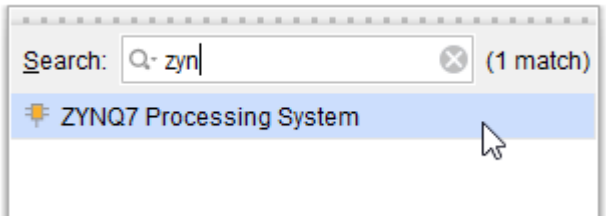
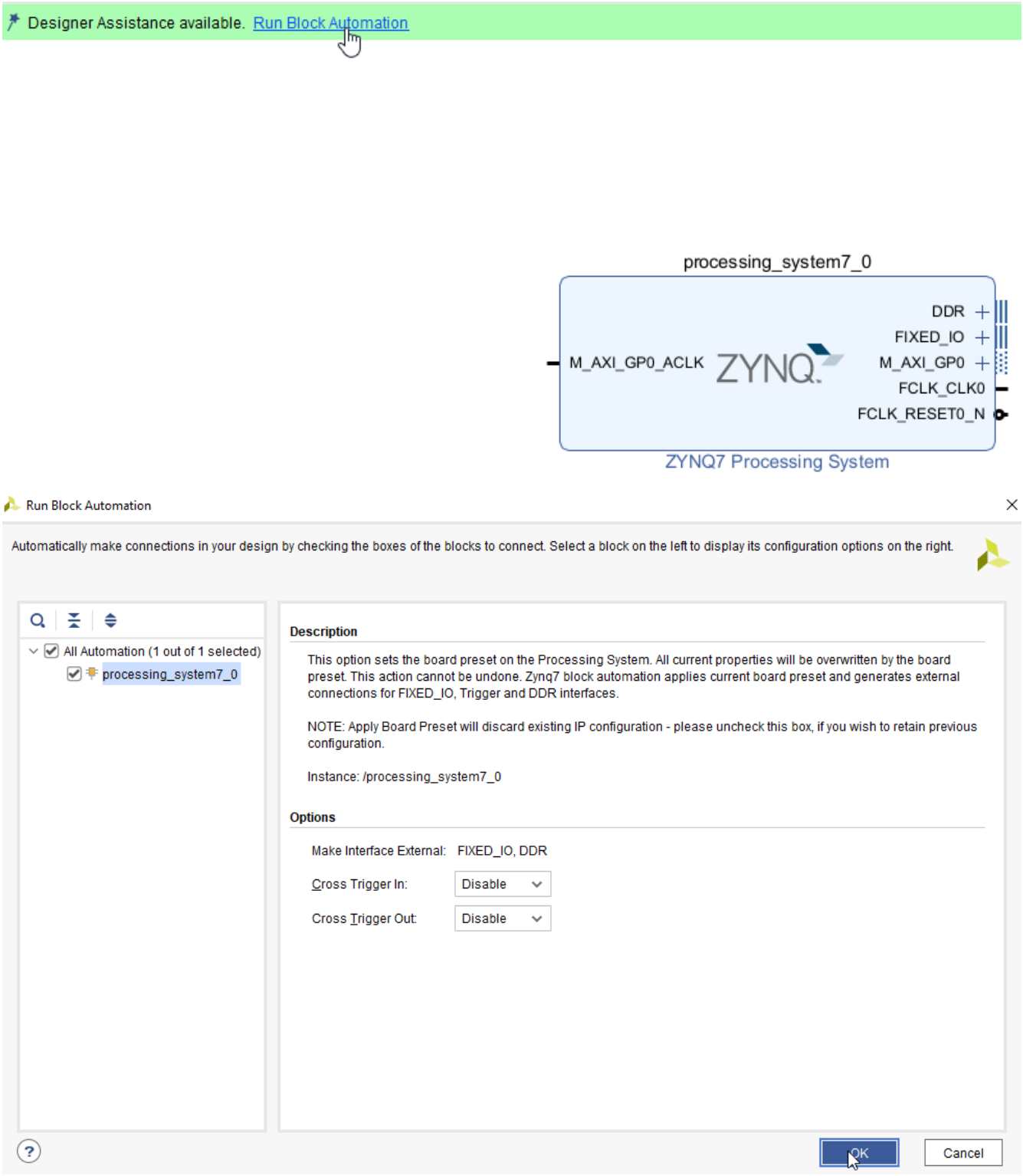

Create Block Design
Please specify name of block design.
Design name:
design_1
Directory:
<Local to Project>
Specify source set:
Design Sources
OK
Cancel

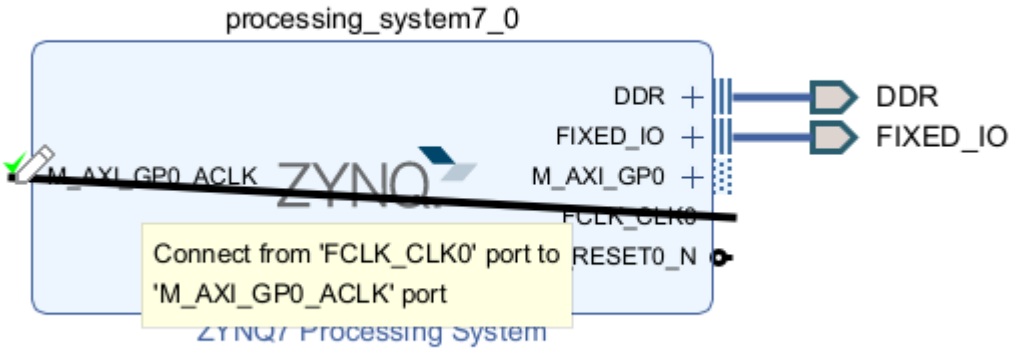

Diagram
Default View

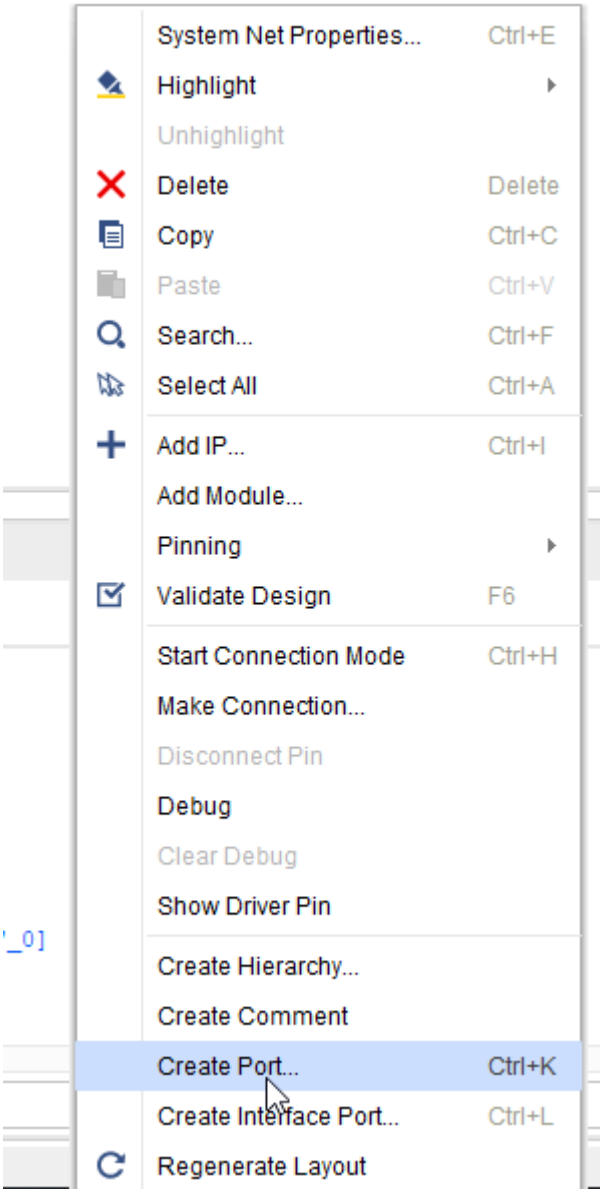

Properties... Ctrl+E
Delete Delete
Copy Ctrl+C
Paste Ctrl+V
Search... Ctrl+F
Select All Ctrl+A
Add IP... Ctrl+I
Add Module...
Pinning
Validate Design F6
Create Hierarchy...
Create Comment
Create Port... Ctrl+K

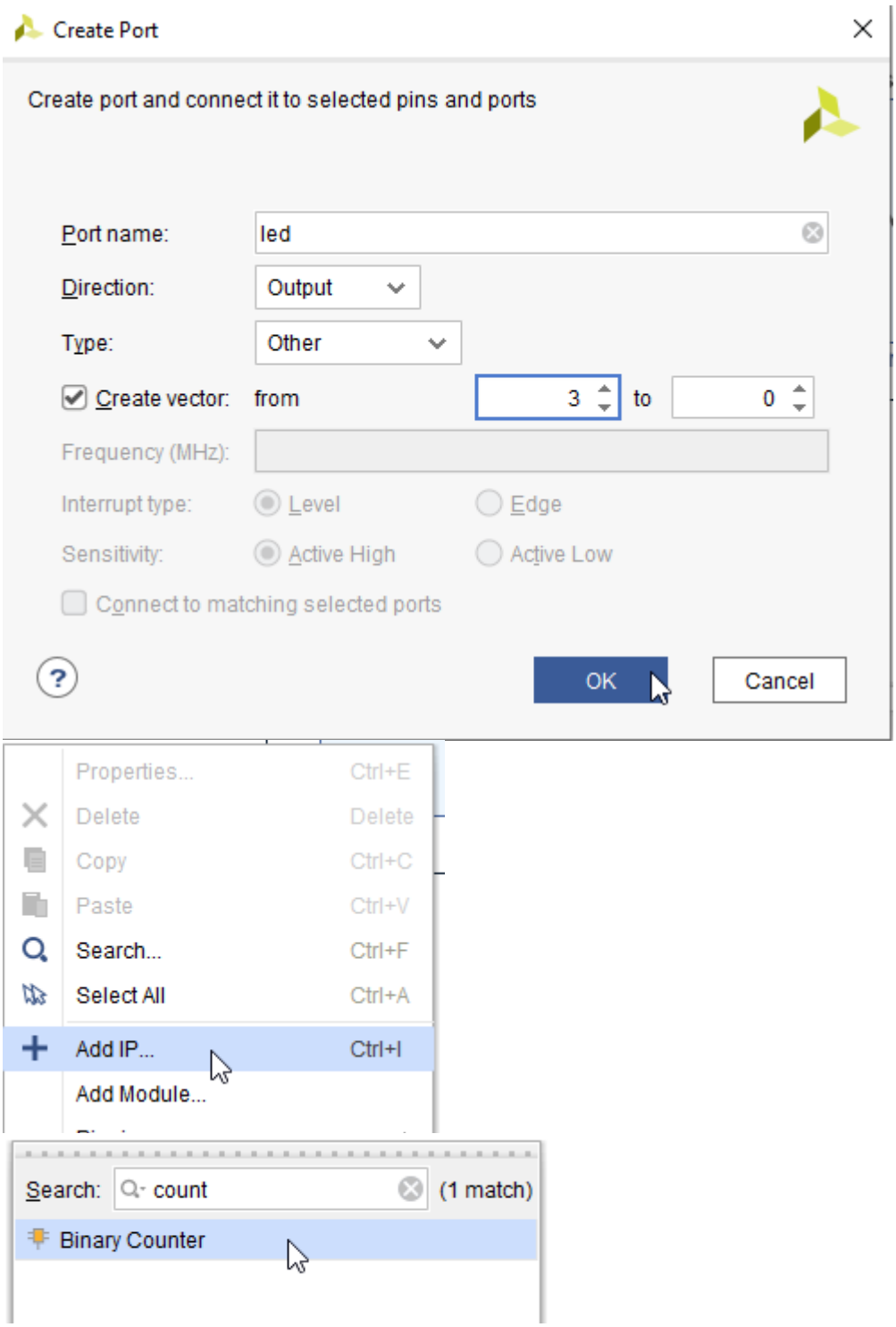

esign is empty. Press the button to add IP.

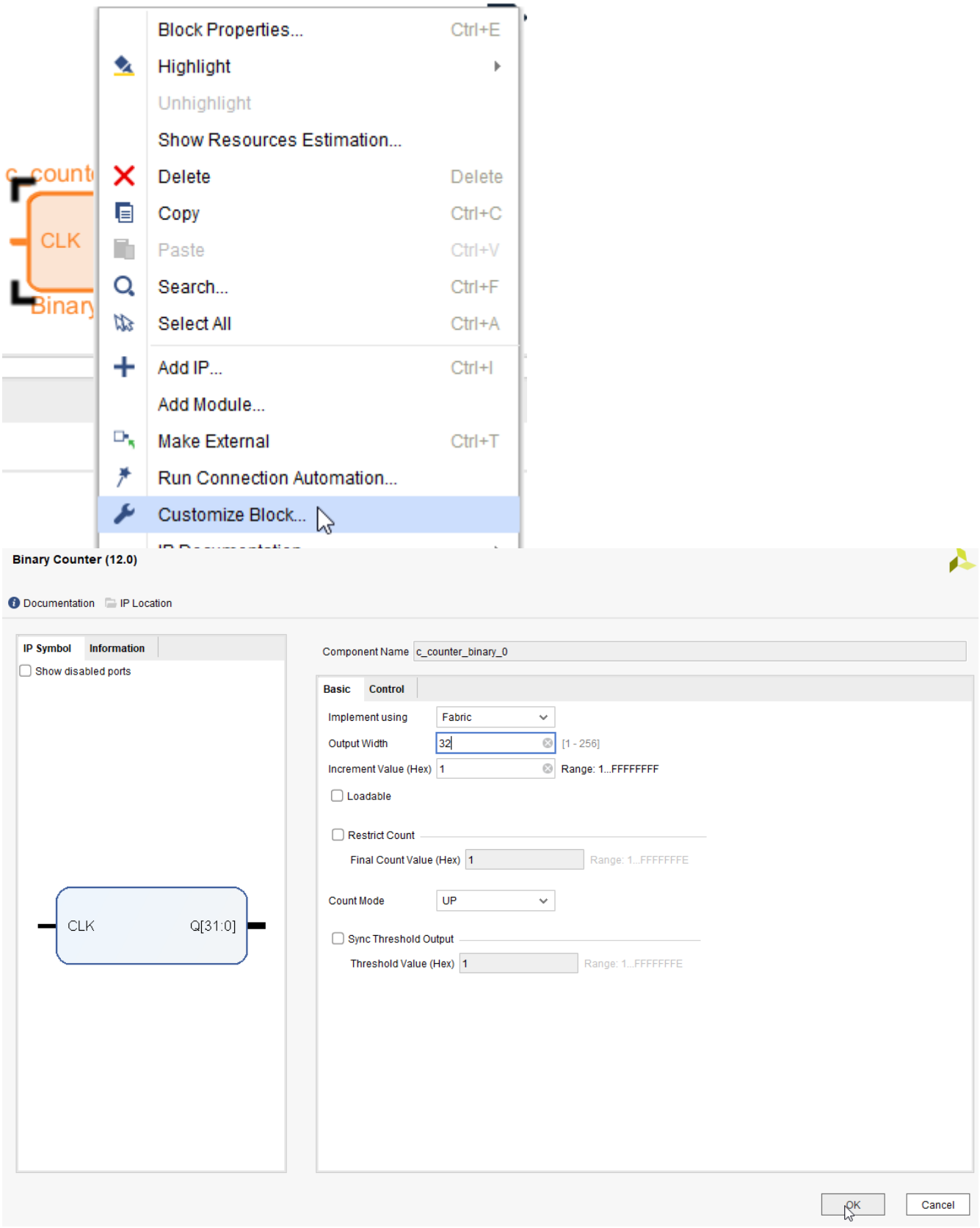

Search: zyn
(1 match)
ZYNQ7 Processing System

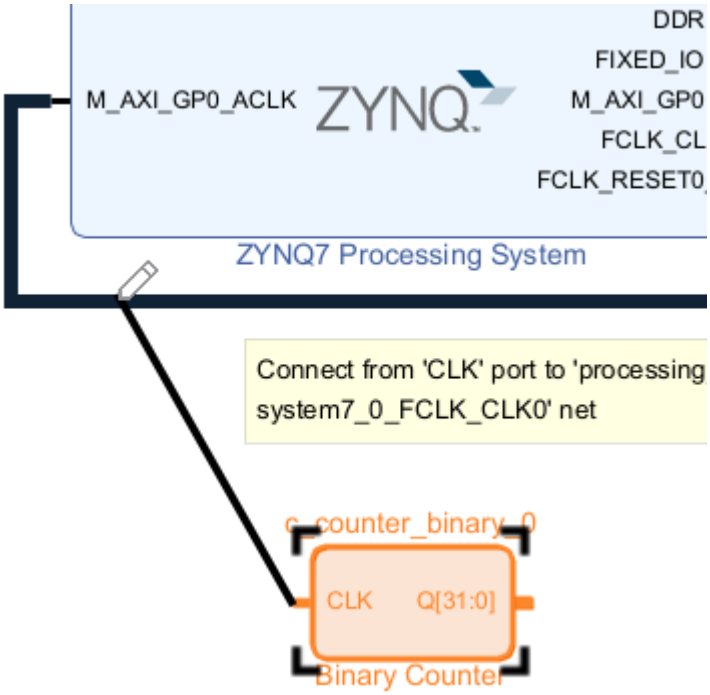

Designer Assistance available. Run Block Automation
processing_system7_0
M_AXI_GP0_ACLK
ZYNQ
DDR
FIXED_IO
M_AXI_GP0
FCLK_CLK0
FCLK_RESET0_N
ZYNQ7 Processing System
Run Block Automation
Automatically make connections in your design by checking the boxes of the blocks to connect. Select a block on the left to display its configuration options on the right.
All Automation (1 out of 1 selected)
processing_system7_0
Description
This option sets the board preset on the Processing System. All current properties will be overwritten by the board preset. This action cannot be undone. Zynq7 block automation applies current board preset and generates external connections for FIXED_IO, Trigger and DDR interfaces.
NOTE: Apply Board Preset will discard existing IP configuration - please uncheck this box, if you wish to retain previous configuration.
Instance: /processing_system7_0
Options
Make Interface External: FIXED_IO, DDR
Cross Trigger In: Disable
Cross Trigger Out: Disable
OK
Cancel

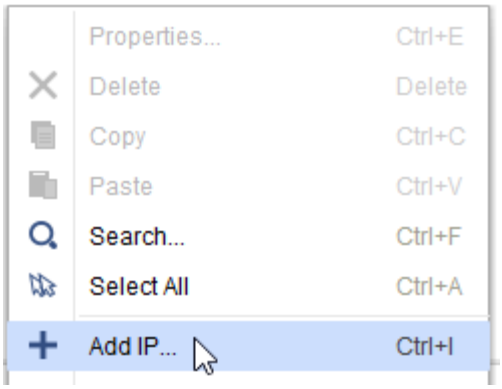

processing_system7_0
DDR
FIXED_IO
M_AXI_GP0
M_AXI_GP0_ACLK
ZYNQ
FCLK_CLK0
RESET0_N
Connect from 'FCLK_CLK0' port to 'M_AXI_GP0_ACLK' port
ZYNQ7 Processing System
DDR
FIXED_IO

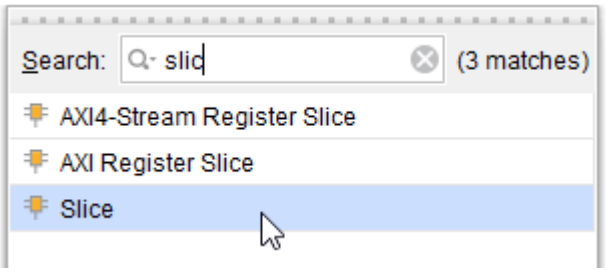

System Net Properties... Ctrl+E
Highlight
Unhighlight
Delete Delete
Copy Ctrl+C
Paste Ctrl+V
Search... Ctrl+F
Select All Ctrl+A
Add IP... Ctrl+I
Add Module...
Pinning
Validate Design F6
Start Connection Mode Ctrl+H
Make Connection...
Disconnect Pin
Debug
Clear Debug
Show Driver Pin
Create Hierarchy...
Create Comment
Create Port... Ctrl+K
Create Interface Port... Ctrl+L
Regenerate Layout

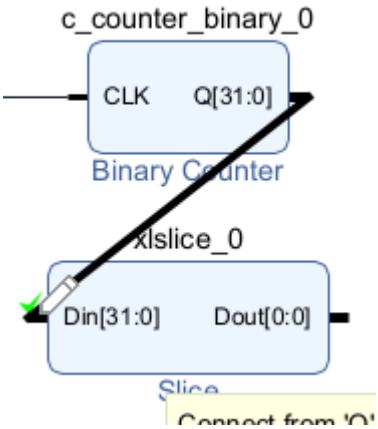

Create Port
Create port and connect it to selected pins and ports
Port name:
led
Direction:
Output
Type:
Other
Create vector:
from
3
to
0
Frequency (MHz):
Interrupt type:
Level
Edge
Sensitivity:
Active High
Active Low
Connect to matching selected ports
OK
Cancel
Properties... Ctrl+E
Delete Delete
Copy Ctrl+C
Paste Ctrl+V
Search... Ctrl+F
Select All Ctrl+A
Add IP... Ctrl+I
Add Module...
Search:
count
(1 match)
Binary Counter

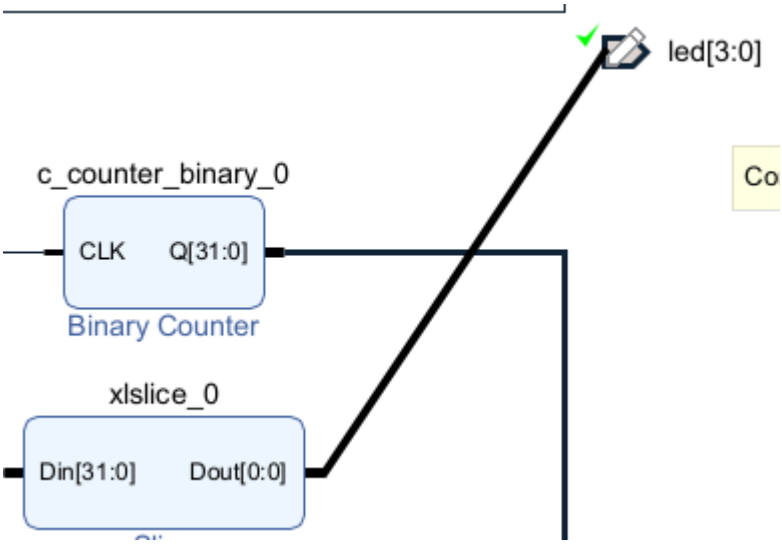

c_count
CLK
Binary
Block Properties... Ctrl+E
Highlight
Unhighlight
Show Resources Estimation...
Delete Delete
Copy Ctrl+C
Paste Ctrl+V
Search... Ctrl+F
Select All Ctrl+A
Add IP... Ctrl+I
Add Module...
Make External Ctrl+T
Run Connection Automation...
Customize Block...
Binary Counter (12.0)
Documentation
IP Location
IP Symbol
Information
Show disabled ports
CLK
Q[31:0]
Component Name
c_counter_binary_0
Basic
Control
Implement using
Fabric
Output Width
32
[1 - 256]
Increment Value (Hex)
1
Range: 1...FFFFFFFF
Loadable
Restrict Count
Final Count Value (Hex)
1
Range: 1...FFFFFFFE
Count Mode
UP
Sync Threshold Output
Threshold Value (Hex)
1
Range: 1...FFFFFFFE
OK
Cancel

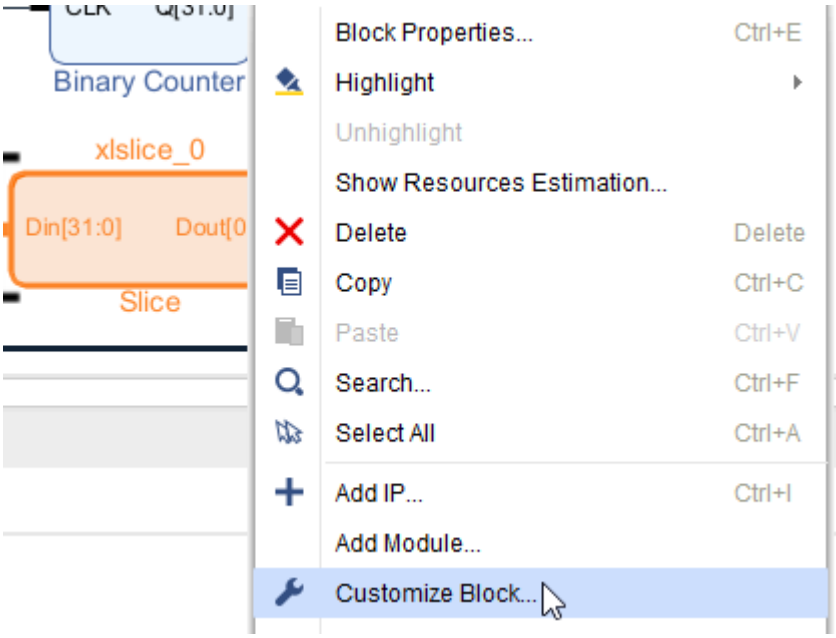

DDR
FIXED_IO
M_AXI_GP0_ACLK
ZYNQ
M_AXI_GP0
FCLK_CL
FCLK_RESET0_
ZYNQ7 Processing System
Connect from 'CLK' port to 'processing
system7_0_FCLK_CLK0' net
counter_binary_0
CLK
Q[31:0]
Binary Counter

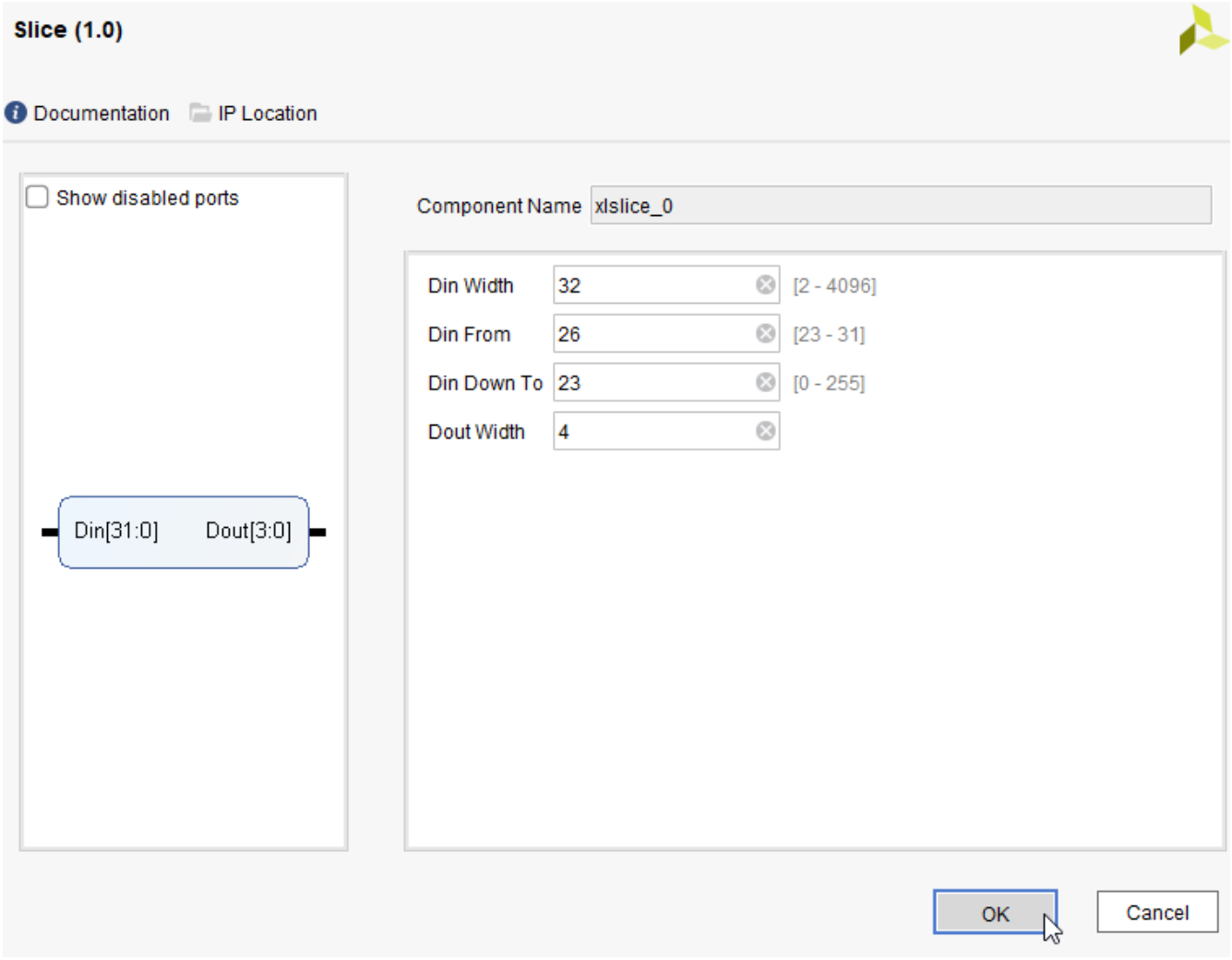

Properties... Ctrl+E
Delete Delete
Copy Ctrl+C
Paste Ctrl+V
Search... Ctrl+F
Select All Ctrl+A
Add IP... Ctrl+I


Search: slic
(3 matches)
AXI4-Stream Register Slice
AXI Register Slice
Slice


c_counter_binary_0
CLK
Q[31:0]
Binary Counter
xlslice_0
Din[31:0]
Dout[0:0]


led[3:0]
c_counter_binary_0
CLK
Q[31:0]
Binary Counter
xlslice_0
Din[31:0]
Dout[0:0]


Binary Counter
xlslice_0
Din[31:0]
Slice
Block Properties... Ctrl+E
Highlight
Unhighlight
Show Resources Estimation...
Delete Delete
Copy Ctrl+C
Paste Ctrl+V
Search... Ctrl+F
Select All Ctrl+A
Add IP... Ctrl+I
Add Module...
Customize Block...


Slice (1.0)
Documentation
IP Location
Show disabled ports
Component Name
xlslice_0
Din Width
32
[2 - 4096]
Din From
26
[23 - 31]
Din Down To
23
[0 - 255]
Dout Width
4
Din[31:0]
Dout[3:0]
OK
Cancel

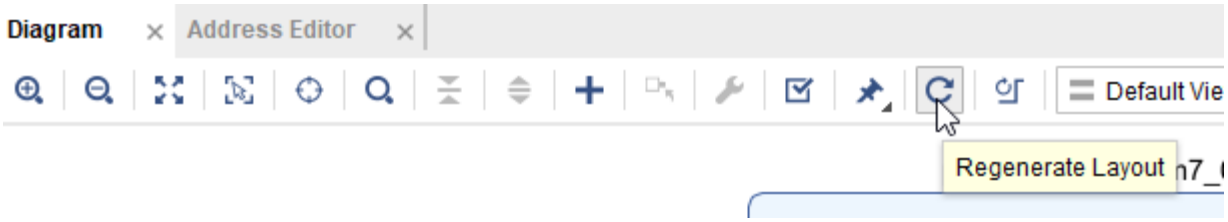
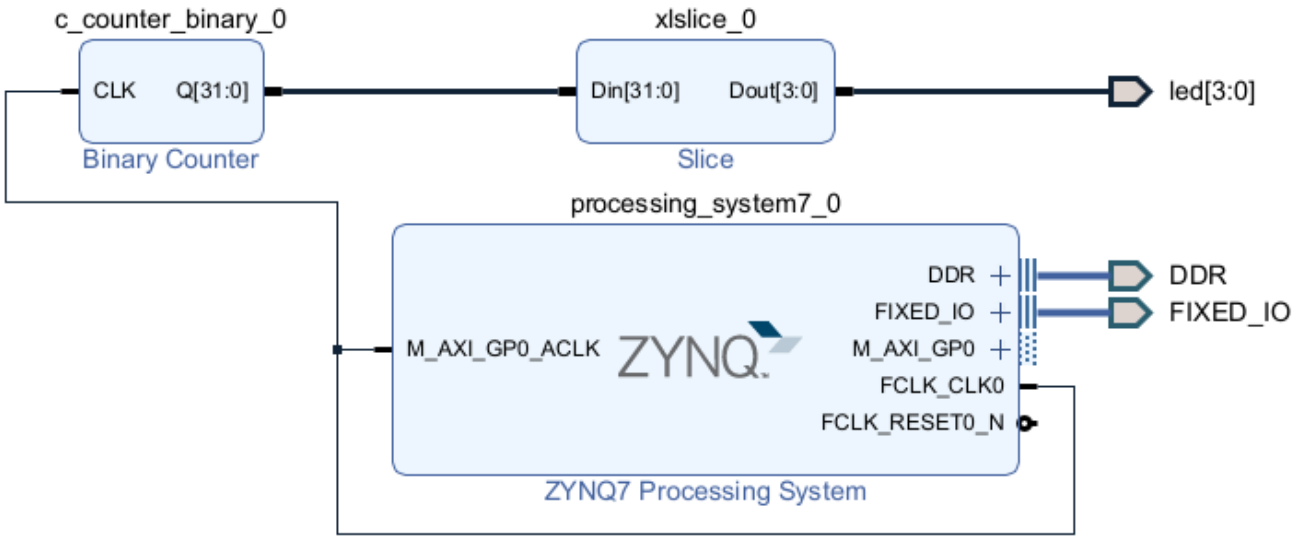
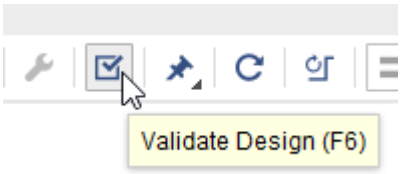
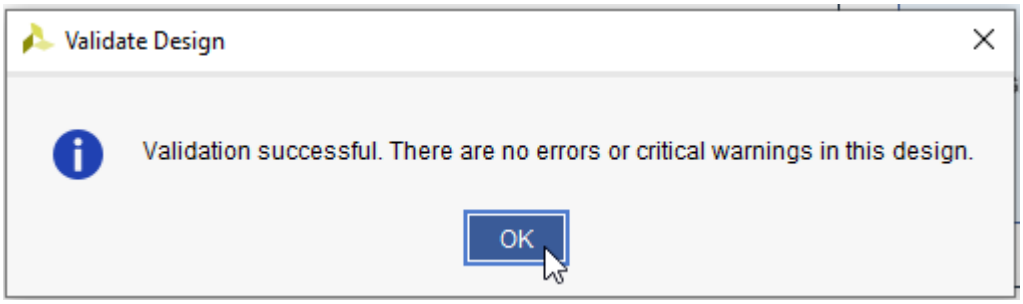
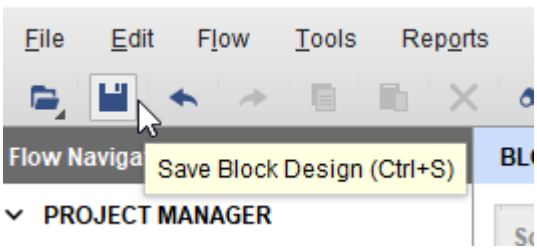


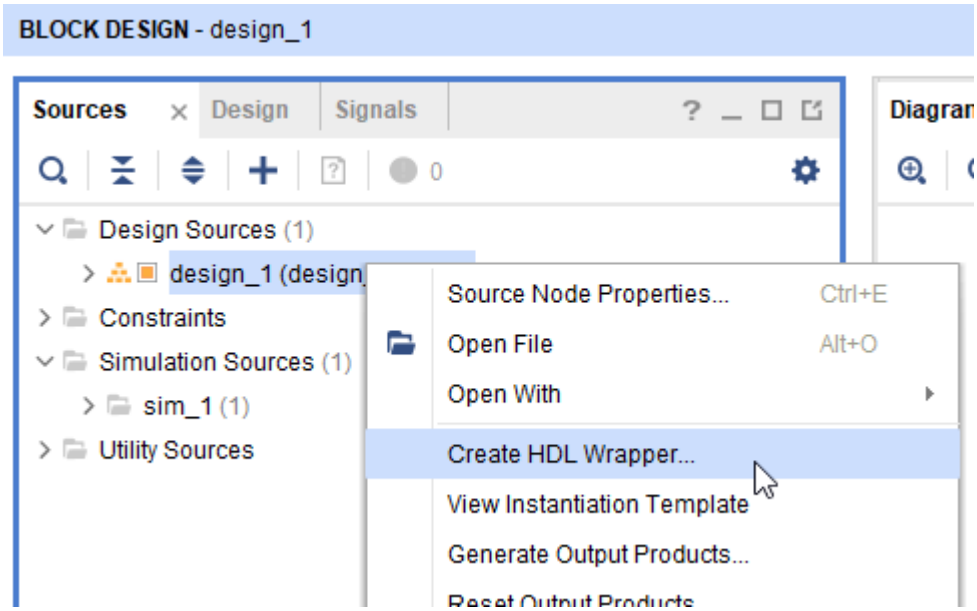
Diagram
Address Editor
Default Vie
Regenerate Layout

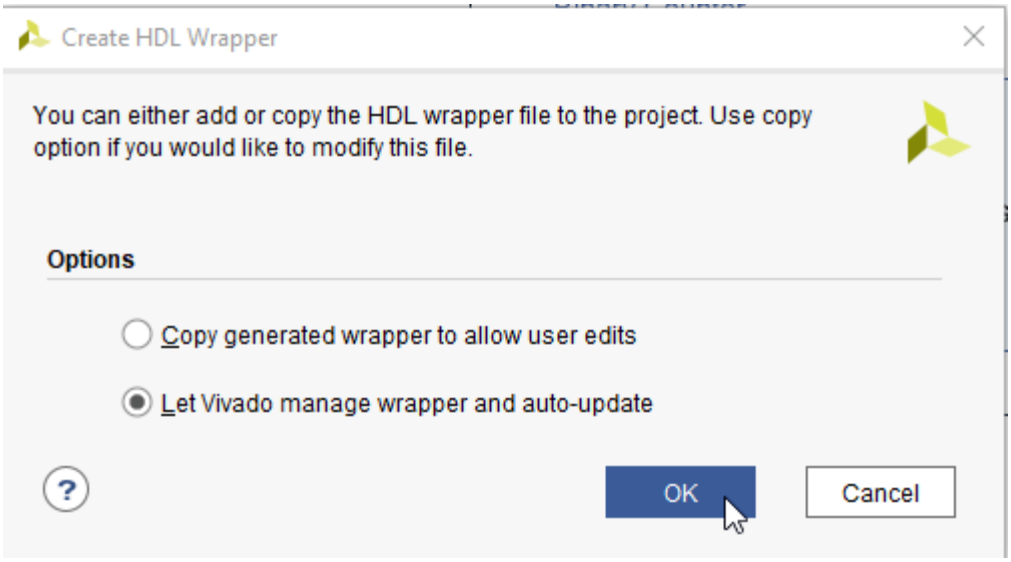

c_counter_binary_0
CLK
Q[31:0]
Binary Counter
xlslice_0
Din[31:0]
Dout[3:0]
Slice
led[3:0]
processing_system7_0
M_AXI_GP0_ACLK
ZYNQ
DDR
FIXED_IO
M_AXI_GP0
FCLK_CLK0
FCLK_RESET0_N
ZYNQ7 Processing System
DDR
FIXED_IO

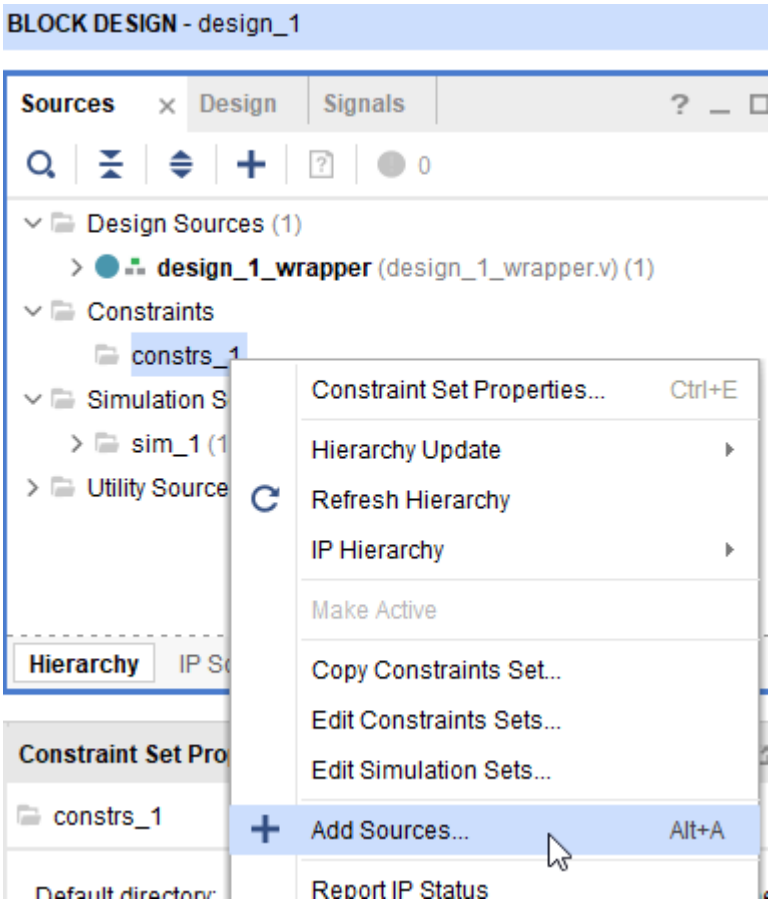

Validate Design (F6)

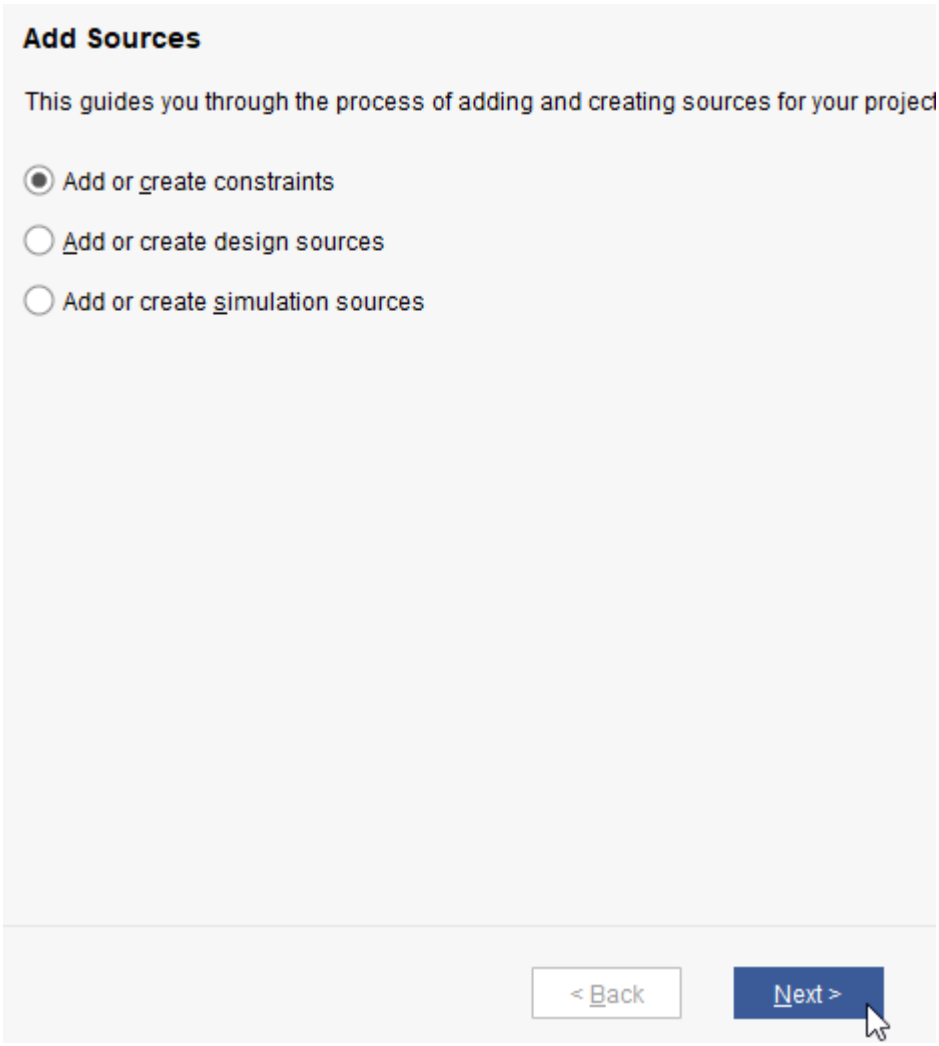

Validate Design
Validation successful. There are no errors or critical warnings in this design.
OK

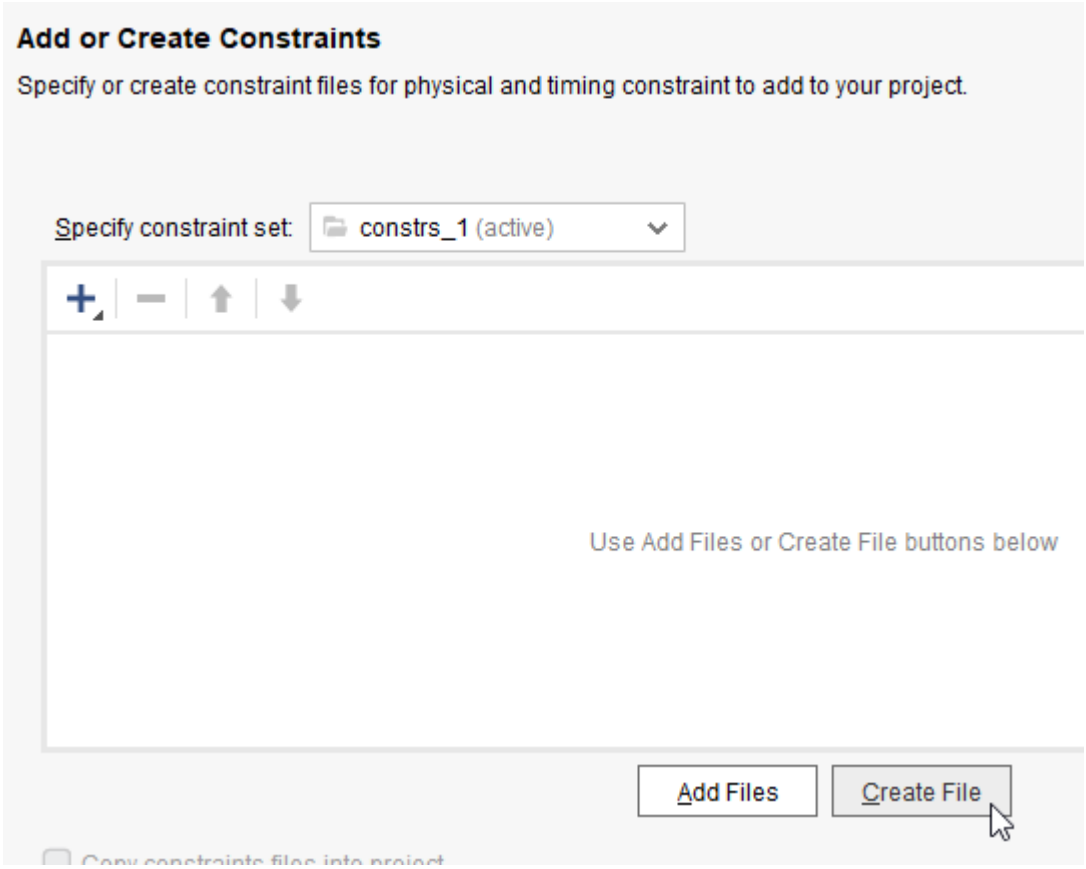

File
Edit
Flow
Tools
Reports
Save Block Design (Ctrl+S)
PROJECT MANAGER

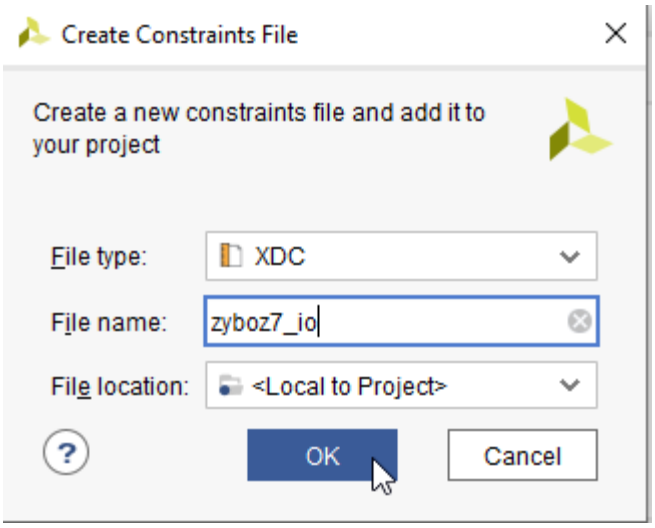

BLOCK DESIGN - design_1
Sources
Design
Signals
Design Sources (1)
design_1 (design_
Constraints
Simulation Sources (1)
sim_1 (1)
Utility Sources
Source Node Properties... Ctrl+E
Open File Alt+O
Open With
Create HDL Wrapper...
View Instantiation Template
Generate Output Products...

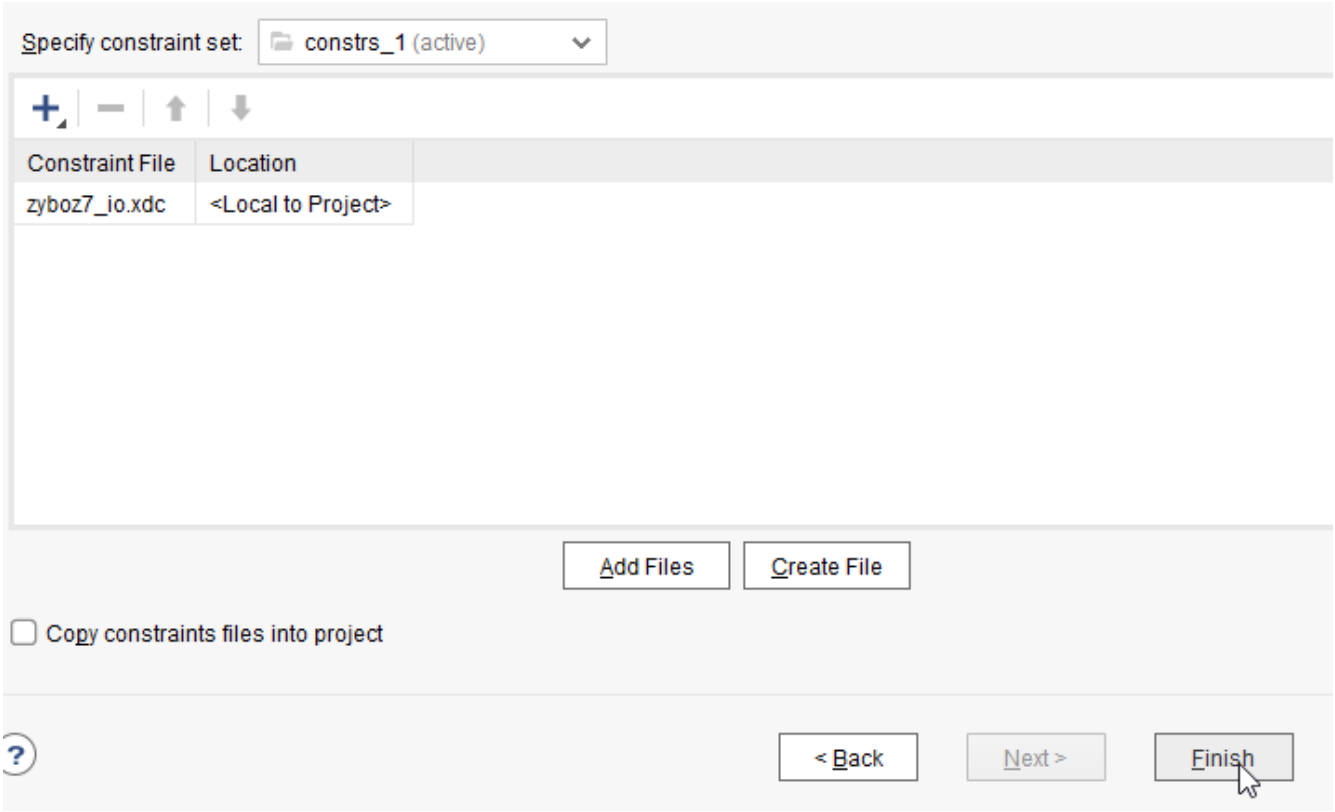

Create HDL Wrapper
You can either add or copy the HDL wrapper file to the project. Use copy option if you would like to modify this file.
Options
Copy generated wrapper to allow user edits
Let Vivado manage wrapper and auto-update
OK
Cancel

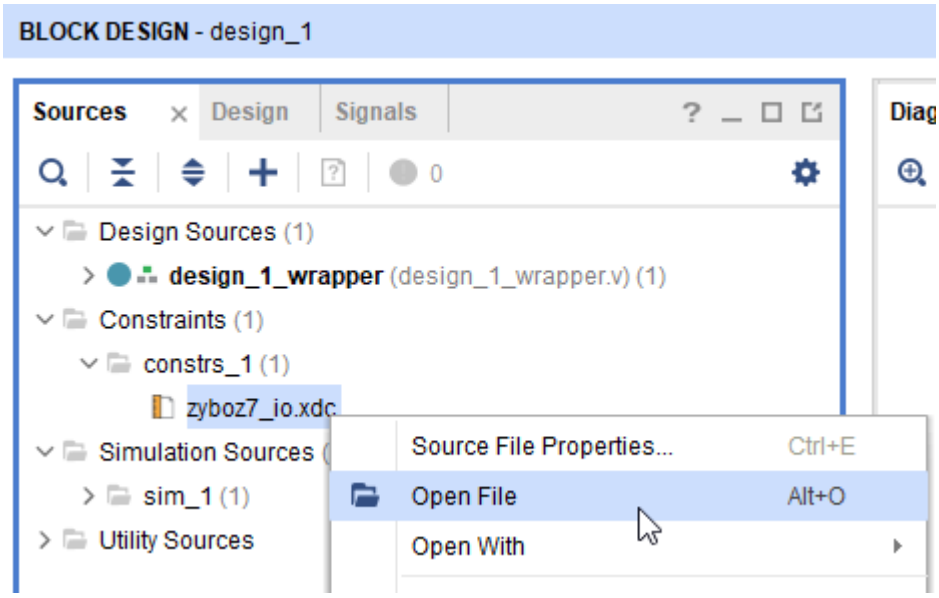

BLOCK DESIGN - design_1
Sources
Design
Signals
Design Sources (1)
design_1_wrapper (design_1_wrapper.v) (1)
Constraints
constrs_1
Simulation S
sim_1 (1
Utility Source
Hierarchy
IP S
Constraint Set Pro
constrs_1
Default directory:
Constraint Set Properties... Ctrl+E
Hierarchy Update
Refresh Hierarchy
IP Hierarchy
Make Active
Copy Constraints Set...
Edit Constraints Sets...
Edit Simulation Sets...
Add Sources... Alt+A
Report IP Status


Add Sources
This guides you through the process of adding and creating sources for your project
Add or create constraints
Add or create design sources
Add or create simulation sources
< Back
Next >


Add or Create Constraints
Specify or create constraint files for physical and timing constraint to add to your project.
Specify constraint set:
constrs_1 (active)
Use Add Files or Create File buttons below
Add Files
Create File


Create Constraints File
Create a new constraints file and add it to your project
File type:
XDC
File name:
zyboz7_io
File location:
<Local to Project>
OK
Cancel


Specify constraint set:
constrs_1 (active)
Constraint File
Location
zyboz7_io.xdc
<Local to Project>
Add Files
Create File
Copy constraints files into project
< Back
Next >
Finish


BLOCK DESIGN - design_1
Sources
Design
Signals
Design Sources (1)
design_1_wrapper (design_1_wrapper.v) (1)
Constraints (1)
constrs_1 (1)
zyboz7_io.xdc
Simulation Sources
sim_1 (1)
Utility Sources
Source File Properties... Ctrl+E
Open File Alt+O
Open With

https://digilent.com/reference/programmable-logic/zybo-z7/start

SHOP REFERENCE

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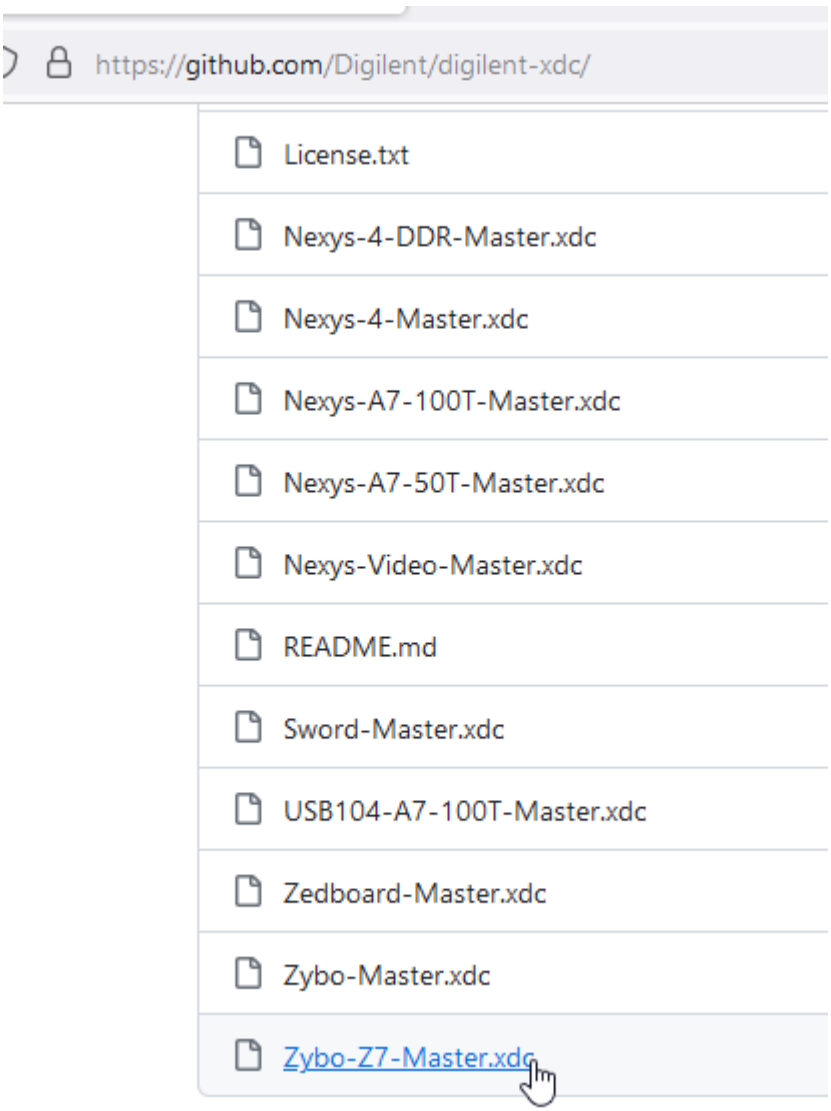
You are here:: Digilent Reference / Programmable Logic / Zybo Z7

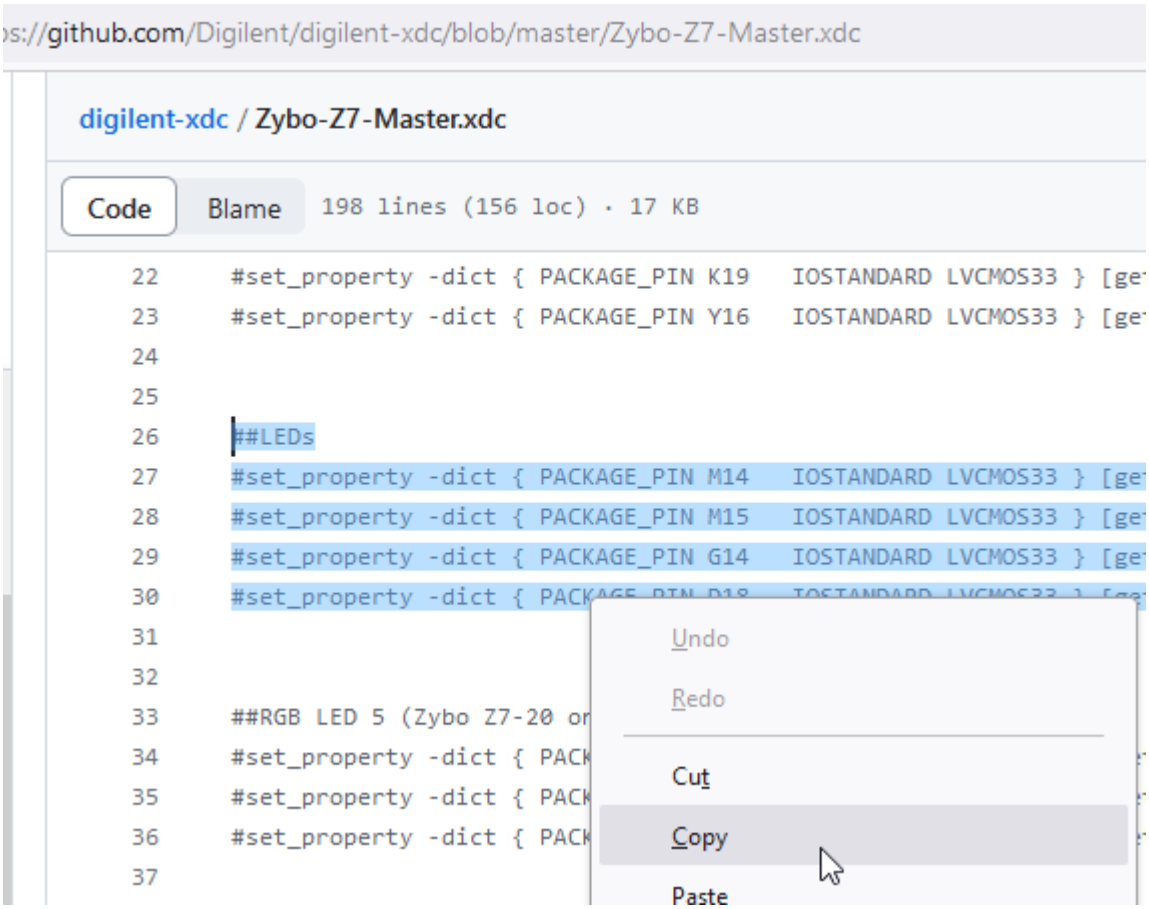
Zybo Z7

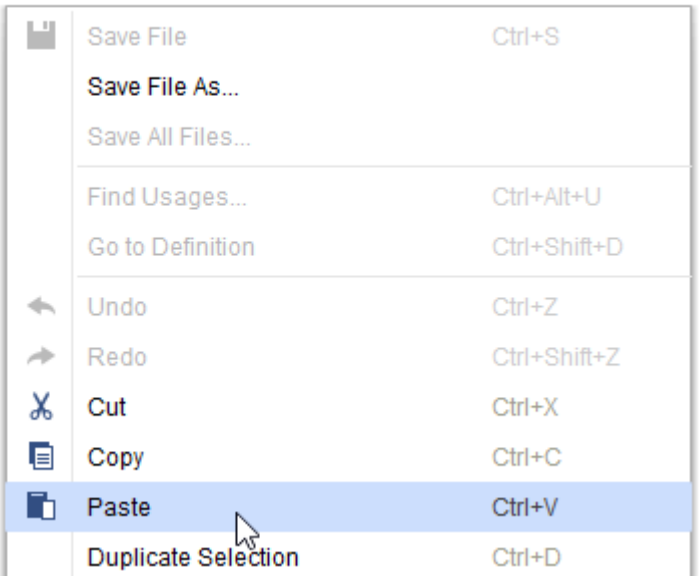
The Zybo Z7 is a feature-rich, ready-to-use embedded software and digital circuit development board built around the Xilinx Zynq-7000 family. The Zynq family is based on the Xilinx All

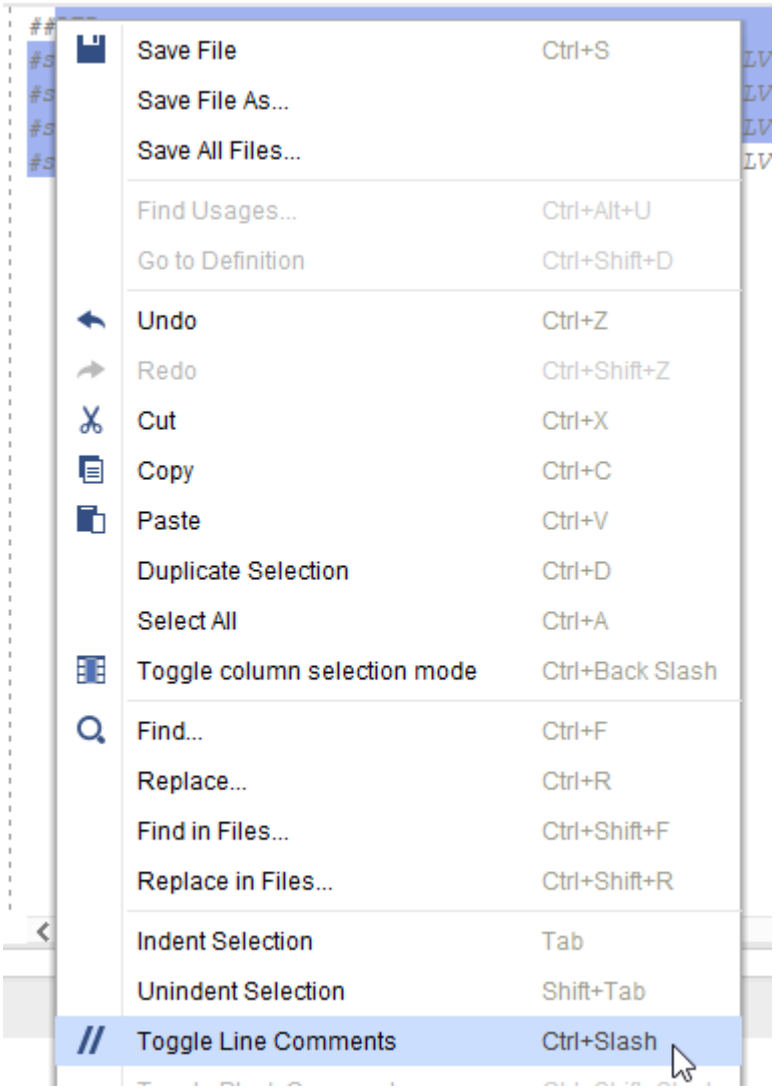
Documentation

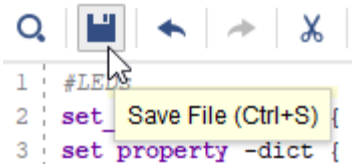
- Zybo Z7 Reference Manual
- Xilinx Zynq Datasheet
- Xilinx Zynq Technical Reference Manual
- Master XDC Files
- Petalinux Support for Digilent Boards
- reVISION Platforms

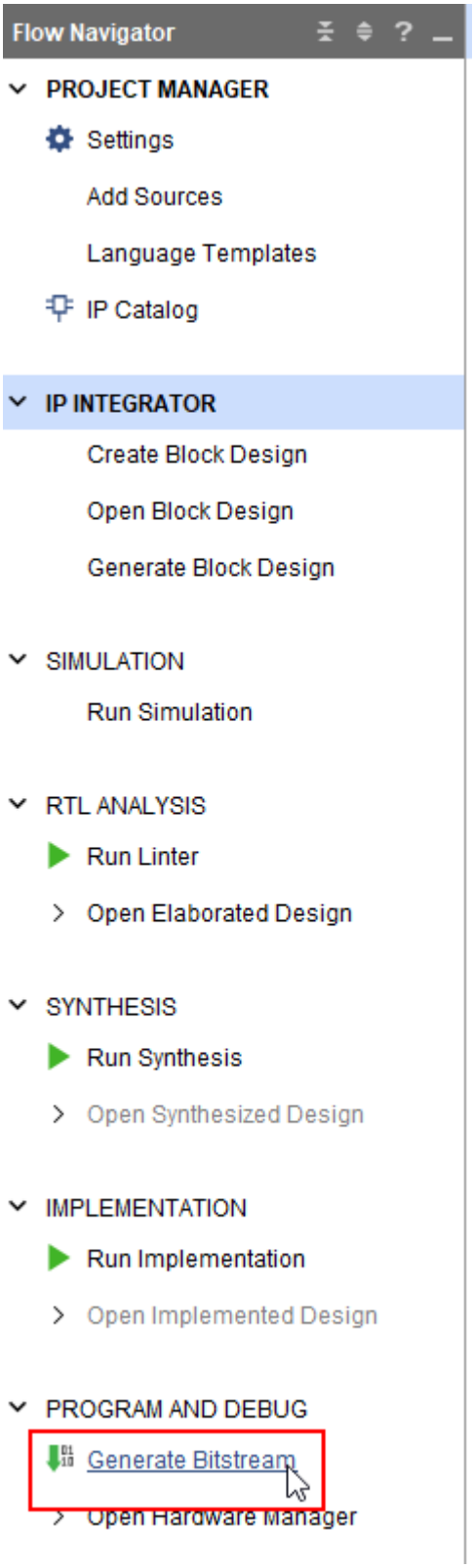

https://github.com/Digilent/digilent-xdc/
License.txt
Nexys-4-DDR-Master.xdc
Nexys-4-Master.xdc
Nexys-A7-100T-Master.xdc
Nexys-A7-50T-Master.xdc
Nexys-Video-Master.xdc
README.md
Sword-Master.xdc
USB104-A7-100T-Master.xdc
Zedboard-Master.xdc
Zybo-Master.xdc
Zybo-Z7-Master.xdc

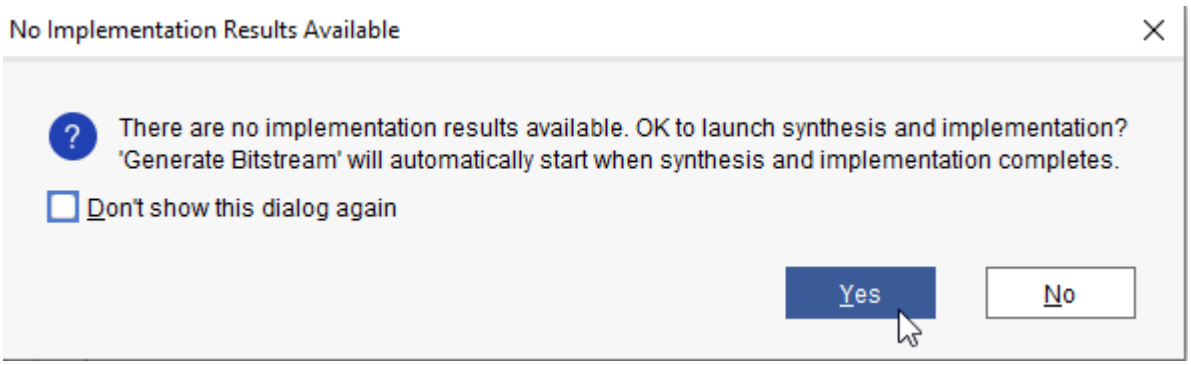

https://github.com/Digilent/digilent-xdc/blob/master/Zybo-Z7-Master.xdc
digilent-xdc / Zybo-Z7-Master.xdc
Code
Blame
198 lines (156 loc) · 17 KB
22 #set_property -dict { PACKAGE_PIN K19 IOSTANDARD LVCMOS33 } [ge
23 #set_property -dict { PACKAGE_PIN Y16 IOSTANDARD LVCMOS33 } [ge
24
25
26 ##LEDs
27 #set_property -dict { PACKAGE_PIN M14 IOSTANDARD LVCMOS33 } [ge
28 #set_property -dict { PACKAGE_PIN M15 IOSTANDARD LVCMOS33 } [ge
29 #set_property -dict { PACKAGE_PIN G14 IOSTANDARD LVCMOS33 } [ge
30 #set_property -dict { PACK
31
32
33 ##RGB LED 5 (Zybo Z7-20 or
34 #set_property -dict { PACK
35 #set_property -dict { PACK
36 #set_property -dict { PACK
37
Undo
Redo
Cut
Copy
Paste

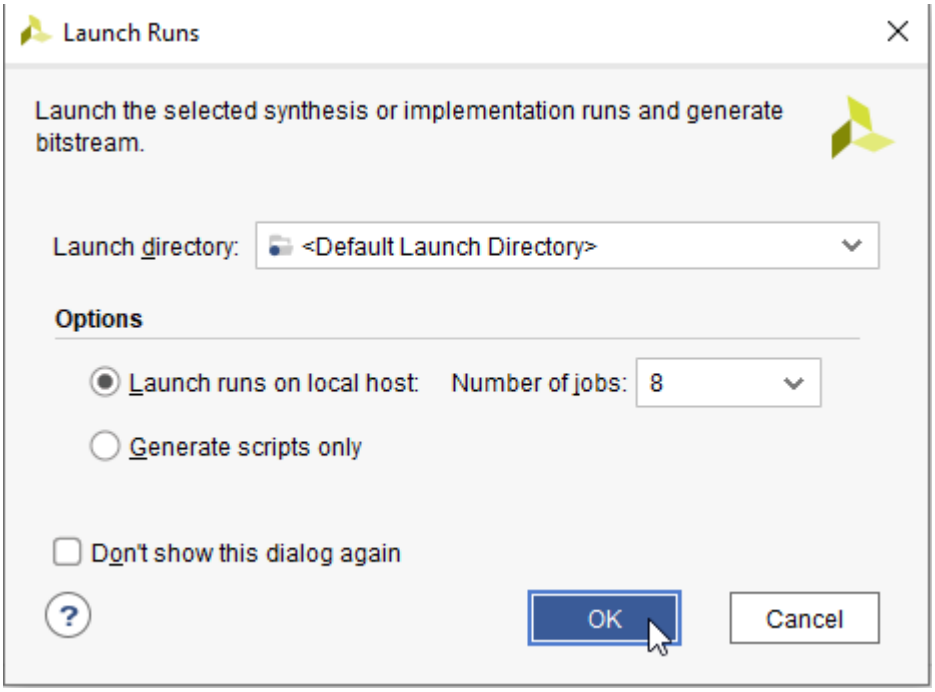

Save File Ctrl+S
Save File As...
Save All Files...
Find Usages... Ctrl+Alt+U
Go to Definition Ctrl+Shift+D
Undo Ctrl+Z
Redo Ctrl+Shift+Z
Cut Ctrl+X
Copy Ctrl+C
Paste Ctrl+V
Duplicate Selection Ctrl+D

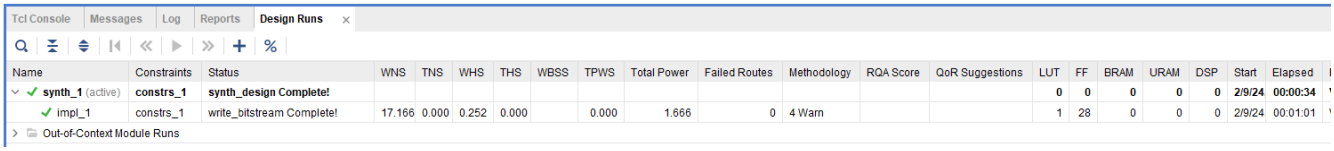

Save File Ctrl+S
Save File As...
Save All Files...
Find Usages... Ctrl+Alt+U
Go to Definition Ctrl+Shift+D
Undo Ctrl+Z
Redo Ctrl+Shift+Z
Cut Ctrl+X
Copy Ctrl+C
Paste Ctrl+V
Duplicate Selection Ctrl+D
Select All Ctrl+A
Toggle column selection mode Ctrl+Back Slash
Find... Ctrl+F
Replace... Ctrl+R
Find in Files... Ctrl+Shift+F
Replace in Files... Ctrl+Shift+R
Indent Selection Tab
Unindent Selection Shift+Tab
Toggle Line Comments Ctrl+Slash

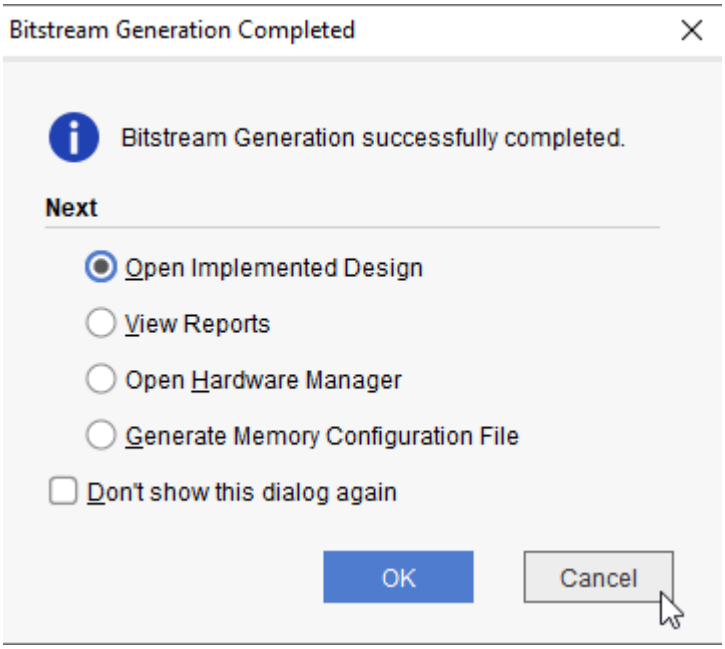

Save File (Ctrl+S)
#LEDS
set_
set property -dict {


Flow Navigator
PROJECT MANAGER
Settings
Add Sources
Language Templates
IP Catalog
IP INTEGRATOR
Create Block Design
Open Block Design
Generate Block Design
SIMULATION
Run Simulation
RTL ANALYSIS
Run Linter
Open Elaborated Design
SYNTHESIS
Run Synthesis
Open Synthesized Design
IMPLEMENTATION
Run Implementation
Open Implemented Design
PROGRAM AND DEBUG
Generate Bitstream
Open Hardware Manager

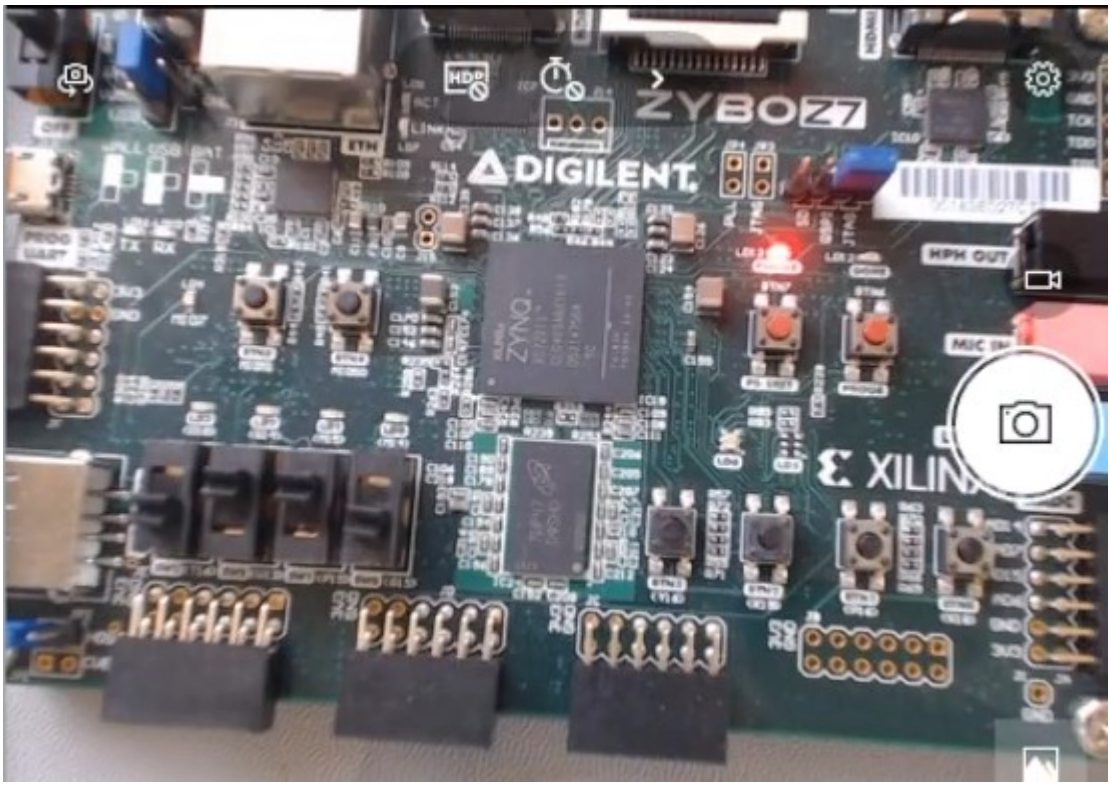

No Implementation Results Available
There are no implementation results available. OK to launch synthesis and implementation?
'Generate Bitstream' will automatically start when synthesis and implementation completes.
Don't show this dialog again
Yes
No

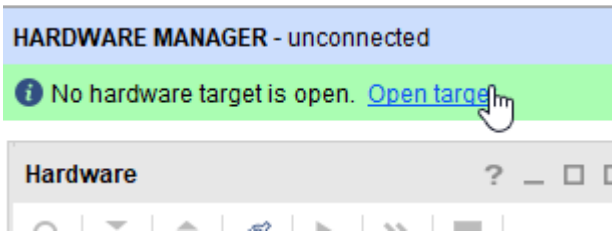

Launch Runs
Launch the selected synthesis or implementation runs and generate bitstream.
Launch directory:
<Default Launch Directory>
Options
Launch runs on local host:
Number of jobs:
8
Generate scripts only
Don't show this dialog again
OK
Cancel

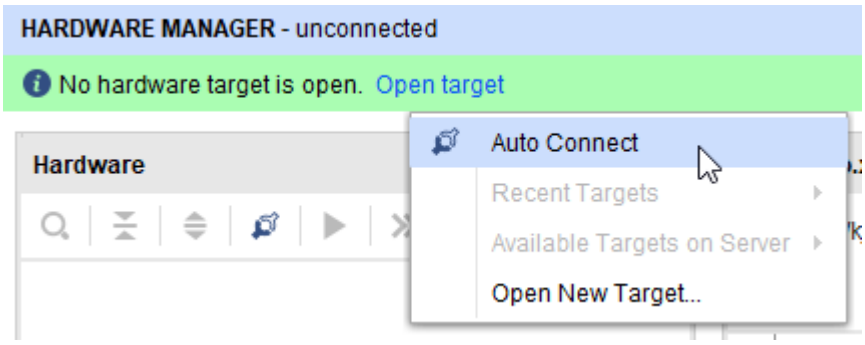

Tcl Console
Messages
Log
Reports
Design Runs
Name
Constraints
Status
WNS
TNS
WHS
THS
WBSS
TPWS
Total Power
Failed Routes
Methodology
RQA Score
QoR Suggestions
LUT
FF
BRAM
URAM
DSP
Start
Elapsed
synth_1 (active)
constrs_1
synth_design Complete!
2/9/24
00:00:34
impl_1
constrs_1
write_bitstream Complete!
17.166
0.000
0.252
0.000
0.000
1.666
0
4 Warn
1
28
2/9/24
00:01:01
Out-of-Context Module Runs

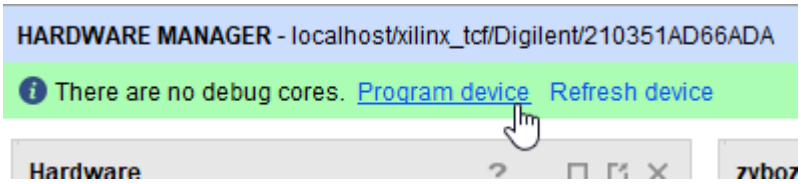

Bitstream Generation Completed
Bitstream Generation successfully completed.
Next
Open Implemented Design
View Reports
Open Hardware Manager
Generate Memory Configuration File
Don't show this dialog again
OK
Cancel

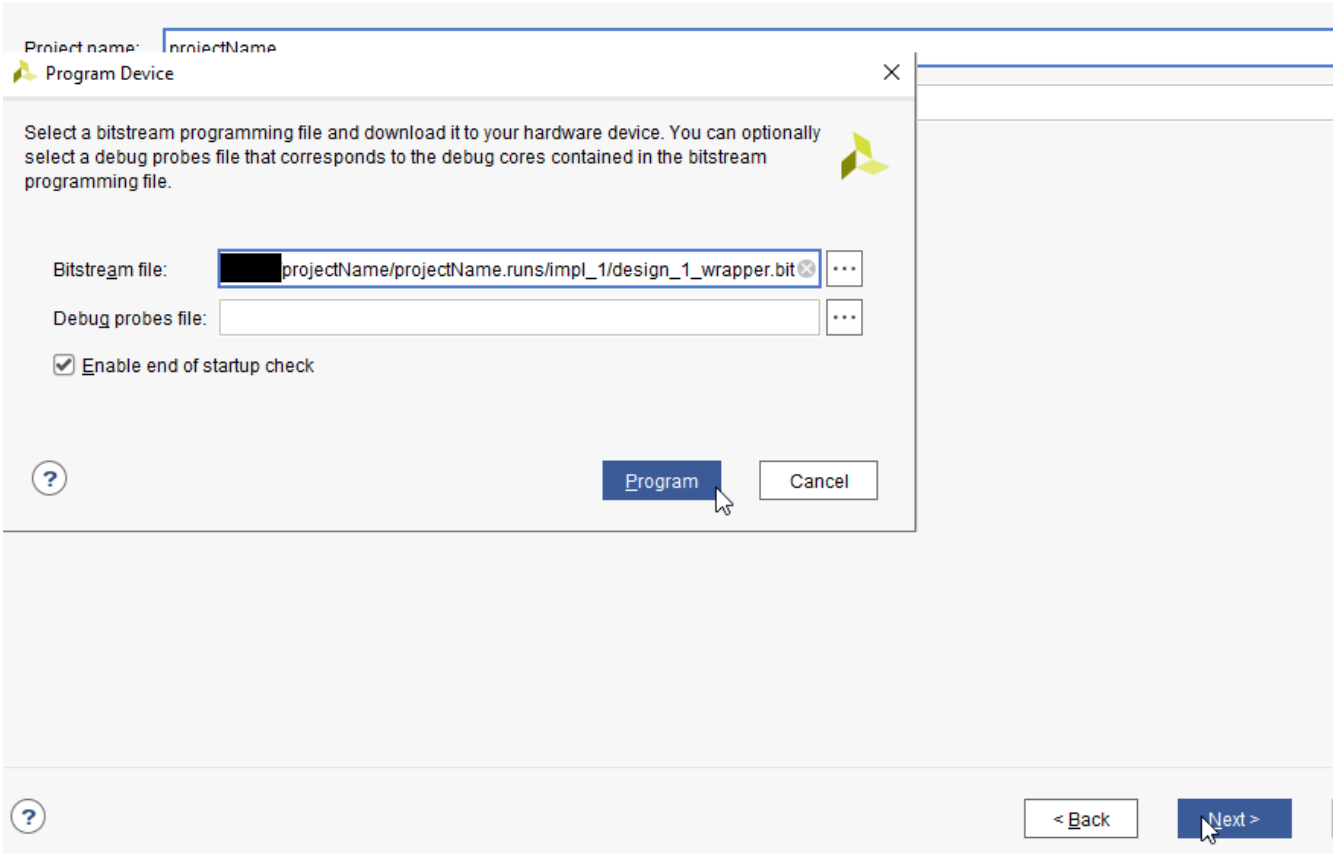

PROGRAM AND DEBUG
Generate Bitstream
Open Hardware Manager

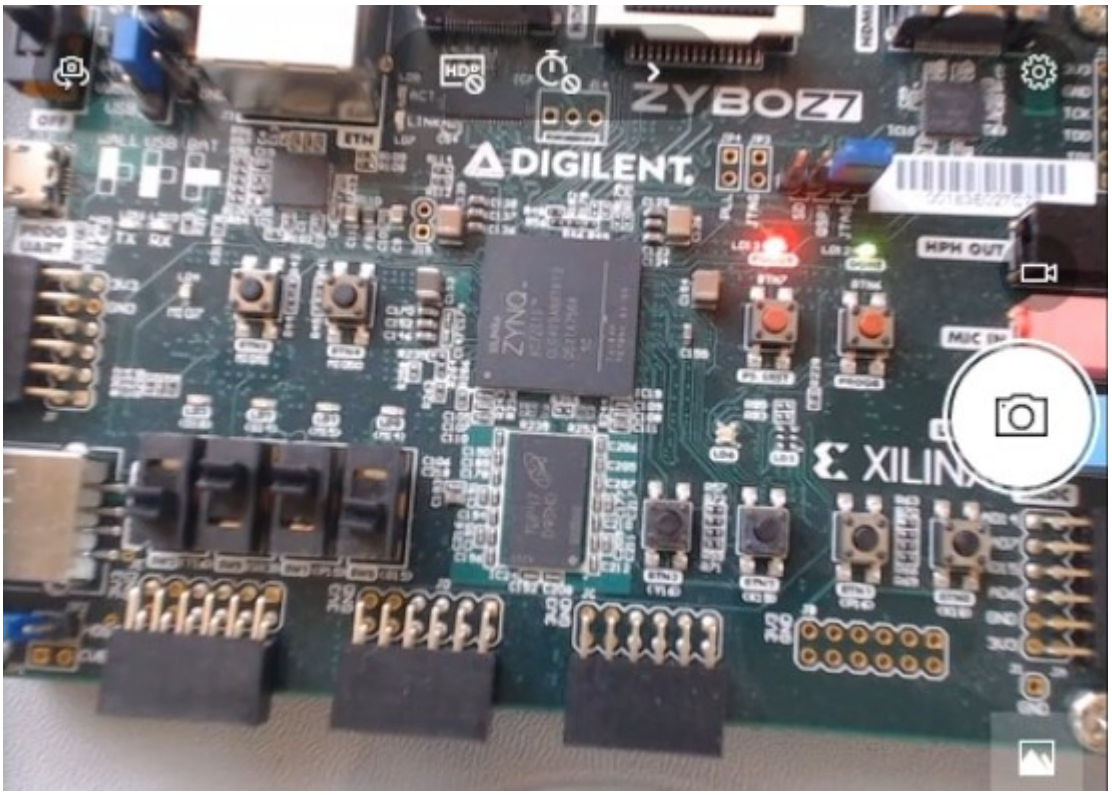

ZYBO Z7
DIGILENT

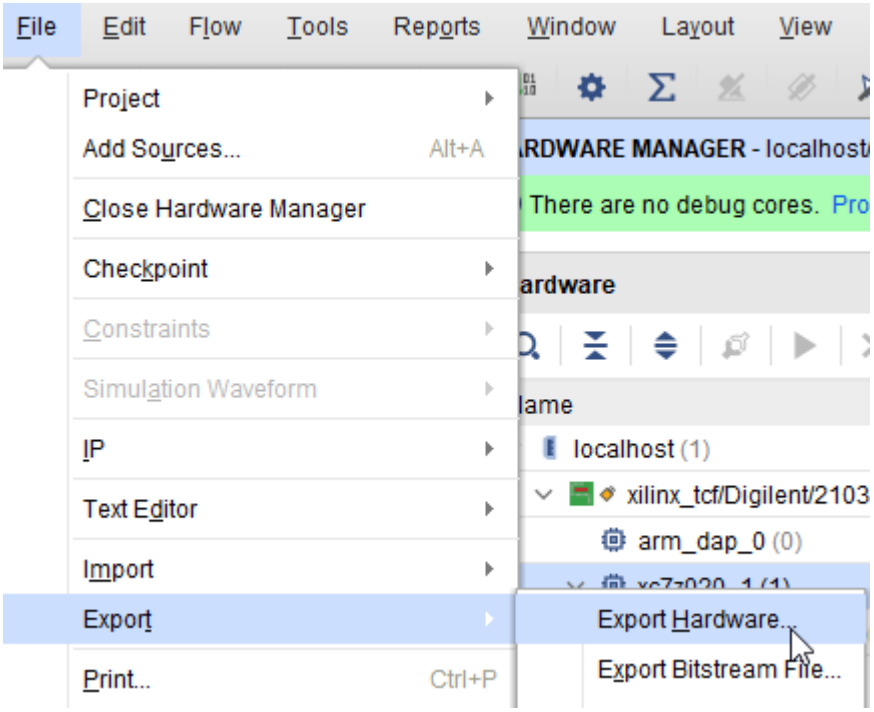

HARDWARE MANAGER - unconnected
No hardware target is open. Open target
Hardware


HARDWARE MANAGER - unconnected
No hardware target is open. Open target
Hardware
Auto Connect
Recent Targets
Available Targets on Server
Open New Target...


HARDWARE MANAGER - localhost/xilinx_tcf/Digilent/210351AD66ADA
There are no debug cores. Program device Refresh device
Hardware


Project name:
projectName
Program Device
Select a bitstream programming file and download it to your hardware device. You can optionally select a debug probes file that corresponds to the debug cores contained in the bitstream programming file.
Bitstream file:
projectName/projectName.runs/impl_1/design_1_wrapper.bit
Debug probes file:
Enable end of startup check
Program
Cancel
< Back
Next >


ZYBO Z7
DIGILENT
XILINX


File
Edit
Flow
Tools
Reports
Window
Layout
View
Project
Add Sources... Alt+A
Close Hardware Manager
Checkpoint
Constraints
Simulation Waveform
IP
Text Editor
Import
Export
Print... Ctrl+P
RDWARE MANAGER - localhost
There are no debug cores. Pro
ardware
lame
localhost (1)
xilinx_tcf/Digilent/2103
arm_dap_0 (0)
Export Hardware...
Export Bitstream File...

Output

Set the platform properties to inform downstream tools of the intended use of the target platform's hardwar

- ○ Pre-synthesis
  This platform includes a hardware specification for downstream software tools.
- ◉ Include bitstream
  This platform includes the complete hardware implementation and bitstream, in addition to the hard
  software tools.

< Back | Next > |

Files

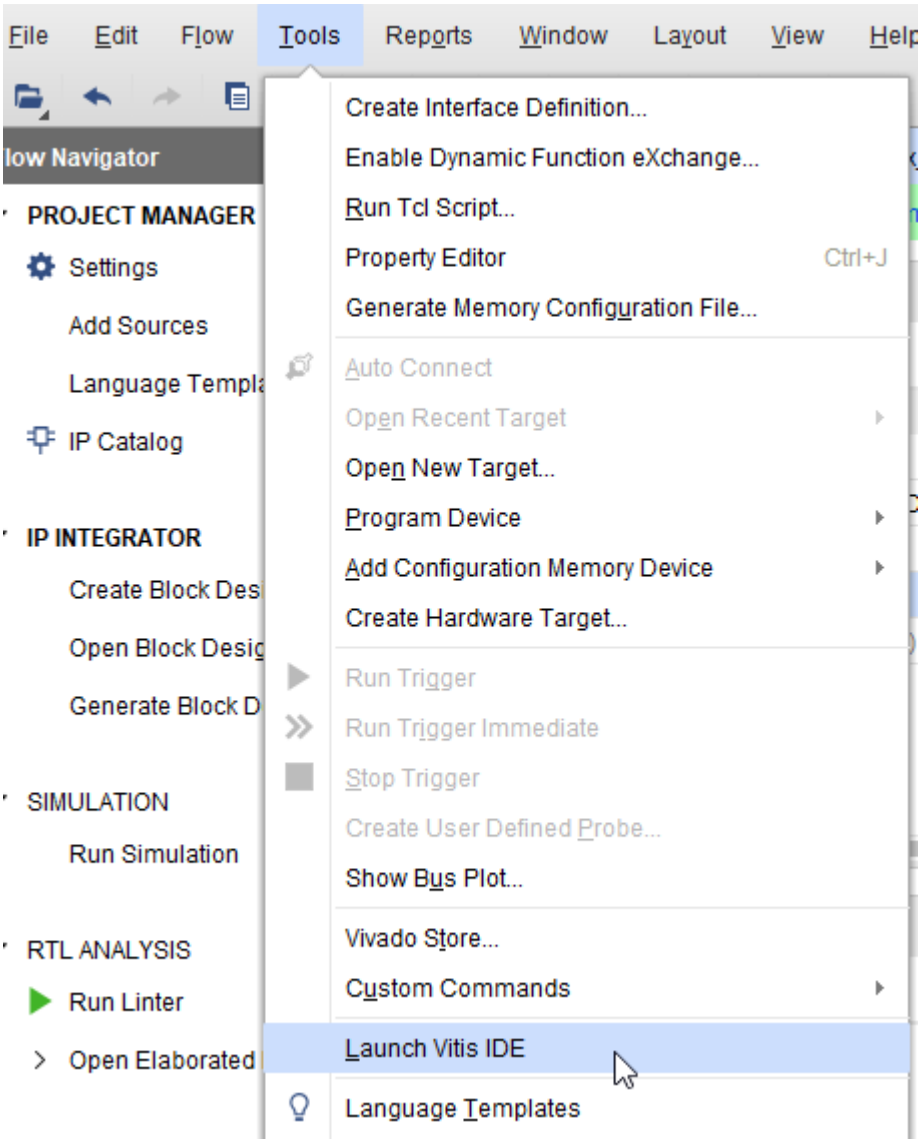
Enter the name of your hardware platform file, and the directory where the XSA file will be stored.

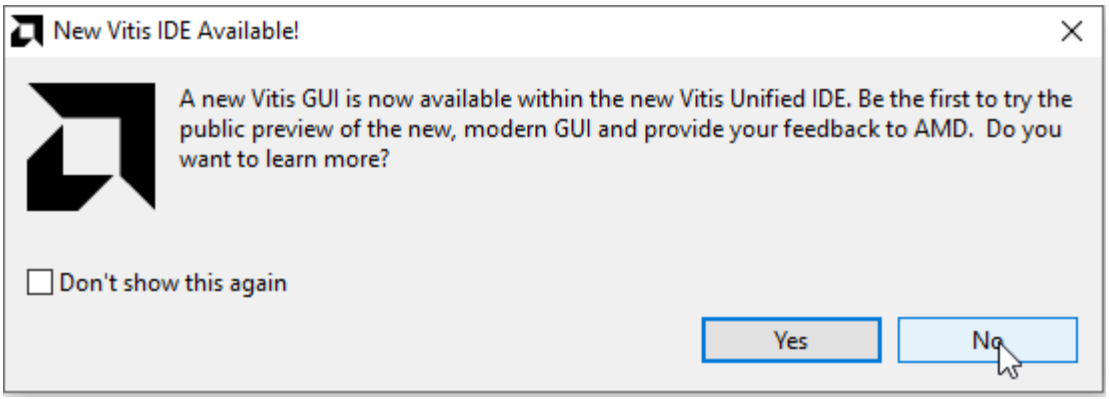
XSA file name: design_1_wrapper

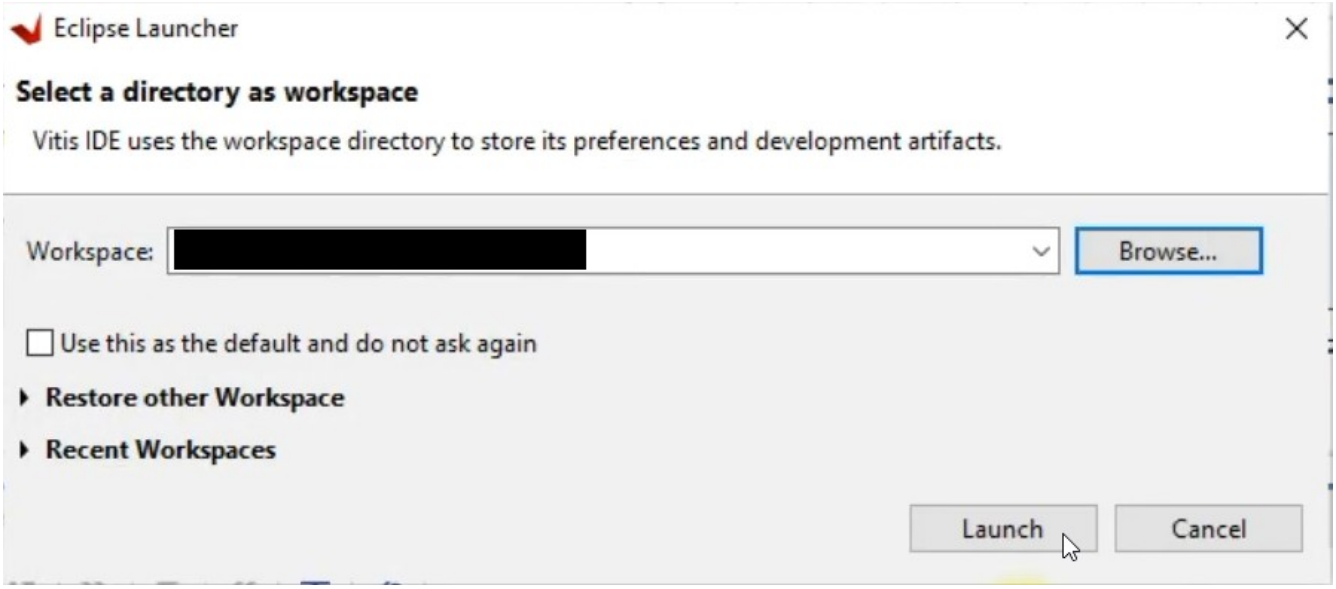
Export to: [redacted]projectName

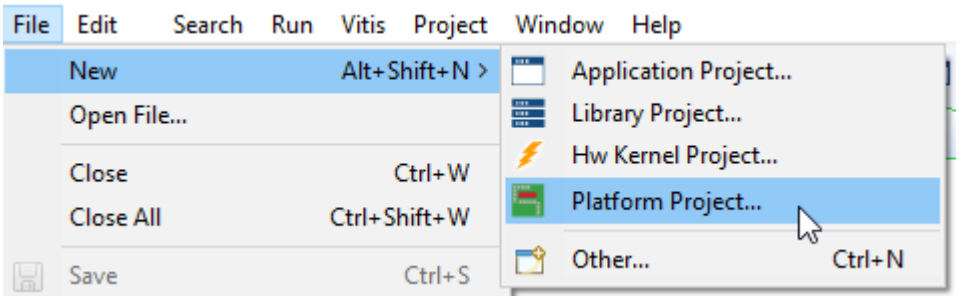
The XSA will be written to: [redacted]projectName\design_1_wrapper.xsa

< Back | Next > | Finish


File
Edit
Flow
Tools
Reports
Window
Layout
View
Help
low Navigator
PROJECT MANAGER
Settings
Add Sources
Language Templa
IP Catalog
IP INTEGRATOR
Create Block Des
Open Block Desig
Generate Block D
SIMULATION
Run Simulation
RTL ANALYSIS
Run Linter
Open Elaborated
Create Interface Definition...
Enable Dynamic Function eXchange...
Run Tcl Script...
Property Editor
Ctrl+J
Generate Memory Configuration File...
Auto Connect
Open Recent Target
Open New Target...
Program Device
Add Configuration Memory Device
Create Hardware Target...
Run Trigger
Run Trigger Immediate
Stop Trigger
Create User Defined Probe...
Show Bus Plot...
Vivado Store...
Custom Commands
Launch Vitis IDE
Language Templates


New Vitis IDE Available!
A new Vitis GUI is now available within the new Vitis Unified IDE. Be the first to try the public preview of the new, modern GUI and provide your feedback to AMD. Do you want to learn more?
Don't show this again
Yes
No


Eclipse Launcher
Select a directory as workspace
Vitis IDE uses the workspace directory to store its preferences and development artifacts.
Workspace:
Browse...
Use this as the default and do not ask again
Restore other Workspace
Recent Workspaces
Launch
Cancel

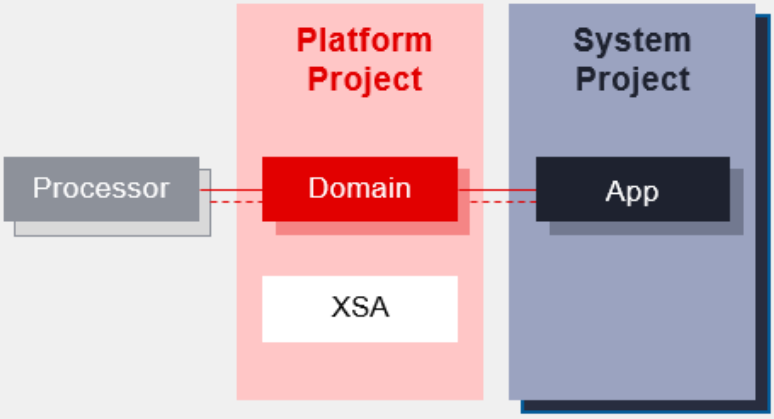

File
Edit
Search
Run
Vitis
Project
Window
Help
New
Alt+Shift+N
Open File...
Close
Ctrl+W
Close All
Ctrl+Shift+W
Save
Ctrl+S
Application Project...
Library Project...
Hw Kernel Project...
Platform Project...
Other...
Ctrl+N

Create new platform project

Enter a name for your platform project

This wizard will guide you through creation of a platform project from the output of Vivado [Xilinx Shell Archive (XSA)] or from an existing platf
you to specify options for the kernels, BSPs, as well as settings required for creating new applications. Platforms are currently supported for emb

Platform project name: project_name_platform



- A platform provides hardware information and so
- A system project contains one or more applicatio
- A domain provides runtime for applications, such
- A workspace can contain unlimited platforms and

A new platform project can be created from one of the two inputs:

From hardware specification (XSA)

Create a new platform project from a hardware specification file. You can specify the OS and processor to start with. The platform can be
platform project editor.

From existing platform

Load the platform definition from an existing platform. You can choose any platform from the platform repository as a base for your platf

< Back | Next >

Create a new platform from hardware (XSA) | Select a platform from repository

Hardware Specification

Provide your XSA file or use a pre-built board description

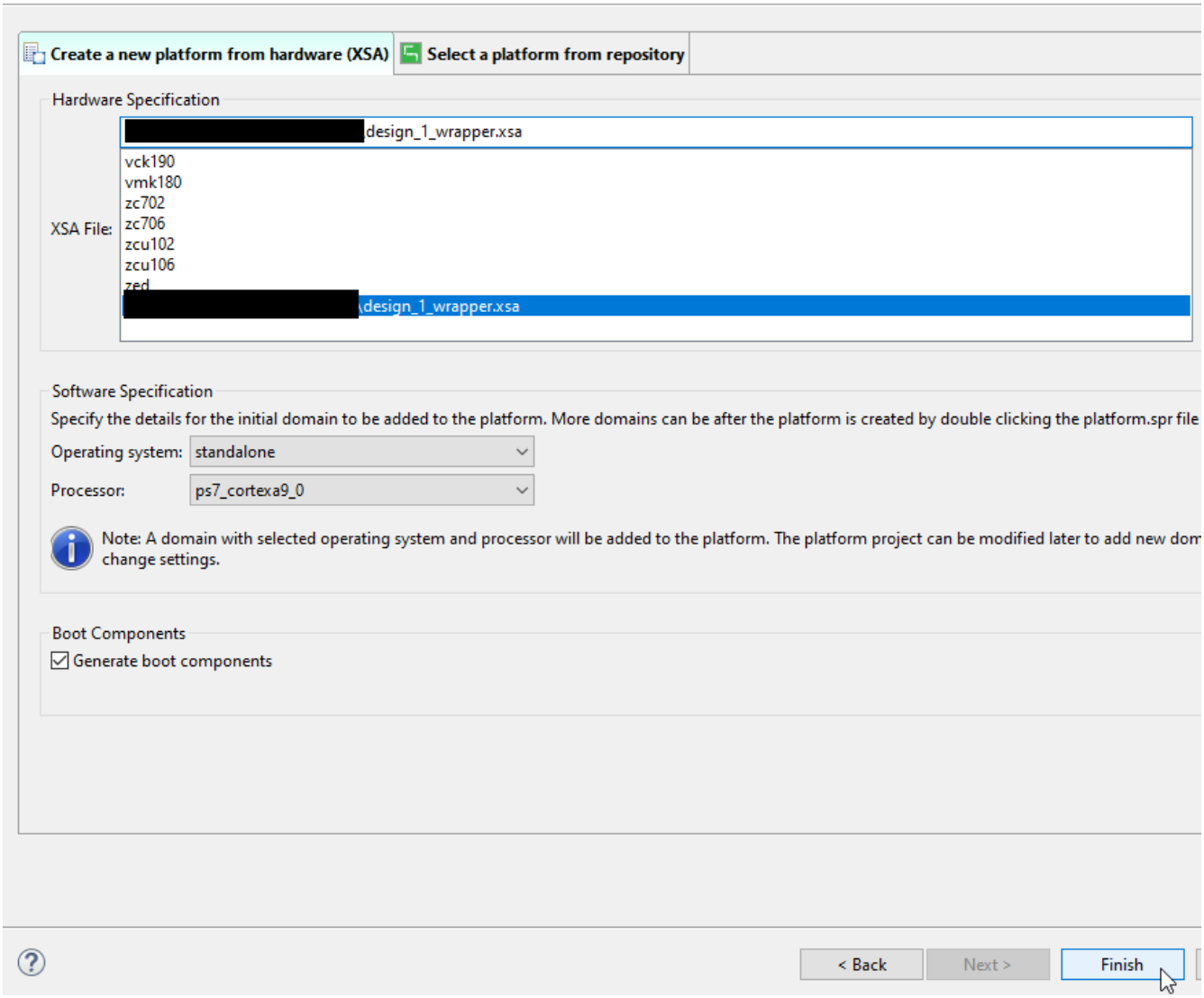
XSA File:

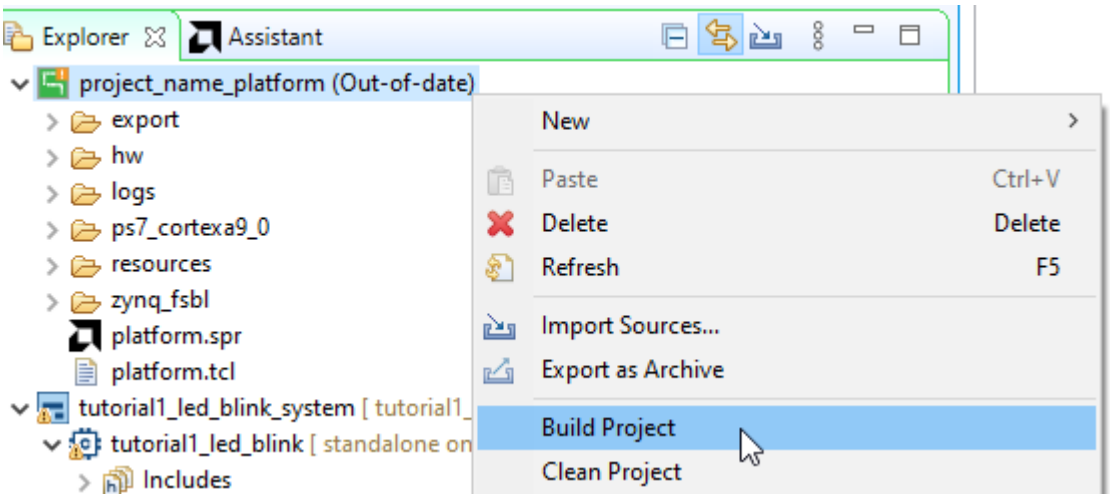
vck190
vmk180
zc702
zc706
zcu102

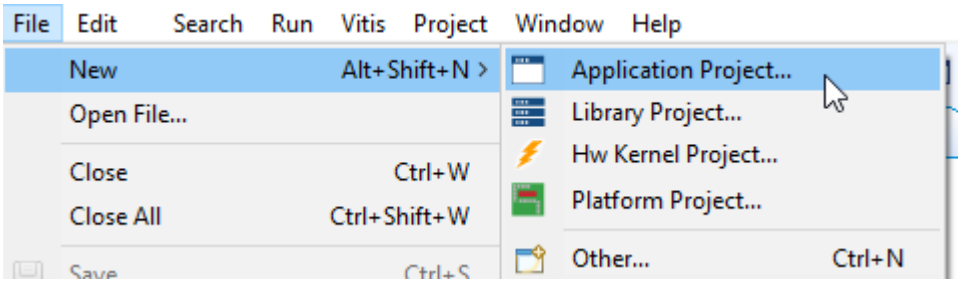
Browse...

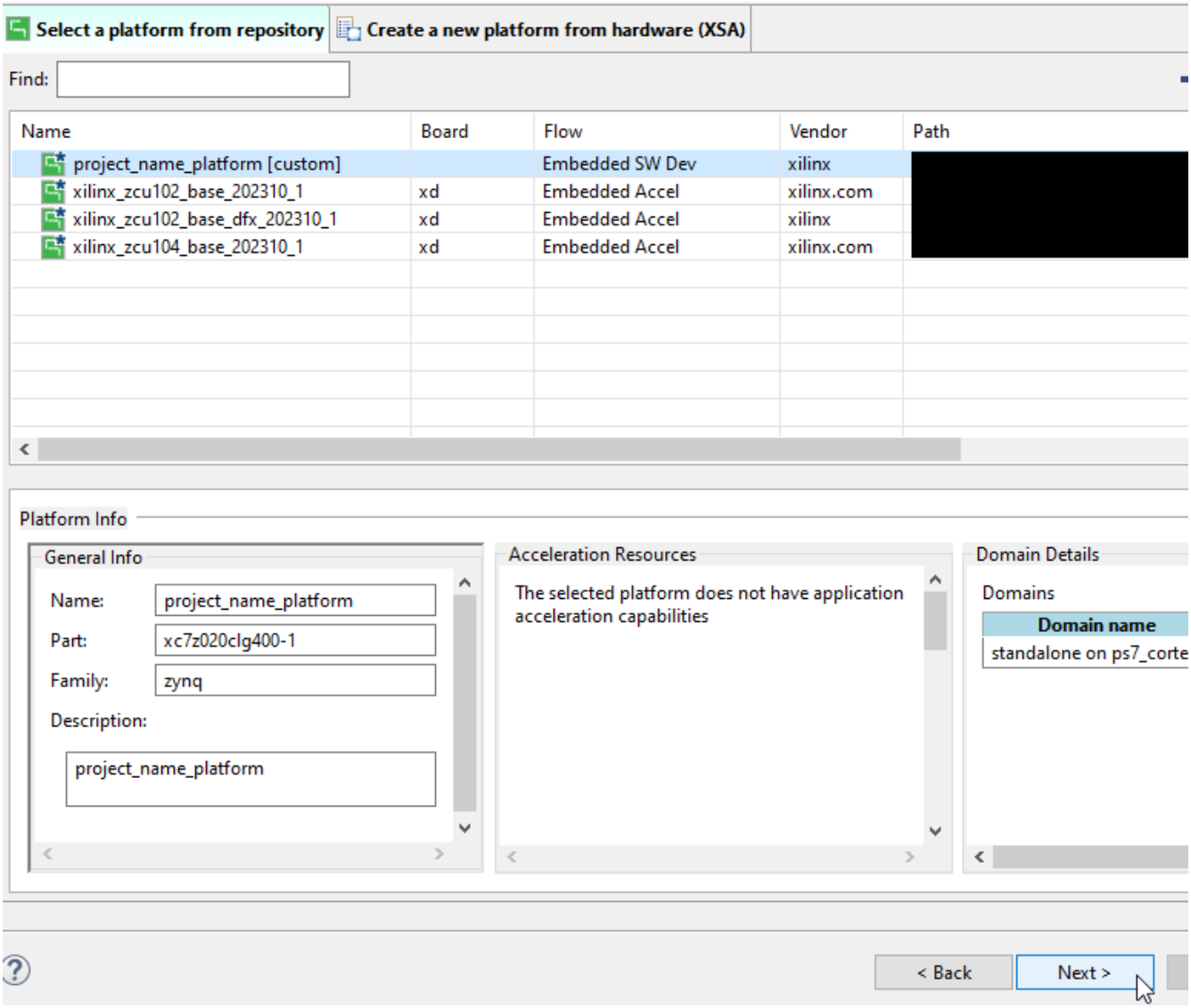
Platform

Choose a platform for your project. You can also create an application from XSA through the 'Create a new platform from hardware (XSA)' tab.



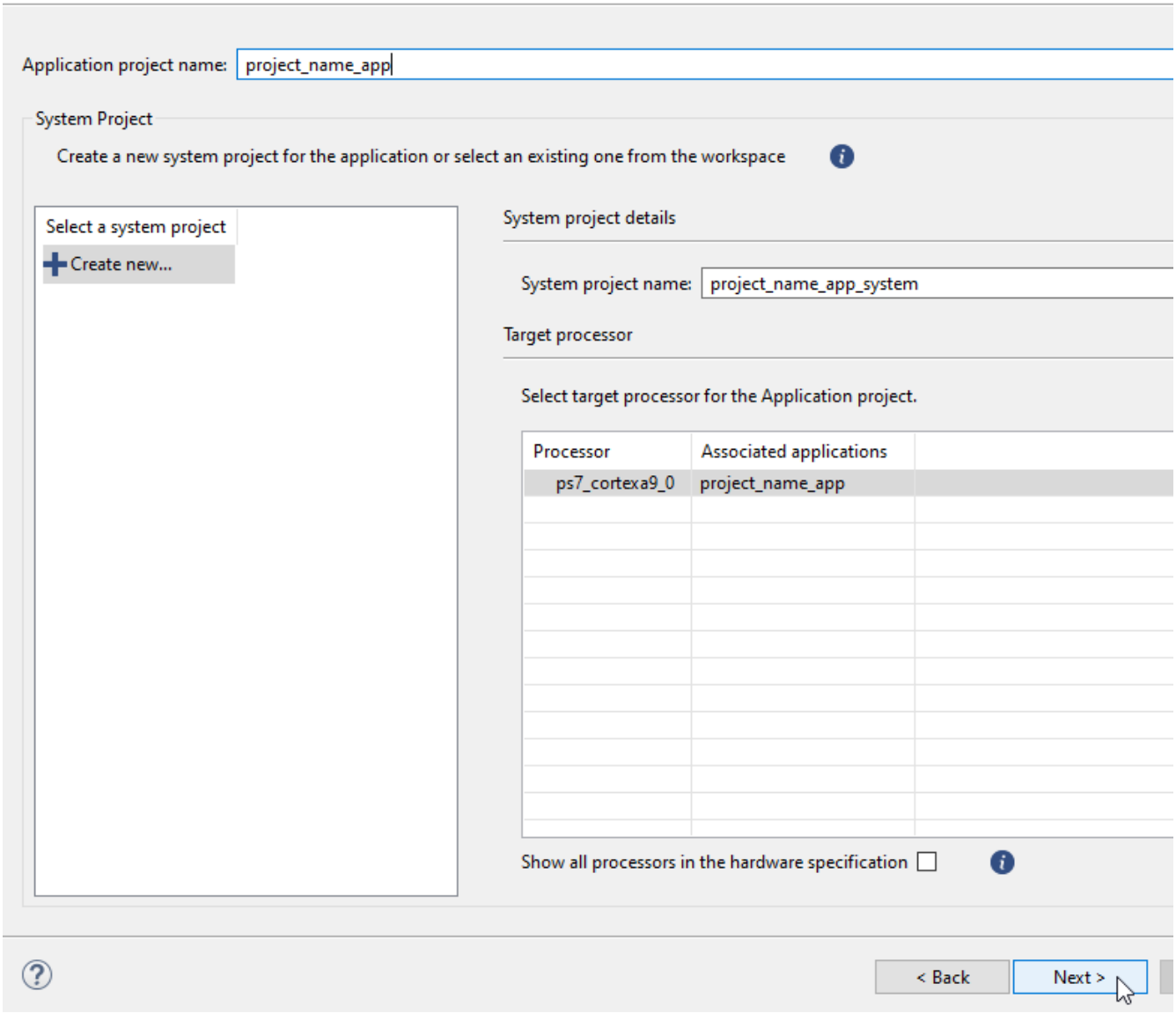



File
Edit
Search
Run
Vitis
Project
Window
Help
New
Alt+Shift+N >
Open File...
Close
Ctrl+W
Close All
Ctrl+Shift+W
Application Project...
Library Project...
Hw Kernel Project...
Platform Project...
Other...
Ctrl+N


Select a platform from repository
Create a new platform from hardware (XSA)
Find:
Name
Board
Flow
Vendor
Path
project_name_platform [custom]
Embedded SW Dev
xilinx
xilinx_zcu102_base_202310_1
xd
Embedded Accel
xilinx.com
xilinx_zcu102_base_dfx_202310_1
xd
Embedded Accel
xilinx
xilinx_zcu104_base_202310_1
xd
Embedded Accel
xilinx.com
Platform Info
General Info
Name:
project_name_platform
Part:
xc7z020clg400-1
Family:
zynq
Description:
project_name_platform
Acceleration Resources
The selected platform does not have application acceleration capabilities
Domain Details
Domains
Domain name
standalone on ps7_corte
< Back
Next >

Application Project Details

Specify the application project name and its system project properties

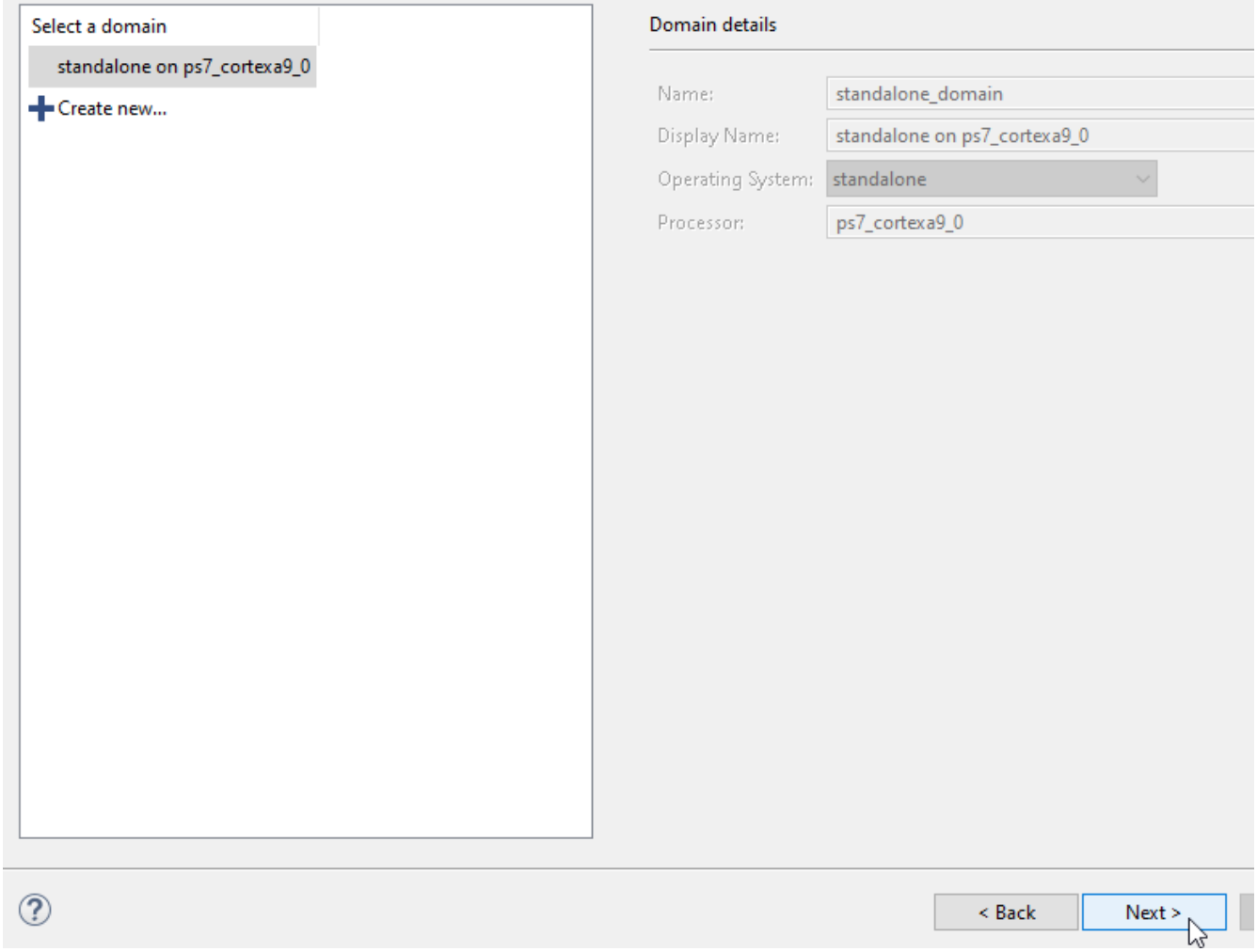


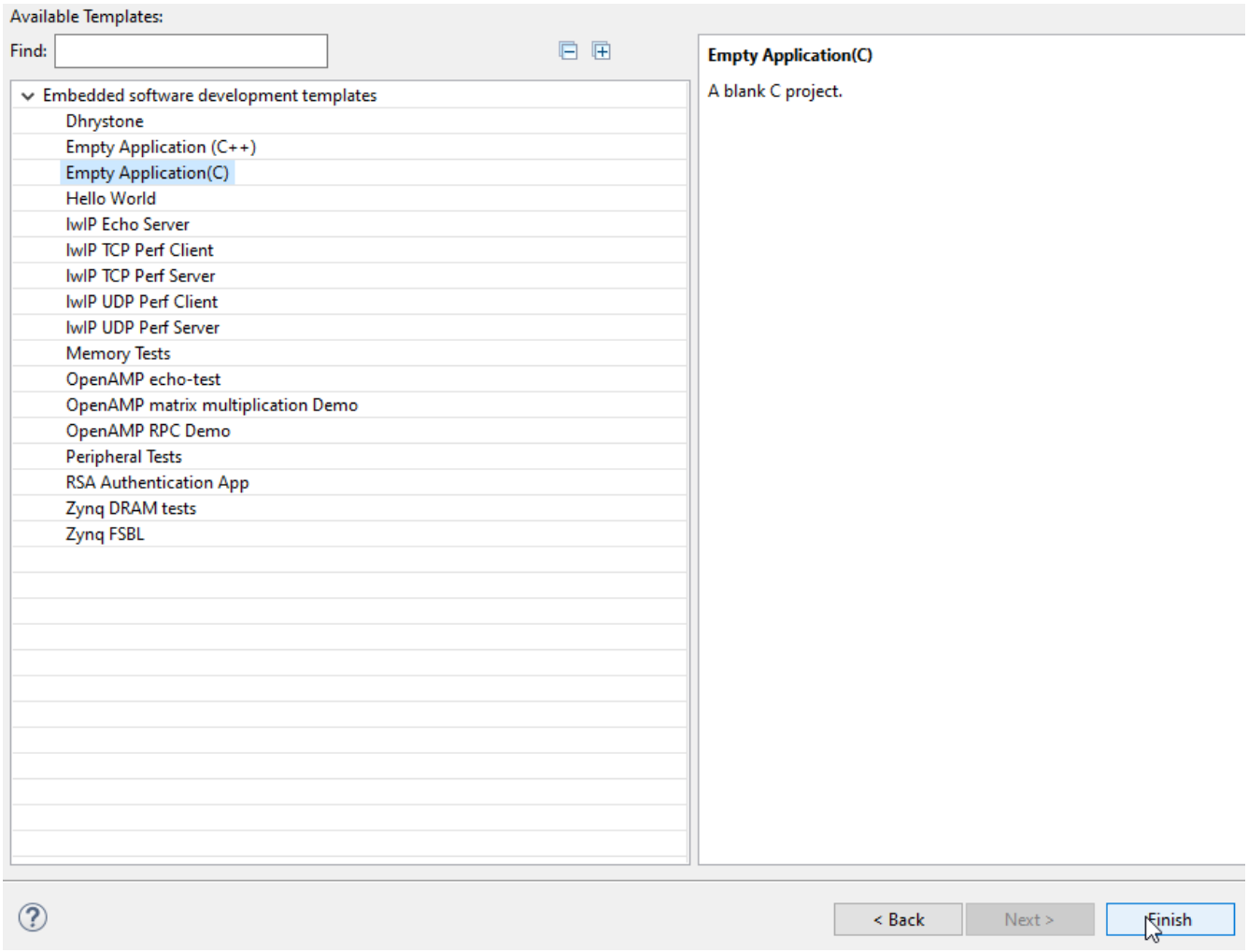
Domain

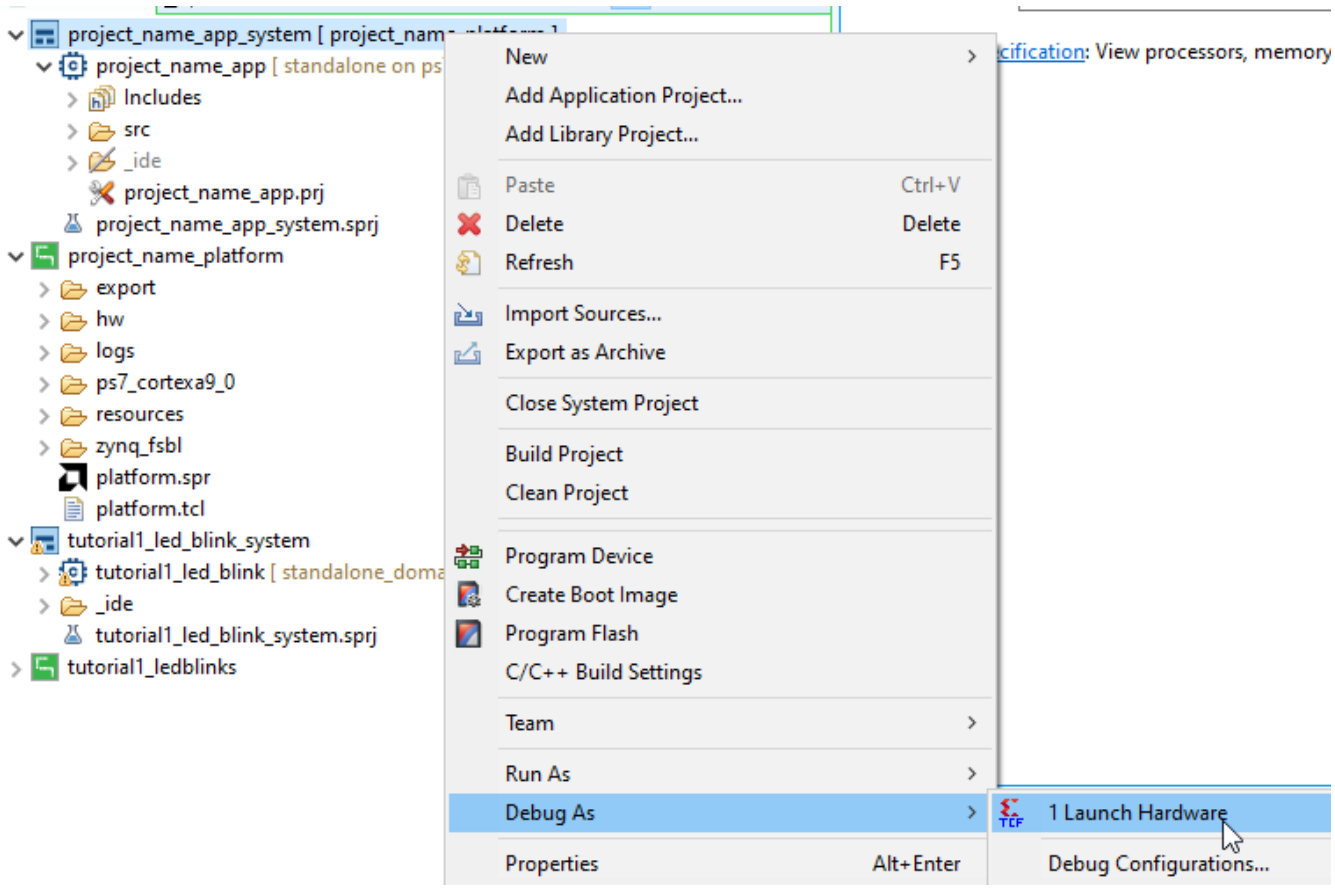
Select a domain for your project or create a new domain

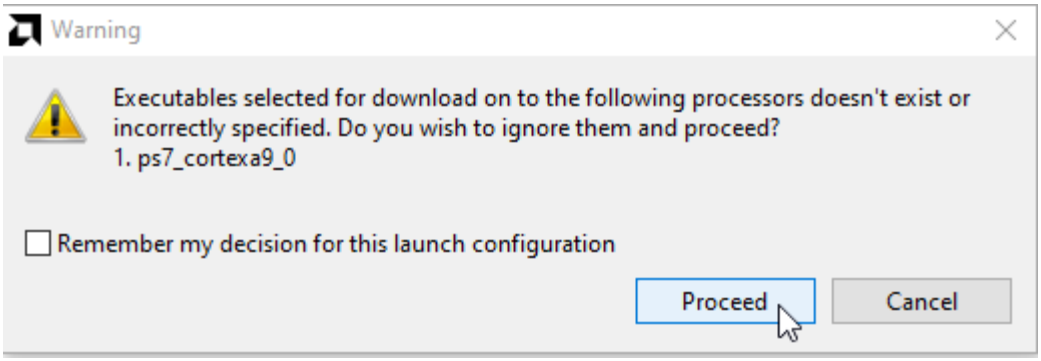
Select the domain that the application would link to or create a new domain

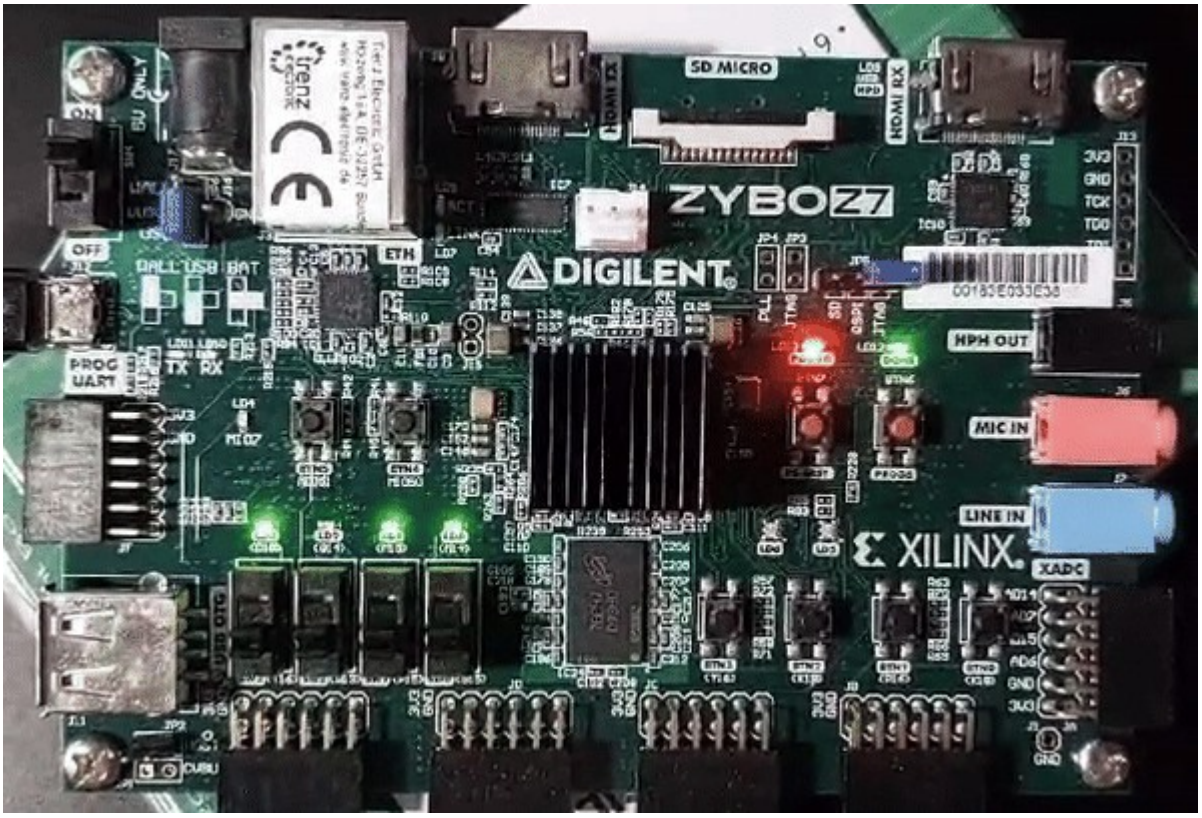
Note: New domain created by this wizard will have all the requirements of the application template selected in the next step




Available Templates:
Find:
Embedded software development templates
Dhrystone
Empty Application (C++)
Empty Application(C)
Hello World
lwIP Echo Server
lwIP TCP Perf Client
lwIP TCP Perf Server
lwIP UDP Perf Client
lwIP UDP Perf Server
Memory Tests
OpenAMP echo-test
OpenAMP matrix multiplication Demo
OpenAMP RPC Demo
Peripheral Tests
RSA Authentication App
Zynq DRAM tests
Zynq FSBL
Empty Application(C)
A blank C project.
< Back
Next >
Finish


project_name_app_system [project_nam
project_name_app [standalone on ps
Includes
src
_ide
project_name_app.prj
project_name_app_system.sprj
project_name_platform
export
hw
logs
ps7_cortexa9_0
resources
zynq_fsbl
platform.spr
platform.tcl
tutorial1_led_blink_system
tutorial1_led_blink [standalone_doma
_ide
tutorial1_led_blink_system.sprj
tutorial1_ledblinks
cification: View processors, memory
New
Add Application Project...
Add Library Project...
Paste Ctrl+V
Delete Delete
Refresh F5
Import Sources...
Export as Archive
Close System Project
Build Project
Clean Project
Program Device
Create Boot Image
Program Flash
C/C++ Build Settings
Team
Run As
Debug As
Properties Alt+Enter
1 Launch Hardware
Debug Configurations...


Warning
Executables selected for download on to the following processors doesn't exist or incorrectly specified. Do you wish to ignore them and proceed?
1. ps7_cortexa9_0
Remember my decision for this launch configuration
Proceed
Cancel


SD MICRO
HDMI TX
HDMI RX
ZYBO Z7
DIGILENT
ETH
OTG
USB
BAT
OFF
ON
PROG UART
TX RX
HPH OUT
MIC IN
LINE IN
XILINX
XADC
3V3
GND
TCK
TDO