Energy-Efficient Low-Latency 600 MHz FIR With High-Overdrive Charge-Recovery Logic

Jerry C. Kao, *Student Member, IEEE*, Wei-Hsiang Ma, *Student Member, IEEE*, Visvesh S. Sathe, *Member, IEEE*, and Marios Papaefthymiou, *Senior Member, IEEE*

***Abstract*—This paper presents a 14-tap 8-bit finite impulse response (FIR) test-chip that has been designed using a novel charge-recovery logic family, called Enhanced Boost Logic (EBL), to achieve high-speed and low-power operation. Compared to previous charge-recovery circuitry, EBL achieves increased gate overdrive, resulting in low latency overhead over static CMOS design. The EBL-based FIR has been designed with only 1.5 cycles of additional latency over its static CMOS counterpart, while consuming 21% less energy per cycle, based on post-layout simulations of the two designs. The test-chip has been fabricated in a 0.13 μm CMOS process with a fully-integrated 3 nH inductor. Correct function has been validated in the 365–600 MHz range. At its resonant frequency of 466 MHz, the test-chip dissipates 39.1 mW with a 93.6 nW/MHz/Tap/InBit/CoeffBit figure of merit, recovering 45% of the energy supplied to it every cycle.**

***Index Terms*—Digital signal processing (DSP), low-power VLSI.**

I. Introduction

CHARGE-RECOVERY circuitry has the potential to reduce dynamic power consumption in digital systems with significant switching activity. To keep energy consumption to a minimum, charge-recovery circuitry is typically designed so that it maintains low voltage drops across device channels, while recovering the charge supplied to it every clock cycle. The overall energy-efficiency of charge-recovery circuitry therefore depends on the rate at which transitions occur, yielding an inverse relationship between energy consumption and clock period [1]. Relying on this energy/latency tradeoff, charge-recovery circuitry can operate with energy consumption below CV^2, the fundamental limit of static CMOS.

Early research on charge-recovery logic design focused on micropipelined dynamic circuits with multiple (four or more) clock phases for recovering charge [2]–[4]. These clock phases were generated by resonating the parasitic capacitance C of the circuitry through the introduction of inductors. To maximize the efficiency of recovery, the inductors were chosen so that the resulting LC tank system resonates at the target clock frequency. In these early multiphase designs, the resulting complexity of the recovery mechanisms was considerable, especially in the case of the so-called reversible designs [5], which theoretically offer the greatest energy saving potential. Moreover, the synchronization of multiple clock phases was impeding high-speed operation.

Aimed at reducing control overheads and increasing operating speeds, several single-phase and two-phase charge-recovery families were proposed [6]–[9]. Such micropipelined logic did achieve clock frequencies comparable with static CMOS [10], [11], but it also resulted in increased latencies, due to the reduction in the number of clock phases and, therefore, in the number of logic functions performed each clock cycle. It thus made the energy/latency tradeoff of charge-recovery circuitry more manifest at the architectural level.

In recent years, a charge-recovery family that uses multiple power supply levels, called Boost Logic, was demonstrated in silicon at clock speeds exceeding 1 GHz [12], [13]. Although micropipelined using a two-phase clocking scheme, Boost Logic improves upon the energy/latency tradeoff of previous charge-recovery circuit families, as it relies on gate overdrive to evaluate logic functions with significantly decreased delay and with minimal short-circuit current. It thus has the potential to achieve high-speed and low-power operation with pipeline latencies that are comparable to those of static CMOS designs.

This paper introduces Enhanced Boost Logic (EBL), an improved version of the basic Boost Logic that achieves shorter pipeline latencies while retaining its energy advantages over static CMOS. Similar to Boost Logic, EBL is capable of operation at high clock frequencies by developing a near-threshold voltage before the onset of the power clock. Evaluation devices in EBL have twice the gate overdrive compared to first-generation Boost Logic [12], [13], however, enabling the design of complex logic gates and thus decreasing total gate counts. Consequently, EBL further improves upon the energy/latency tradeoff of Boost Logic, yielding lower latency while maintaining good energy efficiency. EBL improves upon Boost Logic also with respect to implementation complexity, as it requires a smaller number of power supplies.

The performance and energy efficiency of EBL have been assessed through the design and experimental evaluation of a 14-tap 8-bit FIR filter test-chip implemented in EBL. The latency of this EBL-based FIR is only 1.5 cycles longer than that of a similar-performance static CMOS design that has been implemented separately. Fabricated in a 0.13-μm CMOS process, the test-chip includes a fully-integrated 3 nH inductor and an integrated clock generator with frequency scaling capability. Correct operation has been experimentally validated

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The authors are with the Department of Electrical Engineering and Computer Science, University of Michigan, Ann Arbor, MI 48105 USA (e-mail: jckao@umich.edu).

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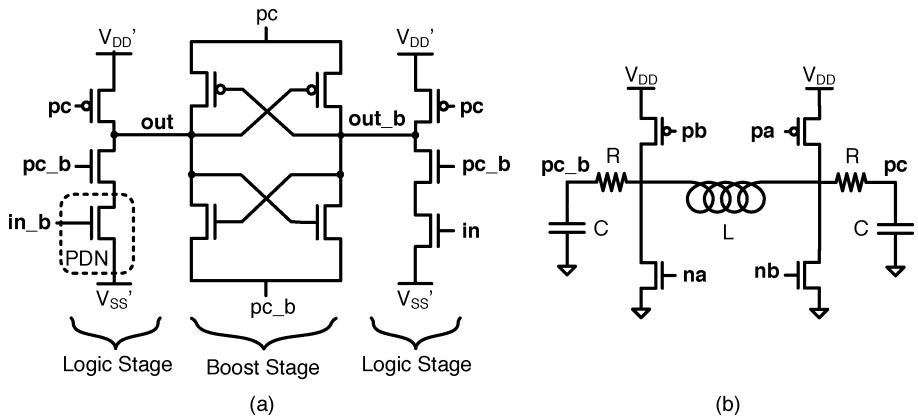

Fig. 1. Boost logic schematic.

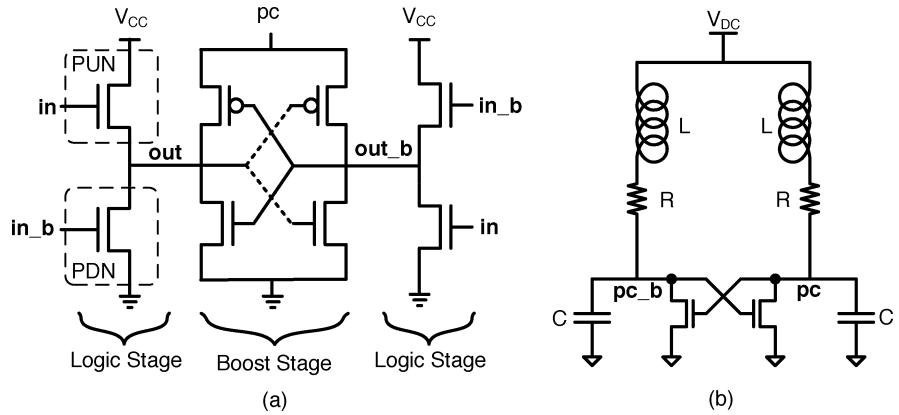

Fig. 2. SBL schematic.

across the 365–600 MHz range. When operating at its resonant frequency of 466 MHz, the FIR test-chip dissipates 39.1 mW and achieves 45% efficiency in the recovery of energy through its two clock phases. The associated figure of merit equals 93.6 nW/MHz/Tap/InBit/CoeffBit, a 29% improvement over previously-reported high-performance FIRs with sampling rates above 500 MHz [14], [15].

The remainder of this paper has six sections. In Section II, we present EBL and discuss its structure and operation. Section III provides an overview of the EBL-based FIR that we design using our semi-custom design methodology. Section IV describes a semi-custom design methodology that we developed for facilitating EBL-based circuit development. Section V gives results from Spice-level simulations of the EBL FIR filter and its static CMOS counterpart with identical architecture. In Section VI, we present measurement results from our EBL FIR filter test-chip. Conclusions are given in Section VII.

II. Enhanced Boost Logic

The origins of EBL can be traced back to Boost Logic, shown in Fig. 1(a). GHz-level operation has been demonstrated in silicon on a chain of simple Boost Logic gates powered by a two-phase clock [12], [13]. The original Boost Logic design uses four supply levels: $V_{\rm DD}$, $V'_{\rm DD}$, $V'_{\rm SS}$, and ground, where $V'_{\rm DD}$ and $V'_{\rm SS}$ are set at approximately $^2/_3V_{\rm DD}$ and $^1/_3V_{\rm DD}$, respectively. Powered by the aggressively-scaled voltage $V'_{\rm DD} - V'_{\rm SS}$, the Logic stage drives the dual-rail outputs conventionally with subthreshold-level energy consumption in the first half of each clock cycle. Subsequently, during the second half of each cycle, the Boost stage amplifies the near-threshold voltage between the two outputs to full rail using the two complementary clock phases pc and pc_b. These clock phases are generated using an H-bridge topology, as shown in Fig. 1(b). When Boost Logic gates are cascaded, the full-rail output from the Boost stage of one gate drives the Logic stage of the next gate, yielding operation in the super-linear region.

Fig. 2(a) shows Subthreshold Boost Logic (SBL), a variant of Boost Logic that is targeted at slower clock rates than Boost Logic. The energy-efficient and multi-MHz operation of SBL with a single subthreshold supply has been demonstrated in silicon [16], [17]. Similar to Boost Logic, SBL uses aggressive voltage scaling, using a subthreshold supply $V_{\rm CC}$ to power the dual-rail Logic stage. Unlike Boost Logic, however, the Logic stage has no clocked devices, and each of its two output rails is evaluated by a complementary all-nMOS stack. Another departure from Boost Logic is that the same subthreshold supply $V_{\rm CC}$ is used to power a "blip" clock generator, as shown in Fig. 2(b), producing two partially-overlapping clock waveforms pc and pc_b with peak values significantly greater than $V_{\rm CC}$. The Boost stage of each gate amplifies its output voltage to the full amplitude of the corresponding clock pc and drives the all-nMOS

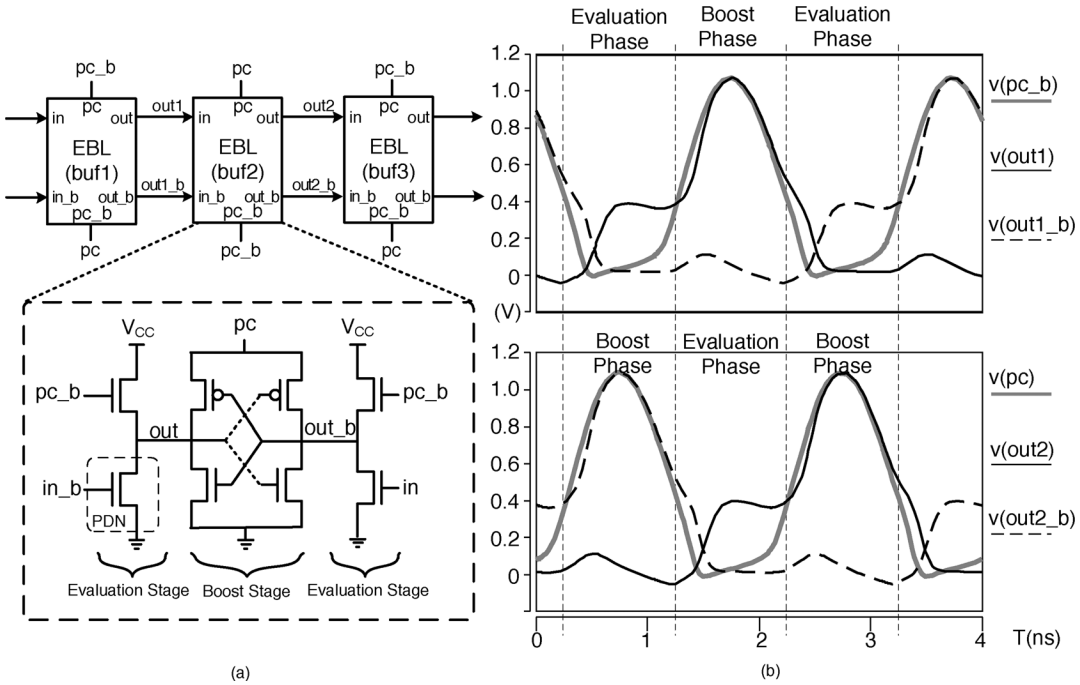

Fig. 3. EBL buffer schematic and operation.

Logic stage in the next SBL gate, yielding increased gate overdrive over Boost Logic. Compared to Boost Logic, SBL simplifies the number of supplies and powers each Boost stage with a single clock, yielding considerable reduction in crowbar current.

The Enhanced Boost Logic presented in this paper is another variant of Boost Logic that is aimed at pushing the iso-energy frequency point higher than SBL, while at the same time decreasing latency overhead. Fig. 3(a) shows a cascade of three EBL buffers. Each EBL gate has two stages: Evaluation and Boost. Similar to SBL, the Boost stage consists of a cross-coupled inverter with the source of the pMOS connected to a charge-recovering clock phase pc, enabling high performance through enhanced gate overdrive. Unlike SBL, however, the Evaluation stage relies on an nMOS precharge device for pull-up, instead of a complementary pull-up network, thus increasing performance by avoiding the series-connected devices in the pull-down network (PDN). The bulk of all nMOS transistors are connected to ground, and the bulk of pMOS transistors in the cross-coupled inverters are connected to the corresponding power-clock phases. From a functional point of view, each EBL gate is equivalent to a combinational logic block (Evaluation stage) that is powered by a near-threshold supply $V_{\rm CC}$ and drives a transparent latch synchronized by clock phase pc (Boost stage). Cascades of EBL gates are clocked by alternating clock phases pc and pc_b.

Each EBL gate operates in two phases: Evaluation and Boost. Fig. 3(b) shows the operating waveforms of EBL buffers buf1 and buf2 in the three-buffer cascade of Fig. 3(a). During the Evaluation phase of buf2, the clock phase pc ramps-up to full $V_{\rm DD}$, then back to ground, while the other clock phase pc_b stays well below threshold voltage. As the inputs of buf2 ramp up with clock phase pc, the Evaluation stage charges node out2 toward the subthreshold supply level $V_{\rm CC}$, and discharges node out2_b towards ground. Notice that even though the Evaluation stage is powered by a near-threshold supply, its PDN operates in super-linear mode, since its inputs are ramped to full $V_{\rm DD}$. Compared to Boost Logic, EBL achieves a gate overdrive of 0.8 V, yielding $2\times$ improvement in gate overdrive. Since the Evaluation stage inputs follow clock phase pc to full $V_{\rm DD}$, the performance of the nMOS precharge device is relatively immune to the Vth drop thanks to the increased gate overdrive. As inputs ramp down toward the threshold voltage level, following clock phase pc, the Evaluation stage is turned off. Throughout the Evaluation phase, the Boost stage is effectively shut off, since the clock phase pc_b is well below the threshold voltage.

During the first half of the Boost phase in the operation of buf2, the Boost stage amplifies the near-threshold voltage difference at out2 and out2_b to full rail as clock phase pc_b rises to full rail. This full-rail signal is used to drive the Logic stage of buf3, yielding enhanced gate overdrive. During the second half of the Boost phase for buf2, the power clock pc_b returns back to ground, recovering the charge at the output nodes of buf2 until it reaches the near-threshold supply level $V_{\rm CC}$.

The two clock waveforms required for EBL operation are generated using a clock generator similar to the blip circuit shown in Fig. 4 [18]. This circuit consists of two cross-coupled RLC oscillators, using the output waveform pc of one oscillator to drive the nMOS switch in the other oscillator and provide negative transconductance gm, and vice versa. The frequency of the oscillation is given by the equation:

$$f = \frac{1}{2\pi}\sqrt{\frac{1}{\rm LC} - \zeta^2} \tag{1}$$

where L denotes total inductance, C denotes the capacitance of the clock distribution and output nodes, and ζ denotes the

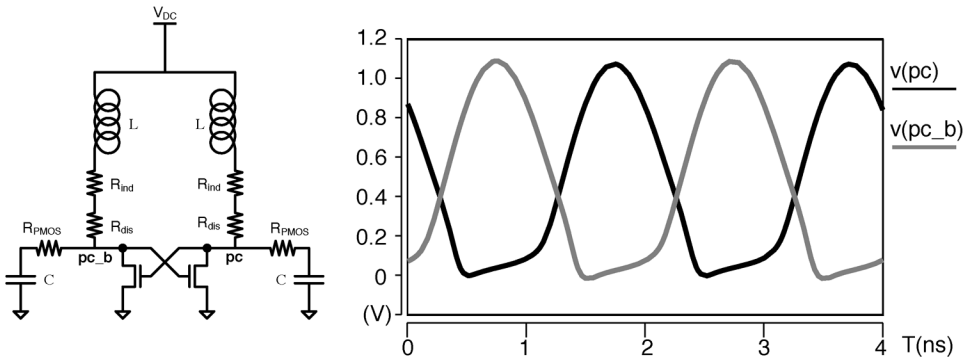

Fig. 4. Blip clock generator and its two-phase power clock waveforms.

damping factor. The amplitude of the clock waveforms is determined by the clock generator supply $V_{\rm DC}$. Since the damping factor varies with the amplitude of the clock driving the negative-transconductance switches, the resonant frequency has a slightly inverse relationship with the supply $V_{\rm DC}$. When the clock oscillates at the full nominal $V_{\rm DD}$ of 1.2 V, the overlap of the two clock phases occurs below the threshold voltage of the regular V_{th} nMOS device. Thus, unlike Boost Logic, EBL does not need a clocked device in the PDN of its Evaluation stage to limit short-circuit current.

In our test-chip, the inductive element has been implemented as a fully-integrated center-tapped symmetrical spiral inductor, due to the relatively high target clock frequency. Moreover, the two switches of the clock generator have been implemented as a collection of smaller switches that are distributed across the clock network. A small centralized switch is also used to enable frequency-scaled operation using current injection locking. A more detailed description of our clock generator design is given in Section III.

EBL improves upon Boost Logic in three ways. First, the use of a single near-threshold DC supply in the Evaluation stage reduces the number of power supplies required and doubles the gate overdrive. Second, the PDN of EBL gates enables the implementation of more complex functions. Specifically, by relying on a blip clock generator with two almost-non-overlapping phases, EBL eliminates the need for a clock-gated device in its PDN. Moreover, the $2\times$ gate overdrive allows more complex functions to develop the near-threshold difference between the dual-rail outputs by the end of the Evaluation phase. Therefore, the maximum pull-down stack height of an EBL gate can be higher than in Boost Logic. (In 1 GHz simulations, it can be seven nMOS devices high.) Third, the Boost stage requires a single clock phase, thus reducing the area overhead over Boost Logic by allowing minimal-sized nMOS devices. It also decreases power consumption compared to Boost Logic by reducing crowbar paths from $V_{\rm CC}$ to pc. Due to the single precharge nMOS device, EBL has lower area overhead over SBL, and can drive its outputs faster than SBL.

Per-cycle energy consumption of an EBL gate is given by the equation

$$E_{\rm EBL} = E_{\rm Evaluation} + E_{\rm Boost} + E_{\rm Crowbar} \tag{2}$$

where $E_{\rm Evaluation}$ and $E_{\rm Boost}$ denote the energy consumed in the two stages of EBL, and $E_{\rm Crowbar}$ denotes the energy consumed by crowbar current during the EBL operation. To derive an expression for $\rm E_{Boost}$, blip power-clock waveforms are modeled using a piecewise model. A sinusoid with amplitude greater than $V_{\rm DD}$ and a slightly negative offset is used to model the pulse region of the blip clock waveform, while a linear model is used to describe the power-clock waveform when it is closed to ground. Similar to the derivation found in [17], the energy consumption of the EBL can be approximated by the equation

$$E_{\rm EBL} = \frac{1}{2}\alpha C_L V_{\rm CC}^2 + \frac{9K(V_a - V_{CC})^2\pi^2 C_L^2 R}{16T} + E_{\rm Crowbar} \tag{3}$$

where α denotes the switching activity of the Logic stage, C_L denotes the capacitive load at the output, $V_{\rm CC}$ denotes the near-threshold supply of the Evaluation stage, K denotes a constant coefficient between 0.5 and 0.6 which depends on the clock amplitude, V_a denotes the amplitude of a sinusoid waveform used to approximate the blip region of the clock waveform, R denotes the sum of the inductor resistance $R_{\rm ind}$, the power clock distribution resistance $R_{\rm dis}$, and the resistance $R_{\rm PMOS}$ associated with the cross-coupled pMOS in the Boost stage, and T denotes the period of the power clock. By assuming V_a to be 1.5 $V_{\rm DD}$, $V_{\rm CC}$ to be 0.3 $V_{\rm DD}$, and K to be 0.56, the energy consumption equation can be rewritten as follows:

$$E_{\rm EBL} = 0.045\alpha C_L V_{\rm DD}^2 + \frac{0.45\pi^2 C_L R}{T} C_L V_{\rm DD}^2 + E_{\rm Crowbar}. \tag{4}$$

Notice that the energy consumed by the Evaluation stage is relatively small compared to the Boost stage, due to aggressive voltage scaling. Moreover, notice that the energy consumed by the Boost stage is not affected by the switching activity of the Evaluation stage, making charge-recovery logic more suitable for datapaths with high switching activity. However, for appropriate values of the RC_L product, an EBL design can achieve high performance and significant energy savings by trading off latency for energy.

III. FIR Test-Chip Overview

Since each EBL gate has a built-in transparent latch, the state-intensive nature of a transpose-type FIR filter coupled with the relatively simple combinational logic between its state elements

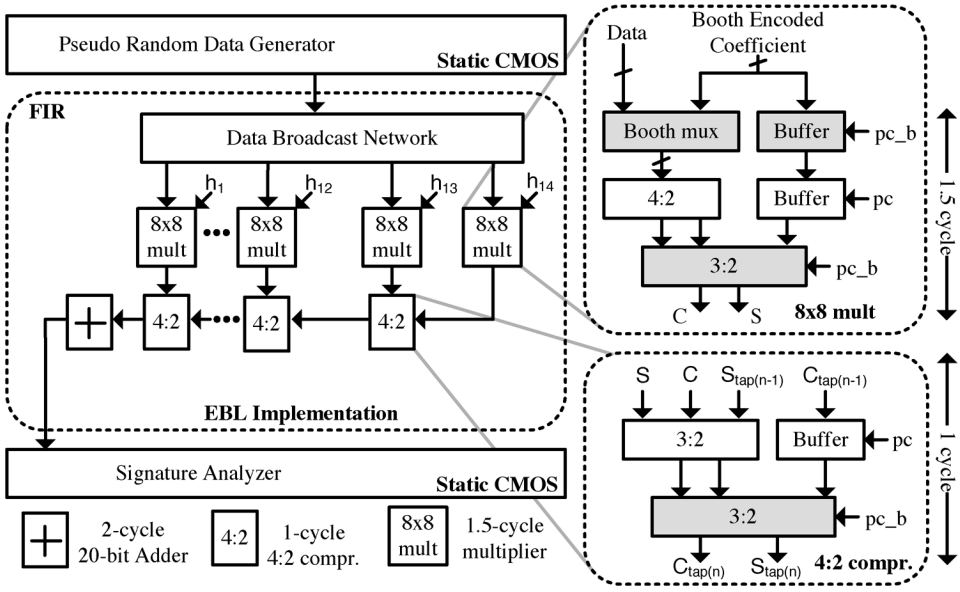

Fig. 5. FIR block diagram with clock generator and pulse generator.

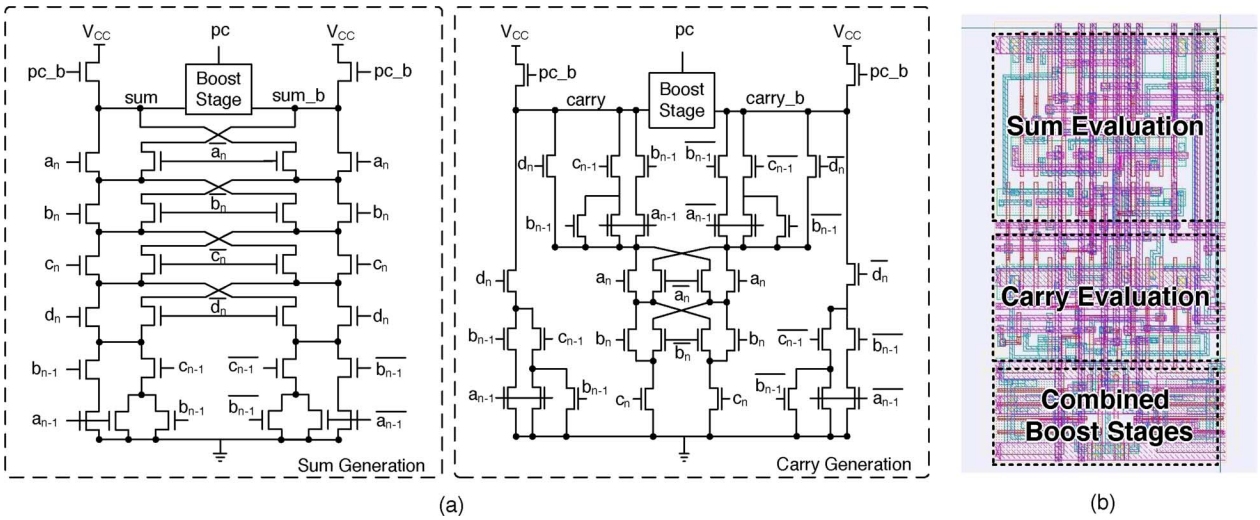

Fig. 6. EBL-based 4–2 compressor schematics and layout.

make it an ideal demonstration platform for EBL. To that end, we have used EBL to design an 8-bit 14-tap transpose-type FIR filter in a 0.13-μm CMOS digital process with 7 levels of Cu and 1 ultra-thick layer of Al. This section gives an overview of our FIR test-chip.

A complete block diagram of the FIR test-chip is shown in Fig. 5. The FIR filter is pipelined to take advantage of EBL's potential for low latency overhead. Input data are broadcast to each tap within 1 cycle. Each 8×8 multiplier takes 1.5 cycles to merge the partial products from the Booth mux to the sum and carry vector pairs. Each tap takes 1 cycle to merge the sum and carry vector pairs from the previous tap and the 8×8 multiplier. The vector pairs are then merged in a 20-bit hybrid carry-look-ahead/carry-select adder with two cycles of latency. The longest path through the EBL-based FIR has a latency of 18.5 cycles. Compared to other high-performance low-latency arithmetic implementations, the latency overhead of the EBL-based FIR is 1.5 cycles: 0.5 cycle in the 8×8 multiplier, and 1 cycle in the 20-bit adder.

EBL's latency improvement over previous generations of charge-recovery logic is based on its ability to implement logic functions of high complexity. The single-stage schematic of an EBL 4-to-2 compressor shown in Fig. 6(a) highlights the capability of EBL for implementing high-complexity functions. The Sum function has an evaluation stack height of six, and the Carry function has an evaluation stack height of five. Fig. 6(b) shows the 121.6 μm^2 layout implementation of the 4-to-2 compressor in EBL, which has only 7.6% area overhead when compared to a static CMOS implementation.

To reduce power dissipation of simple EBL gates, the EBL gates with stack height less than 4 have been implemented with a complementary pull-up network (PUN) in their Evaluation stage, and are thus identical to SBL gates. Due to the simplicity of the logic function they perform, their true and complement PUNs are sized so that the gates have similar performance as when designed with precharge devices. The PUN-based implementation of such relatively simple gates improves energy efficiency, as it prevents the increased crowbar currents of the in-

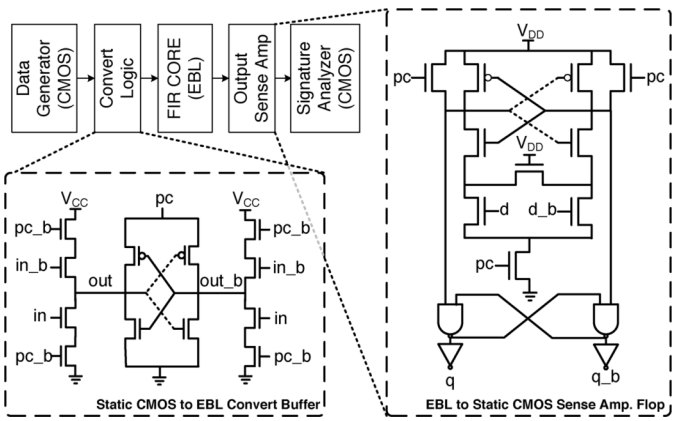

Fig. 7. Conversion circuits between EBL and static CMOS gates.

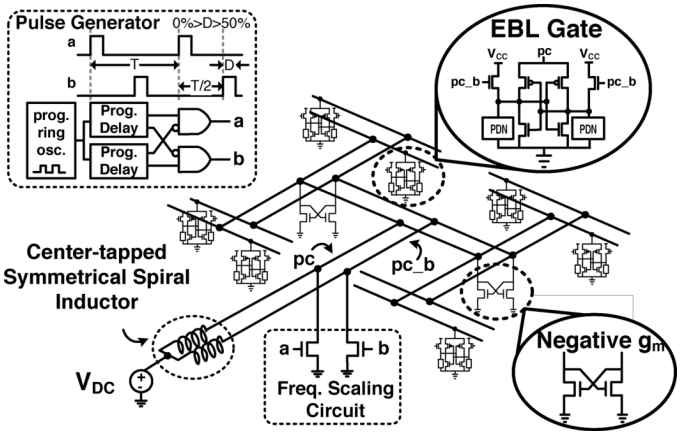

Fig. 8. Blip clock generator with frequency scaling circuits and power clock distribution.

herently (yet, in this case, unnecessarily) faster precharge-based EBL implementation.

The correct functionality of the FIR filter is validated through the use of build-in self test (BIST) circuitry. The BIST generates a pseudo-random cellular automaton sequence [19], processes the filter output using a multiple-input shift register to generate a signature vector, and captures the state of the signature at a user-defined time. When the signature vector matches a scan-in template, a single bit is inverted creating a single-bit signature output, which can be observed off chip.

This chip also demonstrates EBL's ability to be seamlessly integrated with static CMOS circuits. Fig. 7 shows the schematic for the interface circuits between BIST circuitry implemented in static CMOS and the EBL-based FIR filter. From static CMOS to EBL, a clock-gated nMOS is inserted in both the PUN and PDN of an EBL buffer to reduce leakage paths from power-clock to $V_{\rm CC}$. From EBL to static CMOS, a sense-amplifier flip-flop converts signals from an EBL gate output to a standard digital signal. The BIST circuits around the FIR filter, such as the pseudo-random sequence generator, the signature analyzer, and the signature generator, are implemented using standard cells. The output of the pseudo-random sequence generator is sent to convert buffers, and the outputs of the FIR are digitized by the sense-amplifier flip-flops before being processed by the signature analyzer.

The FIR datapath is clocked by two partially-overlapping clock phases that are generated using a blip generator. Extending the original blip design shown in Fig. 4, our clock generator has been designed with a distributed set of switches, rather than a centralized pair of switches. Moreover, it has been supplemented by a pair of switches that are driven by an external reference clock, thus enabling frequency-scaled operation. Our blip generator is shown in Fig. 8. The inductor is a fully-integrated 3 nH symmetrical inductor implemented on the top 2 levels, with a metal stripe ground shield at metal level 1. It has been placed right next to the FIR filter, with its center-tap connected to the clock generator supply $V_{\rm DC}$. Simulation results based on the foundry-provided model show that this inductor has a quality factor of 9.65 at 466 MHz. Twelve blocks of cross-coupled nMOS switches with 2400 μm total active width have been distributed across the FIR filter to provide the negative trans-conductance required to maintain the clock oscillation. The pair of nMOS switches used for frequency scaling are connected to the two inductor terminals and force the clock to oscillate at the reference frequency generated by an on-chip programmable ring oscillator. The inputs a and b of the frequency scaling switches can be selectively gated off to control drive strength, yielding driver sizes W in the range $0 < W < 150$ μm. To provide for maximal energy efficiency, the duty cycle D of a and b can be set in the range $0\% < D < 50\%$ through two programmable delays. The complementary power-clocks are routed out of the same side of the center-tap inductor and connected to the EBL gates, first through a 2-level H-tree, and then through a sparse clock grid.

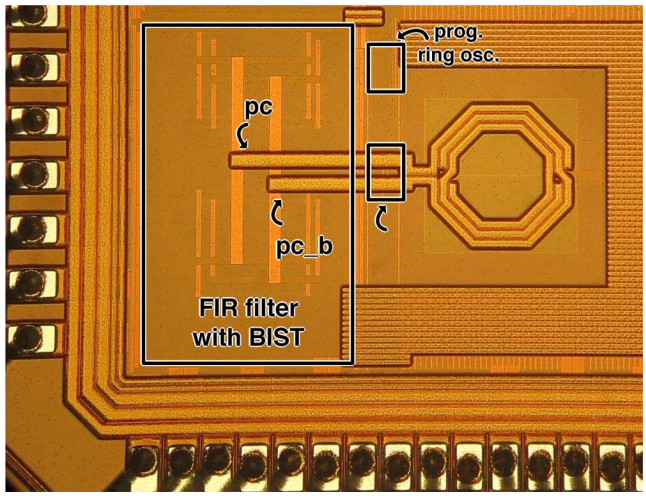

Fig. 9. Microphotograph of the FIR test chip.

Fig. 9 shows a microphotograph of the 600 MHz FIR test-chip. The FIR module occupies a total area of 715 μm $\times$ 350 μm. Including BIST, the design takes 800 μm $\times$ 430 μm. The 3 nH integrated inductor, including its moat, occupies about 0.14 mm^2. The programmable ring oscillator and the frequency scaling clock generation circuit are placed between the inductor and the FIR filter.

IV. EBL Design Methodology

Typically, charge-recovery logic has been designed using transistor-level simulation to verify functionality and electrical properties. The design and verification of large charge-recovery logic systems is therefore challenging, since the number of simulation cycles it takes to excite all possible input combinations and all possible timing arcs is at least exponential with the number of inputs. Even with the use of fast Spice programs such as Synopsys HSIM or Cadence Ultrasim, the computation required for such an approach is still probibitively high.

This section presents a semi-custom design methodology for EBL that led to improvements in the performance of the FIR test chip presented in this paper, while significantly reducing design time. This methodology enables the use of switch-level Verilog simulation. More importantly, it enables the use of industrial static timing analysis tools to verify the electrical properties of an EBL design. We first present an overview of our EBL design methodology, as applied to the FIR test-chip. We then describe the approach to switch-level netlist generation for Verilog simulation and LVS check using the same schematic. Finally, we describe our process to generate a LIBERTY format model file (.LIB) for the static timing analysis tools to verify electrical properties.

For the realization of the EBL-based FIR, we developed an EBL standard cell library with 65 EBL gates. Most of these cells are special cases of a 4-to-2 compressor and a 3-to-2 compressor. Prior to the start of the FIR design, all the cells were verified against their behavioral Verilog models using Spice. A LIBERTY format model file was created for the EBL standard cell library based on post-layout extracted Spice results, which are described in more detail later in this section. The FIR filter was pipelined manually, and correct functionality was verified through Verilog simulation. After manual place-and-route, the final layout was extracted, and the final netlist and the extracted parasitics were sent to the static timing analysis tool for timing closure. Timing violations were fixed either by sizing up gates or through architectural modifications.

Function verification is based on switch-level Verilog simulation by converting each EBL gate to its logic equivalent, a complementary combinational logic driving transparent latches. Even though it is possible to create a behavioral Verilog model for each EBL gate, we choose to generate switch-level Verilog models from schematics, since such a bottom-up verification approach is simpler and less prone to human errors than a top-down behavioral approach. The switch-level model generation proceeds as follows. During switch-level Verilog netlist generation, the Evaluation stage is converted to complementary combinational logic. The pull-up precharge devices in the Evaluation stage are instantiated as special nMOS devices in schematic, so that they would be netlisted as weak nMOS devices in Verilog. The use of these weak devices eliminates the possibility of having contention between the precharge devices and the pull-down networks in Verilog simulation. The Boost stage is netlisted as a pair of transparent latches, one for the true output and another for its complement. To netlist the Boost stage as a pair of transparent latches, the input and the output of the Boost stage need to be separated. In the schematic, a special parameterizable Boost stage cell is created with separate input and output ports and is instantiated in all EBL gates, enabling the Verilog netlister to systematically map all Boost stages in the design.

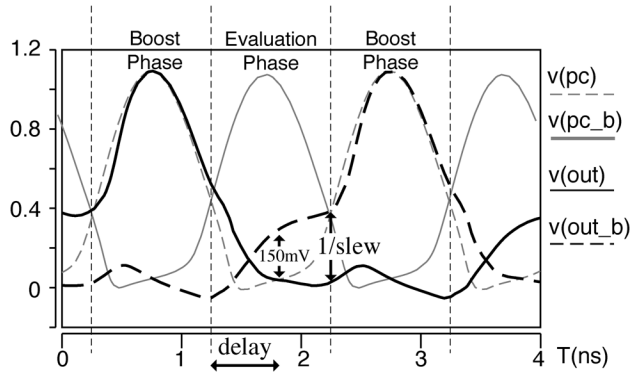

Fig. 10. EBL design methodology static timing delay and slew definition.

To reduce human errors, the same schematic used to generate switch-level model is used for LVS purposes. To that end, the differential inputs and outputs in the Boost stage cell are shorted using schematic shorting elements, cds_thru. By adding a new property in the LVS deck for cds_thru, the LVS program sees the Boost stage as a cell with two differential bidirectional ports, which enables each EBL gate to be LVS clean without maintaining additional schematic.

Making the EBL gate compatible with the LIBERTY format library model file is the key enabler for running static timing analysis on an EBL design. We observe that there is only one EBL gate in each clock phase, and that in the beginning of the Boost phase, the Boost stage behaves more like a sense amplifier in a SRAM array than a transparent latch. Based on these observations, we have developed a characterization script to extract the typical gate-level parameters such as pin capacitance, propagation delay, and transition time based on a new set of definitions.

The propagation delay of an EBL gate is the time it takes the Evaluation stage to switch its output pair. It is defined as the delay between the crossover of the two clock phases and the time when the differential outputs reach a certain voltage, as shown in Fig. 10. The crossover point of the two clock phases is chosen as the onset of the power clock, since its voltage level is close to the threshold voltage of Boost stage devices. For a sufficiently large output voltage difference, an EBL gate would operate correctly even if that voltage difference across the output pair is less than full V_{CC}. For reference, the rule-of-thumb voltage difference across the outputs before the onset of a sense amplifier is set to be at least 120 mV. To margin for higher capacitance mismatch and process variation in our methodology, we used a 150 mV voltage difference across the outputs.

Similar to conventional static CMOS standard cell characterization, the transition time (slew) parameter indicates the quality of a transition. However, since all EBL outputs track the power-clock waveforms, all transitions switch at the same rate as the power clock, making it meaningless to track the actual transition time using the normal 10% to 90% definition. Instead, our

characterization script uses the transition time parameter to assess how well the outputs are able to track the power clocks by redefining the transition time as the inverse of the voltage difference across the outputs at the onset of the power clocks, as shown in Fig. 10. A larger voltage difference across the outputs at the onset of the power clock implies that the Boost stage would be able to amplify the differential output pair more efficiently, in which case the outputs would track the power-clock more closely. In our design, 150 mV was picked as the minimal voltage difference across the outputs at the onset of the power clocks, since this requirement yields a delay between the power clock and the output during the Boost phase to be less than 10% of the cycle time, yielding a smaller voltage drop across the cross-coupled pMOS devices in the Boost stage. As the voltage difference drops below the desired 150 mV, the delay between the power clock and the output increases. In extreme cases, the output pair is amplified in the wrong direction and the gate malfunctions.

During .LIB file generation, our characterization script sweeps across a range of output loads, and generates a 1×7 table for each propagation delay and a 1×7 table for each transition time parameter. One .LIB file is generated for each target clock frequency and clock amplitude, since these two parameters affect the input pulse width and amplitude, which in turn affect the performance of the Evaluation stage. With extracted parasitics from a placed-and-routed layout, the .LIB file enables the use of static timing analysis tools to ensure timing closure and track design margin using the redefined transition time parameter described in the previous paragraph.

V. Simulation Evaluation

In this section, we present results from Spice-level simulations of our EBL FIR filter. For comparison purposes, we also present results from the simulation of a conventional static CMOS FIR filter that we have designed using the same architecture and a standard cell library in the same 0.13 μm process technology as the EBL FIR filter. The simulation results in this section are compared with measurement results obtained from the EBL FIR filter test-chip in Section VI.

The graphs in Fig. 11 give the per-cycle energy consumption of our EBL FIR filter at various clock frequencies when operating in self resonant mode. For each frequency, the graphs give total energy consumption, energy supplied to the clock generator through $V_{\rm DC}$, and energy supplied to the Evaluation stages of the EBL gates through $V_{\rm CC}$. The data at each frequency point have been obtained using the inductance value indicated next to it, and with the minimum supply setting that ensured correct function. Simulations have been performed using Synopsys HSIM with the post-layout extracted netlist based on the BSIM model and with foundry-provided parameterized inductor models. Correct operation has been confirmed from 230 to 800 MHz, with a center-tapped symmetric spiral inductor ranging from 11 to 0.95 nH, respectively.

Our simulation results in Fig. 11 show that the energy consumed by the clock generator $(V_{\rm DC})$ dominates the total energy consumption. They also show that total and clock generator energy requirements generally decrease, as frequency decreases.

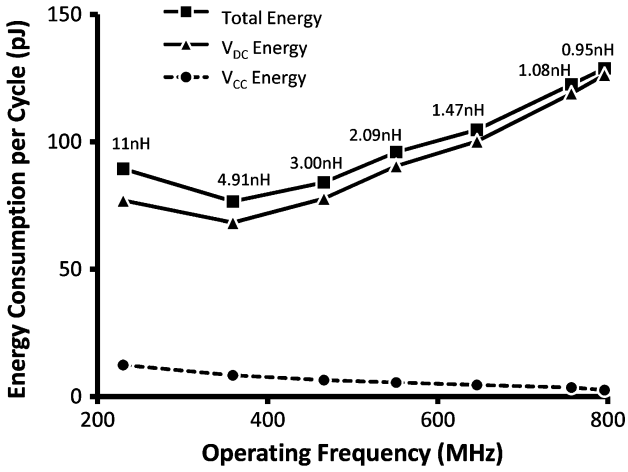

Fig. 11. Simulated energy consumption of self-resonant EBL FIR filter.

From 800 to 350 MHz, the energy supplied to the clock generator decreases almost linearly with the operating frequency, as predicted by the expression for the term $E_{\rm Boost}$ in (2) and (3). However, the energy consumed by the logic increases as operating frequency decreases, due to the increasing crowbar current in the clocked precharge devices of complex logic gates such as the 4-to-2 compressor. Total energy consumption increases from 350 to 230 MHz, a phenomenon that can be explained by the choice of inductor at 230 MHz. Specifically, to provide the larger inductance required for resonance at 230 MHz, inductor width is reduced from 15 μm to 8.5 μm, increasing inductor resistance and impacting efficiency in the following two ways. First, since inductor resistance is a large portion of the overall effective resistance, total resistance increases by a much greater proportion than transition times, resulting in increased energy consumption over 350 MHz. Second, operation at 230 MHz requires an even larger inductor than implied by a straightforward resonant frequency calculation, since the increased inductor resistance results in an increased damping factor and, based on (1), an increased resonant frequency. At frequencies below 300 MHz, it appears that an off-chip discrete inductor would be the preferred choice with regard to energy savings.

The graphs in Fig. 12 give per-cycle energy consumption versus clock frequency when the FIR filter is operating in frequency-scaled mode with a fixed 3 nH integrated inductor. Energy requirements are reported separately for the logic $(V_{\rm CC})$, the clock generator $(V_{\rm DC})$, and the frequency-scaling circuitry $(V_{\rm CK})$. Total energy is given across the frequency range, as well as when the FIR is self-resonating with the frequency-scaling circuitry turned off. The minimum energy point is achieved at the resonant frequency of 466 MHz. When the frequency-scaling circuit is enabled at resonance, the energy consumed by the $V_{\rm CK}$ domain becomes non-zero, while the energy drawn from $V_{\rm DC}$ and $V_{\rm CC}$ remains almost the same. As operating frequency deviates from resonance, higher $V_{\rm DC}$ and $V_{\rm CK}$ supplies are required to maintain clock amplitude at the rails. As operating frequency deviates sharply from resonance, the clock waveforms become more distorted, and their overlap

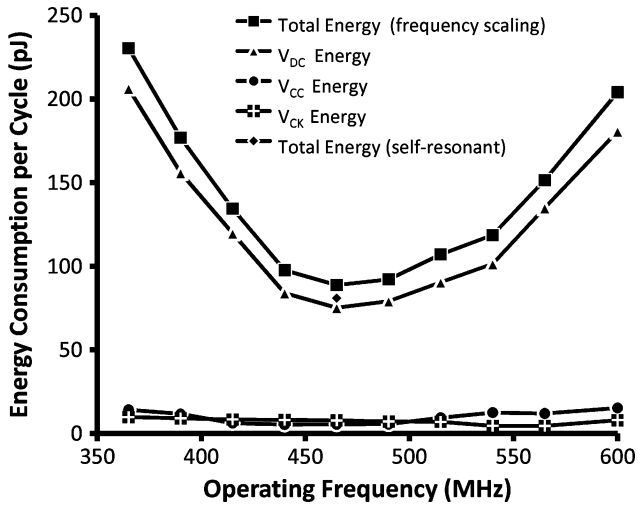

Fig. 12. Simulated energy consumption per cycle of the frequency-scaled EBL FIR filter.

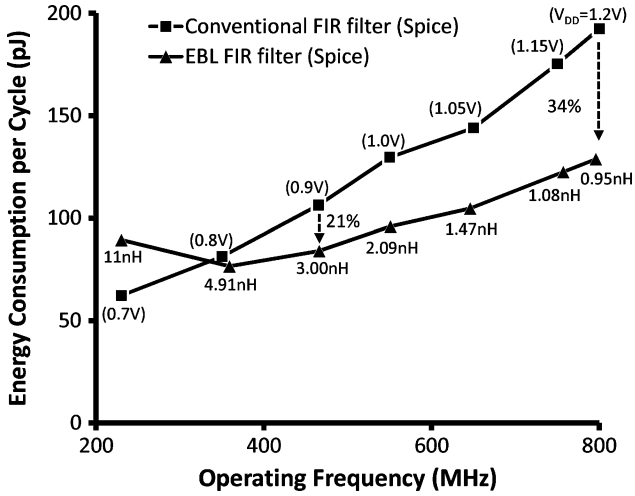

Fig. 13. Energy consumption per cycle comparison between conventional FIR and self-resonant EBL FIR filter.

increases, yielding increased leakage current and increased energy consumption in the $V_{\rm CC}$ domain.

For comparison purposes, we have synthesized a conventional static CMOS FIR filter using Synopsys Design Compiler and a standard cell library in the same 0.13 μm technology as the EBL-based design. The conventional FIR filter is designed with an overall latency of 19 cycles, as flip-flops do not allow for half cycles. The synthesized netlist is automatically placed and routed using Cadence Encounter with 80% area utilization and a synthesized clock tree. The synthesized FIR filter occupies a footprint of 0.35 mm $\times$ 0.7 mm. Compared to the synthesized FIR filter, the EBL FIR filter incurs 37% area overhead mainly due to the on-chip inductor. At the nominal supply of 1.2 V, the conventional FIR filter achieves 800 MHz with more than 80% of the standard cells at X1 or X2 drive strength.

The graphs in Fig. 13 give the energy requirements of the voltage-scaled conventional FIR and the EBL-based FIR in self-resonant mode for a range of operating frequencies. For clock frequencies above 350 MHz, the EBL FIR filter exhibits 21–34% energy savings over its conventional counterpart. Below 350 MHz, the large inductors required to oscillate the system have poor quality factor due to their large dimensions and high turn counts, increasing the energy requirements of the EBL design compared to its conventional counterpart.

The graphs in Fig. 14 compare the energy requirements of the voltage-scaled conventional FIR and the EBL-based FIR in frequency-scaling mode with a fixed 3 nH inductor. With the frequency-scaling circuitry enabled, the EBL FIR filter consumes 17% less energy when operating at its resonant frequency of 466 MHz, and consumes less energy than the static CMOS FIR filter from 440 to 540 MHz. When running in self-resonant mode at 466 MHz, the EBL FIR filter achieves 21% energy savings compared to the conventional FIR filter running with a 0.91 V supply.

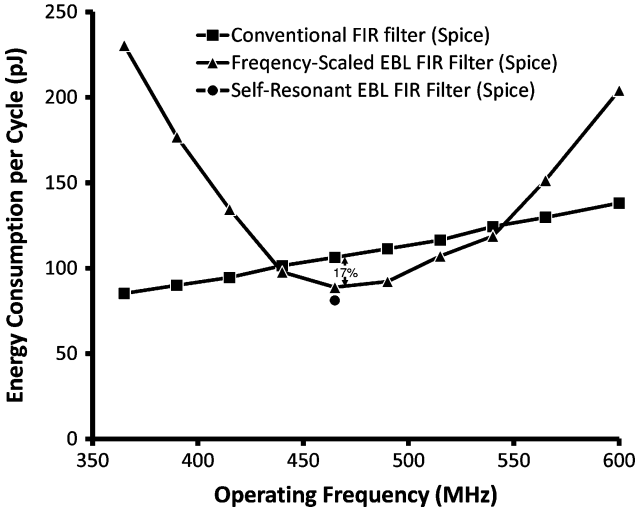

Fig. 14. Energy consumption per cycle comparison between conventional FIR and frequency-scaled EBL FIR filter.

VI. Measurement Results

This section gives measurement results from the experimental evaluation of the EBL FIR filter test-chip. It also presents a comparison of measurement and simulation results, showing good agreement between the two, with relative discrepancy between measurement and simulations staying within 12% for operating frequencies ranging from 365 to 600 MHz.

The graphs in Fig. 15 show current and inferred per-cycle energy consumption in the EBL FIR test-chip for operating frequencies in the 365 to 600 MHz range. Reported energy includes the energy in the clock generator $(V_{\rm DC})$, Evaluation logic $(V_{\rm CC})$, and frequency scaling circuitry $(V_{\rm CK})$. Each point in the plot corresponds to the minimum energy dissipation of the circuit over all possible values of $V_{\rm DC}$, $V_{\rm CC}$, D, and W that result in correct operation, as verified by observing the expected signature waveform. At the resonant frequency of 466 MHz, the minimum energy of 84 pJ is observed for $V_{\rm DC} = 0.57$ V, $V_{\rm CC} = 0.41$ V, and $V_{\rm CK} = 1.2$ V, with all frequency-scaling circuitry disabled. At self-resonance, the clock generator powered by $V_{\rm DC}$ is a significant source of energy consumption, and the Evaluation logic remains a small percentage of the total energy requirements. With frequency scaling enabled, the energy

TABLE I
FIR PERFORMANCE COMPARISON TABLE

Paper	This Work	[14]	[15]
Design Type	14-tap 8-bit FIR	8-tap 6-bit FIR	14-tap 8-bit FIR
Technology	0.13μm	0.18μm	0.13μm
Nominal Supply(V)	1.2	1.8	1.2
Operating Frequency(MHz)	466	225	1010
Sample rate(MSample/s)	466	550	1010
Power Dissipation(mW)	39.1	36	122.5
Area(mm^2)	0.34	0.3	0.85
Power / MHz / Tap / In-Bits / Coeff-Bits	93.6nW	230nW	133nW

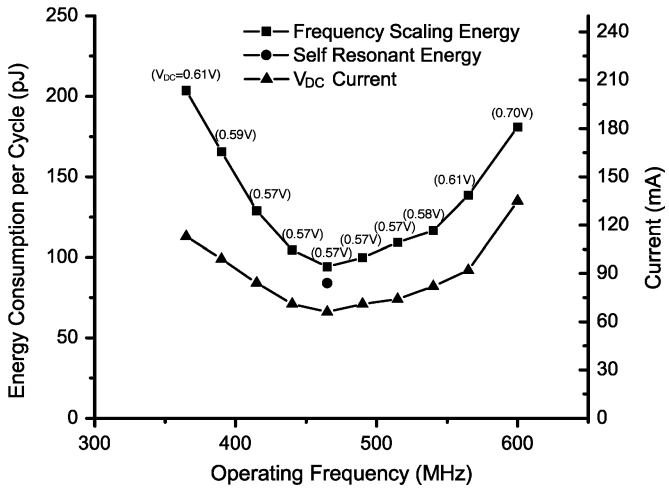

Fig. 15. Energy dissipation and current versus operating frequency.

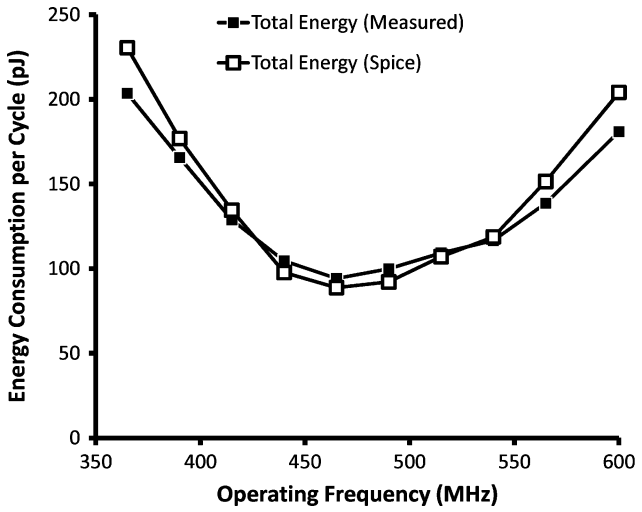

Fig. 17. Energy consumption per cycle comparison between conventional FIR and frequency-scaled EBL FIR filter.

Technology	0.13µm 8M CMOS
Taps, in/out/coeff bit	14, 8 / 20 / 8
EBL Gate count	3330
Total/active area	0.76 / 0.34 mm^2
Frequency range	365MHz – 600MHz
VDC Supply range	0.57V – 0.63V
Resonant Frequency	466MHz
Estimated Q	1.76
Energetics @ resonance	
Power Clock supply (V_{DC})	0.57V
EBL evaluation supply(V_{CC})	0.41V
Total/logic/clock power	39.1 / 2.0 / 37.1 mW
Total/logic/clock energy	83.9 / 4.4 / 79.5 pJ
Figure of Merit	93.6nW/MHz/Tap/InBit/CoeffBit
Input switching activity	0.5

Fig. 16. EBL FIR statistics and performance summary table.

consumption of the Evaluation logic remains relatively constant, while most of the additional energy consumption is caused by additional current in the programmable switches that drive the oscillator off resonance. The ability to scale operating frequency allows post-silicon tuning to mitigate the effects of process variation on the resonant frequency of the system. By increasing $V_{\rm DC}$ to 0.7 V, correct operation is verified at 600 MHz. Fig. 16 summarizes the chip statistics and measurement results, and Table I compares the performance of our EBL FIR with previously reported FIR filter test-chips with equal or greater sampling rate than our design at its 466 MHz resonant point.

In addition to the demonstration of energy-efficient and high-performance operation, our experimental evaluation also addresses the accuracy of the Spice-level simulation results presented in Section VI. The graphs in Fig. 17 show simulated and measured energy requirements of the EBL FIR that have been obtained under identical settings for $V_{\rm DC}$, $V_{\rm CC}$, $V_{\rm CK}$, W, and D. The two graphs track each other quite closely. For operating frequencies in the 365 to 600 MHz range, the discrepancy between simulation and measurement stays within 12%.

VII. CONCLUSION

This paper presents EBL, an energy-efficient charge-recovery logic family that exhibits low latency overheads. EBL uses an aggressively-scaled near-threshold supply to perform logic evaluation with low energy consumption. Increased gate overdrive enables high-speed operation or, alternatively, the single-gate realization of complex logic functions, both of which contribute to low overall latency.

To demonstrate the performance and energy advantages of EBL, we have designed a 14-tap 8-bit FIR filter test-chip in a 0.13 μm CMOS process. Unlike previously-published charge-recovery circuitry, in which overall latency is typically an order

of magnitude higher than static CMOS designs [13], [20], the EBL-based FIR filter achieves an overall latency overhead of 1.5 cycles compared to a high-performance FIR filter that we have designed using a standard cell library. In post-layout simulations, the EBL-based FIR filter running in self-resonant mode consumes 21% to 34% less energy than its voltage-scaled static CMOS counterpart from 466 to 800 MHz while incurring a 37% area overhead due to the on-chip inductor required. With frequency scaling circuitry enabled and a fixed 3 nH integrated inductor, simulation results show that the EBL FIR consumes 17% less energy at its resonant frequency of 466 MHz, and consumes less energy between 440 and 565 MHz even when forced to run off-resonance.

Fabricated in a 0.13 μm bulk-silicon process with regular threshold voltage at 0.4 V, the FIR-filter test-chip functions correctly from 365 to 600 MHz using a 3 nH on-chip symmetric spiral inductor. Clock drivers for self-resonant operation are fully integrated and distributed across the entire clock network. To support frequency-scaled operation, the clock generator includes an additional pair of small drivers that are located between the inductor and the FIR core. At its resonant frequency of 466 MHz, the FIR filter is at its most energy-efficient point, dissipating 39.1 mW and recovering 45% of the energy supplied through its clock generator. The corresponding figure of merit equals 93.6 nW/MHz/Tap/InBit/CoeffBit.

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Jerry C. Kao (S'04) received the B.S. degree in electrical engineering from Columbia University, New York, NY, and the M.S. degree in electrical engineering and computer science from the University of Michigan, Ann Arbor, in 2000 and 2002, respectively, where he is currently pursuing the Ph.D. degree on high-performance and low-power circuit technologies and design methodologies.

From 2002 to 2005, he was with IBM, Rochester, MN, where he was involved in the design of the CELL processor and the XBOX 360 processor.

Wei-Hsiang Ma (S'08) was born in Taipei, Taiwan. He received the B.S. degree in electrical engineering from the National Taiwan University, Taipei, Taiwan, in 2002, and the M.S. degree in electrical engineering and computer science from the University of Michigan, Ann Arbor, in 2007, where he is currently pursuing the Ph.D. degree in electrical engineering.

His research interests include low-power and high-performance circuit technologies and design methodologies.

Visvesh S. Sathe (S'02–M'11) received the B.Tech. degree in electrical engineering from the Indian Institute of Technology, Bombay, India, in 2001, and the M.S. and Ph.D. degrees in electrical engineering and computer science, in 2004 and 2007, respectively, from the University of Michigan, Ann Arbor.

While at Michigan, his research focused on low energy circuit design with particular emphasis on resonant-clocked digital design. He has held internship positions at the IBM T. J. Watson Research Center and Cyclos Semiconductor, a startup focusing on resonant-clocked microprocessors. In 2007, he joined the Advanced Power Technology Group, Advanced Micro Devices, Fort Collins, CO, as a Senior Design Engineer. His current work focuses on the exploration and implementation of power reduction techniques for microprocessors.

Marios C. Papaefthymiou (M'93–SM'02) received the B.S. degree in electrical engineering from the California Institute of Technology, Pasadena, in 1988, and the S.M. and Ph.D. degrees in electrical engineering and computer science from the Massachusetts Institute of Technology, Cambridge, in 1990 and 1993, respectively.

After a three-year term as Assistant Professor at Yale University, he joined the University of Michigan, Ann Arbor, where he is currently Professor of electrical engineering and computer science and Director of the Advanced Computer Architecture Laboratory. He is also cofounder and Chief Scientist of Cyclos Semiconductor, a startup company commercializing low-power devices. His research interests encompass algorithms, architectures, and circuits for energy-efficient high-performance VLSI systems. He is also active in the field of parallel and distributed computing.

Dr. Papaefthymiou was a recipient of an ARO Young Investigator Award, an NSF CAREER Award, and a number of IBM Partnership Awards. Furthermore, together with his students, he has received a Best Paper Award in the 32nd ACM/IEEE Design Automation Conference and the First Prize (Operational Category) in the VLSI Design Contest of the 38th ACM/IEEE Design Automation Conference. He has served multiple terms as an Associate Editor for the IEEE TRANSACTIONS ON THE COMPUTER-AIDED DESIGN OF INTEGRATED CIRCUITS, the IEEE TRANSACTIONS ON COMPUTERS, and the IEEE TRANSACTIONS ON VERY LARGE SCALE INTEGRATION (VLSI) SYSTEMS. He has served as the General Chair and as the Technical Program Chair for the ACM/IEEE International Workshop on Timing Issues in the Specification and Synthesis of Digital Systems. He has also participated several times in the Technical Program Committee of the IEEE/ACM International Conference on Computer-Aided Design.