187 MHz Subthreshold-Supply Charge-Recovery FIR

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***Abstract*—This paper presents a finite impulse response (FIR) filter chip that relies on a charge-recovery logic family to achieve multi-MHz clock frequencies with subthreshold DC supply levels. Fabricated in a 0.13 μm CMOS process with $V_{\mathrm{th,nmos}} = 0.40$ V, the FIR operates with a two-phase power-clock in the 5 MHz–187 MHz range and with DC supplies in the 0.16 V–0.36 V range. Using a single DC supply, the chip achieves its most energy-efficient operating point when resonating at 20 MHz with a 0.27 V supply. Recovering 89% of the energy supplied to its 57 pF per-phase load, it consumes 15.57 pJ per cycle and yields 17.37 nW/Tap/MHz/InBit/CoeffBit. Using two subthreshold DC supplies at 20 MHz, energy per cycle can be further reduced by 17.1%, yielding 14.40 nW/Tap/MHz/InBit/CoeffBit.**

***Index Terms*—Digital signal processing, low-power VLSI.**

I. Introduction

VOLTAGE scaling is one of the most effective methods for reducing energy consumption in digital electronics, as the energy consumed when switching a capacitive load C across a voltage difference V grows quadratically with V. In an aggressive version of voltage-scaled design, power supplies are set at levels below the device thresholds, relying on leakage currents to perform computations. These so-called subthreshold designs achieve extremely low levels of energy consumption per operation while giving up performance at an exponential rate, as power supply levels move deeper into the subthreshold operating regime.

Early subthreshold circuit designs appeared in electronic watches in the 1960s and 1970s, driven by form factor limitations on battery size [1]. The recent emergence of untethered applications and energy scavenging devices has lead to renewed interest in this field. A 1024-point FFT processor explored aggressive subthreshold designs for minimum energy operation, achieving a clock speed of 10 KHz with a 350 mV supply in a 0.18 μm process with $\mathrm{V_{th}} = 450$ mV [1]. The Subliminal subthreshold processor achieved 833 KHz with a 360 mV supply using a 0.13 μm process with $\mathrm{V_{th}} = 400$ mV [2]. The Phoenix processor deployed leakage reduction techniques to achieve pW-level power consumption, targeting multi-year operation in sensor applications [3], [4]. Fabricated in a dual-threshold 0.18 μm process with $\mathrm{V_{th1}} = 400$ mV and $\mathrm{V_{th2}} = 700$ mV, it achieved 2.8 pJ/cycle at 106 KHz with a 385 mV supply.

A common issue underlying all subthreshold circuit designs is that the significant energy advantages are achieved through deep voltage scaling, resulting in subthreshold currents and typically, sub-MHz clock frequencies. Recent subthreshold designs have deployed techniques to improve circuit robustness by improving gate overdrive. The 32-bit RISC core in [5] and the 8×8 FIR filter in [6] both deployed body biasing techniques to enable higher operating frequency, achieving 375 KHz at 230 mV, and 12 KHz at 200 mV, respectively. A high-speed variation-tolerant interconnect technique used capacitive boosting to elevate the critical gate supply voltage and achieve a 6 MHz clock distribution network at 400 mV [7].

In this paper, we present Subthreshold Boost Logic (SBL), a new circuit family that relies on charge-recovery design techniques to achieve order-of-magnitude improvements in operating frequencies while still achieving high energy efficiency using subthreshold DC supply levels. Specifically, SBL uses an inductor and a two-phase power-clock to boost subthreshold supply levels, overdriving devices and operating them in linear mode. Charge recovery switching is used to implement this boosting in an energy-efficient manner.

To demonstrate the performance and energy efficiency of SBL, we also present a 14-tap 8-bit finite-impulse response (FIR) filter test-chip fabricated in a 0.13 μm technology with $V_{\mathrm{th,nmos}} = 400$ mV. The energy-efficient operation of the SBL-based FIR test-chip has been experimentally verified for clock frequencies in the 5 MHz–187 MHz range. With a single 0.27 V supply, the test-chip achieves its most energy efficient operating point at 20 MHz, consuming 15.57 pJ per cycle with a recovery rate of 89% and a figure of merit equal to 17.37 nW/Tap/MHz/InBit/CoeffBit. With the introduction of a second subthreshold supply at 0.18 V, energy consumption at 20 MHz decreases further by 17.1%, yielding 14.40 nW/Tap/MHz/InBit/CoeffBit. At its maximum operating frequency of 187 MHz, the test-chip achieves 35.31 nW/Tap/MHz/InBit/CoeffBit and 34.47 nW/Tap/MHz/InBit/CoeffBit with one and two subthreshold supplies, respectively. To our knowledge, these figures of merit are the lowest published for FIR test-chips to date [8], [9]. In comparison with a static CMOS-based implementation derived by synthesis of the same FIR architecture and automatic place and route, the SBL-based FIR consumes 40% to 50% less energy per cycle in the 17 MHz–187 MHz range, based on device-level simulations, while incurring a 15% area overhead.

The remainder of this paper has six sections. Section II presents SBL and discusses its structure and operation, focusing on its high performance achievable through efficient signal boosting of subthreshold supply levels. Section III

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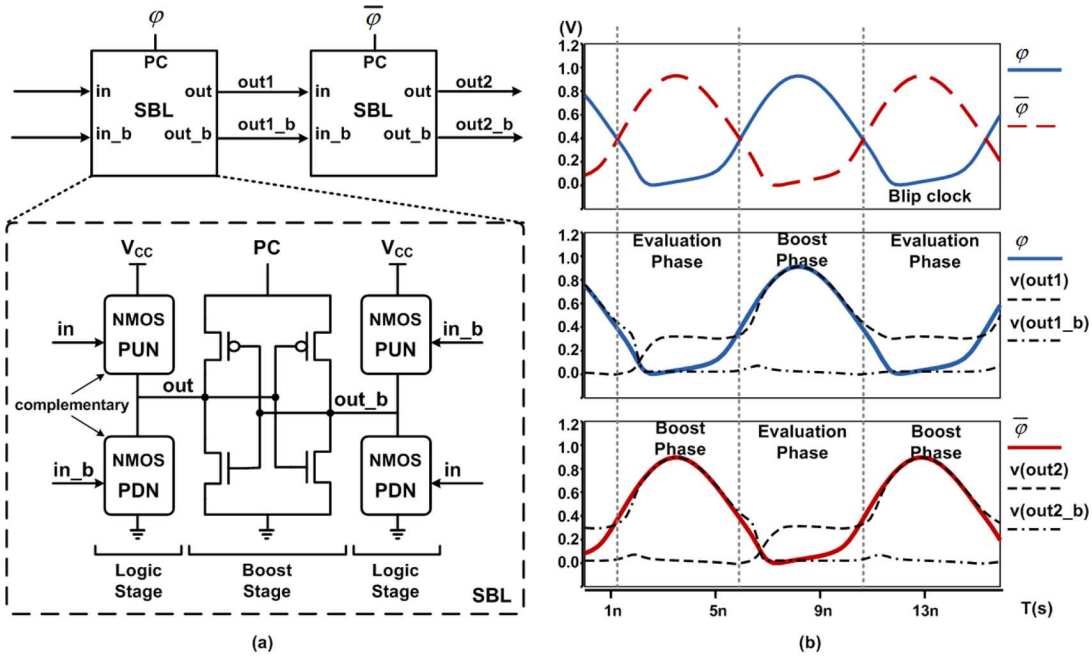

Fig. 1. Schematic of an SBL gate, cascade of SBL gates, and operating waveforms.

analyzes the energy consumption of SBL gates. Section IV presents the architecture and SBL implementation of the FIR test-chip. Section V presents results from device-level simulations of the SBL FIR and its static CMOS counterpart with the same architecture. In Section VI, we present measurement results from our SBL FIR test-chip. Conclusions are given in Section VII.

II. SBL Overview

The structure of a SBL gate and a cascade of SBL gates are shown in Fig. 1(a). Each SBL gate consists of two stages: Logic and Boost. The Logic stage has differential outputs out and $\mathrm{out\_b}$. Each output is driven by a pull-up network (PUN) and a pull-down network (PDN), similar to static CMOS logic, except that an nMOS PUN is used instead of a pMOS one for increased gate overdrive ability. The Boost stage comprises a pair of cross-coupled inverters connected to ground and a charge-recovery power-clock phase φ. From a functional standpoint, each SBL gate consists of a combinational logic block driving a transparent latch. Cascades of SBL gates are formed by clocking the gates on alternating power-clock waveforms φ and $\bar{\varphi}$.

Each SBL gate operates in two phases, Evaluation and Boost, which are active during mutually exclusive intervals. The graphs in Fig. 1(b) show the two phases with respect to the power-clock waveforms φ and $\bar{\varphi}$ and the waveforms at the output nodes of the two gates in Fig. 1(a). During Evaluation of the first SBL gate, φ remains effectively low, whereas $\bar{\varphi}$ transitions from low to high and then back to low. With their inputs boosted by the preceding SBL gate to be much higher than the supply voltage $\mathrm{V_{CC}}$, PUN and PDN charge $\mathrm{out1}$ to $\mathrm{V_{CC}}$ and discharge $\mathrm{out1\_b}$ to $\mathrm{V_{SS}}$ in super-linear mode. Notice that even though the PUN is implemented in NMOS, the output node does not suffer a $\mathrm{V_{th}}$ drop when charged to $\mathrm{V_{CC}}$, since the PUN inputs are boosted to be significantly higher than $\mathrm{V_{CC}}$. During Evaluation, the Boost stage is off, and there is no significant current flowing through any of the devices in the Boost stage, since the power-clock remains close to 0 V. As φ transitions low, the drive strength of the Logic stage gradually weakens, since its inputs gradually ramp down. When its inputs reach the subthreshold supply level $\mathrm{V_{CC}}$, the Logic stage is effectively off.

As the power-clock φ rises, the gate transitions into the Boost phase of its operation. During this phase, the Boost stage acts as an amplifier of the subthreshold voltage $\mathrm{V_{out1}} - \mathrm{V_{out1\_b}}$. The voltage $\mathrm{V_{out1}}$ tracks φ, reaching approximately 1 V as φ rises. As φ falls, the charge at the output node out1 is recovered by the power-clock φ, and the output voltage is brought back to approximately $\mathrm{V_{th}}$ levels. When φ falls below $\mathrm{V_{th}}$, all transistors in the Boost stage are in cut-off, and the next logic evaluation phase begins. Throughout the Boost phase, the node $\mathrm{out1\_b}$ stays essentially at 0 V.

Due to the significant gate overdrive at the Logic stage, SBL can reach higher operating speeds than static CMOS operating with the same subthreshold supply. For example, when the Logic stage is evaluating, SBL can be designed so that the inputs to the Logic stage exceed 0.9 V even with $\mathrm{V_{CC}} = 0.3\,\mathrm{V}$. Compared to static CMOS with a 0.3 V supply level, the Logic stage has 3X the gate overdrive, allowing SBL implementations to operate at higher clock frequencies and drive larger output load.

The power-clock waveforms required by SBL can be generated using a clock generator circuit similar to the "blip" circuit in [10], as shown in Fig. 2. This circuit is formed by connecting two *RLC* oscillators back-to-back, using the output waveform φ of one oscillator to drive the other, and vice versa. The two waveforms are partially overlapping, since the nMOS devices are not fully on until their output voltages exceed the threshold voltage $\mathrm{V_{th}}$. The amplitude of the output waveforms is determined by the voltage $\mathrm{V_{CC}}$. The clock generator that we used in

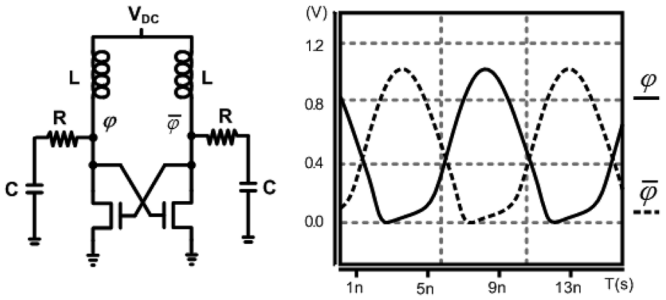

Fig. 2. Simple "blip" clock generator.

our FIR test-chip uses a distributed injection-locked version of this circuit and is described in Section IV.

SBL improves upon Boost Logic [11], its closest charge-recovery logic relative, in a number of significant ways. Specifically, SBL can operate with a single DC supply, whereas Boost Logic requires three DC supply levels. (Still, the energy efficiency of SBL improves when using different DC supply levels for logic and clock generation, as demonstrated by the experimental results in Section VI.) Moreover, the Boost stage in SBL is connected to ground, resulting in greater gate overdrive and thus higher performance than Boost Logic.

Compared to subthreshold logic, SBL accomplishes significant performance improvements through device overdriving. The NMOS-only PUN and PDN in the Logic stage are driven with inputs of approximately 1 V, allowing SBL to operate at clock frequencies in the hundreds of MHz or, alternatively, to realize functions of significant complexity within a single clock cycle. In addition to enhanced performance, gate overdriving leads to improved variation tolerance. All transistors in the Logic stage conduct in super-threshold linear mode, and delay does not vary significantly with variations in the subthreshold supply $\mathrm{V_{CC}}$ or $\mathrm{V_{th}}$.

III. SBL Energetics

The energy consumed during each cycle in the operation of an SBL gate is given by the equation:

$$\mathrm{E_{SBL}} = \mathrm{E_{Logic}} + \mathrm{E_{Boost}} + \mathrm{E_{crowbar}} \tag{1}$$

where $\mathrm{E_{Logic}}$ and $\mathrm{E_{Boost}}$ denote the energy consumed in the two stages of SBL, and $\mathrm{E_{crowbar}}$ denotes the energy consumed by short-circuit currents during SBL operation.

The energy consumption of the Logic stage is given by the equation

$$\mathrm{E_{Logic}} = \frac{1}{2}\mathrm{C_L}\mathrm{V_{CC}^2} \tag{2}$$

where $\mathrm{C_L}$ denotes the total switching capacitance at the SBL output. Compared to conventional switching, this energy consumption is significantly decreased due to the aggressively-scaled subthreshold supply level $\mathrm{V_{CC}}$.

To derive an expression for $\mathrm{E_{Boost}}$, we model the Boost stage as a simple *RC* series system with a "blip" voltage source that is modeled by two regions, sinusoidal and linear, as shown in Fig. 3. Simulations suggest that in the sinusoidal region, a sinusoidal waveform with 1.5 times the peak-to-peak amplitude $\mathrm{V_a}$ of the clock waveform φ provides a good approximation. Moreover, in the linear region, they indicate that the clock waveform rises almost linearly to approximately 0.1 V, independent of clock frequency and amplitude. Accordingly, the clock waveforms in the two regions can be approximated as follows:

$$\varphi_{\mathrm{sine}} = 0.25 \times \mathrm{Va} \times (1 + 3 \times \sin\omega\mathrm{t}), \tag{3}$$

$$\varphi_{\mathrm{linear}} = \frac{0.1 \times \mathrm{t}}{(\mathrm{T} - |\mathrm{t_{P1}} - \mathrm{t_{P2}}|)}, \tag{4}$$

where $\omega = 2\pi/\mathrm{T}$, T is the period of the clock waveform φ, and $\mathrm{t_{P1}}$ and $\mathrm{t_{P2}}$ are the endpoints of the two regions, as shown in Fig. 3. Solving (3) for 0.1 V and 0 V yields the following equation for the endpoints $\mathrm{t_{P1}}$ and $\mathrm{t_{P2}}$, respectively, of the two regions:

$$\mathrm{t_{P1}} = \frac{\sin^{-1}\left[\frac{(\frac{0.1}{0.25} \times \mathrm{V_a} - 1)}{3}\right]}{\omega}$$

$$\mathrm{t_{P2}} = \frac{\sin^{-1}[\frac{-1}{3}]}{\omega}$$

The energy $\mathrm{E_{sine}}$ consumed in the Boost stage of a SBL gate during operation in the sinusoidal region is given by integrating $\mathrm{I^2R}$ over time from $\mathrm{t_{P2}}$ to $\mathrm{t_{P1}}$, where I is the AC component of the current resulting when φ_{sine} drives the reactive load $1/\mathrm{j}\omega\mathrm{C_B}$, and R and $\mathrm{C_B}$ are the effective resistance and effective capacitance, respectively, when looking into the node PC of a SBL gate. (We assume that $\mathrm{R} \ll 1/\mathrm{j}\omega\mathrm{C_B}$, as confirmed by our test-chip.) From (3), we have

$$\mathrm{I} = \left|\frac{\mathrm{V}}{\frac{1}{\mathrm{j}\omega\mathrm{C_B}}}\right| = \left|\frac{0.25\mathrm{Va}\cdot 3\sin\omega\mathrm{t}}{\frac{1}{\mathrm{j}\omega\mathrm{C_B}}}\right|$$

and, therefore,

$$\begin{aligned}\mathrm{E_{sine}} &= \int_{\mathrm{t_{P2}}}^{\mathrm{t_{P1}}} \left|\frac{0.75\mathrm{Va}\cdot\sin\omega\mathrm{t}}{\frac{1}{\mathrm{j}\omega\mathrm{C_B}}}\right| \cdot \mathrm{R}\,\mathrm{dt} \\ &= \frac{9\mathrm{Va}^2\omega^2\mathrm{C_B^2R}}{32}(\mathrm{t} - 2\cos\omega\mathrm{t})|_{\mathrm{t=t_{P1}}}^{\mathrm{t=t_{P2}}} \\ &= \frac{9\mathrm{Va}^2\pi^2\mathrm{C_B^2R}}{8\mathrm{T}^2}\left(\mathrm{t} - \frac{1}{\omega}\cos 2\omega\mathrm{t}\right)|_{\mathrm{t=t_{P1}}}^{\mathrm{t=t_{P2}}} \\ &= \frac{\mathrm{K}\cdot 9\mathrm{Va}^2\pi^2\mathrm{C_B^2R}}{8\mathrm{T}}.\end{aligned} \tag{5}$$

Equation (5) has been simplified by including a coefficient K, $0.5 < \mathrm{K} < 0.6$, which depends on the clock amplitude. Replacing the clock amplitude $\mathrm{V_a}$ by the effective voltage swing in the Boost stage, $\mathrm{V_a} - \mathrm{V_{CC}}$, we obtain

$$\mathrm{E_{sine}} = \frac{9\mathrm{K}(\mathrm{V_a} - \mathrm{V_{CC}})^2\pi^2\mathrm{C_B^2R}}{16\ \mathrm{T}}. \tag{6}$$

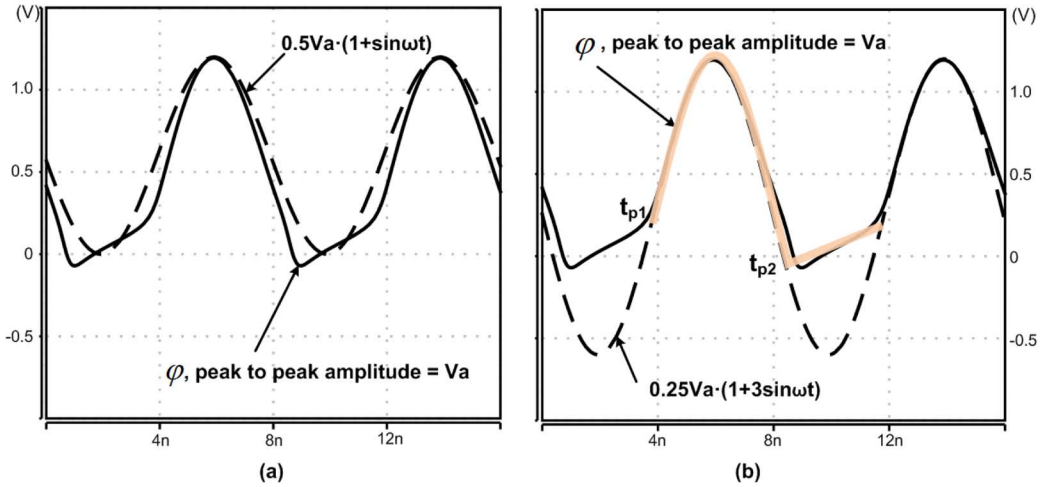

Fig. 3. Clock waveform modeling. (a) Sine clock with equal peak-to-peak swing. (b) Sine clock with 1.5x peak-to-peak swing.

The energy E_{linear} consumed in the Boost stage of a SBL gate during the linear region of the clock waveform is given by integrating I^2R over time, where I is derived from (4):

$$\begin{aligned} E_{linear} &= \int_0^{T-|t_{p1}-t_{p2}|} I^2 \cdot R dt = \int_0^{T-|t_{p1}-t_{p2}|} \left| C_B \frac{dV}{dt} \right|^2 R dt \\ &= \int_0^{T-|t_{p1}-t_{p2}|} \left| C_B \frac{d\left(\frac{0.1}{T-|t_{p1}-t_{p2}|} t\right)}{dt} \right|^2 R dt \\ &= \frac{0.01 C_B^2 R}{T-|t_{p1}-t_{p2}|}. \end{aligned} \quad (7)$$

From (6) and (7), it follows that $E_{linear}/E_{sine} < 1\%$, and therefore the total energy consumption in the Boost stage can be approximated by E_{sine}. From (1), (2), and (6), it follows that the total energy consumption of a SBL gate during a cycle is given by

$$E_{SBL} = \frac{\frac{1}{2} C_L V_{CC}^2 + 9K(V_a - V_{CC})^2 \pi^2 C_B^2 R}{16T} + E_{crowbar}. \quad (8)$$

Based on Spice simulation results, the effective resistance and capacitance seen from each clock phase are about 0.6 Ω and 57 pF, respectively.

The crowbar component of energy consumption in (8) has three components: $E_{V_{CC}\text{-}V_{SS}}$, $E_{V_{CC}\text{-}PC}$, and $E_{PC-V_{SS}}$. The energy $E_{V_{CC}-V_{SS}}$ is associated with the Logic stage. Specifically, due to the relatively slow rise time of the input waveform, short current will flow from V_{CC} to V_{SS} during the evaluation phase. This component dominates $E_{crowbar}$. At very low operating frequencies, it also dominates the total energy consumption E_{total}, as we discuss in Section VI. The energy $E_{V_{CC}\text{-}PC}$ is consumed during the evaluation phase. As V_{CC} charges one of the output nodes, current flows from V_{CC} to the PC pin through the pMOS device in the Boost stage. Since V_{CC} is always at a subthreshold voltage level, this component is relatively small compared to $E_{V_{CC}-V_{SS}}$. The energy $E_{PC\text{-}V_{SS}}$ is consumed during the boost phase. As φ rises, although the Logic stage is turned off, current still flows from the PC pin to V_{SS} through the evaluation NMOS. Similar to $E_{V_{CC}\text{-}PC}$, this component is significant only at very low operating frequencies.

Equation (8) provides guidance for device sizing and illustrates some of the energy trade-offs. For example, in the Boost stage, up-sizing the pMOS devices reduces the effective resistance R, but increases the effective capacitance C_B. In the Logic stage, up-sizing the evaluation pull-up and pull-down networks yields a greater potential difference at the output nodes by the end of the evaluation period, resulting in higher energy efficiency during the Boost stage. At low operating frequencies, however, such up-sized networks result in increased $E_{V_{CC}\text{-}V_{SS}}$.

IV. FIR Overview and SBL Implementation

To demonstrate the fast and energy-efficient operation of SBL, we used it in the implementation of a transpose FIR filter. The relatively state-intensive nature of the transpose type FIR filter, coupled with the relatively simple computation that is performed between state elements present a natural fit for SBL, since each SBL gate comes with a transparent latch timing element, reducing the latency and area overhead of the SBL-based FIR filter compared to a static CMOS counterpart.

A block diagram of the 8-bit 14-tap FIR chip is given in Fig. 4. A static CMOS built-in self-test (BIST) circuit is used to generate and process the FIR input and output. The pseudo-random input sequence generated by BIST is broadcast to 14 modified 8×8 Booth multipliers. The products of these inputs with the 14 FIR coefficients are accumulated through 14 4-to-2 compressors. The final result is obtained from a hybrid adder, and then sent to a signature analyzer, generating a signature vector. To enable SBL to communicate with the static CMOS BIST logic, two interface blocks are inserted before and after the FIR. Broadcast buffers convert the signals from static CMOS to SBL, and sense-amplifier flip-flops that can operate with subthreshold-level inputs latch the SBL signals from the FIR and make them available to the static CMOS signature analyzer.

Gate overdrive at the Logic stage of SBL gates allows the implementation of functions with significant complexity within a

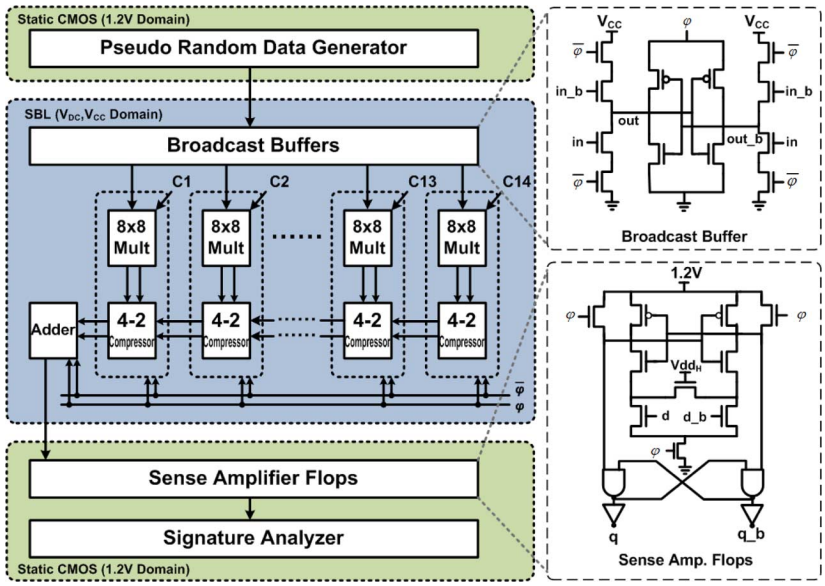

Fig. 4. Block diagram of SBL FIR filter and BIST circuits.

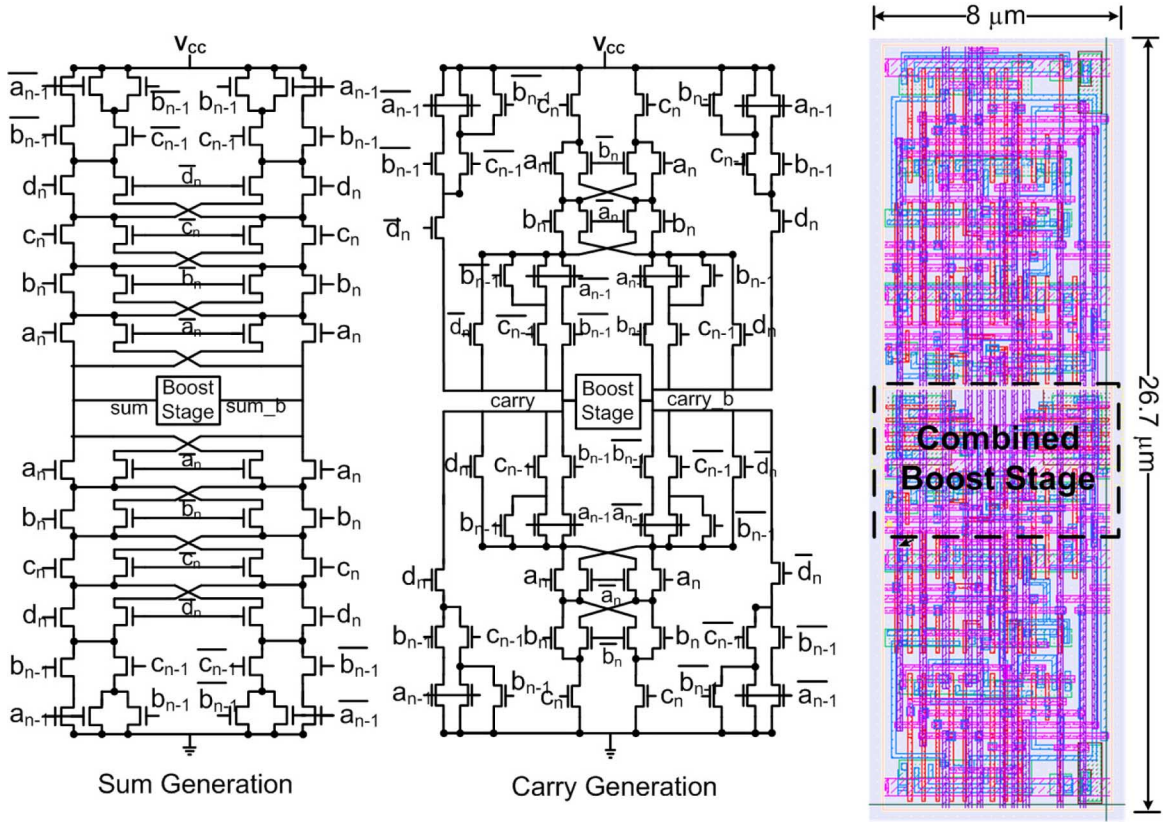

Fig. 5. Schematic and layout of a 4-2 compressor.

single clock cycle. Fig. 5 shows schematics and layout of the SBL-based 4-to-2 compressor used in the FIR. Each SBL gate has a transistor stack height of six and can operate at 187 MHz with $\mathrm{V_{CC}} = 0.36$ V. Due to the dual-rail nature of the SBL gates, the SBL 4-to-2 compressor has 2.1X area overhead compared to a standard-cell implementation.

The SBL FIR uses two power-clock waveforms φ and $\bar{\varphi}$ that are generated by the clock circuit shown in Fig. 6. In this clock generator, the basic "blip" generator circuit has been augmented to include a pair of weak drivers at the root of the tree that allow for the power-clock waveforms to be injection-locked to a target clock frequency. These drivers are pulsed by reference signals A and B that are generated by an on-chip pulse generator. In our test-chip, the drivers can tune the operating frequency by as much as $\pm 3\%$ off resonance. The tuning range can be increased by sizing up the injection-locked devices. Fourteen pairs

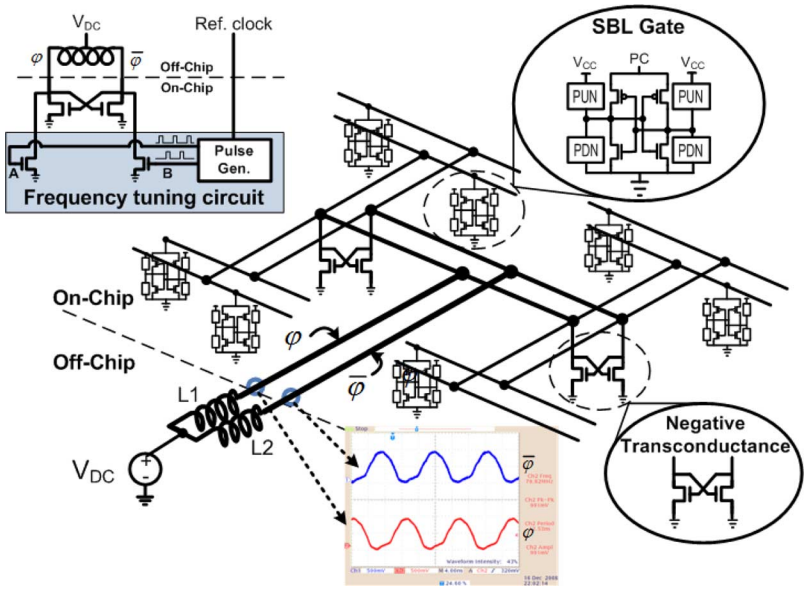

Fig. 6. Distributed "blip" clock generator and measured clock waveform.

of cross-coupled nMOS switches are distributed throughout a hierarchical two-phase distribution network, similar to [9]. Two off-chip inductors are used to resonate the parasitic capacitance of the clock distribution network and the SBL gates. In our test-chip, the load on each phase of the power-clock is approximately 57 pF, as derived from layout extraction.

The clock circuitry is powered by a DC supply V_{DC} that can be controlled independently of the supply V_{CC} for the SBL gates. The level of V_{DC} determines the amount of energy re-introduced into the clock network each cycle, thus affecting the amplitude of the power-clock waveforms and controlling the level of overdrive at the Logic stages. Although not required for correct operation, the independent control of V_{DC} and V_{CC} allows for increased energy efficiency. Specifically, by decreasing V_{CC} to limit crowbar current through the Logic stage while keeping V_{DC} sufficiently high to ensure the requisite overdrive, energy efficiency can be improved without sacrificing performance. As shown in Section VI, the FIR achieves energy-efficient operation with $V_{DC} = V_{CC}$, but its energy consumption per cycle decreases further by 17.1% when V_{DC} and V_{CC} are set to different subthreshold values.

A die photo of the SBL-based FIR is shown in Fig. 7. A variety of statistics related to our test-chip, along with performance measurements results to be discussed in more detail in Section VI, are given in the table of Fig. 8. Implemented in a 0.13 μm bulk silicon regular-V_{th} process, the FIR test-chip comprises a total of approximately 41,000 devices. The FIR filter occupies 0.80 mm $\times$ 0.35 mm $=$ 0.28 mm^2. Including BIST, the entire test-chip occupies a total area of 0.38 mm^2. To reduce the parasitic resistance of I/O pads and bondwires, two pads are used in parallel to connect each power-clock phase to one of the terminals of the corresponding off-chip inductor. With the exception of the inductors, which were discrete devices mounted off the die, all other test-chip circuitry was fully integrated on the die.

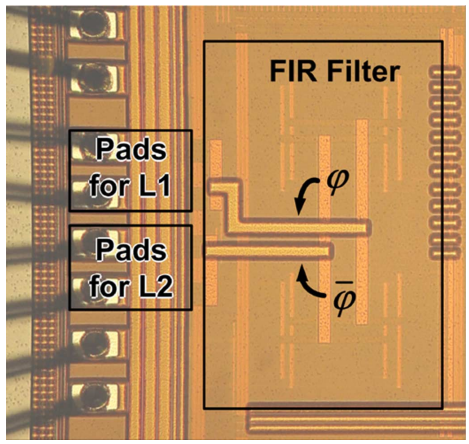

Fig. 7. Die microphotograph.

V. Simulation Evaluation

In this Section, we present results from Spice-level simulations of our SBL test-chip. For comparison purposes, we also present Spice-level simulation results of a conventional static CMOS version of the FIR, which was obtained by performing automatic synthesis, placement, and routing of the same FIR architecture that we used to derive the SBL FIR test-chip. Measurement results from our SBL FIR test-chip, along with a comparison of simulation and measurement results are given in Section VI.

Fig. 9 gives a plot of energy consumption per cycle versus operating frequency for our SBL FIR design. This graph was obtained using Synopsis Hsim with the BSIM model on a netlist of our SBL FIR that was obtained from layout extraction. All data points were obtained with the minimum supply setting $V_{CC} = V_{DC}$ that yielded correct operation at the corresponding operating frequency. Notice that energy consumption is dominated by the component related to the power-clock generator, which corresponds to the power supply V_{DC}. Moreover, notice that

Technology	0.13 µm 8M CMOS (RVT)	
Threshold Voltage	NMOS: 0.40V PMOS: -0.42V	
Taps, In / Coeff Bits / Out	14, 8 / 8 / 20	
Total Transistors Count (including BIST)	PMOS: ~8000 NMOS: ~33000	
Total Area (including BIST)	0.38 mm2	
Effective Cap. per Clock Phase	~57pF	
BIST Supply Voltage	1.2V	
Switching Activity	0.5	
Measured Frequency Range	5MHz – 187MHz	
	Single Supply Setting:	Two Supplies Setting:
Supply Voltage	V_{DC}=V_{CC}=0.27V @ 20MHz V_{DC}=V_{CC}=0.36V @ 187MHz	V_{DC}=0.27V, V_{CC}=0.18V @ 20MHz V_{DC}=0.36V, V_{CC}=0.28V @ 187MHz
Energy per Cycle	15.57 pJ @ 20MHz 31.64 pJ @ 187MHz	12.90 pJ @ 20MHz 30.88 pJ @ 187MHz
Figure of Merit (nW/MHz/Tap/In-Bit/Coeff-Bit)	17.37 @ 20MHz 35.31 @ 187MHz	14.40 @ 20MHz 34.47 @ 187MHz

Fig. 8. SBL FIR filter statistics and performance measurements.

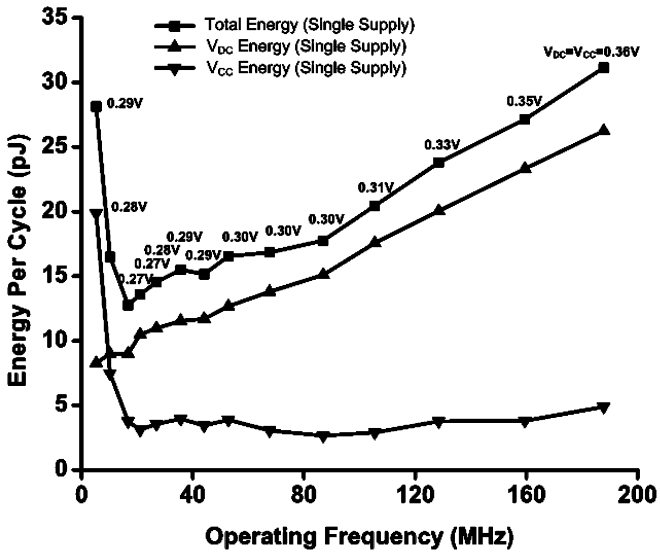

Fig. 9. Simulated energy consumption of SBL FIR filter.

at frequencies below 20 MHz, the energy consumption of the Logic stage, which corresponds to the power supply V_{CC}, starts rising at an increasing rate, due to the increasing crowbar current from V_{CC} to V_{SS} caused by the slowly transitioning inputs of the Logic stage. Consequently, total energy consumption for the SBL FIR starts increasing at operating frequencies below 17 MHz.

To compare our SBL FIR with conventional CMOS design, we synthesized a standard-cell version of the same 19-cycle FIR architecture that we used to derive the SBL design in the same technology. Synthesis was performed by Synopsys Design Compiler, yielding a conventional FIR with the same latency as the SBL FIR. Placement and routing were performed in a fully automatic manner using Cadence SoC Encounter with 80% area utilization and a synthesized clock tree. The layout of the resulting design is shown in Fig. 10(a). With a 0.35 mm $\times$ 0.7 mm footprint, the synthesized FIR occupies approximately 12.5% less area than its SBL counterpart.

Fig. 10(b) gives Spice-derived graphs for the operating frequency and the per-cycle energy consumption of the static CMOS FIR as a function of the supply voltage. With 83% of its cells sized at X1 or X2 drive strength, this FIR achieves a clock frequency close to 800 MHz with a nominal 1.2 V supply. As expected, energy consumption per cycle varies quadratically with supply voltage. Furthermore, operating frequency deteriorates exponentially fast, as supply voltage drops below 0.6 V, barely exceeding 250 KHz when the supply is set at 0.3 V.

For both the SBL and the conventional FIR, simulated per-cycle energy consumption versus operating frequency is given in Fig. 11. In the frequency range from 17 MHz to 187 MHz, the SBL FIR achieves 40% to 50% lower energy consumption than its conventional counterpart. The SBL design yields minimum energy consumption at 17 MHz, achieving 43.7% reduction over its conventional counterpart. The maximum relative energy reduction of 52.9% is achieved at 44 MHz. At 187 MHz, the maximum clock frequency at which the SBL design functions correctly, relative energy savings over the conventional FIR are 41.1%.

Clock skew is introduced due to load variation across the chip. Fig. 12 shows power-clock insertion delay data obtained from Spice-level simulations of the entire chip with extracted resistance, capacitance, and coupling capacitance. At the resonant frequency of 53.7 MHz, the maximum possible power-clock skew is 39.6 ps.

VI. Test-Chip Evaluation

This section gives measurement results from the experimental evaluation of the SBL FIR test-chip, validating its energy-efficient operation with subthreshold supplies at clock frequencies

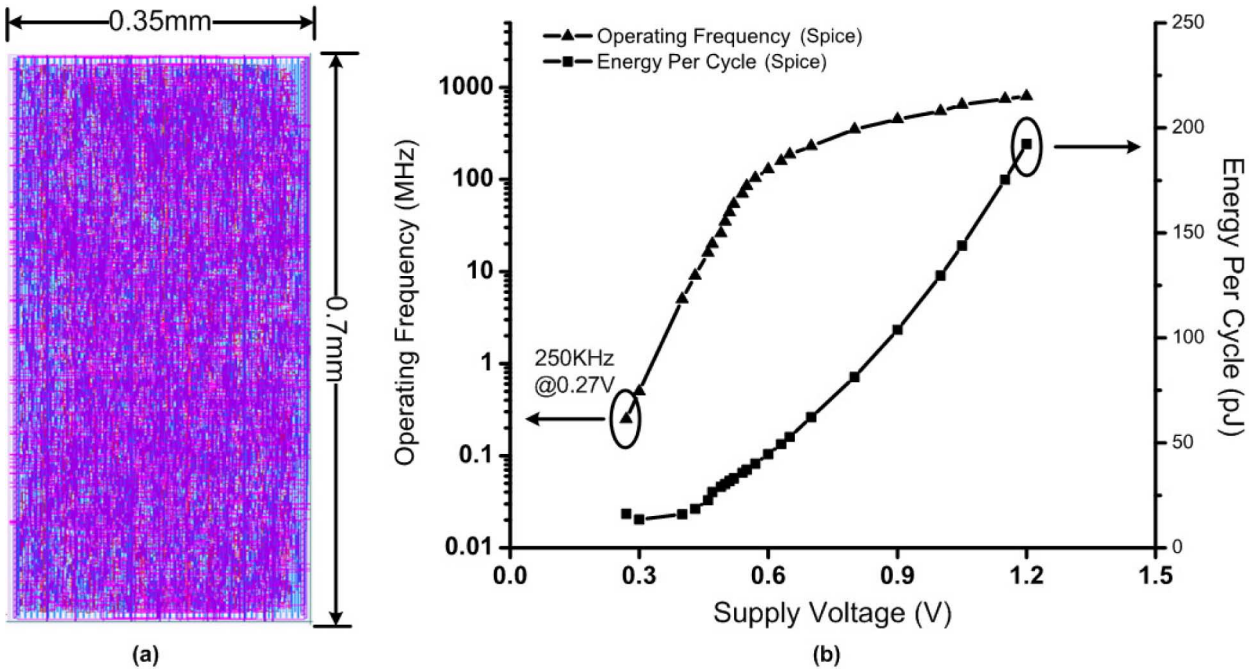

Fig. 10. (a) Layout of conventional CMOS FIR. (b) Simulated operating frequency and energy per cycle versus supply voltage for conventional CMOS FIR filter.

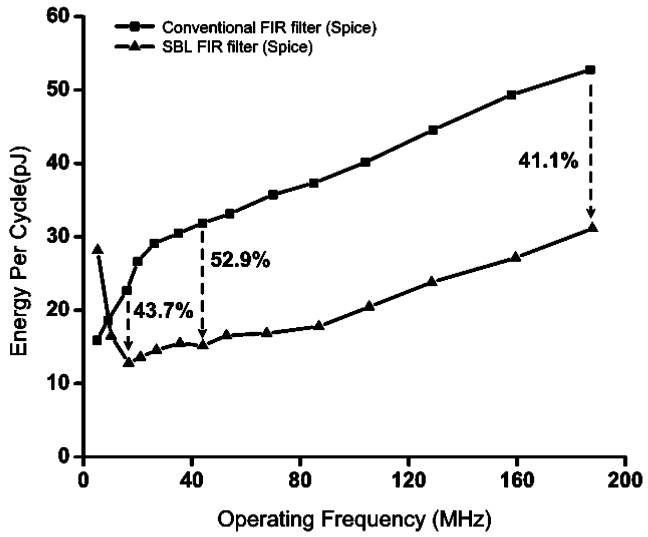

Fig. 11. Simulated energy consumption of conventional and SBL FIR filters.

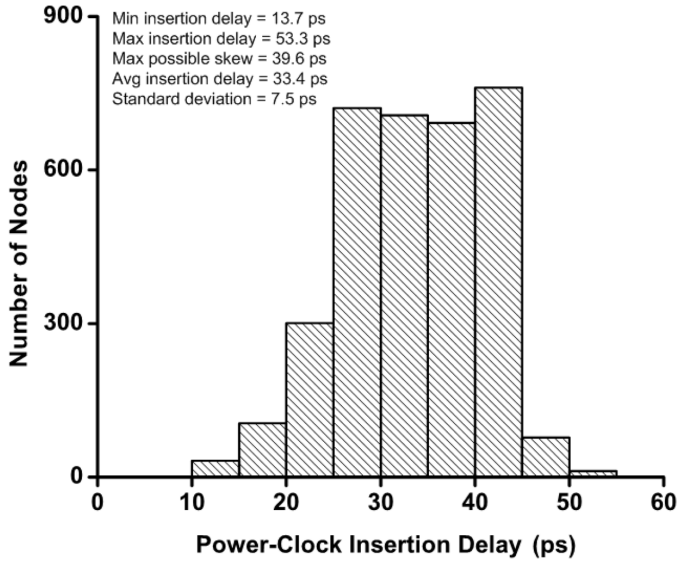

Fig. 12. Histogram of simulated power-clock insertion delays at a resonant frequency of 53.7 MHz.

up to 187 MHz. It also presents a comparison of measurement and simulation results, showing good agreement between the two, with relative discrepancy between measurements and simulations staying within 12% for operating frequencies ranging from 20 MHz to 187 MHz.

Two sets of measurements were obtained. In the first set, the supplies V_{CC} and V_{DC} were set equal to each other. In the second set, the two supplies were controlled independently. As shown in the table of Fig. 8, for both sets of measurements, the FIR test-chip achieves a maximum operating frequency of 187 MHz with all supplies set at levels below $V_{th,nmos} = 400$ mV. With the two supply values tuned independently, the test-chip achieves higher energy efficiency than with a single-supply setting.

Fig. 13 shows the per-cycle energy consumption of our test-chip for operating frequencies ranging from 5 MHz to 187 MHz. Data points are given for both single-supply and dual-supply settings. At each frequency point, the energy drawn from each supply is given separately, along with the total energy consumed. The different operating points are obtained by selecting off-chip inductors that yield a resonant frequency at that clock frequency. In all cases, the off-chip inductors were 0612 discrete devices that were mounted on the printed circuit board in proximity to the test-chip. The maximum operating frequency of 187 MHz was obtained with no external inductors, with the bondwires and package traces related to the clock generator providing all the parasitic inductance.

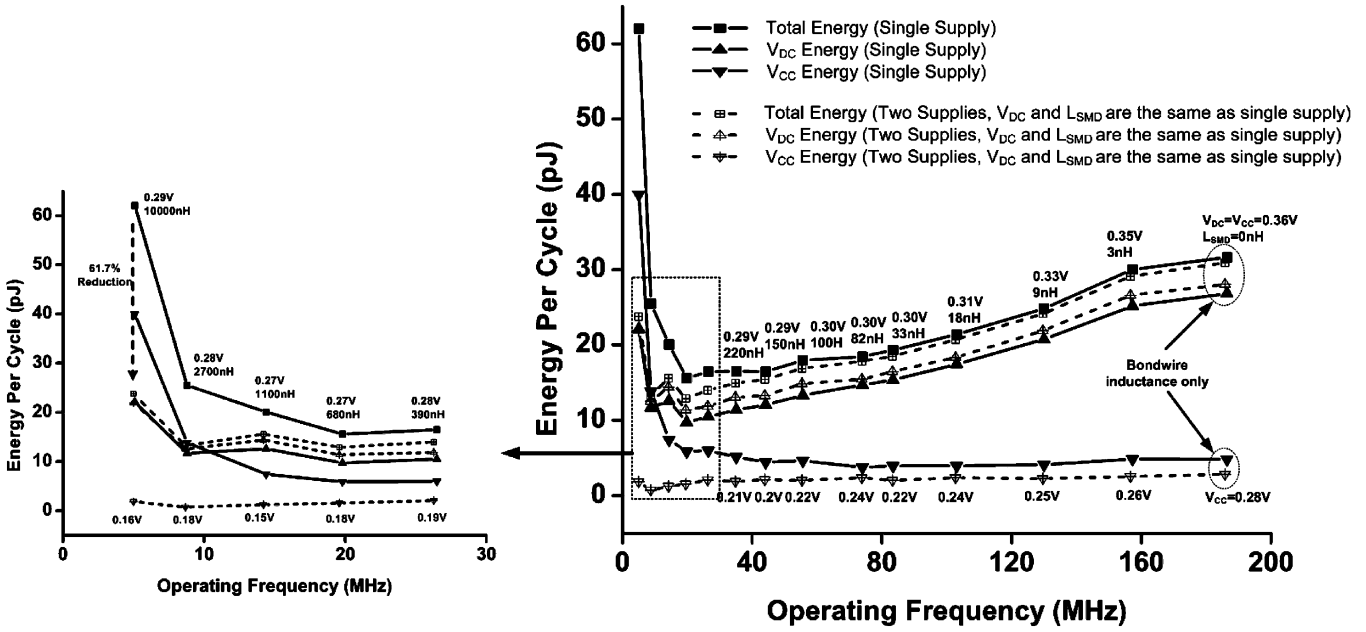

Fig. 13. Measured energy consumption versus operating frequency for SBL FIR filter (single supply and two supplies).

For each single-supply data point in Fig. 13, the corresponding voltage and inductor value are given above the data point. The data show that energy consumption is dominated by the energy drawn from the clock generator, with V_{DC} accounting for more than 80% of total energy consumption. As operating frequency decreases from the maximum operating point of 187 MHz, energy consumption decreases approximately linearly. The minimum energy point of 15.57 pJ per cycle is obtained at 20 MHz with $V_{CC} = V_{DC} = 0.27$ V and two off-chip inductors of 680 nH each. At this frequency, the recovery rate of the energy supplied through V_{DC} is approximately 89%, yielding a 17.37 nW/MHz/Tap/InBit/CoeffBit figure of merit. As operating frequency decreases below 20 MHz, total energy consumption increases at an accelerating rate, due to increasing crowbar currents, with V_{CC} to V_{SS} crowbar currents in the Logic stage quickly dominating, as evidenced by the cut-out that zooms on data in the 5 MHz to 30 MHz range.

The two-supply data points in Fig. 13 have been obtained by keeping the same V_{DC} and inductor values as in the single-supply case, and by decreasing V_{CC} by as much as possible while still achieving correct function. The overall trends observed are similar to the single-supply case. With V_{CC} reduced, the energy drawn from V_{DC} increases, since the power-clock draws more energy to boost the smaller potential difference at the output of the Logic stage. As expected, however, energy consumption in the Logic stage is significantly decreased. The impact of reducing V_{CC} is particularly pronounced as operating frequencies decrease below 30 MHz. Specifically, unlike the single-supply case where V_{CC}-related consumption starts increasing rapidly due to crowbar currents, with two separate supplies the energy consumption in the Logic stage remains relatively flat, even at frequencies as low as 5 MHz. Notice that at 5 MHz, where the crowbar current dominates, by separating V_{DC} and V_{CC}, we can reduce the energy consumption by 61.7%. The minimum energy point is obtained at 20 MHz with $V_{CC} = 0.18$ V, yielding a figure of merit equal to 14.4 nW/MHz/Tap/InBit/CoeffBit, a 17.1% improvement

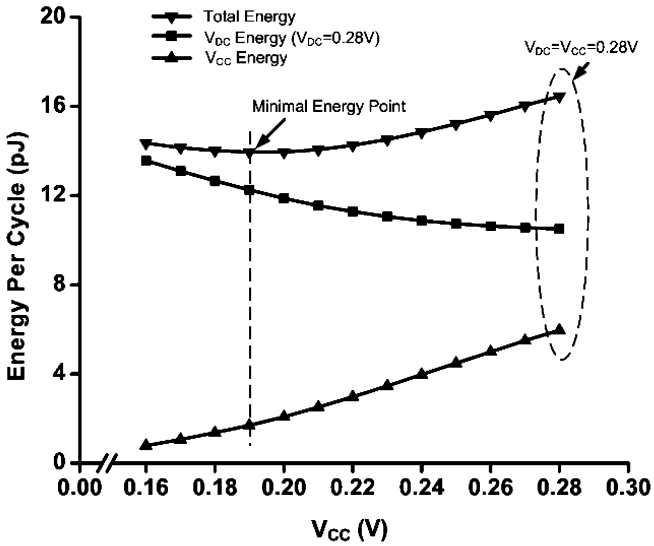

Fig. 14. Measured total energy consumption versus VCC for the SBL FIR when operating at 26.4 MHz with $V_{DC} = 0.28$ V.

over the single-supply case. At this frequency, the recovery rate of the energy supplied through V_{DC} is approximately 86%.

Fig. 14 gives a more detailed view of the trade-off between V_{CC}- and V_{DC}-related energy consumption. The rightmost data points inside the oval on the right-hand side give the energy consumption when a single supply is applied. By decreasing V_{CC}, V_{CC} energy decreases as expected, and V_{DC} energy increases gradually. Minimum total energy is obtained at $V_{CC} = 0.19$ V. When V_{CC} decreases below 0.19 V, total energy consumption increases due to larger V_{DC}-related energy.

The table in Fig. 15 summarizes the performance data for our FIR test-chip. For comparison purposes, it also includes published results for other FIR chips. Depending on operating frequency and number of supplies used, our SBL-based FIR test-chip achieves figures of merit that improve upon previous designs by a factor of at least 3X to 20X.

Paper	This Work			[6]	[8]	[9]
Design Type	14-tap 8x8 FIR			8-tap 8x8 FIR	8-tap 6x6 FIR	14-tap 8x8 FIR
Technology	0.13µm (RVT)			0.13µm (LVT)	0.18µm (RVT)	0.13µm (RVT)
Supply Voltage	0.27V	0.27V	0.36V	0.085V	1.8V	1.08V
2nd Supply	0.18V	N/A	N/A	Chip Dependent Body Bias	N/A	0.59V
Operating Frequency	20MHz	20MHz	187MHz	240Hz	275MHz*	1.01GHz
Power Dissipation	0.25mW	0.31mW	5.9mW	40nW	36mW	124mW
Figure of Merit (nW/MHz/Tap/In-Bit/Coeff-Bit)	14.40	17.37	35.31	325.52**	227.27**	133

* 550 MSamples/s with parallel architecture
** Derived from published results

Fig. 15. Performance table.

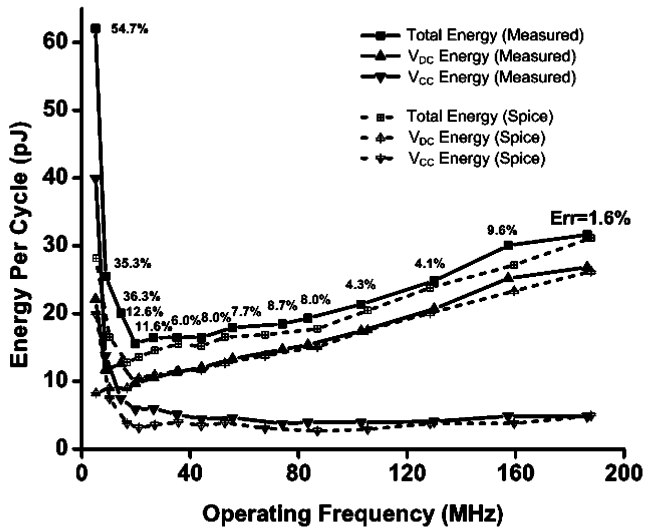

Fig. 16. Comparison of measured and simulated energy consumption for SBL FIR filter (single supply).

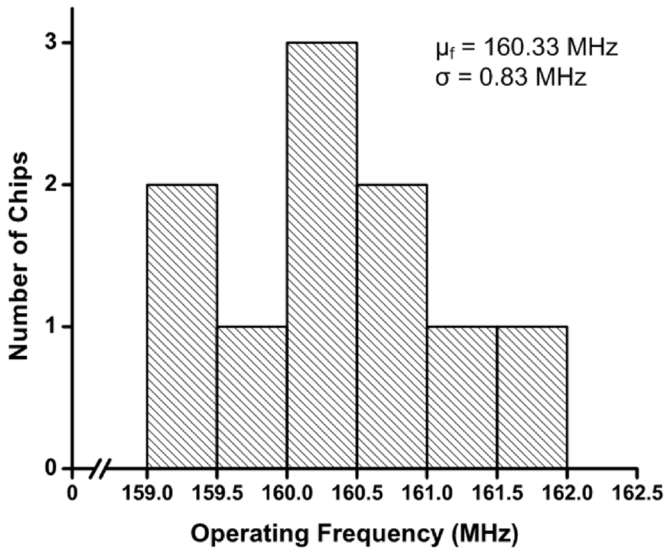

Fig. 17. Measured resonant frequency distribution at $\mathrm{V_{DC}} = \mathrm{V_{CC}} = 0.36$ V.

Beyond energy efficiency and performance, another question addressed by our experimental evaluation is the accuracy of the Spice simulation results presented in Section V. Fig. 16 gives simulation results under the conditions used to obtain measurements with a single supply. For operating frequencies in the 20 MHz to 187 MHz range, the discrepancy between simulations and measurements stays within 12%. At operating frequencies below 20 MHz, the energy consumption of the Boost stage starts increasing. This increase is not reflected to the same extent in the simulations. With voltage supply below 0.27 V, we conjecture that the increasing discrepancy between simulations and measurements is due to increasing model inaccuracies, due to the aggressively scaled voltage supply.

Another focus of our experiments was to determine the variability of resonant frequency across multiple test-chips. Fig. 17 shows the resonant frequencies of 10 test-chips when running free with $\mathrm{V_{DC}} = 0.36$ V and fixed 3 nH surface-mount inductors. Correct function has been validated for all 10 chips, with average resonant frequency $\mu_f = 160.33$ MHz and standard deviation $\sigma = 0.83$ MHz. The resonant frequency of these chips varies by $\pm 1\%$. Even with 3σ variation of 1.4 MHz; it is still within the $\pm 3\%$ tuning range of the clock generator circuit.

The results presented in this paper suggest that SBL is a promising approach for the implementation of regular datapaths with low energy consumption. To access the suitability and robustness of SBL for mass production, further evaluation would be required, including sensitivity to temperature and wafer-to-wafer process variation, device mismatch, and supply voltage variation.

VII. Conclusion

This paper introduces Subthreshold Boost Logic (SBL), a circuit family that is capable of operating at multi-MHz clock fre-

quencies using subthreshold supplies. Unlike subthreshold circuitry, in which computations are performed using subthreshold currents and clock frequencies are typically limited to sub-MHz levels, SBL gates are overdriven to operate in the linear region, achieving order-of-magnitude improvements in operating speed over subthreshold logic. Energy efficient operation is ensured through the use of aggressively-scaled DC supplies at subthreshold levels and by deploying charge recovery design techniques to boost these subthreshold supply levels by 3X to 4X.

To demonstrate the performance and energy efficiency of SBL, this paper also presents a 14-tap 8-bit finite-impulse response filter test-chip implemented using SBL. Fabricated in a 0.13 μm bulk silicon process with regular thresholds, the test-chip functions correctly for clock frequencies ranging from 5 MHz to 187 MHz, relying on two discrete off-chip inductors to boost the subthreshold supplies in an energy-efficient manner. Clock drivers are fully integrated and distributed across the entire clock network. With a single subthreshold supply set to 0.27 V, it achieves its most energy efficient operating point at 20 MHz, yielding a figure of merit equal to 17.37 nW/Tap/MHz/InBit/CoeffBit. With the introduction of a second subthreshold supply set to 0.18 V, energy consumption due to crowbar currents at clock frequencies below 30 MHz is significantly reduced. Maximum energy efficiency is improved by 17.1% and is achieved at 20 MHz, yielding 14.40 nW/Tap/MHz/InBit/CoeffBit. At maximum energy efficiency, energy recovery rates range from 86% to 89%, depending on the number of supplies. Based on Spice simulations of the SBL FIR and a fully-automatic static CMOS implementation of the same FIR architecture, the SBL design consumes 40% to 50% less energy per cycle in the 17 MHz–187 MHz range while incurring a 15% area overhead.

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