RF2 : A 1GHz FIR Filter with Distributed Resonant Clock Generator

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ABSTRACT

In this paper we present the design and experimental validation of RF2, a 1 GHz, two-phase resonant-clocked FIR filter test-chip with a distributed resonant clock generator and an on-chip inductor. RF2 is fabricated in a 0.13µm CMOS process and dissipates 124mW at resonance, with clock power accounting for only 16% of overall power. Implemented using a fully ASIC design flow, RF2 achieves 84% clock-power efficiency over CV^2f, the highest for any fully-integrated resonant-clocked chip. Resonating at 1.01GHz, RF2 reports the highest operating frequency for a resonant-clocked datapath to date.

INTRODUCTION

Increasing throughput and performance requirements have resulted in clock power remaining a major contributor to total power dissipation. By efficiently resonating the entire clock network capacitance using inductance, resonant-clocking techniques offer the opportunity for energy-efficient clocking, resulting in substantial reduction of overall power dissipation.

Previous work in the area involved the use of resonant clocks derived from off-chip inductors to drive flip-flops [1,2,3]. The poor slew of sinusoidal resonant clocks, however, degrades performance and robustness to variation in flop-based designs. Previous adiabatic techniques introduce additional resistance in the resonating clock network [1,2]. Another approach has been to resonate the global clock distribution network [5]. Such a mechanism, which is directed towards clock skew and jitter reduction, does not significantly impact clock power [6].

The basis for the design of RF2 is the key observation that latches are naturally suited to the design of resonant-clocked datapaths. Unlike flip-flops, latch-based systems can be designed so that their performance is nearly insensitive to the slew of resonant clock waveforms. Therefore, such a latch-based design methodology allows for resonant clocks to directly drive latches (with no clock buffers) without incurring performance degradation. RF2 also benefits from the time-borrowing afforded by latch-based design.

For robust and skew-tolerant operation, RF2 utilizes a two-phase clocking scheme driven by a distributed clock generator using a blip topology [7]. The two phases, along with appropriate latch design, achieve two non-overlapping latch transparency regions. The clock generator switches in RF2 are also driven by the resonant clock phases, resulting in increased energy efficiency. RF2 achieves 84% clock-power efficiency over CV^2f while driving 80pF of clock load. Compared to its conventional flop-based counterpart, RF2 drives a lower clock load, resulting in even higher relative clock-power reduction.

LATCH DESIGN

Fig. 1 shows transistor schematics of BLAT the resonant-clocked level-sensitive latch used in RF2. B-LAT is a modified Svensson latch implementation optimized for low T_{DQ} [7]. Post-layout simulations of B-LAT-X2 with 15fF load

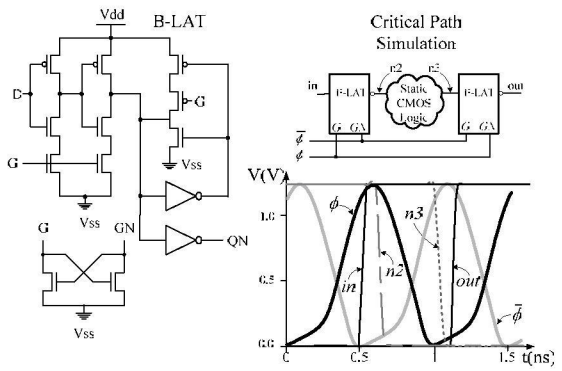

Fig. 1: BLAT schematics and pipeline implementation

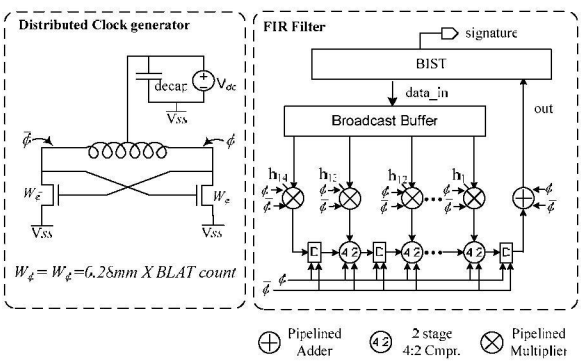

Fig. 2: RF2 block diagram

yield T_{DQ}=97ps with (E_{CK},E_{D+Q})=(0fJ,23fJ) per toggle. As a result, RF2 does not require deeper pipelines and therefore does not incur longer latencies than a corresponding conventional implementation. To avoid crossover current resulting from the poor slews of unbuffered resonant clocks, clocked transistors are incorporated within the logic stack. As seen in Fig.1, pipeline stages in RF2 are designed so that critical data arrives at the latch when the latching clock is nearly at V_{dd}, ensuring full gate overdrive for clocked transistors in B-LAT, thus maximizing performance. Data arriving early at the latch input leaves the latch earlier despite the voltage-dependent T_{DQ} delay, providing additional timing slack to the next pipeline stage. Our methodology can also be shown to work effectively in designs with feedback loops. Post-layout simulations at the 3σ process corner also demonstrate that even with zero logic delay, the setup in Fig. 1 is race-immune at up to 290ps of clock skew. RF2 exhibits low skew, bounded by its insertion delay of 15ps.

RF2 DESIGN

Fig. 2 shows a block diagram of RF2, a 14-tap 8-bit transpose-type FIR filter with BIST, designed for a target frequency of 1GHz. In each tap, pipelined multipliers merge partial products to generate sum and carry vector pairs. These

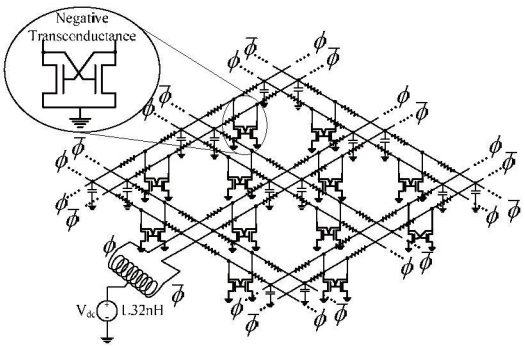

Fig. 3: Distributed clock generator and network

pairs are then merged with clock-delayed multiplier outputs from the previous tap using 4:2 compressors. The final vector-merge adder is implemented as a pipelined carry-save adder. The BIST generates a pseudo-random number sequence, processes the filter output to generate a signature waveform, and captures the state of the signature analyzer at a user-defined time. A center-tapped symmetric on-chip inductor is used to achieve efficient *LC* resonance with the distributed parasitic capacitance of the clock network.

Unlike previous work, RF2 does not use a separate clock generator block. Instead, the cross-coupled NMOS switches providing the required negative trans-conductance are embedded within the B-LAT latch, as shown in Fig. 1. Using a distributed clock generator reduces local clock skew and simplifies design.

A simplified representation of the clock generator and network is illustrated in Fig. 3. In RF2, distributed gain elements drive a lower level clock grid, connected to the inductor through a 2-level H-Tree.

To demonstrate the efficiency of the proposed design methodology, RF2 was implemented in a fully automated ASIC design flow. A gate-level netlist was obtained from Verilog using latch-based synthesis. Physical design was performed using auto place and route tools. In particular, the clock network was automatically generated from standard cell and power route placements using an in-house tool.

MEASUREMENT RESULTS

To investigate variation in the resonant frequency of RF2 across multiple chips, the resonant frequencies of 10 randomly selected chips were measured. All 10 chips were tested successfully with μ_f=1.012GHz and σ_f/μ_f=0.012.

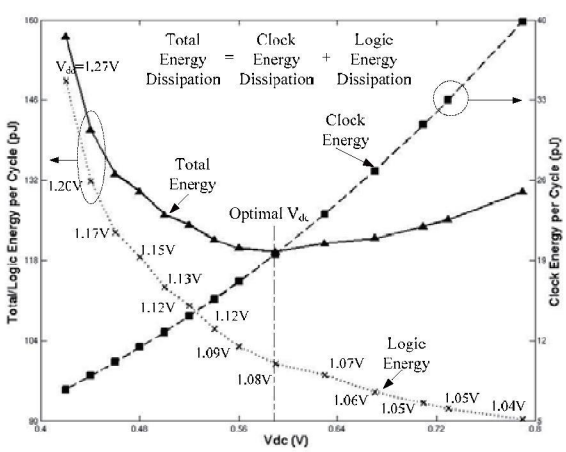

Fig. 4: Clock, Logic, and Total power energy per cycle vs. V_{dc}

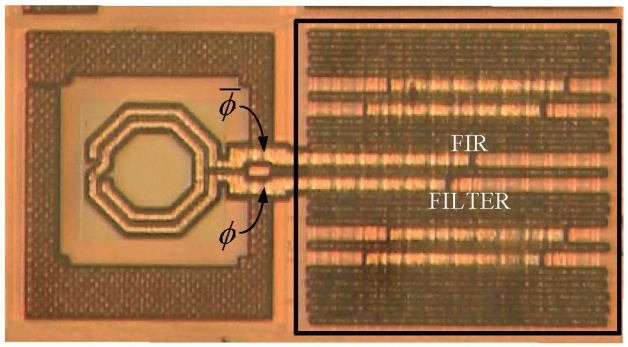

Fig. 5: RF2 microphotograph

Clock insertion delays in RF2 are insensitive to V_{dd} variation and depend only on interconnect delay. Performance degradation in RF2 due to voltage scaling is therefore less pronounced compared to conventionally-clocked designs. Furthermore, efficient clocking in RF2 allows for additional supply-voltage scaling by compensating for the increased logic delay with higher clock amplitude.

Fig. 4 shows the clock, logic and total energy-per cycle dissipation vs. the clock supply voltage V_{dc}. The operating frequency of the design is 1.01GHz. At each value of V_{dc}, the supply voltage V_{dd} was scaled to achieve the minimum total power dissipation. For lower values of V_{dc}, a higher supply voltage is required due to lower clock amplitude. Increasing V_{dc}, increases the clock amplitude, allowing for lower total energy dissipation through V_{dd} scaling. Beyond the optimal value of V_{dc}, the supply voltage scaling afforded by improved latch performance cannot compensate for the increasing clock power dissipation, resulting in an increase in total power dissipation. Driving 76pF of clock load, RF2 achieves 84% clock-power efficiency over CV^2f, with an estimated system quality factor Q of 5. Clock power in RF2 is 19.9mW, accounting for only 16% of the overall 124mW chip power. At 133nW/MHz/Tap/inBit/coeffBit, RF2 features the lowest figure of merit for digital FIR filters published to date. A chip microphotograph of RF2 is shown in Fig 5.

CONCLUSION

This paper describes RF2, a robust two-phase latch-based resonant-clocked FIR filter implemented using a fully-automated ASIC design flow. RF2 demonstrates that a latch-based methodology is natural to resonant clocked design. The distributed clock generator featured in RF2 simplifies design and provides better control of local clock skew. At its resonant frequency of 1GHz, RF2 dissipates 124mW, achieving 84% energy efficiency over CV^2f. RF2 is the first GHz-class implementation of a resonant-clocked datapath.

REFERENCES

1. Athas W. et al. "Clock-powered CMOS VLSI graphics processor for embedded display controller application," ***ISSCC***, pp. 296-297, Feb 2000.
2. Ziesler C. et al. "A 225MHz resonant clocked ASIC chip," ***ISLPED***, pp. 48-53, Aug 2003.
3. Drake A. et al. Resonant Clocking Using Distributed. Parasitic Capacitance", ***JSSC***, vol39, pp1520-1528, 2004 .
4. Chan S. et al. "A 4.6GHz resonant global clock distribution network," ***ISSC***, pp.42-43, Feb 2004.
5. Restle P.J et.al "A clock distribution network for microprocessors", ***JSSC***, vol. 36, pp. 792-799, May 2001.
6. W. Athas et. al, "A resonant signal driver for two-phase almost-nonoverlapping clocks", ***ISCAS***, May 1996, pp129-132.
7. Yuan J. and Svensson C. "High-speed CMOS circuit technique," ***JSSC***, vol.24, pp. 62-70, Feb 1989.