A 0.8-1.2GHz Single-Phase Resonant-Clocked FIR Filter with Level-Sensitive Latches

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ABSTRACT

In this paper we present the design and experimental validation of RF1, a 0.8-1.2GHz frequency-scalable, resonant-clocked FIR filter test-chip with level-sensitive latches. Designed using a fully automated ASIC flow, RF1 was fabricated in a 0.13μm CMOS process with an on-chip inductor and clock generator. At its resonant frequency of 1.03GHz, RF1 dissipates 132mW, with clock power accounting for only 10.8% of total power dissipation. Resonating 42pF of clock load, RF1 achieves 76% clock-power efficiency over CV^2f.

I. INTRODUCTION

Higher operating frequencies and the associated increase in the clock loads of digital circuits are responsible for the growing importance of clock related power dissipation. Resonant clocking is an attractive option for clock power reduction [1], [2], [3]. By achieving sinusoidal clock waveforms from LC resonance, the resulting I^2R power loss in the clock network resistance is substantially lower than the traditional CV^2 dissipation encountered in conventional clocking. In addition to lower clock power, resonant clocking provides other important characteristics, including reduced jitter.

Previous work has provided evidence in support of low-power resonant clocks. Ziesler et al. have demonstrated a 225MHz ASIC for the discrete wavelet transform that uses a single-phase resonant clock to drive adiabatic flip-flops [1]. Off-chip inductors were used, however, and the use of adiabatic techniques degraded flip-flop performance. Recent work on the implementation of resonant-clocked designs has been targeted towards using resonant clocks to synchronize flip-flops using non-adiabatic techniques, thereby reducing network impedance and improving clock network efficiency. The resulting resonant-clocked system consists of conventional CMOS logic pipelined with resonant-clocked timing elements. Drake et al. have demonstrated a 146MHz two-phase resonant clock network to drive an array of master-slave flip-flops [2]. Chan et al. have proposed the use of resonant clocks for global clock distributions to reduce jitter [3], [4] but also have the added benefit of reducing global clock distribution power.

In this paper, we describe an FIR filter test-chip that uses resonant clocking and level-sensitive latches to operate with minimal clock power without performance degradation. The resulting clock architecture of RF1, shown in Figure 1, consists of conventional CMOS logic pipelined with resonant-clocked level-sensitive latches. A key contribution of our work is the observation that level-sensitive latch-based design is naturally suited to resonant clocking due to its robustness to performance degradation and timing variation in the presence of poor clock slew.

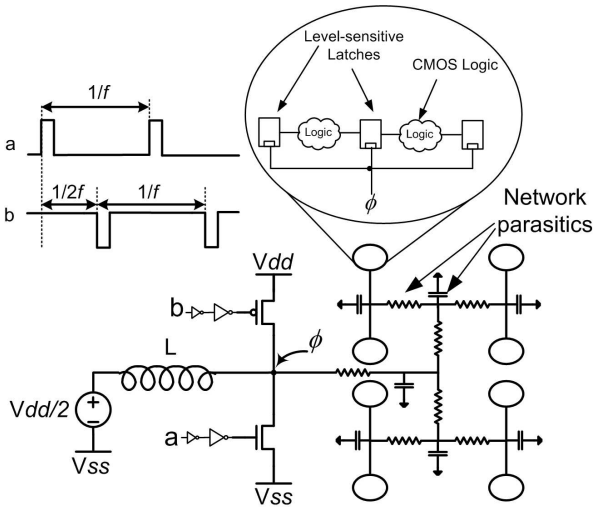

Fig. 1. Resonant clock architecture in RF1

RF1 is the first implementation of a single-phase latch-based resonant-clocked datapath and achieves high performance with greater energy-efficiency than its conventionally-clocked counterparts. Such efficient, high performance operation is achieved through several key distinguishing features: (1) The entire clock network, including the local clock distribution and the clocked transistors of timing elements is "resonated". That is, RF1 does not contain any clock buffers, thus preventing the pruning of the resonant clock network and maximizing the amount of capacitance that can be resonant-clocked. (2) By using a novel Resonant Clocked Latch-based (RCL) design methodology, RF1 avoids the performance degradation arising from poor clock slew in resonant clock waveforms. Instead, the timing characteristics of latches in RF1 are determined by the the full-rail clock amplitude of the resonant clock.

Another distinguishing feature of RF1 is its frequency-scaling capability without any alteration of the circuit parameters in the resonant network. Specifically, as shown in Figure 1, frequency scaling is achieved by setting the reference

clock frequency, f, of the periodically driven resonant clock generator to the desired operating frequency.

Running at clock speeds of up to 1.2GHz, RF1 achieves the highest operating frequency for a resonant-clocked datapath. At its resonant frequency of 1.03GHz, RF1 dissipates 132mW, corresponding to a FIR filter figure of merit of 143nW/MHz/Tap/InBits/Coeff-Bits. With 42pF of clock load, RF1 dissipates 76% less power than CV^2f. Through the design of an efficient clock network and resonant-clock aware latches, RF1 requires no additional pipeline stages– A conventional ASIC implementation of the same FIR filter using an industrial standard-cell library yields an identical computational latency. The RCL methodology used in RF1 also demonstrates that fully automated ASIC implementations of resonant-clocked designs are possible. Furthermore, the use of resonant-clocked latches in digital circuits does not preclude the implementation of other energy minimization techniques in the conventional CMOS logic part of the design.

The remaining sections are organized as follows. Section II describes the latch and pipeline architecture of RF1. The design of the 14-tap FIR filter is discussed in Section III. Key experimental results are provided in Section IV and conclusion and future work are discussed in Section V.

II. Latch Based Design

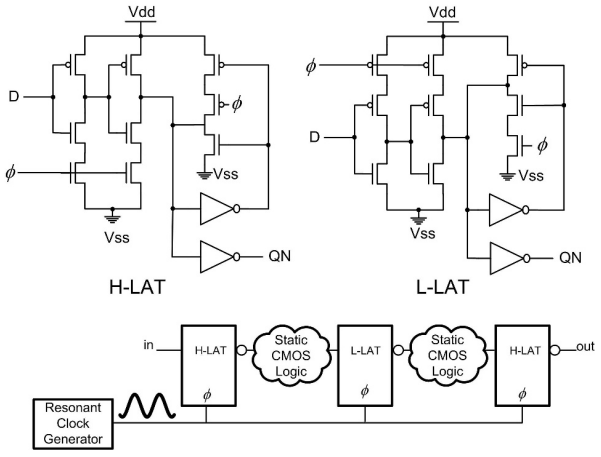

Fig. 2. RF1 H-LAT and L-LAT schematics and interleaved implementation for single-phase datapaths

RF1 achieves substantial clock power reduction by avoiding clock buffers in the resonant network, thereby achieving resonance in the entire clock capacitance. As a result, clocked transistors in the latch are driven by sinusoidal waveforms, impacting the design of latches. Consequently, latch design plays a central role in the implementation of RF1. Latch requirements include (1) the design of true-single phase latches, (2) low $D-Q$ delay despite sinusoidal clock waveforms with poor slew, and (3) avoiding crowbar current in latches due to gradually transitioning sinusoidal clocks. Therefore, although the use of latches in conventionally clocked designs is well known, the benefits and challenges from their use in resonant-clocked systems have yet to be explored.

To operate with a single clock phase, RF1 pipelines consist of interleaved latches, which are transparent during opposite polarities of the resonant clock. Figure 2 shows circuit schematics for the level-sensitive high (H-LAT) and low (L-LAT) latches in RF1. H-LAT and L-LAT are Svensson latch implementations that have been optimized for low T_{DQ}. From post-layout simulations, H-LAT (L-LAT), driving 15fF of load achieves T_{DQ} of 99ps (106 ps) with a total dissipation of 24fJ (22fJ) per toggle. In both designs, the clock switching power in the latch is zero. Clock connections are incorporated within the logic stack so that the pulldown clocked transistor is in series with a complementary logic stack, avoiding the potential increase in crowbar current due to large rise and fall times of the clock.

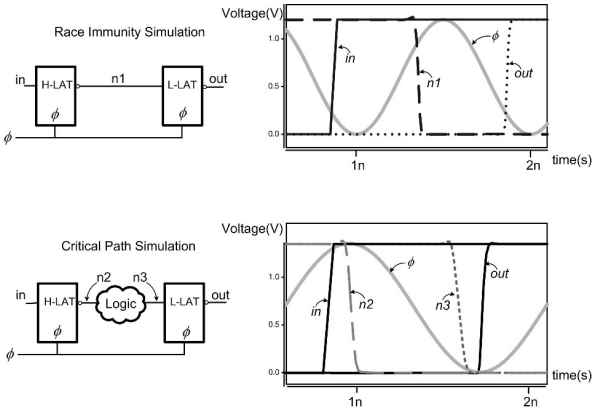

Fig. 3. RF1 race immunity and critical-path simulations

Figure 3 shows waveforms obtained from simulations of interleaved latches in possible race and critical path scenarios at 1GHz. In the race scenario, data latched by H-LAT during the rising transition of the clock does not race through L-LAT during the same transition, which latches the data only in the subsequent transparent window. From 1GHz post-layout simulations of RF1 at the 3σ process corner, the race setup in Figure 3, with zero logic delay is immune to race at clock skews of up to 160ps. Given that clock skew is bounded by the insertion delay of the clock network, and that the insertion delay of RF1 is estimated to be 10ps, RF1 comfortably satisfies the clock skew requirement.

Despite the apparent "overlap" between the transparency windows of the two latches, RF1 comfortably maintains race-immunity due to the increased T_{DQ} in the overlapping transparency regions of the latches. Figure 3 also shows that the pipeline signals on the critical path are designed to arrive at H-LAT (L-LAT) while the resonant clock is at nearly VDD (VSS). For such designs, latch performance is determined by T_{DQ}, which depends on the voltage level of the clock. It should be noted that for circuits exhibiting feedback loops, data arrival times will self-adjust to converge so that critical data arrives during regions of low T_{DQ}. For critical paths that do not consist of loops, critical data arriving at the latch input earlier than the peak of the clock will, despite the increased T_{DQ}, depart from the latch earlier. Consequently,

data arriving early in the clock cycle will provide additional timing slack to the next stage, regardless of the increased T_{DQ} of the latch. Our novel design methodology for implementing resonant-clocked latch-based designs also includes a static timing analysis framework which enables the analysis of data arrival and departure times at latches by including the effects of variable T_{DQ} in order to guide logic design for cycle sharing.

III. RF1 Design

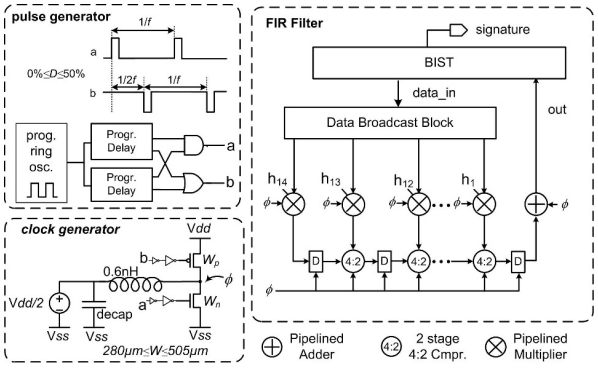

Fig. 4. RF1 block diagram

A block diagram of RF1 is shown in Figure 4. RF1 is a 14-tap, 8-bit transpose-type FIR filter with BIST, targeted to resonate at 1GHz. Pipelined multipliers in each tap scale the input data according to the programmable coefficients of the filter. The multiplier product in each tap then merged with cycle delayed products from the previous taps using 4:2 compressors. The final vector merge addition in each cycle is replenished using pull-down and pull-up transistors. In every cycle, when the clock approaches 0V (V_{dd}), the pull-down (pull-up) transistors conduct, resulting in an RL current buildup in the inductor. The resulting energy stored in the magnetic field of the inductor is used to replenish the lost energy and sustain oscillation at the full clock amplitude. To minimize switching losses, the duration of time that the clock generator switches conduct is kept short. This duration is controlled by periodic pulses a and b generated by the pulse generator block. These pulses drive the clock generator switches that determine the rate at which energy is replenished into the system and therefore the operating frequency of RF1. For efficient operation, the pulse frequency should match the natural frequency f_n of the design:

$$f_n = \frac{1}{2\pi}\sqrt{\frac{1}{LC} - \zeta^2}, \tag{1}$$

where L and C are the inductance and capacitance of the oscillating system respectively, and ζ is its damping factor. The capacitance of the oscillating system is made up of the clock tree parasitic capacitance and the clock input capacitance of the level-sensitive latches used in the design.

The switch width and pulse duty cycle significantly impact clock network efficiency. The use of wider clock generator switches reduces switching losses at the expense of conventional energy dissipation incurred in driving wider switches. Wider pulse widths increase the duration of time over which energy is provided to the inductor, requiring smaller switches but incurring higher switching losses. To explore efficient regions of clock generation, programmable switch widths in the range W_p=(0μm, 950μm) and W_n=(0μm, 630μm)and pulse duty cycles in the range (0,50%) were implemented. A programmable ring oscillator, from which pulses a and b are derived, is used to enable frequency tuning around the resonant frequency. The use of pMOS switches in the clock generator also provides the added flexibility of operating without an additional $Vdd/2$ power supply.

The physical design of the clock network in RF1 was guided by the need for low network resistance from the root of the network (connected to the inductor) to the leaf terminals for maximum energy efficiency. Low network resistance also limits the voltage drop at the leaves and the clock skew in the network. A 2-level H-tree was implemented to distribute the clock globally. A lower-level clock grid was subsequently employed to reduce network impedance and clock skew. The wire widths of the H-tree were chosen to provide minimum energy dissipation in the clock for the given clock load. The integrated inductor used in RF1 is a single-turn two-layer winding providing an inductance of 0.56nH.

RF1 was implemented in a fully-automated ASIC design flow. Design entry was performed in Verilog HDL. Latch-based synthesis and automatic place-and-route (APR) tools were used to perform synthesis and physical design respectively. Switch level simulation and static timing were used to verify the design.

IV. Measurement Results

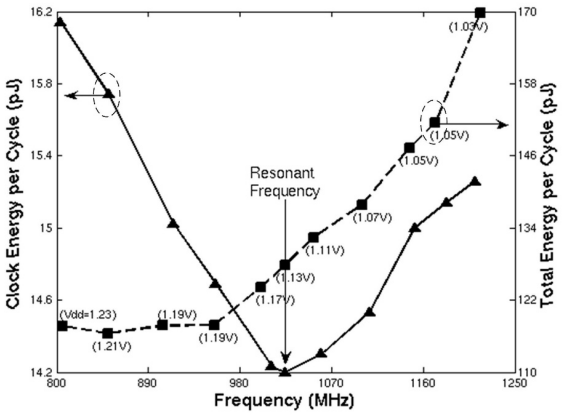

Fig. 5. Clock and total energy dissipation per cycle vs. operating frequency

Figure 5 shows measured clock and total energy dissipation per cycle vs. operating frequency. The clock energy curve is obtained for V_{dd} = 1.2V, (W_n,W_p) = (225μm,0), and D = 20%. The minimum clock energy point at 1.03GHz indicates the resonant frequency of the design. The lowest achievable per-cycle energy dissipation of the clock (clock network + clock

generator) in this configuration at resonance is 14.3pJ. The total energy plot corresponds to the lowest energy dissipation of the design at the operating frequency over all possible values of W_n, W_d, D and V_{dd}. While the energy dissipation of the clock increases away from the natural frequency, the total energy dissipation of RF1 decreases with a reduction in frequency. This decrease in overall power dissipation is due to the power reduction obtained by voltage-scaling RF1 at lower frequencies. At higher frequencies, both logic and clock power increase, resulting in increased power dissipation.

Technology	0.13μm CMOS RF
Taps, in/out/coeff bits	14, 8/20/8
Gate count	22K
H-LAT/L-LAT count	2752/2760
Total/active area	1mm^2/0.5mm^2
Frequency range	800MHz–1.2GHz
Supply voltage range	1.03V–1.21GHz
Resonant frequency	1.03GHz
Estimated Q	3.8
Energetics @ resonance	
Supply voltage (V)	1.13
Clock network efficiency	76%
Total/logic/clock power diss. (mW)	132/ 117.8/ 14.2
Total/logic/clock energy (pJ)	128.2/ 114.4/ 13.8
Power/MHz/Tap/InBits/Coeff-Bits	143nW
Input switching activity	0.5

Fig. 6. RF1 statistics and performance

Figure 6 summarizes the measurement results obtained from RF1. At its natural frequency of 1.03GHz, RF1 achieves correct operation with V_{dd}=1.13V. Although RF1 is a pipelined ASIC implementation of an FIR filter in 0.13μm CMOS, its clock power dissipation is 14.2mW, accounting for only 10.8% of overall power.

The clock network efficiency of RF1 over an identical conventionally switching load at the same voltage swing is 76%. Despite the use of wide top-level metal wires and a lower-metal clock grid, the 42pF of clock network capacitance (including the 5.5K latches) in RF1 is substantially lower than a conventional ASIC implementation of the same FIR filter using an industrial standard-cell library. Therefore, the percentage clock power reduction in RF1 is even higher compared to its conventional counterpart.

At its resonant frequency, the normalized power dissipation of RF1 is 143nW/MHz/Tap/InBits/Coeff-Bits. This figure of merit compares favorably with previously published work using conventional clocking, even though the numbers presented in Figure 6 correspond to a relatively high data input switching activity of 0.5 [5], [6], [7]. A chip microphotograph of RF1 is shown in Figure 7.

V. Conclusions

In this paper, we have presented RF1, a single-phase resonant-clocked 8-bit 14-tap digital FIR filter with an on-chip inductor that operates at frequencies of up to 1.2GHz. The frequency-scalability of RF1 is achieved without altering

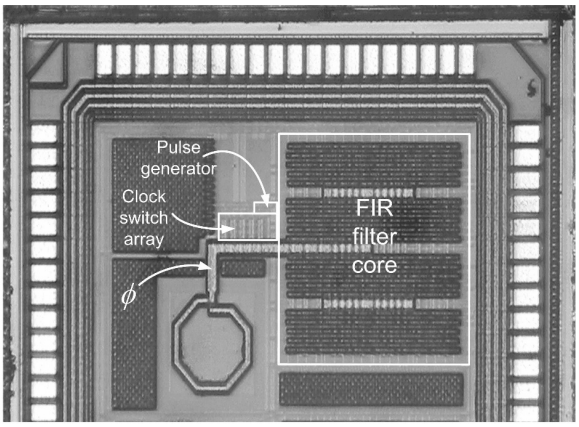

Fig. 7. Chip microphotograph of RF1

circuit parameters of the resonant network. In RF1, the entire clock network up and including the clocked transistors in the latches, is resonant clocked. The latches designed for the resulting sinusoidal clock waveforms exhibit D-Q delays comparable with conventional latches. At its natural frequency of 1.03GHz, RF1 dissipates 143nW/MHz/Tap/InBits/Coeff-Bits, with clock power dissipation accounting for only 10.8% of the total 132mW power dissipation. RF1 achieves 76% clock-power efficiency over CV^2f.

RF1 demonstrates that the RCL resonant-clocked latch-based design methodology can yield energy-efficient designs with identical latency and throughput in comparison with their conventional counterparts. Furthermore, the successful deployment of the RCL methodology for the design of RF1 demonstrates that latch-based design can be implemented using a resonant clock in a fully automated ASIC design flow.

VI. Acknowledgments

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