# A Resonant-Clock 200MHz ARM926EJ-S™ Microcontroller

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## ABSTRACT

An ARM926EJ-S™ microcontroller with a fully resonant clock distribution network and 16KB data and instruction caches has been implemented in 130nm bulk silicon. Workloads execute successfully across process and temperature corners, and at room temperature, typical-process chips run at clock speeds up to 200MHz with 1.2V supply. At resonance, the microcontroller core dissipates 0.23mW/MHz, recovering 85% of the energy in its clock distribution network. Total power savings range from 20% to 35%, depending on application workload and computation profile.

**Keywords:** energy-efficient processors, embedded computing, mobile computing.

## 1. INTRODUCTION

Resonant clocking can reduce clock power and timing uncertainty in digital systems. Using inductance to resonate the parasitic capacitance of the clock node, a resonant-clock network achieves energy-efficient operation by recycling the energy used to charge the clock node each clock cycle. Timing uncertainty is reduced due to the elimination of clock buffers from the clock distribution network.

An early clock-powered microprocessor design was presented in [1]. Resonant-clocked datapaths with off-chip inductors and clock speeds in excess of 100MHz were presented in [5, 9]. GHz-speed datapaths with on-chip inductors and resonant clock distribution networks were presented in [6, 8]. Those early datapaths did not include any memory arrays, however, and their resonant clock networks were not interfaced with conventional clock domains. An implementation of the IBM Cell processor with resonant clocking was described in [3]. In that design, however, the application of resonant clocking was limited to global clock distribution, without driving flip-flops, resulting in limited overall power savings. Resonant clocking for GHz-speed global clock distribution was investigated in [2, 4]. A high-speed IO cell with resonant clocking was described in [7].

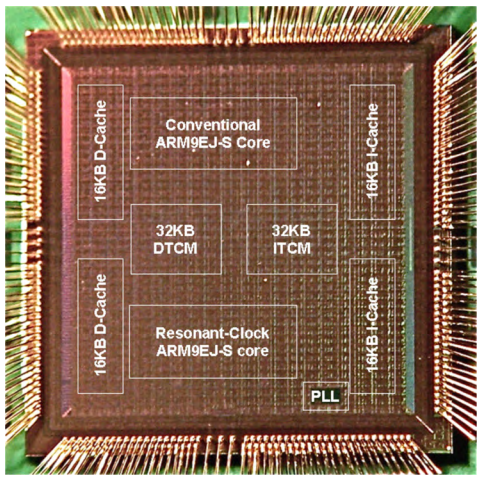


Figure 1: Die microphotograph

This paper presents an ARM926EJ-S™ microcontroller chip with a resonant clock distribution network that has been implemented in a commercial 130nm bulk-silicon process. A microphotograph of the chip is shown in Fig. 1. This chip is the first commercial-strength processor that deploys resonant clocking across its entire clock distribution network, using an off-chip inductor to resonate the parasitic clock capacitance from the root of the clock network and all the way to its flip-flop clock pins. Moreover, this chip provides the first-ever demonstration of interfacing between the resonant clock network with the conventional buffered clock networks that are used to clock the on-chip caches, and tightly-coupled memories.

Functional validation and performance evaluation of the resonant-clock ARM926EJ-S™

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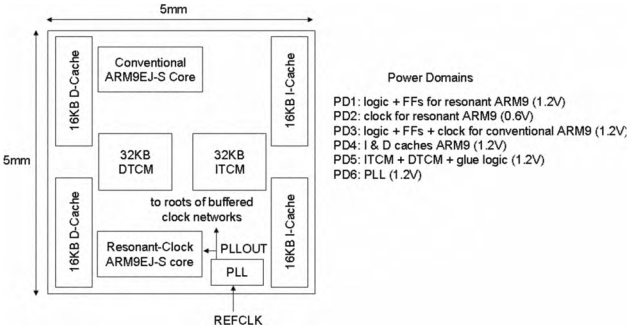


Figure 2: Chip block diagram

has been performed on a standard ARM evaluation board across process and temperature corners. Typical process-corner chips achieve clock speeds up to 200MHz with 1.2V supply at room temperature, while fast process-corner chips achieve clock speeds in excess of 250MHz. Correct operation under dynamic frequency scaling was also validated, with typical process-corner chips achieving correct operation for clock frequencies in the 100MHz to 200MHz range.

Compared to a conventional buffered-clock implementation of the same microcontroller that was designed separately from the same netlist and was fabricated on the same die, the resonant-clock design achieves 85% lower power on its clock network. Total power savings of the resonant microcontroller (clock, flip-flops, logic, caches) range from 20% to 35%, depending on application workload and computation profile.

## 2. CHIP OVERVIEW

Fig. 2 shows the block diagram of the die, which includes a resonant-clock ARM9EJ-S core, 16KB D-Cache and 16KB I-Cache for the resonant-clock core, a conventional ARM9EJ-S with a buffered clock distribution network, 16KB D-Cache and 16KB I-Cache for the conventional core, a 32KB tightly-coupled memory for instructions (ITCM), a 32KB tightly-coupled memory for data (DTCM), a JTAG boundary scan controller, and glue logic for selecting between the two cores. Each core communicates with off-chip peripherals over a standard AHB bus. A reference clock REFCLK is provided by the board to an on-chip PLL which multiplies it to obtain the PLLOUT clock signal that is used as the frequency reference of the resonant and buffered clock networks. Both ARM9EJ-S cores were fully synthesized using a reference flow and a commercial standard-cell library. All caches were generated using a commercial memory compiler and are clocked using a conventional buffered clock network. To enable monitoring of the various sources of power consumption in the chip, six distinct power domains PD1—PD6 are used to supply power to various sub-systems of interest, as listed in Fig. 2.

The 100pF clock network of the resonant-clock ARM9 is driven using an on-chip clock generator, as shown in Fig. 3. A pull-down NMOS at the root of the clock network is switched using RESCLKCTL, a delayed version of PLLOUT with programmable duty cycle from 10% to 50%. In conjunction with a package-mounted off-chip 0603 discrete inductor connected between the root of the resonant clock network and an external Vdd/2 supply, the periodically-switching NMOS generates a clock waveform RCLK of sinusoidal shape that is locked to the reference signal PLLOUT and swings between GND and Vdd at the same frequency as PLLOUT. The buffered clock network for the memory arrays (caches and

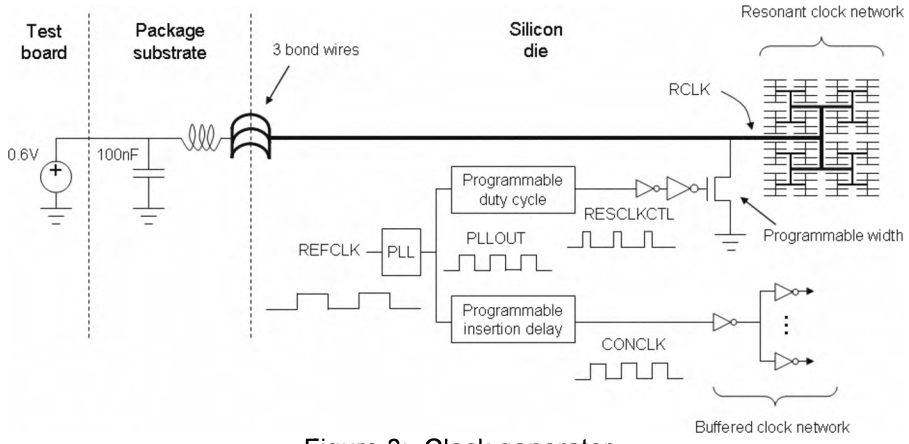


Figure 3: Clock generator

TCMs) and peripheral logic is driven by CONCLK, a delayed version of PLLOUT whose phase is adjustable from 2ns to 8ns to allow for matching the insertion delay of the resonant clock distribution network. To provide for sufficient replenishing of clock energy, the size of the NMOS is programmable from 50µm to 450µm, ensuring that the clock reaches steady-state within 3 cycles. The on-chip clock generator is connected to the off-chip inductor using 3 parallel bond wires, reducing parasitic inductance and resistance.

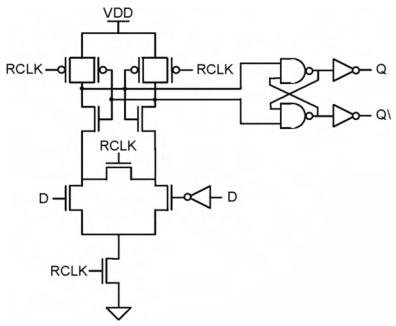

Figure 4: Sense-amplifier flip-flop used

The resonant clock is distributed using an all-metal hierarchical network. Worst-case clock skew between any pair of leaves in the resonant clock network is 21ps, based on simulations of the extracted clock network. Insertion delay from the root to the leaves of the resonant clock network is 60ps. To enable fast operation and reduce flip-flop crowbar current, sense-amplifier based flip-flops are used, as shown in Fig. 4.

To conform to the ARM specification for generic microcontroller test-chips, a standard 352-pin BGA package is used. A photograph of the package is shown in Fig. 5. The package includes a 4mm trace from the lead-frame to the 0603 inductor mounting site, facilitating the retrofitting of different inductors even in the presence of die encapsulation. An additional on-package mounting site is also provided for a Vdd/2 0603 bypass capacitor.

## 3. MEASUREMENT RESULTS

The performance of the resonant-clock ARM926EJ-S is summarized in the table of Fig. 6. Correct function was validated at FF/TT/SS process corners and -25˚C/25˚C/125˚C, respectively. At 25˚C, TT chips run at clock speeds up to 200MHz, and FF chips reach a 250MHz clock limit dictated by the maximum frequency of REFCLK from the board. In all cases, the maximum clock speed of the resonant-clock microcontrollers matched or exceeded the speed of their conventional counterparts on the same die.

Running without caches on a microcontroller application dominated by polling/updating of board peripherals, the ARM9EJ-S core dissipates 0.23mW/MHz when resonating at 125MHz using an 11nH inductor that yields overall Q > 10. Running the more compute-intensive Dhrystone benchmark application with caches fully enabled, total power consumption, inclusive of cache power, increases to 0.42mW/MHz. Compared to the conventional ARM926EJ-S on the same die, the resonant-clock microcontroller achieves equal or higher clock speeds and dissipates 20% to 35% lower total power, depending on which application is run.

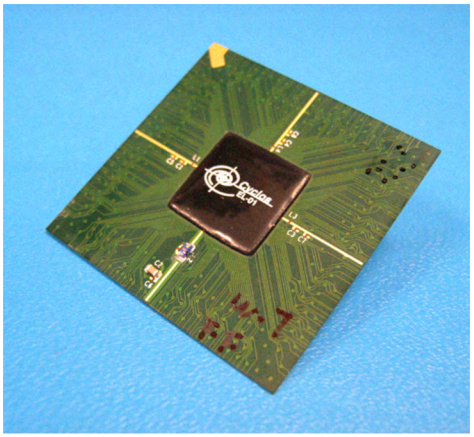
Figure 5: Package with encapsulated die

| | |
|---|---|
| Process | 130nm, 8 levels Cu, Regular Vt |
| I / D-Cache | 16KB / 16KB |
| I / D-TCM | 32KB / 32KB |
| Maximum clock speed | 200MHz, typical, 25 ˚C<br>250MHz+, fast, 25 ˚C<br>150MHz, slow, 125 ˚C |
| Power @ 125MHz resonance with 11nH inductor | |
| Microcontroller application | |
| Core (logic + FFs + clock) | 0.23mW/MHz |
| Dhrystone | |
| Core (logic + FFs + clock) | 0.28mW/MHz |
| Core + Caches | 0.42mW/MHz |

Figure 6: Resonant-clock ARM926EJ-S statistics and performance.

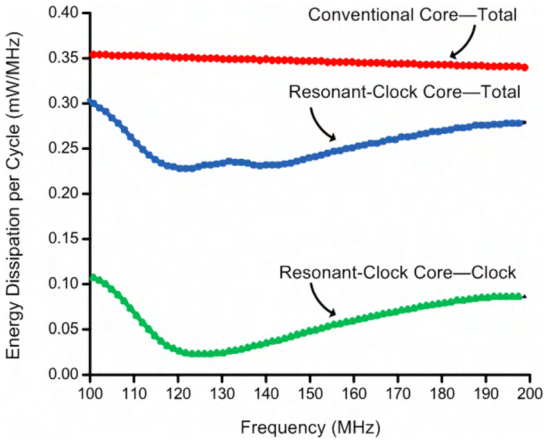


Figure 7: Energy dissipation per cycle vs. clock frequency under dynamic frequency scaling

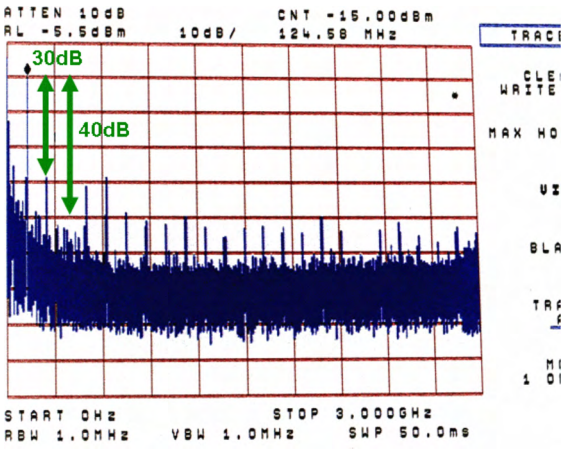


Figure 8: Spectrum of resonant clock waveform

The operating frequency of the resonant-clock ARM9EJ-S can be dynamically scaled, even with a fixed inductor value, by changing the frequency of REFCLK, since the operating frequency of the resonant-clock ARM926EJ-S always remains locked to the frequency of PLLOUT, regardless of the natural frequency of the clock network capacitance and the fitted inductor. As expected, power efficiency degrades as the operating frequency deviates from the natural frequency, but correct function is maintained. With an 11nH inductor, the resonant-clock core resonates at 125MHz and operates correctly from 100MHz to 200MHz. Maximum energy efficiency is achieved around resonance, with a relatively flat 0.23mw/MHz from 120MHz to 130MHz, yielding 35% savings in total power over the conventionally-clocked core. Fig. 7 shows energy dissipation of the resonant-clock, as operating frequency is varied away from the 125MHz natural frequency. Total energy dissipation of the resonant-clock core is also shown, and clock dissipation at resonance is less than 10% of total. For comparison, total energy dissipation of the conventional core is shown. Even at clock speeds away from resonance, total dissipation savings remain appreciable, exceeding 18% at 200MHz.

In addition to reducing clock power, resonant clocking improves electromagnetic compatibility. Fig. 8 gives the measured spectrum of the clock signal in the resonant-clock ARM9EJ-S running at its 125MHz natural frequency. At resonance, the clock waveform is expected to have essentially sinusoidal shape, with harmonics of significantly reduced amplitude. The measured spectrum shown in Fig. 8 confirms this expectation, yielding 2nd / 3rd harmonics at -30dB / -40dB from fundamental, respectively. Moreover, all harmonics after the 5th remain at -40dB from the fundamental.

## 4. CONCLUSION

This paper presents a resonant-clock ARM926EJ-S, the first-ever commercial-strength processor with resonant clocking deployed across its entire clock distribution network and successful interfacing between resonant and conventional clock domains. Clock power is reduced by 85%, and total power savings (clock, FFs, logic, and caches) range from 20% to 35%, depending on application profile.

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