A Gilbert Mixer with High Gain for 18 GHz Application

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***Abstract*—The aim of this paper is presented A Gilbert mixer with passive balun for 18 GHz application. It was used Taiwan Semiconductor provided by TSMC CMOS 0.18 µm process. We proposed mixer consists of Gilbert Cell, RF and LO stage matching and the IF buffer amplifier. Finally, at the operation voltage of Vdd = 1.8 V, RF frequency =18 GHz, LO frequency =17 GHz, the conversion gain is about 11.676 dB, input P1dB and power consumption are about -15 dBm and 54 mW. The chip size including all testing pads is 0.82 × 0.79 mm^2.**

Keywords: Ku-band, Buffer, and Gilbert Mixer.

I. INTRODUCTION

Mixer is one of the key components of wireless communication systems. Many portable communication systems which at least have two mixer, one is the receiving chain and another is transmitting chain. A double-balanced Gilbert-type mixer is widely used as the down-converter in RF CMOS receivers, since it contribute a high impedance input to the LNA, yet is capable of driving a low impedance load at its output. However, due to its relatively high noise figure, it often limits the receiver noise performance. A physical understanding of 1/f noise mechanisms in active mixers is crucial to identify and eliminate the noise sources. Due to frequency translation, the flicker noise of the transconductance stage up-converts to the local oscillator (LO) frequency and its odd harmonics.

We adopted integrated process to fabricate the circuit. Owing to the improvement of the CMOS technology in recent years, CMOS technology is another choice for the RF circuits above 10 GHz [5]. For Ku-band applications, a 12-GHz silicon bipolar receiver is demonstrated for digital satellite applications.

The proposed mixer was designed, simulated, and fabricated based on a 0.18 µm 1P6M standard RF CMOS process design kit (PDK) from Taiwan semiconductor manufacturing company (TSMC).

II. DESIGN OF CIRCUIT

We proposed a Gilbert mixer with IF buffer. This circuit structure of the proposed mixer consists of the input matching, current mirror, common-source transconductance stage, switching mixer core and the IF buffer amplifier, as illustrated in figure 1.

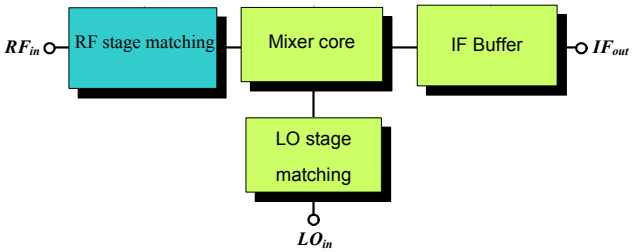


Figure 1. Ku-band Mixer design concept

To design a Gilbert cell mixer, first is to determine the size of the transistor and the bias condition. In conventional Gilbert mixer, the function of the transistors M_1 and M_2 is a differential transconductance amplifier as illustrated in figure 2. Therefore, the large transconductance (g_m) and minimum noise figure is the main consideration for this stage.

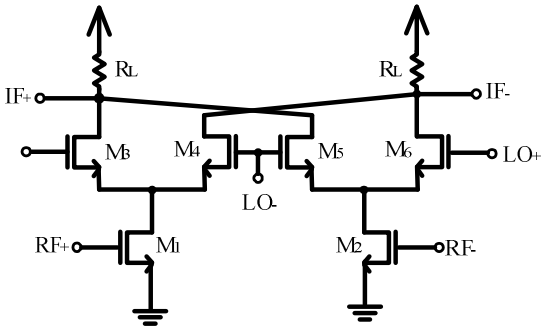


Figure 2. Conventional Gilbert mixer structure

M_1 and the M_2 is the input stage, they will change the RF

voltage single to currant single, gain and linearity is the important factor in concerning the part that design of transconductance, in order to enhance the linearity, and reduce the voltage, we can to use two ground-source pair to replace the convention differential pair in the input stage. In figure 3 because in the same of transistors size and bias, and the ground-source pair linearity was better than differential pair linearity. The differential pair and ground-source pair are shown in figure 3 .

For differential pair

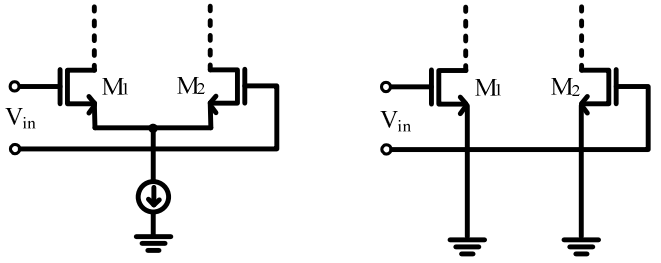
$$I_{D1}-I_{D2}=\frac{1}{2}\mu_n C_{ox}(\frac{W}{L})(V_{in})\sqrt{\frac{4I_{ss}}{\mu_n C_{ox}(W/L)}-(V_{in})^2} \quad (1)$$

For ground-source pair

$$I_{D1}-I_{D2}=\frac{1}{2}\mu_n C_{ox}(\frac{W}{L})[(V_{gs1}-V_{TH})^2-(V_{gs2}-V_{TH})^2]$$

$$=\frac{1}{2}\mu_n C_{ox}(\frac{W}{L})(V_{gs1}-V_{gs2})\cdot(V_{gs1}+V_{gs2}-2V_{TH}) \quad (2)$$

$$=\mu_n C_{ox}(\frac{W}{L})(V_{GS}-V_{TH})\cdot(V_{in})$$



(a) (b)

Figure 3. (a) The differential pair (b) The ground-source pair

The above equations knowing that the output current and input voltage is linearity dependence for ground-source pair, therefore, has the better linearity.

In addition to adopt ground-source part to improvement the linearity, increase gate voltage of M1, M2 (VGS-VT), also may increase mixer linearity of input stage. In the fixed bias, increase gate voltage will result in transconductance decreasingly, therefore, reduce the mixer's gain and increase the noise figure of the second stage, in generally low voltage design, gain and linearity are trade off of the mixer. Increasing M_1 and M_2 width will raise the mixer conversion, but add unnecessary junction capacitance.

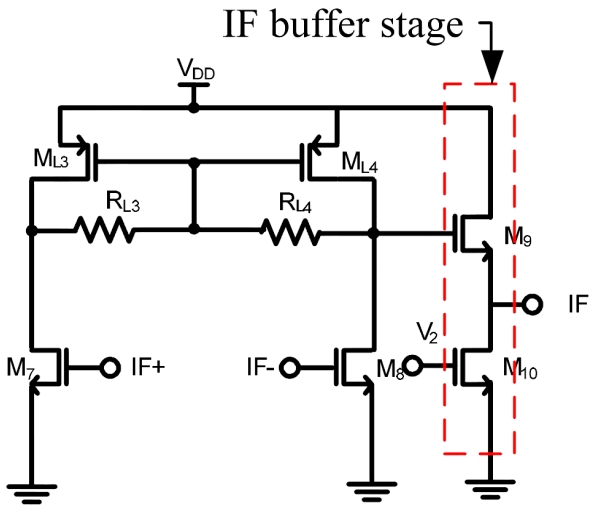


Figure 4. The IF buffer stage

Figure 4 shows the active balun and buffer, it will unbalance input single to transform balance output single, it's consist of the transconductance stage, active load stage, and IF buffer stage. The transistors ML3 and ML4, resistors RL3 and RL3 are active load stage, it same of mixer core, Major increase impedance made gain risen. The transistors M7 and M8 are transconductance stage, it was used to inject differential IF signal. The buffer for 50 Ω output matching network.

The figure 5 is the complete schematic of the Ku-band mixer. In the figure, we can divide the circuit into as Gilbert mixer structure and IF buffer.

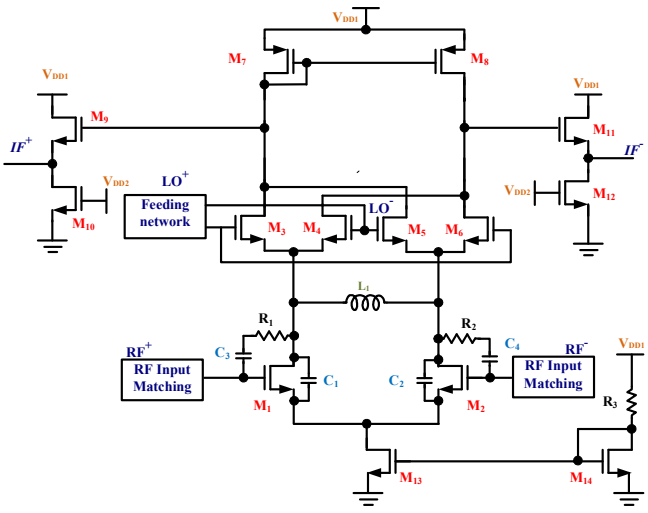


Figure 5. Complete schematic of Ku-band mixer.

III. SIMULATED AND MEASURED RESULTS

The process design kit of the 0.18-μm CMOS technology of the TSMC was proposed. The Agilent advanced design system (ADS) simulator is applied in this paper. The simulated results of a 18 GHz mixer are shown in figure 6 to figure 13.

For the simulated results. When the LO power is decided, we analyze the performances of frequency response by using small signal and large signal, which are illustrated in figure 6 to figure 11. The conversion gain of 11.676 dB at 18 GHz, the noise figure of 7.989 dB, the RF return loss is -25.42 dB at 18 GHz, the LO return loss is -24.748 dB at 17 GHz, the IF return loss is -12.754 dB at 1 GHz, and a P_{1dB} of -15 dBm were obtained. The total chip size was 0.84 × 0.77 mm^2 including the pads. the power consumption was 54 mW.

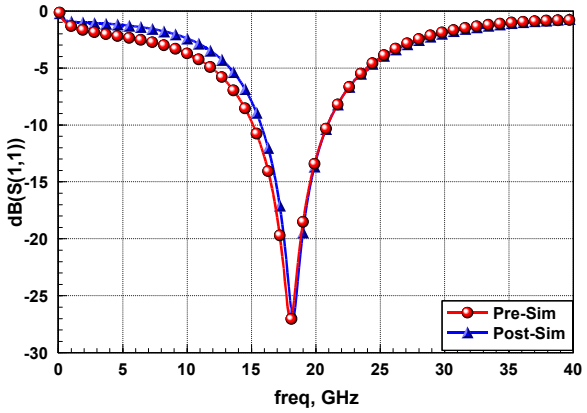


Figure 6. Simulated results of RF input return loss.

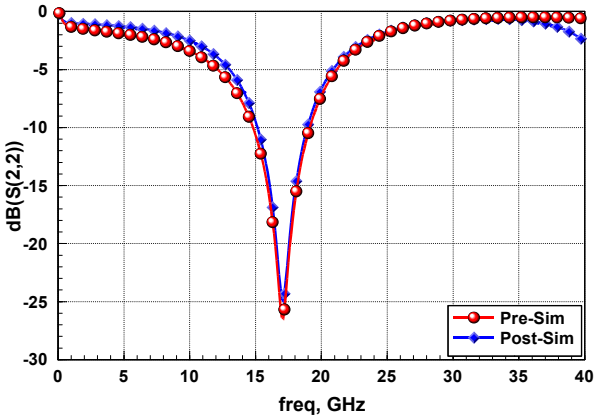


Figure 7. Simulated results of LO input return loss

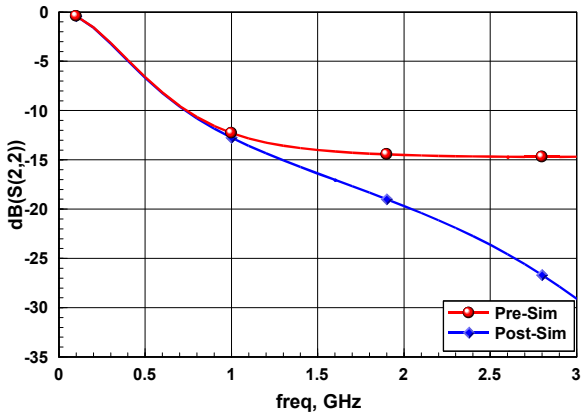


Figure 8. Simulated results of IF output return loss.

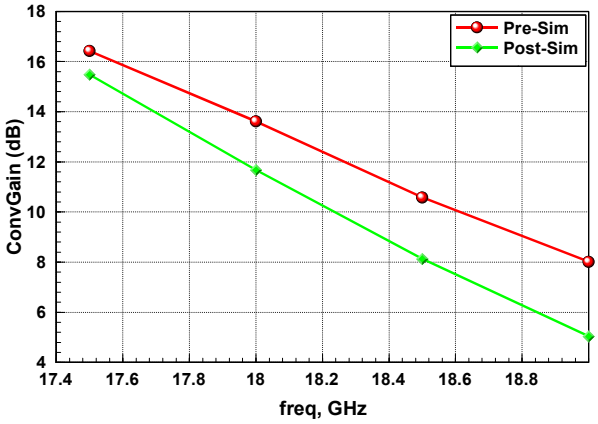


Figure 9. Simulated results of conversion gain.

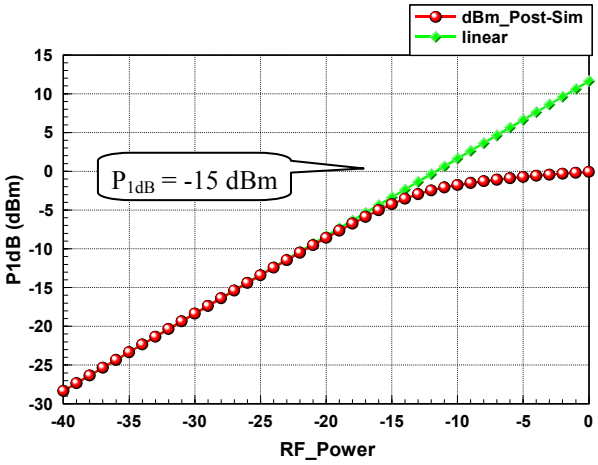


Figure 10. Simulated results of P_{1dB}.

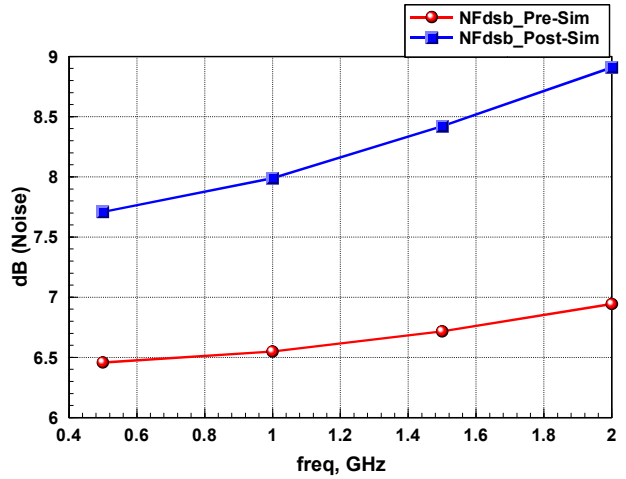


Figure 11. Simulated results of noise figure.

The isolation performance indicates the signal leakage form port to port in mixers. It will influence the quality of the communication. The critical issues are the LO to RF isolation, LO to IF isolation, and RF to IF isolation. Figure 12 is shown the LO to RF isolation, figure 13 shows the LO to IF isolation and figure 14 shows the RF to IF isolation of the CMOS Gilbert cell mixer. Figure 12 is shown the simulated results of LO to RF isolation is 50.713 dB, the LO to IF isolation is 45.021 dB, the RF to IF isolation is 37.738 dB.

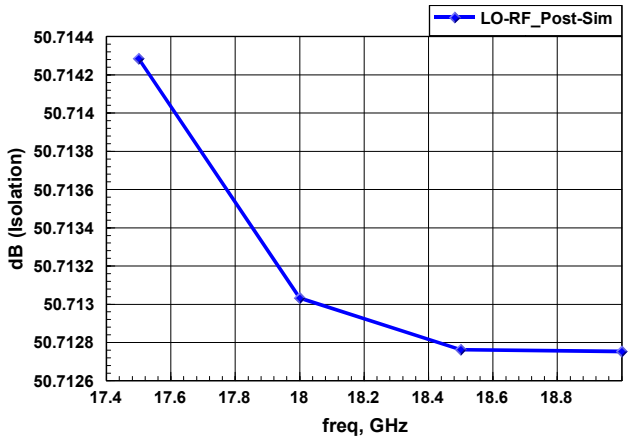


Figure 12. Simulated results of LO to RF isolation.

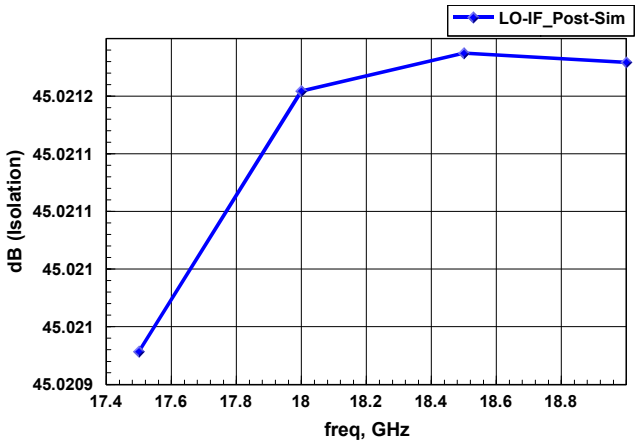


Figure 13. Simulated results of LO to IF isolation.

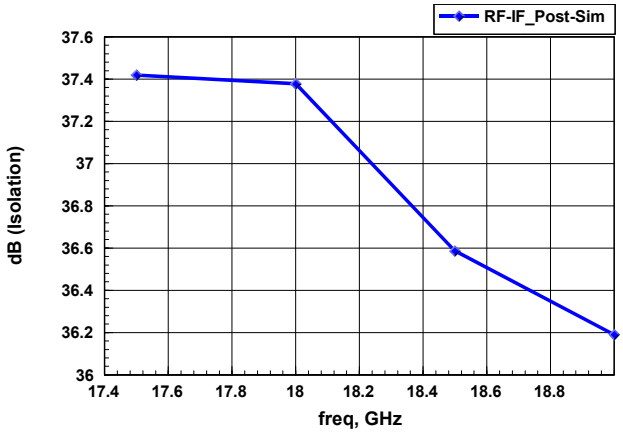


Figure 14. Simulated results of RF to IF isolation.

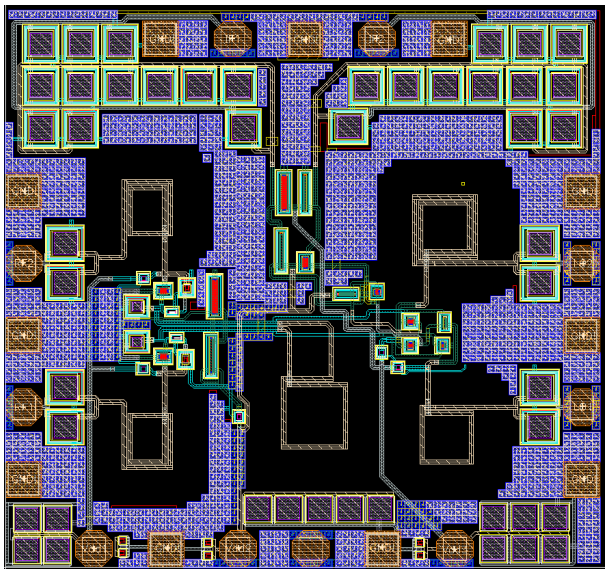


Figure 15. Layout for the Ku-band mixer chip.

IV. CONCLUSIONS

The design of a 18 GHz for CMOS Gilbert mixer wireless application has been presented. The Agilent advanced design system (ADS) simulator is applied in this paper. In mixer design, using an IF buffer to provides good conversion gain, noise figure and return loss. The maximum gain is the 11.676 dB. It consumes 54 mW from 1.8 V supply voltage and occupies an area of only 0.82 × 0.79 mm^2. Figure 15 is Layout of mixer chip.

TABLE I. Mixer Performance Comparison

Specification	This work	[14]	[15]
Technology	0.18 μm CMOS	0.18 μm CMOS	0.18 μm CMOS
Operation Voltage	1.8 V	N/A	1.8 V
RF Input Frequency	18 GHz	12.1 GHz	10.29 GHz
LO Input Frequency	17 GHz	3 GHz	N/A
Conversion Gain	11.676 dB	6 dB	8.8 dB
Input P_{1dB}	-15 dBm	-12 dBm	-16.5 dBm
Noise Figure	7.989 dB (DSB)	15 dB (DSB)	12.5 dB (DSB)
Die Area	0.6478 mm^2	0.7225 mm^2	0.7396 mm^2

V. ACKNOWLEDGMENT

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