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PAPER

A One-Step Input Matching Method for Cascode CMOS Low-Noise Amplifiers

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SUMMARY In the design of cascode CMOS low-noise amplifiers, the gate-drain capacitance is generally neglected because it is thought to be small enough compared to gate-source capacitance. However, a careful examination will reveal the fact that the drain impedance of the input transistor significantly affects the input impedance through the gate-drain capacitance, especially as the CMOS technology getting more and more advanced. Moreover, the substrate coupling network of the input transistor also comes into play when the drain impedance of the input transistor is high enough compared to the substrate coupling network. In order to make input matching easier, it is desirable to know the details of the substrate coupling network. Unfortunately, designers generally do not have enough information about the technology they have used, not to mention knowing the details concerning the substrate coupling network. As a matter of fact, designers generally do have foundry provided component models that contain information about the substrate coupling network. This gives us the chance to minimize its effect and predict the input impedance of a low noise amplifier more accurately. In this paper, we show that the effect of the substrate coupling network can be ignored by keeping the drain impedance of the input transistor low enough and a proper drain impedance can then be chosen to achieve input matching without the need of iteration steps. Simulation results of a 2.4 GHz CMOS low noise amplifier using foundry provided component models are also presented to demonstrate the validation of the proposed input matching method.

key words: *CMOS, radio frequency, cascode, low noise amplifier, input matching*

1. Introduction

It is well known that low noise amplifier (LNA) is a fundamental building block in radio frequency (RF) circuit design. It amplifies very small RF signal and suppresses the noises contributed by itself to the circuit. The structure of a low noise amplifier is usually simple due to the low noise requirement and the desire for low-power portable systems. However, the design of such a simple circuit, especially with CMOS technology at high frequency, has never been an easy task because it is a compromise of many aspects such as impedance matching, power gain, linearity, and noise performance, etc.[1]. In addition to the various design considerations, the lossy substrate of CMOS circuits and the high frequency effects of parasitic components complicate the design problems so that the design targets are hardly achieved or the design process is time-consuming. This is because the parasitic components and the substrate coupling network couple with different parts of the circuit such that accurate design is difficult. Based on the above reasons, we can expect that any modification to the design of a low noise amplifier would invoke design iterations. For example, a cascode CMOS low noise amplifier is expected to have low impedance connected at the drain node of the input transistor, but there are other variations such that the drain node of the input transistor is not directly connected to source node of the common-gate transistor [2]–[4]. As will be clear later in this paper, if the drain impedance of the input transistor is not considered carefully for those variations, it may be high enough to affect the input impedance through the gate-drain capacitance and the substrate coupling network of the input transistor will also come into play. In such cases, input matching would be more difficult and designers have to entirely depend on simulators to achieve the required input impedance at the frequency of interest. This design method needs to adjust various parts of the circuit many times to obtain satisfied result and we can not learn the importance of the substrate coupling network.

Since a low noise amplifier is expected to receive very small RF signal, input matching is especially important for this building block. A good input matching means the possibility to have higher signal to noise ratio (SNR) at the output, and therefore a better noise performance. The input impedance of a low noise amplifier is required to be matched to the external source impedance, usually 50 Ω, in order to have maximum input signal. However, it is not easy to achieve this simple target due to the reasons mentioned above. In an effort to overcome the difficulty to achieve input matching, we first explore the input matching problems of low noise amplifiers and then propose a design method that can achieve input matching in an explicit manner without the need of iteration steps.

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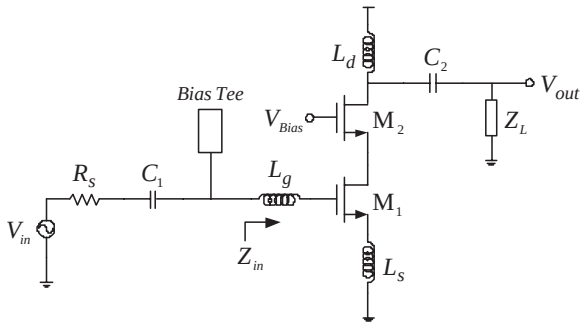

Fig. 1 Cascode low noise amplifier.

2. Traditional Input Matching Method

There are other architectures for low noise amplifiers in RF circuit design [1], [5]; however, the mostly adapted one is the cascode architecture as shown in Fig.1. It consists of a common-source transistor with a small source degeneration inductor and a common-gate transistor as current buffer. It is considered as the best architecture that can achieve both power gain and low noise requirements [5]. The input impedance of a cascode CMOS low-noise amplifier is given by

$$\begin{aligned} Z_{in} &= s(L_g + L_s) + \frac{1}{sC_{gs}} + \frac{g_m}{C_{gs}} L_s \\ &= \frac{g_m}{C_{gs}} L_s \text{ (at resonant)} \end{aligned} \tag{1}$$

where C_{gs} is the gate-source capacitance and g_m is the transconductance of the input transistor M_1. This elegant equation shows that designers have the freedom to adjust bias and source inductance to achieve the required 50 Ω resistance at resonant frequency and then tune the gate inductance to cancel the reactance part of the input impedance. This equation, nevertheless, is a simplified version of the real situation because it neglects the gate-drain capacitance and the CMOS substrate coupling network. It is suitable to use this equation when the frequency of interest is low enough to neglect the high frequency effects of the parasitic components or when the substrate is not very lossy. However, as the CMOS technology getting more advanced, the gate-drain capacitance is getting more importance. Table 1 lists the capacitance models for C_{gs} and C_{gd} in various operation regions of CMOS transistor where C_{OX} and C_{OL} are the gate-oxide and overlap capacitances, respectively [6]. Using the simple model for C_{gd} in Table 1, a simulation result for a typical 0.25μm CMOS technology is shown in Fig.2 where C_{gs} is derived directly by subtract C_{gd} from the total gate capacitance. Note that the gate-bulk capacitance is ignored since its value in saturation and linear regions is much smaller than that of the overlap capacitance. It shows

Table 1 Capacitance models in various regions.

Operation region	C_{gs}	C_{gd}
Cutoff	C_{OL}	C_{OL}
Saturation	$\frac{2}{3}WLC_{OX} + C_{OL}$	C_{OL}
Linear	$\frac{1}{2}WLC_{OX} + C_{OL}$	$\frac{1}{2}WLC_{OX} + C_{OL}$

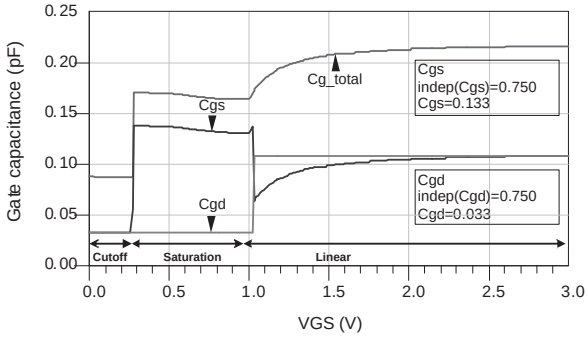

Fig. 2 Gate capacitance versus VGS of CMOS transistor.

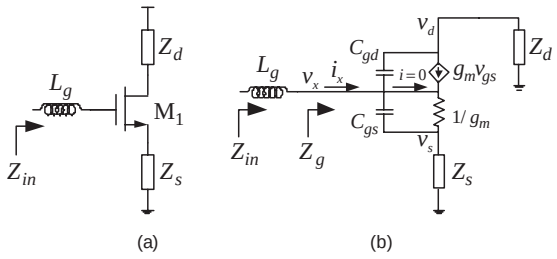

Fig. 3 (a) Input transistor with drain and source impedances, and (b) Small-signal model for input stage.

that the ratio of the gate-drain capacitance to the gate-source capacitance can be as large as 25% such that we can not ignore the gate-drain capacitance any more.

The existence of the gate-drain capacitance motives us to take it into considerations as shown in Fig.3. The node equation at node v_x in Fig.3 (b) is given by

$$i_x = sC_{gs}(v_x - v_s) + sC_{gd}(v_x - v_d) \tag{2}$$

and the Kirchhoff's current law (KCL) states that

$$i_x = \frac{v_s}{Z_s} + \frac{v_d}{Z_d} \tag{3}$$

where Z_d and Z_s are the impedances seen at drain and source nodes, respectively. Substituting v_d in Eq.(3) into Eq.(2) results in the following equation

$$i_x = \frac{(sC_{gs} + sC_{gd})v_x + (sC_{gd}\frac{Z_d}{Z_s} - sC_{gs})v_s}{(1 + sC_{gd}Z_d)}. \tag{4}$$

Also note that the node equation at node v_s gives the relation between v_x and v_s

$$\frac{v_s}{Z_s} = (sC_{gs} + g_m)(v_x - v_s) \tag{5}$$

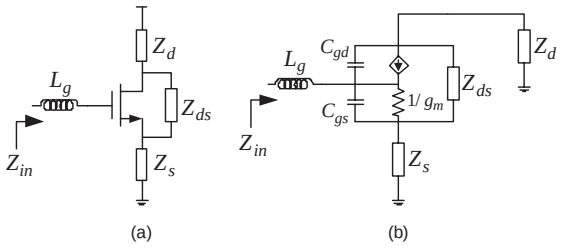

Fig. 4 (a) Input transistor with substrate coupling network, and (b) Equivalent small-signal model.

which is used in Eq.(4) to eliminate v_s. The impedance Z_g defined as $Z_g \equiv v_x/i_x$ is then derived as

$$Z_g = \frac{(Z_s+\frac{1}{sC_{gs}}+\frac{g_m}{sC_{gs}}Z_s)(1+sC_{gd}Z_d)}{1+\frac{C_{gd}}{C_{gs}}+\frac{C_{gd}}{C_{gs}}(g_m+sC_{gs})(Z_s+Z_d)} \tag{6}$$

and the input impedance is consequently given by

$$Z_{in} = sL_g + \frac{(Z_s+\frac{1}{sC_{gs}}+\frac{g_m}{sC_{gs}}Z_s)(1+sC_{gd}Z_d)}{1+\frac{C_{gd}}{C_{gs}}+\frac{C_{gd}}{C_{gs}}(g_m+sC_{gs})(Z_s+Z_d)}. \tag{7}$$

Eq.(7) shows that the gate-drain capacitance significantly affects the input impedance because the drain impedance comes into play due to its existence. There is also a good reason to consider the effect of the substrate coupling network since it couples with different parts of a low noise amplifier as well. As shown in Fig.4 is the input transistor with a simple substrate coupling network between the drain and source nodes. A simple substrate coupling network is used here for simplicity because we do not have exact information about it. Taking the substrate coupling network into further considerations, the input impedance should be modified as

$$\begin{aligned} Z_{in} = {} & sL_g \\ & + \frac{\left(Z_s^{'}+\frac{1}{sC_{gs}}+\frac{g_m}{sC_{gs}}Z_s^{'}\right)(1+sC_{gd}Z_d)}{1+\frac{C_{gd}}{C_{gs}}+\frac{C_{gd}}{C_{gs}}(g_m+sC_{gs})\left(Z_s^{'}+Z_d^{'}\right)} \\ & + \frac{\frac{Z_d^{'}}{Z_{ds}}\left(Z_s-\frac{C_{gd}}{C_{gs}}Z_d\right)}{1+\frac{C_{gd}}{C_{gs}}+\frac{C_{gd}}{C_{gs}}(g_m+sC_{gs})\left(Z_s^{'}+Z_d^{'}\right)} \end{aligned} \tag{8}$$

where

$$Z_s^{'} = \frac{Z_s Z_{ds}}{Z_s+Z_d+Z_{ds}} \tag{9}$$

and

$$Z_d^{'} = \frac{Z_d Z_{ds}}{Z_s+Z_d+Z_{ds}}. \tag{10}$$

Note that $Z_s^{'}+Z_d^{'} = (Z_s+Z_d)//Z_{ds}$ which can be observed from Fig.4. It shows that Eq.(8) is too complex to deal with unless the coupling network can be obtained.

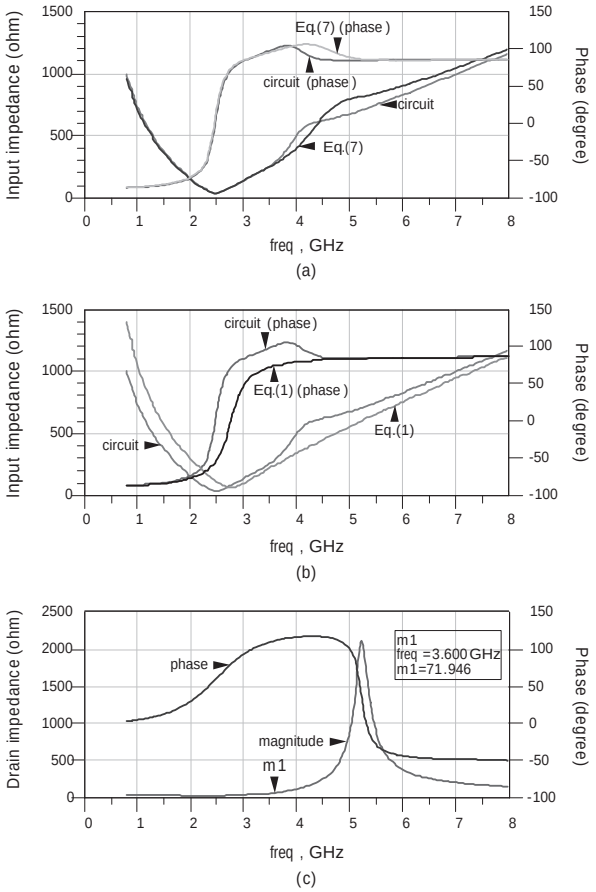

Fig. 5 (a) Input impedances for circuit simulation and Eq.(7), (b) Input impedances for circuit simulation and Eq.(1), and (c) Drain impedance of the input transistor.

3. Proposed Input Matching Method

It seems that we can not easily handle the input impedance. Indeed, we hardly know the details concerning the substrate coupling network. Even we know, it is still hard to deal with. However, we note that the source impedance of a cascode low noise amplifier is often a small source degeneration inductance which is a very low impedance. Therefore, the effect of the substrate coupling network can be neglected provided that the drain impedance Z_d is kept small enough compared to Z_{ds}. In such a case, Eq.(8) reduces to Eq.(7). Also, note that the meaning of keeping drain impedance low enough compared to Z_{ds} is to prevent signal loss through the substrate coupling network. This is the general case in low noise amplifiers with cascode architecture, but how small should Z_d be? The simulation results of the circuit in Fig.1 can give us a general idea. Shown in Fig.5 (a) and Fig.5 (b) are the simulation results of the input impedance for the low noise amplifier using foundry provided 0.25μm CMOS models along with the predictions of Eq.(7) and Eq.(1), re-

spectively. This circuit is intended to operate at 2.4 GHz but the output is tuned to higher frequency in order to illustrate some viewpoints. Fig.5 (a) shows that Eq.(7) predicts input impedance of the circuit well up to around 3.6 GHz where the drain impedance is about 72 Ω as shown in Fig.5 (c), therefore, Eq.(7) is available for drain impedance up to about 72 Ω in this case. However, as the drain impedance getting higher as shown in Fig.5 (c), Eq.(7) is no longer valid because the substrate coupling network of the input transistor comes into play. The high impedance of the drain node in Fig.5 (c) is because that the drain impedance of the common-gate transistor is coupled to the drain node of the input transistor through the substrate coupling network of M_2 transistor. Therefore, without carefully considering the drain impedance of the input transistor, the substrate coupling network of the input transistor may have significant effect if the drain impedance of the input transistor is high enough. We also note from Fig.5 (b) that the prediction of Eq.(1) is far from the simulation result of the low noise amplifier in this case. It means that it is not adequate to neglect the gate-drain capacitance and the substrate coupling network as the CMOS technology getting more advanced, otherwise, the design of the input impedance of low noise amplifiers would require many iteration steps and be time-consuming.

Based on the above discussion, Eq.(7) can help us to design input impedance provided that the drain impedance of the input transistor is kept low enough. Let us define

$$\frac{1}{A_F} = \frac{(1+sC_{gd}Z_d)}{1+\frac{C_{gd}}{C_{gs}}+\frac{C_{gd}}{C_{gs}}(g_m+sC_{gs})(Z_s+Z_d)}, \tag{11}$$

the input impedance predicted by Eq.(7) is therefore given by

$$Z_{in} = sL_g + \frac{1}{A_F}(Z_s + \frac{1}{sC_{gs}} + \frac{g_m}{sC_{gs}}Z_s) \tag{12}$$

where $Z_s = R_s + sL_s$. It returns to the familiar input impedance equation of cascode low-noise amplifiers with the modification of a factor, A_F. We prefer the factor to be real in order to simplify the input matching design. Therefore, the design goal is to find a proper drain impedance, $Z_d = R_d + jX_d$, that makes A_F a real factor. If this is the case, the input impedance at resonant frequency is give by

$$Z_{in} = \frac{1}{A_F}\frac{g_m}{C_{gs}}L_s \tag{13}$$

which is required to be matched to the external source impedance R_{src} at the frequency of interest. Note that the gate resistance R_g is not included in the above and below equations; however, it can be taken into considerations by replacing R_{src} with $R_{src} - R_g$. Also note that R_s is neglected because its value is very small and does not affect the analysis very much. The required source and gate inductances are then given by

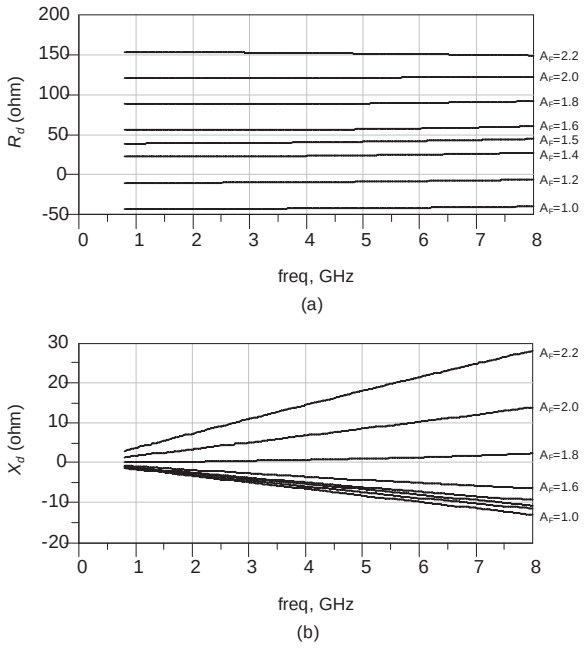

Fig. 6 Simulation results of (a) R_d and (b) X_d for various A_F.

$$L_s = A_F R_{src}\frac{C_{gs}}{g_m} \tag{14}$$

$$L_g = \frac{1}{A_F}\frac{1}{\omega_o^2 C_{gs}} - R_{src}\frac{C_{gs}}{g_m} \tag{15}$$

where ω_o is the frequency of interest. Note that the gate inductance can be smaller than normally expected if A_F can be greater than one. This is desirable because a smaller gate inductor means smaller chip area and less input noise. In an effort to work out the conditions for A_F to be real, substitute into Eq.(11) with $Z_s = sL_s$ and $Z_d = R_d + jX_d$, respectively. After some algebraic calculations and identification of the real and imaginary parts respectively, we derive the equations for R_d and X_d as follows

$$R_d = \frac{g_m\left[(A_F-1)-\frac{C_{gd}}{C_{gs}}\right]+A_F^2\omega^2 C_{gs}C_{gd}R_{src}}{\frac{C_{gd}}{C_{gs}}g_m^2+(A_F-1)^2\omega^2 C_{gs}C_{gd}} \tag{16}$$

$$X_d = \omega\frac{C_{gs}}{g_m}\left[(A_F-1)R_d - A_F R_{src}\right] \tag{17}$$

where a positive X_d means an inductance term while a negative X_d term means a capacitance. Since a negative resistance is hard to implement and may result in instability, negative R_d is not desirable. Shown in Fig.6 are the simulation results of R_d and X_d for various A_F, we see that A_F must be greater than some particular value in order to make R_d positive. This condition is desirable because smaller gate inductor can

be used to benefit both the performance and the chip area. However, note that as A_F increases, the required drain impedance Z_d also increases. As we mentioned earlier, larger drain impedance will prevent us from using Eq.(7) to predict the input impedance. Therefore, although designers have the freedom to choose A_F to meet the requirements, there exists a trade-off in choosing Z_d.

4. Design of the Drain Impedance

It is well known that the noise performance of a low noise amplifier is mainly determined by the input transistor [5]. Therefore, the first step is to determine the dimension and bias condition for the input transistor. For the determined input transistor, a set of drain impedance Z_d is then derived for various A_F based on Eqs.(16) and (17). Designers can then choose a proper drain impedance for the input transistor from the simulation results to achieve input matching and the required source and gate inductances are given by Eqs.(14) and (15), respectively. This method is easy to achieve input matching if the source and gate inductors can be designed accurately. However, the design of on-chip inductors is not as easy as one might expect [7]–[9]. Alternatively, since the A_F factor is determined by Eq.(14) for a given source inductor, the required gate inductance and drain impedance of the input transistor are subsequently determined for the given source inductor. This way is more practical for a given source inductor with known characteristic because the required resistive impedance is mainly provided by this small inductor which need to be assured of its inductance.

We have to keep in mind that the chosen drain impedance should be small enough as compared with the substrate coupling network. Nevertheless, it is not easy to have a criterion in choosing a proper drain impedance because we do not know the details regarding the substrate coupling network. But as will be clear later in this paper, we still can be aware of the situation that the drain impedance is large enough so that the substrate coupling network can not be ignored. In case of higher drain impedance of the input transistor, choosing a smaller A_F factor or a smaller source inductor with known characteristic might solve the problem. For the purpose of illustration, a 2.4 GHz 0.25μm CMOS low noise amplifier is designed based on the proposed input matching method by first determining the A_F factor. Starting from source inductor with known characteristic is almost the same procedure except that A_F factor can not be choosing arbitrarily. The circuit schematic is shown in Fig.7 where the detailed bias circuit is not shown. The inductor L_d, capacitors C_d and C_2 function as both output load and output matching circuit. The output matching is necessary if the low noise amplifier is driving an external filter. The drain impedance of the input transistor indicated by

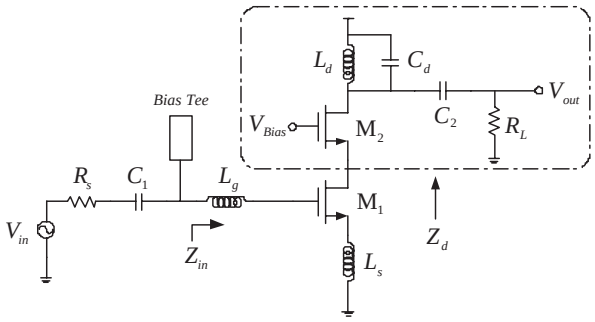

Fig. 7 A 2.4 GHz 0.25μm cascode low noise amplifier.

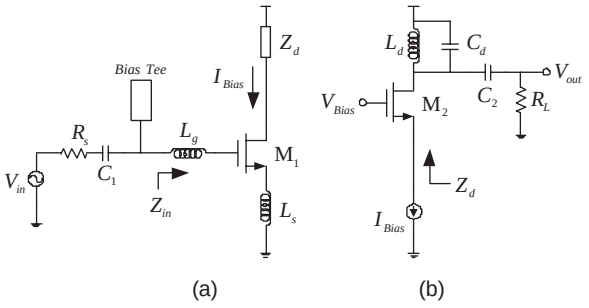

Fig. 8 Separate simulation for (a) Low noise amplifier, and (b) Drain impedance.

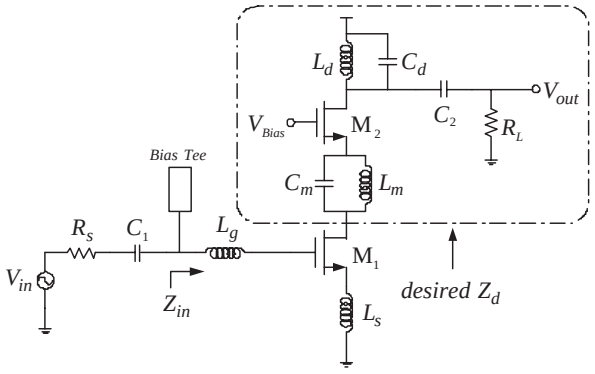

Fig. 9 Low noise amplifier with desired drain impedance.

Z_d is the portion that we need to simulate separately, as shown in Fig.8, after the desired drain impedance for the input transistor is determined. After knowing the information about the difference between the original and the desired drain impedance, designers can modify the load portion that contributes to Z_d and use an impedance transformation network [10] to transform it to the desired drain impedance as shown in Fig.9.

A 5.97 pF capacitor is required to achieve the desired drain impedance in this design and a large 1μH inductor is used to provide dc path in the simulation. In integrated circuit, the LC tank will be designed with reasonable size, e.g. 8.17 pF capacitor and 2 nH in-

Table 2 Some of the circuit parameters.

VDD	1.5 V
VGS	0.75 V
Bias current	2.64 mA
W/L of M_1, M_2	460
L_g	22.9 nH
C_m	8.17 pF
L_m	2 nH
L_s	0.32 nH
L_d	2.84 nH
C_d	0.97 pF
C_2	0.52 pF
R_g	15 Ω

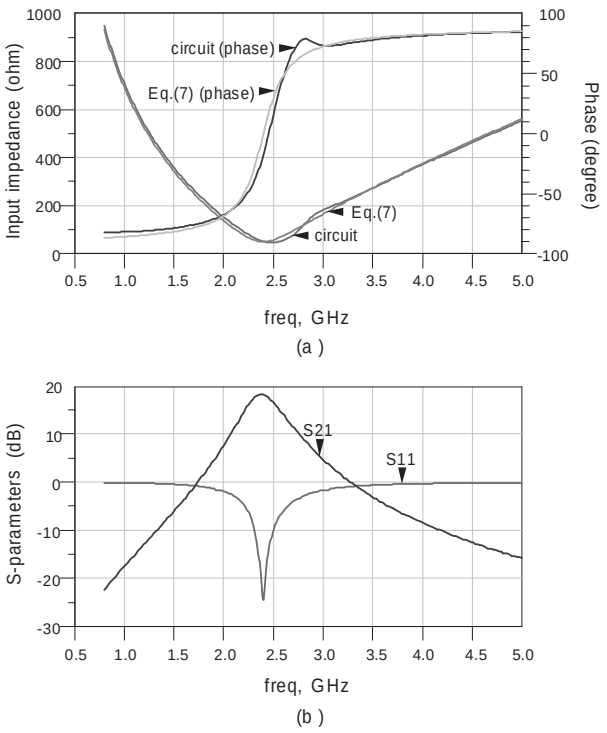

Fig. 10 (a) Input impedance, and (b) S11 and S21 parameters.

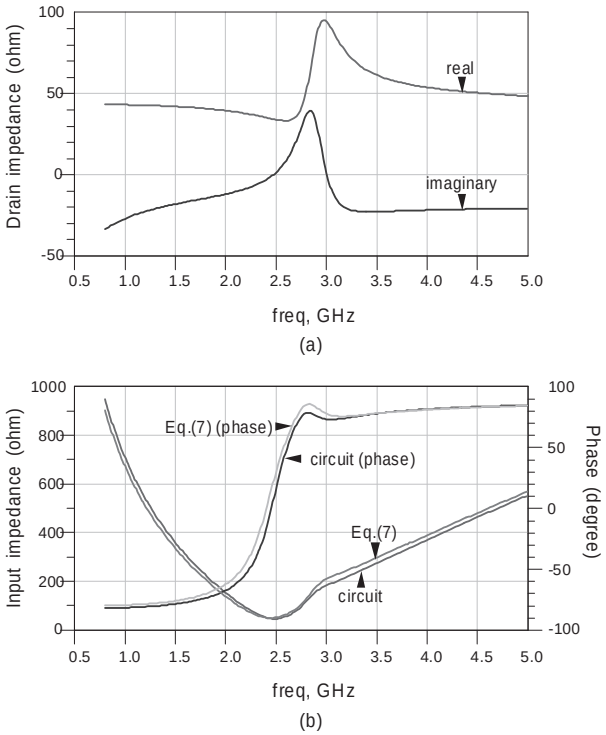

Fig. 11 (a) Actual drain impedance of the input transistor, and (b) Prediction of Eq.(7) using actual drain impedance.

ductor or 10.37 pF capacitor and 1 nH inductor, such that its impedance at resonant frequency meets the difference between the original and the desired drain impedance of the input transistor. Note that the real part of the desired drain impedance is chosen to be equal to the real part of original drain impedance for simplicity. We can modify the real part of the original drain impedance to the desired value in order to have larger A_F factor, but larger resistance in the signal path would suffer the noise performance of the low noise amplifier. Table 2 lists some of the circuit parameters used in this design. Shown in Fig.10 are the simulation results of the input impedance, S11, and S21 parameters of the low noise amplifier. We see that without iterative design process, the input impedance is almost matched at the frequency of interest in the first design. Note that the impedance behavior of the circuit is slightly different from the prediction of Eq.(7) as shown in Fig.10 (a). The underlying reason is that the drain impedance used in Eq.(7) is almost proportional to frequency as shown in Fig.6 while the actual drain impedance is various with frequency as shown in Fig.11 (a). Using the actual drain impedance of the input transistor in Eq.(7), the simulation result in Fig.11 (b) confirms again that Eq.(7) can predict the input impedance provided that the drain impedance of the input transistor is kept low enough compared to the substrate coupling network. Fig.11 (b) also shows slight mismatch between the simulation results of the circuit and the prediction of Eq.(7). This mismatch comes from the unavoidable fact for lossy CMOS substrate that the effect of the substrate coupling network can not be entirely ignored even though the drain impedance of the input transistor is kept very low. The degree of mismatch can serve as an indication of the effect of the substrate coupling network. Large mismatch means that the drain impedance of the input transistor is not low enough compared to the substrate coupling network and therefore the signal might be lost significantly through the substrate coupling network of the input transistor. In such a case, choosing a smaller A_F factor or a smaller source inductor, if starting from it, can solve the problem. If the mismatch is small as in this paper, however, choosing a smaller A_F factor or a smaller source inductor would not help much. To deal with small mismatch or to achieve better input matching, reserve small budget

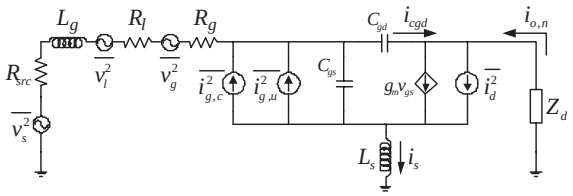

Fig. 12 Noise model used for the input stage.

in advance, e.g. 2.35 GHz instead of 2.4 GHz, should be helpful.

5. Noise Analysis of the Proposed Method

It is essential for a low noise amplifier to have satisfied noise performance in order to make the circuit itself do not degrade the output SNR to an unacceptable level. Noise performance is usually evaluated with Noise Figure (NF) which indicates the noise suppression ability of the circuit. Noise Figure is commonly defined as

$$NF = 10\log(\text{Noise Factor}) \tag{18}$$

where Noise Factor (F) is defined as

$$F = \frac{\text{Total output noise}}{\text{Total output noise due to the source}}. \tag{19}$$

Fig.12 shows the noise model of the input stage where two major noise sources of CMOS transistor, channel thermal noise and gate induced noise [5], are included in addition to the resistive noise sources, $\overline{v_s^2}$, $\overline{v_l^2}$, and $\overline{v_g^2}$. The source resistance R_{src} contributes to $\overline{v_s^2}$ while $\overline{v_l^2}$ and $\overline{v_g^2}$ are due to gate inductor resistance R_l and gate resistance R_g, respectively. The gate induced noise can be separated into two parts; $\overline{i_{g,c}^2}$ is the portion that correlated with the channel thermal noise $\overline{i_d^2}$ while $\overline{i_{g,u}^2}$ is the uncorrelated part. The power spectral densities of the channel thermal noise and the gate induced noise are given respectively by

$$\frac{\overline{i_d^2}}{\Delta f} = 4kT\gamma g_{d0} \tag{20}$$

and

$$\frac{\overline{i_g^2}}{\Delta f} = \underbrace{4kT\delta g_g(1-|c|^2)}_{\overline{i_{g,u}^2}} + \underbrace{4kT\delta g_g|c|^2}_{\overline{i_{g,c}^2}} \tag{21}$$

$$g_g = \frac{\omega^2 C_{gs}^2}{5g_{d0}} \tag{22}$$

where g_{d0} is the zero-bias drain conductance of the transistor and γ is a bias-dependent factor which can be as high as two to three for short-channel devices. The correlation coefficient $c \approx 0.395j$ is positive for the polarity shown in Fig.12 and δ is the coefficient of gate noise that classically equal to 4/3 for long channel devices. The noise power spectral density due to resistance R is given in the form of $\overline{v^2} = 4kTR$ where k is the Boltzmann constant and T is the absolute temperature. The total output noise power density at the frequency of interest due to the source is then given by

$$S_{o,src}(\omega_o) = 4kTR_{src}\left|G_m(\omega_o)\right|^2 \tag{23}$$

where $G_m(\omega)$ is the transconductance of the input stage which is derived from Fig.3 (b) as

$$G_m(\omega) = \frac{\frac{A_F-1}{A_F} - \frac{g_m}{sC_{gs}}}{R_{src} + Z_{in}(\omega)}. \tag{24}$$

The output noise power density due to R_l and R_g can be derived in a similar manner as

$$S_{o,R_l,R_g}(\omega_o) = 4kT(R_l+R_g)\left|G_m(\omega_o)\right|^2. \tag{25}$$

Note that the magnitude of $G_m(\omega)$ does not change drastically for small A_F whose value is less than 2 for practical design.

To evaluate the total output noise due to $\overline{i_d^2}$ is a rather complex task when the gate-drain capacitance is taken into considerations. However, by solving the following equation

$$v_{gs} = (i_{o,n} - i_s)(R_{src} + sL_g) - i_s sL_s \tag{26}$$

to derive v_{gs} in terms of i_d and $i_{o,n}$ and substitute it into the following node and branch equations

$$i_{o,n} = i_d + g_m v_{gs} - i_{cgd} \tag{27}$$

$$i_{cgd} = sC_{gd}(v_{gs} - v_{ds}), \tag{28}$$

the ratio of $i_{o,n}$ to i_d at the frequency of interest is derived as

$$H_d(\omega_o) = \frac{1 + \frac{C_{gd}}{C_{gs}} + \frac{sL_g}{R_{src}}\left(1 + \frac{C_{gd}}{C_{gs}} - A_F\right)}{A_F\left(1 + \frac{Z_{in}(\omega_o)}{R_{src}}\right)(1 + sC_{gd}Z_d)}. \tag{29}$$

Note that the Kirchhoff's current law and Eq.(11) are used in the derivation of $H_d(\omega_o)$. Since the drain impedance Z_d is required to be small enough, $sC_{gd}Z_d$ is negligible at the frequency of interest. In a similar procedure, the ratio of $i_{o,n}$ to the gate induced noise at the frequency of interest can be derived as

$$H_g(\omega_o) = \frac{\left(1 + \frac{sL_g}{R_{src}}\right)\left(\frac{g_m}{sC_{gs}} - \frac{C_{gd}}{C_{gs}}\right) + \omega_T L_s}{A_F\left(1 + \frac{Z_{in}(\omega_o)}{R_{src}}\right)(1 + sC_{gd}Z_d)} \tag{30}$$

and the total output noise power density due to $\overline{i_{g,u}^2}$ is therefore expressed as

$$S_{o,i_{gu}}(\omega_o) = 4kT\delta g_g\left(1-|c|^2\right)\left|H_g(\omega_o)\right|^2. \tag{31}$$

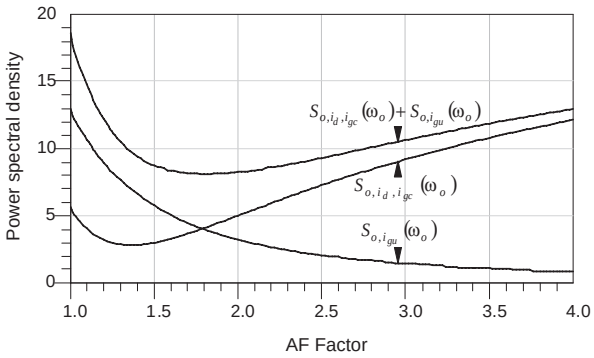

Fig. 13 Noise power spectral density normalized to $4kT\gamma g_{d0}$.

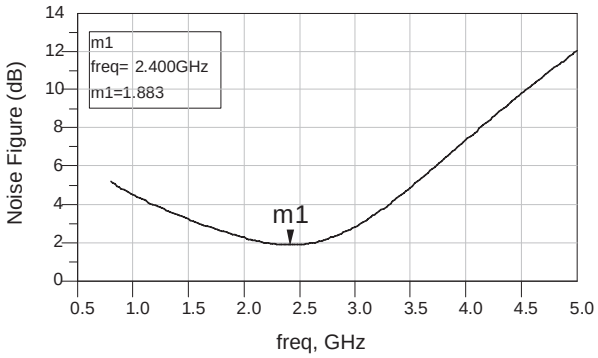

Fig. 14 Noise Figure of the designed low noise amplifier.

Since $\overline{i_{g,c}^2}$ is correlated with $\overline{i_d^2}$, the noise amplitudes appear at the output due to $\overline{i_{g,c}^2}$ and $\overline{i_d^2}$ should be summed before the power spectral density is evaluated [5]. With this in mind and using Eqs.(29) and (30), the total output noise power density due to $\overline{i_{g,c}^2}$ and $\overline{i_d^2}$ is derived as

$$S_{o,i_d,i_{gc}}(\omega_o) = 4kT\left|\sqrt{\gamma g_{d0}}H_d(\omega_o)+\sqrt{\delta g_g}|c|H_g(\omega_o)\right|^2. \quad (32)$$

Using Eqs.(14) and (15) for the determined input transistor, the noise power spectral density of $S_{o,i_d,i_{gc}}(\omega_o)$ that normalized to $4kT\gamma g_{d0}$ shows a minimum for A_F around 1.35 while that of $S_{o,i_{gu}}(\omega_o)$ is decreasing with increasing A_F as shown in Fig.13. The total noise power density, due to the input transistor, normalized to $4kT\gamma g_{d0}$ shows a minimum between $A_F = 1.5$ and $A_F = 2$ that is possible for practical design. Adding all the total output noise power densities due to various noise sources and dividing the result by Eq.(23), the Noise Factor can be expressed as

$$F = 1 + \frac{R_l}{R_{src}} + \frac{R_g}{R_{src}} + \gamma g_{d0}R_{src}\frac{1+\frac{\delta\alpha^2}{5\gamma}\left(1+Q_L^2\right)+2\sqrt{\frac{\delta\alpha^2}{5\gamma}}|c|}{\left(A_F-1\right)^2+\left(A_F\frac{\omega_T}{\omega_o}\right)^2} + \gamma g_{d0}R_{src}\frac{f\left(A_F\right)}{\left(A_F-1\right)^2+\left(A_F\frac{\omega_T}{\omega_o}\right)^2} \quad (33)$$

where α and Q_L are defined respectively as

$$\alpha \equiv \frac{g_m}{g_{d0}} \quad (34)$$

and

$$Q_L = \frac{\omega_o\left(L_g+L_s\right)}{R_{src}}. \quad (35)$$

Q_L is called the input-Q of the circuit when the input circuit is considered as series-resonant network. The term $f\left(A_F\right)$ accounts for the existence of the gate-drain capacitance, i.e., $f\left(A_F\right) = 0$ when the gate-drain capacitance is neglected. Also note that for the traditional input matching method that ignores the gate-drain capacitance, $A_F = 1$, Eq.(33) reduce to the more familiar expression [5]. Shown in Fig.14 is the Noise Figure simulation result of the designed low noise amplifier. Note that due to the difficult to implement large high quality inductors, at least a portion or whole the gate inductor should be implemented with off-chip high quality inductor unless high quality on-chip inductor can be designed, otherwise, NF of the low noise amplifier could be degraded to an unacceptable level due to large R_l.

6. Conclusion

It is important to have good input matching in a low noise amplifier in order to have maximum input signal and better noise performance. However, without taking the gate-drain capacitance and the substrate coupling network of the input transistor into considerations, designers may require many iteration steps to achieve this goal. The effects of the gate-drain capacitance and the substrate coupling network are explored in this paper and a design method is proposed. The drain impedance comes into play due to the existence of the gate-drain capacitance and the substrate coupling network further complicate the design problem. In order to minimize the effect of the substrate coupling network, the drain impedance of the input transistor should be kept low enough. The drain impedance of the input transistor is then adjusted to achieve input matching without the need of iteration steps.

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