# Integrated Passive Components for RF Applications

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**Abstract**

*Integrated passive circuits consisting of precision thin film capacitors, resistors, and inductors optimized for RF applications have been successfully manufactured and characterized over the frequency range 50 MHz to 5 GHz. In the process of doing so, advances were made in a number of areas, including selection of substrate material for RF performance, thin film processing, simulation, and measurement techniques.*

Key words: Filters, passive networks, radio frequency (RF), inductors, capacitors, resistors.

Precision inductors, capacitors, and resistors suitable for RF applications have been integrated on a single substrate and assembled as part of active circuits. In addition, a low cost encapsulation technique has been demonstrated which mechanically ruggedizes the structure without significant change to performance.

Integrated passive components (IPCs) provide benefits for RF applications similar to the benefits realized with integrated circuits: the manufacturing cost is lower than assembled discrete parts, size is reduced, and parasitics are also reduced. The last point is especially important for RF applications, as parasitic effects tend to dominate behavior at high frequency. Mounted in a chip-on-board fashion (with active devices, perhaps more accurately chip-on-chip-on-board), the devices are compatible with existing advanced assembly lines.

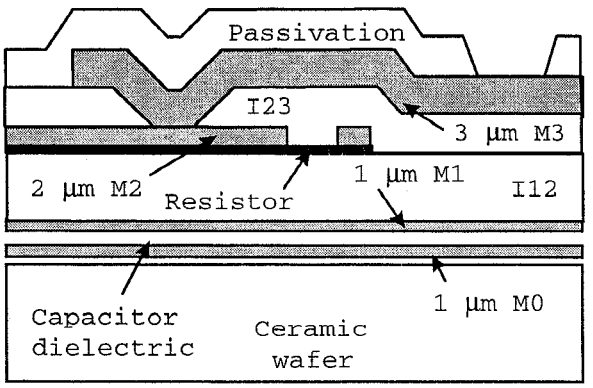



**Figure 1, Cross-section of IPC**

The process used was a modification of one developed by Flextronics for digital and mixed signal multi-chip modules [1]. The original process used a silicon wafer and included four aluminum layers and a thin-film capacitor. For integrated passives, a tantalum nitride resistor layer was added under the M2 routing layer, the M3 routing layer was thickened to 3 µm, and dielectric wafers of alumina ceramic were used (Figure 1). A total metal thickness of 7 µm is available through use of multiple layers, joined by vias. This approach reduces cost and maintains compatibility with conventional wafer processing equipment, compared to depositing a single thick conductor layer in addition to the other layers.

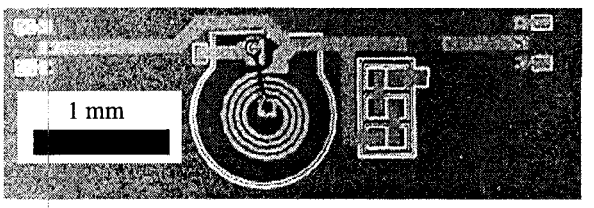



**Figure 2, Band-pass filter**

A variety of packaging methodologies have been successfully applied to our IPCs. Conventional molded plastic packages have been used to produce SMT devices containing purely passive networks. We have demonstrated chip-on-board attachment of our thin-film IPCs to standard PCBs (with gold plating), and we have mounted active die directly to the IPC (Figure 3). With epoxy encapsulation, these boards

have been soldered to conventional PCB boards and demonstrated in consumer hand-held applications.

Chip-on-board deserves a great deal of attention for hand-held and cost-sensitive applications. The issues to consider when evaluating it for a given application are not trivial, however [2]. Some of the lowest cost and highest volume consumer devices, such as calculators and watches, use chip-on-board. The cost of die attach, wirebond, and encapsulation, can be less than the $0.01 per pin that high volume plastic packaging typically costs. The greatest cost savings often comes from something other than the parts actually being integrated. For example, we have found that when integrating a keyboard into the PCB assembly, the gold plating needed for COB assembly also eliminated the need for expensive carbon ink previously used on the keyboard contacts.

There are also advantages in electrical performance with COB. The shorter wirebonds and elimination of the package leads will substantially reduce parasitic inductance. It also places the wirebonds nearer to a ground plane, further reducing emissions.

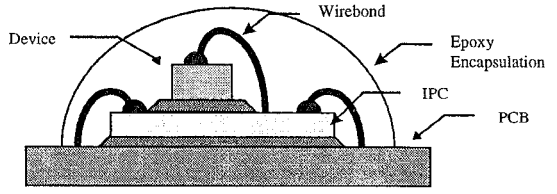
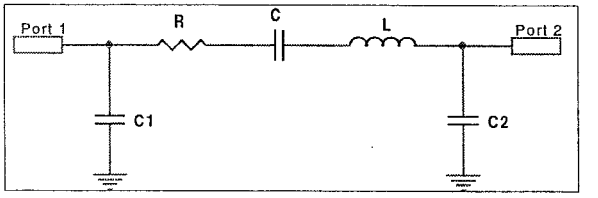



**Figure 3, Encapsulated Chip on Board assembly**

Capacitors in thin-film processes are often available at 10% tolerance, but have historically been difficult to manufacture to precision tolerances [3]. The anodization process[4] developed for MCM-D applications provides 500 pF per square millimeter with 3% tolerance[5] and greater than 40V breakdown. It is suitable for capacitors between 3 pF and 1 nF. Below 3 pF, metal etch tolerances begin to contribute more to capacitance variations than does dielectric thickness. However, multiple capacitors may be connected in series to produce precision capacitors of 1 pF or less. Above 1 nF, due to area occupied, the cost exceeds that of a placed SMT component.

Thin-film capacitors with $Al_2O_3$ dielectric were formed by anodization of a 1 μm aluminum layer (M0) and deposition of a second aluminum layer (M1). This results in an extremely well controlled non-polar capacitor with approximately 500 pF/mm$^2$. Measurement of the capacitance is not trivial, because low frequency measurements would not reflect the dielectric constant for RF frequencies, while high frequency measurement will show a significant effect from parasitic resistance and inductance. Therefore, analysis was performed to correlate nominal capacitor values with low frequency and RF measurements. The RF measurements show an effective capacitance which matches the reactive effect of both capacitance and inductance (at 50 MHz). The schematic shown had component values optimized (with Hewlett-Packard's EEsof Microwave Development System) until the response accurately matched measurements up to 5 GHz. (See Figure 4.)




| nom. C pF | C, 15 KHz pF | C, 50 MHz pF | RF model C1 pF | RF model C2 pF | RF model C pF | RF model R Ω | RF model L nH |
|---|---|---|---|---|---|---|---|
| 1.2 | 1.25 | 1.29 | 0.157 | 0.167 | 1.14 | 0.21 | 0.174 |
| 1.5 | 1.54 | 1.60 | 0.155 | 0.168 | 1.43 | 0.22 | 0.180 |
| 1.8 | 1.73 | 1.86 | 0.173 | 0.181 | 1.67 | 0.19 | 0.192 |
| 2.1 | 2.08 | 2.16 | 0.178 | 0.187 | 1.96 | 0.29 | 0.214 |
| 2.2 | 2.16 | 2.25 | 0.172 | 0.181 | 2.04 | 0.17 | 0.199 |
| 3.9 | 3.64 | 3.85 | 0.168 | 0.195 | 3.55 | 0.30 | 0.205 |
| 10 | 9.55 | 10.14 | 0.195 | 0.086 | 8.63 | 0.40 | 0.089 |
| 15 | 14.40 | 14.97 | 0.144 | 0.164 | 14.25 | 0.39 | 0.134 |

**Figure 4, Model of Capacitor**

Resistors which are embedded in a substrate must offer high yield and good tolerances, and preferably not require trimming. Tantalum nitride resistor films used in wafer processing can provide of the order of +/- 5% control, low thermal coefficient of resistance (approximately -140 ppm/°C), and high power handling capability (> 0.036 mW/μm$^2$). Additionally, they allow laser trimming (even through $SiO_2$ passivation) if 1% tolerances are required. However, many applications only require an accurate ratio of resistors, rather than absolute tolerances, and the as-deposited films provide 1% tracking of resistors within the area of a single device. This process had been previously used for fabrication of resistor packs for termination of 1 GHz digital signals[6], with 10 Ω/square material. For this application, a 100 Ω/square film was developed.

Resistors are formed with tantalum nitride, under the M2 layer. As deposited, the film offers +/- 5% tolerance. Additional variation in resistor value comes from critical dimension (CD) variations in resistor width and length. In design, there is therefore a tradeoff between area occupied and absolute tolerance. Tracking between resistors within a substrate is extremely tight, however, so long as they are laid out to match the effect of systematic variations (Figure 5).

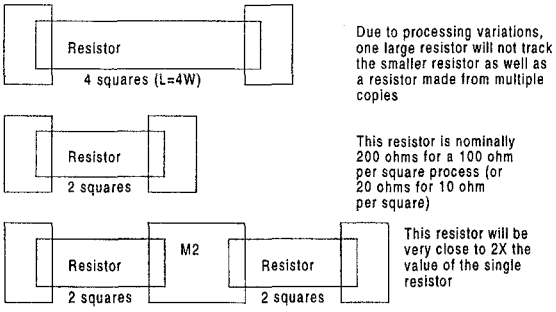
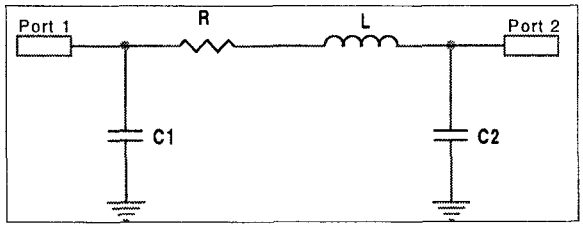



**Figure 5, Designing Resistors for Tracking**

Equivalent circuits were created to match the measured resistors across the frequency range 50 MHz to 5 GHz. These models were optimized by the same technique as the capacitor models.




| nom R Ω | DC R Ω | 50 MHz R Ω | RF model C1 pF | RF model C2 pF | RF model Ω | RF model L nH |
|---|---|---|---|---|---|---|
| 10 | 10.4 | 10.7 | 0.025 | 0.049 | 9.69 | 0.518 |
| 47 | 46.9 | 49.9 | 0.014 | 0.022 | 48 | 0.365 |
| 50 | 50.4 | 54.5 | 0.015 | 0.021 | 52.6 | 0.38 |
| 70 | 71.4 | 77.7 | 0.010 | 0.023 | 77.4 | 0.22 |
| 100 | 103.0 | 107 | 0.021 | 0.014 | 104 | 0.48 |
| 150 | 155.7 | 163 | 0.016 | 0.019 | 159 | 0.62 |
| 220 | 232.5 | 241 | 0.017 | 0.021 | 237 | 0.82 |
| 300 | 318.3 | 329 | 0.020 | 0.023 | 327 | 1.09 |
| 330 | 349.9 | 363 | 0.021 | 0.024 | 362 | 1.21 |
| 470 | 491.2 | 515 | 0.014 | 0.016 | 516 | 0.95 |
| 560 | 582.8 | 612 | 0.027 | 0.017 | 626 | 1.11 |

**Figure 6, Model of Resistor**

Inductors are among the most expensive passive components, and the magnetic field they create extends beyond their footprint, so placement on a board affects performance. Inductors are often integrated in boards where the cost/performance tradeoff is appropriate, but the footprint occupied tends to be large, and the magnetic field generated (as well as sensitivity to the fields of other inductors) is greater. Sometimes, inductors are replaced with striplines, at the expense of using blind vias in the PCB to avoid stubs. With thin-film processes, the area occupied by a spiral inductor is greatly reduced (as is the extent of the magnetic field), and often a cost savings over stripline techniques may be realized. Inexpensive dielectric substrates allow much higher Q inductors than semiconducting substrates and comparable to that of discrete components.

An array of spiral inductors ranging from 5 to 70 nH was designed, simulated, fabricated, and tested. Simulation was performed with the method of moments simulator Momentum, part of HP's EEsof design system. The optimization goal was maximum quality factor (Q), while minimizing area and keeping self resonant frequency sufficiently above the desired operating frequency. While inductor space would be minimized by continuing the spiral to the center, optimum Q was found to occur when the inner radius was approximately 1/3 the outer radius. Since the ground plane was extremely close to the inductor (7 μm), a circular cut-out was made in the ground plane. Although Q would increase (line length could decrease while holding inductance constant) for an arbitrarily large cutout, diminishing returns were found when the radius of the cutout was approximately 3/2 of the outer radius of the spiral. (See Figure 7, an optimized spiral inductor, shown with meshing for finite element analysis.) Wider conductors increase Q at the expense of area, and also reduce resonant frequency. Table 1 shows the size and Q for 50 nH inductors of various line widths. (Line space was 20 μm and thickness was 5.5 μm in all cases.)

**Table 1, Spiral inductors of various linewidths**

| Conductor Width | Ground Cutout Diameter | Q @ 200 MHz | Resonant Frequency (GHz) |
|---|---|---|---|
| 20 | 1470 | 12 | 1.77 |
| 30 | 1760 | 16 | 1.73 |
| 54 | 1960 | 23 | 1.58 |
| 100 | 3240 | 37 | 1.26 |
| 203 | 4870 | 58 | 0.87 |

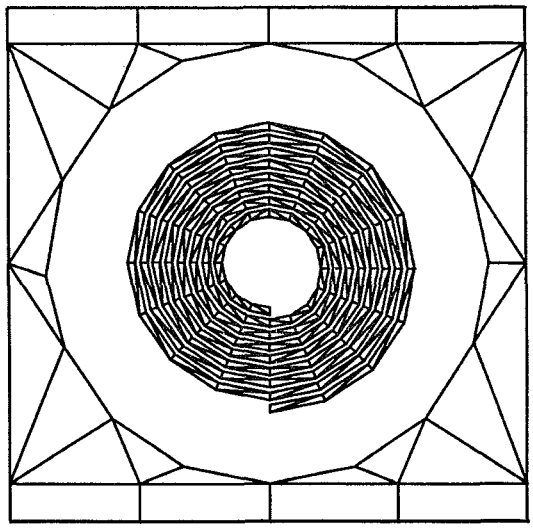


**Figure 7: Spiral inductor, meshed for simulation**

Escape from the center of the spiral was made with a 1 mil aluminum wirebond. For simulation purposes, this was approximated as a staple shape. The simulation resulted in inductance being 3% greater and Q being 18% greater than measured (Figure 8). The predicted accuracy of the inductance is quite satisfactory. The error in Q measurement or simulation is a concern, but does not prevent practical design for real applications.

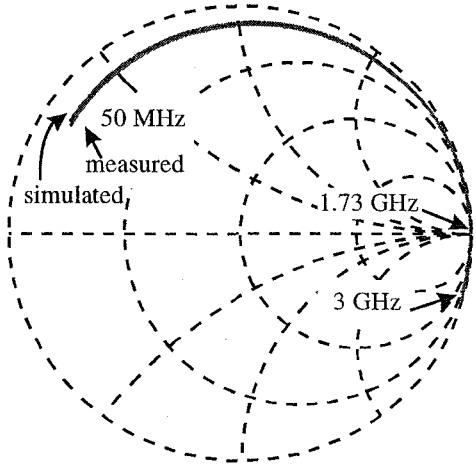



**Figure 8, Measured vs. Simulated Spiral Inductor**

An attempt was made to develop equivalent circuits for the inductors, as was done for resistors and capacitors. While 1-port measurements (with the second terminal of the inductor grounded) matched reasonably well, it was apparent that a simple model would not predict all four S-parameters of inductors measured in a 2-port fashion. The total dimensions and conductor length are large relative to wavelength, and mutual inductance is weak between inner and outer turns of the spiral inductor. We decided not to pursue developing more complicated models, and simply use measured or simulated S-parameters directly in our simulations.

Substrate materials play a significant role in integrated passive components. Roughness, thermal conductivity, and dielectric constant (or conductivity) all affect the performance of the circuit. Originally, work centered around silicon wafers, which are the least expensive substrates compatible with IC processing equipment and smooth enough for thin-film processing. However, parasitic capacitance to the lower terminal of pass capacitors was a concern, and spiral inductors formed over a semi-conducting ground plane were quite lossy. Ordinary ceramic wafers consisting of alumina were successfully used for interconnect, but, due to roughness, capacitor yield was poor. Attempts at planarizing the rough ceramic wafers by depositing $SiO_2$ and performing chemical-mechanical polishing (CMP) were unsuccessful, due to wafer bow. Polished ceramic wafers were found to be satisfactory and the most cost effective for the integrated passive process, however, they do constitute a sizable percentage of the finished wafer cost.

Design of integrated passive circuits requires accurate simulation of circuit behavior. Unlike discrete circuits, components can't easily be substituted until operation is satisfactory. One test pattern fabricated had both filters (Figure 2) and individual passive components (Figure 9) made from the same elements. Measurement was performed with an HP 8753D Vector Network Analyzer, Cascade Air Coplanar probes (Tungsten), and a Micro-Manipulator. Calibration was performed on a Cascade Impedance Standard Substrate, except that a shorting structure with aluminum metalization was used, to better match the contact resistance on the substrate under test. We have found that this avoids a systematic error in contact resistance which occurs when calibrating a tungsten probe on gold, then using it on aluminum. However, there is still a slight (ca. 50 m$\Omega$) variation in contact resistance, and this can be a significant factor when measuring low-loss elements. Measured S-parameters were brought into the HP EESOF Microwave Development System, where circuits simulated with libraries of individual passive elements were compared with measured filter circuits. With interconnect models properly accounted for, the correlation was excellent.

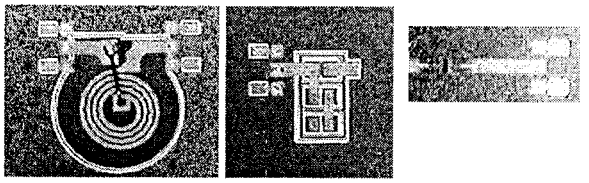



**Figure 9, Individual Components for Filter**

The mixed signal process, and variants, has been used for several applications. Filters consisting of LC and RLC elements are most appropriate for 100 MHz and higher frequency applications, because conductor dimensions allow inductors with performance comparable to discrete parts. Filters consisting of RC networks are applicable for a wider range of frequencies. In both cases, due to low parasitics, high frequency performance is superior to discrete parts.
Networks consisting of resistors and capacitors have been used for bus termination and EMI filters. One of the simplest devices is a 50 Ω parallel termination, used for ECL-level signals. It matches the 50 Ω line impedance, absorbing most of the energy so reflections (overshoot or undershoot) are minimized.
Another common device is the R-C-R "T" network, which implements a low-pass filter. It is used as a series terminator, reducing reflections and electro-magnetic interference (EMI).

One particularly appropriate application for RLC circuits in the mixed signal process is filters for intermediate frequency (IF) stage of a radio. The mixing products, which include RF +/- LO (local oscillator) as well as some RF and LO feed-through, are filtered to remove all frequencies except the desired IF (e.g. RF - LO). A band-pass filter is appropriate for this task. Two filters of this type were prototyped and tested.

The first one, a series LC circuit, had a 9 nH spiral inductor and a 1.5 pF capacitor. As measured, the filter showed insertion loss of 0.55 dB, and a center frequency of 1.38 GHz. Loaded with 50 Ω test equipment, the filter bandwidth was 1.6 GHz (Figure 10). Interconnect in the circuit contributed to loss, so lower loss and a narrower passband could have been achieved with a tighter layout. Individual inductors and capacitors were measured separately, and a simulation was run using these extracted models together with simulated models of interconnect. As shown in the graph, correlation with the measured filter circuit is excellent.

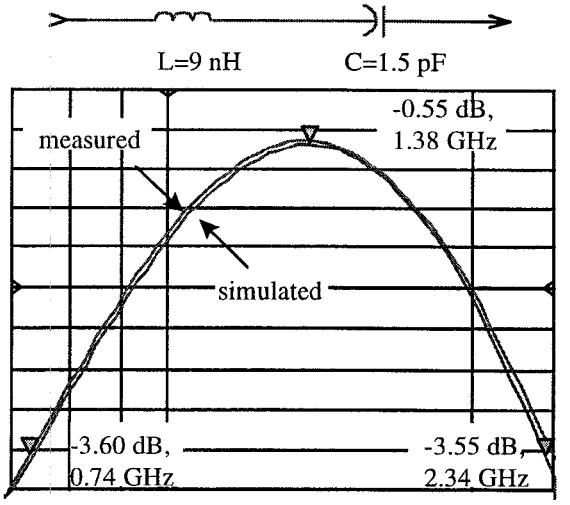



**Figure 10: Series LC filter**

The second filter circuit had parallel LC elements (also 9 nH and 1.5 pF) and a series 47 Ω resistor (Figure 11). At the center frequency of 0.98 GHz, insertion loss was 3.5 dB. The -3 dB bandwidth was 1.47 GHz. Both the filters had wide (100 μm) conductors to minimize loss, but with just 10 μm of dielectric between the microstrip and the ground plane, capacitance was high. This is shown dramatically by the difference in resonant frequency between these two filters. Since simulation accurately predicts this behavior, component values could be adjusted to correct the filter response.

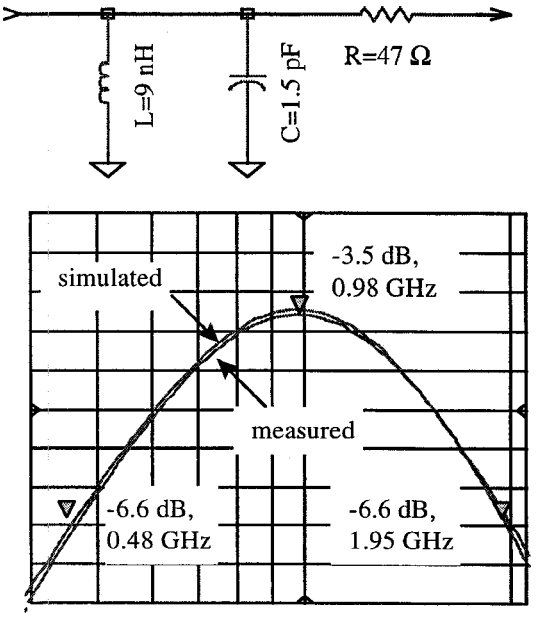



**Figure 11, Parallel LC filter with resistor**

These two filters were used in the RF and IF stages of a receiver circuit designed by Mayo Foundation.

A low pass filter was designed as part of a circuit for a commercial customer, with two capacitors and an inductor in a "π" configuration (Figure 12). At the frequency of operation for this filter, skin depth was on the order of 6 μm, so a spiral inductor implemented with M3, M2, and M0 in parallel (6 μm total) was adequate (although thicker metal would have improved performance, since not all current is confined to a single skin depth). The filter response was measured as -1.0 dB at $f_0$ and -8.0 dB at 2 x $f_0$.

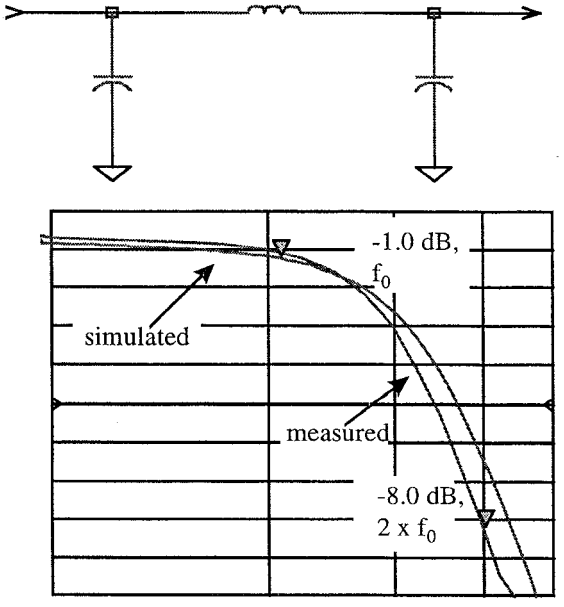



**Figure 12, CLC filter**

In conclusion, it has been demonstrated that Integrated Passive Components fabricated with thin film processes work satisfactorily for RF applications. Hand-held RF designs, especially, can receive substantial benefits in performance, size, and cost from the integration of passive devices as described here. What is more, models are sufficiently accurate that simulation allows first-pass success in designs.

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