LOGIC CIRCUIT DIAGRAM OF 2 TO 4 DECODER

TRUTH TABLE

E	A	B	OUTPUT(Z)
1	0	0	$Z_0 = \overline{A}\ \overline{B}$
1	0	1	$Z_1 = \overline{A}\ B$
1	1	0	$Z_2 = A\ \overline{B}$
1	1	1	$Z_3 = A\ B$
0	x	x	

A, B = Inputs
E = Enable
Z_0 to Z_3 = Outputs