Energy- and Area-Efficient 8T SRAM Cell with FEOL CFETs and BEOL-Compatible Transistors

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Abstract—High energy efficiency and capacity embedded SRAMs are essential for data-centric applications. CFET is remarkably scalable and has been proven to maintain the SRAM scaling track compared to nanosheet (NS) FET. However, the 6T CFET SRAM still suffers the read/write conflict and requires assist-circuits. This paper proposed an optimized 8T $CFET_{BEOL}$ SRAM cell integrated with FEOL CFETs and BEOL-compatible transistors. Compared to the 6T NS SRAM, the optimized 8T $CFET_{BEOL}$ SRAM cell shows 40% cell area reduction, 2.2 times higher RSNM, 1.68 times larger WSNM, 53% reduction in cell read access time, 27.8% decrease in dynamic energy, and 65.7% improvements in energy-delay product. The proposed energy- and area-efficient 8T $CFET_{BEOL}$ SRAM with fast speed, low dynamic energy, and superior stability could be promising candidates for high throughput data-centric applications.

I. Introduction

Data-centric applications which demand high energy efficiency drives rigorous requirements for high capacity embedded SRAM arrays operating at low supply voltage (V_{DD}). Large memory capacity and small cell area are required to increase the computing capabilities. Fig. 1 shows that the bit cell area of 6T FinFET (FF) and nanosheet (NS) SRAM cells continue to reduce as the technology node scales down [1-5]. However, the cell area reduction is slowing down because of a substantial space between nFET and pFET that needs to be preserved to ensure reliable device fabrication and manufacturability.

Complementary field effect transistor (CFET) by vertically stacking nFET and pFET eliminates the scaling barrier and brings SRAM density scaling on track compared to FF and NS [1-2]. Although the 6T CFET SRAM cell maintains the SRAM scaling trend, it is difficult to lower the minimum operation voltage (Vmin) of the 6T CFET SRAM due to the limitation of sharing the same read/write port. Besides, assist circuits are required for 6T CFET SRAM to reduce V_{DD}, which increases the dynamic energy due to assist circuits.

In this work, we propose an energy- and area-efficient 8T SRAM cell with FEOL CFET and BEOL-compatible transistors, i.e., $CFET_{BEOL}$ SRAM (Fig. 2). A back-gated (BG) gate topology is considered for BEOL transistors. The proposed 8T $CFET_{BEOL}$ SRAM cell preserves the advantage of reduced cell area compared to FF and NS SRAM cells. Moreover, there is no read/write conflict, and separating the read and write ports improve the read static noise margin (SNM). The write SNM can be enhanced by optimizing the pass-gate (PG) transistors and 8T write port [5], which also avoids the write assist-circuit energy overhead. We have analyzed several CFET-based SRAM cells with BEOL-compatible transistors compared with 6T CFET-only SRAM and 6T NS SRAM cells. This work demonstrates that the optimized 8T $CFET_{BEOL}$ SRAM cell with comparable cell area shows enhanced read and write SNM, improved read/write speed, and reduced energy-delay product (EDP) compared to 6T NS and 6T CFET-only SRAM cells.

II. Area-Efficient CFET-Based SRAMs and Layouts

The CFET SRAM with stacked n- and p-type NS has been proven to be a practical approach to maintaining the SRAM scaling trend. Fig. 3 shows the schematic of NS CFET, including two stacked NS to improve the driving capability of nFET and pFET, respectively. Several CFET-based SRAM cells in Table 1 have been analyzed compared to the baseline case (A) 6T NS SRAM cell. The corresponding SRAM circuits and layouts are shown in Fig. 4 and Fig. 5. Case (B) is 6T CFET SRAM by stacking pull-up (PU) above pull-down (PD) transistors, which reduces the track height and cell area. Fig. 5(b) shows the layout of 6T CFET SRAM cells, including 1st bottom layer PG/PD nFETs and 2nd top layer PU pFETs.

Three $CFET_{BEOL}$ SRAM cells, i.e., FEOL CFET combined with BEOL-compatible transistors, are analyzed to improve the stability, speed, and Vmin without increasing cell area. Stacking BEOL-compatible PG nFETs above PD/PU CFETs can further reduce the cell area of the case (C) 6T $CFET_{BEOL}$ SRAM cell. Since the cell area is shrunk, the maximum width of the BEOL PG transistor of case (C) is 22 nm, which may not provide sufficient strength of PG and need to optimize the BEOL PG FETs for case (C). Case (D) is a double word-line (DW) 8T $CFET_{BEOL}$ SRAM cell shown in Fig. 4(b) and Fig. 5(d). During the read operation, only RWL is activated, while during the write operation, both WWL and RWL are activated. Case (E) is the 8T $CFET_{BEOL}$ SRAM cell with separate read and write ports shown in Fig. 4(c) and Fig. 5(e). By utilizing BEOL-transistors for the read pass-gate (RPG, M7/M8) of case (D) and the read port M7/M8 nFETs of the case (E), the allowed maximum width of M7/M8 BEOL n-FETs is 36 nm.

Table 2 shows the design rules at the 2.1 nm node specified in IRDS [6]. The buried power rail (BPR) technique [7] for reducing the wire resistance and IR drop has been implemented for all SRAM cells in Fig. 5. Fig. 6 shows that the various CFET-based SRAM cells reduce the cell area by 40% and 55% compared to the baseline 6T NS SRAM cell. In other words, introducing BEOL-compatible transistors can: (1) further reduce the cell area of the 6T SRAM cell (case C) or (2) add extra transistors above the FEOL CFETs to provide extra functions without any area penalty (case D and E).

III. NS CFET, BEOL-Compatible Transistor, and Parasitic RC Extraction

Fig. 3 and Table 3 show the NS CFET structure and parameters at the 2.1 nm node [6], considering the inner spacer design. With NS CFET Si data calibration [8], the simulated I_{DS}-V_{GS} characteristics of NS CFETs are shown in Fig. 7. BEOL-compatible MOS transistors with a low thermal budget enable 3D integrations for SoC scaling. Fig. 8 shows the potential channel materials for BEOL-compatible transistors, such as two-dimensional materials, metal oxide semiconductors, carbon nanotube (CNT), recrystallized Si, etc. [9-14]. Various device structures, including back-gated (BG), double gate (DG), and gate-all-around (GAA), are explored to boost the driving capability of BEOL-compatible transistors. Conventional all Si 8T SRAM cells may show higher cell leakage currents than the 6T SRAM cell since more transistors are introduced in the bit cell. However, utilizing the ultra-low (~1fA/μm) OFF-state leakage IWO FETs [10-11] as the M7/M8 BEOL-compatible transistors for DW8T and 8T $CFET_{BEOL}$ SRAM cells can maintain comparable leakage power compared to the 6T NS and CFET SRAM cells.

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Fig. 9 shows the I_{DS}-V_{GS} characteristics of FEOL NS CFET and BEOL BG nFET for analyzing SRAM cells. The baseline threshold voltage (Vt) is designed with 0.35V for adequate SNM if not stated otherwise. Fig. 10 shows the 3D schematics of CFET-based SRAM cells for cases (B) to (E), including the FEOL CFET, BEOL-compatible transistors, BEOL interconnect, and BPR. 3D field solver and BEOL wire resistance and capacitance [6] are used for parasitic resistance and capacitance extraction. Fig. 11 shows the WL and BL capacitance and resistance per cell for various SRAMs. The case (A) 6T NS SRAM with a more significant track height and longer WL shows larger WL capacitance and resistance, degrading the WL activation delay. The CFET-based SRAM cells (case B to E) show lower or comparable resistance and capacitance than the baseline case (A).

IV. Energy-Efficient 8T $CFET_{BEOL}$ SRAM

A. Read and Write Static Noise Margin (SNM)

Fig. 12 shows the RSNM and WSNM comparisons. The bar chart data showcases the SRAM cells designed with baseline Vt (0.35V). As can be seen, the 6T $CFET_{BEOL}$, DW8T, and 8T $CFET_{BEOL}$ SRAM cells show larger RSNM than cases (A) 6T NS and (B) 6T CFET SRAM cells (~120 mV). During the read operation, the case (D) DW8T $CFET_{BEOL}$ SRAM cell turns on the RWL, which improves the read stability (142.7 mV) since the BEOL RPG (M7/M8) FETs are weaker than FEOL PD transistors, hence suppressing the read disturb voltage. Case (E) 8T $CFET_{BEOL}$ SRAM cell significantly improves RSNM by 2.2 times compared to cases (A) and (B) due to its separate read and write ports which eliminates the read disturb voltages.

For the write operation, the case (D) DW8T $CFET_{BEOL}$ SRAM cell shows 1.37 times more improvements in WSNM than case (A) because both WWL and RWL are turned on to improve the writability. Case (C) with baseline Vt design shows write failure due to its weaker BEOL PG transistors. However, case (C) can be optimized by adjusting the Vt of PG to 0.2V, which improves the writability and balances RSNM and WSNM. Case (E) 8T $CFET_{BEOL}$ SRAM cell can be optimized by reducing the Vt of FEOL PG to 0.2V for WSNM improvements (1.68 times) without degrading the RSNM. As can be seen, the optimized (E) 8T $CFET_{BEOL}$ SRAM cell shows superior RSNM (266.5 mV) and WSNM (312 mV) compared to other CFET-based SRAM cells.

B. Speed and Energy

During the read operation, the 6T and DW8T SRAM cells use a differential sense amplifier to sense the stored data. The 8T $CFET_{BEOL}$ SRAM cell using a decoupled single-ended read port with domino-style hierarchical read BL shows a fast read evaluation path. Fig. 13 shows the optimization guidelines of the case (E) 8T $CFET_{BEOL}$ SRAM cell. By reducing the Vt of PG (from 0.35 V to 0.2 V), stronger PG improves the WSNM from 185 mV to 312 mV (1.68 times). Moreover, by adjusting the Vt of BEOL M7/M8 FETs of the case (E) 8T $CFET_{BEOL}$ SRAM cell, the read access time and write time are improved by 42.6% and 9.8%, respectively, without degrading the read stability.

Fig. 14 shows the comparison of read access time and write time among various CFET-based SRAM cells. The read access time consists of WL activation and BL delays. The BL delay is defined as the time required for developing a 100 mV BL differential voltage for 6T and DW8T SRAM cells (or 100mV BL voltage drop for 8T $CFET_{BEOL}$ SRAM). The WL activation delay consists of the inverter buffer propagation delay and WL wire delay.

Compared to case (A) 6T NS SRAM cell, the case (B) CFET SRAM cell with a smaller cell area and shorter WL improves the WL activation delay, reducing the cell read access time and write time. Case (C) with baseline Vt design shows write failure due to its weaker PG transistors. However, the optimized case (C) 6T $CFET_{BEOL}$ SRAM with Vt of PG equal to 0.2V shows comparable cell read access time and write time compared to case (B) 6T CFET SRAM. Case (D) DW8T $CFET_{BEOL}$ SRAM with weaker RPG (M7/M8) shows longer cell read access time than case (B) 6T CFET SRAM. Reducing the Vt of RPG (M7/M8) for case (D) DW8T CFETBEOL SRAM is not practical because the stronger RPG improves the cell read access time while degrading the RSNM. As illustrated in Fig. 13, the proposed case (E) 8T $CFET_{BEOL}$ SRAM cell can be optimized to improve its WSNM, cell read access time, and write time without degrading the RSNM. The optimized (E) 8T $CFET_{BEOL}$ SRAM shows ~53% improvements in cell read access time and write time compared to the case (A) 6T NS SRAM cell. Fig. 15 compares the dynamic energy and energy-delay product (EDP). The dynamic energy, including the read and write energy, depends on the capacitance of the wire and access transistors. Owing to its reduced wire capacitance and improved speed, the optimized (E) 8T $CFET_{BEOL}$ SRAM cell shows 27.8% and 65.7% improvements in dynamic energy and EDP compared to case (A).

C. Improved Vmin and Benchmark

Fig. 16 compares the RSNM and WSNM between the optimized (E) 8T $CFET_{BEOL}$ SRAM and (B) 6T CFET SRAM cells considering various process corners. The Vt difference ($3\sigma_{Vt}$) between fast and slow corners is 90 mV. The fast N slow P (FNSP) is the most critical process corner for the read operation, and the slow N fast P (SNFP) is the most critical process corner for the write operation. As can be seen, by considering the FNSP and SNFP process corners, the optimized (E) 8T $CFET_{BEOL}$ SRAM cell still shows adequate RSNM and WSNM as V_{DD} scales down to below 0.3V. However, the case (B) 6T CFET SRAM cell with FNSP corner shows read failure as V_{DD} scales down to below 0.55V and the SNFP corner shows write failure as V_{DD} scales down to below 0.35V. In other words, the optimized (E) 8T $CFET_{BEOL}$ SRAM cell shows excellent potential for lowering Vmin.

Fig. 17 shows the visualized benchmarking of CFET-based SRAM cells in Table 1. The radar plot indicates the degree of improvements compared to case (A), the blue line shown in the radar plot. As can be seen, the optimized (E) 8T $CFET_{BEOL}$ SRAM cell shows the largest radar area, which means it surpasses the other CFET-based SRAM cells in terms of read speed, read/write stability, and EDP.

V. Conclusion

Energy- and area-efficient 8T $CFET_{BEOL}$ SRAM cell has been proposed for the first time to improve the cee area, speed, stability, energy efficiency, and Vmin of CFET-based SRAM cells. Utilizing the BEOL-compatible transistors combined with FEOL CFETs to separate the read and write ports improves the read stability. The proposed 8T $CFET_{BEOL}$ SRAM cell can be further optimized to improve the write stability and read/write speed without degrading the read stability and with no area penalty. The optimized 8T $CFET_{BEOL}$ SRAM cell achieves excellent performance in all aspects and may provide the path for energy-efficient computing serving data-centric and high-throughput applications.

Acknowledgment

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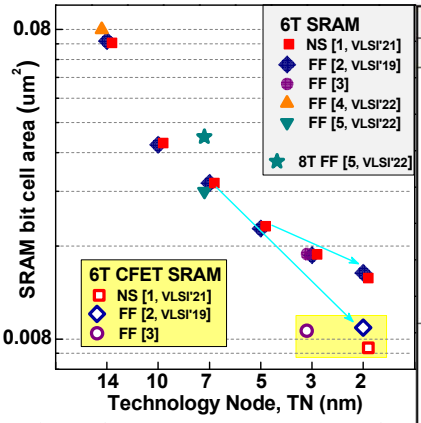

Fig. 1. The 6T CFET SRAM preserves the SRAM scaling trend compared to nanosheet (NS) and FinFET (FF) SRAM cells.

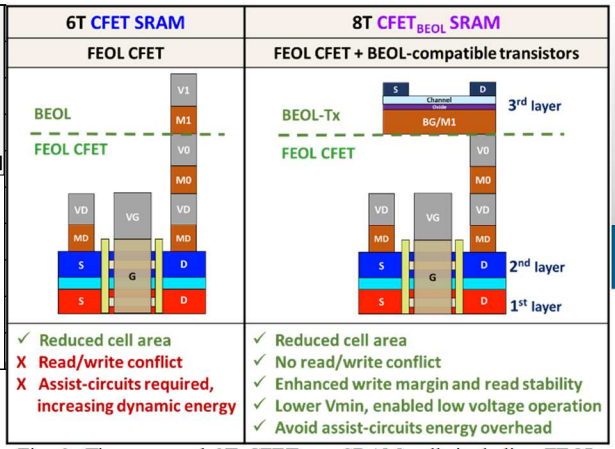

Fig. 2. The proposed 8T $CFET_{BEOL}$ SRAM cell, including FEOL monolithic NS CFET and BEOL-compatible transistors, shows great potential for low voltage operation.

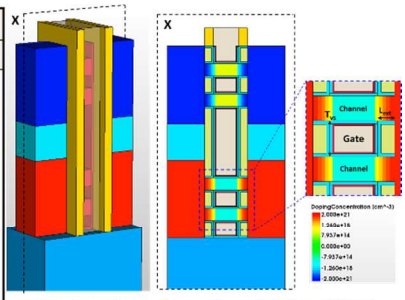

Fig. 3. The schematic of NS CFET includes two stacked nanosheets for 1st layer nFET (bottom-tier) and 2nd layer pFET (top-tier), respectively. The vertical space between two stacked NS channels (T_{VS}) is 10 nm. The inner spacer materials (SiO_2/nitride) reduce the parasitic capacitance compared to the entire nitride spacer.

PD = M1/M4, PU = M3/M6, PG = M2/M5

Case	SRAM cells	1st layer	2nd layer	3rd layer (BEOL)
(A)	6T NS	PD, PG, PU	--	--
(B)	6T CFET	PD, PG	PU	--
(C)	6T $CFET_{BEOL}$	PD	PU	PG
(D)	DW8T $CFET_{BEOL}$	PD, PG	PU	RPG (M7/M8)
(E)	8T $CFET_{BEOL}$	PD, PG	PU	M7/M8

Table 1. The baseline case (A) is the 6T NS SRAM cell with all six transistors built at the 1st layer. Case (B) is the 6T CFET SRAM with PD and PG at the 1st layer and PU at the 2nd layer. Various $CFET_{BEOL}$ SRAM cells are proposed and analyzed compared to cases (A) and (B).

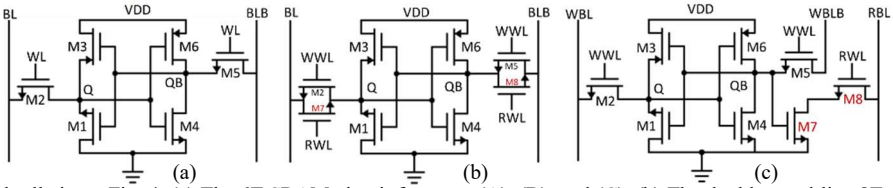

Fig. 4. (a) The 6T SRAM circuit for cases (A), (B), and (C). (b) The double word-line 8T SRAM circuit for case (D) DW8T $CFET_{BEOL}$ SRAM cell. M7/M8 are read pass-gate (RPG). (c) The 8T SRAM circuit for case (E) 8T $CFET_{BEOL}$ SRAM cell.

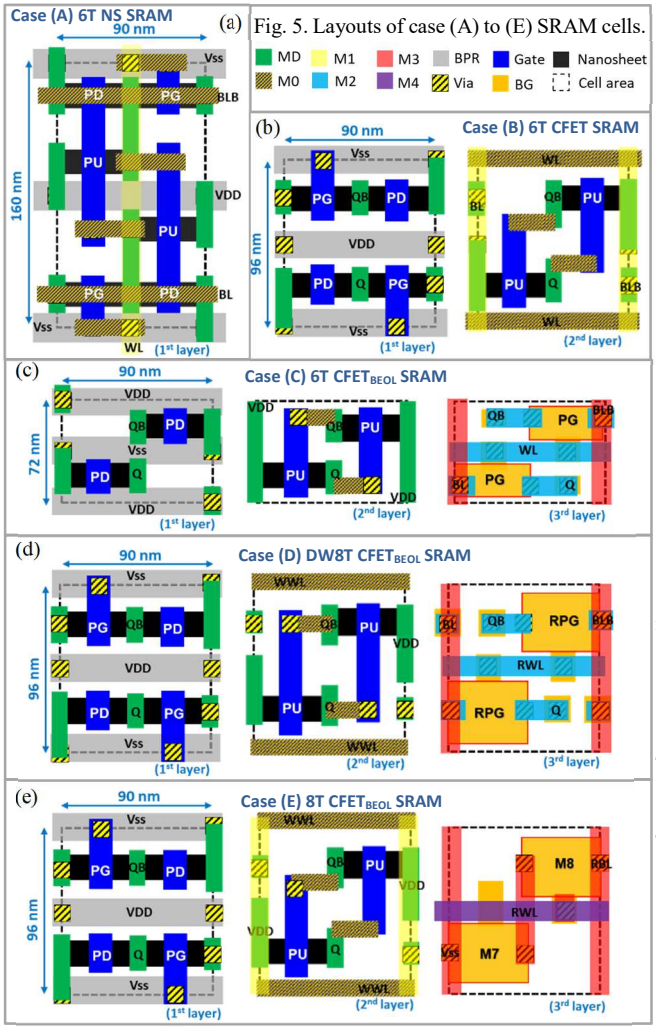

Fig. 5. Layouts of case (A) to (E) SRAM cells.

IRDS 2.1nm Design Rules	
Mx pitch / width (nm)	24 / 12
M1 pitch / width (nm)	23 / 11.5
M0 pitch / width (nm)	20 / 10
Gate pitch (nm)	45
BPR width / thickness (nm)	18 / 147

Table 2. Design rules for 2.1 nm node [6]. Buried power rail (BPR) [7] is considered for all SRAM cells listed in Table 1.

CFET Parameters	Value
Gate length, Lg (nm)	14
Nanosheet width, W_{NS} (nm)	15
Nanosheet thickness, T_{NS} (nm)	7
Extension length, L_{ext} (nm)	5
# of stacked NS	2
Vertical channel space, T_{VS} (nm)	10
N/P-FET space (nm)	20
N/P-FET space material	SiO_2
Inner spacer materials	SiO_2 / Nitride
Channel doping conc. (cm^{-3})	1×10^{16}
Substrate doping conc. (cm^{-3})	1×10^{19}
S/D & ext. doping conc. (cm^{-3})	1×10^{21} / 1×10^{17}
EOT (nm) (0.8nm SiO_2 / 0.5nm HfO_2)	0.81

Table 3. NS CFET device parameters at 2.1 nm node. Lg, W_{NS} and T_{NS} are specified in IRDS [6].

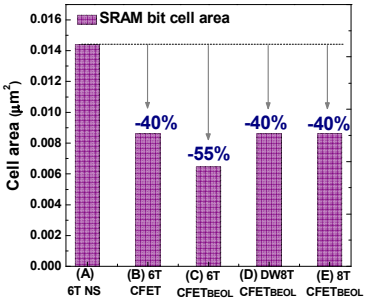

Fig. 6. CFET SRAM shows 40% and 55% cell reduction than NS SRAM. $CFET_{BEOL}$ cell shows the same cell area as CFET SRAM cell.

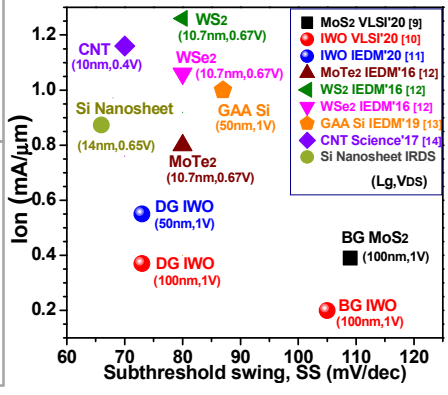

Fig. 8. Potential channel materials for BEOL-compatible transistors, such as two-dimensional materials, metal oxide semiconductors, carbon nanotube, recrystallized Si, etc. [8-13]. (DG: double gate, BG: back gate, GAA: gate-all-around)

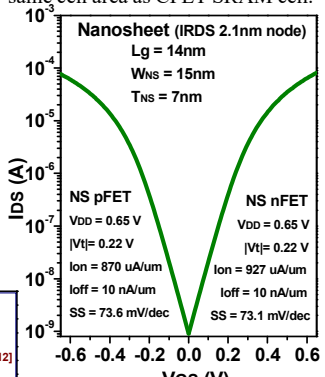

Fig. 7. The simulated I_{DS}-V_{GS} characteristics of NS FETs with |Vt| = 0.22V meet the high-performance Ion and Ioff requirements specified in IRDS.

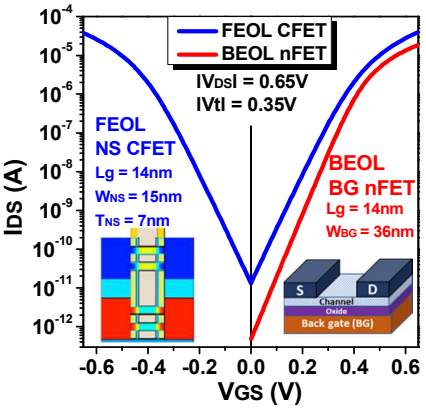

Fig. 9. For SRAM analysis, FEOL CFET and BEOL back-gated (BG) nFET are designed with $|V_{th}|$ = 0.35V if not stated otherwise.

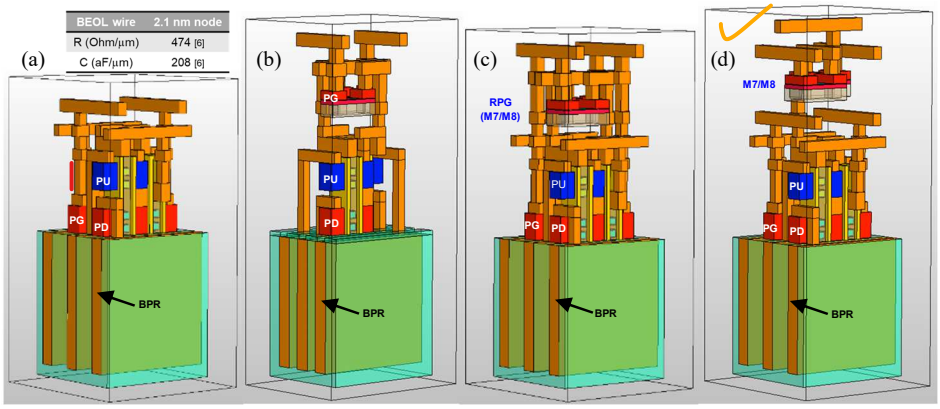

Fig. 10. 3D SRAM schematics for BEOL RC extraction. The 3D structures include FEOL CFETs, BEOL transistors, buried power rail (BPR) and BEOL interconnect for (a) 6T CFET SRAM, (b) 6T $CFET_{BEOL}$ SRAM, (c) DW8T $CFET_{BEOL}$ SRAM, and (d) 8T $CFET_{BEOL}$ SRAM cells.

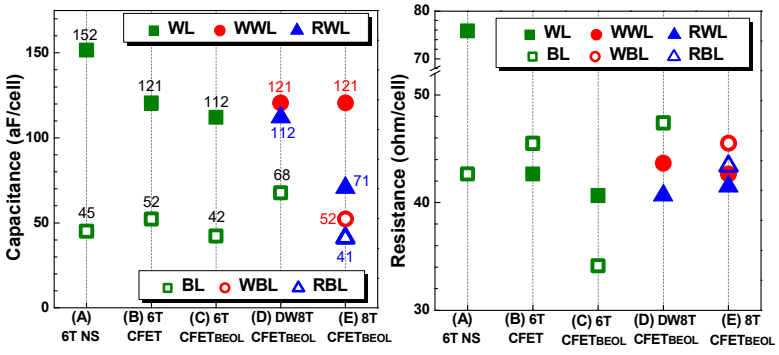

Fig. 11. (a) SRAM WL and BL capacitance, including the metal wire capacitance and access device capacitance. (b) SRAM wire resistance at TN = 2.1nm.

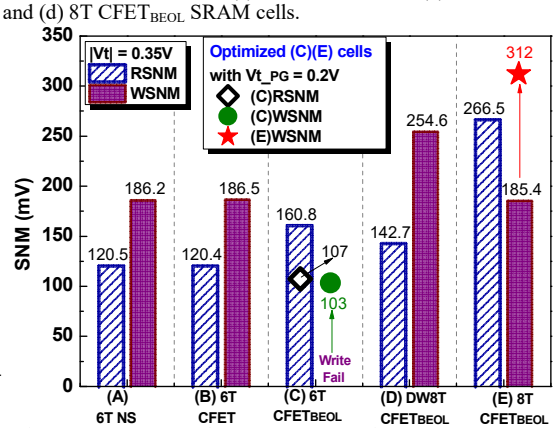

Fig. 12. RSNM and WSNM comparisons. Case (C) 6T $CFET_{BEOL}$ cell with |Vt| = 0.35V fails to write. The optimized case (C) and (E) are analyzed by changing the Vt of PG to 0.2V.

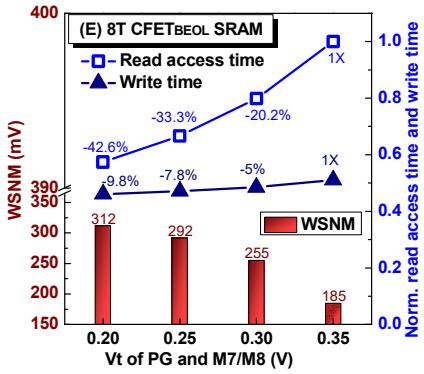

Fig. 13. Decreasing Vt of PG and M7/M8 improves WSNM and read/write speed. The optimized (E) SRAM is designed with Vt = 0.2 for PG (M2/M5), M7, and M8.

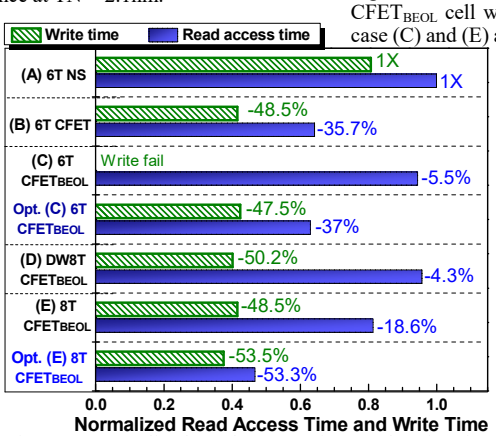

Fig. 14. Normalized read access time and write time comparisons. The optimized (E) 8T $CFET_{BEOL}$ SRAM exhibits significant improvements in speed.

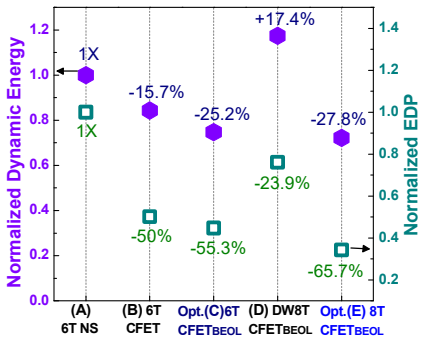

Fig. 15. Normalized dynamic energy and energy-delay product (EDP) comparisons. The opt. (E) 8T $CFET_{BEOL}$ shows significant improvements in EDP.

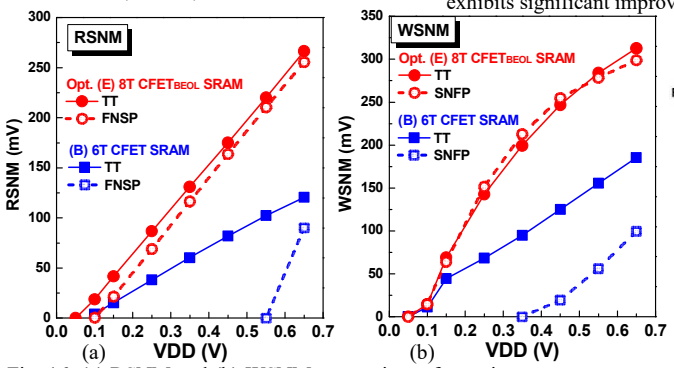

Fig. 16. (a) RSNM and (b) WSNM comparisons for various process corners. The Vt difference ($3\sigma_{Vt}$) between Fast and Slow corners is 90mV. The opt. (E) 8T $CFET_{BEOL}$ SRAM maintains adequate RSNM and WSNM at the worst process corners, which improve read Vmin and write Vmin.

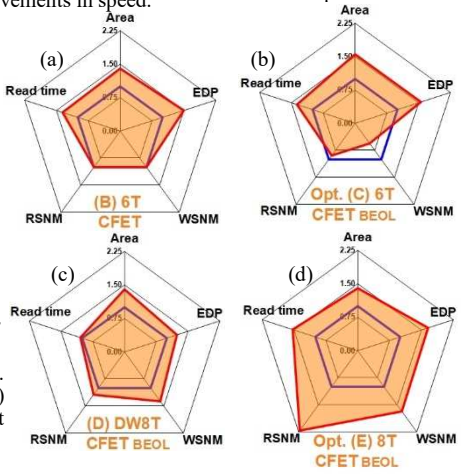

Fig. 17. Visualized benchmarking of CFET-based SRAM cells. The radar plot indicates the degree of improvements compared to case (A) 6T NS SRAM (blue line in the radar plot). A larger orange area in the radar plot is better, which means more significant improvements. The opt. (E) 8T $CFET_{BEOL}$ SRAM shows 2.2X and 1.7X improvements in RSNM and WSNM. The read time, EDP, and area are improved by 53.3%, 4 65.7%, and 40% compared to case (A).