

HSPICE® Reference Manual: MOSFET Models

Version I-2013.12, December 2013

SYNOPSYS®

Copyright and Proprietary Information Notice

Copyright © 2012 Synopsys, Inc. All rights reserved. This software and documentation contain confidential and proprietary information that is the property of Synopsys, Inc. The software and documentation are furnished under a license agreement and may be used or copied only in accordance with the terms of the license agreement. No part of the software and documentation may be reproduced, transmitted, or translated, in any form or by any means, electronic, mechanical, manual, optical, or otherwise, without prior written permission of Synopsys, Inc., or as expressly provided by the license agreement.

Destination Control Statement

All technical data contained in this publication is subject to the export control laws of the United States of America. Disclosure to nationals of other countries contrary to United States law is prohibited. It is the reader's responsibility to determine the applicable regulations and to comply with them.

Disclaimer

SYNOPSYS, INC., AND ITS LICENSORS MAKE NO WARRANTY OF ANY KIND, EXPRESS OR IMPLIED, WITH REGARD TO THIS MATERIAL, INCLUDING, BUT NOT LIMITED TO, THE IMPLIED WARRANTIES OF MERCHANTABILITY AND FITNESS FOR A PARTICULAR PURPOSE.

Trademarks

Synopsys and certain Synopsys product names are trademarks of Synopsys, as set forth at <http://www.synopsys.com/Company/Pages/Trademarks.aspx>.

All other product or company names may be trademarks of their respective owners.

Synopsys, Inc.
700 E. Middlefield Road
Mountain View, CA 94043
www.synopsys.com

Contents

| | |
|--|------|
| Conventions | xiii |
| Customer Support | xiv |
| <hr/> | |
| 1. Overview of MOSFET Models | 1 |
| MOSFET Model Usage | 1 |
| HSPICE and MOSFET Libraries | 2 |
| MOSFET Device Definition | 3 |
| HSPICE Automatic Model Selector | 6 |
| General MOSFET Model Statement | 8 |
| Model Name Identification Rule | 10 |
| Measuring the Value of MOSFET Model Card Parameters | 10 |
| Using a Model Card Defined with a Subckt Wrapper | 10 |
| MOSFET Capacitors | 11 |
| MOSFET Diodes | 13 |
| MOSFET Control Options | 13 |
| Scale Units | 14 |
| Bypass Option for Latent Devices | 15 |
| Searching Models as Function of W, L | 16 |
| Number of Fingers, WNFLAG Option | 17 |
| MOSFET Output Templates | 19 |
| Output Templates for BSIM-CMG, Level 72 | 30 |
| Output Templates for HiSIM_HV, Level=73 | 35 |
| Output Templates for UTSoI, Level=76 | 39 |
| Additional Output Templates for PSP and Other Models | 41 |
| MOSFET SUBCKT Output Templates | 45 |
| Safe Operating Area Voltage Warning | 48 |
| Model Pre-Processing and Parameter Flattening | 49 |
| Use of Example Syntax | 49 |

Contents

| | |
|---|-----------|
| 2. MOSFET Models | 51 |
| Common MOSFET Model Parameters | 54 |
| LEVEL 1: Schichman-Hodges Model. | 69 |
| Schichman-Hodges Model Parameters | 69 |
| Schichman-Hodges Model Equations | 69 |
| LEVEL 2: MOS2 Grove-Frohman (SPICE 2G) Model | 71 |
| Grove-Frohman (SPICE 2G) Model Parameters | 71 |
| Grove-Frohman (SPICE 2G) Model Equations | 71 |
| LEVEL 3: MOS3 Empirical Model (SPICE 2G) | 77 |
| MOS3 Empirical Model Parameters | 77 |
| MOS3 Empirical Model Equations | 77 |
| MOS3 Empirical Model — Compatibility Notes | 82 |
| MOS3 Empirical Model — Temperature Compensation Example | 83 |
| LEVEL 4: Grove-Frohman-LEVEL 2 Model Derived from SPICE 2E.3 | 86 |
| LEVEL 5: AMI-ASPEC Depletion and Enhancement (Taylor-Huang) Model | 87 |
| AMI-ASPEC Model Parameters | 87 |
| AMI-ASPEC Model Equations — Cutoff Region ($V_{gs} < V_{th}$) | 88 |
| AMI-ASPEC Model Equations — Depletion ($V_{gs} - V_{fb} < 0$) | 92 |
| AMI-ASPEC Model — Depletion Mode DC Model, ZENH=0 | 98 |
| LEVEL 6: Lattin-Jenkins-Grove (ASPEC) Model | 100 |
| Lattin-Jenkins-Grove (ASPEC) Model Parameters | 100 |
| Lattin-Jenkins-Grove (ASPEC) Model — UPDATE Parameter | 101 |
| Lattin-Jenkins-Grove (ASPEC) Model Equations, (UPDATE=0 or 2) | 103 |
| Lattin-Jenkins-Grove (ASPEC) Model Equations, UPDATE=1 | 114 |
| Lattin-Jenkins-Grove (ASPEC) Model — Compatibility Notes | 126 |
| LEVEL 7: Lattin-Jenkins-Grove (SPICE) Model. | 128 |
| LEVEL 8: Advanced LEVEL 2: MOS2 Grove-Frohman Model (SPICE 2G). | 129 |
| Advanced LEVEL 2: MOS2 Grove-Frohman (SPICE 2G) Model Parameters | 129 |
| Advanced LEVEL 2: MOS2 Grove-Frohman (SPICE 2G) — Model Equations | |
| 130 | |
| LEVEL 13: BSIM Model | 136 |
| BSIM Model Features | 136 |
| BSIM Model Parameters | 137 |
| BSIM Model — Sensitivity Factors | 142 |
| BSIM Models — .MODEL VERSION Changes | 143 |

| | |
|--|-----|
| BSIM Model Equations..... | 143 |
| BSIM Model — Charge-Based Capacitance Model..... | 147 |
| BSIM Model — Preventing Negative Output Conductance | 151 |
| BSIM Model Calculations..... | 151 |
| BSIM Model — Compatibility Notes..... | 153 |
| LEVEL 27: SOSFET Model | 160 |
| SOSFET Model Parameters..... | 161 |
| SOSFET Model — Non-Fully Depleted SOI Model | 163 |
| SOSFET Model — Components | 163 |
| SOSFET Model — Obtaining Model Parameters..... | 164 |
| SOSFET Model — Fully Depleted SOI Model Considerations | 167 |
| SOSFET Model — Example | 168 |
| LEVEL 28: BSIM Derived Model | 171 |
| BSIM Derived Model Parameters..... | 171 |
| BSIM Derived Model Equations | 177 |
| LEVEL 38: Cypress Depletion Model..... | 182 |
| Cypress Depletion Model Parameters | 184 |
| Cypress Depletion Model Equations | 184 |
| Cypress Depletion Model — Sample Model File | 190 |
| LEVEL 39: BSIM2 Model..... | 192 |
| BSIM2 Model Parameters | 192 |
| BSIM2 Model Equations..... | 196 |
| BSIM2 Model — Geometry and Bias of Model Parameters..... | 199 |
| BSIM2 Model — Compatibility Notes..... | 200 |
| BSIM2 Model — Preventing Negative Output Conductance | 202 |
| BSIM2 Model — Charge-based Gate Capacitance Model (CAPOP=39) | 203 |
| BSIM2 Model — Synopsys Device Model Enhancements..... | 204 |
| BSIM2 Model — Modeling Example | 208 |
| BSIM2 Model — Typical Listing | 212 |
| LEVEL 40: HP a-Si TFT Model | 215 |
| Using the HP a-Si TFT Model | 215 |
| HP a-Si TFT Model Equations | 217 |
| HP a-Si TFT Model — Device Model and Element Statement Example . | 222 |
| LEVEL 47: BSIM3 Version 2 MOSFET Model..... | 223 |
| Using the BSIM3 Version 2 MOSFET Model | 223 |
| BSIM3 Version 2 MOSFET Model Parameters | 223 |
| BSIM3 Version 2 MOSFET Model Equations..... | 227 |

Contents

| | |
|---|-----|
| BSIM3 Version 2 MOSFET Model — Usage Notes | 234 |
| BSIM3 Version 2 MOSFET Model — PMOS Model Example | 236 |
| LEVEL 49 and 53: BSIM3 Version 3 MOSFET Model | 238 |
| BSIM3 Version 3 MOSFET Model — Selecting Model Versions | 239 |
| BSIM3 Version 3.x MOSFET Model Features | 242 |
| Using BSIM3 Version 3 MOSFET Model | 244 |
| BSIM3 Version 3 MOSFET Model — Usage Notes | 246 |
| BSIM3 Version 3 MOSFET Model Parameters | 261 |
| BSIM3 Version 3 MOSFET Model — Parameter Range Limits | 272 |
| BSIM3 Version 3 MOSFET Model Equations. | 275 |
| BSIM3 Version 3 MOSFET Model — Additional Information | 276 |
| BSIM3 Version 3 MOSFET Model Examples. | 278 |
| LEVEL 50: Philips MOS9 Model | 280 |
| Philips MOS9 Model Parameters | 280 |
| Philips MOS9 Model — JUNCAP Parameters | 285 |
| Using the Philips MOS9 Model | 286 |
| Philips MOS9 Model — Example | 287 |
| LEVEL 54: BSIM4 MOSFET Model | 289 |
| BSIM4 MOSFET Model — General Syntax | 289 |
| BSIM4 MOSFET Model Parameters | 289 |
| BSIM4 MOSFET Model — Usage Notes | 291 |
| BSIM4 MOSFET Model — Version Updates | 323 |
| BSIM4 MOSFET Model — Output Templates | 329 |
| LEVEL 55: EPFL-EKV MOSFET Model | 330 |
| EPFL-EKV MOSFET Model — Single Equation Model | 330 |
| EPFL-EKV MOSFET Model — Effects Modeled | 331 |
| EPFL-EKV MOSFET Model — Coherence of Static and Dynamic Models | 331 |
| EPFL-EKV MOSFET Model — Bulk Reference and Symmetry. | 332 |
| EPFL-EKV MOSFET Model — EKV Intrinsic Model Parameters. | 333 |
| EPFL-EKV MOSFET Model — Static Intrinsic Model Equations. | 337 |
| EPFL-EKV MOSFET Model — Quasi-static Model Equations. | 348 |
| EPFL-EKV MOSFET Model — Intrinsic Noise Model Equations. | 351 |
| EPFL-EKV MOSFET Model — Operating Point Information | 351 |
| EPFL-EKV MOSFET Model — Estimation and Limits of Static Intrinsic Model Parameters. | 353 |
| EPFL-EKV MOSFET Model Updates. | 355 |
| LEVEL 57: BSIM3 SOI Model | 357 |
| BSIM3 SOI Model — General Syntax | 358 |

| | |
|--|-----|
| BSIM3 SOI Model Parameters | 360 |
| BSIM3 SOI Model — Range Limit Parameters | 370 |
| BSIM3 SOI Model — Version Updates | 376 |
| BSIM3 SOI Version 3.2 Updates | 376 |
| BSIM3 SOI Version 3.1 Updates | 381 |
| BSIM3 SOI Model — PD Version Updates | 385 |
| BSIM3 SOI Model — Output Templates. | 387 |
| LEVEL 58: UFSOI MOSFET Model. | 388 |
| UFSOI Model — FDSOI Parameters | 389 |
| UFSOI Model — NFDSOI Parameters. | 393 |
| UFSOI MOSFET Model Template | 398 |
| LEVEL 59: BSIM3 SOI FD Model | 399 |
| BSIM3 SOI FD Model — General Syntax | 399 |
| BSIM3 SOI FD Model Parameters. | 400 |
| BSIM3 SOI FD Model — Template Output. | 407 |
| LEVEL 60: BSIM3 SOI DD Model | 408 |
| BSIM3 SOI DD Model — Features | 408 |
| BSIM3 SOI DD Model — General Syntax | 409 |
| BSIM3 SOI DD Model Parameters. | 410 |
| LEVEL 61: RPI a-Si TFT Model. | 419 |
| RPI a-Si TFT Model Features | 419 |
| Using RPI a-Si TFT Model with Synopsys Simulators | 420 |
| RPI a-Si TFT Model Parameters | 421 |
| RPI a-Si TFT Model Equations | 422 |
| LEVEL 62: RPI Poli-Si TFT Model. | 425 |
| RPI Poli-Si TFT Model Features | 425 |
| Using RPI Poli-Si TFT Model with Synopsys Simulators | 426 |
| RPI Poli-Si TFT Model Parameters | 427 |
| RPI Poli-Si TFT Model Equations. | 431 |
| RPI Poli-Si TFT Model Version 2 Equations. | 437 |
| LEVEL 63: Philips MOS11 Model | 442 |
| Using the Philips MOS11 Model | 443 |
| Philips MOS11 Model Parameters. | 444 |
| Philips MOS11 Model Examples | 461 |
| LEVEL 64: STARC HiSIM MOSFET Model | 464 |
| STARC HiSIM Model Parameters | 465 |
| LEVEL 65: SSIMSOI Model. | 476 |

Contents

| | |
|---|-----|
| Using SSIMSOI Model with HSPICE | 476 |
| SSIMSOI Model — General Syntax | 476 |
| SSIMSOI Model Parameters | 477 |
| LEVEL 66: HSPICE HVMOS Model | 486 |
| HSPICE HVMOS Model — General Syntax | 486 |
| HSPICE HVMOS Model Parameters | 487 |
| LEVEL 68: STARC HiSIM2 MOSFET Model | 489 |
| STARC HiSIM2 Model — General Syntax (All Versions) | 489 |
| STARC HiSIM2 Model Parameters | 490 |
| STARC HiSIM2 Model Instance Parameters | 507 |
| STARC HiSIM2 Model Updates | 508 |
| LEVEL 69: PSP Model | 518 |
| PSP Model Features | 518 |
| PSP Model Updates | 519 |
| Using PSP Model in HSPICE | 523 |
| PSP 103.1 Model Parameters | 524 |
| PSP 103.1 Instance Parameters | 560 |
| PSP Model — Output Templates | 561 |
| LEVEL 70: BSIMSOI4 Model | 563 |
| BSIMSOI4 Model — General Syntax | 564 |
| BSIMSOI4 Model Parameters | 564 |
| BSIMSOI4 Model — Parameter Range Limit | 583 |
| BSIMSOI4 Model — Version Updates | 589 |
| LEVEL 71: TFT Model | 592 |
| TFT Model — General Syntax | 592 |
| TFT Model Parameters | 593 |
| LEVEL 72: BSIM-CMG MOSFET Model | 605 |
| BSIM-CMG Model — General Syntax | 606 |
| BSIM-CMG Model — Version Updates | 606 |
| BSIM-CMG Model Parameters (Version >= 105) | 614 |
| BSIM-CMG Model Parameters (Version < 105) | 638 |
| BSIM-CMG Model (Version=105.03) — WPE Model Support | 652 |
| BSIM-CMG Model — Deactivating Model Equations | 653 |
| BSIM-CMG Model — Searching Models as Function of NFIN and L | 655 |
| BSIM-CMG Model — Binning Calculation | 655 |
| BSIM-CMG Model — Additional Operating Point Outputs | 656 |
| LEVEL 73: HiSIM_HV Model | 658 |

| | |
|--|-----|
| HiSIM_HV Model — General Syntax | 661 |
| HiSIM_HV Model Parameters | 662 |
| HiSIM_HV Model Updates | 667 |
| HiSIM_HV Model — Template Output | 681 |
| LEVEL 74: MOS Model 20 Model | 682 |
| MOS Model 20 Model — General Syntax | 682 |
| MOS Model 20 Model — Instances and Parameters | 682 |
| LEVEL 76: LETI-UTSOI MOSFET Model | 690 |
| LETI-UTSOI MOSFET Model Updates | 691 |
| UTSOI MOSFET Model — Global Model Flags and Parameters | 693 |
| UTSOI MOSFET Model — Local Level Parameters (SWSCALE=0) | 694 |
| UTSOI MOSFET Model — Global Level Parameters (SWSCALE=1) | 700 |
| LEVEL 77: BSIM6 MOSFET Model | 712 |
| BSIM6 MOSFET Model — General Syntax | 712 |
| BSIM6 MOSFET Model Parameters | 713 |
| BSIMx and BSIMx SOI — Supported Instance Parameters | 735 |
| References | 739 |
| <hr/> | |
| 3. MOSFET Capacitance Models | 741 |
| MOS Gate Capacitance Models | 742 |
| Selecting Capacitor Models | 742 |
| Transcapacitance | 744 |
| Operating Point Capacitance Printout | 746 |
| Element Template Printout | 747 |
| Calculating Gate Capacitance | 748 |
| Gate Capacitance — Input File | 749 |
| Gate Capacitance — Calculations | 749 |
| Gate Capacitance — Results | 751 |
| Gate Capacitance — Plotting Gate Capacitances | 751 |
| Gate Capacitance — Control Options | 752 |
| Gate Capacitance — Scaling | 753 |
| MOSFET Gate Capacitance — Model Parameters | 753 |
| Specifying XQC and XPART for CAPOP=4, 9, 11, 12, 13 | 755 |
| Overlap Capacitance Equations | 756 |

Contents

| | |
|---|------------|
| CAPOP=0 — SPICE Meyer Gate Capacitances | 757 |
| CAPOP=1 — Modified Meyer Gate Capacitances | 759 |
| CAPOP=2—Parameterized Modified Meyer Capacitance | 762 |
| CAPOP=3 — Gate Capacitances (Simpson Integration) | 766 |
| CAPOP=4 — Charge Conservation Capacitance Model | 768 |
| CAPOP=5 — No Gate Capacitance | 773 |
| CAPOP=6 — AMI Gate Capacitance Model | 774 |
| CAPOP=13 — BSIM1-based Charge-Conserving Gate Capacitance Model | 775 |
| CAPOP=39 — BSIM2 Charge-Conserving Gate Capacitance Model | 776 |
| Calculating Effective Length and Width for AC Gate Capacitance | 776 |
| | |
| 4. MOSFET Diode Models | 777 |
| Selecting MOSFET Diode Models | 777 |
| Enhancing Convergence | 778 |
| MOSFET Diode Model Parameters | 778 |
| Using an ACM=0 MOS Diode | 781 |
| Calculating Effective Areas and Peripheries | 783 |
| Calculating Effective Saturation Current | 783 |
| Calculating Effective Drain and Source Resistances | 783 |
| Using an ACM=1 MOS Diode | 784 |
| Calculating Effective Areas and Peripheries | 785 |
| Calculating Effective Saturation Current | 786 |
| Calculating Effective Drain and Source Resistances | 786 |
| Using an ACM=2 MOS Diode | 787 |
| Calculating Effective Areas and Peripheries | 788 |
| Calculating Effective Saturation Currents | 789 |
| Calculating Effective Drain and Source Resistances | 790 |
| Using an ACM=3 MOS Diode | 790 |
| Calculating Effective Areas and Peripheries | 791 |
| Effective Saturation Current Calculations | 792 |
| Effective Drain and Source Resistances | 792 |
| MOS Diode Equations | 792 |
| DC Current | 793 |
| Using MOS Diode Capacitance Equations | 793 |

| | |
|---|-----|
| 5. CMC MOS Varactor Model | 797 |
| LEVEL 7: CMC Varactor Model | 797 |
| CMC Varactor Model Parameters | 798 |
| | |
| 6. MOSFET Noise Models | 803 |
| MOSFET Model — Noise Parameters | 803 |
| MOSFET Model — Noise Equations | 804 |
| | |
| A. Technology Summary for HSPICE MOSFET Models | 807 |
| MOSFET Equivalent Circuits | 807 |
| Equation Variables | 808 |
| Using MOSFET Current Convention | 809 |
| Using MOSFET Equivalent Circuits | 810 |
| MOSFET DC Operating Point Output | 814 |
| Common Threshold Voltage Equations | 817 |
| Common Threshold Voltage Parameters | 817 |
| Calculating PHI, GAMMA, and VTO | 818 |
| MOSFET Impact Ionization | 819 |
| Calculating the Impact Ionization Equations | 820 |
| Calculating Effective Output Conductance | 821 |
| Cascoding Example | 822 |
| Cascode Circuit | 823 |
| Temperature Parameters and Equations | 823 |
| Temperature Parameters | 824 |
| MOS Temperature Coefficient Sensitivity Parameters | 825 |
| Temperature Equations | 826 |
| | |
| Index | 831 |

Contents

About this Manual

This manual describes available MOSFET models that you can use when simulating your circuit designs in HSPICE.

The material covered includes:

- Design model and simulation aspects of MOSFET models.
- Parameters of each model level, and associated equations.
- Parameters and equations for MOSFET diode and MOSFET capacitor models.

In addition, Synopsys has introduced LEVELs that are compatible with models developed by UC Berkeley, The University of Florida, Rensselaer Polytechnic Institute, and other institutions, developers, and foundries.

Conventions

The following typographical conventions are used in Synopsys HSPICE documentation.

| Convention | Description |
|---------------|--|
| Courier | Indicates command syntax. |
| <i>Italic</i> | Indicates a user-defined value, such as <i>object_name</i> . |
| Bold | Indicates user input—text you type verbatim—in syntax and examples. For a graphical user interface, Bold indicates a GUI element. |
| [] | Denotes optional parameters, such as: <code>write_file [-f filename]</code> |
| () | When shown, the parentheses () are part of the syntax. For example: <code>+ LISTFREQ=(1k 100k 10meg)</code> |
| ... | Indicates that parameters can be repeated as many times as necessary: <code>pin1 pin2 ... pinN</code> |

| Convention | Description |
|-------------|--|
| | Indicates a choice among alternatives, such as low medium high |
| + | Indicates a continuation of a command line. |
| / | Indicates levels of directory structure. |
| Edit > Copy | Indicates a path to a menu command, such as opening the Edit menu and choosing Copy. |
| Control-c | Indicates a keyboard combination, such as holding down the Control key and pressing c. |

Customer Support

Customer support is available through SolvNet online customer support and through contacting the Synopsys Technical Support Center.

Accessing SolvNet

SolvNet includes an electronic knowledge base of technical articles and answers to frequently asked questions about Synopsys tools. SolvNet also gives you access to a wide range of Synopsys online services, which include downloading software, viewing Documentation on the Web, and entering a call to the Support Center.

To access SolvNet:

1. Go to the SolvNet Web page at <https://solvnet.synopsys.com>.
2. If prompted, enter your user name and password. (If you do not have a Synopsys user name and password, follow the instructions to register with SolvNet.)

If you need help using SolvNet, click Help on the SolvNet menu bar.

Contacting the Synopsys Technical Support Center

If you have problems, questions, or suggestions, you can contact the Synopsys Technical Support Center in the following ways:

- Go to the Synopsys [Global Support](#) site on synopsys.com. There you can find e-mail addresses and telephone numbers for Synopsys support centers throughout the world.
- Go to either the Synopsys SolvNet site or the Synopsys Global Support site and [open a case online](#) (Synopsys user name and password required).

Customer Support

Overview of MOSFET Models

Provides an overview of MOSFET model types and general information on using and selecting MOSFET models.

The following topics are discussed in these sections:

- [MOSFET Model Usage](#)
- [HSPICE and MOSFET Libraries](#)
- [MOSFET Device Definition](#)
- [HSPICE Automatic Model Selector](#)
- [General MOSFET Model Statement](#)
- [MOSFET Capacitors](#)
- [MOSFET Diodes](#)
- [MOSFET Control Options](#)
- [MOSFET Output Templates](#)
- [Safe Operating Area Voltage Warning](#)
- [Model Pre-Processing and Parameter Flattening](#)
- [Use of Example Syntax](#)

MOSFET Model Usage

A circuit netlist describes the basic functionality of an electronic circuit that you are designing. In HSPICE format, a netlist consists of a series of elements that define the individual components of the overall circuit. You can use your

Chapter 1: Overview of MOSFET Models

HSPICE and MOSFET Libraries

HSPICE-format netlist to help you verify, analyze, and debug your circuit design, before you turn that design into actual electronic circuitry.

Synopsys provides a series of standard models. Each model is like a template that defines various versions of each supported element type used in an HSPICE-format netlist. Individual elements in your netlist can refer to these standard models for their basic definitions. When you use these models, you can quickly and efficiently create a netlist and simulate your circuit design.

Referring to standard models this way reduces the amount of time required to:

- Create the netlist
- Simulate and debug your circuit design
- Turn your circuit design into actual circuit hardware.

Within your netlist, each element that refers to a model is known as an *instance* of that model. When your netlist refers to predefined device models, you reduce both the time required to create and simulate a netlist, and the risk of errors, compared to fully defining each element within your netlist.

One type of model that you can use as a template to define an element in your netlist is a Metal Oxide Semiconductor Field Effect Transistor (MOSFET) device. This manual describes the MOSFET models supplied for use with HSPICE.

A MOSFET device is defined by the MOSFET model and element parameters, and two submodels selected by the CAPOP and ACM model parameters.

- The CAPOP model parameter specifies the model for the MOSFET gate capacitances.
- The Area Calculation Method (ACM) parameter selects the type of diode model to use for the MOSFET bulk diodes.

Parameters in each submodel define the characteristics of the gate capacitances and bulk diodes.

MOSFET models are either p-channel or n-channel models; they are classified according to level, such as LEVEL 1 or LEVEL 50.

HSPICE and MOSFET Libraries

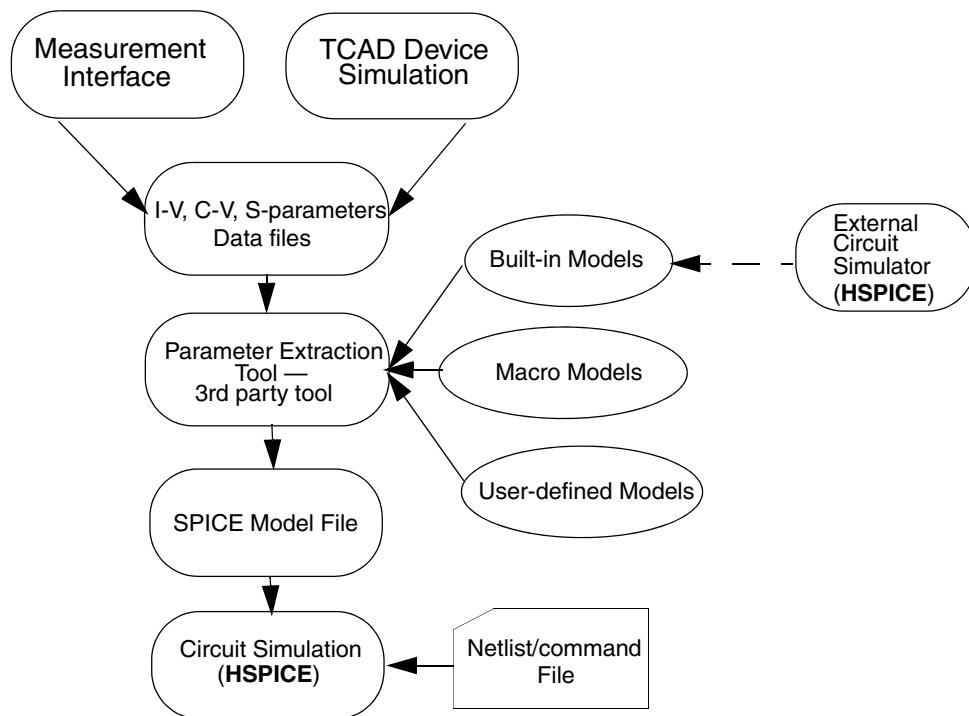
The following figure illustrates the generic flow of creating a MOSFET library-based circuit simulation. The `.LIB` call statement is used to call portions or all of a model file from a model library (see [.LIB](#) in the *HSPICE Reference*

Manual: Command and Control Options and [Invoking MOSFET Library Files](#):
below.

Support for Parameter Extraction:

The accuracy and a support for industry standard models makes HSPICE a strong option as an external circuit simulator in a parameter extraction flow. HSPICE built-in models are viable alternatives for any parameter extraction tool, such as the Agilent Technologies Integrated Circuits Characterization and Analysis Program (IC-CAP).

Note: Run HSPICE in client-server mode for best performance in a parameter extraction flow (See [Using HSPICE in Client-Server Mode](#)).



MOSFET Device Definition

To define a MOSFET device in your netlist, use both an element statement and a .MODEL statement.

Chapter 1: Overview of MOSFET Models

MOSFET Device Definition

The element statement defines the connectivity of the transistor and references the .MODEL statement. The .MODEL statement specifies either an n- or p-channel device, the level of the model, and several user-selectable model parameters.

The following example specifies a PMOS MOSFET. PCH is the model reference name. The transistor is modeled using the [LEVEL 13: BSIM Model](#). Select the parameters from the MOSFET model parameter lists in this chapter.

```
M3 3 2 1 0 PCH <parameters>
.MODEL PCH PMOS LEVEL=13 <parameters>
```

Invoking MOSFET Library Files:

You can use the .LIB command to create and read from libraries of commonly used commands, device models, subcircuit analyses, and statements.

Use the following syntax for library calls:

```
.LIB '<filepath> filename' entryname
```

Use the following syntax to define library files:

```
.LIB entryname1
. $ ANY VALID SET OF HSPICE STATEMENTS
.ENDL entryname1
.LIB entryname2
.
. $ ANY VALID SET OF HSPICE STATEMENTS
.ENDL entryname2
.LIB entryname3
.
. $ ANY VALID ET OF HSPICE STATEMENTS
.ENDL entryname3
```

To build libraries (library file definition), use the .LIB statement in a library file. For each macro in a library, use a library definition statement (.LIB entryname) and an .ENDL statement. The .LIB statement begins the library macro and the .ENDL statement ends the library macro. The text after a library file entry name must consist of HSPICE statements. Library calls can call other libraries (nested library calls) if they are different files. You can nest library calls to any depth. Use nesting with the .ALTER statement to create a sequence of model runs. Each run can consist of similar components by using different model parameters without duplicating the entire input file.

The simulator uses the .LIB statement and the .INCLUDE statement to access the models and skew parameters. The library contains parameters that modify .MODEL statements.

This section covers the following topics:

- [Reliability Analysis for HSPICE MOSFET Devices](#)
- [HSPICE Custom Common Model Interface \(CMI\)](#)
- [TSMC Model Interface \(TMI\)](#)

Reliability Analysis for HSPICE MOSFET Devices

As CMOS technology scales down, reliability requirements become more challenging and important in maintaining the long-term reliability of these devices. Two of the most critical reliability issues, the hot carrier injection (HCI) and the negative bias temperature instability (NBTI) effects have been demonstrated to change the characteristics of the MOS devices.

The HSPICE reliability analysis feature allows circuit designers to be able to predict the reliability of their designs such that there are enough margins for their circuits to function correctly over the entire lifetime.

Refer to [MOSFET Model Reliability Analysis \(MOSRA\)](#) in the *HSPICE User Guide: Simulation and Analysis* for more information. In addition, a unified custom reliability modeling MOSRA API is available with an application note. Consult your Synopsys support team for full information.

HSPICE Custom Common Model Interface (CMI)

HSPICE can use a dynamically-linked shared library to integrate models with the Custom CMI with use of the `cmiflag` global option to load the dynamically linked Custom CMI library. Consult your HSPICE technical support team for access to the HSPICE CMI application note and source code.

TSMC Model Interface (TMI)

You can invoke the TMI flow using proprietary TSMC model files and compiled libraries. Jointly developed by Synopsys and TSMC the TMI technology and API is a compact model with additional instance parameters and equations for an advanced modeling approach to support TSMC's extension of the standard BSIM4 model. Modeling API code is written in C and available in a compiled format for HSPICE and HSIM to link to during the simulation. TMI-required settings to invoke the flow and the location of a `.so` file are set by TSMC. The API also performs automatic platform selection on the `.so` file. Both HSPICE and HSIM provide the tool binaries and support the same `.so` file.

Use the existing HSPICE and HSIM commands to run the simulation. For more information, see the *HSPICE Reference Manual: Commands and Control Options* for [.OPTION TMIFLAG](#) and [.OPTION TMIPATH](#).

HSPICE Automatic Model Selector

For libraries with multiple models of a specific element, you can use a built-in model selector in HSPICE to automatically find the proper model for each transistor size.

The automatic model selector uses the following criteria:

$$LMIN + XLREF \leq L < LMAX + XLREF$$

$$WMIN + XWREF \leq W < WMAX + XWREF$$

If you do not specify `XLREF`, the simulation sets it to `XL`. If you do not specify `XWREF`, the simulation sets it to `XW`.

The model selector syntax is based on a common model root name, with a unique extension for each model.

The following is an example of HSPICE syntax for MOSFET models:

```
M1 drain gate source bulk NJ W=2u L=1u
  .MODEL NJ4 NJF WMIN=1.5u WMAX=3u LMIN=.8u LMAX=2u
  .MODEL NJ5 NJF WMIN=1.5u WMAX=3u LMIN=2u LMAX=6u
```

[Figure 1](#) illustrates the MOSFET model selection method.

This example illustrates several `pch.x` models, with varying drawn channel lengths and widths, in the model library. The model root name is “`pch`”, and the extensions are 1, 2, ..., 6. The `NJ4` instance of the `NJ` Element ($W=2\mu$, $L=1\mu$) requires a model for which $1.5\mu \leq \text{channel width} \leq 3\mu$, and $0.8\mu \leq \text{channel length} \leq 2\mu$.

The automatic model selector chooses the `pch.4` model because that model satisfies these requirements. Similarly, the `NJ5` transistor requires a model with $1.5\mu \leq \text{channel width} \leq 3\mu$, and $2\mu \leq \text{channel length} \leq 6\mu$. The `pch.5` model satisfies these requirements. If a device size is out of range for all models, the automatic model selector issues an error message.

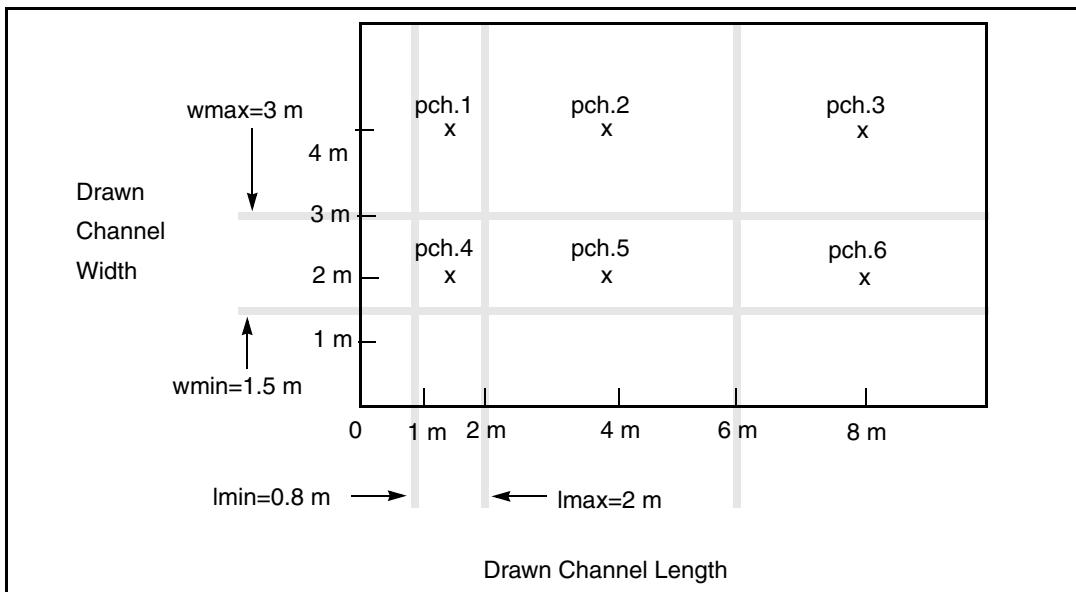


Figure 1 Automatic Model Selector Method

If the automatic model selector cannot find a model within a subcircuit, the automatic model selector searches the top level. If the automatic model selector fails to find a model, simulation terminates.

The following combination of conditions causes the automatic model selector to fail and terminates the simulation:

- The element statement uses a model name that contains a period (.).
- The model library was not designed for use with the automatic model selector.
- The simulation input includes either a multi-sweep specification or a .TEMP temperature analysis statement.

The following example illustrates how a period in a model name can cause problems in automatic model selection.

Example 1:

```
M1 d g s b N.CHN W=10u L=5u          * Element statement
.MODEL N.CHN LMN=1u LMAX=4u WMIN=2u WMAX=100u
* .MODEL statement
```

Chapter 1: Overview of MOSFET Models

General MOSFET Model Statement

Example 2:

```
.TEMP 25
.M1 d g s b N.CHN W=10u L=5u           * Element statement
.MODEL N.CHN LMIN=1u LMAX=4u WMIN=2u WMAX=100u
* .MODEL statement
```

Because Example 1 does not specify multi-sweep or temperature analysis, simulation does not invoke the model selector feature, so simulation uses the N.CHN model with no problems.

In Example 2, however, the .TEMP statement invokes the model selector feature. The model selector tries to find a model named “N.nnn” that fits within the length and width ranges specified in the element statement.

Because the length in the element statement (5 μm) is not within the 1 to 4 μm range specified in the .MODEL statement, the model selector cannot find a model that matches the element statement, and simulation issues a “device ‘N’ not found” error message.

General MOSFET Model Statement

You can use the .MODEL statement to include a MOSFET model in your HSPICE netlist. For more information, see [.MODEL](#) in the *HSPICE Reference Manual: Commands and Control Options*.

The following syntax applies to all MOSFET model specifications. All related parameter levels are described in their respective sections.

Note: The ENCMODE parameter can only be set in [LEVEL 54: BSIM4 MOSFET Model](#) to suppress warning messages. The TMI MODEL and CMI MODEL parameters avoid potential conflicts when the TMI or custom CMI model and other standard models are used together in a shared object file.

Syntax:

```
.MODEL mname [PMOS | NMOS] [ENCMODE=0 | 1]
+ ([LEVEL=val keyname1=val1 keyname2=val2...])
+ [VERSION=version_number]
+ [TMIMODEL=0 | 1] [CMIMODEL=0 | 1]
```

| Parameter | Description |
|-----------|--|
| mname | Model name. Elements refer to the model by this name. See Model Name Identification Rule below. |
| PMOS | Identifies a p-channel MOSFET model. |
| NMOS | Identifies an n-channel MOSFET model. |
| ENCMODE | Applicable to BSIM4 (level 54 only); use to suppress warning messages originating in CMI code while inside encrypted code. Default is 0 (off). Set to off if this parameter is not present. This parameter cannot be overwritten through the instance line. |
| LEVEL | Use the LEVEL parameter to select from several MOSFET model types. Default=1.0. |
| VERSION | Specifies the version number of the model for LEVEL=13 BSIM and LEVEL=39 BSIM2 models only. See the .MODEL statement description for information about the effects of this parameter. |
| TMIMODEL | This parameter takes effect when .option tmiflag is on. If you set it to 1, the simulator seeks models from a shared object file to avoid potential conflicts. TMIMODEL default (1) with TMI model cards. Set it to 'zero' in non-TMI models when both TMI and non-TMI models are used in a design. When 0, the flag directs the simulator to ignore models in compiled TMI libraries. |
| CMIMODEL | This parameter takes effect when .option cmiflag is on. If you set it to 1, the simulator seeks models from a shared object file to avoid potential conflicts. |

Example:

```
.MODEL MODP PMOS LEVEL=7 VTO=-3.25 GAMMA=1.0)
.MODEL MODN NMOS LEVEL=2 VTO=1.85 TOX=735e-10)
.MODEL MODN NMOS LEVEL=39 TOX=2.0e-02 TEMP=2.5e+01
+ VERSION=95.1
```

This section covers the following topics:

- [Model Name Identification Rule](#)
- [Measuring the Value of MOSFET Model Card Parameters](#)
- [Using a Model Card Defined with a Subckt Wrapper](#)

Model Name Identification Rule

MOSFETs can support up to 7 nodes. HSPICE model name identification uses the following rule:

If the model names 'nch' and 'pch' appear at the same time, then 'nch' is regarded as a node name and 'pch' is considered the model. However, after the 4th node, HSPICE regards 'nch' as the model name instead of 'pch'.

For example:

```
m1 n1 n2 n3 n4 nch pch p1 p2 p3
```

Measuring the Value of MOSFET Model Card Parameters

The keywords `val()` and `valm()` are supported by `.MEAS/.PRINT/.PROBE` commands (only).

The syntax for instance parameters is: `val(element.parameter)`

The syntax for model parameters is: `valm(elem_name.model_param)`

The parameters currently supported for `valm()` include: vth0, lmin, lmax, wmin, wmax, lref, wref, xl, dl, dell, xw, dw, delw, scalm, lmlt, wmlt, and levels 54, 57, and 70. If the modelcard in `valm()` is not a valid model parameter for the level, an error is reported.

For example:

```
.meas delvto1 param='val(m1.l)'  
.meas tran m_vth0 param='valm(m1.vth0)'
```

For cmi models, `valm()` only supports levels 54, 57, and 70 and model card parameters: vth0, lmin, lmax, wmin, wmax, lref, wref, xl, dl, dll, xw, dw, delw, scalm, lmlt, wmlt.

Using a Model Card Defined with a Subckt Wrapper

The increased complexity of MOSFET models sometimes renders the `.MODEL` construct inefficient to implement statistical, DFM, WPE modeling, etc. As a countermeasure, foundries have used a macro model process in which they wrap `.MODEL` statements under a `.SUBCKT` structure to accommodate additional equations and parameter definitions. The arguments for MOSFET

output templates when used with a macro model card differ slightly from a standard model card.

For example:

```
xm1 1 2 3 4 nmos_mac
.subckt nmos_mac 1 2 3 4
mn1 d g s b nmos ....
.model nmos nmos ...
.ends
```

In this case the format would be:

template_name(circuit_element_name.subckt_element_name)

For example: LV9 (xm1.mn1)

In some cases, however, even though the model card is subcircuit-based, the netlist could still contain an M-element statement. Traditionally, HSPICE requires the .SUBCKT statement to be called by an X-element statement. But if you use .OPTION MACMOD=3, this requirement can be bypassed and the M-element statement can be directly mapped to a .SUBCKT statement in the absence of a .MODEL statement. For example, you can modify the example above as follows:

```
.option macmod=3
m1 1 2 3 4 nmos_mac
```

In this case, the threshold voltage monitoring command would be:

lv9 (m1.mn1)

For more information, see [.SUBCKT](#) and [.OPTION MACMOD](#) in the *HSPICE Reference Manual: Commands and Control Options*.

MOSFET Capacitors

CAPOP is the MOSFET capacitance model parameter. This parameter determines which capacitor models to use when modeling the MOS gate capacitance; that is, the gate-to-drain capacitance, the gate-to-source capacitance, and the gate-to-bulk capacitance. Using the CAPOP parameter, you can select a specific version of the Meyer and charge conservation model.

Chapter 1: Overview of MOSFET Models

MOSFET Capacitors

Some capacitor models are tied to specific DC models; they are stated as such. Others are for general use by any DC model.

| Parameter | Description |
|-----------|---|
| CAPOP=0 | SPICE original Meyer gate-capacitance model (general) |
| CAPOP=1 | Modified Meyer gate-capacitance model (general) |
| CAPOP=2 | Modified Meyer gate-capacitance model with parameters (general default) |
| CAPOP=3 | Modified Meyer gate-capacitance model with parameters and Simpson integration (general) |
| CAPOP=4 | Charge conservation capacitance model (analytic), LEVELs 2, 3, 6, 7, 13, 28, and 39 only |
| CAPOP=5 | No capacitor model |
| CAPOP=6 | AMI capacitor model (LEVEL 5) |
| CAPOP=9 | Charge conservation model (LEVEL 3) |
| CAPOP=11 | Ward-Dutton model specialized (LEVEL 2) |
| CAPOP=12 | Ward-Dutton model specialized (LEVEL 3) |
| CAPOP=13 | Generic BSIM Charge-Conserving Gate Capacitance model (Default for Levels 13, 28, and 39) |
| CAPOP=39 | BSIM2 Charge-Conserving Gate Capacitance Model (LEVEL 39) |

CAPOP=4 selects the recommended charge-conserving model (from among CAPOP=11, 12, or 13) for the specified DC model.

| MOS Level | Default CAPOP | CAPOP=4 selects: |
|------------|---------------|------------------|
| 2 | 2 | 11 |
| 3 | 2 | 12 |
| 13, 28, 39 | 13 | 13 |
| others | 2 | 11 |

LEVELs 49 and 53 use the Berkeley CAPMOD capacitance-model parameter. Proprietary models, and LEVELs 5, 17, 21, 22, 25, 27, 31, 33, 49, 53, 55, and 58, use built-in capacitance routines.

MOSFET Diodes

The Area Calculation Method (ACM) model parameter controls the geometry of the source and drain diffusions, and selects the modeling of the bulk-to-source and bulk-to-drain diodes of the MOSFET model. The diode model includes the diffusion resistance, capacitance, and DC currents to the substrate.

For more information on ACM, see [MOSFET Diode Model Parameters](#).

MOSFET Control Options

Specific control options (set in the .OPTION statement) used for MOSFET models include the following. For flag options, 0 is unset (off) and 1 is set (on).

| Option | Description |
|---------|---|
| ASPEC | This option uses ASPEC MOSFET model defaults and set units. Default=0. |
| BYPASS | This option avoids recomputing nonlinear functions that do not change with iterations. Default=1. |
| MBYPASS | BYPASS tolerance multiplier (BYTOL = MBYPASSxVNTOL). Default=1 if DVDT=0, 1, 2, or as 3. Default=2 if DVDT=4. |
| DEFAD | Default drain diode area. Default=0. |
| DEFAS | Default source diode area. Default=0. |
| DEFL | Default channel length. Default=1e-4m. |
| DEFNRD | Default number of squares for drain resistor. Default=0. |
| DEFNRS | Default number of squares for source resistor. Default=0. |
| DEFPD | Default drain diode perimeter. Default=0. |
| DEFPS | Default source diode perimeter. Default=0. |

Chapter 1: Overview of MOSFET Models

MOSFET Control Options

| Option | Description |
|--------|---|
| DEFW | Default channel width. Default=1e-4m. |
| GMIN | Pn junction parallel transient conductance. Default=1e-12mho. |
| GMINDC | Pn junction parallel DC conductance. Default=1e-12mho. |
| SCALE | Element scaling factor. Default=1. |
| SCALM | Model scaling factor. Default=1. Note: the SCALM parameter is only available in some models below Level 49. At Level 49 and higher, it is ignored. |
| WL | Reverses order in VSIZE MOS element from the default order (length-width) to width-length. Default=0. |

- The AD element statement overrides the DEFAD default.
- The AS element statement overrides the DEFAS default.
- The L element statement overrides the DEFL default.
- The NRD element statement overrides the DEFNRD default.
- The NRS element statement overrides the DEFNRS default.
- The PD element statement overrides the DEFPD default.
- The PS element statement overrides the DEFPS default.
- The W element statement overrides the DEFW default.

The following sections discuss additional options:

- [Scale Units](#)
- [Bypass Option for Latent Devices](#)
- [Searching Models as Function of W, L](#)
- [Number of Fingers, WNFLAG Option](#)

Scale Units

The SCALE and SCALM options control the units.

- `SCALE` scales element statement parameters.
- `SCALM` scales model statement parameters. It also affects the MOSFET gate capacitance and diode model parameters.

Note: `SCALM` is ignored in Level 49 and higher.

In this chapter, scaling applies only to parameters that you specify as scaled. If you specify `SCALM` as a parameter in a `.MODEL` statement, it overrides the `SCALM` option. In this way, you can use models with different `SCALM` values in the same simulation. MOSFET parameter scaling follows the same rules as for other model parameters, for example:

| Parameter Units | Parameter Value |
|---------------------------------|--|
| <code>meter</code> | multiplied by <code>SCALM</code> |
| <code>meter²</code> | multiplied by <code>SCALM²</code> |
| <code>meter⁻¹</code> | divided by <code>SCALM</code> |
| <code>meter⁻²</code> | divided by <code>SCALM²</code> |

To override global model size scaling for individual MOSFET, diode, and BJT models that use the `.OPTION SCALM=<val>` statement, include `SCALM=<val>` in the `.MODEL` statement. `.OPTION SCALM=<val>` applies globally for JFETs, resistors, transmission lines, and all models other than MOSFET, diode, and BJT models. You cannot override `SCALM` in the model.

Scaling for LEVEL 25 and 33

When using the proprietary LEVEL 25 (Rutherford CASMOS) or LEVEL 33 (National) models, the `SCALE` and `SCALM` options are automatically set to `1e-6`. However, if you use these models with other scalable models, you must explicitly set the `SCALE=1e-6` and `SCALM=1e-6` options.

Bypass Option for Latent Devices

Use the `BYPASS` (latency) option to decrease simulation time in large designs. To speed simulation time, this option does not recalculate currents, capacitances, and conductances, if the voltages at the terminal device nodes have not changed. The `BYPASS` option applies to MOSFETs, MESFETs, JFETs, BJTs, and diodes. Use `.OPTION BYPASS` to set `BYPASS`.

BYPASS might reduce simulation accuracy for tightly-coupled circuits such as op-amps, high gain ring oscillators, and others. Use .OPTION MBYPASS to set MBYPASS to a smaller value for more accurate results.

Searching Models as Function of W, L

Model parameters are often the same for MOSFETs that have width and length dimensions within specific ranges. To take advantage of this, create a MOSFET model for a specific range of width and length. These model parameters help the simulator to select the appropriate model for the specified width and length.

The automatic model selection program searches a data file for a MOSFET model where the width and length are within the range specified in the MOSFET element statement. Simulation then uses this model statement.

To search a data file for MOSFET models within a specified range of width and length:

- Provide a root extension for the model reference name (in the .MODEL statement).
- Use the model geometric range parameters (LMIN, LMAX, WMIN, and WMAX). These model parameters define the range of physical length and width dimensions to which the MOSFET model applies.

Example 1:

If the model reference name in the element statement is NCH, the model selection program examines the models with the same root model reference name (NCH), such as NCH.1, NCH.2 or NCH.A.

The model selection program selects the first MOSFET model statement whose geometric range parameters include the width and length specified in the associated MOSFET element statement.

Example 2:

The following example shows how to call the MOSFET model selection program from a data file. The model selector program examines the .MODEL statements where the model reference names have the root extensions NCHAN.2, NCHAN.3, NCHY.20, and NCHY.50.

Note: The scalm parameter is ignored in Level 49 and higher.

The following example is based on demonstration netlist selector.sp, which is available in directory \$installdir/demo/hspice/mos:

```

file: selector.sp test of mos model selector
.option post list wl scale=1u scalm=1u nomod
.op
.probe i(m1)
v1 1 0 5
v2 2 0 4
v3 3 0 1
v4 4 0 -1
m1 1 2 3 4 nchan 10 2
m2 1 2 3 4 nchan 10 3
m3 1 2 3 4 nch 10 4
m4 1 2 3 4 nchx 10 5
m5 1 2 3 4 nchy 20 5
m6 1 2 3 4 nchy 50 5
$$$$$$ for channel length selection
.model nchan.2 nmos level=2 vto=2.0 uo=800 tox=500 nsub=1e15
+ rd=10 rs=10 capop=5
+ lmin=1 lmax=2.5 wmin=2 wmax=15
.model nchan.3 nmos level=2 vto=2.2 uo=800 tox=500 nsub=1e15
+ rd=10 rs=10 capop=5
+ lmin=2.5 lmax=3.5 wmin=2 wmax=15
$$$$$$ no selection for channel length and width
.model nch nmos level=2 vto=2.3 uo=800 tox=500 nsub=1e15
+ rd=10 rs=10 capop=5
+$ lmin=3.5 lmax=4.5 wmin=2 wmax=15
.model nchx nmos level=2 vto=2.4 uo=800 tox=500 nsub=1e15
+ rd=10 rs=10 capop=5
+$ lmin=4.5 lmax=100 wmin=2 wmax=15
$$$$$$ for channel width selection
.model nchy.20 nmos level=2 vto=2.5 uo=800 tox=500 nsub=1e15
+ rd=10 rs=10 capop=5
+ lmin=4.5 lmax=100 wmin=15 wmax=30
.model nchy.50 nmos level=2 vto=2.5 uo=800 tox=500 nsub=1e15
+ rd=10 rs=10 capop=5
+ lmin=4.5 lmax=100 wmin=30 wmax=500
.end

```

Number of Fingers, WNFLAG Option

This section discusses number of fingers, categorization bin, channel currents and NF vs. M parameter.

This section covers the following topics:

- [Number and Width of Fingers](#)
- [Categorizing Bins in Model File for MOSFETs](#)

Chapter 1: Overview of MOSFET Models

MOSFET Control Options

- [Values for IDs with Different Values of NF](#)
- [How NF Differs from Multiplication Parameter M](#)

Number and Width of Fingers

Specify the number of fingers for fingered MOSFETs in HSPICE by using the instance parameter **NF**. The resultant width is explained below.

Example:

```
M1 out in vdd vdd pmos w=10u l=1u nf=5
```

M1 has a total drawn width of 10um with 5 fingers, each having a finger gate width of 2um. Both HSPICE and UCB BSIM4 models employ the same, consistent definition.

Categorizing Bins in Model File for MOSFETs

By default, HSPICE uses **w/nf** for model selection of the MOSFET. This is the default behavior because the parameter **wnflag** has been set to 1. If **wnflag = 1**, then HSPICE uses the ratio **w/nf** for model selection. If **wnflag = 0**, then HSPICE uses **w** for model selection. If you want to use the total width for binning model selection, you need to explicitly set **wnflag** to 0.

Only BSIM4-based models can have **wnflag** as an instance parameter. But the netlist option, **.option wnflag**, is not strictly for BSIM4 model usage, it is for all levels of MOSFETs. For example,

For BSIM4 models only:

```
M1 out in vdd vdd pmos w=10u l=1u nf=5 wnflag=1
```

For all other levels:

```
.option wnflag  
M1 out in vdd vdd pmos w=10u l=1u nf=5
```

Values for IDs with Different Values of NF

While one might expect the MOSFET to have the same value of channel current even if you layout a device with a different number of fingers, you get different values of channel current (IDs).

Example:

```
M1 out in vdd vdd pmos w=10u l=1u nf=1  
M2 out in vdd vdd pmos w=10u l=1u nf=5
```

Ideally, M1 (one finger) and M2 (five fingers) should have same values of channel current since their W and L values are same, but these values are different because for the fingered MOSFETs, the channel current, effective

width, and effective resistance of source and drain are functions of `nf`. Hence, the channel current value also differs slightly.

How NF Differs from Multiplication Parameter M

'M' stands for multiplicity factor. It means that 'M' identical transistors are in parallel. For example,

```
M1 out in vdd vdd pmos w=10u l=1u m=5
```

indicates that 5 identical transistors are connected in parallel with a total width of 50 um.

MOSFET Output Templates

Many MOSFET models produce an output template, consisting of a set of parameters that specify the output of state variables, stored charges, capacitances, parasitic diode current, and capacitor currents. Different MOSFET model levels support different subsets of these output parameters.

For example, if your netlist contains four transistors `m0`, `m1`, `m2`, and `m3`, you can print the parameter values during the transient analysis using the following `.print` statement:

```
.print tran LX3(m1) LX4(m1) LX7(m1) LX8(m1)
```

This command prints the values of `Vds`, `Ids`, `Gm` and `Gds` to the `*.lis` file. For more information on MOSFET information, use the [.OPTION LIST](#) command as described in the *HSPICE User Guide: Basic Simulation and Analysis*.

To enable HSPICE to print PMOS template output voltage polarity as real bias, use the [.OPTION TMPLT_POL](#) as described in the *HSPICE Reference Manual: Commands and Control Options*.

Wildcards are also supported, so you can also use the following, which prints the `Vds` of all transistors:

```
.print tran LX3(*)
```

Chapter 1: Overview of MOSFET Models

MOSFET Output Templates

The following table lists parameters in the MOSFET output templates, and indicates which model levels support each parameter.

| Name | Alias | Description | MOSFET Level |
|-------|-------|--|--|
| L | LV1 | Channel length (L) (also the effective channel length for all MOSFET models except Levels 54, 57, 69 and 70) | All |
| W | LV2 | Channel width (W) (also the effective channel width for all MOSFET models except Levels 54, 57, 69 and 70) | All |
| AD | LV3 | Area of the drain diode (AD) | All |
| AS | LV4 | Area of the source diode (AS) | All |
| ICVDS | LV5 | Initial condition for the drain-source voltage (VDS) | All |
| ICVGS | LV6 | Initial condition for the gate-source voltage (VGS) | All |
| ICVBS | LV7 | Initial condition for the bulk-source voltage (VBS) | All except 57, 58, 59, 70, 71 |
| ICVES | LV7 | Initial condition for the substrate-source voltage (VES) | 57, 58, 59, 70, 71 |
| – | LV8 | Device polarity: ■ 1 = forward ■ -1 = reverse (not used after HSPICE release 95.3). | All |
| VTH | LV9 | Threshold voltage (bias dependent) | All, including 54 (BSIM4) and 72 (CMG) |
| VDSAT | LV10 | Saturation voltage (VDSAT) | All |
| PD | LV11 | Drain diode periphery (PD) | All |
| PS | LV12 | Source diode periphery (PS) | All |
| RDS | LV13 | Drain resistance (squares) (RDS) (equals the value of instance parameter nrd/nrs) | All |
| RSS | LV14 | Source resistance (squares) (RSS) (equals the value of instance parameter nrd/nrs) | All |
| XQC | LV15 | Charge-sharing coefficient (XQC). | All |
| GDEFF | LV16 | Effective drain conductance (1/RDeff), rgeoMod is not 0 | All |
| GSEFF | LV17 | Effective source conductance (1/RSeff), rgeoMod is not 0 | All |

Chapter 1: Overview of MOSFET Models
MOSFET Output Templates

| Name | Alias | Description | MOSFET Level |
|----------|-------|--|---|
| CDSAT | LV18 | Drain-bulk saturation current, at -1 V bias. | All |
| CSSAT | LV19 | Source-bulk saturation current, at -1 V bias. | All |
| VDBEFF | LV20 | Effective drain bulk voltage. | All |
| BETAEFF | LV21 | BETA effective | All |
| GAMMAEFF | LV22 | GAMMA effective | All |
| DELTAL | LV23 | ΔL (MOS6 amount of channel length modulation) | 1, 2, 3, 6 |
| UBEFF | LV24 | UB effective | 1, 2, 3, 6 |
| VG | LV25 | VG drive | 1, 2, 3, 6 |
| VFBEFF | LV26 | VFB effective. | All |
| – | LV31 | Drain current tolerance (not used in HSPICE releases after 95.3) | All |
| IDSTOL | LV32 | Source-diode current tolerance | All |
| IDDTOL | LV33 | Drain-diode current tolerance | All |
| COVLGS | LV36 | Gate-source overlap and fringing capacitances | All |
| COVLGD | LV37 | Gate-drain overlap and fringing capacitances | All |
| COVLGB | LV38 | Gate-bulk overlap capacitances | All except 57, 59, 70, 71 |
| COVLGE | LV38 | Gate-substrate overlap capacitances | 57, 59, 70, 71 |
| VBD | LX0 | Bulk-drain voltage | All, including 54 (BSIM4) and 72 (CMG) |
| VBS | LX1 | Bulk-source voltage (VBS) | All except 57, 59, 70, 71 and including 54 (BSIM4) and 72 (CMG) |
| VES | LX1 | Substrate-source voltage (VES) | 57, 59, 70, 71 |

Chapter 1: Overview of MOSFET Models

MOSFET Output Templates

| Name | Alias | Description | MOSFET Level |
|-------|-------|---|--|
| VGS | LX2 | Gate-source voltage (VGS) | All, including 54 (BSIM4) and 72 (CMG) |
| VDS | LX3 | Drain-source voltage (VDS) | All, including 54 (BSIM4) and 72 (CMG) |
| CDO | LX4 | Channel current (IDS) | All |
| CBSO | LX5 | DC source-bulk diode current (CBSO) | All |
| CBDO | LX6 | DC drain-bulk diode current (CBDO) | All |
| GMO | LX7 | DC MOSFET gate transconductance (GMO) ■ Current is I_{ds} , from drain-to-source, ■ Voltage is v_{gs} | All |
| GDSO | LX8 | DC drain-source conductance (GDSO) | All |
| GMBSO | LX9 | DC substrate transconductance (GMBSO) | All except 57, 58, 59, 70, 71 |
| GMESO | LX9 | DC substrate transconductance (GMBSO/GMESO) | 57, 58, 59, 70, 71 |
| GBDO | LX10 | Conductance of the drain diode (GBDO) | All |
| GBSO | LX11 | Conductance of the source diode (GBSO) | All |
| QB | LX12 | Total bulk (body) charge (QB)—Meyer and Charge Conservation | All |
| CQB | LX13 | Bulk (body) charge current (CQB)—Meyer and Charge Conservation | All |
| QG | LX14 | Total Gate charge (QG)—Meyer and Charge Conservation | All |
| CQG | LX15 | Gate charge current (CQG)—Meyer and Charge Conservation | All |
| QD | LX16 | Total Drain charge (QD) | 49, 53 |
| QD | LX16 | Channel charge (QD)—Meyer and Charge Conservation | All except 49 and 53 |
| CQD | LX17 | Drain charge current (CQD) | 49, 53 |

Chapter 1: Overview of MOSFET Models
MOSFET Output Templates

| Name | Alias | Description | MOSFET Level |
|-------|-------|--|---------------------------------------|
| CQD | LX17 | Channel charge current (CQD)—Meyer and Charge Conservation | All except 49 and 53 |
| CGGBO | LX18 | $CGGBO = dQg/dVg = CGS + CGD + CGB$ - Meyer and Charge Conservation | All except 54, 57, 59, 60, 70, 71 |
| CGGBO | LX18 | Intrinsic gate capacitance | 54, 57, 59, 60, 66, 70, 71 |
| CGDBO | LX19 | $CGDBO = -dQg/dVd$ - Meyer and Charge Conservation; this cap is the total capacitance, including derivative of charge (dQg/dVd) and overlap capacitance. | All except 54, 57, 59, 60, 66, 70, 71 |
| CGDBO | LX19 | Intrinsic gate-to-drain capacitance | 54, 57, 59, 60, 66, 70, 71 |
| CGSBO | LX20 | $CGSBO = -dQg/dVd$ - Meyer and Charge Conservation | All except 54, 57, 59, 60, 66, 70, 71 |
| CGSBO | LX20 | Intrinsic gate-to-source capacitance | 54, 57, 59, 60, 66, 70, 71 |
| CBGBO | LX21 | $CBGBO = -dQb/dVg$ - Meyer and Charge Conservation | All except 54, 57, 59, 60, 66, 70, 71 |
| CBGBO | LX21 | Intrinsic bulk-to-gate capacitance | 54, 66 |
| CBGBO | LX21 | Intrinsic floating body-to-gate capacitance | 57, 59, 60, 70, 71 |
| CBDBO | LX22 | $CBDBO = -dQb/dVd$ - Meyer and Charge Conservation | All except 54, 57, 59, 60 |
| CBDBO | LX22 | Intrinsic bulk-to-drain capacitance | 54, 66 |
| CBDBO | LX22 | Intrinsic floating body-to-drain capacitance | 57, 59, 60, 70, 71 |
| CBSBO | LX23 | $CBSBO = -dQb/dVs$ - Meyer and Charge Conservation | All except 54, 57, 59, 60, 66, 70, 71 |
| CBSBO | LX23 | Intrinsic bulk-to-source capacitance | 54, 66 |
| CBSBO | LX23 | Intrinsic floating body-to-source capacitance | 57, 59, 60, 70, 71 |
| QBD | LX24 | Drain-bulk charge (QBD) | All |
| - | LX25 | Drain-bulk charge current (CQBD), (not used in HSPICE releases after 95.3). | All |
| QBS | LX26 | Source-bulk charge (QBS) | All |

Chapter 1: Overview of MOSFET Models

MOSFET Output Templates

| Name | Alias | Description | MOSFET Level |
|--------|-------|--|---------------------------------------|
| - | LX27 | Source-bulk charge current (CQBS), (not used after HSPICE release 95.3). | All |
| CAP_BS | LX28 | Extrinsic drain to substrate Capacitances—Meyer and Charge Conservation. CAP_BS=csbox+csesw <ul style="list-style-type: none">■ csbox is the substrate-to-source bottom capacitance■ csesw is the substrate-to-source sidewall capacitance | 57, 58, 70, 71 |
| CAP_BS | LX28 | Bias dependent bulk-source capacitance | All except 57, 58, 70, 71 |
| CAP_BD | LX29 | Extrinsic source to substrate Capacitances—Meyer and Charge Conservation. CAP_BD=cdbox+cdesw <ul style="list-style-type: none">■ cdbox is the substrate-to-drain bottom capacitance■ cdesw is the substrate-to-drain sidewall capacitance | 57, 58, 70, 71 |
| CAP_BD | LX29 | Bias dependent bulk-drain capacitance | All except 57, 58, 70, 71 |
| CQS | LX31 | Channel-charge current (CQS). | All |
| CDGBO | LX32 | CDGBO = -dQd/dVg - Meyer and Charge Conservation | All except 54, 57, 59, 60, 66, 70 |
| CDGBO | LX32 | Intrinsic drain-to-gate capacitance | 54, 57, 59, 60, 66, 70 |
| CDDBO | LX33 | CDDBO = dQd/dVd - Meyer and Charge Conservation | All except 54, 57, 59, 60, 66, 70, 71 |
| CDDBO | LX33 | Intrinsic drain capacitance | 54, 57, 59, 60, 66, 70, 71 |
| CDSBO | LX34 | CDSBO = -dQd/dVs Drain-to-source capacitance - Meyer and Charge Conservation | All |
| QE | LX35 | Substrate charge (QE)—Meyer and Charge Conservation | 57, 58, 59, 70, 71 |
| CQE | LX36 | Substrate charge current (CQE)—Meyer and Charge Conservation | 57, 58, 59, 70, 71 |
| CDEBO | LX37 | CDEBO = -dQd/dVe intrinsic drain-to-substrate capacitance | 57, 59, 70, 71 |
| CBEBO | LX38 | CBEBO = -dQb/dVe intrinsic floating body-to-substrate capacitance | 59, 70, 71 |

Chapter 1: Overview of MOSFET Models
MOSFET Output Templates

| Name | Alias | Description | MOSFET Level |
|---------|-------|--|--------------------|
| igso | LX38 | Gate-to-Source Current | 54, 69 |
| CEEBO | LX39 | CEEBO = dQe/dVe intrinsic substrate capacitance | 59, 70, 71 |
| igdo | LX39 | Gate-to-Drain Current | 54, 69 |
| CEGBO | LX40 | CEGBO = $-dQe/dVg$ intrinsic substrate-to-gate capacitance | 57, 59, 70, 71 |
| CEDBO | LX41 | CEDBO = $-dQe/dVd$ intrinsic substrate-to-drain capacitance | 57, 59, 70, 71 |
| CESBO | LX42 | CESBO = $-dQe/dVs$ intrinsic substrate-to-source capacitance | 57, 59, 70, 71 |
| VBSI | LX43 | Body-source voltage (VBS)—Meyer and Charge Conservation | 57, 58, 59, 70, 71 |
| ICH | LX44 | Channel current—Meyer and Charge Conservation | 57, 58, 59, 70, 71 |
| IBJT | LX45 | Parasitic BJT collector current—Meyer and Charge Conservation | 57, 58, 59, 70, 71 |
| III | LX46 | Impact ionization current—Meyer and Charge Conservation | 57, 58, 59, 70, 71 |
| IGIDL | LX47 | GIDL current—Meyer and Charge Conservation | 57, 58, 59, 70, 71 |
| ITUN | LX48 | Tunneling current—Meyer and Charge Conservation | 57, 58, 59, 70, 71 |
| Qbacko | LX49 | Back gate charge | 57, 59, 70, 71 |
| Ibp | LX50 | Body contact current | 57, 59, 70, 71 |
| Sft | LX51 | Value of the temperature node with shmod=1 | 57, 59, 70, 71 |
| VBFLOAT | LX52 | Internal body node voltage, if you do not specify the terminal | 57, 59, 70, 71 |
| Rbp | LX53 | Combination of rbody and rhalo | 57, 59, 70, 71 |
| IGB | LX54 | Gate tunneling current | 57, 59, 70, 71 |
| QSRCO | LX55 | Total Source charge (Charge Conservation: QS=- (QG+QD+QB)) | 49, 53 |
| QSRCO | LX55 | Total Source charge (Charge Conservation: QS=- (QG+QD+QB+QE)) | 57, 59, 70, 71 |
| CQs | LX56 | Source charge current | 57, 59, 70, 71 |
| CGEBO | LX57 | CGEBO = $-dQg/dVe$ intrinsic gate-to-substrate capacitance | 57, 59, 70, 71 |

Chapter 1: Overview of MOSFET Models

MOSFET Output Templates

| Name | Alias | Description | MOSFET Level |
|--------|-------|--|--------------------|
| CSSBO | LX58 | $\text{CSSBO} = \frac{dQ_s}{dV_s}$ intrinsic source capacitance | 57, 59, 70, 71 |
| CSGBO | LX59 | $\text{CSGBO} = -\frac{dQ_s}{dV_g}$ intrinsic source-to-gate capacitance | 57, 59, 70, 71 |
| CSDBO | LX60 | $\text{CSDBO} = -\frac{dQ_s}{dV_d}$ intrinsic source-to-drain capacitance | 57, 59, 70, 71 |
| CSEBO | LX61 | $\text{CSEBO} = -\frac{dQ_s}{dV_e}$ intrinsic source-to-substrate capacitance | 57, 59, 70, 71 |
| weff | LX62 | Effective channel width | 54, 57, 66, 69, 70 |
| leff | LX63 | Effective channel length | 54, 57, 66, 69, 70 |
| weffcv | LX64 | Effective channel width for CV | 54, 66, 69 |
| leffcv | LX65 | Effective channel length for CV | 54, 66, 69 |
| igbo | LX66 | Gate-to-Substrate Current ($I_{gb} = I_{gacc} + I_{gbinv}$) | 54, 69 |
| igcso | LX67 | Source Partition of Ig | 54, 69 |
| igcdo | LX68 | Drain Partition of Ig | 54, 69 |
| iimi | LX69 | Impact ionization current | 54, 69 |
| igidlo | LX70 | Gate-induced drain leakage current | 54, 69 |
| igdt | LX71 | Gate Dielectric Tunneling Current ($I_g = I_{gs} + I_{gd} + I_{gcs} + I_{gcd} + I_{gb}$) | 54, 69 |
| igc | LX72 | Gate-to-Channel Current at zero Vds | 54, 69 |
| igbacc | LX73 | Determined by ECB (Electron tunneling from the Conduction Band); significant in the accumulation | 54 |
| igbinv | LX74 | Determined by EVB (Electron tunneling from the Valence Band); significant in the inversion | 54 |
| vfbstd | LX75 | Flat-band Voltage between the Gate and S/D diffusions | 54, 66 |
| vgse | LX76 | Effective Gate-to-Source Voltage | 54, 66 |
| vox | LX77 | Voltage Across Oxide | 54, 66 |
| rdv | LX78 | Asymmetric and Bias-Dependent Source Resistance, (rdsMod = 1) | 54, 66 |
| rsv | LX79 | Asymmetric and Bias-Dependent Drain Resistance, (rdsMod = 1) | 54, 66 |

Chapter 1: Overview of MOSFET Models
MOSFET Output Templates

| Name | Alias | Description | MOSFET Level |
|---------|-------|--|--------------------------------|
| cap_bsz | LX80 | Zero voltage bias bulk-source capacitance | 54, 66 |
| cap_bdz | LX81 | Zero voltage bias bulk-drain capacitance | 54, 66 |
| CGGBM | LX82 | Total gate capacitance (including intrinsic), and all overlap and fringing components | 54, 57, 59, 60, 66, 70, 69, 71 |
| CGDBM | LX83 | Total gate-to-drain capacitance (including intrinsic), and overlap and fringing components | 54, 57, 59, 60, 66, 69, 70, 71 |
| CGSBM | LX84 | Total gate-to-source capacitance (including intrinsic), and overlap and fringing components | 54, 57, 59, 60, 66, 69, 70, 71 |
| CDDBM | LX85 | Total drain capacitance (including intrinsic), overlap and fringing components, and junction capacitance | 54, 57, 59, 60, 66, 69, 70, 71 |
| CDSBM | LX86 | Total drain-to-source capacitance | 54, 57, 60, 66, 69, 70, 71 |
| CDGBM | LX87 | Total drain-to-gate capacitance (including intrinsic), and overlap and fringing components | 54, 57, 59, 60, 66, 69, 70, 71 |
| CBGBM | LX88 | Total bulk-to-gate (floating body-to-gate) capacitance, including intrinsic and overlap components | 54, 57, 59, 60, 66, 70, 71 |
| CBDBM | LX89 | Total bulk-to-drain capacitance (including intrinsic), and junction capacitance | 54, 66 |
| CBDBM | LX89 | Total floating body-to-drain capacitance (including intrinsic), and junction capacitance. | 57, 59, 60, 70, 71 |
| CBSBM | LX90 | Total bulk-to-source capacitance (including intrinsic), and junction capacitance | 54, 66 |
| CBSBM | LX90 | Total floating body-to-source capacitance (including intrinsic), and junction capacitance. | 57, 59, 60, 70, 71 |
| CAPFG | LX91 | Fringing capacitance | 54, 66 |
| CDEBM | LX92 | Total drain-to-substrate capacitance (including intrinsic), and junction capacitance. | 57, 59, 60, 70, 71 |
| CSGBM | LX93 | Total source-to-gate capacitance (including intrinsic), and overlap and fringing components. | 57, 59, 60, 70, 71 |
| CSSBM | LX94 | Total source capacitance (including intrinsic), overlap and fringing components, and junction capacitance. | 57, 59, 60, 70, 71 |

Chapter 1: Overview of MOSFET Models

MOSFET Output Templates

| Name | Alias | Description | MOSFET Level |
|---------|-------|---|--------------------|
| CSEBM | LX95 | Total source-to-substrate capacitance (including intrinsic), and junction capacitance. | 57, 59, 60, 70, 71 |
| CEEBM | LX96 | Total substrate capacitance (including intrinsic), overlap and fringing components, and junction capacitance. | 57, 59, 60, 70, 71 |
| QGI | LX97 | Intrinsic Gate charge | 49, 53 |
| QSI | LX98 | Intrinsic Source charge | 49, 53 |
| QDI | LX99 | Intrinsic Drain charge | 49, 53 |
| QBI | LX100 | Intrinsic Bulk charge (Charge Conservation: QBI= -(QGI+ QSI+ QDI)) | 49, 53 |
| CDBBI | LX101 | Intrinsic drain capacitance; only includes derivative of charge | 49, 53 |
| CBDBI | LX102 | Intrinsic bulk-to-drain capacitance; only includes derivative of charge | 49, 53 |
| CBSBI | LX103 | Intrinsic bulk-to-source capacitance; only includes derivative of charge | 49, 53 |
| VBDI | LX109 | Body-drain voltage(VBD)—Meyer and Charge Conservation | 57, 58, 59, 70, 71 |
| IGISLO | LX110 | Gate-induced source leakage current | 54 |
| GRII | LX118 | Intrinsic channel reflected gate conductance | 54 |
| GRGELTD | LX119 | Gate electrode conductance | 54 |
| Ibs1 | LX120 | Bulk to source diffusion current | 57, 59, 60 |
| Ibd1 | LX121 | Bulk to drain diffusion current | 57, 59, 60 |
| Ibs2 | LX122 | Bulk to source recombination/trap-assisted tunneling current | 57, 59, 60 |
| Ibd2 | LX123 | Bulk to drain recombination/trap-assisted tunneling current | 57, 59, 60 |
| Ibs3 | LX124 | Bulk to source recombination current in neutral body | 57, 59, 60 |
| Ibd3 | LX125 | Bulk to drain recombination current in neutral body | 57, 59, 60 |
| Ibs4 | LX126 | Bulk to source reversed bias tunneling leakage current | 57, 59, 60 |
| Ibd4 | LX127 | Bulk to drain reversed bias tunneling leakage current | 57, 59, 60 |
| b4_sca | LX128 | sca for WPE effect | 54 |

Chapter 1: Overview of MOSFET Models
MOSFET Output Templates

| Name | Alias | Description | MOSFET Level |
|------------------|----------------|---|--------------|
| b4_scb | LX129 | scb for WPE effect | 54 |
| b4_scc | LX130 | scc for WPE effect | 54 |
| b4_sc | LX131 | sc for WPE effect | 54 |
| Ueff | LX132 | Effective mobility at the specified analysis temperature. | 66 |
| VGB | LX133 | Gate to bulk voltage | All |
| VDG | LX134 | Drain to gate voltage | All |
| mult | LX135 | Prints value of multiplier (M) for a specified MOSFET | All |
| b4_sa | LX136 | sa for STI or LOD-induced mechanical stress-effects | 54 |
| b4_sb | LX137 | sb for STI or LOD-induced mechanical stress-effects | 54 |
| b4_sd | LX138 | sd for STI or LOD-induced mechanical stress-effects | 54 |
| b4_nf | LX139 | nf for STI or LOD-induced mechanical stress-effects | 54 |
| b4_saeff | LX140 | saeff for STI or LOD-induced mechanical stress-effects | 54 |
| b4_sbeff | LX141 | sbeff for STI or LOD-induced mechanical stress-effects | 54 |
| ivth (m*) | LX142 (m*) | New vth output, based on the monotony Id/Vgs curve obtained through .OPTION IVTH; ivthn and ivthp support NMOS and PMOS, respectively | 54, 69, 70 |
| soiq0 | LX143 (bqi) | Initial floating body charge at t=0 for BQI. If it is not given, 1e35 will be printed. For tran analysis (t>0), the floating body charge will be printed. This parameter only supports BQI. | 57, 60, 70 |
| vdmargin (m*) | LX286 (m*) | Output based on .iVdmargin or .OPTION ivdmargin simulation | 54 |
| TOXE | LX287 | Electrical gate equivalent oxide thickness | 54 |

Additional MOSFET Output templates include:

- [Output Templates for BSIM-CMG, Level 72](#)
- [Output Templates for HiSIM_HV, Level=73](#)
- [Output Templates for UTSOI, Level=76](#)

Chapter 1: Overview of MOSFET Models

MOSFET Output Templates

- Additional Output Templates for PSP and Other Models
- MOSFET SUBCKT Output Templates

Output Templates for BSIM-CMG, Level 72

The following output templates are all in support of the BSIM-CMG model (available beginning with version=103, level=72). The output parameters after IDS (or LX550) are available beginning with version=105.03, level=72. See [BSIM-CMG 105.03 Updates](#).

| Name | Alias | Description |
|-----------|-------|---|
| LEFF | LX501 | Effective channel length |
| WEFF | LX502 | Effective channel width per fin |
| LEFFCV | LX503 | Effective channel length for CV |
| WEFFCV | LX504 | Effective channel width per fin for CV |
| AS | LX505 | Source area |
| AD | LX506 | Drain area |
| PS1 | LX507 | 1st part of the source perimeter |
| PD1 | LX508 | 1st part of the drain perimeter |
| PS2 | LX509 | 2nd part of the source perimeter |
| PD2 | LX510 | 2nd part of the drain perimeter |
| D | LX511 | Diameter of cylinder |
| NFIN | LX512 | Number of fins per finger |
| NFINTOTAL | LX513 | Number of the total fins |
| TFIN | LX514 | Fin (channel) thickness |
| CGSP | LX515 | Constant gate to source fringe capacitance |
| CGDP | LX516 | Constant gate to drain fringe capacitance |
| CDSP | LX517 | Constant drain to source fringe capacitance |

| Name | Alias | Description |
|------------|-------|--|
| NBODY | LX518 | Channel doping concentration after geometry scaling |
| PHIG | LX519 | Work function of gate after geometry scaling |
| NGATE | LX520 | Parameter for Poly Gate doping (0 for metal gate) after geometry scaling |
| U0 | LX521 | Low field mobility after geometry scaling |
| MEXP | LX522 | Smoothing function factor for Vdsat after geometry scaling |
| VSAT | LX523 | Saturation velocity after geometry scaling |
| UA | LX524 | MOBMOD = 0 phonon / surface roughness scattering after geometry scaling |
| UD | LX525 | MOBMOD = 0 coulombic scattering (Experimental) after geometry scaling |
| CS | LX526 | MOBMOD = 1 coulombic scattering parameter after geometry scaling |
| THETAMU | LX527 | MOBMOD = 1 mobility reduction exponent after geometry scaling |
| THETASAT | LX528 | Velocity saturation parameter after geometry scaling |
| PTWG | LX529 | Correction factor for velocity saturation after geometry scaling |
| MUE | LX530 | MOBMOD = 1 mobility reduction co-efficient after geometry scaling |
| NSD | LX531 | S/D doping concentration after geometry scaling |
| RSOURCEGO | LX532 | Geometry dependent source resistance after geometry scaling |
| RDRAINAGEO | LX533 | Geometry dependent drain resistance after geometry scaling |
| GTH | LX534 | Thermal resistance for self-heating calculation after geometry scaling |
| CTH | LX535 | Thermal capacitance for self-heating calculation after geometry scaling |
| VDSAT | LX536 | Saturation voltage (VDSAT) |
| UEFF | LX537 | Effective mobility at the specified analysis temperature |
| RSOURCE | LX538 | Source series resistance |
| RDRAIN | LX539 | Drain series resistance |
| RGELTD | LX540 | Gate electrode resistance |

Chapter 1: Overview of MOSFET Models

MOSFET Output Templates

| Name | Alias | Description |
|----------|-------|---|
| III | LX541 | Impact ionization current |
| IGBINV | LX542 | Gate to body current |
| IGCINV | LX543 | Gate to channel current |
| IGIDL | LX544 | Gate-induced drain leakage current |
| IGISL | LX545 | Gate-induced source leakage current |
| IGSO | LX546 | Total gate-to-source current including both the source partition of gate-to-channel tunneling current (Igcs) and the tunneling current due to gate-to-source overlap (Igs). |
| IGDO | LX547 | Total gate-to-drain current including both the drain partition of gate-to-channel tunneling current (Igcd) and the tunneling current due to gate-to-drain overlap (Igd). |
| QD | LX548 | Intrinsic drain charge |
| QG | LX549 | Intrinsic gate charge |
| IDS | LX550 | Channel current |
| QG_TOTAL | LX551 | Total Gate charge |
| QD_TOTAL | LX552 | Total Drain charge |
| QS_TOTAL | LX553 | Total Source charge |
| QB_TOTAL | LX554 | Total Bulk charge |
| IGS | LX555 | Tunneling current due to gate-to-source overlap (Igs). |
| IGD | LX556 | Tunneling current due to gate-to-drain overlap (Igd). |
| IGBS | LX557 | Source part of gate to Body Tunneling current for BULKMOD=0 |
| IGBD | LX558 | Drain part of gate to Body Tunneling current for BULKMOD=0 |
| IGCS | LX559 | Source Partition of IGC |
| IGCD | LX560 | Drain Partition of IGC |
| RSGEO | LX561 | External bias independent Source Resistance |
| RDGEO | LX562 | External bias independent Drain Resistance |

| Name | Alias | Description |
|----------|-------|---|
| CFGEO | LX563 | Geometric Parasitic Cap for CGEOMOD=2 |
| DIDSDVG | LX564 | DC MOSFET gate transconductance (G_m) |
| DIDSDVS | LX565 | DC source-drain conductance |
| DIDSDVD | LX566 | DC drain-source conductance (G_{ds}) |
| DIDSDVTH | LX567 | DC temperature transconductance |
| CGG | LX568 | Total gate capacitance ($C_{GG} = dQ_g/dV_g$) |
| CGS | LX569 | Total gate-to-source capacitance ($C_{GS} = -dQ_g/dV_s$) |
| CGD | LX570 | Total gate-to-drain capacitance ($C_{GD} = -dQ_g/dV_d$) |
| CSG | LX571 | Total source-to-gate capacitance ($C_{SG} = -dQ_s/dV_g$) |
| CSD | LX572 | Total source-to-drain capacitance ($C_{SD} = -dQ_s/dV_d$) |
| CSS | LX573 | Total Source capacitance ($C_{SS} = dQ_s/dV_s$) |
| CDG | LX574 | Total drain-to-gate capacitance ($C_{DG} = -dQ_d/dV_g$) |
| CDD | LX575 | Total drain capacitance ($C_{DD} = dQ_d/dV_d$) |
| CDS | LX576 | Total drain-to-source capacitance ($C_{DS} = -dQ_d/dV_s$) |
| CGT | LX577 | Temperature dependence of gate charge |
| CST | LX578 | Temperature dependence of source charge |
| CDT | LX579 | Temperature dependence of drain charge |
| ITH | LX580 | Power dissipation ($I_{ds} * V_{ds}$) of channel current |
| CJDB | LX581 | Bias dependent bulk-drain capacitance |
| CJSB | LX582 | Bias dependent bulk-source capacitance |
| COVLGS | LX583 | Gate-source overlap and fringing capacitances |
| COVLGD | LX584 | Gate-drain overlap and fringing capacitances |
| COVLGB | LX585 | Gate-bulk overlap capacitances |
| CGGBO | LX586 | Intrinsic gate capacitance |

Chapter 1: Overview of MOSFET Models

MOSFET Output Templates

| Name | Alias | Description |
|---------|-------|--|
| CGDBO | LX587 | Intrinsic gate-to-drain capacitance |
| CGSBO | LX588 | Intrinsic gate-to-source capacitance |
| CAP_BS | LX589 | Bias dependent bulk-source capacitance (alias to CJSB) |
| CAP_BD | LX590 | Bias dependent bulk-drain capacitance (alias to CJDB) |
| CGGBM | LX591 | Total gate capacitance (including intrinsic), and all overlap and fringing components |
| IVTH | LX592 | New vth output, based on the monotonic Id/Vgs curve obtained through .OPTION IVTH/IVTHN/IVTHP (supporting NMOS and PMOS, respectively) or the command .IVTH. |
| DIDSDVB | LX593 | DC MOSFET bulk transconductance (Gmbs) |
| VTH | LV9 | Threshold voltage |
| SFT | LX594 | Self-heating temperature |
| CGB | LX595 | Total gate-to-bulk capacitance ($CGB = -dQg/dVb$) |
| CDB | LX596 | Total drain-to-bulk capacitance ($CDB = -dQd/dVb$) |
| CSB | LX597 | Total source-to-bulk capacitance ($CSB = -dQs/dVb$) |
| CBG | LX598 | Total bulk-to-gate capacitance ($CBG = -dQb/dVg$) |
| CBD | LX599 | Total bulk-top-drain capacitance ($CBD = -dQb/dVd$) |
| CBS | LX600 | Total bulk-to-source capacitance ($CBS = -dQb/dVs$) |
| CBB | LX601 | Total bulk capacitance ($CBB = dQb/dVb$) |
| CGBBO | LX602 | Intrinsic gate-to-bulk capacitance |
| CSGBO | LX603 | Intrinsic source-to-gate capacitance |
| CSDBO | LX604 | Intrinsic source-to-drain capacitance |
| CSSBO | LX605 | Intrinsic source capacitance |
| CSBBO | LX606 | Intrinsic source-to-bulk capacitance |
| CDGBO | LX607 | Intrinsic drain-to-gate capacitance |
| CDDBO | LX608 | Intrinsic drain capacitance |

| Name | Alias | Description |
|-------|-------|---------------------------------------|
| CDSBO | LX609 | Intrinsic drain-to-source capacitance |
| CDBBO | LX610 | Intrinsic drain-to-bulk capacitance |
| CBGBO | LX611 | Intrinsic bulk-to-gate capacitance |
| CBDBO | LX612 | Intrinsic bulk-to-drain capacitance |
| CBSBO | LX613 | Intrinsic bulk-to-source capacitance |
| CBBBO | LX614 | Intrinsic bulk capacitance |

Output Templates for HiSIM_HV, Level=73

HSPICE supports parameter output templates for all HiSIM_HV versions beginning with version 1.00 through 2.10

| Name | Alias | Description |
|-------|-------|--|
| L | LX291 | Channel Length (L) |
| W | LX292 | Channel Width (W) |
| AD | LX293 | Area of the drain diode (AD) |
| AS | LX294 | Area of the source diode (AS) |
| ICVDS | LX295 | Initial condition for the drain-source voltage (VDS) |
| ICVGS | LX296 | Initial condition for the gate-source voltage (VGS) |
| ICVBS | LX297 | Initial condition for the bulk-source voltage (VBS) |
| PD | LX298 | Drain diode periphery (PD) |
| PS | LX299 | Source diode periphery (PS) |
| RSS | LX301 | Source resistance (squares) (RSS) |
| WEFF | LX302 | Effective channel width |
| LEFF | LX303 | Effective channel length |
| CAPFG | LX304 | Fringing capacitance |

Chapter 1: Overview of MOSFET Models

MOSFET Output Templates

| Name | Alias | Description |
|----------|-------|---|
| VTH | LX305 | Threshold voltage (bias dependent) |
| VDSAT | LX306 | Saturation voltage (VDSAT) |
| GDEFF | LX307 | Effective drain conductance (1/RDeff) |
| GSEFF | LX308 | Effective source conductance (1/RSeff) |
| VDBEFF | LX309 | Effective drain bulk voltage. |
| BETAEFF | LX310 | BETA effective |
| GAMMAEFF | LX311 | GAMMA effective |
| VFBEFF | LX312 | VFB effective |
| COVLGS | LX313 | Gate-source overlap and fringing capacitances |
| COVLGD | LX314 | Gate-drain overlap and fringing capacitances |
| COVLGB | LX315 | Gate-bulk overlap capacitances |
| VBD | LX316 | Bulk-drain voltage |
| VBS | LX317 | Bulk-source voltage (VBS) |
| VGS | LX318 | Gate-source voltage (VGS) |
| VDS | LX319 | Drain-source voltage (VDS) |
| CDO | LX320 | Channel current (IDS) |
| CBSO | LX321 | DC source-bulk diode current (CBSO) |
| CBDO | LX322 | DC drain-bulk diode current (CBDO) |
| GMO | LX323 | DC MOSFET gate transconductance (GMO) |
| GDSO | LX324 | DC drain-source conductance (GDSO) |
| GMBSO | LX325 | DC substrate transconductance (GMBSO) |
| GBDO | LX326 | Conductance of the drain diode (GBDO) |
| GBSO | LX327 | Conductance of the source diode (GBSO) |
| QB | LX328 | Total bulk (body) charge (QB)—Meyer and Charge Conservation |

| Name | Alias | Description |
|--------|-------|--|
| CQB | LX329 | Bulk (body) charge current (CQB)—Meyer and Charge Conservation |
| QG | LX330 | Total Gate charge (QG)—Meyer and Charge Conservation |
| CQG | LX331 | Gate charge current (CQG)—Meyer and Charge Conservation |
| QD | LX332 | Channel charge (QD) |
| CQD | LX333 | Channel charge current (CQD) |
| CGGBO | LX334 | Intrinsic gate capacitance |
| CGDBO | LX335 | Intrinsic gate-to-drain capacitance |
| CGSBO | LX336 | Intrinsic gate-to-source capacitance |
| CBGBO | LX337 | Intrinsic bulk-to-gate capacitance |
| CBDBO | LX338 | Intrinsic bulk-to-drain capacitance |
| CBSBO | LX339 | $CBSBO = -dQb/dVs$ |
| QBD | LX340 | Drain-bulk charge (QBD) |
| QBS | LX341 | Source-bulk charge (QBS) |
| CAP_BS | LX342 | Bias dependent bulk-source capacitance |
| CAP_BD | LX343 | Bias dependent bulk-drain capacitance |
| CDGBO | LX344 | Intrinsic drain-to-gate capacitance |
| CDDBO | LX345 | Intrinsic drain capacitance |
| CDSBO | LX346 | $CDSBO = -dQd/dVs$, Drain-to-source capacitance |
| SFT | LX347 | Value of the temperature node |
| weffcv | LX348 | Effective channel width for CV |
| leffcv | LX349 | Effective channel length for CV |
| igso | LX350 | Gate-to-Source Current |
| igdo | LX351 | Gate-to-Drain Current |
| igbo | LX352 | Gate-to-Substrate Current |

Chapter 1: Overview of MOSFET Models

MOSFET Output Templates

| Name | Alias | Description |
|---------|-------|--|
| igcso | LX353 | Source Partition of Ig _c |
| igcdo | LX354 | Drain Partition of Ig _c |
| iimi | LX355 | Impact ionization current |
| igidlo | LX356 | Gate-induced drain leakage current |
| igislo | LX357 | Gate-induced source leakage current |
| igdt | LX358 | Gate Dielectric Tunneling Current ($I_g = I_{gs} + I_{gd} + I_{gcs} + I_{gcd} + I_{gb}$) |
| vgse | LX359 | Effective Gate-to-Source Voltage |
| rdv | LX360 | Asymmetric and Bias-Dependent Source Resistance |
| rsv | LX361 | Asymmetric and Bias-Dependent Drain Resistance |
| cap_bsz | LX362 | Zero voltage bias bulk-source capacitance |
| cap_bdz | LX363 | Zero voltage bias bulk-drain capacitance |
| CGGBM | LX364 | Total gate capacitance (including intrinsic), and overlap and fringing components |
| CGDBM | LX365 | Total gate-to-drain capacitance (including intrinsic), and overlap and fringing components |
| CGSBM | LX366 | Total gate-to-source capacitance (including intrinsic), and overlap and fringing components |
| CDDBM | LX367 | Total drain capacitance (including intrinsic), overlap and fringing components, and junction capacitance |
| CDSBM | LX368 | Total drain-to-source capacitance |
| CDGBM | LX369 | Total drain-to-gate capacitance (including intrinsic), and overlap and fringing components |
| CBGBM | LX370 | Total bulk-to-gate (floating body-to-gate) capacitance, including intrinsic and overlap components |
| CBDBM | LX371 | Total bulk-to-drain capacitance (including intrinsic) and junction capacitance |
| CBSBM | LX372 | Total bulk-to-source capacitance (including intrinsic), and junction capacitance |
| Ueff | LX373 | Effective mobility at the specified analysis temperature |

| Name | Alias | Description |
|----------|-------|---|
| VGB | LX374 | Gate to bulk voltage |
| VDG | LX375 | Drain to gate voltage |
| mult | LX376 | Prints value of multiplier (M) for a specified MOSFET |
| sa | LX377 | sa for STI or LOD-induced mechanical stress-effects |
| sb | LX378 | sb for STI or LOD-induced mechanical stress-effects |
| sd | LX379 | sd for STI or LOD-induced mechanical stress-effects |
| hsmhv_nf | LX380 | nf for STI or LOD-induced mechanical stress-effects |

Output Templates for UTSOI, Level=76

HSPICE supports parameter output templates for all UTSOI versions beginning with version 1.1.1 through 2.2.0

| Name | Alias | Description |
|-------|-------|---------------------------------|
| L | LV1 | Channel length (L) |
| W | LV2 | Channel width (W) |
| VTH | LV9 | Threshold voltage |
| VDSAT | LV10 | Saturation voltage |
| VBD | LX0 | Bulk-drain voltage |
| VBS | LX1 | Bulk-source voltage |
| VGS | LX2 | Gate-source voltage |
| VDS | LX3 | Drain-source voltage |
| CDO | LX4 | Channel current (IDS) |
| GMO | LX7 | DC MOSFET gate transconductance |
| GDSO | LX8 | DC drain-source conductance |
| GMBSO | LX9 | DC substrate transconductance |

Chapter 1: Overview of MOSFET Models

MOSFET Output Templates

| Name | Alias | Description |
|-------|-------|--|
| QB | LX12 | Total bulk charge |
| CQB | LX13 | Bulk charge current |
| QG | LX14 | Total gate charge |
| CQG | LX15 | Gate charge current |
| QD | LX16 | Total drain charge |
| CQD | LX17 | Drain charge current |
| CGGBO | LX18 | Total gate capacitance (Including intrinsic/overlap/fringing) |
| CGDBO | LX19 | Gate to drain capacitance (Including intrinsic/overlap/fringing) |
| CGSBO | LX20 | Gate to source capacitance (Including intrinsic/overlap/fringing) |
| CBGBO | LX21 | Substrate to gate capacitance (Including intrinsic/overlap/fringing) |
| CBDBO | LX22 | Substrate to drain capacitance (Including intrinsic/overlap/fringing) |
| CBSBO | LX23 | Substrate to source capacitance (Including intrinsic/overlap/fringing) |
| CDGBO | LX32 | Drain to gate capacitance (Including intrinsic/overlap/fringing) |
| CDDBO | LX33 | Total drain capacitance (Including intrinsic/overlap/fringing) |
| CDSBO | LX34 | Drain to source capacitance (Including intrinsic/overlap/fringing) |
| IGSO | LX501 | Gate to source current |
| IGDO | LX502 | Gate to drain current |
| IGIDL | LX503 | Gate induced drain leakage current |
| IGISL | LX504 | Gate induced source leakage current |
| CGSF | LX505 | Fringing capacitance at source side |
| CGDF | LX506 | Fringing capacitance at drain side |
| CGSOV | LX507 | Overlap capacitance at source side |
| CGDOV | LX508 | Overlap capacitance at drain side |
| CGBOV | LX509 | Oxide capacitance for gate to substrate overlap |

| Name | Alias | Description |
|------|-------|---|
| CBDE | LX510 | Drain to substrate extrinsic capacitance |
| CBSE | LX511 | Source to substrate extrinsic capacitance |
| CDSE | LX512 | Drain to source coupling capacitance |
| SFT | LX513 | Value of the temperature node |
| WEFF | LX514 | Effective channel width |
| LEFF | LX515 | Effective channel length |

Additional Output Templates for PSP and Other Models

The following output templates do not require an HSPICE alias and are all in support of the PSP model. Note that LPOLY and WPOLY also support BSIM3, BSIM4, BSIM3-SOI, and BSIM4-SOI models.

| Name | Description | Model Level |
|--------|---|------------------------|
| LPOY | POLY Length | 49,53,54,57, 69, 70 |
| WPOLY | POLY Width | 49,53,54,57,69 ,70 |
| VFB | Flat-band voltage at TR after geometry scaling | 69 |
| STVFB | Temperature dependence of VFB after geometry scaling | 69 |
| TOX | Gate oxide thickness after geometry scaling | 69 |
| EPSROX | Relative permittivity of gate dielectric after geometry scaling | 69 |
| NEFF | Substrate doping after geometry scaling | 69 |
| VNSUB | Effective doping bias-dependence parameter after geometry scaling | 69 |
| NSLP | Effective doping bias-dependence parameter after geometry scaling | 69 |
| DNSUB | Effective doping bias-dependence parameter after geometry scaling | 69 |
| DPHIB | Offset of φB after geometry scaling | 69 |

Chapter 1: Overview of MOSFET Models

MOSFET Output Templates

| Name | Description | Model Level |
|----------|--|-------------|
| NP | NP Gate poly-silicon doping after geometry scaling | 69 |
| CT | Interface states factor after geometry scaling | 69 |
| TOXOV | Overlap oxide thickness after geometry scaling | 69 |
| NOV | Effective doping of overlap region after geometry scaling | 69 |
| CF | DIBL parameter after geometry scaling | 69 |
| CFB | Back-bias dependence of CF after geometry scaling | 69 |
| BETN | Product of channel aspect ratio and zero field mobility at TR after geometry scaling | 69 |
| STBET | Temperature dependence of BETN after geometry scaling | 69 |
| MUE | Mobility reduction coefficient at TR after geometry scaling | 69 |
| STMUE | Temperature dependence of MUE after geometry scaling | 69 |
| THEMU | Mobility reduction exponent at TR after geometry scaling | 69 |
| STTHEMU | Temperature dependence of THEMU after geometry scaling | 69 |
| CS | Coulomb scattering parameter at TR after geometry scaling | 69 |
| STCS | Temperature dependence of CS after geometry scaling | 69 |
| XCOR | Non-universality parameter after geometry scaling | 69 |
| STXCOR | Temperature dependence of XCOR after geometry scaling | 69 |
| FETA | Effective field parameter after geometry scaling | 69 |
| RS | Source/drain series resistance at TR after geometry scaling | 69 |
| STRS | Temperature dependence of RS after geometry scaling | 69 |
| RSB | Back-bias dependence of RS after geometry scaling | 69 |
| RSG | Gate-bias dependence of RS) after geometry scaling | 69 |
| THESAT | Velocity saturation parameter at TR after geometry scaling | 69 |
| STTHESAT | Temperature dependence of THESAT after geometry scaling | 69 |

Chapter 1: Overview of MOSFET Models
MOSFET Output Templates

| Name | Description | Model Level |
|---------|---|-------------|
| THESATB | Back-bias dependence of velocity saturation after geometry scaling | 69 |
| THESATG | Gate-bias dependence of velocity saturation) after geometry scaling | 69 |
| AX | Linear/saturation transition factor after geometry scaling | 69 |
| ALP | CLM pre-factor after geometry scaling | 69 |
| ALP1 | CLM enhancement factor above threshold) after geometry scaling | 69 |
| ALP2 | CLM enhancement factor below threshold) after geometry scaling | 69 |
| VPO | CLM logarithmic dependence parameter) after geometry scaling | 69 |
| A1 | Impact-ionization pre-factor after geometry scaling | 69 |
| A2 | Impact-ionization exponent at TR after geometry scaling | 69 |
| STA2 | Temperature dependence of A2 after geometry scaling | 69 |
| A3 | Saturation-voltage dependence of II after geometry scaling | 69 |
| A4 | Back-bias dependence of II after geometry scaling | 69 |
| GCO | Gate tunneling energy adjustment after geometry scaling | 69 |
| IGINV | Gate channel current pre-factor after geometry scaling | 69 |
| IGOV | Gate overlap current pre-factor after geometry scaling | 69 |
| STIG | Temperature dependence of gate current after geometry scaling | 69 |
| GC2 | Gate current slope factor after geometry scaling | 69 |
| GC3 | Gate current curvature factor after geometry scaling | 69 |
| CHIB | Tunneling barrier height) after geometry scaling | 69 |
| AGIDL | GIDL pre-factor after geometry scaling | 69 |
| BGIDL | GIDL probability factor at TR after geometry scaling | 69 |
| STBGIDL | Temperature dependence of BGIDL after geometry scaling | 69 |
| CGIDL | Back-bias dependence of GIDL after geometry scaling | 69 |
| COX | Oxide capacitance for intrinsic channel after geometry scaling | 69 |

Chapter 1: Overview of MOSFET Models

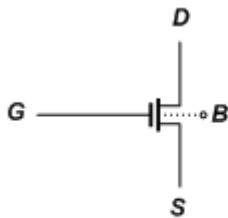
MOSFET Output Templates

| Name | Description | Model Level |
|-----------|--|-------------|
| CGOV | Oxide capacitance for gate-drain/source overlap after geometry scaling | 69 |
| CGBOV | Oxide capacitance for gate-bulk overlap after geometry scaling | 69 |
| CFR | Outer fringe capacitance after geometry scaling | 69 |
| NFA | First coefficient of flicker noise after geometry scaling | 69 |
| NFB | Second coefficient of flicker noise) after geometry scaling | 69 |
| NFC | Third coefficient of flicker noise after geometry scaling | 69 |
| KVTHOWE | Threshold shift parameter after geometry scaling | 69 |
| KUOWE | Mobility degradation factor after geometry scaling | 69 |
| TOXOVD | Overlap oxide thickness for drain side after geometry scaling | 69 |
| NOVD | Effective doping of overlap region for drain side after geometry scaling | 69 |
| IGOVD | Gate overlap current pre-factor for drain side after geometry scaling | 69 |
| AGIDLD | GIDL pre-factor for drain side after geometry scaling | 69 |
| BGIDLD | GIDL probability factor at TR for drain side after geometry scaling | 69 |
| STBGIDLD | Temperature dependence of BGIDL for drain side after geometry scaling | 69 |
| CGIDLD | Back-bias dependence of GIDL for drain side after geometry scaling | 69 |
| CGOVD | Oxide capacitance for gate-drain/source overlap for drain side after geometry scaling | 69 |
| CFRD | Outer fringe capacitance for drain side after geometry scaling | 69 |
| EF | Flicker noise frequency exponent after geometry scaling | 69 |
| FACNEFFAC | Pre-factor for effective substrate doping in separate charge calculation when SWDELVTAC = 1 after geometry scaling | 69 |
| GFACNUD | Body factor change due to NUD-effect after geometry scaling | 69 |
| VSBNUD | Lower VSB-value for NUD-effect after geometry scaling | 69 |
| DVSBNUD | VSB-range for NUD-effect after geometry scaling | 69 |

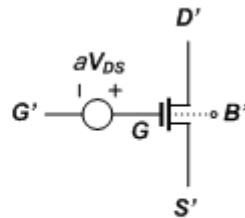
| Name | Description | Model Level |
|---------|---|-------------|
| DELVTAC | Offset of φB in separate charge calculation when SWDELVTAC=1 after geometry scaling | 69 |
| MOBEFF | Effective mobility at the specified analysis temperature. Note: For PSP, the effective mobility calculation considers geometry and temperature scaling, plus mechanical stress and electrical field-induced mobility change. | 54, 69, 70 |
| CGGI | Intrinsic gate capacitance | 69 |
| CGDI | Intrinsic gate to drain capacitance | 69 |
| CGSI | Intrinsic gate to source capacitance | 69 |

MOSFET SUBCKT Output Templates

Given modeling limitations of intrinsic MOSFET models such as BSIM4 across process corners, it is necessary to define a MOSFET model as a SUBCKT macro-model comprising not only the intrinsic MOSFET model but also additional circuit elements, so that the resulting SUBCKT describes expected silicon behavior more accurately. The following is an illustration of a simple SUBCKT macro-model where an intrinsic BSIM4.6 MOSFET model has been modified by a voltage-dependent voltage source in series with the gate input to modify DIBL behavior.



Intrinsic MOSFET model



MOSFET macro-model

The conventional HSPICE output template infrastructure provides MOSFET biasing information such as V_{GS} , V_{GD} , V_{DS} , V_T , I_D , I_G , I_D , I_B , g_m , g_{ds} , and V_{Dsat} for only the intrinsic MOSFET model inside the SUBCKT, whereas the output template of the overall SUBCKT macro-model is really desired. To overcome this limitation, the output template infrastructure has been extended to report critical device characteristics of a SUBCKT macro-model.

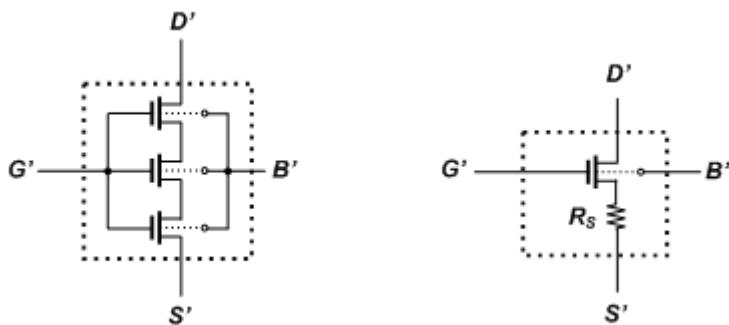
Chapter 1: Overview of MOSFET Models

MOSFET Output Templates

Conventional output template = $f(V_D, V_G, V_S, V_B)$

Macro-model output template = $f(V_{D'}, V_{G'}, V_{S'}, V_{B'})$

The output template capability has been generalized to facilitate macro-model hierarchy for a generalized 4-terminal MOSFET structure. The following illustration shows a macro-model defined as a composite stack of MOSFETs (each MOSFET potentially a macro-model itself) with a common gate connection or as a MOSFET with resistive source degeneration. These are typical approaches in nanoscale analog design to overcome channel length and output resistance limitations.



In these situations, the designer is primarily interested in the collective behavior of the stacked MOSFETs, for example, as opposed to the individual behavior of each MOSFET in the stack.

Macro-model output templates are calculated based on probing the SUBCKT ports or terminals and observing the subsequent “black-box” behavior. Such terminal-based measurements facilitate easier correlation of simulations to silicon measurements. Parameters such as V_{dsat} that are based on model-specific equations are no longer available as output templates for the SUBCKT macro-model.

Analysis Type: DC/AC/OP and user specified TRAN point (normal TRAN analysis is not supported as runtime impact would be too significant).

Example of user specified TRAN point: `.op 1n 2.5n 10n` (The SUBCKT output templates are probed and available only at the three specified time instances and are not available at other time instances in the TRAN analysis).

For example,

```
.print dc LX7(X1)
.print ac LX7(X1)
.print tran LX7(X1)
```

Models: No restrictions except for VA module and VEC source.

Date Input Requirement: SUBCKT consists of exactly 4 terminals with order fixed as Drain (d), Gate (g), Source (s), and Bulk (b) which can constrain number of levels of hierarchy.

For example,

```
.subckt nch_mac d g s b
+ w=0 l=0
rd d d1 r=20
rg g g1 r=20
rs s s1 r=20
main d1 g1 s1 b nch w='w' l='l'
.ends
.subckt nmos d g s b
+ w=0 l=0
rd d d1 r=100
rg g g1 r=100
rs s s1 r=100
XMN d1 g1 s1 b nch_mac w='w' l='l'
.ends
X1 d g s b nmos w='w' l='l'
```

Note: LX7(X1) and LX7(X1.XMN) are all supported.

| Name | Alias | Description |
|------|-------|--|
| VBD | LX0 | SUBCKT body to drain voltage ($V_B - V_D$). |
| VBS | LX1 | SUBCKT body to source voltage ($V_B - V_S$). |
| VGS | LX2 | SUBCKT gate to source voltage ($V_G - V_S$). |
| VDS | LX3 | SUBCKT drain to source voltage ($V_D - V_S$). |
| VDG | LX134 | SUBCKT drain to gate voltage ($V_D - V_G$). |
| ID | | Current flow into/out of SUBCKT D', flow into SUBCKT is "+". |
| IG | | Current flow into/out of SUBCKT G', flow into SUBCKT is "+". |
| IS | | Current flow into/out of SUBCKT S', flow into SUBCKT is "+". |
| IB | | Current flow into/out of SUBCKT B', flow into SUBCKT is "+". |
| GM | LX7 | SUBCKT gate transconductance ($d i(V_D) / d V_G$). |

Chapter 1: Overview of MOSFET Models

Safe Operating Area Voltage Warning

| Name | Alias | Description |
|----------|-------|--|
| GDS | LX8 | SUBCKT drain conductance ($d i(V_D) / d V_D$). |
| GMBS | LX9 | SUBCKT body transconductance ($d i(V_D) / d V_B$). |
| IVTH | LX142 | Constant-current based threshold voltage. Device w and L must be explicitly declared to compute LX142. |
| VDMARGIN | LX286 | MOSFET drain voltage margin available before MOSFET drain conductance degrades (increases) by user-specified target with respect to existing bias point. |

Safe Operating Area Voltage Warning

The following warning message is issued when terminal voltages of a device (MOSFET, BJT, Diode, Resistor, Capacitor, etc.) exceed their safe operating area (SOA):

```
**warning** (filename:line number) resulted during SOA check
<node voltage name> (=val) of <device/element name> has exceeded
<node voltage name>_max (=val)
```

To turn it off use .option WARN=0

Example Warnings

```
**Warning** (res1 : r1) : Vr = 1.00      has exceeded Bv_max = 0.900
**Warning** (cap1 : c1) : Vr = 1.00      has exceeded Bv_max = 0.900
**Warning** (dio1 : d1) : Vr = 1.00      has exceeded Bv_max = 0.900
**Warning** (bjt1: q_gp1) :Vbe = 1.00 has exceeded Vbe_max = 0.800
**Warning** (mos49 : m1) : Vgs = 1.00 has exceeded Vgs_max = 0.900
**Warning** (mos49 : m1) : Vgb = 1.00 has exceeded Vgs_max = 0.900
**Warning** (mos49 : m1) : Vds = 1.00 has exceeded Vds_max = 0.900
**Warning** (mos49 : m1) : Vbd = -1.00 has exceeded Vbd_max = 0.900
```

See the following control options for details:

- [.OPTION WARN](#)
- [.OPTION MAXWARNS](#)

For details on the warnings issued, see [Safe Operating Area \(SOA\) Warnings](#) in the *HSPICE User Guide: Basic Simulation and Analysis*.

Model Pre-Processing and Parameter Flattening

You can invoke model pre-processing and parameter flattening by using .OPTION MODPRT=1. For details, see [.OPTION MODPRT](#) in the *HSPICE Reference Manual: Commands and Control Options*.

Use of Example Syntax

To copy and paste proven syntax use the demonstration files shipped with your installation of HSPICE (see [Listing of Demonstration Input Files](#)). Attempting to copy and paste from the book or help documentation may present unexpected results, as text used in formatting may include hidden characters, white space, etc. for visual clarity.

Chapter 1: Overview of MOSFET Models

Use of Example Syntax

2

MOSFET Models

Lists and describes standard MOSFET models.

This section covers the following MOSFET models:

| Synopsys Level: Model | Model Parameters | Comments |
|-------------------------------------|--|--|
| | Common MOSFET Model Parameters | |
| LEVEL 77: BSIM6 MOSFET Model | BSIM6 Model Parameters | - |
| LEVEL 76: LETI-UTSOI MOSFET Model | <ul style="list-style-type: none">■ UTSOI Model-Global Flags and Parameters■ UTSOI Model-Local Parameters (SWSCALE=0)■ UTSOI Model-Global Parameters (SWSCALE=1) | - |
| LEVEL 74: MOS Model 20 Model | MOS Model 20 Instances and Parameters | - |
| LEVEL 73: HiSIM_HV Model | HiSIM_HV Model Parameters | CMC Open Standards |
| LEVEL 72: BSIM-CMG MOSFET Model | <ul style="list-style-type: none">■ BSIM-CMG Model Parameters (Version >= 105)■ BSIM-CMG Model Parameters (Version < 105)■ BSIM-CMG Model WPE Support (Version=105.03) | CMC Open Standards. Popularly known as FinFET. |
| LEVEL 71: TFT Model | TFT Model Parameters | - |
| LEVEL 70: BSIMSOI4 Model | BSIMSOI4 Model Parameters | CMC Open Standards |
| LEVEL 69: PSP Model | <ul style="list-style-type: none">■ PSP 103.1 Model Parameters■ PSP 103.1 Instance Parameters | CMC Open Standards |
| LEVEL 68: STARC HiSIM2 MOSFET Model | <ul style="list-style-type: none">■ STARC HiSIM2 Model Parameters■ STARC HiSIM2 Model Instance Parameters | CMC Open Standards |

Chapter 2: MOSFET Models

| Synopsys Level: Model | Model Parameters | Comments |
|---|---|--------------------------------------|
| LEVEL 66: HSPICE HVMOS Model | HSPICE HVMOS Model Parameters | - |
| LEVEL 65: SSIMSOI Model | SSIMSOI Model Parameters | - |
| LEVEL 64: STARC HiSIM MOSFET Model | STARC HiSIM Model Parameters | - |
| LEVEL 63: Philips MOS11 Model | Philips MOS11 Model Parameters | - |
| LEVEL 62: RPI Poli-Si TFT Model | RPI Poli-Si TFT Model Parameters | - |
| LEVEL 61: RPI a-Si TFT Model | RPI a-Si TFT Model Parameters | - |
| LEVEL 60: BSIM3 SOI DD Model | BSIM3 SOI DD Model Parameters | - |
| LEVEL 59: BSIM3 SOI FD Model | BSIM3 SOI FD Model Parameters | - |
| LEVEL 58: UFSOI MOSFET Model | <ul style="list-style-type: none"> ■ UFSOI Model — FDSOI Parameters ■ UFSOI Model — NFDSOI Parameters | - |
| LEVEL 57: BSIM3 SOI Model | BSIM3 SOI Model Parameters | CMC Open Standards |
| LEVEL 55: EPFL-EKV MOSFET Model | - | - |
| LEVEL 54: BSIM4 MOSFET Model | BSIM4 MOSFET Model Parameters | CMC Open Standards |
| LEVEL 50: Philips MOS9 Model | <ul style="list-style-type: none"> ■ Philips MOS9 Model Parameters ■ Philips MOS9 Model — JUNCAP Parameters | - |
| LEVEL 49 and 53: BSIM3 Version 3 MOSFET Model | BSIM3 Version 3 MOSFET Model Parameters | CMC Open Standards |
| LEVEL 47: BSIM3 Version 2 MOSFET Model | BSIM3 Version 2 MOSFET Model Parameters | - |
| LEVEL 40: HP a-Si TFT Model | - | - |
| LEVEL 39: BSIM2 Model | BSIM2 Model Parameters | - |
| LEVEL 38: Cypress Depletion Model | Cypress Depletion Model Parameters | Used to model depletion MOS devices. |
| LEVEL 28: BSIM Derived Model | BSIM Derived Model Parameters | - |

| Synopsys Level: Model | Model Parameters | Comments |
|---|--|--|
| LEVEL 27: SOSFET Model | SOSFET Model Parameters | Used to model Silicon-On-Sapphire MOS devices. You can include photocurrent effects at this level. |
| LEVEL 13: BSIM Model | BSIM Model Parameters | - |
| LEVEL 8: Advanced LEVEL 2: MOS2 Grove-Frohman Model (SPICE 2G) | Advanced LEVEL 2: MOS2 Grove-Frohman (SPICE 2G) Model Parameters | - |
| LEVEL 7: Lattin-Jenkins-Grove (SPICE) Model | - | - |
| LEVEL 6: Lattin-Jenkins-Grove (ASPEC) Model | Lattin-Jenkins-Grove (ASPEC) Model Parameters | Compatible with models originally developed using ASPEC. Used to model ion-implanted devices. |
| LEVEL 5: AMI-ASPEC Depletion and Enhancement (Taylor-Huang) Model | AMI-ASPEC Model Parameters | Used to model depletion MOS devices. |
| LEVEL 4: Grove-Frohman-LEVEL 2 Model Derived from SPICE 2E.3 | - | - |
| LEVEL 3: MOS3 Empirical Model (SPICE 2G) | MOS3 Empirical Model Parameters | Requires less simulation time, provides as much accuracy as LEVEL 2, and has a greater tendency to converge. |
| LEVEL 2: MOS2 Grove-Frohman (SPICE 2G) Model | MOS3 Empirical Model Parameters | Considers bulk charge effects on current. |
| LEVEL 1: Schichman-Hodges Model | Schichman-Hodges Model Parameters | - |

Common MOSFET Model Parameters

This section covers the following topics:

- [Basic Model Parameters](#)
- [Effective Width and Length Parameters](#)
- [Threshold Voltage Parameters](#)
- [Mobility Parameters](#)

Basic Model Parameters

| Name (Alias) | Units | Default | Description | Level |
|--------------|-------|---------|---|-------|
| LEVEL | | 1.0 | DC model selector: <ul style="list-style-type: none">■ LEVEL=1 (default) is the Schichman-Hodges model.■ LEVEL=2 is the Grove-Frohman model.■ LEVEL=3 is an empirical model.■ LEVEL=4 is a modified version of Level 2.■ LEVEL=5 is the IDS model with enhancement and depletion modes.■ LEVEL=6 is the Lattin-Jenkins-Grove model us using ASPEC-style parasitics.■ LEVEL=7 is the Lattin-Jenkins-Grove model us using SPICE-style parasitics.■ LEVEL=8 is an advanced model using finite differences.■ LEVEL=13 is the University of California (UC) Berkeley BSIM1 model.■ LEVEL=27 is the SOSFET model.■ LEVEL=28 is a Synopsys proprietary model, based on the UC Berkeley BSIM1 model, Level 13.■ LEVEL=38 is the Cypress Depletion model.■ LEVEL=39 is the UC Berkeley BSIM2 model.■ LEVEL=40 is the Hewlett-Packard amorphous-silicon Then-Film Transistor (a-Si TFT) model.■ LEVEL=47 is the UC Berkeley BSIM3 version 2 model■ LEVEL=49 is a Synopsys proprietary model, based on the UC Berkeley BSIM3 version 3 model, Level 53. | All |

Chapter 2: MOSFET Models
Common MOSFET Model Parameters

| Name (Alias) | Units | Default | Description | Level |
|----------------------|-----------------|---------|--|----------|
| LEVEL (continued) | | | <ul style="list-style-type: none"> ■ LEVEL=50 is the Philips MOS9 model. ■ LEVEL=53 is the original UC Berkeley BSIM3 version 3 model, not modified as Level 49 is. ■ LEVEL=54 is the UC Berkeley BSIM4 model ■ LEVEL=55 is the EPFL-EKV model. ■ LEVEL=57 is the UC Berkeley BSIM3-SOI Partially-Depleted (PD) model. ■ LEVEL=58 is the University of Florida SOI model ■ LEVEL=59 is the UC Berkeley BSIM3-SOI Fully-Depleted (FD) model ■ LEVEL=60 is the UC Berkeley BSIM3-SOI Dynamically-Depleted (DD) model ■ LEVEL=61 is the Rensselaer Polytechnic Institute (RPI) a-Si TFT model ■ LEVEL=62 is the Rensselaer Polytechnic Institute (RPI) poly-silicon Thin-Film Transistor (Poli-Si TFT) model ■ LEVEL=63 is the Philips MOS11 model ■ LEVEL=64 is the Hiroshima University Semiconductor Technology Academic Research Center (STARC) IGFET (HiSIM) model. ■ LEVEL=69 is Pennsylvania State University and Philips Research PSP100 model | All |
| ACM | - | 0 | Selects MOS S/D parasitics. ACM=0 is SPICE style. Use ACM=2 or 3 for LDD. | 39 |
| ALPHA | V ⁻¹ | 0 | Impact ionization coefficient. This parameter includes geometry-sensitivity parameters. Choose between BSIM2 (A10>0 and HSPICE (ALPHA>0) impact ionization modeling. <i>Do not use both.</i> | 39 |
| CAPOP | - | * | MOS gate cap model selector: CAPOP=39 for BSIM2 or CAPOP=13 for BSIM1. CAPOP=4 is the same as CAPOP=13. <ul style="list-style-type: none"> ■ If SPICE3=0, default CAPOP=13 ■ If SPICE3=1, default CAPOP=39 | 4, 13 39 |
| CGBO | F/m | - | Gate-to-bulk overlap capacitance. If you specify WD and TOX, but you do not specify CGBO, then simulation calculates CGBO. | 39 |
| CGDO | F | 1.0p | TFT gate-to-drain overlap capacitance. | 40 |
| | F/m | - | Gate-to-drain overlap capacitance. If you specify TOX, and you specify either LD or METO, but you do not specify CGDO, then simulation calculates CGDO. | 39 |
| CGSO | F | 1.0p | TFT gate-to-source overlap capacitance. | 40 |

Chapter 2: MOSFET Models

Common MOSFET Model Parameters

| Name (Alias) | Units | Default | Description | Level |
|--------------|-------------------|----------|---|------------|
| | F/m | - | Gate-to-source overlap capacitance. If you specify TOX, but you do not specify either LD or METO, and you do not specify CGSO, then simulation calculates CGSO. | 39 |
| CHI | | 0.5 | Temperature exponential part. | 40 |
| CJ | F/m ² | 0 | Source/drain bulk zero-bias junction capacitance. | 39 |
| CJSW | F/m | 0 | Sidewall junction capacitance. | 39 |
| CLM (GDS) | | 0.0 | Selects a channel length modulation equation. | 6, 7, 8 |
| COX | F/m ² | 3.453e-4 | Oxide capacitance per unit gate area. If you do not specify COX, simulation calculates it from TOX. | 1, 2, 3, 8 |
| CSC | F/m ² | 10μ | Space charge capacitance. | 40 |
| DEFF | | 2.0 | Drain voltage effect for the TFT leakage current. | 40 |
| DERIV | | 1 | Derivative method selector: <ul style="list-style-type: none"> ■ DERIV=0: analytic ■ DERIV=1: finite difference | 3, 39 |
| DP | μm | 1.0 | Implant depth (depletion model only). | 5, 38 |
| ECRIT (ESAT) | V/cm | 0.0 | Critical electric field for the carrier velocity saturation. From Grove: <ul style="list-style-type: none"> ■ electrons 6e4 ■ holes 2.4e4. Zero indicates an infinite value. The ECRIT equation is more stable than VMAX. Simulation estimates ECRIT as: $\text{ECRIT}=100 * (\text{VMAX} / \text{UO})$ | 2, 8 |
| | V/cm | 0.0 | Drain-source critical field. Zero indicates an infinite value, typically 40,000 V/cm. | 6, 7 |
| ECV | V/μm | 1000 | Critical field. | 5, 38 |
| FEFF | | 0.5 | Frequency effect constant. | 40 |
| FREQ | Hz | 400 | Frequency of the device. | 40 |
| GO | ohm ⁻¹ | 10e-15 | Conductance of the TFT leakage current. | 40 |

Chapter 2: MOSFET Models
Common MOSFET Model Parameters

| Name (Alias) | Units | Default | Description | Level |
|------------------|-------------------------|---------|---|---------|
| IIRAT | - | 0 | Impact ionization source bulk current partitioning factor. One corresponds to 100% source. Zero corresponds to 100% bulk. | 39 |
| JS | A/m ² | 0 | Source/drain bulk diode reverse saturation current density. | 39 |
| K2 | | 2.0 | Temperature exponential part. | 40 |
| KAPPA | V ⁻¹ | 0.2 | Saturation field factor. The channel length modulation equation uses this parameter. | 3 |
| KCS | | 2.77 | Implant capacitance integration constant. | 38 |
| KP (BET, BETA) | A/V ² | | Intrinsic transconductance parameter. If you specify UO and TOX, but you do not specify KP, simulation computes the parameter from: KP=UO * COX ■ Level 1 default=2.0718e-5 (NMOS), 8.632e-6 (PMOS). ■ Level 2, 3 default=2.0e-5 | 1, 2, 3 |
| LAMBDA (LAM, LA) | V ⁻¹ | 0.0 | Channel length modulation. | 2, 8 |
| MJ | - | 0.5 | Source/drain bulk junction grading coefficient. | 39 |
| MJSW | | 0.33 | Sidewall junction grading coefficient. | 39 |
| NEFF | | 1.0 | Total channel charge (fixed and mobile) coefficient. | 2 |
| NI | cm ⁻² | 2e11 | Implant doping (depletion model only). | 5, 38 |
| NU | | 0.0 | First order temperature gradient. | 40 |
| PB | V | 0.8 | Source/drain bulk junction potential. | 39 |
| PBSW | V | PB | Sidewall junction potential. | 39 |
| PSI | | 1e-20 | Temperature exponential part. | 40 |
| RD | ohm | 1.0K | (External) drain resistance. | 40 |
| RS | ohm | 1.0K | (External) source resistance. | 40 |
| RSH | ohm/sq | 0 | Source/drain sheet resistance. | 39 |
| SNVB | 1/(V· cm ³) | 0.0 | Slope of the doping concentration versus vsb (element parameter). (Multiplied by 1e6). | 8 |

Chapter 2: MOSFET Models

Common MOSFET Model Parameters

| Name (Alias) | Units | Default | Description | Level |
|---------------------|-----------------------------|--------------------|--|-------------|
| SPICE3 | - | 0 | Selects SPICE3 model compatibility. For accurate SPICE3 BSIM2, set SPICE3=1. | 39 |
| TAU | s | 10n | Relaxation time constant. | 40 |
| TCV | V/C | 0 | Zero-bias threshold voltage temperature coefficient. The sign of TCV adjusts automatically for NMOS and PMOS to decrease the magnitude of the threshold with rising temperature. | 39 |
| TOX | m | 1e-7 | Gate oxide thickness. | 1, 2, 3, 8 |
| | Å | 0.0 | Oxide thickness. | 5, 38 |
| | m | 7.0e-8 | Oxide thickness. | 27 |
| TRD | 1/K | 0.0 | Temperature coefficient for the Rd drain diffusion and contact resistances. | 54 |
| TREF | | 1.5 | Temperature gradient of UO. | 40 |
| TRS | 1/K | 0.0 | Temperature coefficient for the Rs source diffusion and contact resistances. | 54 |
| TUH | | 1.5 | Implant channel mobility temperature exponent (depletion model only). | 5 |
| UO | cm ² / (V· s) | | Carrier mobility. Default for LEVEL 40 is 1.0. | 1, 40 |
| UO (UB, UBO) | cm ² /(V·s) | 600 (N) 250 (P) | Low-field bulk mobility. Simulation calculates this parameter from the KP value that you specify. | 2 |
| VB0 (VB) | V | 0.0 | Reference voltage for the GAMMA switch. <ul style="list-style-type: none"> ■ If vsb < VB0, the equation uses GAMMA. ■ If vsb > VB0, the equation uses LGAMMA. | 6, 7 |
| VCR | V | 0 | Impact ionization critical voltage. This parameter includes geometry-sensitivity parameters. | 39 |
| VMAX (VMX, VSAT) | m/s | 0.0 | Maximum drift velocity of the carriers. Zero indicates an infinite value. Default VMAX value for Level 40 is 1e6. | 2, 3, 8, 40 |

| Name (Alias) | Units | Default | Description | Level |
|--------------|-------|---------|---|-------|
| VMAX (VMX) | cm/s | 0.0 | Maximum drift velocity of the carriers. Selects a calculation scheme to use for vdsat. Zero indicates an infinite value. Typical values: <ul style="list-style-type: none">■ electrons8.4e6 cm/s■ holes4.3e6 cm/s | 6, 7 |
| VTIME | s | 10m | Voltage stress. | 40 |
| ZENH | | 1.0 | Mode flag (enhancement). Set ZENH=0.0 for the depletion mode. | 5 |

Effective Width and Length Parameters

| Name (Alias) | Units | Default | Description | Level |
|--------------|---------|----------------|---|---|
| DEL | m | 0.0 | Channel length reduction on each side: $DEL_{scaled} = DEL \cdot SCALM$ MOSFET Level 13 does not support DEL. | 1, 2, 3, 6, 7, 8, 38 |
| DEL (WDEL) | μm | 0.0 | Channel length reduction on each side | 5 |
| DELVTO | V | 0 | Threshold voltage shift. This parameter is type sensitive. For example, DELVTO>0 increases the magnitude of the n-channel threshold, decreases the magnitude of the p-channel threshold, and adds to the element-line DELVTO parameter. | 39, 40, 47, 49, 53, 54, 70, |
| LATD (LD) | μm | $1.7 \cdot XJ$ | Lateral diffusion on each side | 5, 38 |
| LDAC | m | | This parameter is the same as LD, but if you specify LDAC in the .MODEL statement, it replaces LD in the Leff calculation for the AC gate capacitance. | 1, 2, 3, 6, 7, 8, 13, 28, 38, 39 |
| LMLT | | 1.0 | Gate length shrink factor. | 1, 2, 3, 5, 6, 7, 8, 13, 28, 38, 39 |
| | | | Scale MOSFET drawn length | 54 |

Chapter 2: MOSFET Models

Common MOSFET Model Parameters

| Name (Alias) | Units | Default | Description | Level |
|--------------------|---------------------------|----------------|---|---|
| LD (DLAT, LATD) | m | | Lateral diffusion into the channel from the source and the drain diffusion. <ul style="list-style-type: none"> ■ If you do not specify LD and XJ: LD Default=0.0 ■ If you specify XJ, but you do not specify LD, simulation calculates LD as: LD default=0.75 · XJ $LD_{scaled}=LD \cdot SCALM$ | 1, 2, 3, 6, 7, 8, 13, 28 |
| LD | m | 0 | Lateral diffusion under the gate (per side) of the S/D junction. Use this parameter to calculate L_{eff} only if DL=0: $LD_{scaled}=LD \cdot SCALM$ | 39 |
| LREF | m | 0.0 | Channel length reference: $LREF_{scaled}=LREF \cdot SCALM$ If the Level 13 model does not define LREF and WREF, their value is infinity. | 2, 3, 6, 7, 8, 13, 28 |
| | m | 0 (∞) | Reference channel length to adjust the length of the BSIM model parameters. For Berkeley compatibility ($LREF \rightarrow \infty$), use: LREF=0. $LREF_{scaled}=LREF \cdot SCALM$ | 39 |
| OXETCH | μm | 0.0 | Oxide etch | 5, 38 |
| Px | $[x] \cdot \mu\text{m}^2$ | 0 | Px is a Synopsys proprietary, WL-product sensitivity parameter, where x is a model parameter with length and width sensitivity. | 39 |
| WD | m | 0.0 | Lateral diffusion into the channel from the bulk along the width: $WD_{scaled}=WD \cdot SCALM$ | 1, 2, 3, 6, 7, 8, 13 |
| | m | 0 | Channel stop lateral diffusion under the gate (per side). Use this parameter to calculate W_{eff} only if DW=0. $WD_{scaled}=WD \cdot SCALM$ | 39 |
| WDAC | m | | This parameter is the same as WD, but if you specify WDAC in the .MODEL statement, it replaces WD in the Weff calculation for the AC gate capacitance. | 1, 2, 3, 6, 7, 8, 13, 28, 39 |
| WMLT | | 1.0 | Diffusion layer and width shrink factor. | 1, 2, 3, 5, 6, 7, 8, 13, 28, 38, 54 |
| | - | 1.0 | Diffusion and gate width shrink factor. | 39 |

Chapter 2: MOSFET Models
Common MOSFET Model Parameters

| Name (Alias) | Units | Default | Description | Level |
|---------------|---------|----------------|--|------------------------------------|
| | | | Scale MOSFET drawn width | 54 |
| WREF | m | 0.0 | Channel width reference: $WREF_{scaled}=WREF \cdot SCALM$ If the Level 13 model does not define LREF and WREF, their value is infinity. | 2, 3, 6, 7, 8, 13, 28 |
| | m | 0 (∞) | Reference device width to adjust the width of the BSIM model parameters. For Berkeley compatibility ($WREF > \infty$), use $WREF=0$: $WREF_{scaled}=WREF \cdot SCALM$ | 39 |
| XJ | m | 0.0 | Metallurgical junction depth: $XJ_{scaled}=XJ \cdot SCALM$ | 1, 2, 3, 6, 7, 8 |
| | μm | 1.5 | Junction depth | 5, 38 |
| XL (DL, LDEL) | m | 0.0 | Length bias accounts for the masking and etching effects (length): $XL_{scaled}=XL \cdot SCALM$ | 1, 2, 3, 6, 7, 8, 13, 28, 39 |
| XL | m | 0 | Difference between the physical (on the wafer) and the drawn reference channel length. Use this parameter to calculate L_{eff} only if DL=0: $XL_{scaled}=XL \cdot SCALM$ Note: SCALM is ignored for Level 54. | 39, 54 |
| XLREF | m | 0.0 | Difference between the physical (on the wafer) and the drawn reference channel length: $XLREF_{scaled}=XLREF \cdot SCALM$ | 28, 39 |
| XW (DW, WDEL) | m | 0.0 | Width bias accounts for the masking and etching effects (width): $XW_{scaled}=XW \cdot SCALM$ | 1, 2, 3, 6, 7, 8, 13, 28 |
| XW | m | 0 | Difference between the physical (on the wafer) and the drawn S/D active width. Use this parameter to calculate W_{eff} only if DW=0: $XW_{scaled}=XW \cdot SCALM$ Note: SCALM is ignored for Level 54. | 39, 54 |
| XWREF | m | 0.0 | Difference between the physical (on the wafer) and the drawn reference channel width: $XWREF_{scaled}=XWREF \cdot SCALM$ | 28, 39 |

Threshold Voltage Parameters

| Name (Alias) | Units | Default | Description | Level |
|--------------|------------------------------------|---------|--|------------|
| BetaGam | | 1.0 | Body effect transition ratio. | 38 |
| CAV | | 0.0 | Thermal voltage multiplier for the weak inversion equation. | 8 |
| DELTA | | 0.0 | Narrow width factor for adjusting the threshold. | 2, 3, 8 |
| DNB (NSUB) | cm ⁻³ | 0.0 | Surface doping density. | 5, 38 |
| | 1/cm ³ | 1.0e15 | Substrate doping. | 6, 7 |
| DNS (NI) | 1/cm ³ | 0.0 | Surface substrate doping. | 6, 7 |
| DVIN | V | 0.0 | Adjusts the empirical surface inversion voltage. | 38 |
| DVSBC | V | 0.0 | Adjusts the empirical body effect transition voltage. | 38 |
| E1 | | 3.9 | Dielectric constant of first film. | 40 |
| E2 | | 0.0 | Dielectric constant of second film. | 40 |
| ETA | V ⁻¹ (Level 40) | 0.0 | Static feedback factor for adjusting the threshold voltage (difficulty of band bending). | 3, 40 |
| | 0.0 | 0.0 | Drain-induced barrier lowering (DIBL) effect coefficient for the threshold voltage. | 8 |
| | 0.0 | 0.0 | Channel-length independent drain-induced barrier lowering. | 38 |
| FDS | | 0.0 | Field, drain to source. Controls the threshold reduction due to the source-drain electric field. | 6, 7 |
| FSS (NFS) | cm ⁻² . V ⁻¹ | 0.0 | Number of fast surface states | 5, 38 |
| GAMMA | V ^{1/2} | 0.5276 | Body effect factor. If you do not specify GAMMA, simulation calculates it from NSUB. | 1, 2, 3, 8 |

| Name (Alias) | Units | Default | Description | Level |
|--------------------|-------------------------------|---------|---|------------------|
| | $V^{1/2}$ | | <p>Body effect factor.</p> <ul style="list-style-type: none"> ▪ If you do not specify GAMMA, simulation calculates it from DNB. ▪ GAMMA is the body effect, if $v_{sb} < V_{B0}$. ▪ If $v_{sb} > V_{B0}$, simulation uses LGAMMA. <p>GAMMA, LGAMMA, and VB0 perform a two-step approximation of a non-homogeneous substrate.</p> | 6, 7 |
| LBetaGam. | μm | 0.0 | BetaGam dependence on the channel length. | 38 |
| LDVSBC | $V \cdot \mu\text{m}$ | 0.0 | Adjusts the L-dependent body effect transition voltage. | 38 |
| LETA(DIBL) | μm | 0.0 | Channel-length dependent drain-induced barrier lowering. | 38 |
| LGAMMA | $V^{1/2}$ | 0.0 | This parameter is the body effect factor if $v_{sb} > V_{B0}$. | 6, 7 |
| | | | If you use the Poon-Yau GAMMA expression, LGAMMA is the junction depth in microns. Simulation multiplies LGAMMA by SCALM. | |
| LND | $\mu\text{m}/V$ | 0.0 | ND length sensitivity. | 2, 3, 6, 7, 8 |
| LN0 | μm | 0.0 | N0 length sensitivity. | 2, 3, 6, 7, 8 |
| LVT (LVTO) | $V \cdot \mu\text{m}$ | 0.0 | VT dependence on the channel length. | 38 |
| ND | V^{-1} (1/V) | 0.0 | Drain subthreshold factor. Typical value=1. | 2, 3, 6, 7, 8 |
| N0 | | 0.0 | Gate subthreshold factor. Typical value=1. | 2, 3, 6, 7, 8 |
| NFS (DFS, NF, DNF) | $\text{cm}^{-2} \cdot V^{-1}$ | 0.0 | Fast surface state density. | 1, 2, 3, 6, 7, 8 |
| NFS | cm^2 | 0.0 | Fast surface state density. | 40 |
| NSS | cm^2 | 0.0 | Surface state density. | 40 |
| NSUB (DNB, NB) | cm^{-3} | 1e15 | Bulk surface doping. If you do not specify NSUB, simulation calculates it from GAMMA. | 1, 2, 3, 8 |

Chapter 2: MOSFET Models

Common MOSFET Model Parameters

| Name (Alias) | Units | Default | Description | Level |
|--------------|-------|---------|--|----------------------|
| NWE | m | 0.0 | Narrow width effect, direct compensation of VTO: $NWE_{scaled} = NWE \cdot SCALM$ | 6, 7 |
| NWM | | 0.0 | Narrow width modifier. | 5, 38 |
| | | 0.0 | Narrow width modulation of GAMMA. | 6, 7 |
| PHI | V | 0.576 | Surface inversion potential. If you do not specify PHI, HSPICE calculates it from NSUB. | 1, 2, 3, 8 |
| | | 0.8 | Built-in potential. | 5, 38 |
| | | 0.0 | Surface potential. | 40 |
| SCM | | 0.0 | Short-channel drain source voltage multiplier | 5, 38 |
| | | 0.0 | Short-channel modulation of GAMMA. | 6, 7 |
| T1 | m | 280n | First thin film thickness. | 40 |
| T2 | m | 0.0 | Second thin film thickness. | 40 |
| TDVSBC | V/K | 0.0 | Body effect transition voltage shift due to the temperature. | 38 |
| UFDS | | 0.0 | High field FDS. | 6, 7 |
| UPDATE | | 0.0 | Selects different versions of the LEVEL 6 model. For the UPDATE=1 or 2 alternate saturation voltage, simulation modifies the MOB=3 mobility equation and the RS and RD series resistances so they are compatible with ASPEC. UPDATE=1 is a continuous Multi-Level GAMMA model. | 6, 7 |
| VFDS | V | 0.0 | Reference voltage for selecting FDS or UFDS: <ul style="list-style-type: none"> ▪ Uses FDS if $vds \leq VFDS$. ▪ Uses UFDS if $vds > VFDS$. | 6, 7 |
| VSH | V | 0.0 | Threshold voltage shifter for reducing the zero-bias threshold voltage (VTO) as a function of the ratio of LD to Leff. | 6, 7 |
| VT (VTO) | V | 0.0 | Extrapolated threshold voltage | 5, 38 |
| VTO (VT) | V | 0.0 | Zero-bias threshold voltage. If you do not specify VTO, simulation calculates it. | 1, 2, 3, 6, 7, 8, 40 |

| Name (Alias) | Units | Default | Description | Level |
|--------------|-------|---------|---|---------------|
| WBetaGam | μm | 0.0 | BetaGam dependence on the channel width. | 38 |
| WDVSBC | V· μm | 0.0 | Adjusts the W-dependent body effect transition voltage. | 38 |
| WETA | μm | 0.0 | Channel-width dependent drain-induced barrier lowering. | 38 |
| WEX | | | Weak inversion exponent. | 6, 7 |
| WIC | | 0.0 | Subthreshold model selector. | 2, 3, 6, 7, 8 |
| WND | μm/V | 0.0 | ND width sensitivity. | 2, 3, 6, 7, 8 |
| WN0 | μm | 0.0 | N0 width sensitivity. | 2, 3, 6, 7 |
| WVT (WVTO) | V· μm | 0.0 | VT dependence on the channel width. | 38 |

Mobility Parameters

Use curve fitting to determine the mobility parameters. Generally, you should set UTRA between 0.0 and 0.5. Nonzero values for UTRA can result in negative resistance regions at the onset of saturation.

| Name (Alias) | Units | Default | Description | Level |
|-----------------|----------------------------|---------|--|--------|
| BEX | - | -1.5 | Surface channel mobility temperature exponent. | 38, 39 |
| BFRC | Å· s/(cm ² · V) | 0.0 | Field reduction coefficient variation due to the substrate bias. | 38 |
| FACTOR | | | Mobility degradation factor. Default=1.0. | 6, 7 |
| FEX | - | 0 | Temperature exponent for velocity saturation. | 39 |
| FRC | Å· s/cm ² | 0.0 | Field reduction coefficient. | 5, 38 |
| FRCEX (F1EX) | | 0.0 | Temperature coefficient for FRC | 38 |

Chapter 2: MOSFET Models

Common MOSFET Model Parameters

| Name (Alias) | Units | Default | Description | Level |
|-------------------|---|---------|---|------------|
| FSB | $V^{1/2} \cdot s/cm^2$ | 0.0 | Lateral mobility coefficient. | 5, 38 |
| HEX(TUH) | | -1.5 | Implant channel mobility temperature exponent. | 38 |
| KBeta1 | | 1.0 | Effective implant-channel mobility modifier. | 38 |
| KI0(KIO) | | 1.0 | Residue current coefficient. | 38 |
| LBFR _C | $10^{-4} \text{\AA} \cdot s/(cm \cdot V)$ | 0.0 | BFRC sensitivity to the effective channel length. | 38 |
| LFRC | $10^{-4} \text{\AA} \cdot s/cm$ | 0.0 | FRC sensitivity to the effective channel length. | 38 |
| LKBeta1 | μm | 0.0 | Length-dependent implant-channel mobility modifier. | 38 |
| LKI0(LKIO) | μm | 0.0 | Length-dependent residue current coefficient. | 38 |
| LUO(LUB) | $cm^2 \cdot \mu m/(V \cdot s)$ | 0.0 | UO sensitivity to the effective channel length. | 38 |
| LVFRC | $10^{-4} \text{\AA} \cdot s/(cm \cdot V)$ | 0.0 | VFRC sensitivity to the effective channel length. | 38 |
| LFSB | $10^{-4} V^{1/2} \cdot s/cm$ | 0.0 | FSB sensitivity to the effective channel length. | 38 |
| MOB | | 0.0 | Selects a mobility equation. You can set this parameter to MOB=0 or MOB=7. MOB=7 changes both the model and the channel length calculation. The MOB=7 flag invokes the channel length modulation and mobility equations in MOSFET LEVEL 3. | 2, 6, 7, 8 |
| | | | In MOSFET Level 8, you can set MOB to 2, 3, 6, or 7. | |
| THETA | V^{-1} | 0.0 | Mobility modulation. MOSFET models use THETA only if MOB=7. A typical value is THETA=5e-2. | 2, 40 |
| | V^{-1} | 0.0 | Mobility degradation factor. | 3 |

Chapter 2: MOSFET Models
Common MOSFET Model Parameters

| Name (Alias) | Units | Default | Description | Level |
|--------------|-------------------------------|---------------------|---|----------------------|
| UB (UO) | cm ² /(V· s) | 0.0 | Low field bulk mobility | 5 |
| UCRIT | V/cm | 1.0e4 | Critical field for mobility degradation, UCRIT. This parameter is the limit where UO surface mobility begins to decrease as specified in the empirical relation. | 2 |
| | V/cm | 1e4 | <ul style="list-style-type: none"> ■ MOB=6, UEXP>0 Critical field for the mobility degradation. UEXP operates as a switch. ■ MOB=6, UEXP<0 Critical field for mobility degradation. Typical value is 0.01 V⁻¹. | 8 |
| UEFF | | | Effective mobility at the specified analysis temperature. | 6, 7 |
| UEXP (F2) | | 0.0 | Critical field exponent in the empirical formula that characterizes the surface mobility degradation. | 2, 8 |
| | | | Typical value in MOSFET Level 8 with MOB=6 is 0.01 V ⁻¹ . | |
| UH | cm ² /(V· s) | 900 (N) 300 (P)* | Implant - channel mobility *(For depletion model only) | 5, 38 |
| UHSAT | μm/V | 0.0 | Implant-channel mobility saturation factor. | 38 |
| UO (UB, UBO) | cm ² /(V·s) | 600 (N) 250 (P) | Low-field bulk mobility. Simulation calculates this parameter from the KP value that you specify. | 2, 3, 6, 7, 8, 38 |
| UTRA | | 0.0 | Transverse field coefficient (mobility). | 2, 8 |
| | | | Traditional SPICE does not use UTRA. HSPICE can use UTRA, but simulation issues a warning, because UTRA can hinder convergence. | |
| VFRC | Å· s/(cm ² · V) | 0.0 | Field reduction coefficient variation due to the drain bias. | 38 |
| VST | cm/s | 0.0 | Saturation velocity. | 5, 38 |
| WBFRC | 10 ⁻⁴ Å· s/(cm· V) | 0.0 | BFRFC sensitivity to the effective channel width. | 38 |

Chapter 2: MOSFET Models

Common MOSFET Model Parameters

| Name (Alias) | Units | Default | Description | Level |
|----------------|--|---------|--|-------|
| WFRC | $10^{-4} \text{Å} \cdot \text{s/cm}$ | 0.0 | FRC sensitivity to the effective channel width. | 38 |
| WFSB | $10^{-4} \text{V}^{1/2} \cdot \text{s/cm}$ | 0.0 | FSB sensitivity to the effective channel width. | 38 |
| WKBeta1 | μm | 0.0 | Width-dependent implant-channel mobility modifier. | 38 |
| WKIO (WKIO) | μm | 0.0 | Width-dependent residue current coefficient. | 38 |
| WUO(WUB) | $\text{cm}^2 \cdot \mu\text{m}/(\text{V} \cdot \text{s})$ | 0.0 | UO sensitivity to the effective channel width. | 38 |
| WVFRC | $10^{-4} \text{Å} \cdot \text{s}/(\text{cm} \cdot \text{V})$ | 0.0 | VFRC sensitivity to the effective channel width. | 38 |

LEVEL 1: Schichman-Hodges Model

Use this model if accuracy is less important to you than simulation turn-around time. For digital switching circuits, especially if you need only a “qualitative” simulation of the timing and the function, LEVEL 1 run-time can be about half that of a simulation using the LEVEL 2 model. The agreement in timing is approximately 10%. The LEVEL 1 model, however, results in severe inaccuracies in DC transfer functions of any TTL-compatible input buffers in the circuit.

The `LAMBDA` channel-length modulation parameter is equivalent to the inverse of the Early voltage for the bipolar transistor. `LAMBDA` measures the output conductance in the saturation. If you specify this parameter, the MOSFET has a finite but constant output conductance in saturation. If you do not specify `LAMBDA`, the LEVEL 1 model assumes zero output conductance.

This section covers the following topics:

- [Schichman-Hodges Model Parameters](#)
 - [Schichman-Hodges Model Equations](#)
-

Schichman-Hodges Model Parameters

MOSFET Level 1 uses only the generic MOSFET model parameters described in [Common MOSFET Model Parameters](#) section.

Schichman-Hodges Model Equations

This section covers the following topics:

- [Schichman-Hodges Model — IDS Equations](#)
- [Schichman-Hodges Model — Effective Channel Length and Width](#)

Schichman-Hodges Model — IDS Equations

The LEVEL 1 model does not include the carrier mobility degradation, the carrier saturation effect, or the weak inversion model. This model determines the DC current:

Cutoff Region,

Chapter 2: MOSFET Models

LEVEL 1: Schichman-Hodges Model

$$v_{gs} \leq v_{th} , I_{ds} = 0.0$$

Linear Region, $v_{ds} < v_{gs} - v_{th}$

$$I_{ds} = KP \cdot \frac{W_{eff}}{L_{eff}} \cdot (1 + LAMBDA \cdot v_{ds}) \cdot \left(v_{gs} - v_{th} - \frac{v_{ds}}{2} \right) \cdot v_{ds}$$

Saturation Region, $v_{ds} \geq v_{gs} - v_{th}$

$$I_{ds} = \frac{KP}{2} \cdot \frac{W_{eff}}{L_{eff}} \cdot (1 + LAMBDA \cdot v_{ds}) \cdot (v_{gs} - v_{th})^2$$

Schichman-Hodges Model — Effective Channel Length and Width

The Level 1 model calculates the effective channel length and width from the drawn length and width:

$$L_{eff} = L_{scaled} \cdot LMLT + XL_{scaled} - 2(LD_{scaled} + DEL_{scaled})$$

$$W_{eff} = M \cdot (W_{scaled} WMLT + XW_{scaled} - 2WD_{scaled})$$

Threshold Voltage, v_{th}

$$v_{sb} \geq 0 , v_{th} = v_{bi} + GAMMA \cdot (PHI + v_{sb})^{1/2}$$

$$v_{sb} < 0, v_{th} = v_{bi} + GAMMA \cdot \left(PHI^{1/2} + 0.5 \frac{v_{sb}}{PHI^{1/2}} \right)$$

The preceding equations define the built-in voltage (v_{bi}) as:

$$v_{bi} = v_{fb} + PHI, v_{bi} = VTO - GAMMAPHI^{1/2}$$

See [Common Threshold Voltage Equations](#) for calculation of VTO, GAMMA, and PHI if you do not specify them.

Saturation Voltage, v_{sat}

The saturation voltage for the LEVEL 1 model is due to the channel pinch-off at the drain side. The following equation computes this voltage:

$$v_{sat} = v_{gs} - v_{th}$$

The LEVEL 1 model does not include the carrier velocity saturation effect.

LEVEL 2: MOS2 Grove-Frohman (SPICE 2G) Model

This section describes the parameters and equations for the LEVEL 2: MOS2 Grove-Frohman model:

- [Grove-Frohman \(SPICE 2G\) Model Parameters](#)
 - [Grove-Frohman \(SPICE 2G\) Model Equations](#)
-

Grove-Frohman (SPICE 2G) Model Parameters

This model uses only the generic MOSFET model parameters described in [Common MOSFET Model Parameters](#) section.

Grove-Frohman (SPICE 2G) Model Equations

This section covers the following topics:

- [Grove-Frohman \(SPICE 2G\) Model — IDS Equations](#)
- [Grove-Frohman \(SPICE 2G\) Model — Effective Channel Length and Width](#)
- [Grove-Frohman \(SPICE 2G\) Model — Threshold Voltage, \$v_{th}\$](#)
- [Grove-Frohman \(SPICE 2G\) Model — Saturation Voltage, \$v_{dsat}\$](#)
- [Grove-Frohman \(SPICE 2G\) Model — Mobility Reduction, \$u_{eff}\$](#)
- [Grove-Frohman \(SPICE 2G\) Model — Channel Length Modulation](#)
- [Grove-Frohman \(SPICE 2G\) Model — Subthreshold Current, \$I_{ds}\$](#)

Grove-Frohman (SPICE 2G) Model — IDS Equations

This section describes how this model calculates the drain current of n-channel and p-channel MOSFETs.

Cutoff Region, $v_{gs} \leq v_{th}$, $I_{ds} = 0$ (see subthreshold current)

On Region, $v_{gs} > v_{th}$

$$I_{ds} = \beta \cdot \left\{ \left(v_{gs} - v_{bi} - \frac{\eta \cdot v_{de}}{2} \right) \cdot v_{de} - \frac{2}{3} \gamma [(\Phi_l + v_{de} + v_{sb})^{3/2} - (\Phi_l + v_{sb})^{3/2}] \right\}$$

The following equations calculate values used in the preceding equation:

Chapter 2: MOSFET Models

LEVEL 2: MOS2 Grove-Frohman (SPICE 2G) Model

$$v_{de} = \min(v_{ds}, v_{dsat})$$

$$\eta = 1 + \text{DELTA} \cdot \frac{\pi \cdot \epsilon s i}{4 \cdot COX \cdot W_{eff}}, \beta = KP \cdot \frac{W_{eff}}{L_{eff}}$$

Grove-Frohman (SPICE 2G) Model — Effective Channel Length and Width

The Level 2 model calculates effective channel length and width from the drawn length and width:

$$L_{eff} = L_{scaled} \cdot LMLT + XL_{scaled} - 2(LD_{scaled} + DEL_{scaled})$$

$$W_{eff} = M \cdot (W_{scaled} \cdot WMLT + XW_{scaled} - 2WD_{scaled})$$

$$LREF_{eff} = LREF_{scaled} \cdot LMLT + XL_{scaled} - 2(LD_{scaled} + DEL_{scaled})$$

$$WREF_{eff} = M \cdot (WREF_{scaled} \cdot WMLT + XW_{scaled} - 2WD_{scaled})$$

Grove-Frohman (SPICE 2G) Model — Threshold Voltage, v_{th}

The VTO model parameter is an extrapolated zero-bias threshold voltage for a large device. The following equation calculates the effective threshold voltage, including the device size effects and the terminal voltages:

$$v_{th} = v_{bi} + \gamma \cdot (PHI + v_{sb})^{1/2}$$

The following equation calculates the v_{bi} value used in the preceding equation:

$$v_{bi} = VTO - GAMMA(PHI)^{1/2} + (\eta - 1) \cdot (PHI + v_{sb})$$

To include the narrow width effect, use v_{bi} and η . To include the narrow width effect, specify the DELTA model parameter. The effective γ specifies the short-channel effect. To include short-channel effects, the XJ model parameter must be greater than zero.

$$\gamma = GAMMA \cdot \left\{ 1 - \frac{XJ_{scaled}}{2 \cdot L_{eff}} \left[\left(1 + \frac{2 \cdot W_s}{XJ_{scaled}} \right)^{1/2} + \left(1 + \frac{2 \cdot W_d}{XJ_{scaled}} \right)^{1/2} - 2 \right] \right\}$$

The following equations determine the W_s and W_d depletion widths:

$$W_s = \left[\frac{2 \cdot E_{si}}{q \cdot NSUB} \cdot (PHI + v_{sb}) \right]^{1/2}$$

$$W_d = \left[\frac{2 \cdot E_{si}}{q \cdot NSUB} \cdot (PHI + v_{ds} + v_{sb}) \right]^{1/2}$$

If you do not specify parameters such as VTO, GAMMA, and PHI, simulation calculates them automatically. The Level 2 model uses these parameters to calculate the threshold voltage. (See [Common Threshold Voltage Equations](#)).

Grove-Frohman (SPICE 2G) Model — Saturation Voltage, v_{dsat}

If you do not specify the VMAX model parameter, the program computes the saturation voltage due to channel pinch off at the drain side. If you specify the corrections for small-size effects, then:

$$v_{sat} = \frac{v_{gs} - v_{bi}}{\eta} + \frac{1}{2} \left(\frac{\gamma}{\eta} \right)^2 \cdot \left\{ 1 - \left[1 + 4 \cdot \left(\frac{\eta}{\gamma} \right)^2 \cdot \left(\frac{v_{gs} - v_{bi}}{\eta} + PHI + v_{sb} \right) \right]^{1/2} \right\}$$

$$v_{dsat} = v_{sat}$$

If you specify ECRIT, the program modifies v_{sat} to include carrier velocity saturation effect:

$$v_{dsat} = v_{sat} + v_c - (v_{sat}^2 + v_c^2)^{1/2}$$

The following equation calculates the v_c value used in the preceding equation:

$$v_c = ECRIT \cdot L_{eff}$$

Note: If you specify VMAX, simulation calculates a different v_{dsat} value. Refer to the Vladimirescu document[\[1\]](#) for details.

Grove-Frohman (SPICE 2G) Model — Mobility Reduction, u_{eff}

The mobility of carriers in the channel decreases as speeds of the carriers approach their scattering limited velocity. The mobility degradation for the LEVEL 2 MOS model uses two different equations, depending on the MOB mobility equation selector value.

If MOB=0, (default):

$$u_{eff} = UO \cdot \left[\frac{UCRIT \cdot E_{si}}{COX \cdot (v_{gs} - v_{th} - UTRA Pv_{ds})} \right]^{UEXP}$$

Because u_{eff} is less than UO , the program uses the above equation if the bracket term is less than one; otherwise the program uses $u_{eff}=UO$.

Chapter 2: MOSFET Models

LEVEL 2: MOS2 Grove-Frohman (SPICE 2G) Model

If MOB=7, THETA ≠ 0

$$u_{eff} = \frac{UO}{1 + THETA \cdot (v_{gs} - v_{th})}$$

$v_{gs} < v_{th}$, $u_{eff} = UO$

If MOB=7, THETA=0

$$u_{eff} = UO \cdot \left[\frac{UCRIT \cdot E_{si}}{COX \cdot (v_{gs} - v_{th})} \right]^{UEXP}$$

If MOB=7, VMAX>0

$$u_{eff} = \frac{u_{eff}}{1 + u_{eff} \cdot \frac{v_{de}}{VMAX \cdot L_{eff}}}$$

Grove-Frohman (SPICE 2G) Model — Channel Length Modulation

To include the channel length modulation effect, the LEVEL 2 MOS model modifies the I_{ds} current:

$$I_{ds} = \frac{I_{ds}}{1 - \lambda P v_{ds}}$$

If you do not specify the LAMBDA model parameter, the model calculates the λ value.

LAMBDA>0:

$\lambda = \text{LAMBDA}$

$VMAX > 0$, $NSUB > 0$, and $\text{LAMBDA} < 0$

$$\lambda = \frac{X_d}{NEFF^{1/2} \cdot L_{eff} \cdot v_{ds}} \cdot \left\{ \left[\left(\frac{VMAX \cdot X_d}{2 \cdot NEFF^{1/2} \cdot u_{eff}} \right)^2 + v_{ds} - v_{dsat} \right]^{1/2} - \frac{VMAX \cdot X_d}{2 \cdot NEFF^{1/2} \cdot u_{eff}} \right\}$$

$VMAX = 0$, $NSUB > 0$, and $\text{LAMBDA} < 0$

If MOB=0

$$\lambda = \frac{X_d}{L_{eff} \cdot v_{ds}} \cdot \left\{ \frac{v_{ds} - v_{dsat}}{4} + \left[1 + \left(\frac{v_{ds} - v_{dsat}}{4} \right)^2 \right]^{1/2} \right\}^{1/2}$$

This equation does not include the effect of the field between the gate and the drain. It also tends to overestimate the output conductance in the saturation region.

If MOB=7

$$\lambda = \frac{X_d}{L_{eff} \cdot v_{ds}} \cdot \left\{ \left[\frac{v_{ds} - v_{dsat}}{4} + \left(1 + \left(\frac{v_{ds} - v_{dsat}}{4} \right)^2 \right)^{1/2} \right]^{1/2} - 1 \right\}$$

This equation does not include the effect of the field between the gate and the pinch-off point. It also tends to overestimate the output conductance in the saturation region.

The following equation calculates the X_d value used in the two preceding equations:

$$X_d = \left(\frac{2 \cdot E_{si}}{q \cdot NSUB} \right)^{1/2}$$

Modifying I_{ds} by a factor of $(1 - \lambda \cdot v_{ds})$ is equivalent to replacing L_{eff} with:

$$Le = L_{eff} - \lambda_{ds} \cdot L_{eff}$$

To prevent the channel length (Le) from becoming negative, the value of Le is limited.

If $Le < xwb$, then simulation replaces Le with:

$$\frac{xwb}{1 + \frac{xwb - Le}{xwb}}$$

The following equation calculates the xwb value used in the preceding equation:

$$xwb = X_d \cdot PB^{1/2}$$

Grove-Frohman (SPICE 2G) Model — Subthreshold Current, I_{ds}

The fast surface states model parameter (NFS) characterizes this region of operation. For $NFS > 0$ the model determines the modified threshold voltage (v_{on}):

Chapter 2: MOSFET Models

LEVEL 2: MOS2 Grove-Frohman (SPICE 2G) Model

$$v_{on} = v_{th} + fast$$

The following equation calculates the fast value used in the preceding equation:

$$fast = vt \cdot \left[\eta + (PHI + v_{sb})^{1/2} \cdot \frac{\partial \gamma}{\partial v_{sb}} + \frac{\gamma}{2 \cdot (PHI + v_{sb})^{1/2}} + \frac{q \cdot NFS}{COX} \right]$$

In the preceding equations, vt is the thermal voltage.

The following equation calculates the I_{ds} current for $v_{gs} < v_{on}$:

$$I_{ds} = I_{ds}(v_{on}, v_{de}, v_{sb}) \cdot e^{\frac{v_{gs} - v_{on}}{fast}}$$

$v_{gs} > v_{on}$:

$$I_{ds} = I_{ds}(v_{gs}, v_{de}, v_{sb})$$

The following equation calculates the v_{de} value used in the preceding equation:

$$v_{de} = \min(v_{ds}, v_{dsat})$$

Note: The modified threshold voltage (v_{on}), due to NFS specification, is also used in strong inversion instead of v_{th} , mostly in the mobility equations.

If WIC=3, the Level 2 model calculates the subthreshold current differently. In this case the I_{ds} current is:

$$I_{ds} = I_{ds}(v_{gs}, v_{de}, v_{sb}) + isub(N0_{eff}, ND_{eff}, v_{gs}, v_{ds})$$

$N0_{eff}$ and ND_{eff} are functions of effective device width and length.

LEVEL 3: MOS3 Empirical Model (SPICE 2G)

This section describes the LEVEL 3 IDS: MOS3 Empirical model parameters and equations.

- [MOS3 Empirical Model Parameters](#)
 - [MOS3 Empirical Model Equations](#)
 - [MOS3 Empirical Model — Compatibility Notes](#)
 - [MOS3 Empirical Model — Temperature Compensation Example](#)
-

MOS3 Empirical Model Parameters

This model uses only the generic MOSFET model parameters described in [Common MOSFET Model Parameters](#) section.

MOS3 Empirical Model Equations

This section covers the following topics:

- [MOS3 Empirical Model — IDS Equations](#)
- [MOS3 Empirical Model — Effective Channel Length and Width](#)
- [MOS3 Empirical Model — Threshold Voltage, \$v_{th}\$](#)
- [MOS3 Empirical Model — Saturation Voltage, \$v_{dsat}\$](#)
- [MOS3 Empirical Model — Effective Mobility, \$u_{eff}\$](#)
- [MOS3 Empirical Model — Channel Length Modulation](#)
- [MOS3 Empirical Model — Subthreshold Current, \$I_{ds}\$](#)

MOS3 Empirical Model — IDS Equations

The following equations describe how this model calculates the I_{ds} drain current.

Cutoff Region, $v_{gs} < v_{th}$

$I_{ds} = 0$ (See subthreshold current)

On Region, $v_{gs} > v_{th}$

Chapter 2: MOSFET Models

LEVEL 3: MOS3 Empirical Model (SPICE 2G)

$$I_{ds} = \beta \cdot \left(V_{gs} - V_{th} - \frac{1+fb}{2} \cdot vde \right) \cdot vde$$

The following equations calculate values used in the preceding equation:

$$\beta = K \cdot P \cdot \frac{W_{eff}}{L_{eff}} = u_{eff} \cdot COX \cdot \frac{W_{eff}}{L_{eff}}$$

Since

$$K \cdot P = u_{eff} \cdot COX$$

$$vde = \min(v_{ds}, v_{dsat})$$

$$fb = f_n + \frac{GAMMA \cdot f_s}{4 \cdot (PHI + v_{sb})^{1/2}}$$

Note: In the above equation, the factor 4 should be 2, but because SPICE uses a factor of 4, this model uses a factor of 4 as well.

The f_n parameter specifies the narrow width effect:

$$f_n = \frac{DELTA}{W_{eff}} \cdot \frac{1}{4} \cdot \frac{2\pi \cdot E_{si}}{COX}$$

The f_s term expresses the effect of the short channel:

$$f_s = 1 - \frac{XJ_{scaled}}{L_{eff}} \left\{ \frac{LD_{scaled} + W_c}{XJ_{scaled}} \cdot \left[1 - \left(\frac{W_p}{XJ_{scaled} + W_p} \right)^2 \right]^{1/2} - \frac{LD_{scaled}}{XJ_{scaled}} \right\}$$

$$W_p = X_d \cdot (PHI + v_{sb})^{1/2}$$

$$X_d = \left(\frac{2 \cdot E_{si}}{q \cdot NSUB} \right)^{1/2}$$

$$W_c = XJ_{scaled} \cdot \left[0.0631353 + 0.8013292 \cdot \left(\frac{W_p}{XJ_{scaled}} \right) - 0.01110777 \left(\frac{W_p}{XJ_{scaled}} \right)^2 \right]$$

MOS3 Empirical Model — Effective Channel Length and Width

The following equations determine the effective channel length and width in the LEVEL 3 model:

$$L_{eff} = L_{scaled} \cdot LMLT + XL_{scaled} - 2(LD_{scaled} + DEL_{scaled})$$

$$W_{eff} = M \cdot (W_{scaled} \cdot WMLT + XW_{scaled} - 2WD_{scaled})$$

$$LREF = LREF_{scaled} \cdot LMLT + XL_{scaled} - 2(LD_{scaled} + DEL_{scaled})$$

$$WREF_{eff} = M \cdot (WREF_{scaled} \cdot WMLT + XW_{scaled} - 2WD_{scaled})$$

MOS3 Empirical Model — Threshold Voltage, v_{th}

The following equation calculates the effective threshold voltage, including the device size and terminal voltage effects:

$$v_{th} = v_{bi} - \frac{8.14e-22ETA}{COX \cdot L_{eff}^3} \Rightarrow v_{ds} + GAMMA \cdot f_s \cdot (PHI + v_{sb})^{1/2} + f_n \cdot (PHI + v_{sb})$$

The following equation calculates the v_{bi} value used in the preceding equation:

$$v_{bi} = v_{fb} + PHI \text{ or } v_{bi} = VTO - GAMMAPHI^{1/2}$$

VTO is the extrapolated zero-bias threshold voltage of a large device. If you do not specify VTO , $GAMMA$, or PHI , simulation computes these values (see [Common Threshold Voltage Equations](#)).

MOS3 Empirical Model — Saturation Voltage, v_{dsat}

The LEVEL 3 model determines the saturation voltage due to the channel pinch-off at the drain side. The $VMAX$ parameter specifies the reduction of the saturation voltage due to the carrier velocity saturation effect.

$$v_{sat} = \frac{v_{gs} - v_{th}}{1 + f_b}$$

$$v_{dsat} = v_{sat} + v_c - (v_{sat}^2 + v_c^2)^{1/2}$$

The following equation calculates the v_c value used in the preceding equations:

$$v_c = \frac{VMAX \cdot L_{eff}}{us}$$

The next section defines the us surface mobility parameter. If you do not specify the $VMAX$ model parameter, then:

$$v_{dsat} = v_{sat}$$

Chapter 2: MOSFET Models

LEVEL 3: MOS3 Empirical Model (SPICE 2G)

MOS3 Empirical Model — Effective Mobility, u_{eff}

The Level 3 model defines the carrier mobility reduction due to the normal field as the effective surface mobility (u_s).

$v_{gs} > v_{th}$

$$u_s = \frac{UO}{1 + THETA \cdot (v_{gs} - v_{th})}$$

The VMAX model parameter determines the degradation of mobility due to the lateral field and the carrier velocity saturation.

VMAX>0:

$$u_{eff} = \frac{u_s}{1 + \frac{v_{de}}{v_c}}$$

Otherwise, $u_{eff} = u_s$

MOS3 Empirical Model — Channel Length Modulation

For $v_{ds} > v_{dsat}$, this model computes the channel length modulation factor. The VMAX model parameter value determines the amount of channel length reduction (ΔL).

VMAX=0

$$\Delta L = X_d \cdot [KAPPA \cdot (v_{ds} - v_{dsat})]^{1/2}$$

VMAX>0

$$\Delta L = -\frac{E_p \cdot X_d^2}{2} + \left[\left(\frac{E_p \cdot X_d^2}{2} \right)^2 + KAPPA \cdot X_d^2 \cdot (v_{ds} - v_{dsat}) \right]^{1/2}$$

In the preceding equation, E_p is the lateral electric field at the pinch off point. The following equation approximates its value:

$$E_p = \frac{v_c \cdot (v_c + v_{dsat})}{L_{eff} \cdot v_{dsat}}$$

The LEVEL 3 model modifies the I_{ds} current to include the channel length modulation effect:

$$I_{ds} = \frac{I_{ds}}{1 - \frac{\Delta L}{L_{eff}}}$$

To prevent a zero denominator, the ΔL value is limited:

$$\text{If } \Delta L > \frac{L_{eff}}{2} \text{ then } \Delta L = L_{eff} - \frac{\left(\frac{L_{eff}}{2}\right)^2}{\Delta L}$$

MOS3 Empirical Model — Subthreshold Current, I_{ds}

This region of operation is characterized by the model parameter for the fast surface state (NFS). The following equation determines the modified threshold voltage (v_{on}):

$$NFS > 0 \quad v_{on} = v_{th} + fast$$

The following equation calculates the fast value used in the preceding equation:

$$fast = v_{tm} \cdot \left[1 + \frac{q \cdot NFS}{COX} + \frac{GAMMA \cdot f_s \cdot (PHI + v_{sb})^{1/2} + f_n \cdot (PHI + v_{sb})}{2 \cdot (PHI + v_{sb})} \right]$$

The following equations calculate the I_{ds} current:

$v_{gs} < v_{on}$:

$$I_{ds} = I_{ds}(v_{on}, v_{de}, v_{sb}) \cdot e^{\frac{v_{gs} - v_{on}}{fast}}$$

$v_{gs} > v_{on}$:

$$I_{ds} = I_{ds}(v_{gs}, v_{de}, v_{sb})$$

Note: Strong inversion does not use the modified threshold voltage.

If WIC=3, the model calculates subthreshold current differently. In this case, the I_{ds} current is:

$$I_{ds} = I_{ds}(v_{gs}, v_{de}, v_{sb}) + isub(N0_{eff}, ND_{eff}, v_{gs}, v_{ds})$$

The isub subthreshold current for LEVEL=3 is the same as for LEVEL=13 (see [BSIM Model — ids Subthreshold Current](#)).

$N0_{eff}$ and ND_{eff} are functions of the effective device width and length.

MOS3 Empirical Model — Compatibility Notes

Differences between the Synopsys Level 3 MOSFET device model and Berkeley SPICE3 can arise in the following situations:

This section covers the following topics:

- [MOS3 Empirical Model — Compatibility Notes: Small XJ](#)
- [MOS3 Empirical Model — Compatibility Notes: ETA](#)
- [MOS3 Empirical Model — Compatibility Notes: NSUB Missing](#)
- [MOS3 Empirical Model — Compatibility Notes: LD Missing](#)
- [MOS3 Empirical Model — Compatibility Notes: KP Given and U0 Not Given](#)

MOS3 Empirical Model — Compatibility Notes: Small XJ

LEVEL 3 and SPICE3 differ for small X_J values, typically >0.05 microns. Do not use such small values for X_J ; they are physically unreasonable. X_J calculates the short-channel reduction of the GAMMA effect:

$$GAMMA \rightarrow f_s \cdot GAMMA$$

f_s is normally less than or equal to 1. For very small values of X_J , f_s can be greater than one. The Synopsys Level 3 model imposes the limit $f_s \leq 1.0$, but SPICE3 allows $f_s > 1.0$.

MOS3 Empirical Model — Compatibility Notes: ETA

In this model, 8.14 is the constant in the ETA equation, which varies the V_{ds} threshold. Berkeley SPICE3 uses 8.15.

Solution: To convert a SPICE3 model to the Synopsys Level 3 MOSFET device model, multiply ETA by 815/814.

MOS3 Empirical Model — Compatibility Notes: NSUB Missing

If you do not specify NSUB in SPICE3, the KAPPA equation becomes inactive. The Synopsys Level 3 MOSFET model generates a default NSUB from GAMMA, and the KAPPA equation is active.

Solution: If you do not specify NSUB in the SPICE3 model, set KAPPA=0 in the Synopsys Level 3 MOSFET model.

MOS3 Empirical Model — Compatibility Notes: LD Missing

If you do not specify LD, simulation uses the default (0.75XJ). The SPICE3 default for LD is zero.

Solution: If you do not specify `LD` in the SPICE3 model, set `LD=0` in the Level 3 MOSFET model.

MOS3 Empirical Model — Compatibility Notes: KP Given and U0 Not Given

If `KP` is specified but `U0` is not specified, HSPICE calculates `U0` from `KP`. SPICE3 uses the default value ($600\text{cm}^2/\text{Vs}$) for `U0`.

In summary, MOS3 in HSPICE is not compatible with that of SPICE3. However, the same I-V characteristics can still be obtained from both SPICE and HSPICE, when proper model parameters are given in the model cards.

Some of the key model parameters include:

1. `TOX`, `U0`, `VT0`, `NSUB`, `XJ`, `LD`: Key technology scaling parameters.
2. `VMAX`, `KAPPA`, `ETA`, `THETA`: Velocity saturation, DIBL, mobility degradation parameters.

These parameters are used to address the major features of MOS3, and they should be extracted, and explicitly given in the model cards to simulate MOS3 model based circuit design.

| Name | Symbol | Value |
|---------------------------------|------------------------|--|
| Boltzmann constant | k | = $1.3806226\text{e-23}\text{J}\cdot\text{K}^{-1}$ |
| Electron charge | e | = $1.6021918\text{e-19}\text{C}$ |
| Permittivity of silicon dioxide | ϵ_{ox} | = $3.45314379969\text{e-11}\text{F/m}$ |
| Permittivity of silicon | ϵ_{si} | = $1.035943139907\text{e-10}\text{F/m}$ |

MOS3 Empirical Model — Temperature Compensation Example

This example is based on demonstration netlist `tempdep.sp`, which is available in directory `$installdir/demo/hspice/mos`:

Chapter 2: MOSFET Models

LEVEL 3: MOS3 Empirical Model (SPICE 2G)

```
$ test of temp dependence for LEVEL=3 Tlevc=0 Tlev=1
.option ingold=2 numdgt=6 post=2
.temp 25 100
vd d 0 5
vg g 0 2
m1 d g 0 0 nch w=10u L=1u
.op
.print id=LX4(m1) vdsat=lv10(m1)
.model nch nmos LEVEL=3 tlev=1 tlevc=0 acm=3
+ uo=600 tox=172.6572
+ vto=0.8 gamma=0.8 phi=0.64
+ kappa=0 xj=0
+ nsub=1e16 rsh=0
+ tcv=1.5e-3 bex=-1.5
.end
```

This simple model, with XJ=0 and KAPPA=0, has a saturation current:

$$I_{ds} = \frac{\text{beta} \cdot 0.5 \cdot (v_{gs} - v_{tm})^2}{1 + fb}$$

$$\text{beta} = COX \cdot \left(\frac{W}{L}\right) \cdot UO(t), fb = \frac{GAMMA}{(4 \cdot \sqrt{\phi(t)})}$$

Using the model parameters in the input file, and the preceding equations, produces these results:

$$\text{beta} = (1.2e - 3) \cdot \left(\frac{t}{tref}\right)^{BEX}$$

$$v_{tm} = 0.8 - TCV \cdot (t - tref)$$

$$\phi(t) = 0.64 \cdot \left(\frac{t}{tref}\right) - vtherm \cdot \left(egarg + 3 \cdot \log\left(\frac{t}{tref}\right)\right)$$

At room temperature:

$$\text{beta} = (1.2e - 3)$$

$$v_{tm} = 0.8$$

$$\phi(t) = 0.64$$

$$I_{ds} = (1.2e - 3) \cdot 0.5 \cdot \frac{(2 - 0.8)^2}{1 + \frac{0.2}{\sqrt{0.64}}} = 6.912e - 4$$

At T=100:

$$\text{beta} = 1.2e - 3 \cdot (1.251551)^{-1.5} = 0.570545e - 4$$

$$v_{tm} = 0.8 - (1.5e - 3) \cdot 75 = 0.6875$$

$$\text{egarg} = 9.399920, \text{vtherm} = 3.215466e - 2$$

$$\text{phi}(t) = 0.64 \cdot 1.251551 - 0.3238962 = 0.4770964$$

$$I_{ds} = \text{beta} \cdot 0.5 \cdot \frac{(2 - vt)^2}{1 + \frac{0.2}{\sqrt{\text{phi}(t)}}} = 5.724507e - 4$$

Simulation results:

T=25, id=6.91200e-04

T=100, id=5.72451e-04

These results agree with the hand calculations.

LEVEL 4: Grove-Frohman-LEVEL 2 Model Derived from SPICE 2E.3

This model is the same as [LEVEL 2: MOS2 Grove-Frohman \(SPICE 2G\) Model](#) with the following exceptions:

- No narrow width effects: $h=1$
- No short-channel effects: $\gamma=GAMMA$
- For lateral diffusion, $LD_{scaled}=LD \cdot XJ \cdot SCALM$. If you specify XJ , the LD default=0.75. If you do not specify XJ , the default is 0.
- TPG, the model parameter for type of gate materials, defaults to zero (AL gate). The default is 1 for other levels. If you do not specify VTO, this parameter computes VTO (see [Common Threshold Voltage Equations](#)).
- Starting in 2001.4.2, MOSFET LEVEL 4 and LEVEL 9 support both M and AREA scaling.

LEVEL 5: AMI-ASPEC Depletion and Enhancement (Taylor-Huang) Model

This model uses micrometer units rather than the typical meter units. Units and defaults are often unique in LEVEL 5. Level 5 does not use the SCALM option:

- [AMI-ASPEC Model Parameters](#)
 - [AMI-ASPEC Model Equations — Cutoff Region \(\$V_{gs} < V_{th}\$ \)](#)
 - [AMI-ASPEC Model Equations — Depletion \(\$V_{gs} - V_{fb} < 0\$ \)](#)
 - [AMI-ASPEC Model — Depletion Mode DC Model, ZENH=0](#)
-

AMI-ASPEC Model Parameters

This model uses the generic MOSFET model parameters described in [Common MOSFET Model Parameters](#) section. In addition, it also uses the following parameters:

| Name (Alias) | Units | Default | Description |
|--------------|---------------|---------|------------------------------------|
| AFC | | 1.0 | Area factor for MOSFET capacitance |
| CAPOP | | 6 | Gate capacitance selector |
| METO | μm | 0.0 | Metal overlap on gate |

Use the ZENH flag mode parameter to select one of two modes: enhancement or depletion.

| Parameter | Description |
|-----------|---|
| ZENH=1 | This enhancement model (default mode) is a portion of the Synopsys MOS5 device model, and is identical to AMI SPICE MOS LEVEL 4. |
| ZENH=0 | This depletion model is revised in the Synopsys MOS5 device model (from previous depletion mode) and is identical to AMI SPICE MOS LEVEL 5. |

The Synopsys enhancement and depletion modes are basically identical to the AMI models. However, the Synopsys enhancement and depletion modes let you choose either SPICE or ASPEC temperature compensation.

Chapter 2: MOSFET Models

LEVEL 5: AMI-ASPEC Depletion and Enhancement (Taylor-Huang) Model

- TLEV=1 (default) uses ASPEC-style temperature compensation.
- TLEV=0 uses SPICE-style temperature compensation.

CAPOP=6 represents AMI Gate Capacitance in the Synopsys device models. CAPOP=6 is the default setting for LEVEL 5 only. LEVEL 5 models can also use CAPOP=1, 2, and 3.

The ACM parameter defaults to 0 in LEVEL 5, invoking SPICE-style parasitics. You can also set ACM to 1 (ASPEC) or to 2 (Synopsys device models). All MOSFET models follow this convention.

You can use .OPTION SCALE with the LEVEL 5 model; however, you cannot use the SCALM option, due to the difference in units.

You *must* specify the following parameters for MOS LEVEL 5: VTO (VT), TOX, UO (UB), FRC, and NSUB (DNB).

AMI-ASPEC Model Equations — Cutoff Region ($V_{gs} < V_{th}$)

This section covers the following topics:

- [AMI-ASPEC Model — Cutoff Region, \$V_{gs} < V_{th}\$](#)
- [AMI-ASPEC Model — Effective Channel Length and Width](#)
- [AMI-ASPEC Model — Threshold Voltage, \$V_{th}\$](#)
- [AMI-ASPEC Model — Saturation Voltage, \$V_{dsat}\$](#)
- [AMI-ASPEC Model — Mobility Reduction, \$UB_{eff}\$](#)
- [AMI-ASPEC Model — Channel Length Modulation](#)
- [AMI-ASPEC Model — Subthreshold Current, \$I_{ds}\$](#)

AMI-ASPEC Model — Cutoff Region, $V_{gs} < V_{th}$

$I_{ds} = 0$ (See [AMI-ASPEC Model — Subthreshold Current, \$I_{ds}\$](#))

On Region, $V_{gs} > V_{th}$

$$I_{ds} = \beta \cdot \left\{ \left(V_{gs} - V_{bi} - \frac{Vde}{2} \right) \cdot Vde - \frac{2}{3} \Rightarrow \frac{1}{2} (\Phi_f + Vde + V_{sb})^{3/2} - \frac{1}{3} (\Phi_f + V_{sb})^{3/2} \right\}$$

The following equations calculate values used in the preceding equation:

$$vde = \min(v_{ds}, v_{dsat})$$

$$\beta = UB_{eff} \cdot cox \cdot \frac{W_{eff}}{L_{eff}}$$

$$\Phi_f = 2 \cdot v_{tm} \cdot \ln\left(\frac{DNB}{ni}\right)$$

The following equation calculates the gate oxide capacitances per unit area:

$$cox = \frac{E_{ox}}{TOX \cdot 1E-10} \text{ F/m}$$

AMI-ASPEC Model — Effective Channel Length and Width

The following equations determine the effective channel length and width in the LEVEL 5 model:

$$W_{eff} = W_{scaled} \cdot WMLT + OXETCH$$

$$L_{eff} = L_{scaled} \cdot LMLT - 2 \Rightarrow LATD + DEL$$

AMI-ASPEC Model — Threshold Voltage, v_{th}

The VTO model parameter is an extrapolated zero-bias threshold voltage for a large device. The following equation calculates the effective threshold voltage, including the device size effects and the terminal voltages:

$$v_{th} = v_{bi} + \gamma \cdot (\Phi_f + v_{sb})^{1/2}$$

The following equations calculate values used in the preceding equation:

$$v_{bi} = v_{fb} + \Phi_f = VTO - \gamma_0 = \Phi_f^{1/2}$$

$$\gamma_0 = \frac{(2 \cdot E_{si} \cdot q \cdot DNB)^{1/2}}{cox}$$

Note: You must specify DNB and VTO parameters for the LEVEL 5 model. The Synopsys device model uses DNB to compute γ_0 , and ignores the GAMMA model parameter.

The following equation computes the γ effective body effect, including the device size effects:

Chapter 2: MOSFET Models

LEVEL 5: AMI-ASPEC Depletion and Enhancement (Taylor-Huang) Model

$$\gamma = \gamma_0 \cdot (1 - scf) \cdot (1 + ncf)$$

If $SCM < 0$, then $scf=0$.

$$\text{Otherwise, } scf = \frac{XJ}{L_{eff}} \cdot \left\{ \left[1 + \frac{2xd}{XJ} \cdot (SCM \cdot v_{ds} + v_{sb} + \Phi_f)^{1/2} \right]^{1/2} - 1 \right\}$$

If $NWM < 0$, then $ncf=0$.

$$\text{Otherwise, } ncf = \frac{NWM \cdot X_d \cdot (\Phi_f)^{1/2}}{W_{eff}}$$

The following equation calculates the x_d value used in the preceding equations:

$$X_d = \left(\frac{2 \cdot E_{si}}{q \cdot DNB} \right)^{1/2}$$

AMI-ASPEC Model — Saturation Voltage, v_{dsat}

The following equation computes the saturation voltage due to the channel pinch-off at the drain side:

$$v_{sat} = v_{gs} - v_{bi} + \frac{\gamma^2}{2} \cdot \left\{ 1 - \left[1 + \frac{4}{\gamma^2} \cdot (v_{gs} - v_{bi} + \Phi_f + v_{sb}) \right]^{1/2} \right\}$$

$$v_{dsat} = v_{sat}$$

If ECV does not equal 1000, the program modifies v_{sat} to include the carrier velocity saturation effect:

$$v_{dsat} = v_{sat} + v_c - (v_{sat}^2 + v_c^2)^{1/2}$$

, where

$$v_c = ECV \cdot L_{eff}$$

AMI-ASPEC Model — Mobility Reduction, UB_{eff}

The following equation computes the mobility degradation effect in the LEVEL 5 MOSFET model:

$$UB_{eff} = \frac{1}{\frac{1}{UB} + \frac{FRC \cdot (v_{gs} - v_{th})}{TOX} + \frac{v_{de}}{VST \cdot L_e} + FSB \cdot v_{sb}^{1/2}}$$

The following equations calculate the L_e value used in the preceding equation:

$$L_e = L_{eff} \text{ linear region}$$

$$L_e = L_{eff} - \Delta L \text{ saturation region}$$

The next section describes the ΔL channel length modulation effect.

AMI-ASPEC Model — Channel Length Modulation

The LEVEL 5 model modifies the I_{ds} current to include the channel length modulation effect:

$$I_{ds} = \frac{I_{ds}}{1 - \frac{\Delta L}{L_{eff}}}$$

The following equation calculates the ΔL value used in the preceding equation:

$$\Delta L = 1e4 \cdot \left[\frac{2.73e3 \cdot XJ}{DNB \cdot \ln\left(\frac{1e20}{DNB}\right)} \right]^{1/3} \cdot [(v_{ds} - v_{dsat} + PHI)^{1/3} - PHI^{1/3}]$$

ΔL is in microns, if XJ is in microns and DNB is in cm^{-3} .

AMI-ASPEC Model — Subthreshold Current, I_{ds}

The Fast Surface State (FSS) characterizes this region of operation if it is greater than $1e10$. The following equation then calculates the effective threshold voltage, separating the strong inversion region from the weak inversion region:

$$von = v_{th} + fast$$

The following equation calculates the fast value used in the preceding equation:

$$fast = v_{tm} \cdot \left[1 + \frac{q \cdot FSS}{cox} + \frac{\gamma}{2 \cdot (\Phi_f + v_{sb})^{1/2}} \right]$$

In the preceding equations, vt is the thermal voltage.

The following equations calculate I_{ds} .

Weak Inversion Region, $v_{gs} < v_{th}$

Chapter 2: MOSFET Models

LEVEL 5: AMI-ASPEC Depletion and Enhancement (Taylor-Huang) Model

$$I_{ds} = (v_{on}, v_{de}, v_{sb}) \cdot e^{\frac{v_{gs} - v_{on}}{fast}}$$

Strong Inversion Region, $v_{gs} > v_{th}$

$$I_{ds} = I_{ds}(v_{gs}, v_{de}, v_{sb})$$

Note: Strong inversion also use the modified threshold voltage (v_{on}) that FSS produces; that is, the mobility equations use v_{on} instead of v_{th} .

AMI-ASPEC Model Equations — Depletion ($V_{gs}-V_{fb} < 0$)

$$I_{ds} = \beta_1 \cdot \left\{ q \cdot NI \cdot v_{de} + cav \cdot \left[(v_{gs} - v_{fb}) \cdot v_{de} - \frac{v_{de}^2}{2} \right] \right.$$

$$\left. - \frac{2}{3} \cdot cav \cdot \gamma \cdot [(v_{de} + v_{sb} + \Phi_d)^{3/2} - (v_{sb} + \Phi_d)^{3/2}] \right\}$$

Enhancement, $v_{gs}-v_{fb} > v_{de} > 0$

$$I_{ds} = \beta_1 \cdot \left\{ q \cdot NI \cdot v_{de} - \frac{2}{3} \cdot cav \cdot \gamma \cdot [(v_{de} + v_{sb} + \Phi_d)^{3/2} - (v_{sb} + \Phi_d)^{3/2}] \right\}$$

$$\beta \cdot \left[(v_{gs} - v_{fb}) \cdot v_{de} - \frac{v_{de}^2}{2} \right]$$

Partial Enhancement, $v_{gs}-v_{fb} < v_{de}$

$$I_{ds} = \beta_1 \cdot \left\{ q \cdot NI \cdot v_{de} + cav \cdot \left[(v_{gs} - v_{fb}) \cdot v_{de} - \frac{v_{de}^2}{2} \right] \right.$$

$$\left. - \frac{2}{3} \cdot cav \cdot \gamma \cdot [(v_{de} + v_{sb} + \Phi_d)^{3/2} - (v_{sb} + \Phi_d)^{3/2}] \right\}$$

$$\left(\frac{1}{2} \beta - \beta_1 \cdot cav \right) \cdot (v_{gs} - v_{fb})^2$$

The following equations calculate values used in the preceding equations:

$$\beta_1 = UH \cdot \frac{W_{eff}}{L_{eff}}$$

$$\beta = UBe_{eff} \cdot cox \cdot \frac{W_{eff}}{L_{eff}}$$

$$cav = \frac{cox \cdot cs}{cox + cs}$$

$$cs = \frac{2.77E_{si}}{DP \cdot 1e-4}$$

$$\Phi_d = v_{tm} \cdot \ln\left(\frac{DNB \cdot nd}{ni^2}\right)$$

$$nd = \frac{NI \cdot 1e4}{DP}$$

$$vde = \min(v_{ds}, v_{dsat})$$

The following sections describe the saturation voltage, threshold voltage, and effective γ .

This section covers the following topics:

- AMI-ASPEC Model — Depletion: Threshold Voltage, v_{th}
- AMI-ASPEC Model — Depletion: Saturation Voltage, v_{dsat}
- AMI-ASPEC Model — Depletion: Mobility Reduction, UB_{eff}
- AMI-ASPEC Model — Depletion: Channel Length Modulation
- AMI-ASPEC Model — Depletion: Subthreshold Current, I_{ds}

AMI-ASPEC Model — Depletion: Threshold Voltage, v_{th}

The VTO model parameter is an extrapolated zero-bias threshold voltage for a large device. The following equations calculate the effective threshold voltage, including the device size effects and the terminal voltages:

$$v_{th} = v_{fb} - \beta d \Rightarrow [v_{ch} - \gamma = (\Phi_d + v_{sb})^{1/2}]$$

The following equations calculate values used in the preceding equation:

Chapter 2: MOSFET Models

LEVEL 5: AMI-ASPEC Depletion and Enhancement (Taylor-Huang) Model

$$v_{fb} = VTO + \beta d \cdot (vch - \gamma_0 \Phi_d^{1/2})$$

$$\beta d = \frac{UH \cdot cav}{UB \cdot cox}$$

$$vch = \frac{q \cdot NI}{cav}$$

$$\gamma_0 = \frac{(2 \cdot E_{si} \cdot q \cdot na1)^{1/2}}{cav}$$

$$na1 = \frac{nd \cdot DNB}{nd + DNB}$$

$$nd = \frac{NI}{DP \cdot 1e-4}$$

The following equation computes the effective γ , including the small device size effects:

$$\gamma = \gamma_0 \cdot (1 - scf) \cdot (1 + ncf)$$

The following equations calculate values used in the preceding equation:

If SCM $\neq 0$, then $scf=0$. Otherwise,

$$scf = \frac{XJ}{L_{eff}} \cdot \left\{ \left[1 + \frac{2xd}{XJ} \cdot (SCM \cdot v_{ds} + v_b + \Phi_d)^{1/2} \right]^{1/2} - 1 \right\}$$

If NWM $\neq 0$, then $ncf=0$. Otherwise,

$$ncf = \frac{NWM \cdot X_d \cdot \Phi_d^{1/2}}{W_{eff}}$$

The following equation calculates the x_d value used in the preceding equation:

$$X_d = \left(\frac{2 \cdot E_{si}}{q \cdot DNB} \right)^{1/2}$$

Note: If $v_{gs} \leq v_{th}$, the surface is inverted and a residual DC current exists.

If v_{sb} is large enough to make $v_{th} > v_{in_{th}}$, then v_{th} is the inversion threshold voltage. To determine the residual current, this model

inserts $v_{in_{th}}$ into the I_{ds} , v_{sat} , and mobility equation in place of v_{gs} (except for v_{gs} in the exponential term of the subthreshold current).

The inversion threshold voltage at a specified v_{sb} is $v_{in_{th}}$, which the following equation computes:

$$v_{in_{th}} = v_{fb} - \frac{q \cdot NI}{cox} - v_{sb}$$

AMI-ASPEC Model — Depletion: Saturation Voltage, v_{dsat}

The following equation computes the saturation voltage (v_{sat}):

$$v_{sat} = v_{gs} - v_{fb} + v_{ch} + \frac{\gamma^2}{2} \cdot \left\{ 1 - \left[1 + \frac{4}{\gamma^2} \cdot (v_{gs} - v_{fb} + v_{ch} + v_{sb} + \Phi_d) \right]^{1/2} \right\}$$

$$v_{dsat} = v_{sat}$$

If ECV is not equal to 1000 (V/ μ m), the Synopsys device models modify v_{sat} to include the carrier velocity saturation effect:

$$v_{dsat} = v_{sat} + v_c - (v_{sat} + v_c^2)^{1/2}$$

The following equation calculates the v_c value used in the preceding equation:

$$v_c = ECV \cdot L_{eff}$$

AMI-ASPEC Model — Depletion: Mobility Reduction, UB_{eff}

The surface mobility (UB) depends on terminal voltages as follows:

$$UB_{eff} = \frac{1}{\frac{1}{UB} + \frac{FRC \cdot (v_{gs} - v_{th})}{TOX} + \frac{v_{de}}{VST \cdot le} + FSB \cdot v_{sb}^{1/2}}$$

The following equations calculate values used in the preceding equation:

$$L_e = L_{eff} \text{ Linear region}$$

$$L_e = L_{eff} - \Delta L \text{ Saturation region}$$

The next section describes the ΔL channel length modulation effect.

AMI-ASPEC Model — Depletion: Channel Length Modulation

Modify the I_{ds} current to model the channel length modulation effect:

Chapter 2: MOSFET Models

LEVEL 5: AMI-ASPEC Depletion and Enhancement (Taylor-Huang) Model

$$I_{ds} = \frac{I_{ds}}{1 - \frac{\Delta L}{L_{eff}}}$$

The following equation calculates the ΔL value used in the preceding equation:

$$\Delta L = 1e4 \cdot \left[\frac{2.73e3 \cdot XJ}{na1 \cdot \ln\left(\frac{1e20}{na1}\right)} \right]^{1/3} \cdot [(v_{ds} - v_{dsat} + PHI)^{1/3} - PHI^{1/3}]$$

The ΔL parameter is in microns, if XJ is in microns and $na1$ is in cm^{-3} .

AMI-ASPEC Model — Depletion: Subthreshold Current, I_{ds}

If device leakage currents become important for operation near or below the normal threshold voltage, then this model considers the subthreshold characteristics. The Level 5 MOSFET model uses the subthreshold model only if the number of fast surface states (FSS) is greater than $1e10$. The following equation determines the effective threshold voltage (v_{on}):

$$v_{on} = v_{th} + fast$$

The following equation calculates the fast value used in the preceding equation:

$$fast = v_{tm} \cdot \left[1 + \frac{q \cdot FSS}{cox} + \frac{\gamma}{2 \cdot (\Phi_d + v_{sb})^{1/2}} \right]$$

If $v_{on} < v_{in_{th}}$, then simulation substitutes $v_{in_{th}}$ for v_{on} .

Note: The Level 5 MOSFET device model uses the following subthreshold model only if $v_{gs} < v_{on}$, and if the device is either in partial or full enhancement mode. Otherwise, it uses the model in enhancement mode ($ZENH=1$). The subthreshold current calculated below includes the residual DC current.

If $v_{gs} < v_{on}$ then:

Partial Enhancement, $v_{gs}-v_{fb} < v_{de}$

$$I_{ds} = \beta1 \cdot \left\{ q \cdot NI \cdot vde + cav \cdot \left[(v_{on} - v_{fb}) \cdot vde - \frac{vde^2}{2} \right] \right\}$$

$$-\frac{2}{3} \cdot cav \cdot \gamma \cdot [(vde + v_{sb} + \Phi_d)^{3/2} - (v_{sb} + \Phi_d)^{3/2}] \Bigg\}$$

$$\frac{1}{2} \cdot \left(\beta \cdot e^{\frac{v_{gs} - von}{fast}} - \beta_1 \right) \cdot (von - v_{fb})^2$$

Full Enhancement, $v_{gs} - v_{fb} > 0$

$$I_{ds} = \beta_1 \cdot \left\{ q \cdot NI \cdot vde - \frac{2}{3} \cdot cav \cdot \gamma \cdot [(vde + v_{sb} + \Phi_d)^{3/2} - (v_{sb} + \Phi_d)^{3/2}] \right\}$$

$$\beta \cdot \left[(von - v_{fb}) \cdot vde - \frac{vde^2}{2} \right] \cdot e^{\frac{v_{gs} - von}{fast}}$$

This example is based on demonstration netlist m15iv.sp, which is available in directory \$installdir/demo/hspice/mos:

```

FILE ML5IV.SP HSPICE LEVEL 5 MODEL EXAMPLES
*OUTPUT CHARACTERISTICS FOR ENHANCEMENT & DEPLETION MODE
.OPT ACCT LIST CO=132 POST=2
.OP
VDS 3 0 .1
VGS 2 0
M1 1 2 0 0 MODEN L=20U W=20U
.MODEL MODEN NMOS LEVEL=5
+ VT=.7 TOX=292 FRC=2.739E-2 DNB=2.423E16 UB=642.8
+ OXETCH=-.98 XJ=.29 LATD=.34 ECV=4 VST=5.595E7
+ FSB=7.095E-5 SCM=.4 FSS=2.2E11 NWM=.93 PHI=.61
+ TCV=1.45E-3 PTC=9E-5 BEX=1.8
*
VIDS 3 1
.DC VGS 0 5 0.2
.PRINT DC I(VIDS) V(2)
.PRINT DC I(VIDS)
$$$$$$
.ALTER
$$$$$$
M1 1 2 0 0 MODDP L=20U W=20U
.MODEL MODDP NMOS LEVEL=5 ZENH=0.
+ VT=-4.0 FRC=.03 TOX=800 DNB=6E14 XJ=0.8 LATD=0.7
+ DEL=0.4 CJ=0.1E-3 PHI=0.6 EXA=0.5 EXP=0.5 FSB=3E-5
+ ECV=5 VST=4E7 UB=850 SCM=0.5 NI=5.5E11 DP=0.7 UH=1200
*
.END

```

AMI-ASPEC Model — Depletion Mode DC Model, **ZENH=0**

This model uses depletion mode devices as the load element in contemporary standard n-channel technologies[2]. This model assumes a silicon gate construction with an ion implant used to obtain the depletion characteristics. A special model is required for depletion devices, because the implant used to create the negative threshold also results in a complicated impurity concentration profile in the substrate. The implant profile changes the basis for the traditional calculation of the QB bulk charge. The additional charge from the implant, QBI, must be calculated.

This implanted layer also forms an additional channel, offering a conductive pathway through the bulk silicon as well as through the surface channel. This second pathway can cause difficulties when trying to model a depletion device using existing MOS models.

The surface channel partially shields the bulk channel from the oxide interface, and the mobility of the bulk silicon can be substantially higher. Yet with all of these differences, a depletion model still can share the same theoretical basis as the Ihantola and Moll gradual channel model.

The depletion model differs from the Ihantola and Moll model:

- Implant charge accounted for.
- Finite implant thickness (D_P).
- Assumes two channels: a surface channel and a bulk channel.
- Bulk channel has a bulk mobility (U_H).
- Assumes that the bulk gain is different from the surface gain.

In the depletion model, the gain is lower at low gate voltages and higher at high gate voltages. Due to this variation in gain, the enhancement models cannot accurately represent a depletion device. The physical model for a depletion device is basically the same as an enhancement model, except that a one-step profile with D_P depth approximates the depletion implant.

Due to the implant profile, simulation calculates the drain current equation by region. The MOSFET Level 5 model has three regions: depletion, enhancement, and partial enhancement.

Depletion Region, $V_{GS} - V_{FB} < 0$

The bulk channel dominates the low gate voltage region.

Enhancement Region, $v_{gs} - v_{fb} > 0$, $v_{ds} < v_{gs} - v_{fb}$

High gate voltage and low drain voltage define the enhancement region. In this region, both channels are fully turned on.

Partial enhancement region, $v_{gs} - v_{fb} > 0$, $v_{ds} > v_{gs} - v_{fb}$

The region has high gate and drain voltages so the surface region is partially turned on and the bulk region is fully turned on.

LEVEL 6: Lattin-Jenkins-Grove (ASPEC) Model

These models represent ASPEC, MSINC, and ISPICE MOSFET model equations. The only difference between LEVEL 6: Lattin-Jenkins-Grove (ASPEC) Model and [LEVEL 7: Lattin-Jenkins-Grove \(SPICE\) Model](#) equations is the handling of the parasitic elements and the method of temperature compensation. See [Grove-Frohman \(SPICE 2G\) Model — Channel Length Modulation](#) for those model parameters.

This section covers the following topics:

- [Lattin-Jenkins-Grove \(ASPEC\) Model Parameters](#)
 - [Lattin-Jenkins-Grove \(ASPEC\) Model — UPDATE Parameter](#)
 - [Lattin-Jenkins-Grove \(ASPEC\) Model Equations, \(UPDATE=0 or 2\)](#)
 - [Lattin-Jenkins-Grove \(ASPEC\) Model Equations, UPDATE=1](#)
 - [Lattin-Jenkins-Grove \(ASPEC\) Model — Compatibility Notes](#)
-

Lattin-Jenkins-Grove (ASPEC) Model Parameters

This model uses the generic MOSFET model parameters described in [Common MOSFET Model Parameters](#) section. In addition, this model also uses the following parameters:

Alternate Saturation Model Parameters

| Name (Alias) | Units | Default | Description |
|--------------|-------|---------|---|
| KA | | 1.0 | Alternate saturation model: coefficient for the short-channel vds scaling factor. |
| KU | | 0.0 | Lateral field mobility parameter. |
| MAL | | 0.5 | Alternate saturation model: exponent of the short-channel vds scaling factor. |
| MBL | | 1.0 | Exponent for mobility reduction due to the source-drain electric field. |
| NU | | 1.0 | Mobility reduction due to the source-drain electric field. |

Lattin-Jenkins-Grove (ASPEC) Model — UPDATE Parameter

The general form of the I_{ds} equation for this model 6 is the same as [LEVEL 2: MOS2 Grove-Frohman \(SPICE 2G\) Model](#). However, the small size effects, mobility reduction, and channel length modulation are included differently. Also, you can use the multi-level GAMMA capability to model MOS transistors with ion-implanted channels.

This model can represent the ASPEC, MSINC, or ISPICE MOSFET model. Use the UPDATE model parameter to invoke different versions of this model.

| Statement | Description |
|---------------|---|
| UPDATE=0 | This is the original Synopsys Level 6 MOSFET device model, which is not quite compatible with the ASPEC model. It has some discontinuities in the weak inversion, mobility equations ($MOB=3$), and multi-level GAMMA equations. |
| UPDATE=1 | This enhanced version of the LEVEL 6 model contains improved multi-level GAMMA equations. The saturation voltage, drain-source current, and conductances are continuous. |
| UPDATE=2 | This version of the LEVEL 6 model is compatible with the ASPEC model. The multi-level GAMMA model is not continuous as it is in the ASPEC program. See Lattin-Jenkins-Grove (ASPEC) Model — Compatibility Notes . <ul style="list-style-type: none">■ Set UPDATE to 1.0 to use changes to the device equations.■ Set UPDATE to 1.0 or 2 to use the default <code>RD</code> and <code>RS</code> handling. These values and changes provide a more accurate ASPEC model. |
| UPDATE=1 or 2 | $TOX=690$ $UO (UB)=750 \text{ cm}^2/(\text{V} \cdot \text{s}) (\text{N-ch})$ $UTRA (F3)=0.0$ |
| UPDATE=0 | $TOX=1000$ $UO (UB)=750 \text{ cm}^2/(\text{V} \cdot \text{s}) (\text{N-ch})$ $UTRA (F3)=0.0$ If you do not specify <code>LDIF</code> , then the <code>RD</code> and <code>RS</code> values change in the MOSFET: |

Chapter 2: MOSFET Models

LEVEL 6: Lattin-Jenkins-Grove (ASPEC) Model

| Statement | Description |
|--|--|
| UPDATE=1 or 2 and LDIF=0 | $RS = \frac{(RS + NRS \cdot RL)}{M}$ $RD = \frac{(RD + NRD \cdot RL)}{M}$ |
| | Note: The ASPEC program does not use the M multiplier. |
| LDIF ≠ 0: | |
| | $RS = \frac{LATDscaled + LDIFscaled}{Weff} \cdot RS + NRS \cdot \frac{RL}{M}$ |
| | $RD = \frac{LATDscaled + LDIFscaled}{Weff} \cdot RD + NRD \cdot \frac{RL}{M}$ |
| | The vde value in the mobility equations change for the alternate saturation model: |
| | $vde = \min\left(\frac{vds}{vfa}, vsat\right), \text{UPDATE}=1 \text{ or } 2$ |
| | $vde = \min(vds, vfa \cdot vsat), \text{UPDATE}=0$ |
| | The impact ionization equation calculates the saturation voltage: |
| | $vdsat = vfa \cdot vsat, \text{UPDATE}=1 \text{ or } 2$ |
| | $vdsat = vsat, \text{UPDATE}=0$ |
| | The MOB=3 mobility equation changes: |
| UPDATE=1 or 2 and $(vgs - vth)^{F2} > VF1$ | $ueff = \frac{UB}{F4 + (F1 - F3) \cdot VF1 + F3 \cdot (vgs - vth)^{F2}}$ |
| UPDATE=0 and $(vgs - vth)^{F2} > VF1:$ | $ueff = \frac{UB}{F4 + F3 \cdot (vgs - vth)^{F2}}$ |

Lattin-Jenkins-Grove (ASPEC) Model Equations, (UPDATE=0 or 2)

This section covers the following topics:

- ASPEC Model, (UPDATE=0 or 2) — IDS Equation
- ASPEC Model, (UPDATE=0 or 2) — Effective Channel Length and Width
- ASPEC Model, (UPDATE=0 or 2) — Threshold Voltage, v_{th}
- ASPEC Model, (UPDATE=0 or 2) — Single-Gamma, VBO=0
- ASPEC Model, (UPDATE=0 or 2) — Effective Built-in Voltage, v_{bi}
- ASPEC Model, (UPDATE=0 or 2) — Multi-Level Gamma, VBO>0
- ASPEC Model, (UPDATE=0 or 2) — Effective Built-in Voltage, v_{bi} for VBO>0
- ASPEC Model, (UPDATE=0 or 2) — Saturation Voltage, v_{dsat}
- ASPEC Model, (UPDATE=0 or 2) — Improved Multi-Level Gamma, UPDATE=1
- ASPEC Model, (UPDATE=0 or 2) — Saturation Voltage, v_{sat}

ASPEC Model, (UPDATE=0 or 2) — IDS Equation

$$ids = \beta \cdot \left\{ \left(v_{gs} - v_{bi} - \frac{\eta \cdot v_{de}}{2} \right) \cdot v_{de} - \frac{2}{3} \gamma \Rightarrow \{ (PHI + v_{de} + v_{sb})^{3/2} - (PHI + v_{sb})^{3/2} \} \right\}$$

The following equations calculate values used in the preceding equation:

$$v_{de} = \min(v_{ds}, v_{dsat})$$

$$\eta = 1 + \frac{NWE_{scaled}}{w_{eff}}$$

$$\beta = u_{eff} \cdot COX \cdot \frac{w_{eff}}{L_{eff}}$$

- The η , v_{bi} , and γ values define the narrow-width effect.
- The NWE or NWM model parameters also specify the narrow-width effect.
- The v_{bi} and γ parameters specify the short-channel effect.

ASPEC Model, (UPDATE=0 or 2) — Effective Channel Length and Width

The following equations calculate the effective channel length and width from the drawn length and width:

Chapter 2: MOSFET Models

LEVEL 6: Lattin-Jenkins-Grove (ASPEC) Model

$$leff = Lscaled \cdot LMLT + XLscaled - 2 \Rightarrow LDscaled + DELscaled$$

$$weff = M \cdot (Wscaled \cdot WMLT + XWscaled - 2 \Rightarrow WDscaled)$$

$$LREFeff = LREFscaled \cdot LMLT + XLscaled - 2 \Rightarrow LDscaled + DELscaled$$

$$WREFeff = M \cdot (WREFscaled \cdot WMLT + XWscaled - 2 \Rightarrow WDscaled)$$

ASPEC Model, (UPDATE=0 or 2) — Threshold Voltage, v_{th}

The following equation determines the effective threshold voltage:

$$vth = vbi + \gamma \cdot (PHI + vsb)^{1/2}$$

The vbi and γ built-in voltage value depends on the specified model parameters.

ASPEC Model, (UPDATE=0 or 2) — Single-Gamma, VBO=0

If you set the VBO model parameter to zero, simulation uses the single-gamma model, which treats the `LGAMMA` parameter as a junction depth. To modify the `GAMMA` parameter for the short-channel effect, this model then uses the `scf` factor, which the Poon and Yau formulation computes. In this case, simulation multiplies `LGAMMA` by the `SCALM` option.

$$scf = 1 - \frac{LGAMMA}{leff} \Rightarrow \left\{ \left[1 + \frac{2 \cdot LAMBDA}{LGAMMA} \cdot (PHI + vsb)^{1/2} \right]^{1/2} - 1 \right\}$$

The `XJ` model parameter modifies the `GAMMA` model parameter by the short-channel factor (`gl`):

$$gl = 1 - \frac{XJscaled}{leff} \Rightarrow \left\{ \left[1 + \frac{2 \cdot LAMBDA}{XJscaled} \cdot (PHI + vsb + SCM \cdot vds)^{1/2} \right]^{1/2} - 1 \right\}$$

The `gl` factor generally replaces the `scf` factor for the multi-level `GAMMA` model.

The `gw` factor modifies `GAMMA` to compute the narrow-width effect:

$$gw = \frac{1 + NWM \cdot xd}{weff}$$

The following equation calculates the `xd` value used in the preceding equation:

$$xd = \left(\frac{2 \cdot \epsilon si}{q \cdot DNB} \right)^{1/2}$$

Finally, the effective γ , including short-channel and narrow-width effects, is

$$\gamma = \text{GAMMA} \cdot gw \cdot gl \cdot scf$$

ASPEC Model, (UPDATE=0 or 2) — Effective Built-in Voltage, vbi

The Level 6 model includes the narrow-width effect. This effect is the increase in threshold voltage due to the extra bulk charge at the edge of the channel. To use this effect with the NWE model parameter, modify vbi.

Modify vbi to use the short-channel effect, which decreases threshold voltage due to the induced potential barrier-lowering effect. To include this effect, you must specify either the FDS parameter, or the UFDS and VFDS model parameters.

The following equations calculate vbi, which sums up the preceding features.

vds<VFDS, or VFDS=0

$$vbi = VTO - \gamma = \text{PHI}^{1/2} + (\eta - 1) \cdot (\text{PHI} + v_{sb}) - \frac{LD_{scaled}}{Leff}$$

$$= VSH - \frac{\epsilon si}{COX \cdot Leff} = FDS = ds$$

vds>VFDS

$$vbi = VTO - \gamma = \text{PHI}^{1/2} + (\eta - 1) \cdot (\text{PHI} + v_{sb}) - \frac{LD_{scaled}}{leff} = VSH - \frac{\epsilon si}{COX \cdot Leff}$$

$$[(FDS - UFDS) \cdot VFDS + UFDS \cdot vds]$$

The preceding equations describe piecewise linear variations of vbi as a function of vds. If you do not specify VFDS, this model uses the first equation for vbi.

Note: The Level 6 MOSFET device model calculates model parameters such as VTO, PHI, and GAMMA, if you did not specify them (see [Common Threshold Voltage Equations](#)).

ASPEC Model, (UPDATE=0 or 2) — Multi-Level Gamma, VBO>0

Use Multi-Level Gamma to model MOS transistors with Ion-Implanted channels. The doping concentration under the gate is approximated as step functions.

- GAMMA represents the corresponding body effects coefficient for the implant layer.
- LGAMMA represents the corresponding body effects coefficient for the substrate.

Chapter 2: MOSFET Models

LEVEL 6: Lattin-Jenkins-Grove (ASPEC) Model

Figure 2 shows the variation of v_{th} as a function of v_{sb} for Multi-Level Gamma.

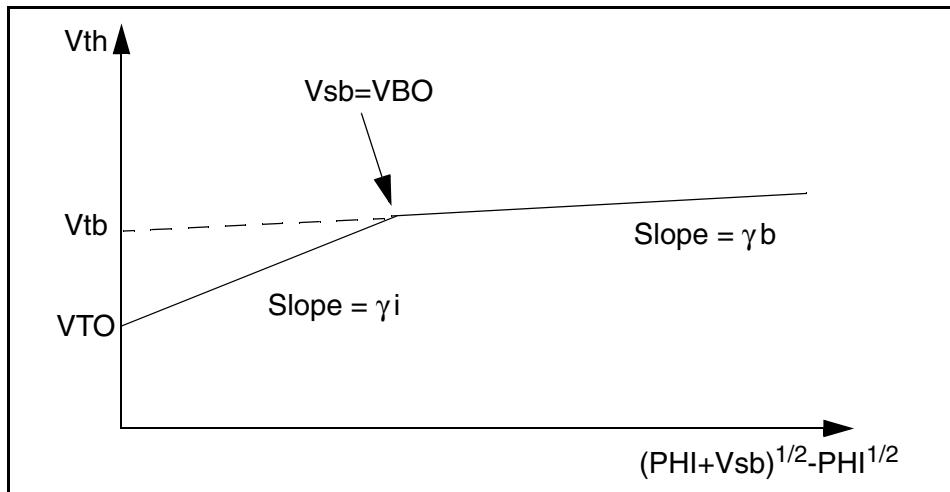


Figure 2 Threshold Voltage Variation

The following equations calculate the threshold voltage for different regions:

Channel Depletion Region is in the Implant Layer, $v_{sb} < V_{BO}$

$$\gamma = \gamma_i$$

$$v_{th} = v_{bi} + \gamma_i \cdot (v_{sb} + \Phi_H)^{1/2}$$

$$v_{bi} = V_{TO} - \gamma_i \cdot (\Phi_H)^{1/2}$$

Channel Depletion Region Expands into the Bulk, $v_{sb} > V_{BO}$

$$\gamma = \gamma_b$$

$$v_{th} = v_{bi} + \gamma_b \cdot (v_{sb} + \Phi_H)^{1/2}$$

$$v_{bi} = v_{tb} - \gamma_b \cdot (\Phi_H)^{1/2}$$

For the threshold voltage to be continuous at $v_{sb}=V_{BO}$, v_{tb} must be:

$$v_{tb} = V_{TO} + (\gamma_i - \gamma_b) \cdot [(V_{BO} + \Phi_H)^{1/2} - (\Phi_H)^{1/2}]$$

- γ_i is the effective value of GAMMA.
- γ_b is the effective value of LGAMMA.

The model computes them as γ in single-gamma models, except the scf factor is 1.0.

$$\gamma i = GAMMA \cdot gw \cdot gl$$

$$\gamma b = LGAMMA \cdot gw \cdot gl$$

**ASPEC Model, (UPDATE=0 or 2) — Effective Built-in Voltage, vbi for VBO>0
For vds < VFDS**

if $v_{sb} \leq VBO$:

$$v_{bi} = VTO - \gamma i = (PHI)^{1/2} + (\eta - 1) \cdot (PHI + v_{sb}) - \frac{LDscaled}{Leff}$$

$$= VSH - \frac{\epsilon si}{COX \cdot Leff} = FDS \Rightarrow ds$$

if $v_{sb} > VBO$:

$$v_{bi} = VTO - \gamma b = (PHI)^{1/2} + (\gamma i - \gamma b) \cdot [(VBO + PHI)^{1/2} - (PHI)^{1/2}] + (\eta - 1)$$

$$(PHI + v_{sb}) - \frac{LDscaled}{Leff} = VSH - \frac{\epsilon si}{COX \cdot Leff} = FDS \Rightarrow ds$$

For vds > VFDS

if $v_{sb} \leq VBO$:

$$v_{bi} = VTO - \gamma i = (PHI)^{1/2} + (\eta - 1) \cdot (PHI + v_{sb})$$

$$- \frac{LDscaled}{Leff} = VSH - \frac{\epsilon si}{COX \cdot Leff}$$

$$[(FDS - UFDS) \cdot VFDS + UFDS \cdot vds]$$

if $v_{sb} > VBO$:

$$v_{bi} = VTO - \gamma b = (PHI)^{1/2} + (\gamma i - \gamma b) \cdot [(VBO + PHI)^{1/2} - (PHI)^{1/2}] + (\eta - 1)$$

$$PHI + v_{sb} - \frac{LDscaled}{Leff} = VSH - \frac{\epsilon si}{COX \cdot Leff}$$

$$= [(FDS - UFDS) \cdot VFDS + UFDS \cdot vds]$$

ASPEC Model, (UPDATE=0 or 2) — Saturation Voltage, vdsat

The following formula determines the saturation voltage due to channel pinch-off at the drain side:

Chapter 2: MOSFET Models

LEVEL 6: Lattin-Jenkins-Grove (ASPEC) Model

$$vsat = \frac{vgs - vbi}{\eta} + \frac{1}{2} \left(\frac{\gamma}{\eta} \right)^2 \cdot \left\{ 1 - \left[1 + \left(\frac{2 \cdot \eta}{\gamma} \right)^2 \cdot \left(\frac{vgs - vbi}{\eta} + PHI + vsb \right) \right]^{1/2} \right\}$$

The following equation calculates the reduction of the saturation voltage due to the carrier velocity saturation effect:

$$vdsat = vsat + vc - (vsat^2 + vc^2)^{1/2}$$

In the preceding equation, determines vc if the ECRIT model parameter >0 , or VMAX >0 , and KU ≤ 1 . If you specify both ECRIT and VMAX, then simulation uses only the VMAX equation. However, this model does not use the VMAX equation if MOB=4 or MOB=5, because these mobility equations already contain a velocity saturation term.

$$vc = ECRIT \cdot Leff \text{ or } vc = \frac{VMAX \cdot Leff}{ueff}$$

Because $v_{sb} > VBO$, γ switches from γ_1 to γ_2 , and the ids , $vsat$, and conductance values are not continuous as in the following example. To correct this discontinuity problem, specify the UPDATE=1 model parameter. The next section discusses this improvement.

This example is based on demonstration netlist tgam2.sp, which is available in directory $\$installdir/demo/hspice/mos$:

```
$ tgam2.sp---multi-level gamma model
* this data is for the comparison of multi-level gamma
* update=0 or 2 and the improved multi-level gamma update=1.
*
.options post aspec nomod vntol=.1u reli=.001 relv=.0001
*
.model nch nmox bulk=99 update=2
+ fds=0.9 ku=1.6 mal=0.5 mob=1 clm=1
+ latd=0.2 phi=0.3 vt=0.9 gamma=0.72 lgamma=0.14
+ vb0=1.2 f1=0.08 esat=8.6e+4 kl=0.05
+lambd=3.2u ub=638 f3=0.22
+ ka=0.97 mbl=0.76 nfs=1.0e+12 wic=0
+ ldel=0.084 wdel=0.037 tox=365 vsh=0.7
*
vd 1 0 5
vb 0 99 0
vg 2 0 1
ma 1 2 0 99 nch 26.0 1.4
.dc vb 1.0 1.3 .01
.probe ids=par('i(ma)') vth=par('lv9(ma)') vdsat=par('lv10(ma)')
.probe gm=par('LX7(ma)') ds=par('LX8(ma)') gmb=par('LX9(ma)')
.end
```

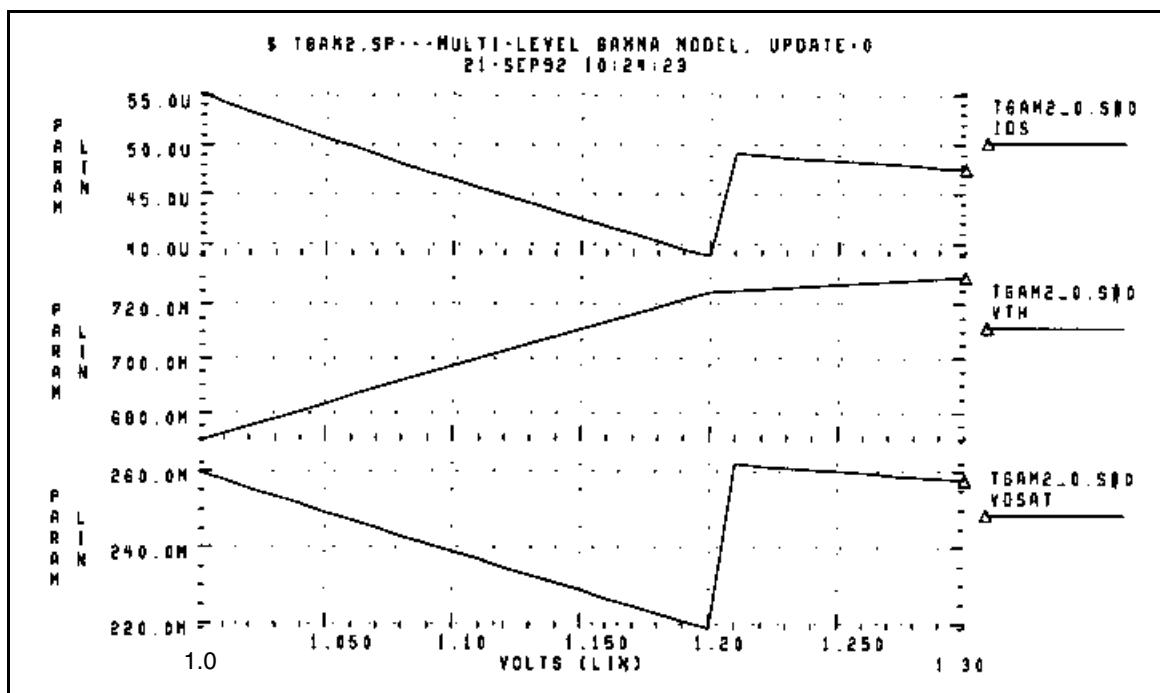


Figure 3 Variation of IDS , VTH and $VDSAT$ for $UPDATE=0$

Chapter 2: MOSFET Models

LEVEL 6: Lattin-Jenkins-Grove (ASPEC) Model

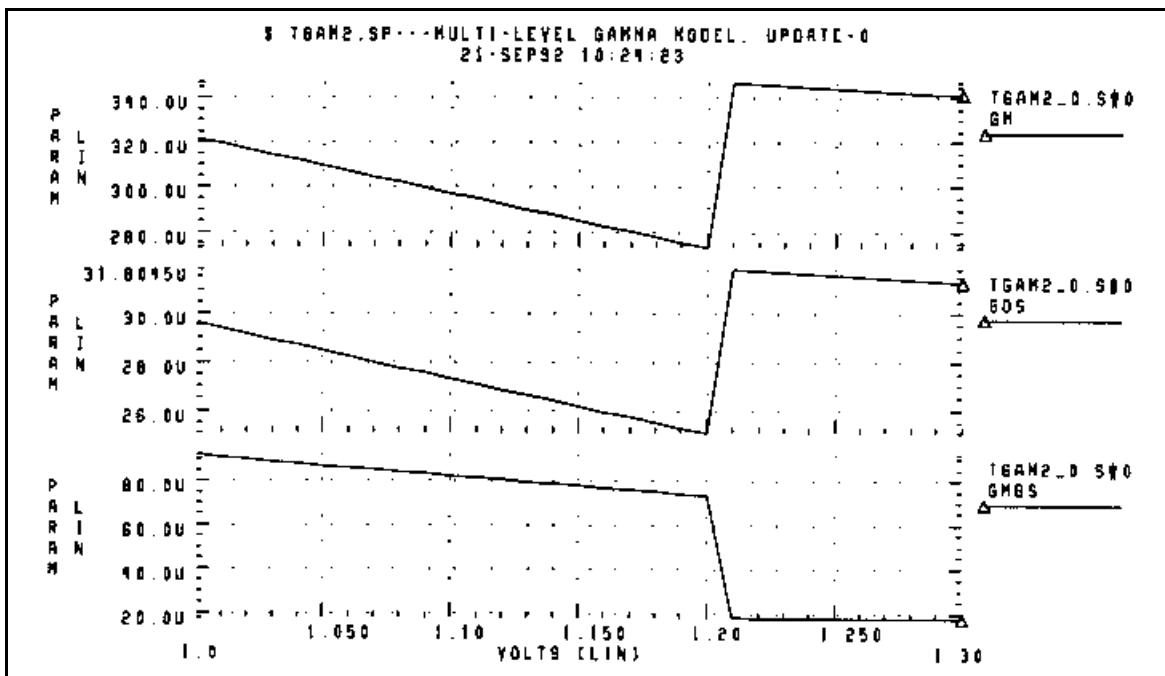


Figure 4 Variation of GM, GDS and GMBS for UPDATE=0

Each plot compares IDS, VTH, VDSAT, GM, GDS and GMBS as a function of v_{sb} for UPDATE=0.

ASPEC Model, (UPDATE=0 or 2) — Improved Multi-Level Gamma, UPDATE=1

As demonstrated in previous sections, the regular Multi-Level Gamma displays some discontinuities in saturation voltage and drain current. This occurs because when v_{sb} is less than VBO, simulation sets γ to γ_i and uses it to calculate i_{ds} and v_{sat} . This is not correct; if $(v_{ds} + v_{sb})$ exceeds VBO, then the depletion regions at the drain side expands into the substrate region, and the v_{sat} computation must use γ_b instead of γ_i . Because $v_{sat}=v_{gs} - v_{th}$ (drain), this model uses γ_i to compute the threshold voltage at the drain for $v_{sb}<VBO$. As a result, the existing model overestimates the threshold voltage ($\gamma_i > \gamma_b$), and underestimates the saturation voltage and the drain current in the saturation region.

This causes a discontinuous increase in the saturation drain current, crossing from the $v_{sb}<VBO$ region to the $v_{sb}>VBO$ region.

The improved Multi-Level model upgrades the saturation voltage and drain current equations, compared to the regular Multi-Level model. To use the improved model, set the model parameter to UPDATE=1.

You can see an example of a multi-level gamma model with UPDATE=2 using a netlist from a previous example. Change UPDATE=0 to UPDATE=2 in the netlist located in directory `$installdir/demo/hspice/mos/tgam2.sp`:

```
$ tgam2.sp---multi-level gamma model
* this data is for the comparison of multi-level gamma
* update=0 or 2 and the improved multi-level gamma update=1.
*
.options post aspec nomod vntol=.1u reli=.001 relv=.0001
*
.model nch nmos bulk=99 update=2
+ fds=0.9 ku=1.6 mal=0.5 mob=1 clm=1
+ latd=0.2 phi=0.3 vt=0.9 gamma=0.72 lgamma=0.14
+ vb0=1.2 f1=0.08 esat=8.6e+4 kl=0.05
+ lambda=3.2u ub=638 f3=0.22
+ ka=0.97 mbl=0.76 nfs=1.0e+12 wic=0
+ ldel=0.084 wdel=0.037 tox=365 vsh=0.7
*
vd 1 0 5
vb 0 99 0
vg 2 0 1
ma 1 2 0 99 nch 26.0 1.4
.dc vb 1.0 1.3 .01
.probe ids=par('i(ma)') vth=par('lv9(ma)') vdsat=par('lv10(ma)')
.probe gm=par('LX7(ma)') ds=par('LX8(ma)') gmb=par('LX9(ma)')
.end
```

Chapter 2: MOSFET Models

LEVEL 6: Lattin-Jenkins-Grove (ASPEC) Model

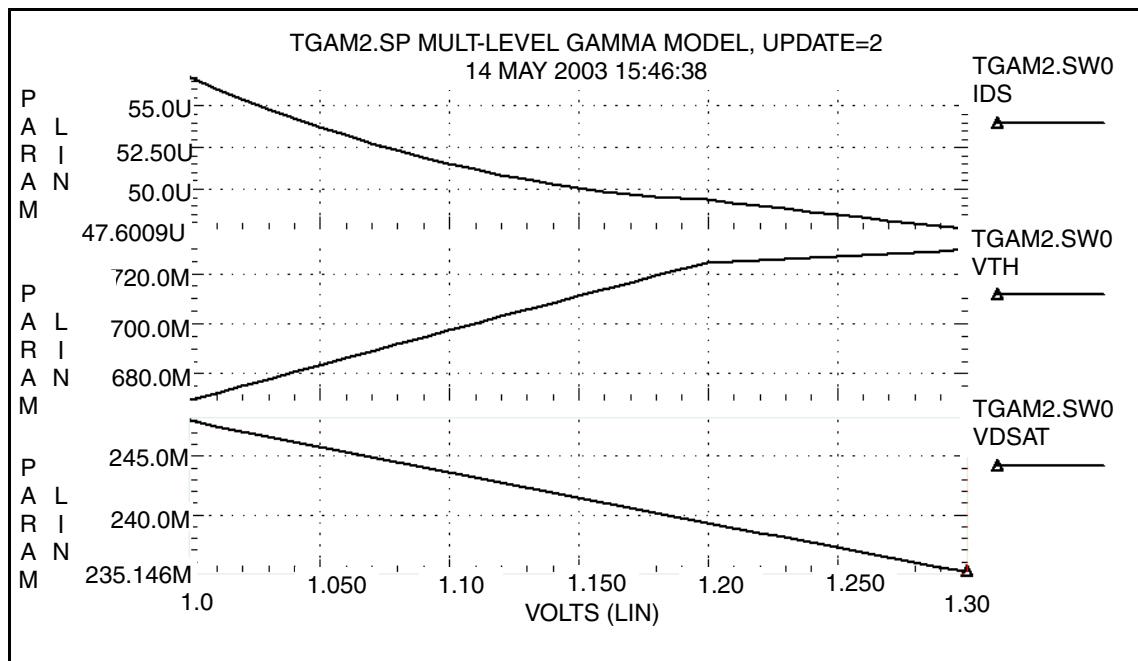


Figure 5 Variation of IDS , VTH and $VDSAT$ for UPDATE=2

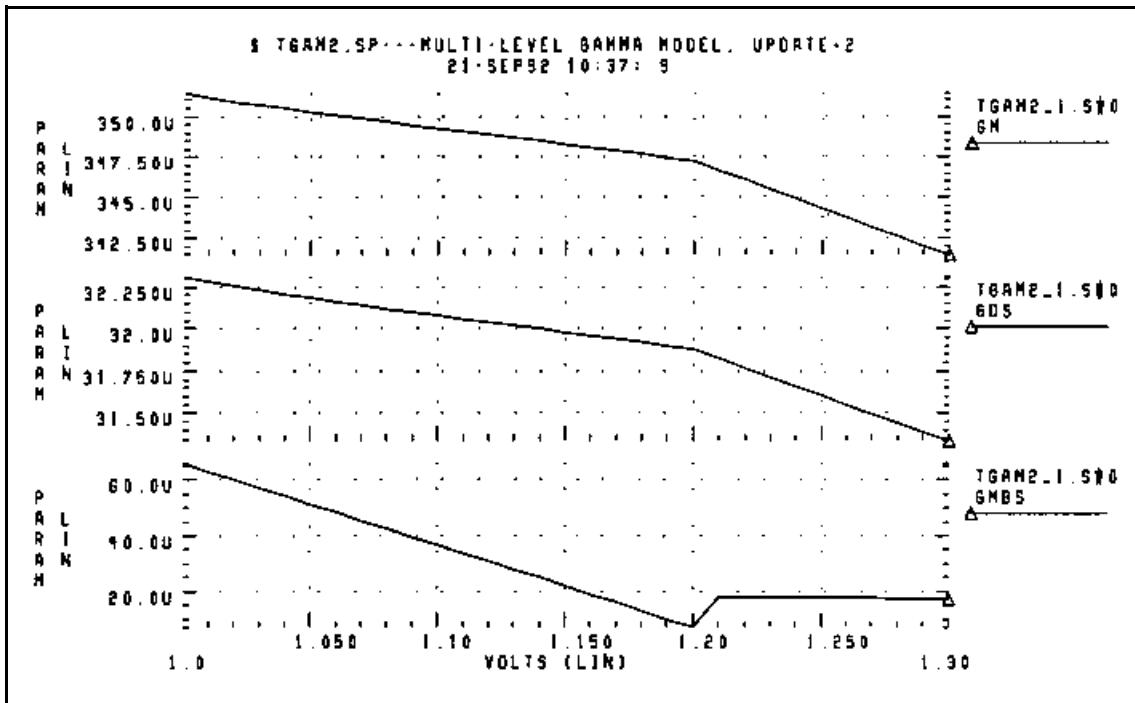


Figure 6 Variation of GM, GDS and GMBS for UPDATE=2

Each plot compares IDS, VTH, VDSAT, GM, GDS, and GMBS as a function of vsb for UPDATE=1.

ASPEC Model, (UPDATE=0 or 2) — Saturation Voltage, vsat

To obtain the right value for vsat, the following equations calculate two trial values of vsat corresponding to γi and γb :

$$vsat1 = \frac{vgs - vbi1}{\eta} + \frac{1}{2} \left(\frac{\gamma i}{\eta} \right)^2 \cdot \left\{ 1 - \left[1 + \left(\frac{2 \cdot \eta}{\gamma i} \right)^2 \cdot \left(\frac{vgs - vbi1}{\eta} + PHI + vsb \right) \right]^{1/2} \right\}$$

$$vsat2 = \frac{vgs - vbi2}{\eta} + \frac{1}{2} \left(\frac{\gamma b}{\eta} \right)^2 \cdot \left\{ 1 - \left[1 + \left(\frac{2 \cdot \eta}{\gamma b} \right)^2 \cdot \left(\frac{vgs - vbi2}{\eta} + PHI + vsb \right) \right]^{1/2} \right\}$$

- vbi1 is the built-in potential corresponding to γi .
- vbi2 is the built-in potential corresponding to γb .

Chapter 2: MOSFET Models

LEVEL 6: Lattin-Jenkins-Grove (ASPEC) Model

- If $(v_{dsat1} + v_{sb}) \leq VBO$, then $v_{dsat}=v_{dsat1}$
- If $(v_{dsat2} + v_{sb}) > VBO$, then $v_{dsat}=v_{dsat2}$

To obtain v_{dsat} , v_c modifies v_{sat} for the carrier velocity saturation.

Lattin-Jenkins-Grove (ASPEC) Model Equations, UPDATE=1

You can use one of three equations for i_{ds} , depending on the region of operation. To derive these equations, this model integrates the bulk charge ($v_{gs} - v_{th}(v)$) from the source to the drain.

For $v_{sb} < VBO - v_{de}$, the model forms an entire gate depletion region in the implant layer.

$$i_{ds} = \beta \cdot \left\{ \left(v_{gs} - v_{bi1} - \frac{\eta \cdot v_{de}}{2} \right) \cdot v_{de} - \frac{2}{3} \cdot \gamma_i \cdot [(PHI + v_{de} + v_{sb})^{3/2} - (PHI + v_{sb})^{3/2}] \right\}$$

In the preceding equation, v_{bi1} is the same as v_{bi} for $v_{sb} \leq VBO$.

For $v_{sb} \geq VBO$, the entire gate depletion region expands into the bulk area.

$$i_{ds} = \beta \cdot \left\{ \left(v_{gs} - v_{bi2} - \frac{\eta \cdot v_{de}}{2} \right) \cdot v_{de} - \frac{2}{3} \cdot \gamma_b \cdot [(PHI + v_{de} + v_{sb})^{3/2} - (PHI + v_{sb})^{3/2}] \right\}$$

In the preceding equation, v_{bi2} is the same as v_{bi} for $v_{sb} > VBO$.

$$i_{ds} = \beta \cdot \left\{ \left(v_{gs} - v_{bi2} - \frac{\eta \cdot v_{de}}{2} \right) \cdot v_{de} - \frac{2}{3} \cdot \gamma_i \cdot [(VBO + PHI)^{3/2} - (v_{sb} + PHI)^{3/2}] \right. \\ \left. (\gamma_i - \gamma_b) \cdot (VBO + PHI)^{1/2} \cdot (VBO - v_{sb}) \right\}$$

For $VBO - v_{de} < v_{sb} < VBO$, the source side gate depletion region is in the implant layer, but the drain side gate depletion region expands into the bulk area.

This section covers the following topics:

- ASPEC Model, (UPDATE=1) — Alternate DC Model (ISPICE model)
- ASPEC Model, (UPDATE=1) — Subthreshold Current, ids
- ASPEC Model, (UPDATE=1) — WIC=0
- ASPEC Model, (UPDATE=1) — WIC=1
- ASPEC Model, (UPDATE=1) — WIC=2
- ASPEC Model, (UPDATE=1) — WIC=3
- ASPEC Model, (UPDATE=1) — Effective Mobility, $ueff$
- ASPEC Model, (UPDATE=1) — MOB=0 Default, No Mobility
- ASPEC Model, (UPDATE=1) — MOB=1
- ASPEC Model, (UPDATE=1) — MOB=2, Frohman-Bentchkowski Equation
- ASPEC Model, (UPDATE=1) — MOB=3, Normal Field Equation
- ASPEC Model, (UPDATE=1) — MOB=4 or 5, Universal Field Mobility Reduction
- ASPEC Model, (UPDATE=1) — MOB=5
- ASPEC Model, (UPDATE=1) — MOB=6 or 7, Modified MOB=3:
- ASPEC Model, (UPDATE=1) — Channel Length Modulation
- ASPEC Model, (UPDATE=1) — CLM=0, No Channel Modulation—Default
- ASPEC Model, (UPDATE=1) — CLM=1, Step Depletion Equation
- ASPEC Model, (UPDATE=1) — CLM=2, Electrostatic Fringing Field
- ASPEC Model, (UPDATE=1) — CLM=3, Carrier Velocity Saturation Equation
- ASPEC Model, (UPDATE=1) — CLM=4, Wang's Equation
- ASPEC Model, (UPDATE=1) — CLM=5, Channel Length Modulation
- ASPEC Model, (UPDATE=1) — CLM=6, ΔL Equation

ASPEC Model, (UPDATE=1) — Alternate DC Model (ISPICE model)

To invoke this model, set the `KU>1` model parameter. Then, the model computes `vfu` and `vfa` scale factors to scale both the `vds` voltage and the `ids` current. These scale factors are functions of `ECRIT` and the `vgs` voltage. The following equations compute the `vfa` and `vfu` factors:

Chapter 2: MOSFET Models

LEVEL 6: Lattin-Jenkins-Grove (ASPEC) Model

$$vfu = 1 - \frac{KU}{(\alpha^2 + KU^2)^{1/2} + \alpha(KU - 1)}$$

$$vfa = KA \cdot vfu^{(2 \cdot MAL)}$$

The following equation calculates the α value used in the preceding equations:

$$\alpha = \frac{ECRIT \cdot L_{eff}}{vgs - vth}$$

Note: The vfu factor is always less than one.

The following equation modifies the ids current:

$NU=1$

$$ids = vfu^{(2 \cdot MBL)} \cdot ids$$

For $NU=0$, the

$$vfu^{(2 \cdot MBL)}$$

factor is set to one.

The ids current is a function of the effective drain to source voltage (vde):

$$vde = \min(vds/vfa, vsat)$$

$$vdsat = vfa \cdot vsat$$

This alternate model is generally coupled with the mobility normal field equations ($MOB=3$) and the channel length modulation drain field equation ($CLM=3$).

The mobility equations use the following vde and vds values:

$$vde = \min(vds, vfa \cdot vsat), UPDATE=0$$

$$vds = \min(vds/vfa, vsat), UPDATE=1, 2$$

ASPEC Model, (UPDATE=1) — Subthreshold Current, ids

is the choice of two different equations, selected through The WIC (Weak Inversion Choice) model parameter characterizes this region of operation.

| Parameter | Description |
|-----------|-----------------------------|
| WIC=0 | No weak inversion (default) |
| WIC=1 | ASPEC-style weak inversion |

| Parameter | Description |
|-----------|--------------------------------------|
| WIC=2 | Enhanced HSPICE-style weak inversion |

In addition to WIC, set the NFS parameter. NFS represents the number of fast states per centimeter squared. Reasonable values for NFS range from 1e10 to 1e12.

ASPEC Model, (UPDATE=1) — WIC=0

No weak inversion.

ASPEC Model, (UPDATE=1) — WIC=1

The vth threshold voltage increases by the fast term.

$$von = vth + fast$$

The following equation calculates the fast value used in the preceding equation:

$$fast = vt \cdot \left[1 + \frac{q \cdot NFS}{COX} + \frac{\gamma}{2 \cdot (vsb + PHI)^{1/2}} \right]$$

In the preceding equations, vt is the thermal voltage. The following equation specifies the ids current for $vgs < von$:

$$ids = ids(von, vde, vsb) \cdot e^{\frac{vgs - von}{fast}}$$

if $vgs < von$, then

$$ids = ids(vge, vde, vsb)$$

Note: Strong inversion conditions do not use the modified threshold voltage (von).

ASPEC Model, (UPDATE=1) — WIC=2

The subthreshold region is limited between the cutoff region and the strong inversion region. If the gate voltage is less than $vth - PHI$, this model cannot include any weak inversion conduction. However, this model can still include diffusion conduction from the drain-to-bulk rather than from the drain-to-source.

$$von = vth + fast$$

The following equation calculates the fast value used in the preceding equation:

Chapter 2: MOSFET Models

LEVEL 6: Lattin-Jenkins-Grove (ASPEC) Model

$$fast = vt \cdot \left[1 + \frac{q \cdot NFS}{COX} + \frac{\gamma}{2 \cdot (v_{sb} + PHI)^{1/2}} \right]$$

Cutoff Region, v_{gs} ≤ v_{th} - PHI

$$ids = 0$$

Weak Inversion, v_{th} - PHI < v_{gs} ≤ v_{on}

$$ids = ids(v_{on}, v_{de}, v_{sb}) \cdot \left(1 - \frac{v_{on} - v_{gs}}{fast + PHI} \right)^{WEX}$$

Strong Inversion, v_{gs} > v_{on}

$$ids = ids(v_{gs}, v_{de}, v_{sb})$$

Note: Strong inversion conditions do not use the modified threshold voltage (v_{on}).

ASPEC Model, (UPDATE=1) — WIC=3

If WIC=3, simulation calculates the subthreshold current differently. In this case, the ids current is:

$$ids = ids(v_{gs}, v_{de}, v_{sb}) + i_{sub}(N0eff, NDeff, v_{gs}, v_{ds})$$

N0eff and NDeff are functions of the effective device width and length.

ASPEC Model, (UPDATE=1) — Effective Mobility, ueff

All mobility equations have the following general form:

$$ueff = UO \cdot factor$$

| Parameter | Description |
|-----------|---|
| UEFF | Effective mobility at the specified a specified analysis temperature. |
| FACTOR | Mobility degradation factor. Default=1.0 |

Use the MOB model parameter to select the mobility modulation equation used in the Level 6 MOSFET model.

| Parameter | Description |
|-----------|---------------------------------|
| MOB=0 | No mobility reduction (default) |

| Parameter | Description |
|-----------|--|
| MOB=1 | Gm equation |
| MOB=2 | Frohman-Bentchkowski equation |
| MOB=3 | Normal field equation |
| MOB=4 | Universal field mobility reduction |
| MOB=5 | Universal field mobility reduction with an independent drain field |
| MOB=6 | Modified MOB=3 equations (lateral field effect included) |
| MOB=7 | Modified MOB=3 equations (lateral field effect not included) |

The following sections describe these equations.

ASPEC Model, (UPDATE=1) — MOB=0 Default, No Mobility

FACTOR=1.0 No mobility reduction

ASPEC Model, (UPDATE=1) — MOB=1

| Name (Alias) | Units | Default | Description |
|--------------|--------|---------|--|
| F1 | 1/V | 0.0 | Gate field mobility reduction |
| UTRA (F3) | factor | 0.0 | Source-drain mobility reduction factor |

Use the MOB=1 equation for transistors with constant source-to-bulk voltage, because the factor does not contain a vsb term. This equation sometimes over-estimates mobility for small gate voltages and large back-bias, such as depletion pull-ups.

$$factor = \frac{1}{1 + F1 \cdot (vgs - vb1 - F3 \Rightarrow vde)}$$

$$vde = \min(vds, vdsat)$$

Note: In the alternate saturation model, vde is different if UPDATE=0 than if UPDATE=1. See [ASPEC Model, \(UPDATE=1\) — Alternate DC Model \(ISPICE model\)](#). Also, if VMAX>0, then vde=min (vds, vsat). If you do not specify VMAX, then vde=min (vds, vdsat).

Chapter 2: MOSFET Models

LEVEL 6: Lattin-Jenkins-Grove (ASPEC) Model

ASPEC Model, (UPDATE=1) — MOB=2, Frohman-Bentchkowski Equation

| Name (Alias) | Units | Default | Description |
|--------------|--------|---------|--|
| F1 | V/cm | 0.0 | Critical gate-bulk electric field at which mobility reduction becomes significant. |
| UEXP (F2) | | 0.0 | Mobility exponent. Use a factor of 0.36 for n-channel and 0.15 for p-channel. |
| UTRA (F3) | factor | 0.0 | Source-drain mobility reduction factor. |
| VMAX (VMX) | cm/s | 0.0 | Maximum drift velocity of carriers. The VMAX setting determines which calculation scheme vdsat uses. Zero indicates an infinite value. |

The mobility reduction equation (MOB=2)[\[3\]](#) produces good results for high gate voltages and drain fields with constant back-bias. Typically, you can use this equation for p-channel pull-ups and n-channel pull-downs. The VMAX value selects the proper vdsat calculation scheme. MOB=2 (SPICE default) corresponds to MSINC UN=2.

$$factor = \left[\frac{F1 \cdot \epsilon_{si}}{COX \cdot (vgs - vbi - F3 \Rightarrow vde)} \right]^{F2}$$

vde is the same in this equation as in the MOB=1 equation.

ASPEC Model, (UPDATE=1) — MOB=3, Normal Field Equation

| Name (Alias) | Units | Default | Description |
|--------------|-------|---------|---|
| F1 | 1/V | 0.0 | Low-field mobility multiplier |
| F4 | | 1.0 | Mobility summing constant |
| UEXP (F2) | | 0.0 | Mobility exponent |
| UTRA (F3) | 1/V | 0.0 | High-field mobility multiplier |
| VF1 | V | 0.0 | Low to high field mobility (voltage switch) |

This equation is the same as MSINC UN=1:

$$(vgs - vth)^{F2}$$

$\leq VF1$:

$$factor = \frac{1}{F4 + F1 \cdot (vgs - vth)^{F2}}$$

If UPDATE=0, and $(vgs - vth)^{F2} > VF1$:

$$factor = \frac{1}{F4 + F3 \cdot (vgs - vth)^{F2}}$$

If UPDATE=1, 2 and $(vgs - vth)^{F2} > VF1$:

$$factor = \frac{1}{F4 + (F1 - F3) \cdot VF1 + F3 \cdot (vgs - vth)^{F2}}$$

ASPEC Model, (UPDATE=1) — MOB=4 or 5, Universal Field Mobility Reduction

| Name (Alias) | Units | Default | Description |
|--------------|--------------------|---------|---|
| ECRIT | V/cm | 0.0 | Critical electric drain field for mobility reduction. Zero indicates an infinite value. |
| F1 | V/cm | 0.0 | Source-drain mobility reduction field (typical values are 1e4 to 5e8). |
| MOB | | 0.0 | Selects a mobility equation: <ul style="list-style-type: none"> ■ Set MOB=4 for the critical field equation. ■ Set MOB=5 for the critical field equation with an independent drain field. |
| UEXP (F2) | 1/V ^{1/2} | 0.0 | Bulk mobility reduction factor (typical values are 0 to 0.5). |
| UTRA (F3) | V/cm | 0.0 | Critical electric drain field for mobility reduction. |

The MOB=4 equation is the same as the MSINC UN=3 equation.

ASPEC Model, (UPDATE=1) — MOB=5

The MOB=5 equation is the same as MOB=4, except that F3 substitutes for ECRIT in the vc expression.

The MOB=5 equation provides a better fit for CMOS devices in the saturation region. Do not specify a VMAX value, because the mobility equation calculates the velocity saturation.

$$factor = \frac{1}{1 + \frac{COX}{F1 \cdot \epsilon_{ox}} \cdot (vgs - cth) + \frac{vde}{vc} + F2 \cdot (vsb + PHI)^{1/2}}$$

Chapter 2: MOSFET Models

LEVEL 6: Lattin-Jenkins-Grove (ASPEC) Model

- If MOB=4, then

$$v_c = ECRIT \cdot L_{eff}$$

- If MOB=5, then

$$v_c = F3 \cdot L_{eff}$$

Note: If you use the alternate saturation model, vde is different for UPDATE=0 than it is for UPDATE=1, 2.

ASPEC Model, (UPDATE=1) — MOB=6 or 7, Modified MOB=3:

This mobility equation is the same as MOB=3, except that the equation uses VTO instead of vth. If you specify MOB=6, the following equation modifies the ids current:

$$ids = \frac{ids}{1 + F1 \cdot \left(vgs - vth - \frac{vde}{2} \right) + \frac{UTRA}{Leff} \cdot vde}$$

ASPEC Model, (UPDATE=1) — Channel Length Modulation

The basic MOSFET current equation for ids describes a parabola, where the peak corresponds to the drain-to-source saturation voltage (vdsat). Long-channel MOSFETs generally demonstrate ideal behavior. For vds voltages greater than vdsat, ids current does not increase. As channel length decreases, current in the saturation region continues to increase.

The simulator models this increase in current as a decrease in the effective channel length. Except for CLM=5 and 6, this model calculates the channel length modulation equations only when the device is in the saturation region.

The Level 6 MOSFET model provides several channel length modulation equations; all (except CLM=5) modify the ids equation:

$$ids = \frac{ids}{1 - \frac{\Delta L}{Leff}}$$

ΔL is the change in channel length due to MOSFET electric fields.

The CLM model parameter designates the channel length modulation equation for the Level 6 MOSFET device model:

| Parameter | Description |
|-----------|--|
| CLM=0 | No channel length modulation (default) |

| Parameter | Description |
|-----------|--|
| CLM=1 | One-sided step depletion layer drain field equation |
| CLM=2 | Frohman's electrostatic fringing field equation |
| CLM=3 | One-sided step depletion layer drain field equation with carrier velocity saturation |
| CLM=4 | Wang's equation: linearly graded depletion layer |
| CLM=5 | Synopsys channel length modulation |
| CLM=6 | Synopsys ΔL equations |

The following sections describe these equations and the associated model parameters.

ASPEC Model, (UPDATE=1) — CLM=0, No Channel Modulation—Default

$$\Delta L = 0$$

This is the default channel length equation, representing no channel length modulation; it corresponds to MSINC GDS=0 . 0.

ASPEC Model, (UPDATE=1) — CLM=1, Step Depletion Equation

| Name (Alias) | Units | Default | Description |
|------------------|---------------------|----------|---|
| KL | | 0.0 | Empirical constant (saturation voltage) |
| LAMBDA (LAM, LA) | cm/V ^{1/2} | 1.137e-4 | Channel length modulation. If you do not specify s, simulation calculates it from NSUB. The default LAMBDA corresponds to the default NSUB value. |

$$\Delta L = LAMBDA \cdot (vds - vdsat)^{1/2} \cdot \left(\frac{vdsat}{vsat} \right)^{KL}$$

If you do not specify LAMBDA, simulation calculates it as:

$$LAMBDA = \left(\frac{2 \cdot \epsilon si}{q \cdot DNB} \right)^{1/2}$$

This is a one-sided step depletion region formulation by Grove: ΔL varies with the depletion layer width, which is a function of the difference between the effective saturation voltage ($vdsat$) and the drain-to-source channel voltage

Chapter 2: MOSFET Models

LEVEL 6: Lattin-Jenkins-Grove (ASPEC) Model

(v_{ds}). Typically, you can use this equation for long channels and high dopant concentrations. This corresponds to GDS=1 in MSINC.

ASPEC Model, (UPDATE=1) — CLM=2, Electrostatic Fringing Field

| Name (Alias) | Units | Default | Description |
|--------------|-------|---------|--|
| A1 | | 0.2 | First fringing field factor, gate-drain |
| A2 | | 0.6 | Second fringing field factor, gate- v_{dsat} |

$$\Delta L = \frac{\epsilon si}{COX} \cdot \frac{v_{ds} - v_{dsat}}{A1 \cdot (v_{ds} - v_{gs} + v_{bi}) + A2 \cdot (v_{gs} - v_{bi} - v_{dsat})}$$

You can use the fringing field equation or electrostatic channel length reduction (developed by Frohman-Bentchkowski) to model short-channel enhancement transistors. In MSINC, the equivalent equation is GDS=2.

ASPEC Model, (UPDATE=1) — CLM=3, Carrier Velocity Saturation Equation

| Name (Alias) | Units | Default | Description |
|------------------|---------------------|----------|--|
| KA | | 1.0 | v_{ds} scaling factor for velocity saturation. |
| KCL | | 1.0 | Exponent for v_{sb} scaling factor. |
| KU | | 0.0 | Velocity saturation switch. If KU \leq 1, simulation uses the standard velocity saturation equation. |
| LAMBDA (LAM, LA) | cm/V ^{1/2} | 1.137e-4 | Channel length modulation. If you do not specify LAMBDA, simulation calculates it from NSUB. The default LAMBDA corresponds to the default NSUB value. |
| MAL | | 0.5 | v_{ds} exponent for velocity saturation. |
| MCL | | 1.0 | Short channel exponent. |

$$\Delta L = vfu^{(2 \cdot MCL)} \cdot LAMBDA$$

$$[(v_{ds} - v_{fa} \Rightarrow sat + KCL \cdot v_{sb} + PHI)^{1/2} - (KCL \cdot v_{sb} + PHI)^{1/2}]$$

This equation is an extension of the first depletion layer equation, CLM=1. It includes effects of carrier velocity saturation, and source-to-bulk voltage (v_{sb}) depletion layer width. It represents the basic ISPICE equation. See [ASPEC](#)

[Model, \(UPDATE=1\) — Alternate DC Model \(ISPICE model\)](#) for definitions of vfa and vfu.

ASPEC Model, (UPDATE=1) — CLM=4, Wang's Equation

| Name (Alias) | Units | Default | Description |
|--------------|------------------|---------|--|
| A1 | m | 0.2 | Junction depth: A1scaled=A1 · SCALM |
| DND | cm ⁻³ | 1e20 | Drain diffusion concentration |

Linearly Graded Depletion Layer:

$$\Delta L = \left[\frac{2.73e5 \cdot A1scaled}{DNB \cdot \ln\left(\frac{DND}{DNB}\right)} \right]^{1/3} \cdot [(vds - vdsat + PHI)^{1/3} - PHI^{1/3}]$$

Wang's equation can include junction characteristics to calculate the channel length modulation. The equation assumes that the junction approximates a linearly-graded junction, and provides a value of 0.33 for the exponent. This equation is similar to MSINC GDS=3.

ASPEC Model, (UPDATE=1) — CLM=5, Channel Length Modulation

| Name (Alias) | Units | Default | Description |
|--------------|--------------------|---------|----------------------|
| LAMBDA | amp/V ² | 0 | Constant coefficient |
| VGLAM | 1/V | 0 | Constant coefficient |

If CLM=5, the ids current increases by idssat:

$$idssat = \frac{w_{eff}}{L_{eff}} \cdot LAMBDA \cdot vds \cdot (vgs - vth) \cdot [1 + VGLAM \cdot (vgs - vth)]$$

$$ids = ids + idssat$$

Note: The equation adds the idssat term to ids in all regions of operation. Also, LAMBDA is a function of the temperature.

Chapter 2: MOSFET Models

LEVEL 6: Lattin-Jenkins-Grove (ASPEC) Model

ASPEC Model, (UPDATE=1) — CLM=6, ΔL Equation

| Name (Alias) | Units | Default | Description |
|--------------|-------------------|---------|----------------------------|
| LAMBDA | 1/V ^{KL} | 0 | vds coefficient |
| LAM1 | 1/m | 0 | Channel length coefficient |
| KL | | 0 | vds exponent |
| VGLAM | 1/V | 0 | Gate drive coefficient |

Unlike the other CLM values, this equation calculates the channel length modulation (ΔL) in all regions of operations, and uses it to modify the i_{ds} current.

$$\Delta L = \frac{Leff \cdot LAMBDA \cdot vds^{KL} \cdot [1 + VGLAM \cdot (vgs - vth)]}{1 + LAM1 \cdot Leff}$$

$$ids = \frac{ids}{1 - \frac{\Delta L}{Leff}}$$

Note: LAMBDA is a function of the temperature.

Lattin-Jenkins-Grove (ASPEC) Model — Compatibility Notes

To make MOSFET models compatible with ASPEC, specify ASPEC=1 in the .OPTION statement and LEVEL=6 in the associated MOSFET model statement.

If you assign the element parameters without keynames, specify the parameters in the same sequence as in the general format. The Level 6 MOSFET model assigns parameters in the order that you list them in the element statement. If parameter names are also element keynames, simulation reports errors.

If you use the ASPEC option, several program variations occur. The LEVEL model parameter is set to 6.

Note: Setting LEVEL=6 in the model does not invoke ASPEC.

| | |
|-------------------------|------------|
| MOSFET control option | WL=1 |
| General control options | SCALE=1e-6 |
| | SCALM=1e-6 |

ASPEC sets the SCALE and SCALM options so it effectively changes the default units in parameters that these options affect. Parameter values must be consistent with these scaling factors.

| | | |
|-------|---|------------------------------------|
| LEVEL | = | 6 |
| ACM | = | 1 |
| CJ | = | 0.0 |
| IS | = | 0.0 |
| NSUB | = | 1e15 |
| PHI | = | 1 . Φ_f (the Fermi potential) |
| TLEV | = | 1 |
| TLEVC | = | 1 |

Note: Do not calculate NSUB from GAMMA, if UPDATE=1 or 2.

TLEV (TLEVC) selects the ASPEC method of updating temperatures for the CJ, CJSW, PB, PHP, VTO, and PHI parameters.

Note: If you explicitly enter PHI, this model does not update it for temperature. SCALM does not affect how simulation scales parameters for the ASPEC mode. If you specify SCALM when you use ASPEC, the Level 7 MOSFET model generates an error stating that it ignores SCALM.

LEVEL 7: Lattin-Jenkins-Grove (SPICE) Model

The LEVEL 7: Lattin-Jenkins-Grove (SPICE) Model is the same as [LEVEL 6: Lattin-Jenkins-Grove \(ASPEC\) Model](#) except for the PHI value. The only difference between the two is the equations that handle the parasitic elements and the method of temperature compensation.

If you specify PHI, then:

For LEVEL=6

$$\Phi_s = \frac{PHI}{2}, \text{ where } \Phi_s^2$$

is the surface potential.

For LEVEL=7

$$\Phi_s = PHI$$

To transform a LEVEL 7 equation to LEVEL 6, make the following substitution:

$$PHI \rightarrow 2 \cdot PHI$$

To transform a LEVEL 6 model into a LEVEL 7 model, make the following substitution:

$$PHI(Level\ 7) = PHI(Level\ 6)/\ 2$$

LEVEL 8: Advanced LEVEL 2: MOS2 Grove-Frohman Model (SPICE 2G)

This model is derived from research at Intersil and General Electric, is an enhanced version of the [LEVEL 2: MOS2 Grove-Frohman \(SPICE 2G\) Model](#). LEVEL 2 differs from LEVEL 8 in the following areas:

- effective substrate doping
- threshold voltage
- effective mobility
- channel length modulation
- subthreshold current.

This section covers the following topics:

- [Advanced LEVEL 2: MOS2 Grove-Frohman \(SPICE 2G\) Model Parameters](#)
 - [Advanced LEVEL 2: MOS2 Grove-Frohman \(SPICE 2G\) — Model Equations](#)
-

Advanced LEVEL 2: MOS2 Grove-Frohman (SPICE 2G) Model Parameters

This model uses the generic MOSFET model parameters described in [Common MOSFET Model Parameters](#) section. In addition, this level also uses the following parameters:

| Name (Alias) | Units | Default | Description |
|------------------|-------|---------|---|
| A1 | | 0.2 | Channel length modulation exponent (CLM=8) |
| CLM | | 7 | Channel length modulation equation selector |
| LAM1 | 1/m | 0.0 | Channel length modulation length correction |
| LAMBDA (LAM, LA) | | 0.0 | Channel length modulation coefficient |

Advanced LEVEL 2: MOS2 Grove-Frohman (SPICE 2G)

— Model Equations

This section covers the following topics:

- Advanced LEVEL 2 Model — IDS Equations
- Advanced LEVEL 2 Model — Effective Channel Length and Width
- Advanced LEVEL 2 Model — Effective Substrate Doping, nsub
- Advanced LEVEL 2 Model — Threshold Voltage, vth
- Advanced LEVEL 2 Model — Saturation Voltage vdsat
- Advanced LEVEL 2 Model — ECRIT > 0:
- Advanced LEVEL 2 Model — ECRIT ≤ 0 or MOB=7:
- Advanced LEVEL 2 Model — Effective Mobility, ueff
- Advanced LEVEL 2 Model — MOB=2 Mobility Reduction
- Advanced LEVEL 2 Model — MOB=3 Mobility Reduction
- Advanced LEVEL 2 Model — MOB=6 Mobility Reduction
- Advanced LEVEL 2 Model — MOB=7 Mobility Reduction
- Advanced LEVEL 2 Model — Channel Length Modulation
- Advanced LEVEL 2 Model — CLM=6, SPICE Channel Length Modulation
- Advanced LEVEL 2 Model — CLM=7, Intersil Channel Length Modulation
- Advanced LEVEL 2 Model — CLM=8
- Advanced LEVEL 2 Model — Subthreshold Current Ids

Advanced LEVEL 2 Model — IDS Equations

The ids equations are the same as that of [LEVEL 2: MOS2 Grove-Frohman \(SPICE 2G\) Model](#).

Advanced LEVEL 2 Model — Effective Channel Length and Width

This model calculates the effective channel length and width from the drawn length and width. See [Grove-Frohman \(SPICE 2G\) Model Equations](#).

Advanced LEVEL 2 Model — Effective Substrate Doping, nsub

The SNVB model parameter varies the substrate doping concentration linearly as a function of vsb:

$$nsub = NSUB + SNVB \cdot vsb$$

The preceding equation computes γ , ϕ , and xd parameters for nsub:

$$\gamma = \frac{\sqrt{2 \cdot \epsilon_{si} \cdot q \cdot nsub}}{COX}$$

$$\Phi = 2 \cdot vt \cdot \ln\left(\frac{nsub}{ni}\right)$$

$$xd = \sqrt{\frac{2 \cdot \epsilon_{si}}{q \cdot nsub}}$$

If SNVB is zero, then $\gamma = \text{GAMMA}$. You can adjust the γ value for the short-channel effect the same way as in the LEVEL 2 model. NSUB calculates the ϕ value.

Advanced LEVEL 2 Model — Threshold Voltage, vth

ETA specifies the threshold voltage reduction due to the potential barrier lowering effect.

$$vbi = VTO - g \Rightarrow \Phi - \frac{8.14e-22 \cdot ETA}{COX \cdot L_{eff}^3} Pvds + (\eta - 1) \cdot (v_{sb} + \Phi)$$

$$vth = vbi + g \cdot \sqrt{v_{sb} + \Phi}$$

Modify γ for the short-channel effect, the same as in the LEVEL 2 model to obtain the effective γ .

Advanced LEVEL 2 Model — Saturation Voltage vdsat

Level 8 computes the vsat saturation voltage the same way as in the LEVEL 2 model. This model includes the carrier velocity effect only if ECRIT is greater than zero.

Advanced LEVEL 2 Model — ECRIT > 0:

$$vdsat = vsat + vc - \sqrt{vsat^2 + vc^2}$$

The following equation calculates the vc value used in the preceding equation:

$$vc = ECRIT \cdot L_{eff}$$

Advanced LEVEL 2 Model — ECRIT ≤ 0 or MOB=7:

$$vdsat = vsat$$

This model computes vsat as in the LEVEL=2 model (see [Grove-Frohman \(SPICE 2G\) Model — Saturation Voltage, v_{dsat}](#)).

Chapter 2: MOSFET Models

LEVEL 8: Advanced LEVEL 2: MOS2 Grove-Frohman Model (SPICE 2G)

Advanced LEVEL 2 Model — Effective Mobility, u_{eff}

The MOB mobility equation selector controls the mobility reduction equations. In the LEVEL 8 model, set MOB to 2, 3, 6, or 7. Default=6.

Advanced LEVEL 2 Model — MOB=2 Mobility Reduction

$$u_{eff} = UO \cdot \left[\frac{\epsilon_{se} \cdot UCRIT}{COX \cdot (vgs - vth - UTRA \Rightarrow vde)} \right]^{UEXP}$$

Advanced LEVEL 2 Model — MOB=3 Mobility Reduction

$$u_{eff} = \frac{UO}{1 + \frac{2.1e-8 \cdot (vgs + vth + egfet - \Phi)}{6 \cdot TOX}}$$

In the preceding equation, $egfet$ is the silicon energy gap at the analysis temperature:

$$egfet = 1.16 - \frac{7.02e-4 \cdot t^2}{t + 1108}$$

In the preceding equation, t is the temperature in degrees Kelvin.

If $VMAX > 1$:

$$u_{eff} = \frac{u_{eff}}{1 + \frac{u_{eff}}{VMAX \cdot L_{eff}} \cdot vde}$$

Advanced LEVEL 2 Model — MOB=6 Mobility Reduction

For $UEXP > 0$:

$$\text{If } (vgs - vth) > \frac{\epsilon_{si} \cdot UCRIT}{COX}, \text{ then } u_{eff} = \frac{UO \cdot \left[\frac{\epsilon_{si} \cdot UCRIT}{COX \cdot (vgs - vth)} \right]^{UEXP}}{1 + \frac{UTRA}{L_{eff}} \cdot vde}$$

$$\text{Otherwise, } u_{eff} = \frac{UO}{1 + \frac{UTRA}{L_{eff}} \cdot vde}$$

For $UEXP = 0$:

$$u_{eff} = \frac{UO}{[1 + UCRIT \cdot (vgs - vth)] \cdot \left(1 + \frac{UTRA}{L_{eff}} \cdot vde\right)}$$

UCRIT for UEXP=0 has a dimension of (1/V).

Advanced LEVEL 2 Model — MOB=7 Mobility Reduction

$$u_{eff} = \frac{UO}{1 + UTRA \cdot \left(vgs - vbi - \eta \Rightarrow \frac{vde}{2} + \frac{body}{vde}\right)}$$

The following equation calculates the body value used in the preceding equation:

$$body = \frac{2}{3} \cdot \gamma \cdot [(vde + vsb + \Phi)^{3/2} - (vsb + \Phi)^{3/2}]$$

Advanced LEVEL 2 Model — Channel Length Modulation

The CLM equation selector controls the channel length modulation equations. In the LEVEL 8 model, set CLM to 6, 7, or 8. Default=7.

Advanced LEVEL 2 Model — CLM=6, SPICE Channel Length Modulation

If LAMBDA=0:

$$\lambda = \frac{xd}{leff \cdot vds} \cdot \sqrt{\frac{vds - vdsat}{4} + \sqrt{1 + \left(\frac{vds - vdsat}{4}\right)^2}}$$

$$\text{Otherwise, } \lambda = LAMBDA. \text{ Then: } \Delta L = \frac{\lambda \cdot L_{eff} \cdot vds}{1 + LAM1 \cdot L_{eff}}$$

Note: The LEVEL 2 model has no LAM1 term.

This model modifies the current for the channel length modulation effect in the entire regions:

$$ids = \frac{ids}{1 - \frac{\Delta L}{L_{eff}}}$$

Advanced LEVEL 2 Model — CLM=7, Intersil Channel Length Modulation

If CLM=7, this model computes ΔL only for the saturation region.

$$vds > vdsat$$

Chapter 2: MOSFET Models

LEVEL 8: Advanced LEVEL 2: MOS2 Grove-Frohman Model (SPICE 2G)

$$\Delta L = \frac{LAMBDA \cdot L_{eff}}{1 + LAM1 \cdot L_{eff}} \cdot (vds - vdsat)$$

$$ids = \frac{ids}{L - \frac{\Delta L}{L_{eff}}}$$

Advanced LEVEL 2 Model — CLM=8

If CLM=8, this model computes ΔL only for the saturation region.

$vds > vdsat$

$$\Delta L = \frac{L_{eff}}{1 + \frac{(1 + LAM1 \cdot L_{eff}) \cdot (1 + vde)^{A1}}{LAMBDA \cdot (vds - vde)}}$$

$$ids = \frac{ids}{1 - \frac{\Delta L}{L_{eff}}}$$

Advanced LEVEL 2 Model — Subthreshold Current Ids

The LEVEL 8 model has different subthreshold current equations, depending on the value of the CAV model parameter.

Define:

$$fast = vt \cdot \left[\eta + \frac{q \cdot NFS}{COX} + \frac{\gamma}{2 \cdot (vsb + \Phi)^{1/2}} + \frac{\epsilon_{si} \cdot q \cdot SNVB \cdot \sqrt{vsb + \Phi}}{\gamma \cdot COX^2} \right]$$

For CAV ≠ 0

$$von = vth + CAV \cdot fast$$

Subthreshold Region, $vgs < von$

If $vgs > vth$:

$$ids = ids(von, vde, vsb) \cdot e^{\left(-1 - \frac{CAV}{2}\right)} \cdot e^{\left\{ \left[\frac{1}{fast} - \frac{(CAV - 2) \cdot (vgs - vth)}{2 \cdot CAV^2 \cdot fast^2} \right] (vgs - vth) \right\}}$$

If $vgs \leq vth$

$$ids = ids(von, vde, vsb) \cdot e^{\left(-1 - \frac{CAV}{2}\right)} \cdot e^{\left(\frac{vgs - vth}{fast}\right)}$$

For CAV=0

If CLM=8: $v_{on} = v_{th} + 3 \cdot fast$

Otherwise, $v_{on} = v_{th} + 2 \cdot fast$

Subthreshold Region, $v_{gs} < v_{on}$

$$ids = ids(v_{on}, v_{de}, v_{sb}) \cdot e^{\left(\frac{v_{gs} - v_{on}}{fast}\right)}$$

If WIC=3, the next equation calculates the ids subthreshold current:

$$ids = ids(v_{gs}, v_{de}, v_{sb}) + i_{sub}(N0eff, NDeff, v_{gs}, v_{ds})$$

$N0eff$ and $NDeff$ are functions of effective device width and length.

LEVEL 13: BSIM Model

This model is based on the SPICE 2G.6 BSIM model, which models the device physics of small-geometry MOS transistors. To invoke the subthreshold region, set the `N0` model parameter (low field weak inversion gate drive coefficient) to less than 200. This model provides the following MOSFET models:

- Wire (resistor) model, compatible with the SPICE BSIM interconnect model for polysilicon and metal layers. Simulates resistors and capacitors with interconnects.
- Capacitor model. Simulates only capacitors with interconnects.
- Diffusion model, compatible with SPICE BSIM diffusion models.

To set the model parameters, either:

- Enter model parameters as numbers (as in SPICE), or
- Assign the model parameters.

If you convert from SPICE to the Synopsys models, use the `S` keyletter for SPICE BSIM, or `M` for the Synopsys model. (see [BSIM Model—Compatibility Notes: IDS and VGS Curves for PMOS and NMOS](#)).

This section covers the following topics:

- [BSIM Model Features](#)
- [BSIM Model Parameters](#)
- [BSIM Model — Sensitivity Factors](#)
- [BSIM Models — .MODEL VERSION Changes](#)
- [BSIM Model Equations](#)
- [BSIM Model — Charge-Based Capacitance Model](#)
- [BSIM Model — Preventing Negative Output Conductance](#)
- [BSIM Model Calculations](#)
- [BSIM Model — Compatibility Notes](#)

BSIM Model Features

- Vertical field dependence of the carrier mobility
- Carrier velocity saturation

- Drain-induced barrier lowering
 - Depletion charge sharing by source and drain
 - Non-uniform doping profile for ion-implanted devices
 - Channel length modulation
 - Subthreshold conduction
 - Geometric dependence of electrical parameters
-

BSIM Model Parameters

This model uses the generic MOSFET model parameters described in [Common MOSFET Model Parameters](#) section. In addition, this model also uses the following parameters:

Note: When you read parameter names, be careful about the difference in appearance between the upper case letter O, the lower case letter o, and the number zero (0).

For reference purposes only, simulation obtains the following default values from a medium size n-channel MOSFET device.

To specify the model parameters, use NMOS conventions, even for PMOS (for example, `ETA0=0 . 02`, not `ETA0=-0 . 02`).

This section covers the following topics:

- [BSIM Model — Transistor Parameters](#)
- [BSIM Model — Diffusion Layer Parameters](#)
- [BSIM Model — Temperature Parameters](#)

BSIM Model — Transistor Parameters

| Name (Alias) | Units | Default | Description |
|---------------|-------|---------|--|
| LEVEL | | 1 | MOSFET model level selector. 13 is the BSIM model |
| CGBOM, (CGBO) | F/m | 2.0e-10 | Gate-to-bulk parasitic capacitance (F/m of length) |
| CGDOM, (CGDO) | F/m | 1.5e-9 | Gate-to-drain parasitic capacitance (F/m of width) |

Chapter 2: MOSFET Models

LEVEL 13: BSIM Model

| Name (Alias) | Units | Default | Description |
|---------------|---|---------|---|
| CGSOM, (CGSO) | F/m | 1.5e-9 | Gate-to-source parasitic capacitance (F/m of width) |
| DL0 | μm | 0.0 | Difference between drawn poly and electrical |
| DUM1 | | 0.0 | Dummy (not used) |
| DUM2 | | 0.0 | Dummy (not used) |
| DW0 | μm | 0.0 | Difference between drawn diffusion and electrical |
| ETA0 | | 0.0 | Linear vds threshold coefficient |
| K1 | $\text{V}^{1/2}$ | 0.5 | Root-vs _b threshold coefficient |
| K2 | | 0.0 | Linear vs _b threshold coefficient |
| LETA | mm | 0.0 | Length sensitivity |
| LK1 | $\text{V}^{1/2} \cdot \mu\text{m}$ | 0.0 | Length sensitivity |
| LK2 | μm | 0.0 | Length sensitivity |
| LMS (LMUS) | $\mu\text{m} \cdot \text{cm}^2 / (\text{V} \cdot \text{s})$ | 0.0 | Length sensitivity |
| LMUZ | $\mu\text{m} \cdot \text{cm}^2 / (\text{V} \cdot \text{s})$ | 0.0 | Length sensitivity |
| LN0 | | 0.0 | Length sensitivity |
| LNB | | 0.0 | Length sensitivity |
| LND | | 0.0 | Length sensitivity |
| LPHI | $\text{V} \cdot \mu\text{m}$ | 0.0 | Length sensitivity |
| LU0 | $\mu\text{m}/\text{V}$ | 0.0 | Length sensitivity |
| LU1 | $\mu\text{m}^2/\text{V}$ | 0.0 | Length sensitivity |
| LVFB | $\text{V} \cdot \mu\text{m}$ | 0.0 | Length sensitivity |
| LX2E | $\mu\text{m}/\text{V}$ | 0.0 | Length sensitivity |
| LX2M (LX2MZ) | $\mu\text{m} \cdot \text{cm}^2 / (\text{V}^2 \cdot \text{s})$ | 0.0 | Length sensitivity |

| Name (Alias) | Units | Default | Description |
|--------------|---|---------|---|
| LX2MS | $\mu\text{m} \cdot \text{cm}^2/(\text{V}^2 \cdot \text{s})$ | 0.0 | Length sensitivity |
| LX2U0 | $\mu\text{m}/\text{V}^2$ | 0.0 | Length sensitivity |
| LX2U1 | $\mu\text{m}^2/\text{V}^2$ | 0.0 | Length sensitivity |
| LX3E | $\mu\text{m}/\text{V}$ | 0.0 | Length sensitivity |
| LX3MS | $\mu\text{m} \cdot \text{cm}^2/(\text{V}^2 \cdot \text{s})$ | 0.0 | Length sensitivity |
| LX3U1 | $\mu\text{m}^2/\text{V}^2$ | 0.0 | Length sensitivity |
| MUS | $\text{cm}^2/(\text{V} \cdot \text{s})$ | 600 | High drain field mobility |
| MUZ | $\text{cm}^2/(\text{V} \cdot \text{s})$ | 600 | Low drain field first order mobility |
| N0 | | 0.5 | Low field weak inversion gate drive coefficient (a value of 200 for N0 disables the weak inversion calculation) |
| NB0 | | 0.0 | V _{sb} reduction to the low field weak inversion gate drive coefficient |
| ND0 | | 0.0 | V _{ds} reduction to the low field weak inversion gate drive coefficient |
| PHI0 | V | 0.7 | Two times the Fermi potential |
| TOXM, (TOX) | $\mu\text{m}, (\text{m})$ | 0.02 | Gate oxide thickness (simulation interprets TOXM or TOX >1 as Angstroms) |
| TREF | $^\circ\text{C}$ | 25.0 | Reference temperature of model (local override of TNOM) |
| U00 | 1/V | 0.0 | Gate field mobility reduction factor |
| U1 | $\mu\text{m}/\text{V}$ | 0.0 | Drain field mobility reduction factor |
| VDDM | V | 50 | Critical voltage for the high-drain field mobility reduction |
| VFB0 (VFB) | V | -0.3 | Flatband voltage |
| WETA | μm | 0.0 | Width sensitivity |
| WK1 | $\text{V}^{1/2} \cdot \mu\text{m}$ | 0.0 | Width sensitivity |

Chapter 2: MOSFET Models

LEVEL 13: BSIM Model

| Name (Alias) | Units | Default | Description |
|--------------|---|---------|--|
| WK2 | μm | 0.0 | Width sensitivity |
| WMS (WMUS) | $\mu\text{m} \cdot \text{cm}^2/(\text{V} \cdot \text{s})$ | 0.0 | Width sensitivity |
| WMUZ | $\mu\text{m} \cdot \text{cm}^2/(\text{V} \cdot \text{s})$ | 0.0 | Width sensitivity |
| WN0 | | 0.0 | Width sensitivity |
| WNB | | 0.0 | Width sensitivity |
| WND | | 0.0 | Width sensitivity |
| WPHI | $\text{V} \cdot \mu\text{m}$ | 0.0 | Width sensitivity |
| WU0 | $\mu\text{m}/\text{V}$ | 0.0 | Width sensitivity |
| WU1 | $\mu\text{m}^2/\text{V}$ | 0.0 | Width sensitivity |
| WVFB | $\text{V} \cdot \mu\text{m}$ | 0.0 | Width sensitivity |
| WX2E | $\mu\text{m}/\text{V}$ | 0.0 | Width sensitivity |
| WX2M (WX2MZ) | $\mu\text{m} \cdot \text{cm}^2/(\text{V}^2 \cdot \text{s})$ | 0.0 | Width sensitivity |
| WX2MS | $\mu\text{m} \cdot \text{cm}^2/(\text{V}^2 \cdot \text{s})$ | 0.0 | Width sensitivity |
| WX2U0 | $\mu\text{m}/\text{V}^2$ | 0.0 | Width sensitivity |
| WX2U1 | $\mu\text{m}^2/\text{V}^2$ | 0.0 | Width sensitivity |
| WX3E | $\mu\text{m}/\text{V}$ | 0.0 | Width sensitivity |
| WX3MS | $\mu\text{m} \cdot \text{cm}^2/(\text{V}^2 \cdot \text{s})$ | 0.0 | Width sensitivity |
| WX3U1 | $\mu\text{m}^2/\text{V}^2$ | 0.0 | Width sensitivity |
| X2E | $1/\text{V}$ | 0.0 | V _{sb} correction to the linear v _{ds} threshold coefficient |
| X2M (X2MZ) | $\text{cm}^2/(\text{V}^2 \cdot \text{s})$ | 0.0 | V _{sb} correction to the low field first-order mobility |
| X2MS | $\text{cm}^2/(\text{V}^2 \cdot \text{s})$ | 0.0 | V _{bs} reduction to the high-drain field mobility |

| Name (Alias) | Units | Default | Description |
|--------------|---------------------------------------|---------|--|
| X2U0 | 1/V ² | 0.0 | V _{sb} reduction to the GATE field mobility reduction factor |
| X2U1 | μm/V ² | 0.0 | V _{sb} reduction to the DRAIN field mobility reduction factor |
| X3E | 1/V | 0.0 | V _{ds} correction to the linear v _{ds} threshold coefficient |
| X3MS | cm ² /(V ² · s) | 5.0 | V _{ds} reduction to the high-drain field mobility |
| X3U1 | μm/V ² | 0.0 | V _{ds} reduction to the drain field mobility reduction factor |
| XPART | | 1.0 | Selects a gate capacitance charge-sharing coefficient |

BSIM Model — Diffusion Layer Parameters

| Name (Alias) | Units | Default | Description |
|--------------|------------------|---------|--|
| CJW, (CJSW) | F/m | 0.0 | Zero-bias bulk junction sidewall capacitance |
| CJM, (CJ) | F/m ² | 4.5e-5 | Zero-bias bulk junction bottom capacitance |
| DS | m | 0.0 | Average size variation due to the side etching or the mask compensation (not used) |
| IJS, (JS) | A/m ² | 0 | Bulk junction saturation current |
| JSW | A/m | 0.0 | Sidewall bulk junction saturation current |
| MJ0, (MJ) | | 0.5 | Bulk junction bottom grading coefficient |
| MJW, (MJSW) | | 0.33 | Bulk junction sidewall grading coefficient |
| PJ, (PB) | V | 0.8 | Bulk junction bottom potential |
| PJW, (PHP) | V | 0.8 | Bulk junction sidewall potential |
| RSHM, (RSH) | ohm/sq | 0.0 | Sheet resistance/square |
| WDF | m | 0.0 | Default width of the layer (not used) |

BSIM Model — Temperature Parameters

| Name (Alias) | Units | Default | Description |
|--------------|-------|---------|---|
| BEX | | -1.5 | Temperature exponent for the MUZ and MUS mobility parameters. |
| FEX | | 0.0 | Temperature exponent for the U1 mobility reduction factor. |
| TCV | V/K | 0.0 | Flat-band voltage temperature coefficient. |
| TREF | °C | 25 | Temperature at which simulation extracts parameters. This parameter defaults to the TNOM option, which defaults to 25 °C. |

BSIM Model — Sensitivity Factors

To denote the L (channel length) and w (channel width) sensitivity factors of a basic electrical parameter in a transistor, add L and w characters at the start of the name. For example, $VFB0$ sensitivity factors are $LVFB$ and $WVFB$. If $A0$ is a basic parameter, then LA and WA are the corresponding L and w sensitivity factors of this parameter. Do not use the SCALM option to scale LA and WA .

This model uses the following equation to obtain this parameter value:

$$A = A0 + LA \cdot \left(\frac{1}{Leff} - \frac{1}{LREFeff} \right) + WA \cdot \left(\frac{1}{Weff} - \frac{1}{WREFeff} \right)$$

Specify LA and WA in units of microns times the units of $A0$.

The left side of the equation represents the effective model parameter value after you adjust the device size. All effective model parameters are in lower case and start with the z character, followed by the parameter name.

Example:

$$VFB0 = -0.350\text{v}, LVFB = -0.1\text{v}\mu$$

$$WVFB = 0.08\text{v}\cdot\mu, Leff = 1 \cdot 10^{-6}\text{m} = 1\mu$$

$$Weff = 2 \cdot 10^{-6}\text{m} = 2\mu, LREFeff = 2 \cdot 10^{-6}\text{m} = 2\mu$$

$$WREFeff = 1 \cdot 10^{-5}\text{m} = 10\mu$$

$$zvfb = VFB0 + LVFB \cdot \left(\frac{1}{Leff} - \frac{1}{LREFeff} \right) + WVFB \cdot \left(\frac{1}{Weff} - \frac{1}{WREFeff} \right)$$

$$zvfb = -0.35v + -0.1v \cdot \mu \cdot \left(\frac{1}{1\mu} - \frac{1}{2\mu} \right) + 0.08v \cdot \mu \cdot \left(\frac{1}{2\mu} - \frac{1}{10\mu} \right)$$

$$zvfb = -0.35v - 0.05v + 0.032v, zvfb = -0.368v$$

BSIM Models — .MODEL VERSION Changes

You can use the VERSION parameter in the .MODEL statement to move LEVEL 13: BSIM and LEVEL 39: BSIM2 models between versions. Using the VERSION parameter in a LEVEL 13 .MODEL statement results in the following changes to the BSIM model.

| Model Version | Effect of VERSION on BSIM model |
|---------------|---|
| 9007B | Introduced the LEVEL 13 BSIM model: no changes |
| 9007D | Removed the K2 limit |
| 92A | Changed the TOX parameter default from 1000 A to 200 A |
| 92B | Added the K2LIM parameter, which specifies the K2 limit |
| 93A | Introduced the gds constraints |
| 93A.02 | Introduced the VERSION parameter |
| 95.1 | Fixed the nonprinting TREF and incorrect GMBS problems |
| 96.1 | Changed the flatband voltage temperature adjustment |

BSIM Model Equations

This section covers the following topics:

- [BSIM Model — Effective Channel Length and Width](#)
- [BSIM Model — IDS Equations](#)
- [BSIM Model — Cutoff Region, \$v_{gs} \leq v_{th}\$](#)
- [BSIM Model — On Region, \$v_{gs} > v_{th}\$](#)

Chapter 2: MOSFET Models

LEVEL 13: BSIM Model

- BSIM Model — Threshold Voltage
- BSIM Model — Saturation Voltage (v_{dsat})
- BSIM Model — i_{ds} Subthreshold Current
- BSIM Model — Resistors and Capacitors Generated with Interconnects
- BSIM Model — Resistances
- BSIM Model — Capacitances
- BSIM Model — Temperature Effect

BSIM Model — Effective Channel Length and Width

The effective channel length and width for Level 13 depends on the specified model parameters.

If you specify $DL0$, then:

$$L_{eff} = L_{scaled} \cdot LMLT - DL0 \Rightarrow e-6$$

$$LREF_{eff} = LREF_{scaled} \cdot LMLT - DL0 \Rightarrow e-6$$

Otherwise, if you specify XL or LD :

$$L_{eff} = L_{scaled} \cdot LMLT + XL_{scaled} - 2 \Rightarrow LD_{scaled}$$

$$LREF_{eff} = LREF_{scaled} \cdot LMLT + XL_{scaled} - 2 \Rightarrow LD_{scaled}$$

If you specify $DW0$, then:

$$W_{eff} = W_{scaled} \cdot WMLT - DW0 \Rightarrow e-6$$

$$WREF_{eff} = WREF_{scaled} \cdot WMLT - DW0 \Rightarrow e-6$$

Otherwise, if you specify XW or WD , then:

$$W_{eff} = W_{scaled} \cdot WMLT + XW_{scaled} - 2 \Rightarrow WD_{scaled}$$

$$WREF_{eff} = WREF_{scaled} \cdot WMLT + XW_{scaled} - 2 \Rightarrow WD_{scaled}$$

BSIM Model — IDS Equations

Process-oriented model parameters model the device characteristics.

Simulation maps these parameters into model parameters at a specific bias voltage. The i_{ds} equations are as follows:

BSIM Model — Cutoff Region, $v_{gs} \leq v_{th}$

$i_{ds} = 0$ (See BSIM Model — i_{ds} Subthreshold Current)

BSIM Model — On Region, vgs >vth

For the vds<vdsat triode region:

$$ids = \frac{\beta}{1 + xu1 \cdot vds} \cdot \left[(vgs - vth) \cdot vds - \frac{body}{2} \Rightarrow vds^2 \right]$$

For the vds>vdsat saturation region:

$$ids = \frac{\beta}{2 \cdot body \cdot arg} \cdot (vgs - vth)^2$$

The following equations calculate values used in the preceding equation:

$$\beta = ueff \cdot COX \cdot \frac{Weff}{Leff}$$

$$ueff = \frac{uo}{1 + xu0 \cdot (vgs - vth)}$$

$$xu0 = zu0 - zx2u0 \text{ Pvsb}$$

Simulation uses quadratic interpolation, through three data points to calculate the uo carrier mobility.

$$uo|_{vds=0} = MUZ - zx2mz \text{ Pvsb}$$

$$uo|_{vds=VDDM} = zmus - zx2ms \text{ Pvsb}$$

Simulation also calculates the sensitivity of uo to vds at $vds=VDDM$, which is $zx3ms$.

The following equation calculates the body factor:

$$body = 1 + \frac{g \cdot zk1}{2 \cdot (zphi + vsb)^{1/2}}$$

The following equation calculates the g value used in the preceding equation:

$$g = 1 - \frac{1}{1.744 + 0.8364 \cdot (zphi + vsb)}$$

The following equation calculates the arg term in the saturation region:

$$arg = \frac{1}{2} \cdot [1 + vc + (1 + 2 \cdot vc)^{1/2}]$$

The following equations calculate values used in the preceding equation:

Chapter 2: MOSFET Models

LEVEL 13: BSIM Model

$$v_c = \frac{xu1 \cdot (vgs - vth)}{body}$$

$$xu1 = zu1 - zx2u1 \Rightarrow sb + zx3u1 \cdot (vds - VDDM), \text{ UPDATE}=2$$

$$xu1 = \frac{zu1 - zx2u1 \Rightarrow sb + zx3u1 \cdot (vds - VDDM)}{Leff}, \text{ UPDATE}=0, 1$$

BSIM Model — Threshold Voltage

You can express the threshold voltage as:

$$vth = zvfb + zphi + gamma \cdot (zphi + vsb)^{1/2} - xeta \Rightarrow vds$$

The following equations calculate values used in the preceding equation:

$$gamma = zk1 - zk2 = (zphi + vsb)^{1/2}$$

$$xeta = zeta - zx2e \Rightarrow sb + zx3e \cdot (vds - VDDM), \text{ UPDATE}=0, 2$$

$$xeta = zeta + zx2e \cdot (zphi + vsb) + zx3e \cdot (vds - VDDM), \text{ UPDATE}=1$$

BSIM Model — Saturation Voltage (vdsat)

The following equation calculates the saturation voltage in the BSIM Level 13 model:

$$vdsat = \frac{vgs - vth}{body \cdot arg^{1/2}}$$

BSIM Model — ids Subthreshold Current

Simulation calculates the isub subthreshold current if zn0 is less than 200:

$$isub = \frac{Il_{lim} \cdot I_{exp}}{Il_{lim} + I_{exp}}$$

The following equations calculate values used in the preceding equation:

$$I_{exp} = \beta_o \cdot vt^2 \cdot e^{1.8} \cdot e^{\frac{vgs - vth}{xn \cdot vt}} \cdot \left(1 - e^{-\frac{vds}{vt}}\right)$$

$$Il_{lim} = 4.5 \cdot \beta_o \cdot vt^2, \beta_o = uo \cdot COX \cdot \frac{Weff}{Leff}$$

$$xn = zn0 - znb \Rightarrow vsb + znd \cdot vds$$

Simulation also adds the isub current to the ids current in the strong inversion.

BSIM Model — Resistors and Capacitors Generated with Interconnects

Refer to the wire model table (resistor element) for the model parameters that you used. For an example, see [BSIM Model—Compatibility Notes: IDS and VGS Curves for PMOS and NMOS](#).

BSIM Model — Resistances

$$r = RSH \cdot \frac{L_{eff}}{W_{eff}}$$

BSIM Model — Capacitances

$$c = COX \cdot L_{eff} \cdot W_{eff} + 2 \cdot CAPSW \cdot (L_{eff} + W_{eff})$$

BSIM Model — Temperature Effect

$$MUZ(t) = MUZ \cdot \left(\frac{t}{tnom} \right)^{BEX}, \text{ UPDATE}=0, 1$$

$$zmus(t) = zmus \cdot \left(\frac{t}{tnom} \right)^{BEX} \text{ UPDATE}=0, 1$$

$$uo(t) = uo \left(\frac{t}{tnom} \right)^{BEX}, \text{ UPDATE}=2$$

$$xu1(t) = xu1 \cdot \left(\frac{t}{tnom} \right)^{FEX}$$

$$zvfb(t) = zvfb - \Delta t \Rightarrow TCV$$

The following equation calculates the Δt value used in the preceding equations:

$$\Delta t = t - tnom$$

BSIM Model — Charge-Based Capacitance Model

The Level 13 capacitance model conserves charge and has nonreciprocal attributes. Using charge as the state variable guarantees charge conservation. To obtain the total stored charge in each of the gate, bulk, and channel regions, integrate the distributed charge densities/area of the active region.

The XPART 40/60 model parameter or 0/100 in the saturation region, partitions the channel charge into drain and source components. This partitioning smoothly changes to 50/50 in the triode region.

Chapter 2: MOSFET Models

LEVEL 13: BSIM Model

- XPART=0 selects 40/60 drain/source charge-partitioning in the saturation region. That is, 40% of the channel charge in the saturation region is at the drain, and 60% is at the source.
- XPART=1 selects 0/100 for drain/source charge-partitioning in the saturation region. That is, 100% of the channel charge in the saturation region is at the source; there is no drain charge.
- XPART=0.5 selects 50/50 partitioning. Half of the channel charge in the saturation region is at the source, and half is at the drain.

Define:

$$vtho = zvfb + zphi + zk1 \cdot (zphi + vsb)^{1/2}$$

$$cap = COX \cdot Leff \cdot Weff, vpo = \frac{vgs - vtho}{body}$$

$$argx = \frac{body \cdot vds}{12 \cdot (vgs - vtho - 0.5)}$$

$$\text{If } (vgs - vtho - 0.5) \leq e-8 \text{ then: } argx = \frac{1}{6}$$

$$argy = \frac{(vgs - vtho)^2 - 0.75}{6 \cdot (vgs - vtho - 0.5)} + 0.15 \cdot body^2 \cdot vds^2$$

$$\text{If } (vgs - vtho - 0.5) \leq e-8 \text{ then: } argy = \frac{4}{15}$$

This section covers the following topics:

- BSIM Model—Regions Charge Expressions: Accumulation Region, $vgs \leq vtho$, $vgs \leq zvfb - vsb$
- BSIM Model—Regions Charge Expressions: Subthreshold Region, $vgs \leq vtho$, $vgs > zvfb - vsb$
- BSIM Model—Regions Charge Expressions: 50/50 Channel-Charge Partitioning for Drain and Source, XPART=.5; Triode Region, $vgs > vtho$, $vds \leq vpo$
- BSIM Model—Regions Charge Expressions: Saturation Region, $vgs > vtho$, $vds > vpo$
- BSIM Model—Regions Charge Expressions: 40/60 Channel-Charge Partitioning for Drain and Source, XPART=0; Triode Region, $vgs > vtho$, $vds \leq vpo$

- BSIM Model—Regions Charge Expressions: Saturation Region, $vgs > vtho$, $vds > vpof$
- BSIM Model—Regions Charge Expressions: 0/100 Channel-Charge Partitioning for Drain and Source, XPART=1; Triode Region, $vgs > vtho$, $vds \leq vpof$
- BSIM Model—Regions Charge Expressions: Saturation Region, $vgs > vtho$, $vds > vpof$

BSIM Model—Regions Charge Expressions: Accumulation Region, $vgs \leq vtho$, $vgs \leq zvfb - vsb$

$$Qg = cap \cdot (vgs - zvfb + vsb)$$

$$Qb = -qg, Qs = 0, Qd = 0$$

BSIM Model—Regions Charge Expressions: Subthreshold Region, $vgs \leq vtho$, $vgs > zvfb - vsb$

$$Qg = \frac{cap \cdot zk1}{2} \cdot \left\{ [(zk1)^2 + 4(vgs - zvfb + vsb)]^{1/2} - zk1 \right\}$$

$$Qb = -qg, Qs = 0$$

BSIM Model—Regions Charge Expressions: 50/50 Channel-Charge Partitioning for Drain and Source, XPART=.5; Triode Region, $vgs > vtho$, $vds \leq vpof$

$$Qg = cap \cdot (vgs - zvfb - zphi - 0.5 \Rightarrow ds + vds \cdot argx)$$

$$Qb = cap \cdot [-vtho + zvfb + zphi + (1 - body) \cdot (0.5 - argx) \cdot vds]$$

$$Qd = -0.5 \Rightarrow (qg + qb), Qs = Qd$$

BSIM Model—Regions Charge Expressions: Saturation Region, $vgs > vtho$, $vds > vpof$

$$Qg = cap \cdot \left(vgs - zvfb - zphi - \frac{vgs - vtho}{3 \cdot body} \right)$$

$$Qb = cap \cdot \left[zvfb + zphi - vtho + (1 - body) \cdot \frac{(vgs - vtho)}{3 \cdot body} \right]$$

$$Qd = -\frac{cap}{3} \Rightarrow (vgs - vtho), Qs = Qd$$

Chapter 2: MOSFET Models

LEVEL 13: BSIM Model

BSIM Model—Regions Charge Expressions: 40/60 Channel-Charge Partitioning for Drain and Source, XPART=0; Triode Region, vgs >vtho, vds £ vpof

$$Qg = cap \cdot (vgs - xvfb - zphi - 0.5 \Rightarrow vds + argx \cdot vds)$$

$$Qb = cap \cdot [-vtho + zvfb + zphi + (1 - body) \cdot (0.5 - argx) \cdot vds]$$

$$Qd = -(cap \cdot [0.5 \cdot (vgs - vtho - body \Rightarrow vds) + body \cdot argy \cdot vds])$$

$$Qs = -(Qg + Qb + Qd)$$

BSIM Model—Regions Charge Expressions: Saturation Region, vgs>vtho, vds >vpof

$$Qg = cap \cdot \left(vgs - zvfb - zphi - \frac{vgs - vtho}{3 \cdot body} \right)$$

$$Qb = cap \cdot \left[zvfb + zphi - vtho + (1 - body) \cdot \frac{(vgs - vtho)}{3 \cdot body} \right]$$

$$Qd = -\frac{4 \cdot cap}{15} \cdot (vgs - vtho), Qs = \frac{3}{2} \cdot Qd$$

BSIM Model—Regions Charge Expressions: 0/100 Channel-Charge Partitioning for Drain and Source, XPART=1; Triode Region, vgs >vtho, vds £ vpof

$$Qg = cap \cdot (vgs - zvfb - zphi - 0.5 \mathbb{P} vds + vds \cdot argx)$$

$$Qb = cap \cdot [-vtho + zvfb + zphi + (1 - body) \cdot (0.5 - argx) \cdot vds]$$

$$Qd = -(cap \cdot [0.5 \cdot (vgs - vtho) - body \mathbb{P} vds \mathbb{P} (0.75 - 1.5 \mathbb{P} argx)])$$

$$Qs = -(Qg + Qb + Qd)$$

BSIM Model—Regions Charge Expressions: Saturation Region, vgs >vtho, vds >vpof

$$Qg = cap \cdot \left(vgs - zvfb - zphi - \frac{vgs - vtho}{3 \cdot body} \right)$$

$$Qb = cap \cdot \left[zvfb + zphi - vtho + (1 - body) \cdot \frac{(vgs - vtho)}{3 \cdot body} \right]$$

$$Qd = 0, Qs = -Qg - Qb$$

BSIM Model — Preventing Negative Output Conductance

The Level 13 model internally protects against conditions that might cause convergence problems, due to negative output conductance. The constraints imposed are:

$$ND \geq 0$$

$$MUS \geq MUZ + X3MS + VDD(M/2)$$

This model imposes these constraints after adjusting the length and width and setting the *V_{BS}* dependence. This feature loses some accuracy in the saturation region, particularly at high *V_{gs}*.

You might need to qualify BSIM1 models again, if the following occur:

- Devices exhibit self-heating during characterization, which causes declining *I_{ds}* at high *V_{ds}*. This does not occur if the device characterization measurement sweeps *V_{ds}*.
- Extraction produces parameters that result in negative conductance.
- This model attempts voltage simulation outside the characterized range of the device.

BSIM Model Calculations

To verify the equations, start some simple simulation and analysis tests, and check the results with a hand calculator. Check the threshold, *v_{dsat}*, and *i_{ds}* for a very simple model with many parameters set to zero:

- series resistance, *R_{SH}*=0.
- Turn off diode current, *J_S*=*J_{SW}*=*I_S*=0.
- Turn off the Level 13 subthreshold current, *n₀*=200.
- Set the geometry parameters to zero so *L_{eff}*=*L*=1u, *W_{eff}*=*W*=1u.

This test returns the following *T_{OX}* value:

$$cox = \frac{2.00000e-3F}{m^2}$$

Chapter 2: MOSFET Models

LEVEL 13: BSIM Model

The test is at $v_{bs}=-0.35$ so that $\phi-v_{bs}=1.0$. The netlist for this test is located in directory $\$installdir/demo/hspice/mos/t1.sp$.

```
$ t1
.option ingold=2 numdgt=6
vd d 0 5
vg g 0 5
vb b 0 -0.35
m1 d g 0 b nch w=10u L=1u
.dc vd 4 5 1
.print ids=LX4(m1) vth=lv9(m1) vdsat=lv10(m1)
.model nch nmos LEVEL=13
+ vfb0=-0.4 lvfb=0 wvfb=0
+ phi0=0.65 lphi=0 wphi=0
+ k1=0.5 lk1=0 wk1=0
+ k2=0 lk2=0 wk2=0
+ eta0=1e-3 leta=0 weta=0
+ muz=600 mus=700 x3ms=10
+ xl=0 ld=0 xw=0 wd=0
+ u00=0 lu0=0 wu0=0
+ u1=0 lul=0 wu1=0
+ tox=172.657
+ acm=2 rsh=0 js=0 jsw=0 is=0 n0=200
.end
```

Simulation Results

| | | |
|-------------|-------------|-------------|
| ids | vth | vdsat |
| 1.09907e-02 | 7.45000e-01 | 3.69000e+00 |

Calculations at $v_{gs}=v_{ds}=5$, $v_{bs}=-0.35$

$$\phi - v_{bs} = 1$$

$$v_{th} = -0.4 + 0.65 + (0.5 \cdot 1) - (ETA \cdot v_{ds}) = 0.75 - (0.001 \cdot v_{ds}) = 0.745$$

$$g = 1 - \frac{1}{(1.744 + 0.8364 \cdot 1)} = 0.612463$$

$$body = 1 + \frac{g \cdot 0.5}{(2 \cdot 1)} = 1 + 0.25 \cdot g = 1.153116$$

$$vc = 0 \text{ arg} = 1$$

$$v_{dsat} = \frac{(v_{gs} - v_{th})}{body \cdot \sqrt{arg}} = \frac{(5 - 0.745)}{body} = 3.69000$$

Calculations at vds=VDDM (default VDDM=5), mobility=mus=700

$$ids = cox \cdot \left(\frac{W_{eff}}{L_{eff}} \right) \cdot 700 \cdot \frac{(vgs - vth)^2}{(2 \cdot body \cdot arg)}$$

$$ids = \left(\frac{10 \cdot 700 \cdot 4.255^2}{2 \cdot 1.15311 \cdot 1} \right) \cdot cox = 54953.36 \cdot cox$$

$$ids = 1.09907e - 2$$

These calculations agree with the above simulation results.

BSIM Model — Compatibility Notes

This section covers the following topics:

- [BSIM Model—Compatibility Notes: Model Parameter Naming](#)
- [BSIM Model—Compatibility Notes: SPICE/Synopsys Model Parameter Differences](#)
- [BSIM Model—Compatibility Notes: Parasitics](#)
- [BSIM Model—Compatibility Notes: Temperature Compensation](#)
- [BSIM Model—Compatibility Notes: BEX Usage](#)
- [BSIM Model—Compatibility Notes: UPDATE Parameter](#)
- [BSIM Model—Compatibility Notes: Explanations](#)
- [BSIM Model—Compatibility Notes: IDS and VGS Curves for PMOS and NMOS](#)

BSIM Model—Compatibility Notes: Model Parameter Naming

The following names are HSPICE-specific: U00, DL0, DWO, PHIO, ETA0, NB0, and ND0. A zero was added to the SPICE names to avoid conflicts with other standard parameter names. For example, you cannot use U0 because it is an alias for UB, the mobility parameter in many other levels. You cannot use DL, because it is an alias for XL, a geometry parameter available in all levels.

You can use DL0 and DWO with this model, but you should use XL, LD, XW, and WD instead (noting the difference in units).

Watch the units of TOX. It is safest to enter a number greater than one, which simulation always interprets as Angstroms.

Chapter 2: MOSFET Models

LEVEL 13: BSIM Model

To avoid negative gds:

1. Set X3U1, LX3U1, and WX3U1 to zero.
2. Check that
 $zx3ms \geq 0$, where $zx3ms = X3MS$ with L , W adjustment
3. Check that
 $zmuz + VDDM - zx3ms < zmus$

BSIM Model—Compatibility Notes: SPICE/Synopsys Model Parameter Differences

The following table compares the UCB BSIM1 and the Synopsys Level 13 model parameters. Units in this table are in brackets. This comparison uses the model parameter name only if it differs from the SPICE name. The model specifies parameter units only if they differ from SPICE units. These aliases are in parentheses. Some parameter aliases match the SPICE names.

An asterisk (*) in front of a UCB SPICE name denotes an incompatibility between the parameter name in the Synopsys Level 13 MOSFET device model and the UCB SPICE name (that is, the parameter alias does not match or the units are different).

Even if the parameter name in this model is not the same as in SPICE, the corresponding L and W sensitivity parameter names might not differ. The following table lists the L and W sensitivity parameters only for the few cases where the parameters are different.

| UC Berkeley SPICE 2, 3 | Synopsys Device Model |
|--------------------------|-----------------------|
| VFB [V] | VFB0 (VFB) |
| PHI [V] | PHI0 |
| K1 [$V^{1/2}$] | same |
| K2 | same |
| * ETA | ETA0 |
| MUZ [$cm^2/V \cdot s$] | same |
| * DL [μm] | DL0 |
| * DW [μm] | DW0 |

| UC Berkeley SPICE 2, 3 | Synopsys Device Model |
|---|------------------------------|
| * U0 [1/V] | U00 |
| * U1 [μ V] | same |
| X2MZ [$\text{cm}^2/\text{V}^2 \cdot \text{s}$] | X2M (X2MZ) |
| LX2MZ [$\mu\text{m} \cdot \text{cm}^2/\text{V}^2 \cdot \text{s}$] | X2M (LX2MZ) |
| WX2MZ [$\mu\text{m} \cdot \text{cm}^2/\text{V}^2 \cdot \text{s}$] | WX2M (WX2MZ) |
| X2E [1/V] | same |
| X3E [1/V] | same |
| X2U0 [$1/\text{V}^2$] | same |
| X2U1 [$\mu\text{m}/\text{V}^2$] | same |
| MUS [$\text{cm}^2/\text{V} \cdot \text{s}$] | same |
| LMUS [$\mu\text{m} \cdot \text{cm}^2/\text{V} \cdot \text{s}$] | LMS (LMUS) |
| WMUS [$\mu\text{m} \cdot \text{cm}^2/\text{V} \cdot \text{s}$] | WMS (WMUS) |
| X2MS [$\text{cm}^2/\text{V}^2 \cdot \text{s}$] | same |
| X3MS [$\text{cm}^2/\text{V}^2 \cdot \text{s}$] | same |
| X3U1 [$\mu\text{m}/\text{V}^2$] | same |
| * TOX [μm] | TOXM[μ] (TOX[m]) |
| * TEMP [$\times\text{C}$] | TREF |
| * VDD [V] | VDDM |
| CGDO [F/m] | CGDOM (CGDO) |
| CGSO [F/m] | CGSOM (CGSO) |
| CGBO [F/m] | CGBOM (CGBO) |
| XPART | same |
| N0 | same |

Chapter 2: MOSFET Models

LEVEL 13: BSIM Model

| UC Berkeley SPICE 2, 3 | Synopsys Device Model |
|------------------------|-----------------------|
| * NB | NB0 |
| * ND | ND0 |
| RSH [ohm/sq] | RSHM (RSH) |
| JS [A/m ²] | IJS (JS) |
| PB [V] | PJ (PB) |
| MJ | MJ0 (MJ) |
| * PBSW [V] | PJW (PHP) |
| MJSW | MJW (MJSW) |
| CJ [F/m ²] | CJM (CJ) |
| CJSW [F/m] | CCJW (CJSW) |
| * WDF [m] | — |
| * DELL [m] | — |

In UCB SPICE, you must specify all BSIM model parameters. The Synopsys model provides default values for the parameters.

BSIM Model—Compatibility Notes: Parasitics

ACM >0 invokes parasitic diode models. ACM=0 (default) is SPICE style.

BSIM Model—Compatibility Notes: Temperature Compensation

The default TNOM model reference temperature is 25°C, unless you use .OPTION SPICE to set the default TNOM value to 27°C. This option also sets some other SPICE compatibility parameters. You set TNOM in an .OPTION line in the netlist, and you can always use the TREF model parameter to override it locally (that is, for a model). (The model “reference temperature” means that the model parameters were extracted at and are valid at that temperature.)

UCB SPICE does not use TNOM (default 27°C) for the BSIM models. Instead, you must specify the TEMP model parameter as both the model reference temperature and the analysis temperature. Analysis at TEMP applies only to thermally-activated exponentials in the model equations. You cannot adjust model parameter values when you use TEMP. Simulation assumes that you

extracted the model parameters at TEMP, because TEMP is both the reference and the analysis temperature.

In contrast to UCB SPICE's BSIM, the Synopsys Level 13 model does provide for temperature analysis. The default analysis temperature is 25°C (and 27°C in UCB SPICE for all model levels except for BSIM as explained in the previous paragraph). Use a .TEMP statement in the netlist to change the analysis temperature.

The Level 13 model provides two temperature coefficients: TCV and BEX. The following equation adjusts the threshold voltage:

$$vth(t) = vth - TCV \cdot (t - t_{nom})$$

This model includes two implementations of the BEX factor. To select a BEX version, use the UPDATE parameter, described in the next section. The mobility in BSIM is a combination of five quantities: MUZ, zmus, z3ms, zx2mz, and zx2ms.

BSIM Model—Compatibility Notes: BEX Usage

$$MUZ(t) = MUZ \cdot \left(\frac{t}{t_{nom}} \right)^{BEX}$$

$$zmus(t) = zmus \cdot \left(\frac{t}{t_{nom}} \right)^{BEX}$$

$$zx3ms(t) = zx3ms \cdot \left(\frac{t}{t_{nom}} \right)^{BEX}$$

$$zx2mz(t) = zx2mz \cdot \left(\frac{t}{t_{nom}} \right)^{BEX}$$

$$zx2ms(t) = zx2ms \cdot \left(\frac{t}{t_{nom}} \right)^{BEX}$$

This is equivalent to multiplying the final mobility by the factor:

$$\left(\frac{t}{t_{nom}} \right)^{BEX}$$

BSIM Model—Compatibility Notes: UPDATE Parameter

The UPDATE parameter selects between variations of the BSIM equations. UPDATE=0 (default) is consistent with UCB SPICE3. UPDATE=3 also is consistent with UCB SPICE3 and BEX usage.

| Parameter | Description |
|-----------|---|
| UPDATE=0 | UCB compatible, previous BEX usage |
| UPDATE=1 | Special X2E equation, previous BEX usage |
| UPDATE=2 | Remove 1/Leff in U1 equation, present BEX usage |
| UPDATE=3 | UCB compatible, present BEX usage |

BSIM Model—Compatibility Notes: Explanations

The normal X2E equation is:

$$xeta = zeta - (zx2e \cdot vsb) + zx3e \cdot (vds - VDDM)$$

The special X2E equation for UPDATE=1 only, is:

$$xeta = zera + zx2e \cdot (zphi + vsb) + zx3e \cdot (vds - VDDM)$$

The special X2E equation was developed to match a parameter extraction program. If you use a parameter extraction program, check the equations carefully.

The original U1 equation divides by L_{eff} in microns:

$$xu1 = \frac{(zu1 - (zx2u1 \cdot vsb) + zx3u1 \cdot (vds - VDDM))}{Leff}$$

This is one of the few places where L_{eff} explicitly enters into the BSIM equations; usually, the L-adjustment model parameters (such as LU1) handles the L_{eff} variation.

Physically xu1 should decrease as 1/L_{eff} at long channels, but when dealing with short-channel devices, you can turn off this variation. Set UPDATE=2 to remove the 1/L_{eff} factor in the xu1 equation.

UPDATE=2 introduces the present BEX usage as the 1/L_{eff} removal ability. UPDATE=3 provides the present BEX using the previous xu1 equation.

BSIM Model—Compatibility Notes: IDS and VGS Curves for PMOS and NMOS

The netlists for the IDS and VGS curves for PMOS and NMOS are located in directory `$installdir/demo/hspice/mos/ml13iv.sp`. This file contains examples of the following model parameter and curve descriptions:

- Two Types of Model Parameter Formats Used
- VGS Curves
- GM Test
- GM B CVN7 5 37 0
- .PROCESS PC Filename=M57R
- N-channel Devices
- First Model Parameter Format
- PMOS Model
- Second Model Parameter Format
- N+ Diffusion Layer
- PMOS Model
- Wire Model for Poly and Metal Layers

LEVEL 27: SOSFET Model

This model is a three-terminal silicon-on-sapphire (SOS) FET transistor model.^[4] This SOSFET model is based on a sapphire insulator that isolates the substrate and models the behavior of SOS devices more accurately than standard MOSFET models with physically unreal parameter values. The SOSFET model also includes a charge conservation model (based on the Ward and Dutton model).

Because the defaults of the SOSFET model parameters depend on the channel length, you must specify the `SOSLEV` model parameter to select either the 5 μm or 3 μm processing model.

`SOSLEV=1` selects the 5 μm model; otherwise, this model automatically uses the 3 μm value, including the second-order effects (default=3 μm).

Note: This model does not include bulk nodes. If you specify bulk nodes, simulation ignores them.

This model does not use the `ACM` model parameter, because it does not include any junction diodes. Also, the only value that the `CAPOP` model parameter accepts is 7. Seven is its own charge conservation model, which you cannot use in other MOSFET models.

Temperature compensation equations for the `VTO` and `UO` SOSFET model parameters are the same as those in the MOSFET model.

Note: This model includes a special option for bulk nodes for silicon on sapphire. In the model definition, if you specify -1 for the bulk node, this model generates a special node for each element. This bulk node is named in the form, `B#<element_name>`, where the element name is the name of the defined element. Use this name in any statement, such as a `.PRINT` statement to refer to the bulk node in the element.

Syntax:

```
.MODEL mname PMOS <LEVEL=27> <SOSLEV=val> <pname1=val1>  
.MODEL mname NMOS <LEVEL=27> <SOSLEV=val> <pname=val1>
```

You can use this .MODEL syntax to include a MOSFET Level 27 model in your HSPICE netlist. For a general description of the [.MODEL statement](#), see the *HSPICE Reference Manual: Commands and Control Options*.

| Parameter | Description |
|-----------|--|
| mname | Model name. |
| PMOS | Identifies a p-channel MOSFET model. |
| NMOS | Identifies an n-channel MOSFET model. |
| LEVEL | Model level selector. |
| SOSLEV | Selects the processing model. If you set SOSLEV=1, the default=5 μ m. The automatic default=3 μ m. |
| pname | Parameter model. |

This section covers the following topics:

- [SOSFET Model Parameters](#)
- [SOSFET Model — Non-Fully Depleted SOI Model](#)
- [SOSFET Model — Components](#)
- [SOSFET Model — Obtaining Model Parameters](#)
- [SOSFET Model — Fully Depleted SOI Model Considerations](#)
- [SOSFET Model — Example](#)

SOSFET Model Parameters

This section covers the following topics:

- [SOSFET Model — 5- \$\mu\$ m Model Parameters](#)
- [SOSFET Model — 3-mm Model Parameters](#)

SOSFET Model — 5- μ m Model Parameters

| Name (Alias) | Units | Default | Description |
|--------------|-------|---------|---|
| CGDO | F/m | | Gate-drain overlap capacitance per unit channel width. Default=3.1e-10 (n-type), 2.2e-10 (p-type). |

Chapter 2: MOSFET Models

LEVEL 27: SOSFET Model

| Name (Alias) | Units | Default | Description |
|--------------|-------------------------|---------|--|
| CGSO | F/m | | Gate-source overlap capacitance per unit channel width. Default=3.1e-10 (n-type), 2.2e-10 (p-type). |
| LD | m | | Lateral diffusion. The default=0.6 μ (n-type), 0.3 μ (p-type). |
| RSH | ohm/sq | | Drain and source diffusion sheet resistance. The default=25 (n!-type), 100 (p-type). |
| SOSLEV | | 1 | Model index. |
| TOX | m | 7.0e-8 | Oxide thickness. |
| UO | cm ² /(V· s) | | Surface mobility. Default=350 (n-type), 220 (p-type). |
| VTO | V | | Threshold voltage. Default=1.25 (n-type), -1.25 (p-type). |

SOSFET Model — 3- μ m Model Parameters

| Name (Alias) | Units | Default | Description |
|--------------|--------|-------------|--|
| A | m/V | 0.1 μ m | Channel length shortening coefficient (2nd effect) |
| ALPHA | V/m | | Threshold voltage length dependence. Default=0.15 μ (n-type), 0.18 μ (p-type). |
| CAPOP | | 7 | Capacitance model selector. |
| CGDO | F/m | | Gate-drain overlap capacitance per unit channel width. Default=4.6e-10 (n-type), 3.6e-10 (p-type). |
| CGSO | F/m | | Gate-source overlap capacitance per unit channel width. The default=4.6e-10 (n-type), 3.6e-10 (p-type). |
| EC | V/m | | Critical electric field for velocity saturation (2nd effect). The default=3.0e6 (n-type), 7.5e6 (p-type). |
| FB | | | Body effect coefficient (2nd effect). Default=0.15 (n-type), 0 (p-type). |
| LD | m | | Lateral diffusion. Default=0.3 μ (n-type), 0.2 μ (p-type). |
| LEVEL | | 27 | Model level selector. |
| RSH | ohm/sq | | Drain and source diffusion sheet resistance. Default=25 (n-type), 80 (p-type). |
| SOSLEV | | 2 | Model index. |

| Name (Alias) | Units | Default | Description |
|--------------|-------------------------|---------|--|
| THETA | 1/V | | Mobility degradation coefficient (2nd effect). Default=0.055 (n-type), 0.075 (p-type). |
| TOX | m | 3.4e-8 | Oxide thickness. |
| UO | cm ² /(V· s) | | Surface mobility. Default=370 (n-type), 215 (p-type). |
| VTO | V | | Threshold voltage. Default=0.83 (n-type), -0.74 (p-type). |

SOSFET Model — Non-Fully Depleted SOI Model

Several MOSFET models are currently available for SOS/SOI applications. The 3-terminal SOS model (LEVEL=27) is stable for circuit design usage, but has some limitations. This model does not provide for depleted bulk. Use it only with applications that are not fully depleted and that do not consider kink effects.

The following circuit example is a 4-terminal SOI model for incompletely depleted bulk with the kink effect. Its sub-circuit allows a parasitic capacitance to the substrate. In this example, the bulk is the region under the channel. This model assumes that the substrate is the conductive layer under the insulator.

- For SOI, the insulator is usually silicon dioxide and the substrate is silicon.
- For SOS, the insulator is sapphire and the substrate is the metal that contacts the back of the integrated circuit die.

SOSFET Model — Components

This model consists of the following subcomponents:

- Core IDS model: any level works because the impact ionization and weak inversion models are common to all DC levels. The example uses a LEVEL=3 DC MOS model.
- Subthreshold model: the WIC=3 model parameter allows the older models to use the more advanced models found in the BSIM (LEVEL=13, LEVEL=28) models. The N0 model parameter should have a typical value around 1.0.
- Impact ionization model: set ALPHA and VCR parameters to enable the impact ionization model, which is available to all MOS DC equations. Typical values are ALPHA=0.1 and VCR=18.

Chapter 2: MOSFET Models

LEVEL 27: SOSFET Model

- Charge conservation gate cap model (`CAPOP=9, XQC=.4`) prevents the floating bulk node from obtaining extreme values.
- The automatic periphery diode area calculation method (`ACM`) is set to 3 to automatically calculate the source and drain resistances and diode junction leakage, and the capacitance. (`ACM=3 CJ=0 CJSW=0 CJGATE=4e-10 JS=0 JSW=1e-9 LD=.1u HDIF=1.5u RS=40 RD=40 N=1`).

Note: These models assume that the source/drain diffusions extend to the buried oxide. The area part of the diode has no capacitance to bulk. However, the subcircuit includes linear capacitors to the substrate.

SOSFET Model — Obtaining Model Parameters

Use the optimizing capabilities in the Level 27 MOSFET model to obtain the core IDS model parameters.

Use the optimizer to obtain the core model, subthreshold, and impact ionization parameters. The subthreshold model selected is an improved BSIM type of model that was altered for the older models. The charge conservation model is more charge conserving than the original Ward-Dutton model in SPICE 2G6.

Calculating the automatic diode area and the resistance estimates the junction capacitance, saturation current, and resistance as a function of the transistor width. Use the `VNDS` and `NDS` parameters for a piecewise linear approximation to reverse the junction current characteristics.

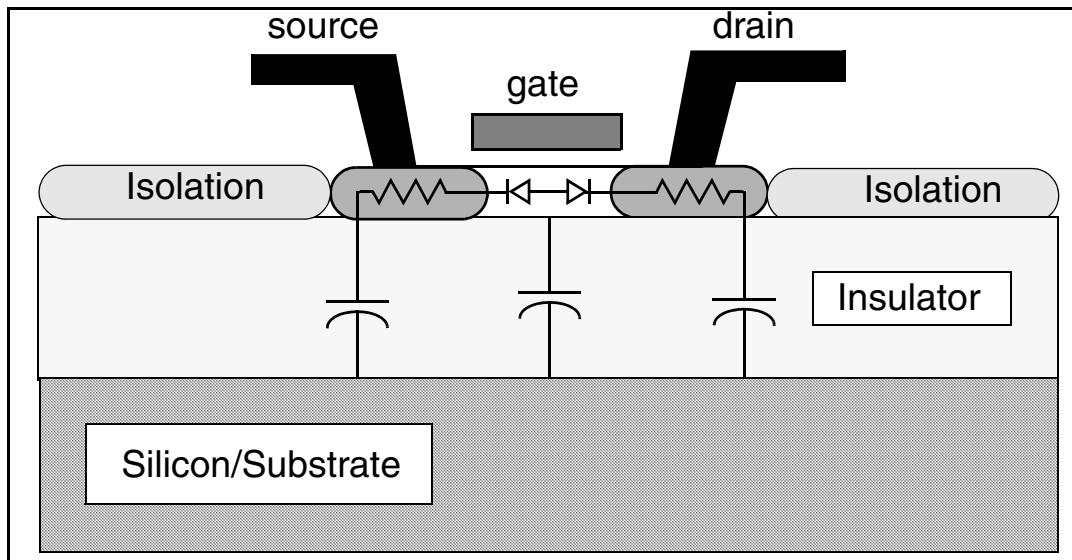


Figure 7 Non Fully Depleted SOI Model

The following example is based on demonstration netlist `ssoi.sp`, which is available in directory `$installdir/demo/hspice/mos`:

Chapter 2: MOSFET Models

LEVEL 27: SOSFET Model

```
ssoi.sp LEVEL=3 floating bulk model
** non-fully depleted
* test 1st order soi model with floating substrate
.option nomod post
* substrate capacitance 3.45e-11 is for SiO2
.param t_sub_ox=.5u subcap='3.45e-11/t_sub_ox' hdif=1.5u
.global substrate
.dc vd 0 5 0.1 sweep vg 1.5 3.5 0.5
.print id=i(xm1.m) vds=v(d) vgs=v(g)
.param vds=0 vgs=0 vbs=0
vd d gnd vds
vg g gnd vgs
vs s gnd 0
vsub substrate gnd vbs
xm1 d g s nch w=50u L=5u
.macro nch d g s w=10u l=2u
* macro definition for fet+ parasitic cap to substrate
* assumes existence of undepleted bulk
m d g s b nch w=w L=L
cx1 d substrate c='w*2*hdif*subcap'
cx2 s substrate c='w*2*hdif*subcap'
cx3 b substrate c='w*L*subcap'
.eom
.model nch nmos LEVEL=3
+ lmin=.5u lmax=100u wmin=.5u wmax=500u $model selector
+ ld=0.1u wd=.15u xl=0 xw=0
$diffusion+photobias
+ acm=3 hdif=hdif rsh=30 rs=10k rd=10k $resistors
+ ldif=0.1u
$junction cap (ACM=3 (h9007 only) allows diode on gate edge
+ cj=0 cjsw=0 cgate=0.4e-9 mjsw=0.33 php=0.6
+ js=0 jsw=1e-9 n=1 vnds=.5 nds=1 $junction leakage
+ bex=-1.5 tcv=2m $temperature
+ tox=200 capop=9 xqc=.4 meto=0.08u $gate cap
+ alpha=0.1 vcr=18 $impact ionization
+ vto=0.7 phi=1 gamma=1 $threshold
+ eta=10 xj=0.1u $threshold
+ wic=3 n0=0.9 nd=0 $subthreshold
+ uo=400 theta=1m $dc mobility
+ vmax=100k kappa=0 $dc saturation
.end
```

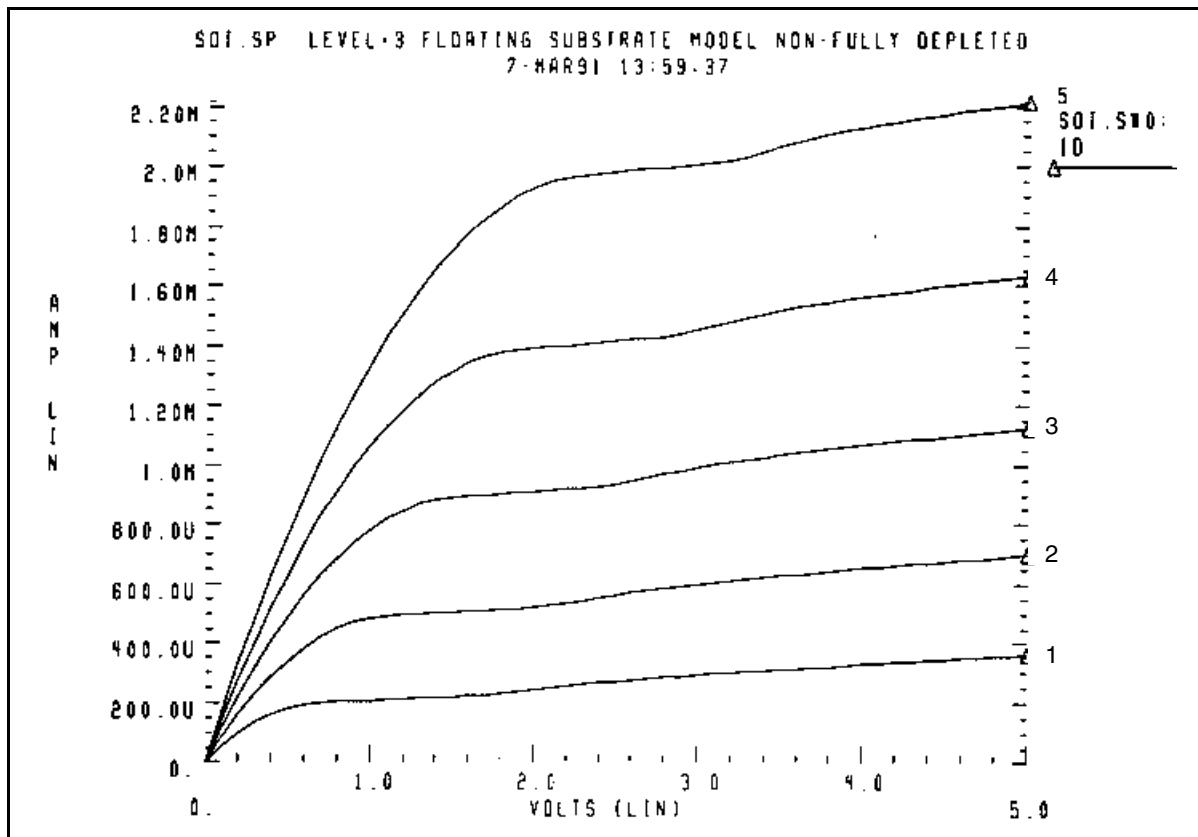


Figure 8 LEVEL 3 Floating Bulk Model

SOSFET Model — Fully Depleted SOI Model Considerations

Fully depleted transistors require additional modeling equations. The first-order effects are:

- Threshold sensitivity to the substrate.
- No kink current.
- Silicon thickness limits the minimum depletion capacitance.

Lack of these effects does not seriously affect an inverter, because the source-to-substrate voltage does not move. Digital circuits with good gate drive are not seriously affected, because a large gate voltage renders a small V_{th} shift to a small change in the IDS current.

The substrate threshold sensitivity can affect circuits such as analog amplifiers that include transistors at back-bias and low gate voltages.

SOSFET Model — Example

This example is based on demonstration netlist `m127iv.sp`, which is available in directory `$installdir/demo/hspice/mos`:

```
*file: ml27iv.sp ids and vgs curves for nmos and pmos sosfets.  
*mosfet level=27 p and n  
  
.options acct list nopage nomod post  
.op  
.dc vddn 0 5.0 .1  
  
* n-channel ids curves (vd=0-&lt;&lt;5, vg=1,2,3,4,5)  
.print dc i(vn1) i(vn2) i(vn3) i(vn4) i(vn5)  
.probe dc i(vn1) i(vn2) i(vn3) i(vn4) i(vn5)  
  
* p-channel ids curves (vd=0-&lt;&lt;-5,vg=-1,-2,-3,-4,-5)  
.print dc i(vp1) i(vp2) i(vp3) i(vp4) i(vp5)  
.probe dc i(vp1) i(vp2) i(vp3) i(vp4) i(vp5)  
  
* v g s curves  
.print dc i(vn6) i(vp6)  
.probe dc i(vn6) i(vp6)  
  
* n-channel LX7=gm(vd=5, vg=0-&lt;&lt;5, vs=0)  
* n-channel LX8=gd (vd=0-&lt;&lt;5, vg=5, vs=0)  
* n-channel LX9=gb (vd=5, vg=5, vs=0)  
.print dc LX7 (m21) LX8 (m5) LX9 (m31)  
  
* p-channel LX7=gm (vd=0, vg=0-&lt;&lt;-5, vs=-5)  
* p-channel LX8=gd (vd=0-&lt;&lt;-5, vg=-5, vs=-5)  
* p-channel LX9=gb (vd=0, vg=0, vs=-5)  
.print dc LX7(m22) LX8(m15) LX9(m32)  
*  
vddn 99 0 5.0  
epd 98 0 99 0 -1  
  
v1 1 0 1  
v2 2 0 2  
v3 3 0 3  
v4 4 0 4  
v5 5 0 5  
v11 11 0 -1  
v12 12 0 -2  
v13 13 0 -3  
v14 14 0 -4  
v15 15 0 -5  
*  
vn1 99 31 0  
vn2 99 32 0  
vn3 99 33 0  
vn4 99 34 0  
vn5 99 35 0
```

Chapter 2: MOSFET Models

LEVEL 27: SOSFET Model

```
m1 31 1 0 n1 8u 8u
m2 32 2 0 n1 8u 8u
m3 33 3 0 n1 8u 8u
m4 34 4 0 n1 8u 8u
m5 35 5 0 n1 8u 8u
*
vp1 98 41 0
vp2 98 42 0
vp3 98 43 0
vp4 98 44 0
vp5 98 45 0

m11 41 11 0 p1 8u 8u
m12 42 12 0 p1 8u 8u
m13 43 13 0 p1 8u 8u
m14 44 14 0 p1 8u 8u
m15 45 15 0 p1 8u 8u
*
* g m test
vn6 5 36 0
vp6 0 46 0
m21 36 99 0 n1 8u 8u
m22 46 98 15 p1 8u 8u
*
* g m b test
vn7 5 37 0
vp7 0 47 0
m31 37 5 0 98 n1 8u 8u
m32 47 0 15 99 p1 8u 8u
*
.model n1 nmos level=27 soslev=2
+vto=0.814 tox=0.34e-7 theta=0.55e-1
+fb=0.15 ec=0.3e7 a=0.1e-6
+uo=370 cgso=0.46e-9 cgdo=0.46e-9
+rsh=25 ld=0.3e-6
*
.model p1 pmos level=27 soslev=2
+vto=-0.7212 tox=0.34e-7 theta=0.75e-1
+fb=0.0 ec=0.75e7 a=0.1e-6
+uo=215 cgso=0.36e-9 cgdo=0.36e-9
+rsh=80 ld=0.2e-6
*
.end
```

LEVEL 28: BSIM Derived Model

This model is derived from the base BSIM Model. The following are the significant features of this model:

- Vertical field dependence of the carrier mobility
- Carrier velocity saturation
- Drain-induced barrier lowering
- Depletion charge sharing by the source and drain
- Non-uniform doping profile for ion-implanted devices
- Channel length modulation
- Subthreshold conduction
- Geometric dependence of the electrical parameters

This section covers the following topics:

- [BSIM Derived Model Parameters](#)
 - [BSIM Derived Model Equations](#)
-

BSIM Derived Model Parameters

This model uses the generic MOSFET model parameters described in [Common MOSFET Model Parameters](#) section. In addition, this model also uses the following parameters:

This section covers the following topics:

- [BSIM Derived Model — Transistor Process Parameters](#)
- [BSIM Derived Model — Temperature Parameters:](#)
- [BSIM Derived Model — Sensitivity Factors of Model Parameters](#)

BSIM Derived Model — Transistor Process Parameters

| Name (Alias) | Units | Default | Description |
|--------------|-------|---------|---|
| LEVEL | 1 | | MOSFET model level selector. Set this parameter to 28 for this model. |
| B1 | 0.0 | | Lower vdsat transition point |

Chapter 2: MOSFET Models

LEVEL 28: BSIM Derived Model

| Name (Alias) | Units | Default | Description |
|--------------|---------------------------|---------|---|
| B2 | | 1 | Upper vdsat transition point |
| CGBO | F/m | 2.0e-10 | Gate-to-bulk parasitic capacitance (F/m of length) |
| CGDO | F/m | 1.5e-9 | Gate-to-drain parasitic capacitance (F/m of width) |
| CGSO | F/m | 1.5e-9 | Gate-to-source parasitic capacitance (F/m of width) |
| ETA0 | | 0.0 | Linear vds threshold coefficient |
| ETAMN | | 0.0 | Minimum linear vds threshold coefficient |
| GAMMN | V ^{1/2} | 0.0 | Minimum root-vs _b threshold coefficient |
| K1 | V ^{1/2} | 0.5 | Root-vs _b threshold coefficient |
| K2 | | 0.0 | Linear vs _b threshold coefficient |
| LB1 | μm | 0.0 | Length sensitivity |
| LB2 | μm | 0.0 | Length sensitivity |
| LETA | μm | 0.0 | Length sensitivity |
| LETAMN | μm | 0.0 | Length sensitivity |
| LGAMN | V ^{1/2} . μm | 0.0 | Length sensitivity |
| LK1 | V ^{1/2} . μm | 0.0 | Length sensitivity |
| LK2 | μm | 0.0 | Length sensitivity |
| LMUZ | μm· cm ² /V· s | 0.0 | Length sensitivity |
| LN0 | μm | 0.0 | Length sensitivity |
| LNB | μm | 0.0 | Length sensitivity |
| LND | μm | 0.0 | Length sensitivity |
| LPHI | V· μm | 0.0 | Length sensitivity |
| LU0 | μm/V | 0.0 | Length sensitivity |
| LU1 | μm/V | 0.0 | Length sensitivity |

| Name (Alias) | Units | Default | Description |
|--------------|---|---------|---|
| LVFB | V· μm | 0.0 | Length sensitivity |
| LWFAC | μm | 0.0 | Length sensitivity |
| LWFACU | μm | 0.0 | Length sensitivity |
| LX2E | μm/V | 0.0 | Length sensitivity |
| LX2M (LX2MZ) | μm· cm ² /V ² · s | 0.0 | Length sensitivity |
| LX2U0 | μm/V ² | 0.0 | Length sensitivity |
| LX2U1 | μm ² /V ² | 0.0 | Length sensitivity |
| LX33M | μm· cm ² /V ² · s | 0.0 | Length sensitivity |
| LX3E | μm/V | 0.0 | Length sensitivity |
| LX3MS | μm· cm ² /V ² · s | 0.0 | Length sensitivity |
| LX3U1 | μm/V ² | 0.0 | Length sensitivity |
| MUZ | cm ² /V· s | 600 | Low drain field first order mobility |
| N0 | | 200 | Low field weak inversion gate drive coefficient (value of 200 for N0 disables the weak inversion calculation) |
| NB0 | | 0.0 | V _{sb} reduction to the low field weak inversion gate drive coefficient |
| ND0 | | 0.0 | V _{ds} reduction to the low field weak inversion gate drive coefficient |
| PHI0 | V | 0.7 | Two times the Fermi potential |
| TOXM (TOX) | μm (m) | 0.02 | Gate oxide thickness (if TOXM or TOX >1, uses Angstroms) |
| U00 | 1/V | 0.0 | Gate field mobility reduction factor |
| U1 | 1/V | 0.0 | Drain field mobility reduction factor |

Chapter 2: MOSFET Models

LEVEL 28: BSIM Derived Model

| Name (Alias) | Units | Default | Description |
|--------------|---|---------|--|
| VDDM | V | 5.0 | Critical voltage for the high-drain field mobility reduction |
| VFB0 (VFB) | V | -0.3 | Flatband voltage |
| WB1 | μm | 0.0 | Width sensitivity |
| WB2 | μm | 0.0 | Width sensitivity |
| WETA | μm | 0.0 | Width sensitivity |
| WETAMN | μm | 0.0 | Width sensitivity |
| WFAC | | 4 | Weak inversion factor |
| WFACU | | 0.0 | Second weak inversion factor |
| WGAMN | $\text{V}^{1/2} \cdot \mu\text{m}$ | 0.0 | Width sensitivity |
| WK1 | $\text{V}^{1/2} \cdot \mu\text{m}$ | 0.0 | Width sensitivity |
| WK2 | μm | 0.0 | Width sensitivity |
| WMUZ | $\mu\text{m} \cdot \text{cm}^2/\text{V} \cdot \text{s}$ | 0.0 | Width sensitivity |
| WN0 | μm | 0.0 | Width sensitivity |
| WNB | μm | 0.0 | Width sensitivity |
| WND | μm | 0.0 | Width sensitivity |
| WPHI | $\text{V} \cdot \mu\text{m}$ | 0.0 | Width sensitivity |
| WU0 | $\mu\text{m}/\text{V}$ | 0.0 | Width sensitivity |
| WU1 | $\mu\text{m}/\text{V}$ | 0.0 | Width sensitivity |
| WVFB | $\text{V} \cdot \mu\text{m}$ | 0.0 | Width sensitivity |
| WWFAC | μm | 0.0 | Width sensitivity |
| WWFACU | μm | 0.0 | Width sensitivity |
| WX2E | $\mu\text{m}/\text{V}$ | 0.0 | Width sensitivity |
| WX2M (WX2MZ) | $\mu\text{m} \cdot \text{cm}^2/\text{V}^2 \cdot \text{s}$ | 0.0 | Width sensitivity |

| Name (Alias) | Units | Default | Description |
|--------------|---|---------|--|
| WX2U0 | $\mu\text{m}/\text{V}^2$ | 0.0 | Width sensitivity |
| WX2U1 | $\mu\text{m}^2/\text{V}^2$ | 0.0 | Width sensitivity |
| WX33M | $\mu\text{m} \cdot \text{cm}^2/\text{V}^2 \cdot \text{s}$ | 0.0 | Width sensitivity |
| WX3E | $\mu\text{m}/\text{V}$ | 0.0 | Width sensitivity |
| WX3MS | $\mu\text{m} \cdot \text{cm}^2/\text{V}^2 \cdot \text{s}$ | 0.0 | Width sensitivity |
| WX3U1 | $\mu\text{m}/\text{V}^2$ | 0.0 | Width sensitivity |
| X2E | 1/V | 0.0 | V _{sb} correction to the linear vds threshold coefficient |
| X2M (X2MZ) | $\text{cm}^2/\text{V}^2 \cdot \text{s}$ | 0.0 | V _{sb} correction to the low field first order mobility |
| X2U0 | $1/\text{V}^2$ | 0.0 | V _{sb} reduction to the GATE field mobility reduction factor |
| X2U1 | $\mu\text{m}/\text{V}^2$ | 0.0 | V _{sb} reduction to the DRAIN field mobility reduction factor |
| X33M | $\text{cm}^2/\text{V}^2 \cdot \text{s}$ | 0.0 | Gate field reduction of X3MS |
| X3E | 1/V | 0.0 | V _{ds} correction to the linear vds threshold coefficient |
| X3MS | $\text{cm}^2/\text{V}^2 \cdot \text{s}$ | 5.0 | V _{ds} correction for the high-drain field mobility |
| X3U1 | $1/\text{V}^2$ | 0.0 | V _{ds} reduction to the drain field mobility reduction factor |
| XPART | | 1.0 | Selects the coefficient for sharing the gate capacitance charge |

Note: Following are some important points:

- When you read parameter names, be careful about the difference in appearance between the capital letter O and the number zero (0).
- Use NMOS conventions to specify all Level 28 parameters, even for PMOS—for example, `ETA0=0.02`, not `ETA0=-0.02`

- You can use the WL -product sensitivity parameter for any parameter with an L and W sensitivity. Replace the leading “L” of the L sensitivity parameter name with a “P”.

BSIM Derived Model — Temperature Parameters:

| Name (Alias) | Units | Default | Description |
|--------------|-----------------|---------|---|
| BEX | | -1.5 | Temperature exponent for the MUZ, X2M, X3MS, and X33M mobility parameters |
| FEX | | 0.0 | Temperature exponent for the U1 mobility reduction factor |
| TCV | V/ $^{\circ}$ K | 0.0 | Flat-band voltage temperature coefficient |

BSIM Derived Model — Sensitivity Factors of Model Parameters

For transistors, drop the 0 from the end of the parameter name, and add one of the following product sensitivity factors for a basic electrical parameter:

- L (channel length)
- W (channel width)
- WL (width and length)

For example, the $VFB0$ sensitivity factors are $LVFB$, $WVFB$, and $PVFB$. If $A0$ is a basic parameter, LA , WA and PA are the corresponding sensitivity factors for this parameter (you cannot use the SCALM option to scale LA , WA , and PA). Then the model uses the following general formula to obtain the parameter value.

The left side of the equation represents the effective model parameter value after you adjust the device size. All effective model parameters are in lower case and start with the z character, followed by the parameter name.

$$za = A0 + LA \cdot \left[\frac{1}{Leff} - \frac{1}{LREFeff} \right] + WA \cdot \left[\frac{1}{Weff} - \frac{1}{WREFeff} \right]$$

$$PA \cdot \left[\frac{1}{Leff} - \frac{1}{LREFeff} \right] \cdot \left[\frac{1}{Weff} - \frac{1}{WREFeff} \right]$$

Specify LA and WA in units of microns times the units of $A0$. Specify PA in units of square microns times the units of $A0$.

If you set $LREF$ or $WREF=0$, you effectively set the parameter value to infinity. This is the default.

Example:

$$VFB0 = -0.350v$$

$$LVFB = -0.1v\mu$$

$$WVFB = 0.08v \cdot \mu$$

$$Leff = 1 \cdot 10^{-6}m = 1\mu$$

$$Weff = 2 \cdot 10^{-6}m = 2\mu$$

$$LREFeff = 2 \cdot 10^{-6}m = 2\mu$$

$$WREFeff = 1 \cdot 10^{-5}m = 10\mu$$

$$zvfb = VFB0 + LVFB \cdot \left(\frac{1}{Leff} - \frac{1}{LREFeff} \right) + WVFB \cdot \left(\frac{1}{Weff} - \frac{1}{WREFeff} \right)$$

$$zvfb = -0.35v + -0.1v \cdot \mu \cdot \left(\frac{1}{1\mu} - \frac{1}{2\mu} \right) + 0.08v \cdot \mu \cdot \left(\frac{1}{2\mu} - \frac{1}{10\mu} \right)$$

$$zvfb = -0.35v - 0.05v + 0.032v$$

$$zvfb = -0.368v$$

BSIM Derived Model Equations

This section covers the following topics:

- [BSIM Derived Model — Effective Channel Length and Width](#)
- [BSIM Derived Model — Threshold Voltage](#)
- [BSIM Derived Model — Effective Mobility](#)
- [BSIM Derived Model — Saturation Voltage \(vdsat\)](#)
- [BSIM Derived Model — Transition Points](#)
- [BSIM Derived Model — Strong Inversion Current](#)
- [BSIM Derived Model — Weak Inversion Current](#)
- [BSIM Derived Model — xweak < -zwfac+A0](#)
- [BSIM Derived Model — -zwfac+A0 < xweak < 0](#)

Chapter 2: MOSFET Models

LEVEL 28: BSIM Derived Model

- BSIM Derived Model — $0 < x_{weak} < A_0$
- BSIM Derived Model — $A_0 < x_{weak}$

BSIM Derived Model — Effective Channel Length and Width

The effective channel length and width for Level 28 is consistent with the LEVEL 3 model. L, W, and the M multiplier are from the .MODEL statement in the netlist. SCALE and SCALM are options. If you do not specify any scaling options or multipliers, then:

$$L_{eff} = L + XL - 2 \cdot LD \quad W_{eff} = W + XW - 2 \cdot WD$$

Note: If you specify LDAC and WDAC in the .MODEL statement,

$$L_{eff} = L + XL - 2 \cdot LDAC \quad W_{eff} = W + XW - 2 \cdot WDAC$$

$$\begin{aligned} L_{scaled} &= L \cdot \text{SCALE} \\ W_{scaled} &= W \cdot \text{SCALE} \\ XL_{scaled} &= XL \cdot \text{SCALM} \\ LD_{scaled} &= LD \cdot \text{SCALM} \\ XW_{scaled} &= XW \cdot \text{SCALM} \\ WD_{scaled} &= WD \cdot \text{SCALM} \\ L_{eff} &= L_{scaled} \cdot LMLT + XL_{scaled} - 2 \cdot LD_{scaled} \\ LREF_{eff} &= LREF_{scaled} \cdot LMLT + XLREF_{scaled} - 2 \cdot LD_{scaled} \\ W_{eff} &= M \cdot (W_{scaled} \cdot WMLT + XWREF_{scaled} - 2 \cdot WD_{scaled}) \\ WREF_{eff} &= MP \cdot (WREF_{scaled} \cdot WMLT + XW_{scaled} - 2 \cdot WD_{scaled}) \end{aligned}$$

BSIM Derived Model — Threshold Voltage

Effective model parameter values for the threshold voltage, after you adjust the device size, are zphi, zvfb, zk1, zk2, zeta, zx2e, zx3e, zgammn, and zetamn. Simulation calculates these values from the PHI0, VFB0, K1, K2, ETA0, X2E, X3E, GAMMN, and ETAMN model parameters, and from their respective length and width sensitivity parameters.

$$xbs = (zphi - vbs) / 2$$

$$xeta = zeta + zx2e \cdot vbs + zx3e \cdot vds$$

$$vth = zvfb + zphi + zk1 \cdot xbs - zk2 \cdot xbs^2 - xeta \cdot vds$$

This equation is quadratic in xbs and vds. It is joined to linear equations at $d(vth)/d(xbs) = zgammn$ and at $d(vth)/d(vds) = -zetamn$, which prevents the quadratics from going in the wrong direction.

Both gammn and etamn default to zero, and typically do not affect behavior in the normal operating region.

BSIM Derived Model — Effective Mobility

The effective model parameter values for mobility, after you adjust the device size, are zmuz, zx2m, zx3m, zx33m, zu0, and zx2u0. Simulation calculates these values from the MUZ, X2M, X3m, X33M, U00, and X2U0 model parameters, and from their respective length and width sensitivity parameters.

$$v_{gst} = v_{gs} - v_{th},$$

$$m_{eff} = (zmuz + zx2m \cdot v_{bs})$$

$$cx3ms = \frac{zx3ms}{(muz + zx33m \cdot v_{gst})}$$

$$(1 + cx3ms \cdot (VDDM + v_{ds} - (VDDM \cdot VDDM + v_{ds} \cdot v_{ds})^{1/2}))$$

$$xu0 = zu0 + zx2u0 \cdot v_{bs}$$

$$u_{eff} = \frac{m_{eff}}{(1 + xu0 \cdot v_{gst})}, \text{ beta} = u_{eff} \cdot COX \cdot \frac{W_{eff}}{L_{eff}}$$

BSIM Derived Model — Saturation Voltage (vdsat)

The effective model parameter values for the saturation voltage, after you adjust the device size, are zu1, zx2u1, and zx3u1. Simulation calculates these values from the U1, X2U1, and X3U1 model parameters, and from their length and width sensitivity parameters.

$$xbs = (zphi - v_{bs})^{1/2}, g = 1 - \frac{1}{(1.744 + 0.8364 \cdot xbs^2)}$$

$$body = \frac{1 + g \cdot zk1}{(2 \cdot xbs)}, xu1 = zu1 + v_{bs} \cdot zx2u1$$

$$rx = (body^2 + zu1 \cdot 2 \cdot body \cdot v_{gst} + zx3u1 \cdot 4 \cdot v_{gst}^2)^{1/2}$$

$$v_{dsat} = \frac{2 \cdot v_{gst}}{(body + rx)}$$

This vds value generates the partial derivative of:

$$f(v_{ds}, v_{gst}, v_{bs}) = (v_{gst} - body / 2 \cdot v_{ds}) \cdot \frac{v_{ds}}{(1 + (xu1 + zx3u1 \cdot v_{ds}) \cdot v_{ds})}$$

In the preceding equation, vds=zero.

BSIM Derived Model — Transition Points

The effective model parameter values for the transition points, after you adjust the device size, are $zb1$ and $zb2$. Simulation calculates these values from the $B1$ and $B2$ model parameters, and from their respective length and width sensitivity parameters.

$$v1 = v_{dsat} - zb1 \cdot \frac{v_{dsat}}{1 + v_{dsat}}, v2 = v_{dsat} + zb2 \cdot v_{gst}$$

BSIM Derived Model — Strong Inversion Current

For $vds < v1$:

$$I_{ds} = beta \cdot (v_{gst} - body/2 \cdot v_{ds}) \cdot \frac{v_{ds}}{(1 + (zu1 + zx3u1 \cdot v_{ds}) \cdot v_{ds})}$$

The vds derivative varies approximately linearly between $v1$ and $v2$.

For $vds > v2$, ids is a function of β and $vgst$ only. If $zb1$ and $zb2$ are both positive, their main effect is to increase the saturation current.

BSIM Derived Model — Weak Inversion Current

The effective model parameter values for weak inversion current, after you adjust the device size, are $zn0$, znb , znd , $zwfac$, and $zwfacu$. Simulation calculates these values from the $N0$, $ND0$, $NB0$, $WFAC$, and $WFACU$ model parameters, and from their respective length and width sensitivity parameters.

Simulation calculates the weak inversion current when $zn0$ is less than 200, and adds it to the strong inversion current:

$$I_{total} = I_{strong} + I_{weak} \cdot \left(1 - \exp\left(\frac{-v_{ds}}{v_{therm}}\right) \right)$$

In deep subthreshold:

$$xn = zn0 + znb \cdot v_{bs} + znd \cdot v_{ds}$$

$$v_{therm} = \frac{KT}{Q}, x_{weak} = \frac{(v_{gs} - vt)}{(xn \cdot v_{therm})}$$

$$I_{weak} = const \cdot \exp(x_{weak})$$

$zwfac$ and $zwfacu$ control the modification of this formula near the threshold. Just above threshold, the device is in saturation:

$$I_{strong} = const \cdot x_{weak}^2$$

I_{weak} needs an x_{weak}^2 term to cancel the kink in gm at the threshold. Then I_{weak} goes to zero for $x_{weak} > A_0$, which is at a small voltage above the threshold. I_{weak} has four regions.

BSIM Derived Model — $x_{weak} < -z_{wfac} + A_0$

$$I_{weak} = const \cdot \exp(x_{weak})$$

BSIM Derived Model — $-z_{wfac} + A_0 < x_{weak} < 0$

$$I_{weak} = const \cdot \exp(x_{weak} - const \cdot wf)$$

In the preceding equation, wf is the integral with respect to the x_{weak} value of:

$$dwf = \frac{(x_{weak} + z_{wfac} - A_0)^2}{[(1 + x_{weak} + z_{wfac} - A_0)(1 + z_{wfac} \cdot (x_{weak} + z_{wfac} - A_0))]}$$

BSIM Derived Model — $0 < x_{weak} < A_0$

$$I_{weak} = (\text{same formula as in region 2}) - const \cdot x_{weak}^2$$

BSIM Derived Model — $A_0 < x_{weak}$

$$I_{weak} = 0$$

A_0 , and the constants in the preceding equations, are not model parameters. Continuity conditions, at the boundaries between regions, uniquely determine these constants.

LEVEL 38: Cypress Depletion Model

This model is a further development of the Synopsys [LEVEL 5: AMI-ASPEC Depletion and Enhancement \(Taylor-Huang\) Model](#). This model provides the following features:

- BSIM-style length and width sensitivities
- Degraded body effect at high substrate bias (second GAMMA)
- Empirical fitting parameters for I_{ds} current calculations in the depletion mode of operations
- A comprehensive surface mobility equation
- Drain-induced barrier lowering

At the default parameter settings, the LEVEL 38 model is basically backwards-compatible with LEVEL 5 /ZENH=0.0 with the exception of the surface mobility degradation equation (see the discussion on the next page). Refer to the documentation for LEVEL 5 for the underlying physics that forms the foundation for the Huang-Taylor construct.

In LEVEL 38, the temperature compensation for threshold is ASPEC-style, concurring with the default in LEVEL 5. This section describes the model parameters that are unique to this depletion model. It also describes additional temperature compensation parameters.

LEVEL 38 lets you use all Synopsys device model capacitance options (CAPOP). CAPOP=2 is the default setting for LEVEL 38. If you set CAPOP=6 (AMI capacitance model), LEVEL 38 capacitance calculations become identical to those of LEVEL 5.

The ACM default parameter (ACM=0 in LEVEL 38) invokes SPICE-style parasitics. You can set ACM to 1 (ASPEC), or to 2 (Synopsys device model). All MOSFET models follow this convention.

You can use .OPTION SCALE with the LEVEL 5 MOSFET device model. However, you cannot use the SCALM option, due to the difference in units. You also cannot use the DERIV option.

You must specify the following parameters for MOS LEVEL 38: VTO (VT), TOX, UO (UB), FRC, ECV, and NSUB (DNB).

As with LEVEL 5, this model calculates the I_{ds} current according to three gate voltage regions:

- *Depletion Region*, $v_{gs} - v_{fb} < 0$
The low gate voltage region, which the bulk channel dominates.
 - *Enhancement Region*, $v_{gs} - v_{fb} > 0, v_{ds} < v_{gs} - v_{fb}$
The region defined by high gate voltage and low drain voltage. In the enhancement region, both channels are fully turned on.
 - *Partial enhancement region*, $v_{gs} - v_{fb} > 0, v_{ds} > v_{gs} - v_{fb}$
This region has high gate and drain voltages so the surface region is partially turned on, and the bulk region is fully turned on.
To better model depletion region operations, empirical fitting constants have been added to the original Huang-Taylor mechanism to account for the effects caused by nonuniform channel implants and also to make up for an oversight in the average capacitance construct[5]. The enhancement region uses a significantly more elaborate surface mobility model.
Body effect in LEVEL 38 is calculated in two regions[6].
 - *Bulk body effect*, $v_{sb}-v_{sbc} > 0$
With sufficiently high (and negative) substrate bias (exceeding v_{sbc}), the depletion region at the implanted channel-substrate junction reaches the Si-oxide interface. Under such circumstances, the free carriers can accumulate only at the interface (as in an enhancement device) and the bulk doping level determines the body effect.
 - *Implant-dominated body effect*, $v_{sb}-v_{sbc} < 0$
Before reaching v_{sbc} , and as long as the implant dose overwhelms the substrate doping level, the deeply-buried transistor (due to the implant) dominates the body effect of the depletion mode device. The γ body effect coefficient is proportional to both the substrate doping and to the first-order implant depth. In Level 38, the BetaGam empirical parameter amplifies the body effect due to deep implant.
- Model parameters that start with L or W represent geometric sensitivities. In the model equations, three model parameters determine the zX quantity (X is the variable name):
- Large-and-wide channel case value (X).
 - Length sensitivity (LX).
 - Width sensitivity (WX).

The model calculates these parameters according to $zX=X+LX/Leff+WX/Weff$. For example, the following equation calculates the zero field surface mobility:

$$zUO = UO + \frac{LUO}{leff} + \frac{WUO}{wef}$$

Note: This model uses mostly micrometer units rather than meter units. Units and defaults are often unique in LEVEL 38. The finite difference method calculates the I_{ds} derivatives that define the gm, gds, and gmbs small signal gains. This model does not use the SCALM and DERIV options.

This section covers the following topics:

- [Cypress Depletion Model Parameters](#)
- [Cypress Depletion Model Equations](#)
- [Cypress Depletion Model — Sample Model File](#)

Cypress Depletion Model Parameters

This model uses the generic MOSFET model parameters described in [Common MOSFET Model Parameters](#) section. In addition, this level also uses the following parameters:

| Name (Alias) | Units | Default | Description |
|--------------|---------------|---------|------------------------------------|
| AFC | | 1.0 | Area factor for MOSFET capacitance |
| CAPOP | | 6 | Gate capacitance selector |
| METO | μm | 0.0 | Metal overlap on gate |

Cypress Depletion Model Equations

This section covers the following topics:

- [Cypress Depletion Model — IDS Equation](#)
- [Cypress Depletion Model — Threshold Voltage, vth](#)

- Cypress Depletion Model — Saturation Voltage, v_{dsat}
- Cypress Depletion Model — Mobility Reduction, U_{BEff}
- Cypress Depletion Model — Channel Length Modulation
- Cypress Depletion Model — Subthreshold Current, i_{ds}

Cypress Depletion Model — IDS Equation

Depletion, $v_{gs}-v_{fb} < 0$

$$i_{ds} = \beta_1 \cdot \left\{ q \cdot zKIO \cdot NI \cdot vde + cav \cdot \left[(v_{gs} - v_{fb}) \cdot vde - \frac{vde^2}{2} \right] \right.$$

$$\left. - \frac{2}{3} \cdot cav \cdot \bar{\gamma} \cdot [(vde + vsb + Phid)^{3/2} - (vsb + Phid)^{3/2}] + I_{crit} \right\}$$

Enhancement, $v_{gs}-v_{fb} > 0$

$$i_{ds} = \beta_1 \cdot \left\{ q \cdot zKIO \cdot NI \cdot vde - \frac{2}{3} cav \cdot \bar{\gamma} \cdot [(vde + vsb + Phid)^{3/2} - (vsb + Phid)^{3/2}] + I_{crit} \right\} + \beta \cdot \left[(v_{gs} - v_{fb}) \cdot vde - \frac{vde^2}{2} \right]$$

Partial Enhancement, $v_{gs}-v_{fb} < vde$

$$i_{ds} = \beta_1 \cdot \left\{ q \cdot zKIO \cdot NI \cdot vde + cav \cdot \left[(v_{gs} - v_{fb}) \cdot vde - \frac{vde^2}{2} \right] \right.$$

$$\left. - \frac{2}{3} \cdot cav \cdot \bar{\gamma} \cdot [(vde + vsb + Phid)^{3/2} - (vsb + Phid)^{3/2}] + I_{crit} \right\}$$

$$\left(\frac{1}{2}\beta - \frac{1}{2}\beta_1 \right) \cdot (v_{gs} - v_{fb})^2$$

The following equations calculate values used in the preceding equations:

$$\beta_1 = \frac{zKBeta1}{1 + UHSAT \cdot \frac{vde}{Leff}} \cdot UH \cdot \frac{Weff}{Leff}$$

Chapter 2: MOSFET Models
 LEVEL 38: Cypress Depletion Model

$$\beta = UBeff \cdot cox \cdot \frac{Weff}{Leff}, cav = \frac{cox \cdot cs}{cox + cs}$$

$$cs = \frac{KCS \cdot \varepsilon Si}{DP \cdot 1e-4}, Phid = vt \cdot \ln\left(\frac{DNB \cdot nd}{ni^2}\right)$$

$$nd = \frac{NI \cdot 1e4}{DP}, vde = \min(vds, vdsat)$$

The temperature dependence of the mobility terms assume the ordinary exponential form:

$$UH(t) = UH(tnom) \cdot \left(\frac{t}{tnom}\right)^{TUH}$$

$$zUO(t) = zUO(tnom) \cdot \left(\frac{t}{tnom}\right)^{TUH}$$

The following equation calculates the continuity term at the body effect transition point:

$$Icrit = \frac{2}{3} \cdot cav \cdot [(vde + vsbc + Phid)^{3/2} - (vsbc + Phid)^{3/2}] \cdot \gamma \cdot \left(\frac{1}{zBetaGam} - 1\right)$$

This model uses the preceding equation if $v_{sb} > v_{sc}$. Otherwise,

$$Icrit = 0$$

The following sections describe saturation voltage, threshold voltage, body effect transition voltage, and the γ body effect coefficient.

Cypress Depletion Model — Threshold Voltage, v_{th}

The VTO model parameter, often called the “pinch-off,” is a zero-bias threshold voltage extrapolated from a large device operating in the depletion mode. The following equation calculates the effective pinch-off threshold voltage, including the device size effects and the terminal voltages:

$$v_{th} = v_{fb} - \beta d = [v_{ch} - \bar{\gamma}] = [Phid + v_{sb}]^{1/2} + v_{crit}$$

The following equations calculate values used in the preceding equation:

$$v_{fb} = zVTO - zETA \Rightarrow ds + \beta d \cdot (v_{ch} - \gamma_0) = Phid^{1/2}$$

$$v_{crit} = \left(\gamma - \frac{\gamma}{zBetaGam}\right) = [Phid + vsbc]^{1/2}$$

for $v_{sb} > v_{sbc}$; 0 otherwise.

$$\beta_d = \frac{UH \cdot cav}{zUO \cdot cox}, v_{ch} = \frac{q \cdot NI}{cav}$$

$$\gamma_0 = \frac{(2 \cdot \varepsilon si \cdot q \cdot na1)^{1/2}}{cav}$$

$$na1 = \frac{nd \cdot DNB}{nd + DNB}, nd = \frac{NI}{DP \cdot 1e-4}$$

The following equation computes the effective γ , including small device size effects: $\bar{\gamma} = \frac{\gamma}{zBetaGam}$ for $v_{sb} > v_{sbc}$, and =g; otherwise,

$$\gamma = \gamma_0 \cdot (1 - scf) \cdot (1 + ncf)$$

The following equations calculate values used in the preceding equations:

If SCM = 0, then $scf = 0$; otherwise,

$$scf = \frac{XJ}{Leff} \cdot \left\{ \left[1 + \frac{2xd}{XJ} \cdot (SCM \cdot vds + v_{sb} + Phid)^{1/2} \right]^{1/2} - 1 \right\}$$

If NWM = 0, then $ncf = 0$; otherwise,

$$ncf = \frac{NWM \cdot xd \cdot (Phid)^{1/2}}{Weff}$$

This equation calculates the xd value used in the preceding equation:

$$xd = \left(\frac{2 \cdot \varepsilon si}{q \cdot DNB} \right)^{1/2}$$

The following equation calculates the body effect transition point:

$$V_{sbc} = \frac{qDP^2}{2\varepsilon si} \left(\frac{NI}{DP \cdot 1e-4} - DNB \right) + zDV_{SBC} + TDV_{SBC} = (t - t_{nom}) - Phid$$

If $v_{gs} \leq v_{th}$, this model inverts the surface and includes a residual DC current. If v_{sb} is large enough to make $v_{th} > v_{inversion}$, then v_{th} is the inversion threshold voltage.

To determine the residual current, simulation inserts $v_{inversion}$ into the ids , $vsat$, and mobility equation in place of v_{gs} (except for v_{gs} in the exponential term of the

subthreshold current). The following equation computes the inversion threshold voltage (v_{inlh}) at a specified v_{sb} :

$$v_{inlh} = v_{fb} - \frac{q \cdot NI}{cox} - v_{sb} + DVIN - zETA \Rightarrow ds$$

Cypress Depletion Model — Saturation Voltage, v_{dsat}

This equation determines the v_{sat} saturation voltage:

$$v_{sat} = v_{gs} - v_{fb} + v_{ch} + \frac{\gamma^2}{2} \cdot \left\{ 1 - \left[1 + \frac{4}{\gamma^2} \cdot (v_{gs} - v_{fb} + v_{ch} + v_{sb} + Phid) \right]^{1/2} \right\}$$

$$v_{dsat} = v_{sat}$$

Simulation modifies v_{sat} to include the carrier velocity saturation:

$$v_{dsat} = v_{sat} + vc - (v_{sat}^2 + vc^2)^{1/2}$$

The following equation calculates the vc value used in the preceding equation:

$$vc = ECV \cdot Leff$$

Cypress Depletion Model — Mobility Reduction, $UBeff$

The UB surface mobility depends on the terminal voltages:

$$UBeff = \frac{1}{\frac{1}{zUO} + \frac{(zFRC + zVFRC \cdot vde + zBFRC \cdot v_{sb}) \cdot (v_{gs} - v_{fb})}{TOX} + \frac{vde}{VST \cdot Le} + zFSB \cdot v_{sb}^{1/2}}$$

The following equations calculate Le for the preceding equation:

$$Le = Leff$$

Linear region

$$Le = Leff - \Delta L$$

Saturation region

At elevated temperatures, the following equation calculates the $zFRC$ value used in the preceding equation:

$$zFRC(t) = zFRC(tnom) \cdot \left(\frac{t}{tnom} \right)^{FRCEX}$$

ΔL is the channel length modulation effect, defined in the next section. v_{fb} assumes the role of v_{th} in the LEVEL 5 mobility equation. The degradation

parameters are semi-empirical, and are grouped according to their (linearized) mathematical dependencies instead of their physical origin to better provide parameter extraction.[7]

Cypress Depletion Model — Channel Length Modulation

To include the channel length modulation, modify the i_{ds} current:

$$i_{ds} = \frac{i_{ds}}{1 - \frac{\Delta L}{L_{eff}}}$$

The following equation calculates ΔL for the preceding equation:

$$\Delta L = 1e4 \cdot \left[\frac{2.73e3 \cdot XJ}{na1 \cdot \ln\left(\frac{1e20}{na1}\right)} \right]^{1/3} \cdot [(v_{ds} - v_{dsat} + PHI)^{1/3} - PHI^{1/3}]$$

ΔL is in microns, if XJ is in microns and $na1$ is in cm^{-3} .

Cypress Depletion Model — Subthreshold Current, i_{ds}

If device leakage currents become important for operation near or below the normal threshold voltage, the model considers the subthreshold characteristics. In the presence of surface states, this equation determines the effective threshold voltage (v_{on}):

$$v_{on} = \max(v_{th}, v_{in th}) + fast$$

The following equation calculates the $fast$ value used in the preceding equation:

$$fast = vt \cdot \left[1 + \frac{q \cdot FSS}{cox} + \frac{\gamma}{2 \cdot (Phid + vsb)^{1/2}} \right]$$

If $v_{gs} < v_{on}$, then:

$$Partial Enhancement, 0 < v_{gs} - v_{fb} < v_{de}$$

$$i_{ds} = \beta1 \cdot \left\{ q \cdot zKI0 \cdot NI \cdot v_{de} + cav \cdot \left[(v_{on} - v_{fb}) \cdot v_{de} - \frac{v_{de}^2}{2} \right] \right.$$

$$\left. - \frac{2}{3} \cdot cav \cdot \bar{\gamma} \cdot [(v_{de} + vsb + Phid)^{3/2} - (vsb + Phid)^{3/2}] + I_{crit} \right\}$$

Chapter 2: MOSFET Models

LEVEL 38: Cypress Depletion Model

$$+ \frac{1}{2} \cdot \left(\beta \cdot e^{\frac{vgs - von}{fast}} - \beta_1 \right) \cdot (von - vfb)^2$$

Full Enhancement, vgs-vfb -vde > 0

$$ids = \beta_1 \cdot \left\{ q \cdot zKI0 \cdot NI \cdot vde - \frac{2}{3} cav \right\} \cdot [(vde + vsb + Phid)^{3/2} - (vsb + Phid)^{3/2}] + Ic$$

$$\beta \cdot \left[(von - vfb) \cdot vde - \frac{vde^2}{2} \right] \cdot e^{\frac{vgs - von}{fast}}$$

Depletion, vgs-vfb < 0

$$ids = \beta_1 \cdot \left\{ q \cdot zKI0 \cdot NI \cdot vde + cav \cdot \left[(vgs - vfb) \cdot vde - \frac{vde^2}{2} \right] \right.$$

$$\left. - \frac{2}{3} cav \cdot \bar{\gamma} \cdot [(vde + vsb + Phid)^{3/2} - (vsb + Phid)^{3/2}] + Icrit \right\} \cdot e^{\frac{vgs - von}{fast}}$$

Cypress Depletion Model — Sample Model File

```
$ file Depstor.mod
.MODEL DEPSTOR NMOS LEVEL=38
* PARASITIC ELEMENTS
+ ACM=1
+ LD=0.15u WD=0.2u $ for LEFF AND WEFF
+ CJ=0.3E-16 MJ=0.4 PB=0.8 JS=2.0E-17 $ INTRINSIC DIODE
+ CJSW=0 MJSW=0.3
+ BULK=98 $ DEFAULT NODE FOR SUBSTRATE
* THRESHOLD
+ VTO=-2.5 LVT=-0.25 WVT=0
+ leta=0.02 eta=0.0 weta=0.0
+ TCV=0.003 $ TEMPERATURE COEFFICIENT
* MISC
+ DVIN=0.5 PHI=0.75
+ NFS=2e10 DNB=3.0E16
```

Mobility Model

```
+ UH=1300
+ UO=495    FRC=0.020  FSB=5e-5      VFRC=-1e-4      BFRC=-0
+ LUO=-100   LFRC=.03   LFSB=-1e-5    LVFRC=-.002    LBFR=-1e-3
+ WUO=-30    WFRC=-0.01  WFSB=5e-5    WVFR=-0.00     + WBFR=-0.4e-3
+ KI0=.9     KBETA1=.5   LKI0=0.16    LKBETA1=-0.15
+ WKI0=0.0    WKBETA1=-0.0
+ BEX=-1.3   TUH=-1.0   Frce=1.0
```

Body Effect

```
+ NWM=0.5    SCM=.1
+ DVSBC=0.1   LDVSBC=0   WDVSBC=0
+ TDVSBC=.002
+ BetaGam=0.9   LBetaGam=-.2  WBetaGam=.1
```

Saturation

```
+ ECV= 2.9   VST=8000   UHSAT=0
* CHANNEL LENGTH MODULATION
+ XJ=0.1
* OXIDE THICKNESS AND CAPACITANCE
+ TOX=165  CGSO=0  CAPOP=2
* CHANNEL IMPLANT
+ NI=1.5e12   KCS=3   DP=0.25
*.END
```

LEVEL 39: BSIM2 Model

BSIM2 (Berkeley Short-Channel IGFET Model 2) is the LEVEL 39 MOSFET model. The Synopsys implementation of this model is based on Berkeley SPICE 3E2.

To provide input to the Level 39 device model, assign the model parameters as for other device models. You can use a tabular model entry without model parameter names in BSIM1, but *not* in BSIM2.

This section covers the following topics:

- [BSIM2 Model Parameters](#)
 - [BSIM2 Model Equations](#)
 - [BSIM2 Model — Geometry and Bias of Model Parameters](#)
 - [BSIM2 Model — Compatibility Notes](#)
 - [BSIM2 Model — Preventing Negative Output Conductance](#)
 - [BSIM2 Model — Charge-based Gate Capacitance Model \(CAPOP=39\)](#)
 - [BSIM2 Model — Synopsys Device Model Enhancements](#)
 - [BSIM2 Model — Modeling Example](#)
 - [BSIM2 Model — Typical Listing](#)
-

BSIM2 Model Parameters

This model uses the generic MOSFET model parameters described in [Common MOSFET Model Parameters](#) section. In addition, this model also uses the following parameters:

Note: The Synopsys model does not use TEMP, DELL, and DFW parameters. The width and length sensitivity parameters are associated with the remaining parameters, except for TOX, VDD, VGG, VBB, DL, and DW. Unlike Berkeley SPICE, the Synopsys

MOSFET model has L and W sensitivity for $MU0$. This does not include the *generic* MOS parameters or the WL -product sensitivity parameters, which are Synopsys enhancements.

| Name (Alias) | Units | Default | Description |
|--------------|-------------------------------------|---------|--|
| AI0 | - | 0 | Impact ionization coefficient |
| AIB | V-1 | 0 | Sensitivity of the impact ionization coefficient to V_{bs} |
| BI0 | V | 0 | Impact ionization exponent |
| BIB | - | 0 | Sensitivity of the impact ionization exponent to V_{bs} |
| DELL | m | - | Length reduction of the source drain diffusion (not used in the Level 39 MOSFET model) |
| DL | m | 0 | Channel length reduction |
| DW | m | 0 | Channel width reduction |
| ETA0 | - | 0 | Drain-induced barrier lowering coefficient |
| ETAB | V-1 | 0 | Sensitivity of the drain-induced barrier lowering coefficient to V_{bs} |
| K1 | V-1 | 0.5 | Body effect coefficient |
| K2 | - | 0 | Second-order body effect coefficient (for nonuniform channel doping) |
| MU0 | cm ² /V· s | 400 | Low-field mobility |
| MU0B | cm ² /V ² · s | 0 | Sensitivity of low-field mobility to V_{bs} |
| MU20 | - | 0 | Empirical parameter for the output resistance |
| MU2B | V-1 | 0 | Sensitivity of the empirical parameter to V_{bs} |
| MU2G | V-1 | 0 | Sensitivity of the empirical parameter to V_{gs} |
| MU30 | cm ² /V ² · s | 0 | Empirical parameter for the output resistance |
| MU3B | cm ² /V ³ · s | 0 | Sensitivity of the empirical parameter to V_{bs} |
| MU3G | cm ² /V ³ · s | 0 | Sensitivity of the empirical parameter to V_{gs} |

Chapter 2: MOSFET Models

LEVEL 39: BSIM2 Model

| Name (Alias) | Units | Default | Description |
|--------------|-------------------------------------|---------|---|
| MU40 | cm ² /V ³ . s | 0 | Empirical parameter for the output resistance |
| MU4B | cm ² /V ⁴ . s | 0 | Sensitivity of the empirical parameter to V _{bs} |
| MU4G | cm ² /V ⁴ . s | 0 | Sensitivity of the empirical parameter to V _{gs} |
| MUS0 | cm ² /V. s | 600 | High-drain field mobility |
| MUSB | cm ² /V ² . s | 0 | Sensitivity of the high-drain field mobility to V _{bs} |
| N0 | - | 0.5 | Subthreshold swing coefficient |
| NB | V ^{1/2} | 0 | Sensitivity of the subthreshold swing to V _{bs} |
| ND | V ⁻¹ | 0 | Sensitivity of the subthreshold swing to V _{ds} |
| PHI | V | 0.8 | Surface potential |
| TEMP | C | - | Not used in Level 39 (see BSIM2 Model — Compatibility Notes on page 200) |
| TOX | m | 0.02 | Gate oxide thickness (assumes that TOX>1 is in Angstroms) |
| U10 | V ⁻¹ | 0 | High-drain field (velocity saturation) mobility reduction factor |
| U1B | V ⁻² | 0 | Sensitivity of the mobility reduction factor to V _{bs} |
| U1D | V ⁻² | 0 | Sensitivity of the mobility reduction factor to V _{ds} |
| UA0 | V ⁻¹ | 0 | First-order vertical-field mobility reduction factor |
| UAB | V ⁻² | 0 | Sensitivity of the first-order factor to V _{bs} |
| UB0 | V ⁻² | 0 | Second-order vertical-field mobility reduction factor |
| UBB | V ⁻³ | 0 | Sensitivity of the second-order factor to V _{bs} |
| VBB | V | -5 | Body supply voltage (NMOS convention) |
| VDD | V | 5 | Drain supply voltage (NMOS convention) |
| VFB | V | -0.3 | Flat band voltage |
| VGG | V | 5 | Gate supply voltage (NMOS convention) |

| Name (Alias) | Units | Default | Description |
|--------------|-------|---------|---|
| VGHIGH | V | 0 | Upper bound of the weak-strong inversion transition region |
| VGLOW | V | 0 | Lower bound of the weak-strong inversion transition region |
| VOF0 | - | 0 | Threshold offset (normalized to NKT/q) for the subthreshold |
| VOFB | V-1 | 0 | Sensitivity of the offset to V_{bs} |
| VOFD | V-1 | 0 | Sensitivity of the offset to V_{ds} |
| WDF | m | - | Default width (not used in the Level 39 MOSFET model); use <code>.OPTION DEFW=#</code> in the netlist instead |

Specify all BSIM2 parameters according to the NMOS convention, even for a PMOS model. Examples: `VDD=5`, not `-5`; `VBB=-5`, not `5`; and `ETA0=0 . 02`, not `-0 . 02`. See [BSIM2 Model — Compatibility Notes](#).

This MOSFET model also includes the `JSW[A/m]` source/drain bulk diode sidewall reverse saturation current density.

Other Device Model Parameters that Affect BSIM2

You must specify the following MOSFET model parameters before you can use some Synopsys enhancements, such as

- LDD-compatible parasitics.
- Adjusts the model parameter geometry, relative to a reference device.
- Impact ionization modeling with bulk-source current partitioning.
- Element temperature adjustment of the key model parameters.

This is a partial list. For complete information, see the following:

- [Calculating Effective Length and Width for AC Gate Capacitance](#)
- [MOSFET Diode Model — Drain and Source Resistance Parameters](#)
- [MOSFET Impact Ionization](#)

[BSIM2 Model — Compatibility Notes](#): [.MODEL VERSION Changes](#) describes how the `VERSION` parameter in the `.MODEL` statement changes the BSIM2 model, depending on the model version number.

BSIM2 Model Equations

In the following expressions, model parameters are in all upper case Roman. These expressions assume that you have already adjusted all model parameters for geometry, and that you have already adjusted parameters without a trailing 0 for the bias as appropriate. The exceptions are U1 and N for which the following equations explicitly calculate the bias dependences.

This section covers the following topics:

- BSIM2 Model — Threshold voltage, V_{th}
- BSIM2 Model — Strong inversion ($V_{gs} > V_{th} + VGHIGH$)
- BSIM2 Model — Weak Inversion ($V_{gs} < V_{th} + VGLOW$; [$VGLOW < 0$])
- BSIM2 Model — Strong inversion-to-weak inversion transition region ($V_{th} + VGLOW \leq V_{gs} \leq V_{th} + VGHIGH$)
- BSIM2 Model — Effective Length and Width: If DL is nonzero
- BSIM2 Model — Effective Length and Width: If DW is nonzero

BSIM2 Model — Threshold voltage, V_{th}

$$V_{th} = V_{bi} + K1\sqrt{PHI - V_{bs}} - K2(PHI - V_{bs}) - ETA \cdot V_{ds}$$

The following equation calculates the v_{bi} value used in the preceding equation:

$$V_{bi} = VFB + PHI$$

BSIM2 Model — Strong inversion ($V_{gs} > V_{th} + VGHIGH$)

Linear region ($V_{ds} < V_{dsat}$) drain-source current I_{DS} :

$$I_{DS} = \frac{\beta' \left(V_{gs} - V_{th} - \frac{a}{2} V_{ds} \right) V_{ds}}{1 + UA(V_{gs} - V_{th}) + UB(V_{gs} - V_{th})^2 + U1 \cdot V_{ds}}$$

The following equations calculate values used in the preceding equation:

$$V_{dsat} = \frac{V_{gs} - V_{th}}{a\sqrt{K}},$$

$$K = \frac{1 + V_c + \sqrt{1 + 2V_c}}{2},$$

$$V_c = \frac{U_{1S}(V_{gs} - V_{th})}{a[1 + UA(V_{gs} - V_{th}) + UB(V_{gs} - V_{th})^2]},$$

$$U_{1S} = U10 + U1B \cdot V_{bs},$$

$$U1 = U_{1S} \left[1 - \Theta(V_{dsat} - V_{ds}) \frac{U1D(V_{ds} - V_{dsat})^2}{V_{dsat}^2} \right]$$

In the preceding equations, $\Theta(x)$ is the usual unit step function:

$$\beta' = \beta_0 + \beta_1 \tanh\left(MU2 \frac{V_{ds}}{V_{dsat}}\right) + \beta_3 V_{ds} - \beta_4 V_{ds}^2$$

$$\beta_0 = \frac{W_{eff}}{L_{eff}} MU \cdot C_{ox},$$

$$\beta_1 = \beta_S - (\beta_0 + \beta_3 VDD - \beta_4 VDD^2),$$

$$\beta_i = \frac{W_{eff}}{L_{eff}} MUi \cdot C_{ox}, i = S, 3, 4, , a = 1 + \frac{gK1}{2\sqrt{PHI - V_{bs}}},$$

$$g = 1 - \frac{1}{1.744 + 0.8364(PHI - V_{bs})}$$

Saturation ($V_{ds} > V_{dsat}$) drain-source current, I_{DS} :

$$I_{DS} = \frac{\beta'(V_{gs} - V_{th})^2}{2aK[1 + UA(V_{gs} - V_{th}) + UB(V_{gs} - V_{th})^2]} \cdot (1+f)$$

In the preceding equation, the f impact ionization term is:

$$f = AI \cdot e^{\frac{-BI}{V_{ds} - V_{dsat}}}.$$

BSIM2 Model — Weak Inversion ($V_{gs} < V_{th} + VGLOW$; [$VGLOW < 0$])

Subthreshold drain-source current, I_{ds} :

$$I_{DS} = \beta' \cdot V_{tm}^2 \cdot \exp\left(\frac{V_{gs} - V_{th}}{N \cdot V_{tm}} + VOFF\right) \cdot \left[1 - \exp\left(-\frac{V_{ds}}{V_{tm}}\right)\right] \cdot (1+f)$$

Chapter 2: MOSFET Models

LEVEL 39: BSIM2 Model

The following equations calculate the V_{tm} and N values used in the preceding equation:

$$V_{tm} = \frac{kT}{q} \text{ and } N = N_0 + \frac{NB}{\sqrt{PHI - V_{bs}}} + ND \cdot V_{ds}$$

BSIM2 Model — Strong inversion-to-weak inversion transition region (V_{th} +VGLOW $\leq V_{gs} \leq V_{th}$ +VGHIGH)

$$V_{geff}(V_{gst}) = \sum_{j=0}^3 C_j V_{gst}^j$$

The preceding equation replaces $V_{gst}=V_{gs} - V_{th}$ in the linear or saturation drain currents, based on V_{dsat} (V_{geff}).

At the lower boundary ($V_{gs}-V_{th}=VGLOW$), the saturation equation is valid for all V_{ds} (that is, $V_{dsat}(V_{geff}(VGLOW)) \approx 0$) to allow a match to the above subthreshold equation.

To internally determine the C_j coefficients of the V_{geff} cubic spline, the I_{DS} and dI_{ds}/dV_{gs} conditions must both be continuous at the $V_{gs}=V_{th} + VGLOW$ and $V_{gs}=V_{th} + VGHIGH$ boundaries.

BSIM2 Model — Effective Length and Width: If DL is nonzero

$$L_{eff} = L_{scaled} \cdot LMLT - DL$$

$$LREF_{eff} = LREF_{scaled} \cdot LMLT - DL$$

Otherwise:

$$L_{eff} = L_{scaled} \cdot LMLT + XL_{scaled} - 2 \cdot LD_{scaled}$$

$$LREF_{eff} = LREF_{scaled} \cdot LMLT + XLREF_{scaled} - 2 \cdot LD_{scaled}$$

BSIM2 Model — Effective Length and Width: If DW is nonzero

$$W_{eff} = (W_{scaled} \cdot WMLT - DW) \cdot M$$

$$WREF_{eff} = (WREF_{scaled} \cdot WMLT - DW) \cdot M$$

Otherwise:

$$W_{eff} = (W_{scaled} \cdot WMLT + XW - 2 \cdot WD_{scaled}) \cdot M$$

$$WREF_{eff} = (WREF_{scaled} \cdot WMLT + XWREF_{scaled} - 2 \cdot WD_{scaled}) \cdot M$$

BSIM2 Model — Geometry and Bias of Model Parameters

Most of the BSIM2 parameters include width and length sensitivity parameters. You can also specify Synopsys-proprietary WL-product sensitivity parameters. If P is a parameter, then its associated width, length, and WL-product sensitivity parameters are WP, LP, and PP.

The value of the P' parameter, adjusted for width, length, and WL-product, is:

$$\begin{aligned} P' = P + WP \cdot \left(\frac{1}{W_{eff}} - \frac{1}{WREF_{eff}} \right) + LP \cdot \left(\frac{1}{L_{eff}} - \frac{1}{LREF_{eff}} \right) \\ + PP \cdot \left(\frac{1}{W_{eff}} - \frac{1}{WREF_{eff}} \right) \cdot \left(\frac{1}{L_{eff}} - \frac{1}{LREF_{eff}} \right) \end{aligned}$$

Berkeley SPICE does not use the WREF and LREF terms. They are effectively infinite, which is the default in the Level 39 MOSFET model.

The following BSIM2 parameters do not have associated geometry-sensitivity parameters:

- TOX
- TEMP (not used)
- VDD
- VGG
- VBB
- DL
- DW

BSIM2 parameters ending in 0 are valid at zero bias, and they have associated bias sensitivities, listed in the BSIM2 parameter table.

If PB, PD, and PG are the geometry-adjusted v_{bs} -, v_{ds} -, and v_{gs} - sensitivity parameters, and if they are associated with the P0 geometry-adjusted zero-bias parameter, then the following equation calculates the P bias-dependent parameter:

$$P = P0 + PB \cdot V_{bs} + PD \cdot V_{ds} + PG \cdot V_{gs}$$

The exceptions are the U1 velocity saturation factor and the N subthreshold swing coefficient. [BSIM2 Model — Synopsys Device Model: Modeling](#)

[Guidelines, Removing Mathematical Anomalies](#) shows expressions for their bias dependences.

BSIM2 Model — Compatibility Notes

This section covers the following topics:

- [BSIM2 Model — Compatibility Notes: SPICE3 Flag](#)
- [BSIM2 Model — Compatibility Notes: Temperature](#)
- [BSIM2 Model — Compatibility Notes: Parasitics](#)
- [BSIM2 Model — Compatibility Notes: Selecting Gate Capacitance](#)
- [BSIM2 Model — Compatibility Notes: Unused Parameters](#)
- [BSIM2 Model — Compatibility Notes: .MODEL VERSION Changes](#)

BSIM2 Model — Compatibility Notes: SPICE3 Flag

If you specify the `SPICE3=0` (default) model parameter, certain Synopsys corrections to the BSIM2 equations are effective. If you set the `SPICE3` value to 1, the equations are as faithful as possible to the BSIM2 equations for SPICE3E2. Even in this mode, certain numerical problems have been addressed and should not normally be noticeable.

BSIM2 Model — Compatibility Notes: Temperature

The default model reference temperature (`TNOM`) is 25°C in the Level 39 MOSFET model, unless you set `.OPTION SPICE`, which sets the `TNOM` default to 27° C. This option also sets some other SPICE compatibility parameters. In the Level 39 model, you set `TNOM` in an `.OPTION` line in the netlist; to override this locally (that is, for a model), use the `TREF` model parameter. (“Reference temperature” means that the model parameters were extracted at, and are therefore valid at, that temperature.)

UCB SPICE 3 does not use `TNOM` (default 27° C) for the BSIM models. Instead, you must specify the `TEMP` model parameter as both the model reference temperature and the analysis temperature. Analysis at `TEMP` applies only to thermally-activated exponentials in the model equations. You cannot adjust the model parameter values if you use `TEMP`. Simulation assumes that you extracted the model parameters at `TEMP`, because `TEMP` is both the reference and analysis temperature.

For model levels *other than* 4 (BSIM1) and 5 (BSIM2) in UCB SPICE3, simulation adjusts the key model parameters for the difference between `TEMP`

(default 27°C) and TNOM. To specify TEMP in the netlist, use .TEMP # as in the Level 39 MOSFET model.

In contrast to UCB SPICE's BSIM models, the Synopsys Level 39 MOSFET model does provide for temperature analysis. The default analysis temperature is 25°C in the Level 39 model. Set .TEMP # in your netlist to change the analysis temperature (you cannot use TEMP as a model parameter). The Level 39 MOSFET model adjusts the temperature of the key model parameters as explained in [BSIM Model — Temperature Effect](#).

BSIM2 Model — Compatibility Notes: Parasitics

ACM > 0 invokes the MOS source-drain parasitics in the Level 39 MOSFET device model. ACM=0 (default) is SPICE style. See [BSIM2 Model — Synopsys Device Model Enhancements](#).

BSIM2 Model — Compatibility Notes: Selecting Gate Capacitance

CAPOP=39 selects the BSIM2 charge-conserving capacitance model as shipped with Berkeley SPICE 3E2. This is the default selection if you set SPICE3=1.

- XPART (charge-sharing flag) is currently not a BSIM2 model parameter, despite its specification in the sample BSIM2 input decks shipped with Berkeley SPICE 3E. It appears that its use in SPICE 3E was as a printback debug aid.
- Saturation charge sharing appears to be fixed at 60/40 (S/D) in the BSIM2 capacitance model. For the charge equations, see [BSIM2 Model — Charge-based Gate Capacitance Model \(CAPOP=39\)](#). See also [BSIM2 Model — Synopsys Device Model: Modeling Guidelines, Removing Mathematical Anomalies](#).

You can choose other CAPOP values. CAPOP=13 (recommended) selects the BSIM1-based charge-conserving capacitance model for the MOSFET LEVEL 13 (BSIM1) or LEVEL 28 (modified BSIM1) device models. This option is the default selection if SPICE3=0. If you use this capacitance model, you can use the XPART or XQC model parameters to adjust charge sharing. See [LEVEL 13: BSIM Model](#) for more information.

BSIM2 Model — Compatibility Notes: Unused Parameters

The Level 39 MOSFET model does not use the DELL (S/D diode length reduction) and WDF (default device width) SPICE model parameters. SPICE 3E does not use the DELL function. You can specify a default width in the Level 39 MOSFET model, on the .OPTION line as DEFW (which defaults to 100μ).

Chapter 2: MOSFET Models

LEVEL 39: BSIM2 Model

BSIM2 Model — Compatibility Notes: .MODEL VERSION Changes

The Level 39 MOSFET model provides a VERSION parameter to the .MODEL statement, which lets you move LEVEL 13 BSIM and LEVEL 39 BSIM2 models between device model versions. Use the VERSION parameter in a LEVEL 13 .MODEL statement. The following table lists the changes in the BSIM model:

| Model Version | Effect of VERSION on BSIM2 Model |
|---------------|---|
| 92A | LEVEL 39 BSIM2 model introduced: no changes |
| 92B | No changes |
| 93A | Introduced gds constraints, fixed a defect in the WMU3B parameter, and introduced a defect in the MU4 parameter |
| 93A.02 | Introduced the VERSION parameter, and fixed an MU4 parameter defect |
| 95.1 | Fixed defects that caused PMUSB, LDAC, and WDAC parameter problems, fixed the GMBS defect if you used gds constraints |
| 96.1 | Limited ETA + ETAB · vb5 ≥ 0 |

BSIM2 Model — Preventing Negative Output Conductance

The Level 39 MOSFET model internally protects against conditions in the LEVEL 13 model that cause convergence problems due to negative output conductance. This model imposes the following constraints:

$$MU2 \geq 0 \quad ND \geq 0 \quad AI \geq 0$$

Simulation imposes these constraints after adjusting the length and width and setting the VBS dependence. This feature loses some accuracy in the saturation region, particularly at high Vgs.

Consequently, you might need to requalify the BSIM2 models in the following situations:

- Devices exhibit self-heating during characterization, which causes declining I_{ds} at high V_{ds} . This does not occur if the device characterization measurement sweeps V_{ds} .
- The extraction technique produces parameters that result in negative conductance.
- This model simulates the voltage outside the device's characterized range.

BSIM2 Model — Charge-based Gate Capacitance Model (CAPOP=39)

The BSIM2 gate capacitance model conserves charge and has non-reciprocal attributes. Using charges as state variables guarantees charge conservation. Charge partitioning is fixed at 60/40 (S/D) in saturation and is 50/50 in the linear region. $Q_s = -(Q_g + Q_d + Q_b)$ in all regions.

This section covers the following topics:

- [BSIM2 Model — CAPOP=39: Accumulation region \(\$V_{gs} < V_{bs} + V_{FB}\$ \)](#)
- [BSIM2 Model — CAPOP=39: Subthreshold region \(\$V_{bs} + V_{FB} < V_{gs} < V_{th} + VGLOW\$ \)](#)
- [BSIM2 Model — CAPOP=39: Saturation region \(\$V_{ds} > V_{dsat}\$ \)](#)

BSIM2 Model — CAPOP=39: Accumulation region ($V_{gs} < V_{bs} + V_{FB}$)

$$Q_g = C_{ox} W_{eff} \cdot L_{eff} (V_{gs} - V_{bs} - V_{FB})$$

$$Q_b = -Q_g$$

$$Q_d = 0$$

BSIM2 Model — CAPOP=39: Subthreshold region ($V_{bs} + V_{FB} < V_{gs} < V_{th} + VGLOW$)

$$Q_g = C_{ox} W_{eff} \cdot L_{eff} (V_{gs} - V_{bs} - V_{FB})$$

$$\left[1 - \frac{V_{gs} - V_{bs} - V_{FB}}{V_{gs} - V_{bs} - V_{FB} - V_{gst}} + \frac{1}{3} \left\{ \frac{V_{gs} - V_{bs} - V_{FB}}{V_{gs} - V_{bs} - V_{FB} - V_{gst}} \right\}^2 \right]$$

$$Q_b = -Q_g$$

$$Q_d = 0$$

Chapter 2: MOSFET Models

LEVEL 39: BSIM2 Model

BSIM2 Model — CAPOP=39: Saturation region ($V_{ds} > V_{dsat}$)

$$Q_g = \frac{2}{3}C_{ox}W_{eff} \cdot L_{eff} \cdot V_{gst} + Q_{bulk}$$

The following equations calculate values used in the preceding equation:

$$Q_{bulk} = \frac{1}{3}C_{ox}W_{eff} \cdot L_{eff}[V_{th} - V_{bs} - VFB]$$

$$Q_b = -Q_{bulk}$$

$$Q_d = -\frac{4}{10} \cdot \frac{2}{3}C_{ox}W_{eff} \cdot L_{eff} \cdot V_{gst} = \left(-\frac{4}{15}\right)C_{ox}W_{eff} \cdot L_{eff} \cdot V_{gst}$$

Linear region ($V_{ds} < V_{dsat}$):

$$Q_g = \frac{2}{3}C_{ox}W_{eff} \cdot L_{eff} \cdot V_{gst} \cdot \left[\frac{\frac{3}{2} \left(1 - \frac{V_{ds}}{V_{dsat}}\right) + \left(\frac{V_{ds}}{V_{dsat}}\right)^2}{2 - \frac{V_{ds}}{V_{dsat}}} \right] + Q_{bulk}$$

$$Q_b = -Q_{bulk}, Q_d = -\frac{1}{3}C_{ox}W_{eff} \cdot L_{eff} \cdot V_{gst}$$

$$\left[\frac{\frac{3}{2} \left(1 - \frac{V_{ds}}{V_{dsat}}\right) + \left(\frac{V_{ds}}{V_{dsat}}\right)^2}{2 - \frac{V_{ds}}{V_{dsat}}} + \frac{\frac{V_{ds}}{V_{dsat}} \left(1 - \frac{V_{ds}}{V_{dsat}}\right) + 0.2 \left(\frac{V_{ds}}{V_{dsat}}\right)^2}{\left(2 - \frac{V_{ds}}{V_{dsat}}\right)^2} \right] + Q_{bulk}$$

BSIM2 Model — Synopsys Device Model Enhancements

In the following expressions, model parameters are in all upper case Roman. Simulation assumes that you have already adjusted all model parameters without a trailing 0 for both geometry and bias as appropriate.

This section covers the following topics:

- BSIM2 Model — Synopsys Device Model: Temperature Effects
- BSIM2 Model — Synopsys Device Model: Alternate Gate Capacitance Model
- BSIM2 Model — Synopsys Device Model: Impact Ionization
- BSIM2 Model — Synopsys Device Model: Parasitic Diode for Proper LDD Modeling
- BSIM2 Model — Synopsys Device Model: Skewing of Model Parameters
- BSIM2 Model — Synopsys Device Model: HSPICE Optimizer
- BSIM2 Model — Synopsys Device Model: Modeling Guidelines, Removing Mathematical Anomalies

BSIM2 Model — Synopsys Device Model: Temperature Effects

LEVEL=39 enforces TLEV=1. You cannot currently use any other TLEV value. The following equation adjusts the threshold voltage for Level 39 TLEV=1:

$$V_{th}(T) = V_{bi}(T) + K1 \cdot \sqrt{\phi(T) - V_{bs}} - K2 \cdot (\phi(T) - V_{bs}) - ETA \cdot V_{ds}$$

The following equations calculate values used in the preceding equation:

$$V_{bi}(T) = V_{to}(T) - K1 \cdot \sqrt{\phi(T)} + K2 \cdot \phi(T)$$

$$V_{to}(T) = V_{to} - TCV \cdot (T - T_{nom})$$

In the preceding equations, the nominal-temperature, zero-bias threshold voltage is:

$$\begin{aligned} V_{to} &= V_{bi} + K1 \cdot \sqrt{PHI} - K2 \cdot PHI \\ &= VFB + PHI + K1 \cdot \sqrt{PHI} - K2 \cdot PHI, \end{aligned}$$

Simulation calculates $\phi(T)$ according to the specified TLEVc value.

The following equation adjusts the mobility:

$$\mu(T) = \mu(T_{nom}) \cdot \left(\frac{T}{T_{nom}} \right)^{BEX} \text{ where } \mu = \frac{\beta'}{C_{ox}(W_{eff}/L_{eff})}.$$

UIS adjusts the velocity saturation:

$$U1S(T) = U1S \cdot \left(\frac{T}{T_{nom}} \right)^{FEX}$$

Chapter 2: MOSFET Models

LEVEL 39: BSIM2 Model

This model also includes all of the usual Synopsys model adjustments to capacitances, parasitics, diodes, and resistors.

BSIM2 Model — Synopsys Device Model: Alternate Gate Capacitance Model

Select CAPOP=13 for the charge-conserving capacitance model, widely used with LEVEL=13 (BSIM1) and LEVEL=28 (improved BSIM1). See [LEVEL 13: BSIM Model](#) for more details.

BSIM2 Model — Synopsys Device Model: Impact Ionization

To select impact ionization modeling (instead of BSIM2), keep the AI0=0 value, and specify the ALPHA [ALPHA · ($V_{ds} - V_{dsat}$) replaces AI in equation for f in the BSIM2 equations section], VCR (replaces BI), and IIRAT (multiplies f) model parameters.

Synopsys impact ionization modeling differs from BSIM2 modeling in two ways:

- A bias term ($V_{ds} - V_{dsat}$) multiplies the exponential and ALPHA values.
- You can use the IIRAT model parameter to partition the impact ionization component of the drain current, between the source and the bulk. IIRAT multiplies f in the saturation I_{ds} equation. Thus, the IIRAT fraction of the impact ionization current goes to the source, and the 1-IIRAT fraction goes to the bulk, adding to IDB . IIRAT defaults to zero (that is, 100% of impact ionization current goes to the bulk).

BSIM2's impact ionization assumes that all of the impact ionization current is part of I_{ds} . In other words, it flows to the source. This assumption can lead to inaccuracies, for example, in cascode circuits.

BSIM2 Model — Synopsys Device Model: Parasitic Diode for Proper LDD Modeling

The Level 39 MOSFET model includes alternative MOS parasitic diodes to replace SPICE-style MOS parasitic diodes. You can use these alternatives to geometrically scale the parasitics with MOS device dimension, properly modeling the LDD parasitic resistances, shared sources and drains, and select different diode sidewall capacitances along the gate edge and field edge.

To select the MOS parasitic diode, use the ACM model parameter.

- ACM=0 (default) chooses SPICE style. The alternatives likely to be of most interest to the BSIM2 user are ACM=2 and 3.
- ACM=2 calculates the diode area based on W, xW, and HDIF (contact to gate spacing). You can override the calculation from the element line. You can specify LDIF (spacer dimension); RS and RD (source and drain sheet

resistance under the spacer) for LDD devices, and R_{SH} (sheet resistance of the heavily-doped diffusion). Thus, simulation properly calculates the total parasitic resistance of the LDD devices.

- ACM=3 uses all features of ACM=2. Its calculations of diode parasitics take into account the sharing of source/drains, and different junction sidewall capacitances along the gate and field edges. Use the GEO parameter to specify source/drain sharing from the element line. See [Using an ACM=3 MOS Diode](#) for details.

BSIM2 Model — Synopsys Device Model: Skewing of Model Parameters

As in any other Synopsys model, you can set up the BSIM2 model file for skewing to reflect the process variation. You can perform Worst-Case or Monte-Carlo analysis, based on fab statistics. For more information, see [Monte Carlo - Traditional Flow Statistical Analysis](#) or [Monte Carlo Analysis - Variation Block Flow](#) in the *HSPICE User Guide: Simulation and Analysis*.

BSIM2 Model — Synopsys Device Model: HSPICE Optimizer

You can tie the BSIM2 model, like any other HSPICE model, into the optimizer in a Synopsys circuit simulator to fit to actual device data. An example fit appears at the end of this chapter.

BSIM2 Model — Synopsys Device Model: Modeling Guidelines, Removing Mathematical Anomalies

Because of the somewhat arbitrary geometric and bias adjustments made in the original BSIM2 parameters, they can take on non-physical values or values that are not mathematically allowed in Berkeley SPICE 3. This can lead to illegal function arguments, program crashes, and unexpected model behavior (for example, negative conductance). You must satisfy the following guidelines and corrections at all geometries of interest, and at biases up to double the supply voltages (that is, to $V_{ds}=2 \cdot V_{DD}$, $V_{gs}=2 \cdot V_{GG}$, and $V_{bs}=2 \cdot V_{BB}$).

To avoid a drain current discontinuity at $V_{ds}=V_{dsat}$, be sure that $BI \neq 0$ if $AI0 \neq 0$.

To prevent negative g_{ds} , be sure that $ETA > 0$, $MU3 > 0$, and $MU4 < MU3 / (4 * VDD)$. This should ensure a positive g_{ds} value at biases up to double the supply voltages. To simplify matters, set all $MU4$ parameters to zero. You can obtain reasonably good fits to submicron devices without using $MU4$ [10].

In the Level 39 MOSFET model, $U1S$ cannot become negative. A negative $U1S$ is physically meaningless, and causes negative arguments in a square root function in one of the BSIM2 equations. The $U1D$ value should be less than unity (between 0 and 1).

For reasonable V_{th} behavior, make sure that:

$$K1 - 2K2 \cdot \sqrt{PHI - V_{bs}} \geq 0$$

For the equations to make sense, the following must hold: $N > 0$, $VGLOW \leq 0$, and $VGHIGH \geq 0$.

The BSIM2 gate capacitance model in SPICE 3E tends to display negative C_{gs} in the subthreshold. This is due to $C_{gg} > 0$ as $V_{gs} < V_{th}$ by construction of the gate charge equation so that $C_{gs} = C_{gg} - C_{gd} - C_{gb} > 0$. Therefore, use $CAPOP=13$ (default) until UC Berkeley releases an improved BSIM2 gate capacitance model.

BSIM2 Model — Modeling Example

The following is the result of fitting data from a submicron channel-length NMOS device to BSIM2. To fit this data, this example uses the Synopsys ATEM characterization software and the Synopsys simulation optimizer.

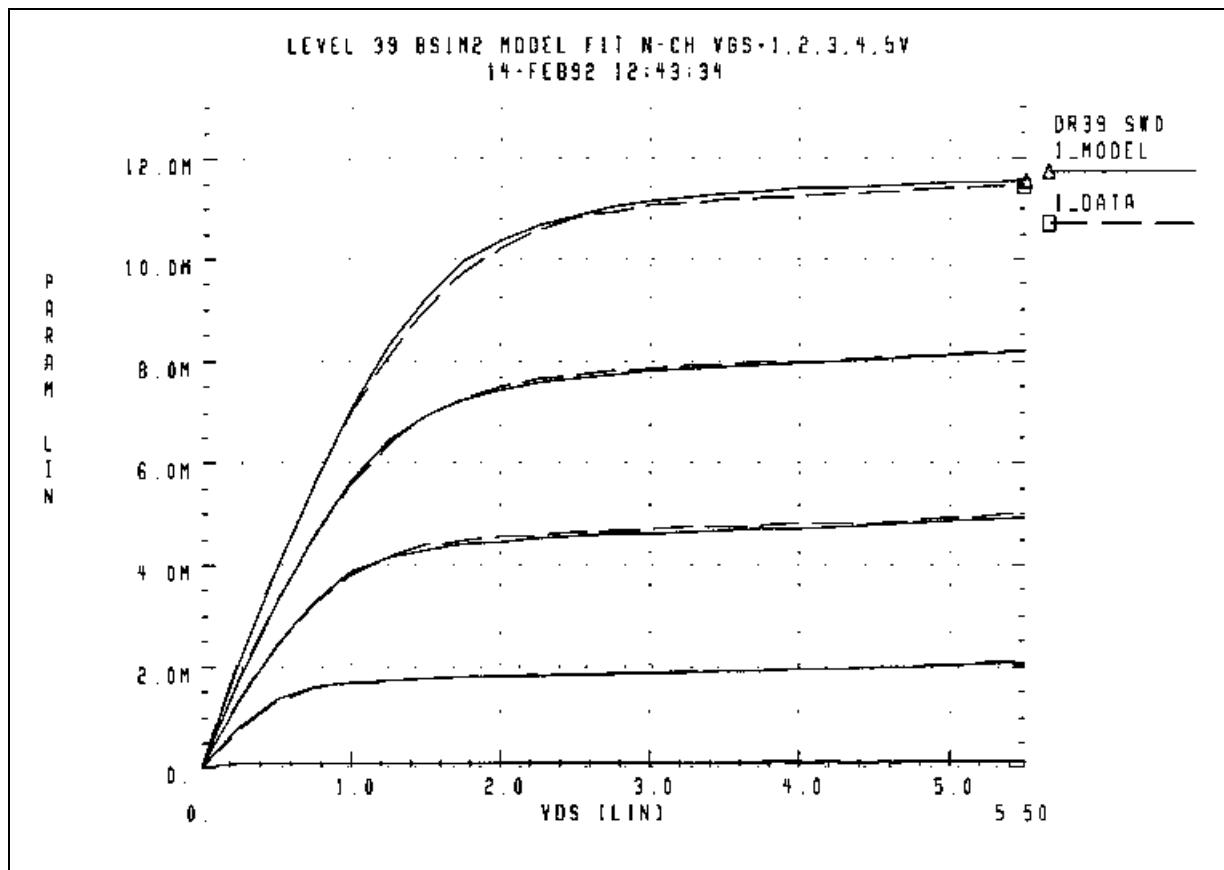


Figure 9 I_{DS} vs. V_{ds} for $V_{gs}=1, 2, 3, 4, 5V$; BSIM2 Model vs. Data

Chapter 2: MOSFET Models

LEVEL 39: BSIM2 Model

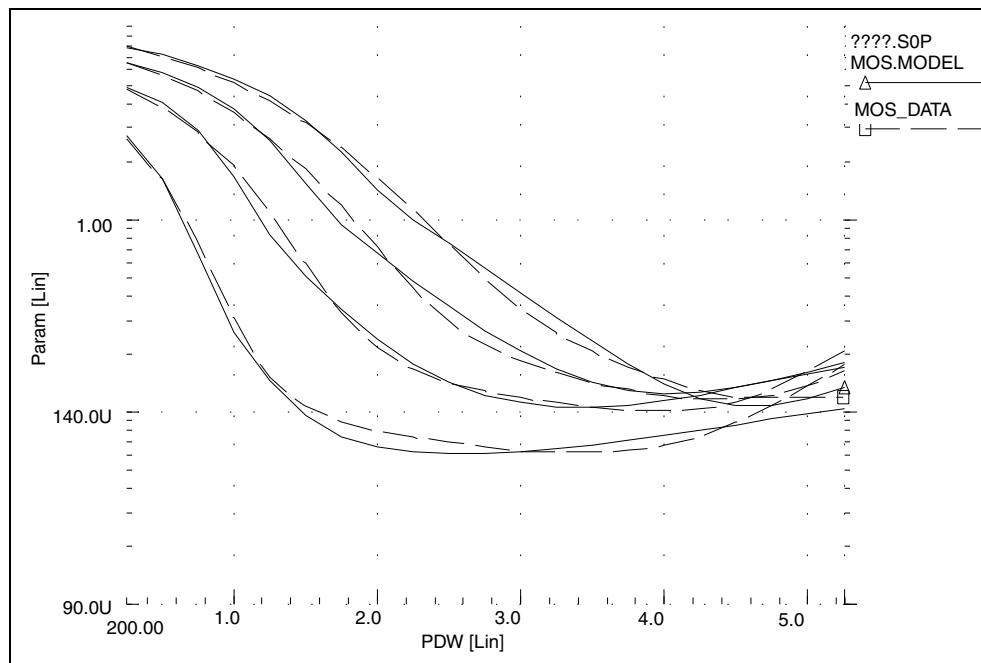


Figure 10 gds vs. Vds for $Vgs=2, 3, 4, 5V$; BSIM2 Model vs. Data, LOG scale

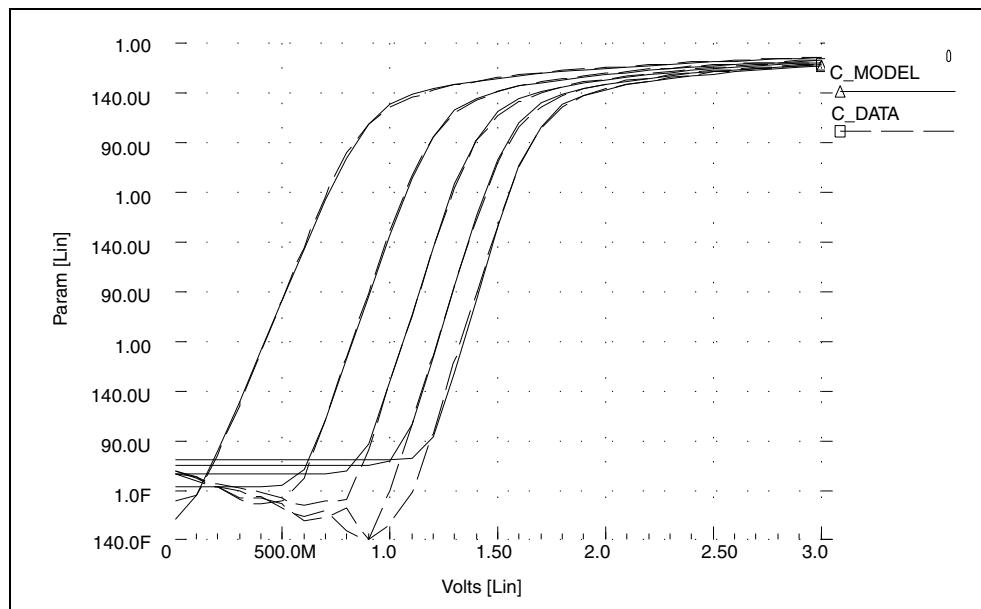


Figure 11 IDS vs. Vgs for $Vds=0.1V$, $Vbs=0, -1, -2, -3, -4V$, Showing Subthreshold Region; Model vs. Data

Chapter 2: MOSFET Models

LEVEL 39: BSIM2 Model

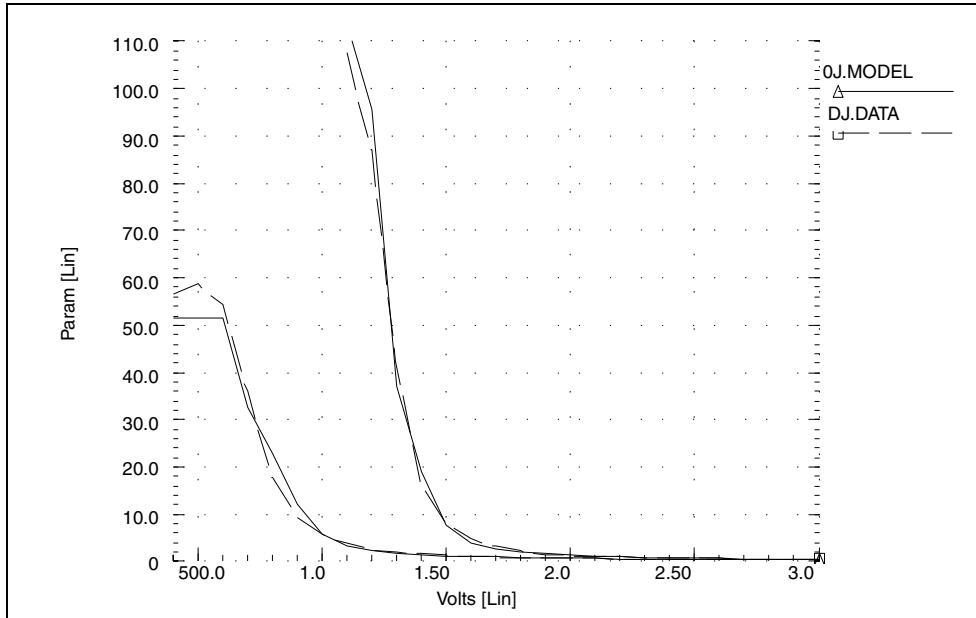


Figure 12 gm/I_{DS} vs. V_{gs} for $V_{ds}=0.1V$, $V_{bs}=0$, $-2V$; BSIM2 Model vs. Data

BSIM2 Model — Typical Listing

In this example, geometry sensitivities are set to zero because a fit at only one geometry has been performed. This example includes extra HSPICE parameters for LDD, temperature, and geometry.

```
.MODEL NCH NMOS LEVEL=39
+ TOX=2.000000E-02 TEMP=2.500000E+01
+ VDD=5.000000E+00 VGG=5.000000E+00
+ VBB =-5.000000E+00 DL =0.000000E+00
+ DW=0.000000E+00 VGHIGH=1.270000E-01
+ LVGHIGH=0.000000E+00 WVGHIGH=0.000000E+00
+ VGLOW =-7.820000E-02 LVGLOW=0.000000E+00
+ WVGLOW=0.000000E+00 VFB =-5.760000E-01
+ LVFB=0.000000E+00 WVFB=0.000000E+00
+ PHI=6.500000E-01 LPHI=0.000000E+00
+ WPHI=0.000000E+00 K1=9.900000E-01
+ LK1=0.000000E+00 WK1=0.000000E+00
+ K2=1.290000E-01 LK2=0.000000E+00
+ WK2=0.000000E+00 ETA0=4.840000E-03
+ LETA0=0.000000E+00 WETA0=0.000000E+00
+ ETAB =-5.560000E-03 LETAB=0.000000E+00
+ WETAB=0.000000E+00 MU0=3.000000E+02
+ MU0B=0.000000E+00 LMU0B=0.000000E+00
+ WMU0B=0.000000E+00 MUS0=7.050000E+02
+ LMUS0=0.000000E+00 WMUS0=0.000000E+00
+ MUSB=0.000000E+00 LMUSB=0.000000E+00
+ WMUSB=0.000000E+00 MU20=1.170000E+00
+ LMU20=0.000000E+00 WMU20=0.000000E+00
+ MU2B=0.000000E+00 LMU2B=0.000000E+00
+ WMU2B=0.000000E+00 MU2G=0.000000E+00
+ LMU2G=0.000000E+00 WMU2G=0.000000E+00
+ MU30=3.000000E+01 LMU30=0.000000E+00
+ WMU30=0.000000E+00 MU3B=0.000000E+00
+ LMU3B=0.000000E+00 WMU3B=0.000000E+00
+ MU3G =-2.970000E+00 LMU3G=0.000000E+00
+ WMU3G=0.000000E+00 MU40=0.000000E+00
+ LMU40=0.000000E+00 WMU40=0.000000E+00
+ MU4B=0.000000E+00 LMU4B=0.000000E+00
+ WMU4B=0.000000E+00 MU4G=0.000000E+00
+ LMU4G=0.000000E+00 WMU4G=0.000000E+00
+ UA0=0.000000E+00 LUA0=0.000000E+00
+ WUA0=0.000000E+00 UAB=0.000000E+00
+ LUAB=0.000000E+00 WUAB=0.000000E+00
+ UB0=7.450000E-03 LUB0=0.000000E+00
+ WUB0=0.000000E+00 UBB=0.000000E+00
+ LUBB=0.000000E+00 WUBB=0.000000E+00
+ U10=0.000000E+00 LU10=7.900000E-01
+ WU10=0.000000E+00 U1B=0.000000E+00
+ LU1B=0.000000E+00 WU1B=0.000000E+00
+ U1D=0.000000E+00 LU1D=0.000000E+00
+ WU1D=0.000000E+00 N0=8.370000E-01
+ LN0=0.000000E+00 WN0=0.000000E+00
+ NB =6.660000E-01 LNB=0.000000E+00
```

Chapter 2: MOSFET Models

LEVEL 39: BSIM2 Model

```
+ WNB=0.000000E+00 ND=0.000000E+00
+ LND=0.000000E+00 WND=0.000000E+00
+ VOF0=4.770000E-01 LVOF0=0.000000E+00
+ WVOF0=0.000000E+00 VOFB =-3.400000E-02
+ LVOFB=0.000000E+00 WVOFB=0.000000E+00
+ VOFD =-6.900000E-02 LVOFD=0.000000E+00
+ WVOFD=0.000000E+00 AI0=1.840000E+00
+ LAI0=0.000000E+00 WAIO=0.000000E+00
+ AIB=0.000000E+00 LAIB=0.000000E+00
+ WAIB=0.000000E+00 BI0=2.000000E+01
+ LBI0=0.000000E+00 WBIO=0.000000E+00
+ BIB=0.000000E+00 LBIB=0.000000E+00
+ WBIB=0.000000E+00 DELL=0.000000E+00
+ WDF=0.000000E+00
```

Common SPICE Parameters

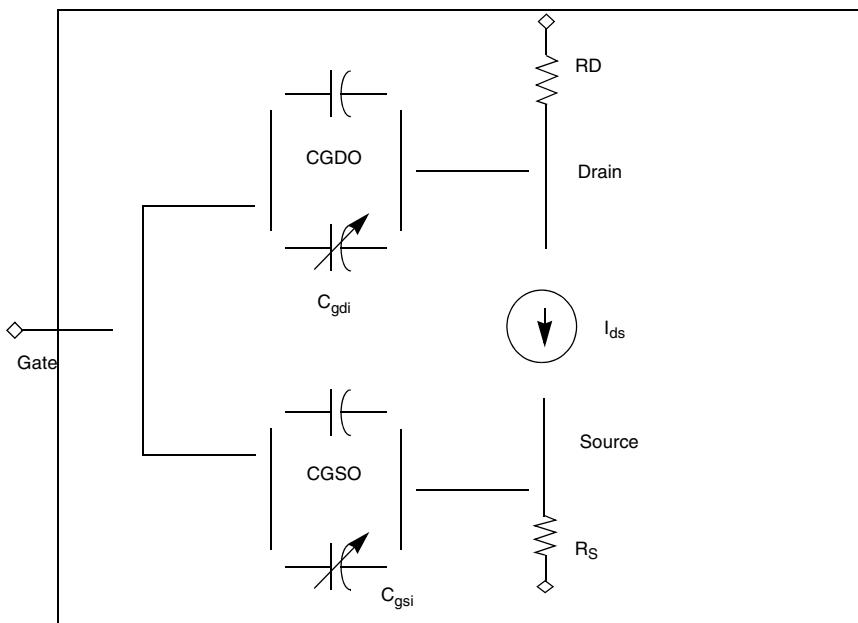
```
+ CGDO=1.000000E-09 CGSO=1.000000E-09
+ CGBO=2.500000E-11
+ RSH=3.640000E+01 JS=1.380000E-06
+ PB=8.000000E-01 PBSW=8.000000E-01
+ CJ=4.310000E-04 CJSW=3.960000E-10
+ MJ=4.560000E-01 MJSW=3.020000E-01
```

Synopsys Parameters

```
+ ACM=3 LMLT=8.500000E-01
+ WMLT=8.500000E-01
+ XL =-5.000000E-08 LD=5.000000E-08
+ XW=3.000000E-07 WD=5.000000E-07
+ CJGATE=2.000000E-10 HDIF=2.000000E-06
+ LDIF=2.000000E-07
+ RS=2.000000E+03 TRS=2.420000E-03
+ RD=2.000000E+03 TRD=2.420000E-03
+ TCV=1.420000E-03 BEX =-1.720000E+00
+ FEX =-2.820000E+00 LMU0=0.000000E+00
+ WMU0=0.000000E+00 JSW =2.400000E-12
```

LEVEL 40: HP a-Si TFT Model

The Synopsys Level 40 MOSFET device model represents a Hewlett-Packard amorphous silicon thin-film transistor model.



This model uses only the generic MOSFET model parameters described in [Common MOSFET Model Parameters](#) section.

This section covers the following topics:

- [Using the HP a-Si TFT Model](#)
- [HP a-Si TFT Model Equations](#)
- [HP a-Si TFT Model — Device Model and Element Statement Example](#)

Using the HP a-Si TFT Model

To use the HP a-Si TFT model:

1. Set `LEVEL=40` to identify the model as the HP a-Si TFT model.
2. Default value for L is $10\mu\text{m}$, and the default value for W is $40\mu\text{m}$.
3. Use the “M” designation for MOSFET rather than the “A” designation for a-Si TFT in the netlist.

Chapter 2: MOSFET Models

LEVEL 40: HP a-Si TFT Model

4. Use the “NMOS” or “PMOS” designation for device type rather than the “NAT” or “PAT” designation.
- Note:** Because of the unavailability of p-channel TFTs, PMOS model testing has been limited.
5. LEVEL 40 is a three-terminal model. It lacks bulk nodes so simulation does not append any parasitic drain-bulk or source-bulk diodes to this model. You can specify a fourth node, but it does not affect the simulation results (except for GMIN terms).
6. Parasitic resistances and overlap capacitances are constant. They are not scaled with width, length, and temperature.
7. Capacitance expressions in this model do not conserve charge.
8. The TREF parameter is an exponent in an expression for mobility temperature dependence.
9. Other models use the BEX parameter for similar mobility temperature dependence expressions. The HP a-Si TFT TREF model parameter is not the same as the TREF reference temperature in other models. The reference temperature for the HP a-Si TFT model is 312 K (or 38.85 °C); you cannot modify it. Experimental results from TFT manufacturers indicate that amorphous silicon materials are most stable at this temperature.
10. The default room temperature is 25° C in Synopsys circuit simulators, but is 27° C in most other simulators. When comparing to other simulators, set the nominal simulation temperature to 27° C by using either .TEMP 27 or .OPTION TNOM=27 in the netlist. Although the reference temperature of the HP a-Si TFT model is fixed at 312° K (or 38.85°C), the behavior of the model adjusts to other simulation temperatures that you specify, or that are defaults in Synopsys circuit simulators. In the Level 40 MOSFET model, temperature dependency is enabled.
11. The default CAPOP value is 40, which is the HP a-Si TFT non-charge-conserving capacitance model. CAPOP values of 0, 1, 2, 3, 4, 5, 9, 12, or 13 have not been thoroughly tested.
12. The DERIV default is zero, which selects the analytical method. Set DERIV to 1 to select the finite difference method.

This section covers the following topics:

- **HP a-Si TFT Model — Effect of SCALE and SCALM**
- **HP a-Si TFT Model — Noise Model**
- **HP a-Si TFT Model — DELVTO Element**

HP a-Si TFT Model — Effect of SCALE and SCALM

.OPTION SCALE has the same effect for LEVEL 40 as for other Synopsys device models, such as MOSFET Level 3 or Level 28. If you specify the L and W values in microns rather than meters (for example, L=1 rather than L=1m or 1e-6), set .OPTION SCALE=1e-6.

The SCALM option is disabled in the LEVEL 40 model. For standard MOSFET models (such as LEVEL 3), SCALM affects the scale of model parameters such as XL, XW, LD, WD, CJ, and CJSW.

Because the LEVEL 40 model ignores the SCALM option, you can mix LEVEL 40 models in a simulation with other models that use SCALM.

In general, netlists for Synopsys simulators should be as standard as possible. Also, you should convert L and W to meters scale instead of microns scale so that you can use the netlist without .OPTION SCALE=1E-6. If you follow these recommendations, a system-level simulation can use I/O sub-circuits from different vendors.

HP a-Si TFT Model — Noise Model

The LEVEL 40 model uses the standard NLEV=0 noise model inherited from other Synopsys MOSFET models.

HP a-Si TFT Model — DELVTO Element

You can use DELVTO and DTEMP on the element line with LEVEL 40.

HP a-Si TFT Model Equations

The following equations show model parameters in all capital letters; working variables are in lower case. Model parameters and the vgs and vds bias voltages are inputs. Ids, gm, and gds are the DC outputs. The Cgs gate-to-source capacitance and the Cgd gate-to-drain capacitance are the AC outputs. The electron charge is q, the Boltzmann's constant is k, and the permittivity of a vacuum is ϵ_0 .

This model applies the SCALE value before evaluating the equations, and scales by M after evaluation.

Chapter 2: MOSFET Models

LEVEL 40: HP a-Si TFT Model

gm_{tft} and gds_{tft} variables are intermediate, not final, quantities.

For a complete description of TFT technology and the device physics underlying these equations, see the Hewlett-Packard HP IC-CAP manual.

Initially, $Cgdi = 0$, $Cgsi = 0$, $phi = PHI$, $vto = VTO$, and $uo = UO$.

If $uo = 0$, then $uo = 1$.

The following equation computes the Cfm dielectric capacitance per unit area:

If $T1 \neq 0$ and $T2 \neq 0$, then $Cfm = \frac{(\epsilon_0 \cdot E1 \cdot E2)}{((T2 \cdot E1) + (T1 \cdot E2))}$

If $T1 = 0$ and $T2 \neq 0$, then $Cfm = \frac{(\epsilon_0 \cdot E2)}{T2}$

If $T2 = 0$ and $T1 \neq 0$, then $Cfm = \frac{(\epsilon_0 \cdot E1)}{T1}$

$$kp = uo \cdot Cfm \cdot 10^{-4}$$

TEMP is the Synopsys device simulation temperature, specified in oC, but converted to o K internally to evaluate these equations.

$$vt = \frac{(k \cdot TEMP)}{q}$$

$$eg = (2 \cdot 10^4 \cdot (TEMP - 312)) + 1.4$$

$$vto = vto + (DELVTOmodel \cdot type) + (DELVTOelement \cdot type)$$

$$vbi = vto, ratio = \frac{TEMP}{312}$$

If $VTIME \leq 1$, then $uo = uo \cdot (ratio^{TREF})$ and $kp = kp \cdot (ratio^{TREF})$

Note: TREF is an exponent in adjusting the temperature. It is not the reference temperature of this device model.

$$vfb = vto - (0.5 \cdot PHI) + (0.5 \cdot (1.4 - eg))$$

$$vbi = vfb + (0.5 + PHI \cdot ratio)$$

$$vto = vbi \text{ (printback definition)}$$

$$phi = phi \cdot ratio \text{ (printback definition)}$$

$$vfb = vbi - phi \text{ (printback definition)}$$

$$vdsat = 0$$

$$\text{beta} = kp \cdot W \cdot L$$

$$vth = vbi + (\text{ETA} \cdot vds)$$

If $NU \neq 0$ $K2 \neq 0$ $PSI \neq 0$ and $VTIME > 1$, then:

$$vth = vth + f(vgs, vds, NU, K2, PSI, CHI, VTIME, TEMP)$$

$$von = vth$$

If $NFS \neq 0$, then:

$$xn = 1 + \left(\frac{(q \cdot NFS \cdot 10^4 \cdot W \cdot L)}{Cfm} \right)$$

$$von = f(vth, (vt \cdot xn))$$

This section covers the following topics:

- HP a-Si TFT Model — Cutoff Region ($NFS=0$, $vgs \leq von$)
- HP a-Si TFT Model — Noncutoff Region ($NFS \neq 0$)
- HP a-Si TFT Model — Cgd , Cgs

HP a-Si TFT Model — Cutoff Region ($NFS=0$, $vgs \leq von$)

If $NFS = 0$ and $vgs \leq von$, then:

$$Cgdi = 0$$

$$Cgsi = 0$$

$$Ids = GO \cdot f(vgs, (DEFF \cdot vds))$$

$$gm = GO \cdot gds = GO \cdot DEFF$$

HP a-Si TFT Model — Noncutoff Region ($NFS \neq 0$)

- If $vgs > von$, then $vgsx = vgs$.
- If $vgs \leq von$, then $vgsx = von$.

Mobility modulation by vgs :

$$ueff = f(uo, \eta, vgs, THETA)$$

If $VMAX > 0$, then:

$$vdsc = \frac{L \cdot VMAX}{ueff}$$

Chapter 2: MOSFET Models

LEVEL 40: HP a-Si TFT Model

$$vdsat = (vgsx - vth) + vdsc - \sqrt{((vgsx - vth)^2 + vdsc^2)}$$

$$Cfmlw = \frac{(Cfm \cdot CSC)}{(Cfm + CSC)} \cdot L \cdot W$$

$Cfmlw$ is the series combination of the dielectric and space charge capacitance for the MIS structure.

If $vds < vdsat$, then:

$$vdsx = vds$$

$$\epsilon psfm = Cfm \cdot \frac{(T2 + T1)}{\epsilon_0}$$

$\epsilon psfm$ is the effective equivalent dielectric constant of the insulator layers.

$$fval = 0.8 + \left(\frac{\epsilon psfm - 0.8}{1 + (2 \cdot \pi \cdot FREQ \cdot TAU)^2} \right)$$

$$Cgdi = f(Cfmlw \cdot f(efm, 0.8) \cdot (\exp(fval, FEFF, vgs - vth - vds)))$$

$$Cgsi = f(Cfmlw \cdot f(efm, 0.8) \cdot (\exp(fval, FEFF, (vgs - vth), vds)))$$

Otherwise, $vds \geq vdsat$:

$$vdsx = vdsat$$

$$Cgdi = Cfmlw$$

$$Cgsi = \frac{Cfmlw}{2}$$

If $vdsx \neq 0$, then

$$cdnorm = vdsx \cdot \left(vgsx - vth - \frac{vdsx}{2} \right)$$

Normalized drain current:

$$gm_{tft} = vdsx$$

$$gds_{tft} = vgsx - vth - vdsx$$

$$cd1 = beta \cdot cdnorm$$

Drain current without velocity saturation effect:

$$\text{beta} = \text{beta} \cdot \text{fgate}, \text{idrain} = \text{beta} \cdot \text{cdnorm}$$

$$gm_{tft} = (\text{beta} \cdot gm_{tft}) + (dfgdvg \cdot cd1)$$

Velocity saturation factor—if $v_{MAX} \neq 0$, then:

$$fdrain = \frac{1}{\left(1 + \left(\frac{v_{dsx}}{vdsc}\right)\right)}$$

$$dfddvg = -dfgdvg \cdot \frac{((fdrain)^2) \cdot v_{dsx}}{(vdsc \cdot fgate)}$$

$$dfddvd = \frac{-(fdrain)^2}{vdsc}$$

Strong inversion current:

$$gm_{tft} = (fdrain \cdot gm_{tft}) + (dfddvg \cdot idrain)$$

$$gds_{tft} = (fdrain \cdot gds_{tft}) + (dfddvd \cdot idrain)$$

$$idrain = fdrain \cdot idrain, \text{beta} = \text{beta} \cdot fdrain$$

$$Ids = idrain \cdot f(GO, vgs, DEFF, vds)$$

$$gm = f(gm_{tft}, GO)$$

$$gds = f(gds_{tft}, GO, DEFF)$$

Weak inversion current—if $v_{gs} < von$, then:

$$idrain = idrain \cdot \exp\left(\frac{(vgs - von)}{(vt \cdot xn)}\right)$$

$$Ids = idrain + f(GO, vgs, DEFF, vds)$$

$$gm_{tft} = \frac{idrain}{(vt \cdot xn)}, gm = f(gm_{tft}, GO)$$

$$gds_{tft} = gds_{tft} \cdot \exp\left(\frac{(vgs - von)}{(vt \cdot xn)}\right)$$

$$gds = gds_{tft} + f(GO, DEFF)$$

Chapter 2: MOSFET Models

LEVEL 40: HP a-Si TFT Model

$vdsx = 0 :$

$Ids = f(GO \cdot vgs, DEFF, vds)$

$gm = GO$

$gds_{tft} = beta \cdot (vgsx - vth)$

If $NFS \neq 0$ and $vgs < von$, then:

$$gds_{tft} = gds_{tft} \cdot \exp\left(\frac{(vgs - von)}{(vt \cdot xn)}\right), gds = f(gds_{tft}, GO, DEFF)$$

HP a-Si TFT Model — Cgd, Cgs

$$Cgd = Cgdi + CGDO, Cgs = Cgsi + CGSO$$

HP a-Si TFT Model — Device Model and Element Statement Example

```
.MODEL nch nmos LEVEL=40 UO=0.4229 VTO=1.645 PHI=1.25 NSS=0
+ NFS=2.248E+21 VMAX=1231
+ THETA=-0.01771 ETA=0.0002703 T1=2.6E-07 T2=0 E1=3.9
E2=0
+ GO=9.206E-15 NU=0 K2=2 CHI=0.5
+ PSI=1E-20 VTME=0.01 TREF=1.5 CGSO=5.203E-14
CGDO=4.43E-14
+ CSC=0.0001447 RD=5097
+ RS=5097 FREQ=1E+06 DEFF=2.15 TAU=1.64E-07 FEFF=0.5
MCKT 1 2 3 nch L=1e-05 W=4e-05
```

LEVEL 47: BSIM3 Version 2 MOSFET Model

The BSIM3 version 2.0 MOS model from UC Berkeley is available as the Synopsys Level 47 model.

The following sections discuss these topics:

- [Using the BSIM3 Version 2 MOSFET Model](#)
 - [BSIM3 Version 2 MOSFET Model Parameters](#)
 - [BSIM3 Version 2 MOSFET Model Equations](#)
 - [BSIM3 Version 2 MOSFET Model — Usage Notes](#)
 - [BSIM3 Version 2 MOSFET Model — PMOS Model Example](#)
-

Using the BSIM3 Version 2 MOSFET Model

The Level 47 model uses the same model parameters for the source/drain diode current, capacitance, and resistance as used in the other supported MOS levels. The `ACM` model parameter controls the choice of source/drain equations.

The Level 47 model also uses the same noise equations as the other MOSFET model levels. The `NLEV` parameter controls the choice of noise equations.

This model, like all Synopsys simulation device models, can include parameters. You can use these parameters to model the process skew, either by worst-case corners or by Monte Carlo. For information about Worst-Case and Monte Carlo analysis, see [Worst Case Analysis](#) and [Monte Carlo Analysis](#) in the *HSPICE User Guide: Simulation and Analysis*.

BSIM3 Version 2 MOSFET Model Parameters

| Name | Unit | Default | Description |
|------|------|---------|--|
| A0 | | 1 | Bulk charge effect. Default is 4.4 for PMOS. |
| A1 | 1/V | 0 | First nonsaturation factor (0 for NMOS, 0.23 for PMOS) |

Chapter 2: MOSFET Models

LEVEL 47: BSIM3 Version 2 MOSFET Model

| Name | Unit | Default | Description |
|---------|-------------------|---|---|
| A2 | | 1.0 | Second nonsaturation factor (1.0 for NMOS, 0.08 for PMOS) |
| AT | m/sec | 3.3e4 | Temperature coefficient of VSAT |
| BULKMOD | | 1 | Bulk charge model selector |
| CDSC | F/m ² | 2.4e-4 | Drain/source and channel coupling capacitance |
| CDSCB | F/Vm ² | 0 | Body coefficient for CDSC |
| CIT | F/m ² | 0.0 | Interface state capacitance |
| DL | m | 0.0 | Channel length reduction on one side (multiplied by SCALM) |
| DSUB | | DROUT | DIBL coefficient in the subthreshold region |
| DVT0 | | 2.2 | Short-channel effect coefficient 0 |
| DVT1 | | 0.53 | Short-channel effect coefficient 1 |
| DVT2 | 1/V | -0.032 | Short-channel effect coefficient 2 |
| DW | m | 0.0 | Channel width reduction on one side (multiplied by SCALM) |
| EM | V/m | 4.1e7 | Electrical field in the channel above which the hot carrier effect dominates |
| ETA | | 0.3 | Coefficient of the drain voltage reduction |
| ETA0 | | 0.08 | DIBL (Drain Induced Barrier Lowering) coefficient for the subthreshold region |
| ETAB | 1/V | -0.07 | Subthreshold region DIBL coefficient |
| GAMMA1 | V ^{1/2} | See BSIM3 Version 2 MOSFET Model Equations. | Body effect coefficient, near interface |
| GAMMA2 | V ^{1/2} | See BSIM3 Version 2 MOSFET Model Equations. | Body effect coefficient in the bulk |
| K1 | V ^{1/2} | 0.53 | First-order body effect coefficient |
| K2 | | -0.0186 | Second-order body effect coefficient |

| Name | Unit | Default | Description |
|---------|-----------------------------|--|--|
| K3 | | 80.0 | Narrow width effect coefficient |
| K3B | 1/V | 0 | Body width coefficient of the narrow width effect |
| KETA | 1/V | -0.047 | Body bias coefficient of the bulk charge effect |
| KT1 | V | -0.11 | Temperature coefficient for the threshold voltage |
| KT1L | Vm | 0 | Channel length sensitivity of the temperature coefficient for the threshold voltage |
| KT2 | | 0.022 | Body bias coefficient of the threshold temperature effect |
| LDD | m | 0.0 | Total length of the LDD region |
| LITL | m | | Characteristic length. Default is: $LITL = \left(\frac{\epsilon_{si} T_{ox} X_j}{\epsilon_{ox}} \right)^{1/2}$ |
| NFACTOR | | 1.0 | Subthreshold region swing |
| NLX | m | 1.74e-7 | Lateral nonuniform doping along the channel |
| NPEAK | cm ⁻³ See (8) | 1.7e17 | Peak doping concentration near the interface |
| NSUB | cm ⁻³ | 6.0e16 | Substrate doping concentration |
| PHI | V | See BSIM3 Version 2 MOSFET Model Equations . | Surface potential under strong inversion |
| PSCBE1 | V/m | 4.24e8 | Exponent 1 for the substrate current induced body effect |
| PSCBE2 | m/V | 1.0e-5 | Coefficient 2 for the substrate current induced body effect |
| PVAG | | 0 | Gate dependence of the output resistance |
| RDS0 | ohm | 0.0 | Source drain contact resistance |
| RDSW | ohm · μm | 0.0 | Source drain resistance per unit width |
| SATMOD | | 2 | Saturation model selector |

Chapter 2: MOSFET Models

LEVEL 47: BSIM3 Version 2 MOSFET Model

| Name | Unit | Default | Description |
|----------------|-------------------------------------|--|--|
| SUBTHMOD | | 2 | Subthreshold model selector |
| TNOM (TREF) | °C | 25 | Temperature at which simulation extracts parameters. This parameter defaults to the TNOM option, which defaults to 25°C. See 4 and 5 in BSIM3 Version 2 MOSFET Model — Usage Notes . |
| TOX | m | 150e-10 | Gate oxide thickness |
| U0 | m^2/Vsec See (8) | 0.067 | Low field mobility at T=TREF <ul style="list-style-type: none"> ■ 0.067 for n-channel ■ 0.025 for p-channel |
| UA | m/V | 2.25e-9 | First-order mobility degradation coefficient |
| UA1 | m/V | 4.31e-9 | Temperature coefficient of UA |
| UB | m^2/V^2 | 5.87e-19 | Second-order mobility degradation coefficient |
| UB1 | m^2/V^2 | -7.61e-18 | Temperature coefficient of UB |
| UC | 1/V | 0.0465 | Body bias sensitivity coefficient of mobility |
| UC0* | $(\text{V}/\text{m})^2$ | | Temperature coefficient |
| UC1 | 1/V | -0.056 | Temperature coefficient of UC |
| UTE | | -1.5 | Mobility temperature exponent |
| VBM | V | -5.0 | Maximum substrate bias |
| VBX | V | See BSIM3 Version 2 MOSFET Model Equations . | V_{bs} at which the depletion width equals XT |
| VFB | V | | Flat-band voltage |
| VGHIGH | V | 0.12 | Upper bound of the weak-strong inversion transition region |
| VGLOW | V | -0.12 | Lower bound of the weak-strong inversion transition region |
| VOFF | V | -0.11 | Offset voltage in the subthreshold region |
| VSAT | cm/sec | 8e6 | Saturation velocity of the carrier at T=TREF |

| Name | Unit | Default | Description |
|-------|------|---------|---|
| VTH0 | V | 0.7 | Threshold voltage of the long channel at $V_{bs}=0$ and small V_{ds} ■ 0.7 for n-channel. ■ -0.7 for p-channel. |
| W0 | m | 2.5e-6 | Narrow width effect coefficient |
| XJ | m | 0.15e-6 | Junction depth |
| XPART | | 1 | Charge partitioning flag |
| XT | m | 1.55e-7 | Doping depth |

* UC0 has no effect on the model

BSIM3 Version 2 MOSFET Model Equations

The following model equations are based on the BSIM3 source code:

- [BSIM3 Version 2 Model — \$L_{eff}\$ and \$W_{eff}\$ Equations](#)
- [BSIM3 Version 2 Model — Threshold Voltage Parameters](#)
- [BSIM3 Version 2 Model — Mobility Parameters](#)
- [BSIM3 Version 2 Model — Drain Saturation Voltage Parameters](#)
- [BSIM3 Version 2 Model — Linear Region](#)
- [BSIM3 Version 2 Model — Saturation Region Parameters](#)
- [BSIM3 Version 2 Model — Drain Current Parameters](#)
- [BSIM3 Version 2 Model — Subthreshold Region Parameters](#)
- [BSIM3 Version 2 Model — Transition Region Parameterds \(subthMod=2\)](#)
- [BSIM3 Version 2 Model — Temperature Compensation Parameters](#)

BSIM3 Version 2 Model — L_{eff} and W_{eff} Equations

The standard equations for L_{eff} and W_{eff} in the Synopsys model are:

$$L_{eff} = L + XL - (2 \cdot LD)$$

$$W_{eff} = W + XW - (2 \cdot WD)$$

BSIM3 uses the following UCB SPICE3 equations:

Chapter 2: MOSFET Models

LEVEL 47: BSIM3 Version 2 MOSFET Model

$$L_{eff} = L - (2 \cdot DL)$$

$$W_{eff} = W - (2 \cdot DW)$$

The units for these parameters are meters with defaults of zero.

Simulation uses the standard Synopsys model equation for both cases, and accepts `DL(DW)` as the value for `LD(WD)`. If you specify both `LD(WD)` and `DL(DW)` in a `.MODEL` statement, simulation uses the `LD(WD)` value.

If you specify `LDAC` and `WDAC` in the `.MODEL` statement, then:

$$L_{eff}=L+XL-2 \cdot LDAC, \quad W_{eff}=W+XW-2 \cdot WDAC$$

This model uses the `LD(DL)` and `WD(DW)` values with the `RS` and `RD` parameters for `ACM>0`.

In the following two models return the same simulation results:

```
* HSPICE style:  
.MODEL n1 nmos Level=47 XL=0.1e6 LD=0.15e-6  
+ SatMod=2 SubthMod=2 BulkMod=1  
+ CGSO=0.3e-9 CGDO=0.3e-9 CGBO=0  
* SPICE3 style:  
.MODEL n2 nmos Level=47 LD=0.1e-6  
+ SatMod=2 SubthMod=2 BulkMod=1  
+ CGSO=0.3e-9 CGDO=0.3e-9 CGBO=0
```

BSIM3 Version 2 Model — Threshold Voltage Parameters

$$V_{th0}, \quad K1, \quad K2, \quad \phi_s, \quad N_{lx}, \quad K3, \quad W_0, \quad T_{ox}, \quad V_{bi}, \quad D_{vt0}, \quad D_{vt1},$$

$$D_{vt2}, \quad N_{peak}, \quad N_{sub}, \quad \Upsilon_1, \quad \Upsilon_2, \quad V_{bx}, \quad V_{bm}, \quad V_{bi}, X_t, \quad TREF$$

$$V_{th} = V_{th0} + K1(\sqrt{\phi_s - V_{bs}} - \sqrt{\phi_s}) - K2V_{bs} + K1\left(\sqrt{1 + \frac{N_{lx}}{L_{eff}}\sqrt{\frac{\phi_s}{\phi_s - V_{bs}}} - 1}\right)\sqrt{\phi_s}$$

$$+ (K3 + K3B \cdot V_{bs}) \cdot \left(\frac{T_{ox}}{W_{eff} + W_0}\right)\phi_s - \Delta V_{th}$$

$$T_{ratio} = \frac{(TEMP + DTEMP + 273.15)}{(TREF + 273.15)}$$

$$\Delta V_{th} = \theta_{th}(L_{eff}) \cdot (V_{bi} - \phi_s)$$

$$\theta_{ih}(L_{eff}) = D_{vt0} \cdot \left[\exp\left(\frac{-D_{vt1} \cdot L_{eff}}{2l_t}\right) + 2 \exp\left(\frac{-D_{vt1} \cdot L_{eff}}{l_t}\right) \right]$$

$$l_t = \sqrt{3 \cdot T_{ox} \cdot X_{dep}} \cdot (1 + D_{vt2} \cdot V_{bs})$$

$$X_{dep} = \sqrt{\frac{2 \cdot \epsilon_{si} \cdot (\phi_s - V_{bs})}{q \cdot N_{peak}}}$$

If you do not specify `Phi` as a model parameter, then:

$$\phi_s = 2 \cdot V_{tm} \cdot \ln\left(\frac{N_{peak}}{n_i}\right) \text{ (Npeak and ni in cm-3)}$$

$$V_{tm} = K \cdot T / q$$

$$n_i = 1.45e10 \cdot \left(\frac{T}{300.15}\right)^{1.5} \cdot \exp(21.5565981 - Eg / (2 \cdot V_{tm}))$$

$$Eg = 1.16 - (7.02e-4) \cdot T^2 / (T + 1108.0)$$

If you do not specify `K1` and `K2` as model parameters, simulation calculates them as follows:

$$K_1 = \Upsilon_2 - 2 \cdot K_2 \cdot \sqrt{\phi_s - V_{bm}}$$

$$K_2 = (\Upsilon_1 - \Upsilon_2) \cdot \frac{\sqrt{\phi_s - V_{bx}} - \sqrt{\phi_s}}{2 \cdot \sqrt{\phi_s} \cdot (\sqrt{\phi_s - V_{bm}} - \sqrt{\phi_s}) + V_{bm}}$$

$$\Upsilon_1 = \frac{\sqrt{2 \cdot q \cdot \epsilon_{si} \cdot N_{peak}}}{C_{ox}}, \quad \Upsilon_2 = \frac{\sqrt{2 \cdot q \cdot \epsilon_{si} \cdot N_{sub}}}{C_{ox}}$$

$$V_{bx} = \phi_s - \left(\frac{q \cdot N_{peak} \cdot X_t^2}{2 \cdot \epsilon_{si}} \right)$$

If you do not specify `Vbi` as a model parameter, then:

$$V_{bi} = \frac{k \cdot T}{q} \cdot \ln\left(\frac{1.0e22 \cdot N_{peak}}{n_i^2}\right)$$

Chapter 2: MOSFET Models

LEVEL 47: BSIM3 Version 2 MOSFET Model

BSIM3 Version 2 Model — Mobility Parameters

$$\mu_0, \quad U_a, \quad U_b, \quad U_c$$

$$\mu_{eff} = \frac{\mu_0}{1 + U_a \cdot \left(\frac{V_{gs} + V_{th}}{T_{ox}} \right) + U_b \cdot \left(\frac{V_{gs} + V_{th}}{T_{ox}} \right)^2 + U_c \cdot V_{bs}}$$

BSIM3 Version 2 Model — Drain Saturation Voltage Parameters

$$A_0, \quad v_{sat}, \quad X_j, \quad A_1, \quad A_2, \quad R_{ds0}, \quad R_{ds_w}$$

Rds and Pfactor:

$$R_{ds} = R_{ds0} + R_{ds_w} / (1e6 \cdot W_{eff})$$

$$Pfactor = A_1 \cdot V_{gst} + A_2$$

If Pfactor > 1, simulation sets it to Pfactor=1.

$$V_{gst} = V_{gs} - V_{th}$$

If Rds=0 and Pfactor=1, then:

$$V_{dsat} = \frac{E_{sat} \cdot L_{eff} \cdot V_{gst}}{A_{bulk} \cdot E_{sat} \cdot L_{eff} + V_{gst}}$$

For BULKMOD=1:

$$A_{bulk} = \left(1 + \frac{K1 \cdot A_0 \cdot L_{eff}}{(L_{eff} + T1) \cdot T1s \cdot 2} \right) / (1 + KETA \cdot V_{bs})$$

For BULKMOD=2:

$$A_{bulk} = \left(\frac{K1 \cdot A_0 \cdot L_{eff}}{(L_{eff} + T1) \cdot \sqrt{\phi_s} \cdot 2} \right) / (1 + KETA \cdot V_{bs})$$

$$T1 = 2 \cdot \sqrt{X_j \cdot X_{dep}}$$

For $V_{bs} \leq 0$:

$$T1s = \sqrt{\phi_s - V_{bs}}$$

For $V_{bs} \geq 0$:

$$T1s = \frac{\phi_s \cdot \sqrt{\phi_s}}{V_{bs}}, E_{sat} = 2 \cdot \frac{v_{sat}}{\mu_{eff}}$$

$$\phi_s + \frac{2}{2}$$

In general, Vdsat solves $Tmpa * Vdsat * Vdsat - Tmpb * Vdsat + Tmpc = 0$:

$$V_{dsat} = (Tmpb - \sqrt{Tmpb^2 - 4 \cdot Tmpa \cdot Tmpc}) / (2 \cdot Tmpa)$$

$$Tmpa = A_{bulk} \cdot (A_{bulk} \cdot W_{eff} \cdot v_{sat} \cdot C_{ox} \cdot R_{ds} - 1 + 1 / Pfactor)$$

$$Tmpb = V_{gst} \cdot (2 / Pfactor - 1) + (A_{bulk} \cdot E_{sat} \cdot L_{eff})$$

$$+ (3 \cdot A_{bulk} \cdot V_{gst} \cdot W_{eff} \cdot v_{sat} \cdot C_{ox} \cdot R_{ds})$$

$$Tmpc = (V_{gst} \cdot E_{sat} \cdot L_{eff}) + (V_{gst}^2 \cdot 2 \cdot W_{eff} \cdot v_{sat} \cdot C_{ox} \cdot R_{ds})$$

BSIM3 Version 2 Model — Linear Region

$$I_{dslin0} = \mu_{eff} \cdot C_{ox} \cdot \frac{W_{eff}}{L_{eff}} \cdot \frac{1}{1 + V_{ds} / (E_{sat} \cdot L)} \cdot \left(V_{gs} - V_{th} - A_{bulk} \cdot \frac{V_{ds}}{2} \right) \cdot V_{ds}$$

$$I_{ds} = \frac{I_{dslin0}}{1 + \frac{R_{ds} \cdot I_{dslin0}}{V_{ds}}}$$

BSIM3 Version 2 Model — Saturation Region Parameters

litl, eta, Ldd, Em, Drout, Pclm, Pdibl1, Pdibl2, Psobe1, Psobe2

V_{asat} and F_{vag}:

$$V_{asat} = \frac{E_{sat} \cdot L_{eff} + V_{dsat} + 2R_{ds} \cdot v_{sat} \cdot C_{ox} \cdot W_{eff} \cdot \left(V_{gst} - \frac{A_{bulk} \cdot V_{dsat}}{2} \right)}{2 / Pfactor - 1 + R_{ds} \cdot v_{sat} \cdot C_{ox} \cdot W_{eff} \cdot A_{bulk}}$$

$$F_{vag} = 1 + \frac{P_{vag} \cdot V_{gst}}{E_{sat} \cdot L_{eff}}$$

Early Voltage, satMod=1

Chapter 2: MOSFET Models

LEVEL 47: BSIM3 Version 2 MOSFET Model

$$V_A = V_{asat} + F_{vag} \cdot \left(\frac{1 + eta \cdot \frac{L_{dd}}{litl}}{P_{clm} \cdot A_{bulk}} \right) \cdot \left(\frac{(A_{bulk} \cdot E_{sat} \cdot L_{eff} + V_{gst} - \lambda \cdot (V_{ds} - V_{dsat})) \cdot (V_{ds} - V_{dsat})}{E_{sat} \cdot litl} \right)$$

$$\lambda = \frac{A_{bulk} \cdot E_{sat} \cdot L_{eff} + (V_{gst})}{2 \cdot litl \cdot E_m}$$

Early Voltage, satMod=2

$$V_A = V_{asat} + F_{vag} \cdot U_{vds} \cdot \left(\frac{1}{V_{aclm}} + \frac{1}{V_{adibl}} \right)^{-1}$$

$$U_{vds} = 1 + eta \cdot \frac{L_{dd}}{litl}$$

$$V_{aclm} = \frac{1}{P_{clm}} \cdot \frac{A_{bulk} \cdot E_{sat} \cdot L_{eff} + V_{gst}}{A_{bulk} \cdot E_{sat} \cdot litl} \cdot (V_{ds} - V_{dsat})$$

$$V_{adibl} = \frac{1}{\theta_{rout}} \cdot \left[(V_{gs} - V_{th}) - \left(\frac{1}{A_{bulk} \cdot V_{dsat}} + \frac{1}{V_{gst}} \right)^{-1} \right]$$

$$\theta_{rout} = P_{dibl1} \cdot \left[\exp\left(\frac{-D_{rout} \cdot L_{eff}}{2 \cdot l_t}\right) + 2 \exp\left(\frac{-D_{rout} \cdot L_{eff}}{l_t}\right) \right] + P_{dibl2}$$

$$V_{ahce} = \left[\frac{P_{scbe2}}{L_{eff}} \cdot \exp\left(\frac{-P_{scbe1} \cdot litl}{V_{ds} - V_{dsat}}\right) \right]^{-1}$$

BSIM3 Version 2 Model — Drain Current Parameters

$$I_{dsat} = W_{eff} \cdot v_{sat} \cdot C_{ox} \cdot (V_{gs} - V_{th} - A_{bulk} \cdot V_{dsat}) \cdot Pfactor$$

$$Pfactor = A_1 \cdot V_{gst} + A_2$$

$$I_{ds} = I_{dsat} \cdot \left(1 + \frac{V_{ds} - V_{dsat}}{V_A} \right) \cdot \left(1 + \frac{V_{ds} - V_{dsat}}{V_{ahce}} \right)$$

BSIM3 Version 2 Model — Subthreshold Region Parameters

$$Nfactor, C_{dsc}, C_{dscb}, V_{off}, C_{it}, D_{sub}, eta_0, eta_b$$

n and DIBL:

$$n = 1 + \frac{Nfactor \cdot 1.034e-10}{X_{dep} \cdot C_{ox}} + \frac{(C_{dsc} + C_{dscb} \cdot V_{bs}) \cdot \left[\exp\left(\frac{-L_{eff}}{2 \cdot l_t}\right) + 2 \exp\left(\frac{-L_{eff}}{l_t}\right) \right] + C_{it}}{C_{ox}}$$

$$DIBL = (eta_0 + eta_b \cdot V_{bs}) \cdot \left[\exp\left(\frac{-D_{sub} \cdot L_{eff}}{2 \cdot l_{t0}}\right) + 2 \exp\left(\frac{-D_{sub} \cdot L_{eff}}{l_{t0}}\right) \right]$$

$$l_{t0} = \sqrt{3 \cdot T_{ox} \cdot X_{dep0}}, X_{dep0} = \sqrt{\frac{2 \cdot \epsilon_{si} \cdot \phi_s}{q \cdot N_{peak}}}$$

subthMod=0

$$I_{ds} = g_m = g_{ds} = g_{mb} = 0$$

subthMod=1

$$I_{ds} = \frac{I_{limit} \cdot I_{exp}}{I_{limit} + I_{exp}} \cdot \left[1 - \exp\left(\frac{-V_{ds}}{V_{tm}}\right) \right],$$

$$I_{limit} = \frac{9}{2} \cdot u0 \cdot \sqrt{\frac{q \epsilon_{si} \cdot N_{peak}}{2 \cdot \phi_s}} \cdot \frac{W_{eff}}{L_{eff}} \cdot V_{tm}^2$$

$$I_{exp} = u0 \cdot \sqrt{\frac{q \epsilon_{si} \cdot N_{peak}}{2 \cdot \phi_s}} \cdot \frac{W_{eff}}{L_{eff}} \cdot V_{tm}^2 \cdot \exp\left(\frac{V_{gs} - V_{th} - V_{off} + DIBL \cdot V_{ds}}{n \cdot V_{tm}}\right)$$

subthMod=2

$$I_{ds} = u0 \cdot \sqrt{\frac{q \epsilon_{si} \cdot N_{peak}}{2 \cdot \phi_s}} \cdot \frac{W_{eff}}{L_{eff}} \cdot V_{tm}^2 \cdot \left[1 - \exp\left(\frac{-V_{ds}}{V_{tm}}\right) \right]$$

$$\cdot \exp\left(\frac{V_{gs} - V_{th} - V_{off} + DIBL \cdot V_{ds}}{n \cdot V_{tm}}\right)$$

Chapter 2: MOSFET Models

LEVEL 47: BSIM3 Version 2 MOSFET Model

BSIM3 Version 2 Model — Transition Region Parameters (subthMod=2)

$$V_{gshigh}, V_{gslow}$$

$$I_{ds} = (1-t)^2 \cdot I_{dslow} + 2 \cdot (1-t) \cdot t \cdot I_p + t^2 \cdot I_{dshigh}$$

$$t = \left(\frac{V_p - V_{gslow}}{V_{gslow} - 2 \cdot V_p + V_{gshigh}} \right) \\ \cdot \left(\sqrt{1 + \frac{(V_{gslow} - 2 \cdot V_p + V_{gshigh})(V_{gs} - V_{th} - V_{gslow})}{(V_p - V_{gslow})^2}} - 1 \right)$$

$$V_p = \frac{(g_{mhigh} \cdot V_{gshigh} - g_{mlow} \cdot V_{gslow}) - (I_{dshigh} - I_{dslow})}{g_{mhigh} - g_{mlow}}$$

$$I_p = I_{dslow} + g_{mlow} \cdot (V_p - V_{gslow})$$

BSIM3 Version 2 Model — Temperature Compensation Parameters

$$A_t, U_{a1}, U_{b1}, U_{c1}, KT1, KT2, UTE$$

$$V_{th}(temp) = V_{th}(tref) + (KT1 + KT2 \cdot V_{bs}) \cdot (T_{ratio} - 1)$$

$$u0(temp) = u0(tref) \cdot (T_{ratio})^{UTE}$$

$$V_{sat}(temp) = V_{sat}(tref) - A_t \cdot (T_{ratio} - 1)$$

$$U_a(temp) = U_a(tref) + U_{a1} \cdot (T_{ratio} - 1)$$

$$U_b(temp) = U_b(tref) + U_{b1} \cdot (T_{ratio} - 1)$$

$$U_c(temp) = U_c(tref) + U_{c1} \cdot (T_{ratio} - 1)$$

BSIM3 Version 2 MOSFET Model — Usage Notes

The following are usage notes regarding Level 47 MOSFETs:

1. Set LEVEL=47 to identify the model as a BSIM3 model.
2. This model is based on BSIM3 version 2.0 from UC Berkeley. Code was received from UC Berkeley in July 1994 in the form of SPICE3e2. Changes announced in a letter from UCB September 13, 1994, have been included. DC sweeps have been checked against SPICE3e2.

3. The default setting for CAPOP is CAPOP=13, which is the BSIM1 charge-conserving capacitance model. This model does not use the BSIM3 capacitance model.
4. The Level 47 model supports the TNOM model parameter name as an alias for TREF. The conventional terminology is TREF, which is supported as a model parameter in all Synopsys MOS levels. Level 47 supports the TNOM alternative name for compatibility with SPICE3.
5. The default room temperature is 25°C in Synopsys simulators, but is 27°C in SPICE3. If you specify the BSIM3 model parameters at 27°C, add TREF=27 to the model so that simulation correctly interprets the model parameters. To set the nominal simulation temperature to 27, add .OPTION TNOM=27 to the netlist when you test the Synopsys model versus SPICE3.
6. The default of DERIV is zero, the analytical method. You can set DERIV to 1 for the finite difference method. Analytic derivatives in the SPICE3e2 code are not exact in some regions. Setting DERIV=1 returns more accurate derivatives (GM, GDS, and GMBS), but consumes more CPU time.
7. You can select one of three ways to calculate V_{th} .
 - Using K1 and K2 values that you specify.
 - Using GAMMA1, GAMMA2, VBM, and VBX values that you enter in the .MODEL statement.
 - Using NPEAK, NSUB, XT, and VBM values that you specify.
8. You can enter the NPEAK and U0 model parameters in meters or centimeters. Simulation converts NPEAK to cm^{-3} as follows: if NPEAK is greater than 1e20, simulation multiplies it by 1e-6, and converts U0 to m^2/Vsec as follows: if U0 is greater than 1, simulation multiplies it by 1e-4. You must enter the NSUB parameter in cm^{-3} units.
9. The specified value of the threshold decreases with increasing temperature for NMOS and PMOS.
10. The default value of KT1 is -0.11. The negative sign ensures that the absolute value of the threshold decreases with increasing temperature for NMOS and PMOS.
11. You cannot set the LITL model parameter below a minimum value of 1.0e-9 m to avoid a possible divide by zero error.
12. After you adjust the temperature, VSAT cannot go below a minimum value of 1.0e4 m/sec to assure that it is positive after temperature compensation.

Chapter 2: MOSFET Models

LEVEL 47: BSIM3 Version 2 MOSFET Model

13. Seven model parameters accommodate the temperature dependencies of six temperature-dependent model variables. These parameters are `KT1` and `KT2` for `VTH`, `UTE` for `U0`, `AT` for `VSAT`, `UA1` for `UA`, `UB1` for `UB`, and `UC1` for `UC`.
14. Set up the temperature conversion between this model and SPICE3 as follows:

```
SPICE3 :    .OPTION TEMP=125
            .MODEL NCH NMOS Level=8
            + TNOM=27 ...
HSPICE :    .TEMP 125
            .MODEL NCH NMOS Level=47
            + TREF=27 ...
```

15. The `SCALM` option does not affect parameters that are unique to this model, but it does affect the common MOS parameters, such as `XL`, `LD`, `XW`, `WD`, `CJ`, `CJSW`, `JS`, and `JSW`.
16. Level 47 uses the common Synopsys MOS parasitic models, which `ACM` specifies.
17. Level 47 uses the common Synopsys MOS noise models, which `NLEV` specifies.
18. You can use `DELVTO` and `DTEMP` on the element line with MOSFET Level 47.
19. The `PSCBE1` and `PSCBE2` model parameters determine the impact ionization current, which contributes to the drain-source current. Impact ionization does not contribute to the bulk current.

BSIM3 Version 2 MOSFET Model — PMOS Model Example

In the following example of a PMOS model for the Level 47 MOSFET, `VTH0` is negative.

```
.model pch PMOS Level=47
+ Tnom=27.0
+ Npeak=1.5E+23 Tox=7.0E-09 Xj=1.0E-07
+ dl=0.2E-06 dw=-0.1E-06
+ SatMod=2 SubthMod=2 BulkMod=1
+ Vth0=-.8 Phi=.7 K1=.5 K2=0.03 K3=0
+ Dvt0=48 Dvt1=.6 Dvt2=-5e-4
+ Nlx=0 W0=0
+ Vsat=9E6 Ua=1E-09 Ub=0 Uc=-3E-02
+ Rds0=180 RdsW=0 U0=7E-03
+ A0=.87
+ Voff=-.07 NFactor=1.5 Cit=-3E-05
+ Cdsc=6E-02 Vglow=-.12 Vghigh=.12
+ Pclm=77 Pdibl1=0 Pdibl2=2E-011
+ Drout=0 Pscbel=0 Pscbe2=1E-28
+ Eta=0 Litl=4.5E-08
+ Em=0 Ldd=0
+ kt1=-.3 kt2=-.03
+ At=33000
+ Ua1=4E-09 Ub1=7E-18 Uc1=0
```

LEVEL 49 and 53: BSIM3 Version 3 MOSFET Model

The Synopsys Level 49 and Level 53 models are based on the BSIM3 version 3 MOSFET model from UC Berkeley.

- Level 49 is an HSPICE-enhanced version of BSIM3 version 3. Level 49 maintains compliance with the UC Berkeley release of BSIM3 version 3 with the following three exceptions:
 - Default parameter values — To eliminate differences in default parameter values, Level 49 explicitly assigns the CAPMOD and XPART parameters, and sets ACM=10. In addition, the default in Level=53 for XPART is “0” whereas in Level=49 it is “1”.
 - Parameter range limits — Provides parameter range limits that are identical to that of the Berkeley release. Differences occur only in the severity of the warning for five parameters. Level 49 issues a warning that the model exceeded the parameter range, but continues with the simulation.
 - However, the Berkeley release issues a fatal error, and aborts the simulation. These five parameters are NGATE, DVT1W, DVT1, DSUB, and DROUT. (See [BSIM3 Version 3 MOSFET Model — Parameter Range Limits](#) for more details.)
 - Improvements in numerical stability—Provides improvements in numerical stability. In most practical situations, these improvements do not affect compliance with the Berkeley release, but improve the convergence and the simulation time.
- Level 53 maintains full compliance with the Berkeley release, including numerically-identical model equations, identical parameter default values, and identical parameter range limits.
- Level 49 and 53 both support the following instance parameters, along with the DELVTO instance parameter for local mismatch and NBTI (negative bias temperature instability) modeling:
 - MULU0, low-field mobility (U_0) multiplier. Default=1.0.
 - MULUA, first-order mobility degradation coefficient (U_A) multiplier.
 - MULUB, second-order mobility degradation coefficient (U_B) multiplier.

Both Levels 49 and 53 support a superset of model parameters that include HSPICE-specific parameters. For Level 53, in all cases, HSPICE-specific parameters default to OFF. The single exception in Level 49 is that ACM defaults

to 0. To achieve Level 49 compliance with Berkeley BSIM3 version 3, set $\text{ACM}=10$.

If you set any of the following parameter values for MOSFET Level 49 and 53, simulation reports a warning:

- $L_{\text{eff}} \leq 5e-8$
- $W_{\text{eff}} \leq 1e-7$
- $L_{\text{eff}}CV \leq 5e-8$
- $W_{\text{eff}}CV \leq 1e-7$

Simulation aborts if you set L_{eff} or $W_{\text{eff}} \leq 0.0$.

For Level=49 and 53, LINT is used in the ACM model to calculate RD_{eff} and RS_{eff} for BSIM3 version 3 (LD gets the LINT value).

The following sections discuss these topics:

- [BSIM3 Version 3 MOSFET Model — Selecting Model Versions](#)
- [BSIM3 Version 3.x MOSFET Model Features](#)
- [Using BSIM3 Version 3 MOSFET Model](#)
- [BSIM3 Version 3 MOSFET Model — Usage Notes](#)
- [BSIM3 Version 3 MOSFET Model Parameters](#)
- [BSIM3 Version 3 MOSFET Model — Parameter Range Limits](#)
- [BSIM3 Version 3 MOSFET Model Equations](#)
- [BSIM3 Version 3 MOSFET Model — Additional Information](#)
- [BSIM3 Version 3 MOSFET Model Examples](#)

BSIM3 Version 3 MOSFET Model — Selecting Model Versions

The recommended BSIM3 version 3 model specification is `LEVEL=49`, `VERSION=3.3.0`. This version provides the most stable and up-to-date representation of the BSIM3 version 3 model.

However, do not change the `VERSION` specification in existing model cards without consulting the foundry or model extraction group that created the model cards.

Chapter 2: MOSFET Models

LEVEL 49 and 53: BSIM3 Version 3 MOSFET Model

The following table lists the available BSIM3 version 3 models and their release dates from UC Berkeley and the equivalent HSPICE versions.

| Berkeley Release | Model Version | HSPICE Version |
|--------------------------------------|-----------------------|----------------------|
| Version 3.3.0 (July, 2005) | 3.3.0 | 06.03 |
| Version 3.2.2 (April 20, 1999) | 3.22 3.23 3.2.4 | 99.2 01.4 02.2 |
| Version 3.2.1 (April 20, 1999) | 3.21 | 99.2 |
| Version 3.2 (June 16, 1998) | 3.2 | 98.2 |
| Version 3.1 with June 1998 bug fixes | 3.1 | 98.2 |
| Version 3.1 (December 1996) | 3.1 | 98.0 |
| Version 3.0 with June 1998 bug fixes | 3.0 | 98.2 |
| Version 3.0 (October 1995) | 3.0 | 98.0 |

As of the 99.2 release, there are multiple BSIM3 version 3 releases from Berkeley and several Level 49 releases. For additional release information from the UCB group, see the BSIM3 home page:

<http://www-device.EECS.Berkeley.EDU/~bsim3/>

To minimize confusion and maintain backward compatibility, you can select the VERSION and HSPVER model parameters. VERSION selects the Berkeley release version; HSPVER selects the Synopsys release version. For example, HSPVER=97.2 and VERSION=3.1 reproduce results from HSPICE 97.2 using the BSIM3 Version 3.1 model. For detailed discussion of how HSPVER relates to the UCB VERSION, see [Using BSIM3 Version 3 MOSFET Model](#).

HSPVER defaults to the current release that you are using. The VERSION model parameter selects among the various Berkeley releases of BSIM3 version 3 as follows:

- Version 3.0 Berkeley release (October 30, 1995) default for HSPICE96.1,96.2,96.3.

Simulation invokes this version if you specify VERSION=3.0 and HSPVER=98.0. To invoke the Synopsys model version that most accurately represents the Berkeley release of October 1995, specify the VERSION=3.0 and HSPVER=98.0 parameters.

- Version 3.1 Berkeley (December 9, 1997) default for HSPICE97.1,97.2. 97.4.

Simulation invokes this version if you specify VERSION=3.1 or 3.11 and HSPVER=98.0. To invoke the Synopsys model version that most accurately represents the Berkeley release of December 1996, specify the VERSION=3.1 or 3.11 and HSPVER=98.0 parameters.
- Berkeley Version 3.0, 3.1 bug fixes. Berkeley corrected several Version 3.0 and 3.1 bugs in the June, 1998 release. These fixes are incorporated into HSPICE98.2, which simulation uses if you specify VERSION=3.0 or VERSION=3.1 and HSPVER=98.2. As a result of bug fixes, you might notice some differences between Version 3.0/3.1 in HSPICE98.2 and previous Version 3.0/3.1 releases. Notably, differences occur if you specify PD and PS perimeter factors that are less than W_{eff} ($PD, PS < W_{eff}$ no longer clamp to W_{eff} in Version 3.1) and if DLC and LINT are not identical ($L_{eff}CV$ calculation bug in Versions 3.0 and 3.1).

For a complete list of bug fixes, see the BSIM3 web site:
<http://www-device.eecs.berkeley.edu/~bsim3>

Note: Version 3.11 was introduced in HSPICE97.4. This version represents Berkeley Version 3.1 (Dec., 1996) with HSPICE bug fixes. This model maintains backward compatibility. Starting with HSPICE98.2, Version 3.1 and 3.11 are identical, and represent Version 3.1 with Berkeley June, 1998 bug fixes.

- Version 3.2 Berkeley release (June 16, 1998). Simulation invokes this version if you specify VERSION=3.2 and HSPVER=98.2.
- Version 3.2.1 Berkeley release (April 20, 1999). Simulation invokes this version if you specify VERSION=3.21 and HSPVER=99.2.
- Version 3.2.2 Berkeley release (April 20, 1999). Simulation invokes this version if you specify VERSION=3.22 and HSPVER=99.2.
- For the latest HSPICE improvements, use VERSION=3.3.0 and HSPVER=06.03.

Note: Versions 3.2.1 and 3.2.2 are identical, except BSIM3 version 3.2.1 uses a bias-dependent Vfb and BSIM3 version 3.2.2 uses a bias-independent Vfb for the CAPMOD=1 and 2 capacitance models.

BSIM3 Version 3.x MOSFET Model Features

This section covers the following topics:

- [BSIM3 Version 3.3 Model Features](#)
- [BSIM3 Version 3.2 Model Features](#)

BSIM3 Version 3.3 Model Features

In July 2005, Berkeley released BSIM3 Version 3.3, which includes the following new features:

- A new small-signal AC charge-deficit ACNQS model that enables the NQS effect in AC simulation. This can be turned on by setting `acnqsMod=1` and off by setting `acnqsMod=0`.
- A new channel thermal noise model “SPICE2new” that the thermal noise coefficient varies smoothly between 4 to 8/3 as the device moves from a linear to a saturation region. The new `noiMod` model flags are:
 - `noiMod=5`: Flicker noise model — SPICE2; Thermal noise model — SPICE2new
 - `noiMod=6`: Flicker noise model — BSIM3 version 3; Thermal noise model —SPICE2new
- Addition of a `LINTNOI` parameter that introduces an offset to the length reduction parameter (`Lint`) to improve the accuracy of the flicker noise model.
- Changed the `Rds0` source drain current contact resistance check model.
- Fixed bugs in BSIM3 version 3.2.4.

For more information about the Berkeley releases, see the BSIM3 web site:
<http://www-device.eecs.berkeley.edu/~bsim3>

BSIM3 Version 3.2 Model Features

In June 1998, Berkeley released BSIM3 Version 3.2, which includes the following new features:

- A new intrinsic capacitance model, `CAPMOD=3`, includes finite charge layer thickness effects; `CAPMOD` now defaults to 3 (new parameters: `CAPMOD=3`, `ACDE`, and `MOIN`).
- Improved modeling of C-V characteristics at the weak-to-strong inversion transition (new parameters: `NOFF` and `VOFFCV`).
- V_{th} dependence on Tox (new parameter: `TOXM`).

- Flatband voltage parameter more accurately models different gate materials (new parameter: VFB).
- Improved substrate current scalability with channel length (new parameter: APLHA1).
- Restructured nonquasi-static (NQS) model includes pole-zero analysis and bug fixes. NQSMOD is a BSIM3 element parameter. Starting from HSPICE H-2013.03 release, this is supported as an element parameter too.
- Junction diode model temperature dependence (new parameters: TCJ, TCJSW, TCJSWG, TPB, TPBSW, and TPBSWG).
- Adjustable current limiting in the junction diode current model (new parameter: IJTH).
- Use C-V inversion charge equations (CAPMOD=0,1,2,3) to calculate the thermal noise if NOIMOD=2 or 4.
- Eliminated the small negative capacitance values (Cgs and Cgd) in the accumulation-depletion regions.
- Separate set of length/width dependence parameters for the CV model (LLC, LWC, LWLC, WLC, WWC, and WWLc parameters).
- Additional parameter checking.
- Bug fixes.

Note: If you use the defaults for all new Version 3.2 parameters, Version 3.2 and Version 3.1 (with June, 1998 bug fixes) return identical DC results. However, transient and AC results generally differ. This discrepancy arises only from differences in the flatband voltage calculations used in the intrinsic charge/capacitance models. These differences occur in all CAPMOD models 1-3.

- Level 53 resets HSPVER < 98.0 to 98.0.
- HSPVER<98.2 resets to 98.2 if VERSION>=3 . 2 for Levels 49/53.
- Version 3.0, 3.1, and 3.1.1 in HSPICE do not support NQSMOD and CAPMOD=3. Only Version 3.2 supports them.
- Version 3.24 added R_{ds} noise to the thermal noise model. Simulation smooths out the unified flicker noise, from the linear region to the saturation region. You might need to re-extract the parameters for the unified flicker noise model.

Chapter 2: MOSFET Models

LEVEL 49 and 53: BSIM3 Version 3 MOSFET Model

For more information about the Berkeley releases, see the BSIM3 website:
<http://www-device.eecs.berkeley.edu/~bsim3>

Using BSIM3 Version 3 MOSFET Model

Note the following points when you use BSIM3 version 3 with a Synopsys circuit simulator:

- Use either the Level 49 or Level 53 model. Level 53 fully complies with the Berkeley BSIM3 version 3 release. In most cases Level 49 returns the same results as Level 53, runs as fast or faster, shows better convergence, and allows a wider range of parameter specifications.
- Explicitly set all Berkeley-specific BSIM3 model parameters in the model card. This minimizes problems resulting from version changes and compatibility with other simulators. You do not explicitly set all lwp binning parameters.
- To match results with simulations from previous HSPICE versions, use the HSPVER=YY.N model parameter, such as HSPVER=97.4. Do not use the full year specification (such as 1997.4). The patch version number format is HSPVER=YY.NN (for example, HSPVER=98.21 is release 98.2.1).
- Levels 49 and 53 support the TNOM model parameter name as an alias for TREF. The conventional terminology in HSPICE is TREF, which all Synopsys model MOS levels support as a model parameter. Both Levels 49 and 53 support the TNOM alternative name for compatibility with SPICE3.

The default room temperature is 25°C in Synopsys circuit simulators, but is 27°C in SPICE3. If you specify the BSIM3 model parameters at 27°C, add TNOM=27 to the model so that simulation correctly interprets the model parameters. To set the nominal simulation temperature to 27, add .OPTION TNOM=27 to the netlist when you test the Synopsys model versus SPICE3.

You can use DELVTO and DTEMP on the element line with Levels 49 and 53. The following equation converts the temperature setup between the Synopsys model and SPICE3:

```
SPICE3 :      .OPTION TEMP=125
          .MODEL NCH NMOS Level=8
          + TNOM=27 ...
Synopsys Model:      .TEMP 125
          .MODEL NCH NMOS Level=49
          + TNOM=27 ...
```

- To automatically calculate the drain, source area, and perimeter factors for Berkeley junction diode models, use `ACM=12` with `CALCACM=1`. Normally, `ACM=10-13` defaults the area and perimeter factors to 0. To override this value for `ACM=12`, specify `CALCACM=1`. Define the HSPICE-specific parameter (`HDIF`) in the model card. If you do not want parasitic `Rs` and `Rd` with the BSIM3 version 3 internal `Rsd`, either do not specify the `RSH`, `RSC`, `RDC`, `RS`, and `RD` HSPICE parameters (default is 0) or set them to 0.
- Simulation and analysis either warns or aborts with a fatal error if certain model parameter values are out of a normal range. To view all warnings, you might need to increase the `.OPTION WARNLIMIT` value (default=1). To turn on full parameter range checking, set the `PARAMCHK=1` model parameter (default is 0). If you use `PARAMCHK=0`, simulation checks a smaller set of parameters. (See Note below; also see [BSIM3 Version 3 MOSFET Model — Parameter Range Limits](#) for more details about parameter limits.) Use the `APWARN=1` model parameter (default=0) to turn off $PS,PD < W_{eff}$ warnings.
- Use `NQSMOD` only with Version 3.2. Starting from HSPICE H-2013.03 release, this is supported as an element parameter too.

Note: The default setting of `PARAMCHK` can influence MOSFET behavior in HSPICE in not checking and/or enforcing the range limits for some MOSFET model parameters. `PARAMCHK` selects between a default and enhanced level of MOSFET parameter checks. If set to 0, only default checks are performed.

If set to 1, an enhanced set of parameter checks are performed and certain parameters will be reset to nominal values if they are found to be out of range.

Because the default setting of `PARAMCHK` can vary between model levels (e.g., 49/53=0 and 54=1), it is important to implicitly set `PARAMCHK` in your model file or insure it has been set by the model vendor. A failure to do so can cause unexpected variations in simulation results and a failure to correlate with other simulators that may have different default settings.

BSIM3 Version 3 MOSFET Model — Usage Notes

This section covers the following topics:

- [BSIM3 Version 3 Model — Usage Notes: Enhanced Diode Model DC Equations](#)
- [BSIM3 Version 3 Model — Usage Notes: Nonquasi-Static \(NQS\) Model](#)
- [BSIM3 Version 3 Model — Usage Notes: HSPICE Junction Diode Model and Area Calculation Method](#)
- [BSIM3 Version 3 Model — Usage Notes: Reverse Junction Breakdown Model](#)
- [BSIM3 Version 3 Model — Usage Notes: TSMC Diode Model](#)
- [BSIM3 Version 3 Model — Usage Notes: STI / LOD Parameters](#)
- [BSIM3 Version 3 Model — Usage Notes: Parameter Differences](#)
- [BSIM3 Version 3 Model — Usage Notes: Noise Model](#)
- [BSIM3 Version 3 Model — Usage Notes: Performance Improvements](#)
- [BSIM3 Version 3 Model — Usage Notes: Reduced Parameter Set \(BSIM3-lite\)](#)
- [BSIM3 Version 3 Model — Usage Notes: Parameter Binning](#)
- [BSIM3 Version 3 Model — Usage Notes: WPE Model](#)
- [BSIM3 Version 3 Model — Usage Notes: Ig Model](#)
- [BSIM3 Version 3 Model — Usage Notes: Charge Models](#)
- [BSIM3 Version 3 Model — Usage Notes: Printback Options](#)
- [BSIM3 Version 3 Model — Usage Notes: Mobility Multiplier](#)

BSIM3 Version 3 Model — Usage Notes: Enhanced Diode Model DC Equations

BSIM3 diode IV equations, considering carrier recombination and trap-assisted tunneling current to improve the I_{off} -related value. This section describes the use model for this enhancement.

The model parameter `bsim4diode` invokes the feature. In addition, 30 related model parameters are also added for this enhancement: `jtss`, `jtsd`, `jtssws`, `jtsswd`, `jtsswgs`, `jtsswgd`, `njts`, `njtssw`, `njtsswg`, `xtss`, `xtsd`, `xtssws`, `xtsswd`, `xtsswgs`, `xtsswgd`, `tnjts`, `tnjtssw`, `tnjtsswg`, `vtss`, `vtsd`, `vtssws`, `vtsswd`,

vtsswgs, vtsswd, njtsd, njtswd, njtsswd, tnjtsd, tnjtswd, and tnjtsswd. This diode model is only available under AMC=12 for version >=3.2.

Syntax:

```
.model nch nmos level=49...
+ bsim4diode=1 acm=12 version=3.2....
```

These equations come from BSIM4.

$$I_{bs_total} = I_{bs} - W_{effc_j} \cdot JTSSWGS(T) \cdot \left(e^{\frac{-V_{bs}}{NJTSSWG(T) \cdot Vtm0}} \cdot \frac{VTSSWGS}{VTSSWGS - V_{bs}} - 1 \right)$$

$$- P_{s_eff} \cdot JTSSWS(T) \cdot \left(e^{\frac{-V_{bs}}{NJTSSW(T) \cdot Vtm0}} \cdot \frac{VTSSWS}{VTSSWGS - V_{bs}} - 1 \right)$$

$$- A_{s_eff} \cdot JTSS(T) \cdot \left(e^{\frac{-V_{bs}}{NJTS(T) \cdot Vtm0}} \cdot \frac{VTSS}{VTSS - V_{bs}} - 1 \right)$$

$$I_{bd_total} = I_{bd} - W_{effc_j} \cdot JTSSWGD(T) \cdot \left(e^{\frac{-V_{bd}}{NJTSSWG(T) \cdot Vtm0}} \cdot \frac{VTSSWGD}{VTSSWGS - V_{bd}} - 1 \right)$$

$$- P_{d_eff} \cdot JTSSWD(T) \cdot \left(e^{\frac{-V_{bd}}{NJTSSW(T) \cdot Vtm0}} \cdot \frac{VTSSWD}{VTSSWD - V_{bd}} - 1 \right)$$

$$- A_{s_eff} \cdot JTSD(T) \cdot \left(e^{\frac{-V_{bd}}{NJTS(T) \cdot Vtm0}} \cdot \frac{VTSS}{VTSD - V_{bd}} - 1 \right)$$

where

Chapter 2: MOSFET Models

LEVEL 49 and 53: BSIM3 Version 3 MOSFET Model

$$JTSSWGS(T) = JTSSWGS \cdot e^{XTSSWGS \cdot \frac{Eg0}{Vtm \cdot \frac{Temp}{Tnom} - 1}}$$

$$JTSSWS(T) = JTSSWS \cdot e^{XTSS \cdot \frac{Eg0}{Vtm \cdot \frac{Temp}{Tnom} - 1}}$$

$$JTSS(T) = JTSS \cdot e^{XTSSWGS \cdot \frac{Eg0}{Vtm \cdot \frac{Temp}{Tnom} - 1}}$$

$$JTSSWGD(T) = JTSSWGD \cdot e^{XTSSWGD \cdot \frac{Eg0}{Vtm \cdot \frac{Temp}{Tnom} - 1}}$$

$$JTSSWD(T) = JTSSWD \cdot e^{XTSSWD \cdot \frac{Eg0}{Vtm \cdot \frac{Temp}{Tnom} - 1}}$$

$$JTSSTD = JTS \cdot e^{XTSD \cdot \frac{Eg0}{Vtm \cdot \frac{Temp}{Tnom} - 1}}$$

$$NJTSSWG(T) = NJTSSWG \cdot \left[1 + TNJTSSWG \cdot \left(\frac{Temp}{Tnom} - 1 \right) \right]$$

$$NJTSSW(T) = NJTSSW \cdot \left[1 + TNJTSSW \cdot \left(\frac{Temp}{Tnom} - 1 \right) \right]$$

$$NJTS(T) = NJTS \cdot \left[1 + TNJTS \cdot \left(\frac{Temp}{Tnom} - 1 \right) \right]$$

Note: These notes apply for this upgrade:

- The BSIM3 model does not have BSIM4-like equations for Aseff/ADeff/Pseff/Pdeff equations. In the above equations, they are replaced by
->BSIM3sourceArea, ->BSIM3drainArea,
->BSIM3sourcePerimeter, and ->BSIM3drainPerimeter.
- Model parameter JTWEFF and related equations are not implemented for BSIM3.
- Eg0-related model parameters including MTRLMOD and BG0SUB / BGASUB / BGBSUB are not implemented for BSIM3.

BSIM3 Version 3 Model — Usage Notes: Nonquasi-Static (NQS) Model

You can also select the Berkeley NonQuasi-Static (NQS) model for Levels 49 and 53. This model provides a first-order correction to the quasi-static charge models. See M.Chan, K.- Y. Hui, C. Hu, and P.-K. Ko, IEEE Trans. Electron Devices, vol. ED-45, pp.834-841, 1998.

The Level 49/53 MOSFET model supports only the model parameter implementation.

To invoke the NQS model, specify the `NQSMOD=1` parameter in the model card. You can use `NQSMOD` with any of the `CAPMOD` Levels (0-3) but only with Version 3.2. Version 3.0 and 3.1 do not support NQS.

Note: Starting from HSPICE H-2013.03 release, both `NDQSMOD` model and element parameters are supported.

BSIM3 Version 3 Model — Usage Notes: HSPICE Junction Diode Model and Area Calculation Method

You can use two junction diode models with both Levels 49 and 53: the HSPICE junction model and the Berkeley junction model.

- For the HSPICE junction model, specify the `ACM=0,1,2, or 3` model parameter value.
- For the Berkeley junction model, specify `ACM=10,11,12, or 13`.

The default `ACM` value is 0 for Levels 49 or 10 for Level 53. For the junction current, junction capacitance, and parasitic resistance equations corresponding to `ACM=0,1,2,3` see [MOS Diode Equations](#).

Set `ACM=10,11,12, or 13` to enable the Berkeley junction diodes and to add parasitic resistors to the MOSFET. The parasitic resistor equations for `ACM=10-13` correspond to the `ACM=0-3` parasitic resistor equations. `ACM=10-13` all use the Berkeley junction capacitance model equations:

```
(Bulk-source capacitance)
if (Ps >Weff)
  Cbs=AS * Cjbs + (PS - Weff) * Cjbssw + Weff *
  Cjbsswg
else
  Cbs=AS * Cjbs + PS * Cjbsswg
```

The `AS` and `PS` area and perimeter factors default to 0, if you do not specify them on the element line.

Chapter 2: MOSFET Models

LEVEL 49 and 53: BSIM3 Version 3 MOSFET Model

```
if (Vbs < 0)
    Cjbs=Cj * (1 - (Vbs/Pb)) - Mj
    Cjbssw=Cjsw * (1 - (Vbs/Pbsw))
    -Mjsw

    Cjbsswg=Cjswg * (1 - (Vbs/Pbswg)) - Mjswg
else
    Cjbs=Cj * (1 + Mj * (Vbs/Pb))
    Cjbssw=Cjsw * (1 + Mjsw * (Vbs/Pbsw))
    Cjbsswg=Cjswg * (1 + Mjswg * (Vbs/Pbswg))
```

Bulk-drain equations are analogous. ACM=10,11,12,13 do not use the HSPICE equations for AS, PS, AD, and PD. In accordance with the BSIM3 version 3 model, the default values for these area and perimeter factors are zero. To invoke the HSPICE calculations for AS, PS, AD, and PD, specify the CALCACM=1 model parameter.

Note: Simulation invokes CALCACM only if ACM=12. The calculations used in ACM=10, 11, and 13 are not consistent with the Berkeley diode calculations.

CALCACM=1 and ACM=12 invoke the following area and perimeter calculations:

If you do not specify AD on the element line:

```
AD=2 * HDIEff * Weff
else:
    AD=AD * WMLT^2
```

If you do not specify AS on the element line:

```
AS=2 * HDIEff * Weff
else:
    AS=AS * WMLT^2
```

If you do not specify PS on the element line:

```
PS=4 * HDIEff + 2 * Weff
else:
    PS=PS * WMLT
```

If you do not specify PD on the element line:

```
PD=4 * HDIEff + 2 * Weff
else:
    PD=PD * WMLT
```

Note: W_{eff} is not the same W_{eff} used in the BSIM3 version 3, and Levels 49 and 53 I-V, C-V model equations.

The preceding equations use the following simple forms:

$$W_{eff} = W * WMLT + XW$$

$$HDIF_{eff} = HDIF * WMLT$$

| Parameter | Description |
|-----------|---|
| HDIF | Heavy diffusion length specified in the model card |
| W | Width specified on the element line |
| WMLT | Shrink factor specified in the model card |
| XW | Etch/mask effect factor specified in the model card |

Note: These equations ignore the SCALM, SCALE, and M factor effects. See [Using an ACM=2 MOS Diode \(ACM=2\)](#) for further details.

BSIM3 Version 3 Model — Usage Notes: Reverse Junction Breakdown Model

Starting with HSPICE version 2009.09 HSPICE MOSFET Level 49-53 (BSIM Level 3.2 or later) supports the Reverse Junction Breakdown model (introduced with BSIM4.6.4). This functionality uses similar diode model equations as for BSIM4.6.4 DIOMOD=2. Refer to Equation (11.5) of the BSIM4.6.4 manual for details. Note that the equation for forward biased region is affected accordingly.

| Parameter | Default | Description |
|-----------|---------------|---|
| BREAKMOD | 0 (off) | Flag to turn on off reverse junction breakdown model, set to 1 to turn on |
| BVD | bvs | Drain diode breakdown voltage |
| BVS | 10 (V) | Source diode breakdown voltage |
| IJTHDREV | ijthsrev | Reverse drain diode forward limiting current |
| IJTHSREV | 0.1 (A) | Reverse source diode forward limiting current |
| XJBVD | xjbvs | Fitting parameter for drain diode breakdown current |
| XJBVS | 1.0 (no unit) | Fitting parameter for source diode breakdown current |

Chapter 2: MOSFET Models

LEVEL 49 and 53: BSIM3 Version 3 MOSFET Model

If the above parameters are less than or equal to zero, the parameters are reset to 0.0 and warnings are issued as follows:

- If ($bvs \leq 0.0$), “ bvs reset to 0.0”.
- If ($bvd \leq 0.0$), “ bvd reset to 0.0”.
- If ($ijthsrev \leq 0.0$), “ $ijthsrev$ reset to 0.0”.
- If ($ijthdrev \leq 0.0$), “ $ijthdrev$ reset to 0.0”.
- If ($xjbvs \leq 0.0$), “ $xjbvs$ reset to 0.0”.
- If ($xjbvd \leq 0.0$), “ $xjbvd$ reset to 0.0”.

BSIM3 Version 3 Model — Usage Notes: TSMC Diode Model

Starting in HSPICE version 2003.09, HSPICE MOSFET Level 49 (ACM=12, BSIM3 version 3.2 or later) supports a TSMC diode model. You can use this TSMC diode model to simulate the breakdown effect, the resistance-induced non-ideality factor, and geometry-dependent reverse current of a diode.

Order this model directly from Taiwan Semiconductor Manufacturing Company (TSMC), not from Synopsys. See the TSMC web site: <http://www.tsmc.com>

BSIM3 Version 3 Model — Usage Notes: STI / LOD Parameters

HSPICE BSIM3 version 3 (Level=49 and 53) supports UC Berkeley's STI/LOD stress effect model. To turn on this stress effect model in BSIM3 version 3, specify `STIMOD=1` in your model cards.

| Parameter | Unit | Default | Bin | Description |
|----------------------------------|------|---------|-----|--|
| STIMOD (Also instance parameter) | | 0.0 | | STI model selector, which gives priority to the instance parameter. <ul style="list-style-type: none">■ 0: No STI effect.■ 1: IDB's STI model■ 2: GSHUNT's STI model |
| KU0 | M | 0.0 | No | Mobility degradation/enhancement coefficient for stress effect |
| KVSAT | M | 0.0 | No | Saturation velocity degradation/enhancement parameter for stress effect. $1.0 \leq kvsat \leq 1.0$ |
| KVTH0 | V*m | 0.0 | No | Threshold shift parameter for stress effect |
| LKU0 | | 0.0 | No | Length dependence of KU0 |
| LLODKU0 | | 0.0 | No | Length parameter for U0 stress effect, >0 |

| Parameter | Unit | Default | Bin | Description |
|-------------------------|------|---------|-----|--|
| LLODVTH | | 0.0 | No | Length parameter for Vth stress effect, >0 |
| LODETA0 | M | 1.0 | No | ETA0 shift modification factor for stress effect, >0 |
| LODK2 | m | 1.0 | No | K2 shift modification factor for stress effect, >0 |
| PKVTH0 | | 0.0 | No | Cross-term dependence of KVTH0 |
| SA (instance parameter) | | 0.0 | | Distance between S/D diffusion edge to poly gate edge from one side. If not given, or, if (<=0), the stress effect is turned off. |
| SAREF | M | 1e-06 | No | Reference distance for SA, >0.0 |
| SB (instance parameter) | | 0.0 | | Distance between S/D diffusion edge to poly gate edge from the other side. If not given, or, if (<=0), the stress effect is turned off |
| SBREF | M | 1e-06 | No | Reference distance for SB, >0.0 |
| STETA0 | | 0.0 | No | ETA0 shift factor related to VTH0 change |
| STK2 | | 0.0 | No | K2 shift factor related to VTh0 change |
| TKU0 | | 0.0 | No | Temperature coefficient of KU0 |
| WKU0 | | 0.0 | No | Width dependence of KU0 |
| WKVTH0 | | 0.0 | No | Width dependence of KVTH0 |
| WLOD | M | 0.0 | No | Width parameter for stress effect |
| WLODKU0 | | 0.0 | No | Width parameter for U0 stress effect, >0 |
| WLODVTH | | 0.0 | No | Width parameter for Vth stress effect, >0 |

BSIM3 Version 3 Model — Usage Notes: Parameter Differences

Some parameter names differ between the Synopsys model and the Berkeley junction models. The Synopsys models (ACM=0-3) do not recognize the following BSIM3 version 3 parameters:

- NJ (ignored, use N instead)
- CJSWG (ignored, use CJGATE instead)
- MJSWG (ignored; HSPICE has no equivalent parameter, and simulation sets the gate sidewall grading coefficient=MJSW)

Chapter 2: MOSFET Models

LEVEL 49 and 53: BSIM3 Version 3 MOSFET Model

- PBSW (ignored, use PHP instead)
- PBSWG (ignored; HSPICE has no equivalent parameter, and simulation sets the gate sidewall contact potential=PHP)

The Berkeley model (ACM=10,11,12,13) does not recognize the following parameters:

- CJGATE (ignored, use CJSWG instead)
- PHP (ignored, use PBSW instead)

BSIM3 Version 3 Model — Usage Notes: Noise Model

The HSPICE NLEV parameter overrides the BSIM3 version 3 NOIMOD parameter. Specifying NLEV invokes the HSPICE noise model. See [MOSFET Noise Models](#) for more information. If you do not specify NLEV, simulation invokes the Berkeley noise equations.

BSIM3 Version 3 Model — Usage Notes: Performance Improvements

To improve the performance of Levels 49 and 53 reduce the complexity of model equations, replacing some calculations with spline functions and compiler optimization. For Level 49, the result is a reduction in simulation time of up to 40% compared to releases before 97.4 while maintaining accuracy to 5 digits or better. To use the spline functions, set the SFVTFLAG=1 model parameter in the model card. SFVTFLAG=0, the default value, disables the spline functions. For Level 53, all BSIM3 version 3 non-compliant features default to off.

BSIM3 Version 3 Model — Usage Notes: Reduced Parameter Set (BSIM3-lite)

Setting the LITE=1 model parameter in Level 49 to invoke the BSIM3 version 3-lite reduced parameter set model. Use it with model binning. Without binning to account for geometry effects, the full BSIM3 version 3 model specifies several model parameters. However, it is often difficult to extract a “global” BSIM3 version 3 model that is accurate over the entire geometry range.

To improve accuracy over a range of geometries, you can bin the model parameters. That is, this model divides the entire length-width geometry range into rectangular regions or bins. Simulation extracts a different set of parameters for each bin. The built-in bilinear parameter interpolation scheme maintains continuity (over length-width) at the boundaries between bins. Because many BSIM3 model parameters account for MOSFET geometry effects, these geometry-effect parameters are redundant. You can eliminate them when you use binning.

The BSIM3-lite model parameter set was created in response to the question: What BSIM3 parameters should be excluded when using a binned model? To invoke the BSIM3-lite model, specify the LITE=1 model parameter in the model card.

Simulation checks the model card to determine if it conforms to the BSIM3-lite parameter set. BSIM3-lite takes advantage of the smaller number of calculations, and reduces simulation times by up to 10% compared to the full parameter set BSIM3 model. Only Level 49 supports LITE=1.

The following table lists model parameters (total 49) that the BSIM3-lite model excludes. Either exclude all parameters in this list from the model card or explicitly set them to the default value specified in the list. In some cases, as noted, the BSIM3-lite default value differs from the standard BSIM3 version 3 default value. You should also exclude WR, ALPHA0, and CIT, but the BSIM3-lite model card does not require this exclusion.

| Parameter | Comments |
|-----------|--|
| MOBMOD | Recommended default or set=1 |
| NQSMOD | Recommended default or set=0 |
| ALPHA0 | Recommended default or set=0 for Version 3.2 |
| B0 | default=0 |
| B1 | default=0 |
| CIT | Recommended default or set=0 |
| DROUT | default=0, std default=0.56 |
| DSUB | default=0 |
| DVT0 | default=0, std default=2.2 |
| DVT0W | default=0 |
| DVT1 | default=0, std default=0.53 |
| DVT1W | default=0, std default=5.3e6 |
| DVT2 | default=0, std default=-0.032 |
| DVT2W | default=0, std default=-0.032 |

Chapter 2: MOSFET Models

LEVEL 49 and 53: BSIM3 Version 3 MOSFET Model

| Parameter | Comments |
|-----------|--------------------------------|
| DWB | default=0 |
| DWG | default=0 |
| GAMMA1 | do not define |
| GAMMA2 | do not define |
| K3 | default=0, std default=80 |
| K3B | default=0 |
| KT1L | default=0 |
| LL | default=0 |
| LLC | default=0 |
| LLN | default=1 |
| LW | default=0 |
| LWC | default=0 |
| LWL | default=0 |
| LWLC | default=0 |
| LWN | default=1 |
| NGATE | Recommended default or set=0 |
| NLX | default=0, std default=1.74e-7 |
| NSUB | do not define |
| PDIBLC1 | default=0, std default=0.39 |
| PRWB | default=0 |
| PRWG | default=0 |
| TOXM | default=tox |
| VBM | do not define |
| VBX | do not define |

| Parameter | Comments |
|-----------|------------------------------|
| W0 | no effect |
| WL | default=0 |
| WLC | default=0 |
| WLN | default=1 |
| WR | Recommended default or set=1 |
| WW | default=0 |
| WWC | default=0 |
| WWL | default=0 |
| WWLC | default=0 |
| WWN | default=1 |
| XT | do not define |

BSIM3 Version 3 Model — Usage Notes: Parameter Binning

To support parameter binning, Berkeley BSIM3 version 3 specifies L_{WP} parameters. To bilinearly interpolate a subset of model parameters over $1/L_{eff}$ and $1/W_{eff}$, you specify four terms:

- Xo parameter
- X length term
- Xw width term
- Xp product term

The simulation then interpolates the parameter value at specified L, W .

$$X = X_o + X_l/L_{eff} + X_w/W_{eff} + X_p/L_{eff}/W_{eff}$$

See [BSIM3 Version 3 MOSFET Model — Parameter Range Limits](#) to determine whether you can bin a parameter. Simulation adds the LMIN, LMAX, WMIN, WMAX, LREF, and WREF parameters to allow multiple cell binning. LMIN, LMAX, WMIN, WMAX define the cell boundary. LREF and WREF are offset values that provide a convenient interpolation scheme. The simulation uses the LREF and WREF offsets if you define both values and you specify the BINFLAG > 0.9 model parameter.

Chapter 2: MOSFET Models

LEVEL 49 and 53: BSIM3 Version 3 MOSFET Model

The simulation then interpolates the parameter value at a specified L, W :

$$X = X_0 + X_L * (1/L_{eff} - 1/L_{REF}) + X_w * (1/W_{eff} - 1/W_{REF}) \\ + X_p / (1/L_{eff} - 1/L_{REF}) / (1/W_{eff} - 1/W_{REF})$$

To select micron units for the L_{wp} geometry parameters, set the `BINUNIT=1` model parameter. For other choices of `BINUNIT`, the lengths are in units of meters. Simulation handles the `XL`, `XLREF`, `XW`, and `XWREF` parameters in a manner consistent with other Synopsys MOSFET models, and they produce shifts in parameter values without disrupting the continuity across the bin boundaries.

BSIM3 Version 3 Model — Usage Notes: WPE Model

HSPICE BSIM3 version 3 (Level=49, BSIM3 Version 3.2.2 or later) supports UC Berkeley's BSIM4.5 WPE (well-proximity effects) model. To turn on this WPE model in BSIM3 version 3, specify `WPEMOD=1` in your model cards.

WPE Model Parameters:

| Name | Default | Min | Max | Bin | Description |
|---------|---------|-----|-----|-----|---|
| WPEMOD | 0 | 0 | 1 | No | Flag for WPE model (WPEMOD=1 to activate this model) |
| K2WE | 0.0 | | | Yes | K2 shift factor for well-proximity effect |
| KU0WE | 0.0 | | | Yes | Mobility degradation factor for well-proximity effect |
| KVTH0WE | 0.0 | | | Yes | Threshold shift factor for well-proximity effect |
| SCREF | 1.0e-6 | 0.0 | | No | Reference distance to calculate SCA, SCB and SCC |
| WEB | 0.0 | | | No | Coefficient for SCB |
| WEC | 0.0 | | | No | Coefficient for SCC |

WPE Instance Parameters:

| Name | Default | Min | Max | Description |
|------|---------|-----|-----|--|
| SC | 0.0 | 0.0 | | Distance to a single well edge |
| SCA | 0.0 | 0.0 | | Integral of the first distribution function for scattered well dopant |
| SCB | 0.0 | 0.0 | | Integral of the second distribution function for scattered well dopant |

| Name | Default | Min | Max | Description |
|------|---------|-----|-----|---|
| SCC | 0.0 | 0.0 | | Integral of the third distribution function for scattered well dopant |

BSIM3 Version 3 Model — Usage Notes: Ig Model

HSPICE BSIM3 version 3 (Level=49, BSIM3 Version 3.2.2 or later) supports UC Berkeley's BSIM4.5 Ig (gate direct tunneling currents) model. To turn on this Ig model in BSIM3 version 3, specify IGCMOD=1 and/(or) IGBMOD=1 in your model cards.

Ig Model Parameters:

| Name | Default | Min | Max | Bin | Description |
|---------|-------------------------------|-----|-----|-----|---|
| AIGBACC | 1.36e-2 | | | Yes | Parameter for Ig _b |
| AIGBINV | 1.11e-2 | | | Yes | Parameter for Ig _b |
| AIGC | NMOS:1.36e-2/ PMOS:9.80e-3 | | | Yes | Parameter for Ig _c |
| AIGSD | NMOS:1.36e-2/ PMOS:9.80e-3 | | | Yes | Parameter for Ig _{s,d} |
| BIGBACC | 1.71e-3 | | | Yes | Parameter for Ig _b |
| BIGBINV | 9.49e-4 | | | Yes | Parameter for Ig _b |
| BIGC | NMOS:1.71e-3/ PMOS:7.59e-4 | | | Yes | Parameter for Ig _c |
| BIGSD | NMOS:1.71e-3/ PMOS:7.59e-4 | | | Yes | Parameter for Ig _{s,d} |
| CIGBACC | 0.075 | | | Yes | Parameter for Ig _b |
| CIGBINV | 0.006 | | | Yes | Parameter for Ig _b |
| CIGC | NMOS:0.075/ PMOS:0.03 | | | Yes | Parameter for Ig _c |
| CIGSD | NMOS:0.075/ PMOS:0.03 | | | Yes | Parameter for Ig _{s,d} |
| DLCIG | 0.0 | | | No | Delta L for Ig model |
| EIGBINV | 1.1 | | | Yes | Parameter for the Si bandgap for Igbinv |

Chapter 2: MOSFET Models

LEVEL 49 and 53: BSIM3 Version 3 MOSFET Model

| Name | Default | Min | Max | Bin | Description |
|-----------|----------|-----|-----|-----|---|
| IGBMOD | 0 | 0 | 1 | No | Gate-to-body Ig model selector |
| IGCMOD | 0 | 0 | 2 | No | Gate-to-channel Ig model selector |
| NIGBACC | 1.0 | 0.0 | | Yes | Parameter for lgbacc slope |
| NIGBINV | 3.0 | 0.0 | | Yes | Parameter for lgbinv slope |
| NIGC | 1.0 | 0.0 | | Yes | Parameter for lgc slope |
| NSD | 1.0e20 | | | Yes | S/D doping concentration |
| NTOX | 1.0 | | | Yes | Exponent for Tox ratio |
| PIGCD | 1.0 | 0.0 | | Yes | Parameter for lgc partition |
| POXEDGE | 1.0 | 0.0 | | Yes | Factor for the gate edge Tox |
| TEMPMOD | 0 | 0 | 2 | No | Temperature model selector |
| TOXE | TOX | 0.0 | | No | Electrical gate oxide thickness in meters |
| TOXREF | 30.0e-10 | 0.0 | | No | Target tox value |
| TVFBSDOFF | 0.0 | | | Yes | Temperature parameter for vfbsoff |
| VFBSDOFF | 0.0 | | | Yes | S/D flatband voltage offset |

BSIM3 Version 3 Model — Usage Notes: Charge Models

In BSIM3 version 3, the BSIM1 capacitance model is CAPMOD=0. Simulation replaces this with a modified BSIM1 capacitance model, based on the CAPOP=13 model in Level 49. Level 53 uses the Berkeley BSIM1 capacitance model for CAPMOD=0. The following table lists CAPMOD defaults for the Berkeley BSIM3 version 3 model, and for Levels 49 and 53.

| Version | BSIM3 version 3 | Level 49 | Level 53 |
|---------|-----------------|----------|----------|
| 3.0 | 1 | 1 | 1 |
| 3.1 | 2 | 0 | 2 |
| 3.2 | 3 | 3 | 3 |
| 3.3 | 3 | 3 | 3 |

VFBFLAG: The CAPMOD=0 capacitance model normally calculates the threshold voltage as $V_{th} = vfbc + \phi + k_1 * \sqrt{\phi - v_{bs}}$, where vfbc is the VFBCV model parameter. This eliminates any dependence on the VTH0 parameter. To allow capacitance dependence on VTH0, set the VFBFLAG=1 model parameter. The CAPMOD=0 capacitance model calculates the threshold voltage as $V_{th} = v_{th0} + k_1 * \sqrt{\phi - v_{bs}} - k_1 * \sqrt{\phi}$. The VFBFLAG default value is 0.

BSIM3 Version 3 Model — Usage Notes: Printback Options

You can printback all model parameters with units. The printback also indicates whether Berkeley or Synopsys model junction diodes and noise models are invoked, and which parameters are not used (for example, simulation does not use CJGATE if ACM=0-3).

BSIM3 Version 3 Model — Usage Notes: Mobility Multiplier

You can define mobility multiplier parameters in the BSIM3 version 3 instance line.

| Name | Default | Description |
|-------|---------|---|
| MULU0 | 1.0 | Low-field mobility (U0) multiplier |
| MULUA | 1.0 | First-order mobility degradation coefficient (UA) multiplier |
| MULUB | 1.0 | Second-order mobility degradation coefficient (UB) multiplier |

When HSPICE prints back a MOSFET element summary (.OPTION LIST), it identifies the BSIM3 version 3 MOSFET, and prints back these three additional instance parameters.

BSIM3 Version 3 MOSFET Model Parameters

These tables are a superset of the BSIM3 version 3 model parameter set, and include HSPICE parameters. These HSPICE parameters are noted in the description column, and always default (for Level 53) to maintain compliance with the BSIM3 version 3 standard. These parameters also apply to Level 49 with the following exceptions:

- [BSIM3 Version 3 Model — Model Flags](#)
- [BSIM3 Version 3 Model — Basic Parameters](#)
- [BSIM3 Version 3 Model — AC and Capacitance Parameters](#),

Chapter 2: MOSFET Models

LEVEL 49 and 53: BSIM3 Version 3 MOSFET Model

- [BSIM3 Version 3 Model — Length and Width Parameters](#)
- [BSIM3 Version 3 Model — Temperature Parameters](#)
- [BSIM3 Version 3 Model — Bin Description Parameters](#)
- [BSIM3 Version 3 Model — Process Parameters](#)
- [BSIM3 Version 3 Model — Noise Parameters](#)
- [BSIM3 Version 3 Model — Junction Parameters](#)
- [BSIM3 Version 3 Model — NonQuasi-Static \(NQS\) Parameters](#)
- [BSIM3 Version 3.2 Model — Parameters](#)

BSIM3 Version 3 Model — Model Flags

| Name | Unit | Default | Bin | Description |
|----------|------|---------|-----|---|
| VERSION | - | 3.3 | No | Selects from BSIM3 Versions 3.0, 3.1, 3.2, and 3.3. Issues a warning if you do not explicitly set it. |
| HSPVER | - | 98.2 | No | Selects from HSPICE Versions: 98.2, 97.4, 97.2, 96.4, 96.3, 96.1 |
| PARAMCHK | - | 0 | No | PARAMCHK=1 checks the model parameters for range compliance |
| APWARN | - | 0 | No | When >0 turns off the warning message for PS,PD < Weff (HSPICE specific) |
| BINFLAG | - | 0 | No | Uses wref, lref if you set this flag >0.9 (HSPICE) |
| MOBMOD | - | 1 | No | Selects a mobility model |
| CAPMOD | - | 3 | No | Selects from the 0,1,2,3 charge models Level 49 CAPMOD defaults to 0. |
| CAPOP | - | - | No | Obsolete for Levels 49 and 53. HSPICE ignores it (HSPICE specific) in all versions. |
| NOIMOD | - | 1 | No | Berkeley noise model flag |
| NLEV | - | -(off) | No | The noise model flag (non-zero overrides NOIMOD) (HSPICE specific). See MOSFET Noise Models for more information. |
| NQSMOD | - | 0 (off) | No | NQS Model flag |
| SFVTFLAG | - | 0 (off) | No | Spline function for Vth (HSPICE specific) |
| VFBFLAG | - | 0 (off) | No | VFB selector for CAPMOD=0 (HSPICE specific) |

| Name | Unit | Default | Bin | Description |
|----------|------|---------|-----|------------------------------------|
| ACNQSMOD | - | 0 | No | AC small-signal NQS model selector |

BSIM3 Version 3 Model — Basic Parameters

| Name | Unit | Default | Bin | Description |
|--------|-------------------|---------|-----|--|
| A0 | - | 1.0 | Yes | Bulk charge effect coefficient, channel length |
| A1 | 1/V | 0 | Yes | First nonsaturation factor |
| A2 | - | 1.0 | Yes | Second nonsaturation factor |
| AGS | 1/V | 0.0 | Yes | Gate bias coefficient of Abulk |
| ALPHA0 | m/V | 0 | Yes | First parameter of the impact ionization current |
| B0 | m | 0.0 | Yes | Bulk charge effect coefficient, channel width |
| B1 | m | 0.0 | Yes | Bulk charge effect width offset |
| BETA0 | V | 30 | Yes | Second parameter of the impact ionization current |
| CDSC | F/m ² | 2.4e-4 | Yes | Drain/source and channel coupling capacitance |
| CDSCB | F/Vm ² | 0 | Yes | Body coefficient for CDSC |
| CDSCD | F/Vm ² | 0 | Yes | Drain bias sensitivity of CDSC |
| CIT | F/m ² | 0.0 | Yes | Interface state capacitance |
| DELTA | V | 0.01 | Yes | Effective Vds parameter |
| DROUT | - | 0.56 | Yes | Length dependence coefficient of the DIBL correction parameter in R _{out} |
| DSUB | - | DROUT | Yes | DIBL coefficient exponent in the subthreshold region |
| DVT0 | - | 2.2 | Yes | Short channel effect coefficient 0 for V _{th} |
| DVT0W | 1/m | 0 | Yes | Narrow width coefficient 0 for V _{th} , small L |
| DVT1 | - | 0.53 | Yes | Short channel effect coefficient 1 for V _{th} |
| DVT1W | 1/m | 5.3e6 | Yes | Narrow width coefficient 1 for V _{th} , small L |

Chapter 2: MOSFET Models

LEVEL 49 and 53: BSIM3 Version 3 MOSFET Model

| Name | Unit | Default | Bin | Description |
|---------|----------------------|---------|-----|---|
| DVT2 | 1/V | -0.032 | Yes | Short channel effect coefficient 2 for V_{th} |
| DVT2W | 1/V | -0.032 | Yes | Narrow width coefficient 2 for V_{th} , small L |
| ETA0 | - | 0.08 | Yes | DIBL (drain induced barrier lowering) coefficient for the subthreshold region |
| ETAB | 1/V | -0.07 | Yes | DIBL coefficient for the subthreshold region |
| K1 | $V^{1/2}$ | 0.50 | Yes | First-order body effect coefficient |
| K2 | - | -0.0186 | Yes | Second-order body effect coefficient |
| K3 | - | 80.0 | Yes | Narrow width effect coefficient |
| K3B | 1/V | 0 | Yes | Body width coefficient, narrow width effect |
| KETA | 1/V | -0.047 | Yes | Body-bias coefficient of the bulk charge effect |
| NCH | cm^{-3} See (6) | 1.7e17 | Yes | Peak doping concentration near the interface |
| NFACTOR | - | 1.0 | Yes | Subthreshold region swing |
| NGATE | cm^{-3} | 0 | Yes | Poly gate doping concentration |
| NLX | m | 1.74e-7 | Yes | Lateral nonuniform doping along the channel |
| NSUB | cm^{-3} | 6.0e16 | Yes | Substrate doping concentration |
| PCLM | - | 1.3 | Yes | Coefficient of the channel length modulation values ≤ 0 result in an error message and program exit. |
| PDIBLC1 | - | 0.39 | Yes | Coefficient 1 for the DIBL (drain-induced barrier lowering) effect |
| PDIBLC2 | - | 0.0086 | Yes | Coefficient 2 for the DIBL effect |
| PDIBLCB | 1/V | 0 | Yes | Body effect coefficient of the DIBL effect coefficients |
| PRWB | $1/V^{1/2}$ | 0 | Yes | Body effect coefficient of RDSW |
| PRWG | 1/V | 0 | Yes | Gate bias effect coefficient of RDSW |
| PSCBE1 | V/m | 4.24e8 | Yes | Exponent 1 for the substrate current induced body effect |

Chapter 2: MOSFET Models
 LEVEL 49 and 53: BSIM3 Version 3 MOSFET Model

| Name | Unit | Default | Bin | Description |
|----------------|--------------------------------|-------------------------|-----|---|
| PSCBE2 | V/m | 1.0e-5 | Yes | Coefficient 2 for the substrate current induced body effect |
| PVAG | - | 0 | Yes | Gate dependence of Early voltage |
| RDSW | ohm · μm | 0.0 | Yes | Parasitic source drain resistance per unit width |
| RSH | 0.0 | ohm/square | No | Source/drain sheet resistance in ohm per square |
| TOX | m | 150e-10 | No | Gate oxide thickness |
| U0 | cm ² /V/sec | 670 nmos 250 pmos | Yes | Low field mobility at T=TREF=TNOM |
| UA | m/V | 2.25e-9 | Yes | First-order mobility degradation coefficient |
| UB | m ² /V ² | 5.87e-19 | Yes | Second-order mobility degradation coefficient |
| UC | 1/V | -4.65e-11 or -0.0465 | Yes | Body bias sensitivity coefficient of mobility -4.65e-11 for MOBMOD=1,2 or, -0.0465 for MOBMOD=3 |
| VBM | V | -3.0 | Yes | Maximum substrate bias for calculating V_{th} |
| VGSLIM | V | 0 | No | Asymptotic Vgs value, The Min value is 5V. 0—value indicates an asymptote of infinity. (HSPICE and Level 49 specific) |
| VOFF | V | -0.08 | Yes | Offset voltage in the subthreshold region |
| VSAT | m/sec | 8e4 | Yes | Saturation velocity of the carrier at T=TREF=TNOM |
| VTH0 (VTHO) | V | 0.7 NMOS -0.7 PMOS | Yes | Threshold voltage of the long channel device at $V_{bs}=0$ and small V_{ds} |
| W0 | m | 2.5e-6 | Yes | Narrow width effect coefficient |
| WR | - | 1.0 | Yes | Width offset from Weff for the Rds calculation |
| XJ | m | 0.15e-6 | Yes | Junction depth |

Chapter 2: MOSFET Models

LEVEL 49 and 53: BSIM3 Version 3 MOSFET Model

BSIM3 Version 3 Model — AC and Capacitance Parameters,

| Name | Unit | Default | Bin | Description |
|--------|------|------------|-----|--|
| XPART | - | 0 | No | Charge partitioning rate flag (default deviates from BSIM3 version 3=0) Level 49 XPART defaults to 1 |
| CGBO | F/m | 0 | No | Gate-bulk overlap capacitance per unit channel length |
| CGDO | F/m | p2 See (2) | No | Non-LDD region source-gate overlap capacitance per unit channel length |
| CGS1 | F/m | 0.0 | Yes | Lightly-doped source-gate overlap region capacitance |
| CGSO | F/m | p1 See (1) | No | Non-LDD region source-gate overlap capacitance per unit channel length |
| CF | F/m | See (3) | Yes | Fringing field capacitance |
| CGD1 | F/m | 0.0 | Yes | Lightly-doped drain-gate overlap region capacitance |
| CKAPPA | F/m | 0.6 | Yes | Coefficient for the lightly-doped region overlap capacitance fringing field capacitance |
| CLC | m | 0.1e-6 | Yes | Constant term for short channel model |
| CLE | - | 0.6 | Yes | Exponential term, short channel model |
| VFBCV | V | -1.0 | Yes | Flat band voltage, used only in CAPMOD=0 C-V calculations |

BSIM3 Version 3 Model — Length and Width Parameters

| Name | Unit | Default | Bin | Description |
|------|-------------|---------|-----|---|
| DLC | m | LINT | No | Length offset fitting parameter from CV |
| DWB | $m/V^{1/2}$ | 0.0 | Yes | Coefficient of the substrate body bias dependence for W_{eff} |
| DWC | m | WINT | No | Width offset fitting parameter from CV |
| DWG | m/V | 0.0 | Yes | Coefficient of the gate dependence for W_{eff} |
| LINT | m | 0.0 | No | Length offset fitting the parameter from the I-V without the bias |
| LL | m^{LLN} | 0.0 | No | Coefficient of the length dependence for the length offset |

| Name | Unit | Default | Bin | Description |
|------|---------------------|---------|-----|--|
| LLN | - | 1.0 | No | Power of the length dependence of the length offset |
| LW | m^{LWN} | 0.0 | No | Coefficient of the width dependence for the length offset |
| LWL | $m^{LWN} * m^{LLN}$ | 0.0 | No | Coefficient of the length and width cross term for the length offset |
| LWN | - | 1.0 | No | Power of the width dependence of the length offset |
| WINT | m | 0.0 | No | Width offset fitting parameter from I-V without bias |
| WLN | - | 1.0 | No | Power of the length dependence of the width offset |
| WW | m^{WWN} | 0.0 | No | Coefficient of the width dependence for the width offset |
| WWL | $m^{WWN} * m^{WLN}$ | 0.0 | No | Coefficient of the length and width cross term for the width offset |
| WWN | - | 1.0 | No | Power of the width depends on the width offset. |

BSIM3 Version 3 Model — Temperature Parameters

| Name | Unit | Default | Bin | Description |
|------|-------------|-----------|-----|--|
| AT | m/sec | 3.3e4 | Yes | Temperature coefficient for the saturation velocity |
| KT1 | V | -0.11 | Yes | Temperature coefficient for Vth |
| KT1L | $m \cdot V$ | 0.0 | Yes | Temperature coefficient for the channel length dependence of Vth |
| KT2 | - | 0.022 | Yes | Body bias coefficient of the Vth temperature effect |
| PRT | ohm-um | 0 | Yes | Temperature coefficient for RDSW |
| UA1 | m/V | 4.31e-9 | Yes | Temperature coefficient for UA |
| UB1 | $(m/V)^2$ | -7.61e-18 | Yes | Temperature coefficient for UB |
| UC1 | m/V^2 | -5.69e-11 | Yes | Temperature coefficient for UC |
| UTE | - | -1.5 | Yes | Mobility temperature exponent |
| XTI | - | 3.0 | No | Junction current temperature exponent |

Chapter 2: MOSFET Models

LEVEL 49 and 53: BSIM3 Version 3 MOSFET Model

BSIM3 Version 3 Model — Bin Description Parameters

| Name | Unit | Default | Bin | Description |
|---------|------|---------|-----|---|
| BINUNIT | | | | Assumes that WEFF, LEFF, WREF, Iref units are in microns if BINUNIT=1, or, in meters, otherwise |
| LMAX | m | 1.0 | No | Maximum channel length |
| LMIN | m | 0.0 | No | Minimum channel length |
| WMAX | m | 1.0 | No | Maximum channel width |
| WMIN | m | 0.0 | No | Minimum channel width |

BSIM3 Version 3 Model — Process Parameters

| Name | Unit | Default | Bin | Description |
|---------------------------|------------------|----------|-----|---|
| DTOXCV (capmod=3 only) | | | | Difference between the electrical and physical gate oxide thicknesses, due to the effects of the gate poly-depletion and finite channel charge layer thickness. |
| GAMMA1 | V ^{1/2} | See (8) | Yes | Body effect coefficient near the surface |
| GAMMA2 | V ^{1/2} | See (9) | Yes | Body effect coefficient in the bulk |
| VBX | V | See (10) | Yes | VBX at which the depletion region width equals XT |
| XT | m | 1.55e-7 | Yes | Doping depth |

BSIM3 Version 3 Model — Noise Parameters

| Name | Unit | Default | Bin | Description |
|---------|------|----------------------------|-----|--|
| AF | - | 1.0 | No | Flicker noise exponent |
| EF | - | 1.0 | No | Flicker noise frequency exponent |
| EM | V/m | 4.1e7 | No | Flicker noise parameter |
| KF | - | 0.0 | No | Flicker noise coefficient |
| LINTNOI | m | 0.0 | No | Length reduction parameter offset |
| NIOA | - | 1.0e20 nmos 9.9e18 pmos | No | Body effect coefficient near the surface |

| Name | Unit | Default | Bin | Description |
|------|------|-------------------------------|-----|---|
| NOIB | - | 5.0e4 nmos 2.4e3 pmos | No | Body effect coefficient in the bulk |
| NOIC | - | -1.4e-12 nmos 1.4e-12 pmos | No | VBX at which the depletion region width equals XT |

Note: See also [MOSFET Noise Models](#) for HSPICE noise model usage (the NLEV parameter for HSPICE overrides the Berkeley NOIMOD parameter).

BSIM3 Version 3 Model — Junction Parameters

| Name | Unit | Default | Bin | Description |
|--------|------------------|---------|-----|--|
| ACM | - | 10 | No | Area calculation method selector (HSPICE specific) <ul style="list-style-type: none"> ■ ACM=0-3 uses the HSPICE junction models ■ ACM=10-13 uses the Berkeley junction models Level 49 ACM defaults to 0 |
| CJ | F/m ² | 5.79e-4 | No | Zero-bias bulk junction capacitance (Default deviates from BSIM3 version 3=5.0e ⁻⁴) |
| CJGATE | F/m | CJSW | No | Zero-bias gate-edge sidewall bulk junction capacitance (HSPICE-specific) (use only if ACM=3) |
| CJSW | F/m | 0.0 | No | Zero-bias sidewall bulk junction capacitance (Default deviates from BSIM3 version 3=5.0e ⁻¹⁰) |
| CJSWG | F/m | CJSW | No | Zero-bias gate-edge sidewall bulk junction capacitance (use only with the Berkeley junction model, ACM=10-13) |
| JS | A/m ² | 0.0 | No | Bulk junction saturation current. (Default deviates from BSIM3 version 3=1.0e ⁻⁴) |
| JSW | A/m | 0.0 | No | Sidewall bulk junction saturation current |
| MJ | - | 0.5 | No | Bulk junction grading coefficient |
| MJSW | - | 0.33 | No | Sidewall bulk junction grading coefficient |

Chapter 2: MOSFET Models

LEVEL 49 and 53: BSIM3 Version 3 MOSFET Model

| Name | Unit | Default | Bin | Description |
|----------|------|---------|-----|---|
| MJSWG | - | MJSW | No | Gate-edge sidewall bulk junction grading coefficient (use only with the Berkeley junction model: ACM=10-13) HSPICE has no equivalent parameter. Always set the gate-edge grading coefficient to MJSW for the HSPICE junction model. |
| N | - | 1 | No | Emission coefficient (HSPICE-specific), (use only with the HSPICE junction model, ACM=0-3) |
| NJ | - | 1 | No | Emission coefficient (use only with the Berkeley junction model: ACM=10-13) |
| PB, PHIB | V | 1.0 | No | Bulk junction contact potential |
| PBSW | V | 1.0 | No | Sidewall bulk junction contact potential |
| PBSWG | V | PBSW | No | Gate-edge sidewall bulk junction contact potential (use only with the Berkeley junction model, ACM=10-13). HSPICE has no equivalent parameter. Gate-edge contact potential is always set to PHP for the HSPICE junction model. |
| PHP | V | 1.0 | No | Sidewall bulk junction contact potential (HSPICE) (use only with the HSPICE junction model: ACM=0-3) |

Note: See [MOSFET Noise Models](#) for HSPICE junction diode model usage.

BSIM3 Version 3 Model — NonQuasi-Static (NQS) Parameters

| Name | Unit | Default | Bin | Description |
|------|------|---------|-----|-----------------|
| ELM | - | 5.0 | Yes | Elmore constant |

BSIM3 Version 3.2 Model — Parameters

| Name | Unit | Default | Bin | Description |
|--------|------|---------|-----|--|
| ACDE | m/V | 1.0 | Yes | Exponential coefficient for the charge thickness in the accumulation and depletion regions |
| ALPHA1 | V-1 | 0.0 | Yes | Substrate current parameter |
| JTH | A | 0.1 | No | Diode limiting current |

| Name | Unit | Default | Bin | Description |
|--------|----------|----------|-----|--|
| LLC | mlln | LL | No | Coefficient of the length dependence for the C-V channel length offset |
| LWC | mlwn | LW | No | Coefficient of the width dependence for the C-V channel length offset |
| LWLC | mlln+lwn | LWL | No | Coefficient of the length and width for the C-V channel length offset |
| MOIN | m/V | 15.0 | Yes | Coefficient, gate-bias dependent surface potential |
| NOFF | - | 1.0 | Yes | I-V parameter, weak to strong inversion transition |
| TCJ | V/K | 0.0 | No | Temperature coefficient of CJ |
| TCJSW | V/K | 0.0 | No | Temperature coefficient of CJSW |
| TCJSWG | V/K | 0.0 | No | Temperature coefficient of CJSWG |
| TOXM | m | TOX | No | Reference gate oxide thickness |
| TPB | V/K | 0.0 | No | Temperature coefficient of PB |
| TPBSW | V/K | 0.0 | No | Temperature coefficient of PBSW |
| TPBSWG | V/K | 0.0 | No | Temperature coefficient of PBSWG |
| VFB | V | See (11) | Yes | DC flatband voltage |
| VOFFCV | - | 0.0 | Yes | C-V parameter, weak to strong inversion transition |
| WLC | mwln | WL | No | Coefficient of the length dependence for the C-V channel width offset |
| WWC | mwwn | WW | No | Coefficient of the width dependence for the C-V channel width offset |
| WWLC | mwln+ | WWL | No | Coefficient of the length and width cross terms for the C-V channel width offset |
| | | wwn | | |

BSIM3 Version 3 MOSFET Model — Parameter Range Limits

Simulation reports either a warning or a fatal error if BSIM3 version 3 parameters fall outside predefined ranges. These range limitations prevent (or at least warn of) potential numerical problems. Level 53 follows exactly the BSIM3 version 3 range limit reporting scheme. Level 49 deviates from the BSIM3 version 3 scheme as noted in the comments column in the following tables.

To control the maximum number of simulation warning messages printing to the output file, use:

```
.OPTION WARNLIMIT=#
```

In the preceding .OPTION statement, # is the maximum number of warning messages that simulation reports. The default WARNLIMIT value is 1. In some cases, simulation checks parameters only if you set the PARMAMCHK=1 model parameter.

This section covers the following topics:

- [BSIM3 Version 3 Model — Model Parameter Range Limit](#)
- [BSIM3 Version 3 Model — Element Parameter Range Limit](#)

BSIM3 Version 3 Model — Model Parameter Range Limit

| Name | Limits | Comments |
|-------|--|------------------------------------|
| A1 | - | See A2 conditions on the next line |
| A2 | <ul style="list-style-type: none">■ < 0.01 Warn and reset a2=0.01 if paramchk=1■ > 1 Warn and reset a2=1,a1=0 if paramchk=1 | |
| ACDE | < 0.4, >1.6 Warn | |
| B1 | =-Weff Fatal B1 + Weff < 10^{-7} Warn if paramchk=1 | |
| CDSC | < 0 Warn if paramchk=1 | |
| CDSCD | < 0 Warn if paramchk=1 | |
| CGB0 | < 0 Warn and reset to 0 if paramchk=1 | |

| Name | Limits | Comments |
|---------|---|--|
| CGD0 | < 0 Warn and reset to 0 if paramchk=1 | |
| CGS0 | < 0 Warn and reset to 0 if paramchk=1 | |
| DELTA | < 0 Fatal | |
| DROUT | < 0 Fatal if paramchk=1 | Level 49 reports a warning |
| DSUB | < 0 Fatal | < 0 Level 49 reports a warning |
| DVT0 | < 0 Warn if paramchk=1 | |
| DVT1 | < 0 Fatal | < 0 Level 49 reports a warning |
| DVT1W | < 0 Fatal | < 0 Level 49 reports a warning |
| ETA0 | <=0 Warn if paramchk=1 | |
| IJTH | < 0 Fatal | |
| MOIN | < 5.0, >25 Warn | |
| NCH | <=0 Fatal <=10 ¹⁵ Warn if paramchk=1 >=10 ²¹ Warn if paramchk=1 | if >10 ²⁰ simulation multiplies NCH by 10 ⁻⁶ before the other limit checks. |
| NFACTOR | < 0 Warn if paramchk=1 | |
| NGATE | < 0 Fatal > 10 ²⁵ Fatal <=10 ¹⁸ Fatal if paramchk=1 | if >10 ²³ simulation multiplies NGATE by 10 ⁻⁶ before the other limit checks. Level 49 returns: < 0 Fatal > 10 ²⁵ Warn <=10 ¹⁸ Warn if paramchk==1 |
| NLX | < -Leff Fatal < 0 Warn if paramchk=1 | |
| NOFF | < 0.1, >4.0 Warn | |
| NSUB | <=0 Fatal <=10 ¹⁴ Warn if paramchk=1 >=10 ²¹ Warn if paramchk=1 | Ignores NSUB if k1,k2 are defined |
| PCLM | <=0 Fatal | |
| PDIBLC1 | < 0 Warn if paramchk=1 | |

Chapter 2: MOSFET Models

LEVEL 49 and 53: BSIM3 Version 3 MOSFET Model

| Name | Limits | Comments |
|---------|---|--|
| PDIBLC2 | < 0 Warn if paramchk=1 | |
| PS | < Weff Warn | |
| PSCBE2 | <=0 Warn if paramchk=1 | |
| RDSW | < 0 Warn if paramchk=1 and reset rdsw=0 | |
| TOX | Min value=5e-10 <=0 Fatal < 10 ⁻⁹ Warn if paramchk=1 | BSIM3tox < 5e-10 is automatically reset to min value 5e-10 |
| TOXM | <=0 Fatal < 10 ⁻⁹ Warn if paramchk=1 | |
| U0 | <=0 Fatal | |
| VBM | | Ignored if you defined K1 and K2 |
| VSAT | <=0 Fatal < 10 ³ Warn if paramchk==1 | |
| W0 | =-Weff Fatal w0 + Weff < 10 ⁻⁷ Warn if paramchk==1 | |
| XJ | <=0 Fatal | |

BSIM3 Version 3 Model — Element Parameter Range Limit

| Name | Limits | Comments |
|--------|--------------------------------|----------|
| Leff | < 5.0 x 10 ⁻⁸ Fatal | |
| LeffCV | < 5.0 x 10 ⁻⁸ Fatal | |
| PD | < Weff, Warn | |
| PS | < Weff, Warn | |
| Weff | < 1.0 x 10 ⁻⁷ Fatal | |
| WeffCV | < 1.0 x 10 ⁻⁷ Fatal | |

For a list of output template parameters in the MOSFET models, and which parameters this model supports, see [MOSFET Output Templates](#).

BSIM3 Version 3 MOSFET Model Equations

The effective channel length and width in all model equations are:

$$L_{eff} = L_{drawn} - 2dL$$

$$W_{eff} = W_{drawn} - 2dW$$

$$W'_{eff} = W_{drawn} - 2dW'$$

$$W_{drawn} = W * WMULT + XW$$

$$L_{drawn} = L * LMULT + XL$$

- The unprimed W_{eff} is bias-dependent.
- The primed quantity is bias-independent.

$$dW = dW' + dW_g V_{gsteff} + dW_b (\sqrt{\phi_s - V_{bseff}} - \sqrt{\phi_s})$$

$$dW' = W_{int} + \frac{W_L}{L^{WLN}} + \frac{W_W}{W^{WWN}} + \frac{W_{WL}}{L^{WLN} W^{WWN}}$$

$$dL = L_{int} + \frac{L_L}{L^{LLN}} + \frac{L_W}{W^{LWN}} + \frac{L_{WL}}{L^{LLN} W^{LWN}}$$

C-V calculations replace dW' with:

$$dW' = DWC + \frac{W_{LC}}{L^{WLN}} + \frac{W_{WC}}{W^{WWN}} + \frac{W_{WLC}}{L^{WLN} W^{WWN}}$$

C-V also replaces dL' with:

$$dL = DLC + \frac{L_{LC}}{L^{LLN}} + \frac{L_{WC}}{W^{LWN}} + \frac{L_{WLC}}{L^{LLN} W^{LWN}}$$

Note: For details of BSIM3 Version 3 equations, see the web site:
<http://www-device.eecs.berkeley.edu/~bsim3/get.html>

BSIM3 Version 3 MOSFET Model — Additional Information

1. If you do not specify C_{gso} , simulation calculates it as follows:

- If you specify a d/c value that is greater than 0.0, then,

$cgs0=p1=\max(0, dlc*cox - cgs1)$

Otherwise, $cgs0=0.6*xj*cox$

2. If you do not specify C_{gdo} , simulation calculates it as follows:

- if you specify a d/c value that is greater than 0.0, then,

$cndo=p2=\max(0, dlc*cox - cndo1)$

Otherwise $cndo=0.6*xj*cox$

3. If you do not specify C_f , simulation calculates it using:

$$C_f = \frac{2\epsilon_{ox}}{\pi} \log\left(1 + \frac{4 \times 10^{-7}}{T_{ox}}\right)$$

4. If you do not specify V_{th0} in the .MODEL statement, simulation calculates it with $V_{fb}=-1$, using:

$$V_{th0} = V_{fb} + \phi_s + K_1 \sqrt{\phi_s}$$

5. If you do not specify K_1 and K_2 , simulation calculates it using:

$$K_1 = GAMMA_2 + 2K_2 \sqrt{\phi_s - V_{bs}}$$

$$K_2 = \frac{(GAMMA_2 - GAMMA_1)(\sqrt{\phi_s - V_{bs}} - \sqrt{\phi_s})}{2\sqrt{\phi_s}(\sqrt{\phi_s - V_{bm}} - \sqrt{\phi_s}) + V_{bm}}$$

6. If you do not specify n_{ch} , but you specify $GAMMA1$, then simulation calculates n_{ch} from:

$$n_{ch} = \frac{GAMMA_1^2 C_{ox}^2}{2q\epsilon_{si}}$$

7. If you do not specify n_{ch} or $GAMMA1$, then nch defaults to $1.7e17$ per cubic meter and simulation calculates $GAMMA1$ from n_{ch} .

8. If you do not specify `PHI`, simulation calculates it using:

$$\phi_s = 2 \frac{k_B T}{q} \log\left(\frac{n_{ch}}{n_i}\right)$$

$$n_i = 1.45 \times 10^{10} \left(\frac{T}{300.15}\right)^{1.5} \exp\left(21.5565981 - \frac{qE_g(T)}{2k_B T}\right)$$

$$E_g(T) = 1.16 - \frac{7.02 \times 10^{-4} T^2}{T + 1108}$$

9. If you do not specify `GAMMA1`, simulation calculates it using:

$$GAMMA_1 = \frac{\sqrt{2q\epsilon_{si}n_{ch}}}{C_{ox}}$$

10. If you do not specify `GAMMA2`, simulation calculates it using:

$$GAMMA_2 = \frac{\sqrt{2q\epsilon_{si}n_{sub}}}{C_{ox}}$$

11. If you do not specify `Vbx`, simulation calculates it using:

$$V_{bx} = \phi_s - \frac{qn_{ch}X_t^2}{2\epsilon_{si}}$$

12. The BSIM3 model can calculate `Vth` in any of three ways:

- Using `K1` and `K2` values that you specify
- Using `GAMMA1`, `GAMMA2`, `VBM`, and `VBX` values that you enter in the `.MODEL` statement
- Using `NPEAK`, `NSUB`, `XT`, and `VBM` values that you specify

You can enter the `U0` model parameter in meters or centimeters. Simulation converts `U0` to m²/Vsec as follows: if `U0` is greater than 1, it is multiplied by 1e-4. You must enter the `NSUB` parameter in cm⁻³ units.

Specify a negative value of `VTH0` for the p-channel in the `.MODEL` statement.

The `PSCBE1` and `PSCBE2` model parameters determine the impact ionization current, which contributes to the bulk current.

Chapter 2: MOSFET Models

LEVEL 49 and 53: BSIM3 Version 3 MOSFET Model

BSIM3 Version 3 MOSFET Model Examples

The following is an example of a NMOS model for the Level 49 MOSFET. VTH0 is positive.

```
.model nch nmos Level=49
+ Tnom=27.0
+ nch=1.024685E+17 tox=1.00000E-08 xj=1.00000E-07
+ lint=3.75860E-08 wint=-2.02101528644562E-07
+ vth0=.6094574 k1=.5341038 k2=1.703463E-03 k3=-17.24589
+ dvt0=.1767506 dvt1=.5109418 dvt2=-0.05
+ nlx=9.979638E-08 w0=1e-6
+ k3b=4.139039
+ vsat=97662.05 ua=-1.748481E-09 ub=3.178541E-18 uc=1.3623e-10
+ rdsW=298.873 u0=307.2991 prwb=-2.24e-4
+ a0=.4976366
+ keta=-2.195445E-02 a1=.0332883 a2=.9
+ voff=-9.623903E-02 nFactor=.8408191 cit=3.994609E-04
+ cdsc=1.130797E-04
+ cdscb=2.4e-5
+ eta0=.0145072 etab=-3.870303E-03
+ dsub=.4116711
+ pclm=1.813153 pdiblc1=2.003703E-02 pdiblc2=.00129051
+ pdiblcb=-1.034e-3
+ drout=.4380235 pscbe1=5.752058E+08 pscbe2=7.510319E-05
+ pvag=.6370527 prt=68.7 ngate=1.e20 alpha0=1.e-7 beta0=28.4
+ prwg=-0.001 ags=1.2
+ dvt0w=0.58 dvt1w=5.3e6 dvt2w=-0.0032
+ kt1=-.3 kt2=-.03
+ at=33000
+ ute=-1.5
+ ua1=4.31E-09 ub1=7.61E-18 uc1=-2.378e-10
+ kt1l=1e-8
+ wr=1 b0=1e-7 b1=1e-7 dwg=5e-8 dwb=2e-8 delta=0.015
+ cgdl=1e-10 cgsl=1e-10 cgbo=1e-10 xpart=0.0
+ cgdo=0.4e-9 cgso=0.4e-9
+ clc=0.1e-6
+ cle=0.6
+ ckappa=0.6
```

The following is an example of a PMOS model for the Level 49 MOSFET. VTH0 is negative.

```
.model pch PMOS Level=49
+ Tnom=27.0
+ nch=5.73068E+16 tox=1.00000E-08 xj=1.00000E-07
+ lint=8.195860E-08 wint=-1.821562E-07
+ vth0=-.86094574 k1=.341038 k2=2.703463E-02 k3=12.24589
```

```
+ dvt0=.767506 dvt1=.65109418 dvt2=-0.145
+ nlx=1.979638E-07 w0=1.1e-6
+ k3b=-2.4139039
+ vsat=60362.05 ua=1.348481E-09 ub=3.178541E-19 uc=1.1623e-10
+ rdsW=498.873 u0=137.2991 prwb=-1.2e-5
+ a0=.3276366
+ keta=-1.8195445E-02 a1=.0232883 a2=.9
+ voff=-6.623903E-02 nFactor=1.0408191 cit=4.994609E-04
+ cdsc=1.030797E-3
+ cdscb=2.84e-4
+ eta0=.0245072 etab=-1.570303E-03
+ dsub=.24116711
+ pclm=2.6813153 pdiblc1=4.003703E-02 pdiblc2=.00329051
+ pdiblcb=-2.e-4
+ drout=.1380235 pscbe1=0 pscbe2=1.e-28
+ pvag=-.16370527
+ prwg=-0.001 ags=1.2
+ dvt0w=0.58 dvt1w=5.3e6 dvt2w=-0.0032
+ kt1=-.3 kt2=-.03 prt=76.4
+ at=33000
+ ute=-1.5
+ ua1=4.31E-09 ub1=7.61E-18 uc1=-2.378e-10
+ kt1l=0
+ wr=1 b0=1e-7 b1=1e-7 dwg=5e-8 dwb=2e-8 delta=0.015
+ cgdl=1e-10 cgsl=1e-10 cgbo=1e-10 xpart=0.0
+ cgdo=0.4e-9 cgso=0.4e-9
+ clc=0.1e-6
+ cle=0.6
+ ckappa=0.6
```

LEVEL 50: Philips MOS9 Model

This model defaults to version 903. if you set the model parameter VERSION, you can control it to either version 902 or 903. The 903 version includes parameters NFMOD, NFAR, NFBR, NFCR, SL3VT0. If you set version=902, it will select the 902 model. The Phillips MOS Model 9 is available as Level 50 in the Synopsys models (based on the “Unclassified Report NL-UR 003/94” by R.M.D.A. Velghe, D.B.M. Klaassen, and F.M. Klaassen).

MOSFET Level 50 incorporates all features of Philips MOS 9, except for the gate noise current. You can select either of two MOSFET Level 50 diode models:

- ACM Parasitic Diode Model by using the JS, JSW, N, CJ, CJSW, CJGATE, MJ, MJSW, PB, PHP, ACM, and HDIF parameters. This version does not use the older IS parameter. To use this model, select the JUNCAP=0 (default) parameter.
- Philips JUNCAP Parasitic Diode Model. To use this model, select the JUNCAP=1 model parameter.

This section covers the following topics:

- [Philips MOS9 Model Parameters](#)
- [Philips MOS9 Model — JUNCAP Parameters](#)
- [Using the Philips MOS9 Model](#)
- [Philips MOS9 Model — Example](#)

Philips MOS9 Model Parameters

| Name | Unit | Default (N) | Default (P) | Description |
|-------|------------------|-------------|-------------|---|
| A1R | - | 6.0 | 10.0 | Weak-avalanche current factor |
| A2R | V | 38.0 | 59.0 | Exponent of weak-avalanche current |
| A3R | - | 650.0e-3 | 520.0e-3 | Factor of minimum drain bias, above which avalanche sets in |
| ALPR | - | 3.0e-3 | 44.0e-3 | Channel length modulation factor |
| BETSQ | AV ⁻² | 83.0e-6 | 26.1e-6 | Gain factor of infinite square transistor |

| Name | Unit | Default (N) | Default (P) | Description |
|---------|------------|-------------|-------------|---|
| COL | F/m | 320.0e-12 | 320.0e-12 | Gate overlap capacitance per unit width |
| ETAALP | - | 150.0e-3 | 170.0e-3 | Exponent of length dependence of ALPR |
| ETABET | - | 1.6 | 1.6 | Exponent of temperature dependence of gain factor |
| ETADSR | - | 600.0e-3 | 600.0e-3 | Exponent of drain dependence of GAM1R |
| ETAGAMR | - | 2.0 | 1.0 | Exponent of back-bias dependence of zero gate-drive, drain-induced threshold shift |
| ETAMR | - | 2.0 | 1.0 | Exponent of back-bias dependence of the subthreshold slope |
| ETAZET | - | 170.0e-3 | 30.0e-3 | Exponent of length dependence of ZET1R |
| FBET1 | - | 0 | 0 | Relative mobility decrease due to the first profile |
| FBET2 | - | 0 | 0 | Relative mobility decrease due to the second profile |
| FTHE1 | - | 0 | 0 | Coefficient describing the width dependence of THE1 for $W < W_{\text{DOG}}$ |
| GAM1R | - | 145.0e-3 | 77.0e-3 | Drain-induced threshold shift coefficient for high gate drive |
| GAMOOR | - | 18.0e-3 | 7.0e-3 | Drain-induced threshold shift coefficient, at zero gate drive, and zero back-bias |
| GTHE1 | - | 0 | 0 | Parameter that selects either the old (=0) or the new (=1) scaling rule of θ_1 |
| KOR | $V^{-1/2}$ | 650.0e-3 | 470.0e-3 | Low-back-bias body factor |
| KR | $V^{-1/2}$ | 110.0e-3 | 470.0e-3 | High-back-bias body factor |
| LAP | m | 100.0e-9 | 25.0e-9 | Lateral diffusion per side |
| LER | m | 1.1e-6 | 1.25e-6 | Reference Leff |
| LP1 | M | 1E-6 | 1E-6 | Characteristic length of the first profile |
| LP2 | M | 1E-8 | 1E-8 | Characteristic length of the second profile |
| LVAR | m | -220.0e-9 | -460.0e-9 | Variation in gate length |

Chapter 2: MOSFET Models
 LEVEL 50: Philips MOS9 Model

| Name | Unit | Default (N) | Default (P) | Description |
|----------|---------------------------------|-------------|-------------|---|
| MOR | - | 500.0e-3 | 375.0e-3 | Subthreshold slope factor |
| NFAR | V ⁻¹ m ⁻² | 7.15e+22 | 1.53xe+22 | 1st flicker noise coefficient added in release 98.4 |
| NFBR | V ⁻¹ m ⁻² | 2.16e+06 | 4.06e+06 | 2nd flicker noise coefficient added in release 98.4 |
| NFCR | V ⁻¹ | 0.0 | 2.92e-10 | 3rd flicker noise coefficient added in release 98.4 |
| NFMOD | | 0 | | Flicker noise selector. 0 selects the old flicker noise model added in release 98.4 |
| NFR | V ² | 70.0e-12 | 21.4e-12 | Flicker noise coefficient |
| NTR | J | 24.4e-21 | 21.1e-21 | Thermal noise coefficient |
| PHIBR | V | 650.0e-3 | 650.0e-3 | Strong inversion surface potential |
| SL2GAMOO | - | 0 | 0 | Second coefficient of the γ_{00} length dependence |
| SL2K | V ^{1/2} m ² | 0 | 0 | Second coefficient of the length dependence of K |
| SL2KO | V ^{1/2} m ² | 0 | 0 | Second coefficient of the length dependence of K_0 |
| SL2VTO | Vm ² | 0.0 | 0.0 | Second length dependence of VTO |
| SL3VTO | V | 0 | 0 | Third coefficient of the length dependence of VTO |
| SLA1 | m | 1.3e-6 | -15.0e-6 | Length dependence of A1R |
| SLA2 | Vm | 1.0e-6 | -8.0e-6 | Length dependence of A2R |
| SLA3 | m | -550.0e-9 | -450.0e-9 | Length dependence of A3R |
| SLALP | - | -5.65e-3 | 9.0e-3 | Coefficient of length dependence of ALPR |
| SLGAM1 | - | 160.0e-9 | 105.0e-9 | Length dependence of GAM1R |
| SLGAMOO | m ² | 20.0e-15 | 11.0e-15 | Length dependence of GAMOOR |
| SLK | V ^{-1/2} m | -280.0e-9 | -200.0e-9 | Length dependence of K |
| SLKO | V ^{-1/2} m | -130.0e-9 | -200.0e-9 | Length dependence of k_0 |
| SLMO | m ^{1/2} | 280.0e-6 | 47.0e-6 | Length dependence coefficient of MOR |

| Name | Unit | Default (N) | Default (P) | Description |
|---------|----------------------|-------------|-------------|---|
| SLTHE1R | V ^{-1m} | 140.0e-9 | 70.0e-9 | Length dependence coefficient of THE1R |
| SLTHE2R | V ^{-1/2m} | -33.0e-9 | -75.0e-9 | Length dependence coefficient of THE2R |
| SLTHE3R | V ^{-1m} | 185.0e-9 | 27.0e-9 | Length dependence coefficient of THE3R |
| SLVSBT | Vm | -4.4e-6 | 0.0 | Length dependence of VSBTR |
| SLVSBX | Vm | 0.0 | 0.0 | Length dependence of VSBX |
| SLVTO | Vm | -135.0e-9 | 35.0e-9 | Length dependence of VTO |
| SLZET1 | - | -390.0e-3 | -2.8 | Length dependence coefficient of ZET1R |
| STA1 | K ⁻¹ | 0.0 | 0.0 | Temperature coefficient of A1R |
| STLTHE1 | V ^{-1m/K} | 0.0 | 0.0 | Temperature dependence of the length dependence for THE1R |
| STLTHE2 | V ^{-1/2m/K} | 0.0 | 0.0 | Temperature dependence of the length dependence for THE2R |
| STLTHE3 | V ^{-1m/K} | -620.0e-12 | 0.0 | Temperature dependence of the length dependence for THE3R |
| STMO | K ⁻¹ | 0.0 | 0.0 | Temperature dependence coefficient MOR |
| STTHE1R | V ^{-1/K} | 0.0 | 0.0 | Temperature dependence coefficient THE1R |
| STTHE2R | V ^{-1m/K} | 0.0 | 0.0 | Temperature dependence coefficient THE2R |
| STTHE3R | V ^{-1/K} | -660.0e-6 | 0.0 | Temperature dependence coefficient of THE3R |
| STVTO | V/K | -1.2e-3 | -1.7e-3 | Temperature dependence of VTO |
| SWA1 | m | 3.0e-6 | 30.0e-6 | Width dependence of A1R |
| SWA2 | Vm | 2.0e-6 | 15.0e-6 | Width dependence of A2R |
| SWA3 | m | 0.0 | -140.0e-9 | Width dependence of A3R |
| SWALP | m | 1.67e-9 | 180.0e-12 | Coefficient of width dependence of ALPR |
| SWGAM1 | - | -10.0e-9 | -11.0e-9 | Width dependence of GAM1R |
| SWK | V ^{-1/2m} | 275.0e-9 | 115.0e-9 | Width dependence of K |

Chapter 2: MOSFET Models
 LEVEL 50: Philips MOS9 Model

| Name | Unit | Default (N) | Default (P) | Description |
|--------|---------------------|-------------|-------------|--|
| SWKO | V ^{-1/2} m | 2.0e-9 | 115.0e-9 | Width dependence of k ₀ |
| SWTHE1 | V ⁻¹ m | -58.0e-9 | -80.0e-9 | Width dependence coefficient of THE1R |
| SWTHE2 | V ^{-1/2} m | 30.0e-9 | 20.0e-9 | Width dependence coefficient of THE2R |
| SWTHE3 | V ⁻¹ m | 20.0e-9 | 11.0e-9 | Width dependence coefficient of THE3R |
| SWVSBX | Vm | -675.0e-9 | 0.0 | Width dependence of VSBX |
| SWVTO | Vm | 130.0e-9 | 50.0e-9 | Width dependence of VTO |
| THE1R | V ⁻¹ | 190.0e-3 | 190.0e-3 | Gate-induced mobility reduction coefficient |
| THE2R | V ^{-1/2} | 12.0e-3 | 165.0e-3 | Back-bias induced mobility reduction coefficient |
| THE3R | V ⁻¹ | 145.0e-3 | 27.0e-3 | Lateral field induced mobility reduction coefficient |
| TOX | m | 25.0e-9 | 25.0e-9 | Oxide thickness |
| TR | °C | 21.0 | 21.0 | Reference temperature for model |
| VPR | V | 340.0e-3 | 235.0e-3 | Characteristic voltage for channel length modulation |
| VSBTR | V | 2.1 | 100.0 | Limiting voltage for back-bias dependence |
| VSBXR | V | 660.0e-3 | 0.0 | Transition voltage for dual-k-factor model |
| VTOR | V | 730.0e-3 | 1.1 | Threshold voltage at zero bias |
| WDOG | m | 0 | 0 | Characteristic drawn gate width, below which dogboning appears |
| WER | m | 20.0e-6 | 20.0e-6 | Reference Weff |
| WOT | m | 0.0 | 0.0 | Channel-stop diffusion per side |
| WVAR | m | -25.0e-9 | -130.0e-9 | Variation in active width |
| ZET1R | - | 420.0e-3 | 1.3 | Weak-inversion correction factor |

Philips MOS9 Model — JUNCAP Parameters

The following are JUNCAP model parameters specific to this model:

| Name | Unit | Default | Description |
|--------|-------------------|----------|---|
| JUNCAP | - | 0 | JUNCAP flag: 0-off, 1-on. |
| CJBR | F*m ⁻² | 1.00e-12 | Bottom junction capacitance at V=V _R . |
| CJGR | F*m ⁻¹ | 1.00e-12 | Gate edge junction capacitance at V=V _R . |
| CJSR | F*m ⁻¹ | 1.00e-12 | Sidewall junction capacitance at V=V _R . |
| DTA | °C | 0.0 | Temperature offset of JUNCAP element relative to T _A . |
| JSDBR | A*m ⁻² | 1.00e-3 | Bottom saturation-current density due to diffusion from back contact. |
| JSDGR | A*m ⁻¹ | 1.00e-3 | Gate edge saturation-current density due to diffusion from back contact. |
| JSDSR | A*m ⁻¹ | 1.00e-3 | Sidewall saturation-current density due to diffusion from back contact. |
| JSGBR | A*m ⁻² | 1.00e-3 | Bottom saturation-current density due to electron-hole generation at V=V _R . |
| JSGGR | A*m ⁻¹ | 1.00e-3 | Gate edge saturation-current density due to electron-hole generation at V=V _R |
| JSGSR | A*m ⁻¹ | 1.00e-3 | Sidewall saturation-current density due to electron-hole generation at V=V _R . |
| NB | - | 1.00 | Emission coefficient of the bottom forward current. |
| NG | - | 1.00 | Emission coefficient of the gate edge forward current. |
| NS | - | 1.00 | Emission coefficient of the sidewall forward current. |
| PB | - | 0.40 | Bottom-junction grading coefficient. |
| PG | - | 0.40 | Gate edge-junction grading coefficient. |
| PS | - | 0.40 | Sidewall-junction grading coefficient. |

| Name | Unit | Default | Description |
|--------|------|---------|---|
| TH3MOD | - | 1 | Switch that activates THE3-clipping: <ul style="list-style-type: none"> ▪ If TH3MOD ==1 (default), effective THE3 can be slightly negative, and clipping does not occur. ▪ If TH3MOD ==0, this model clips the effective THE3 to more than zero. |
| VDBR | v | 1.00 | Diffusion voltage of the bottom junction at $T=T_R$. |
| VDGR | v | 1.00 | Diffusion voltage of the gate edge junction at $T=T_R$. |
| VDSR | v | 1.00 | Diffusion voltage of the sidewall junction at $T=T_R$. |
| VR | V | 0.0 | Voltage at which simulation determines the parameters. |

Using the Philips MOS9 Model

To use the Philips MOS9 model:

1. Set LEVEL=50 to identify the model as the Philips MOS Model 9.
2. The default room temperature is 25°C in Synopsys circuit simulators, but is 27°C in most other simulators. When comparing to other simulators, set the simulation temperature to 27 use .TEMP 27 or .OPTION TNOM=27.
3. The model parameter set must include the TR model reference temperature, which corresponds to TREF in other model levels. The default for TR is 21.0°C to match the Philips simulator.
4. This model has its own charge-based capacitance model. Level 50 ignores the CAPOP parameter, which selects different capacitance models.
5. This model uses analytical derivatives for the conductances. This model ignores the DERIV parameter, which selects the finite difference method.
6. DTEMP increases the temperature of individual elements relative to the circuit temperature. Set DTEMP on the element line.
7. Defaults are nonzero so use the .MODEL statement to set every model parameter listed in the Level 50 Model Parameters table.
8. Use the JUNCAP model parameter to select one of two available parasitic junction diode models, ACM or JUNCAP. JUNCAP=1 selects the Philips JUNCAP model, JUNCAP=0 (default) selects the ACM model.

9. Philips added a switch named TH3MOD to MOS Model 9. You can use this switch to re-activate effective THE3 clipping, which was removed in an earlier version of this model.
- If TH3MOD==1 (default), effective THE3 can be slightly negative, and clipping does not occur.
 - If TH3MOD==0, this model clips the effective THE3 to more than zero.

Philips MOS9 Model — Example

```
.model nch nmos Level=50
+ ler =1e-6 wer=10e-6
+ lvar =0.0 lap=0.05e-6
+ wvar =0.0 wot=0.0
+ tr  = 27.00 vtor=0.8
+ stvto =0 slvto=0
+ sl2vto =0 swvto=0
+ kor =0.7 slko=0
+ swko =0 kr=0.3
+ slk =0 swk=0
+ phibr =0.65 vsbxr=0.5
+ slvsbx =0 swvsbx=0
+ betsq =120e-6 etabet=1.5
+ the1r =0.3 stthe1r=0
+ slthe1r =0 stlthe1=0
+ swthe1 =0 the2r=0.06
+ stthe2r =0 slthe2r=0
+ stlthe2 =0 swthe2=0
+ the3r =0.1 stthe3r=0
+ slthe3r =0 stlthe3=0
+ swthe3 =0 gam1r=0.02
+ slgam1 =0 swgaml=0
+ etadsr =0.60 alpr=0.01
+ etaalp =0 slalp=0
+ swalp =0 vpr=0.4
+ gamoor =0.006 slgamoo=0
+ etagamr =2.0 mor=0.5
+ stmo =0 slmo=0
+ etamr =2.0 zet1r=1.0
+ etazet =0.5 slzet1=0
+ vsbtr =2.5 slvsbt=0
+ a1r =10 sta1=0
+ slal1 =0 swal1=0
```

Chapter 2: MOSFET Models

LEVEL 50: Philips MOS9 Model

```
+ a2r =30 sla2=0
+ swa2 =0 a3r=0.8
+ sla3 =0 swa3=0
+ tox =15.00e-9 col=0.3e-9
+ ntr =2.0e-20 nfr=5.0e-11
+ acm =2 hdif=1u
+ js =1e-3 cj=1e-3
+ mj =0.5 pb=0.8
+ cjsw =1e-9 cjgate=1e-9
+ mjsw =0.3 php=0.8
```

LEVEL 54: BSIM4 MOSFET Model

The UC Berkeley BSIM4 model explicitly addresses many issues in modeling sub-0.13 micron CMOS technology and RF high-speed CMOS circuit simulation. The Level 54 model is based on the UC Berkeley BSIM4 MOS model. BSIM4.5 is fully supported in this release. For details, see the BSIM web site:

<http://www-device.eecs.berkeley.edu/~bsim3/bsim4.html>

The following sections discuss these topics:

- [BSIM4 MOSFET Model — General Syntax](#)
 - [BSIM4 MOSFET Model Parameters](#)
 - [BSIM4 MOSFET Model — Usage Notes](#)
 - [BSIM4 MOSFET Model — Version Updates](#)
 - [BSIM4 MOSFET Model — Output Templates](#)
-

BSIM4 MOSFET Model — General Syntax

The general syntax for including a BSIM4 model element in a netlist is:

```
Mxxx nd ng ns [nb] mname [L=val] [W=val] [M=val]
+ [AD=val] [AS=val] [PD=val] [PS=val]
+ [RGATEMOD=val] [RBODYMOD=val] [TRNQSMOD=val]
+ [ACNQSMOD=val] [GEOMOD=val] [RGEOMOD=val]
+ [NRS=val] [NRD=val] [RBPB=val] [RBPD=val]
+ [RBPS=val] [RBDB=val] [RBSB=val] [NF=val]
+ [MIN=val] [RDC=val] [RSC=val] [DELVTO=val]
+ [MULU0=val] [DELK1=val] [DELNFCT=val]
+ [DELTOX=val] [OFF] [IC=Vds, Vgs, Vbs]
+ [WNFLAG=val] [MULID0=val]
```

BSIM4 MOSFET Model Parameters

| Parameter | Description |
|--------------|-------------------------------------|
| <i>MNAME</i> | MOSFET model name reference. |
| ACNQSMOD | AC small-signal NQS model selector. |

Chapter 2: MOSFET Models

LEVEL 54: BSIM4 MOSFET Model

| Parameter | Description |
|--------------------|--|
| GEOMOD | Geometry-dependent parasitics model selector—specifies how the end S/D diffusions connect. |
| RBODYMOD | Substrate resistance network model selector. |
| RGATEMOD | Gate resistance model selector. |
| RGEOMOD | Source/drain diffusion resistance and contact model selector—specifies the end S/D contact type: point wide or merged) and how to compute the S/D parasitics resistance. |
| TRNQSMOD | Transient NQS model selector. |
| WNFLAG | Turn on to select bin model based on width per NF for multi-finger devices. |
| AD | Drain diffusion area. |
| AS | Source diffusion area. |
| DELK1 | Shift in body bias coefficient (K1). |
| DELNFACT | Shift in subthreshold swing factor (NFACTOR). |
| DELTOX | Shift in gate electrical and physical oxide thickness (TOXE and TOXP). That is, the difference between the electrical and physical gate oxide/insulator thicknesses. |
| DELVTO (DELVT0) | Shift in the VTH0 zero-bias threshold voltage. |
| IC | Initial guess in the order |
| L | BSIM4 MOSFET channel length in meters. |
| MIN | Whether to minimize the number of drain or source diffusions for even-number fingered device. |
| MULID0 | Scaling factor of drain current, the default is 1.0. |
| MULU0 | Low-field mobility (U0) multiplier. |
| NB | Bulk terminal node name. |
| ND | Drain terminal node name. |
| NF | Number of device fingers. |
| NG | Gate terminal node name. |
| NRD | Number of drain diffusion squares. |

| Parameter | Description |
|-----------|---|
| NRS | Number of source diffusion squares. |
| NS | Source terminal node name. |
| OFF | Sets the initial condition to OFF in DC analysis. |
| PD | Perimeter of the drain junction: <ul style="list-style-type: none"> ■ If PERMOD=0, it excludes the gate edge. ■ Otherwise, it includes the gate edge. |
| PS | Perimeter of the source junction: <ul style="list-style-type: none"> ■ If PERMOD=0, it excludes the gate edge. ■ Otherwise, it includes the gate edge. |
| RBDB | Resistance connected between dbNode and bNode. |
| RBPB | Resistance connected between bNodePrime and bNode. |
| RBPD | Resistance connected between bNodePrime and dbNode. |
| RBPS | Resistance connected between bNodePrime and sbNode. |
| RBSB | Resistance connected between sbNode and bNode. |
| RDC | Drain contact resistance for per-finger device. |
| RSC | Source contact resistance for per-finger device. |
| W | BSIM4 MOSFET channel width in meters. |

BSIM4 MOSFET Model — Usage Notes

This section covers the following topics:

- [BSIM4 Model — Usage Notes: Improvements Over BSIM3 Version 3](#)
- [BSIM4 Model — Usage Notes: Parameter Range Limit](#)
- [BSIM4 Model — Usage Notes: TSMC Diode Model](#)
- [BSIM4 Model — Usage Notes: JUNCAP2 Model Support](#)
- [BSIM4 Model — Usage Notes: STI / LOD Parameters](#)
- [BSIM4 Model — Usage Notes: LMLT and WMLT Parameters](#)
- [BSIM4 Model — Usage Notes: HSPICE Junction Diode Model and ACM](#)

BSIM4 Model — Usage Notes: Improvements Over BSIM3 Version 3

BSIM4 includes the following major improvements and additions over BSIM3 version 3:

- An accurate new model of the intrinsic input resistance (R_{ii}) for both RF, high-frequency analog, and high-speed digital applications
- A flexible substrate resistance network for RF modeling
- A new accurate channel thermal noise model, and a noise partition model for the induced gate noise
- A non-quasi-static (NQS) model consistent with the R_{ii} -based RF model, and a consistent AC model that accounts for the NQS effect in both transconductances and capacitances
- An accurate gate direct tunneling model
- A comprehensive and versatile geometry-dependent parasitics model for source/drain connections and multi-finger devices
- An improved model for steep vertical retrograde doping profiles
- A better model for pocket-implanted devices in V_{th} , the bulk charge effect model, and R_{out}
- An asymmetrical and bias-dependent source/drain resistance, either internal or external to the intrinsic MOSFET
- Accepts either the electrical or physical gate oxide thickness as the model input in a physically accurate manner
- A quantum mechanical charge-layer-thickness model for both IV and CV
- A more accurate mobility model for predictive modeling
- A gate-induced drain leakage (GIDL) current model, not available in earlier BSIM models
- An improved unified flicker ($1/f$) noise model, which is smooth over all bias regions, and which considers the bulk charge effect
- Different diode IV and CV characteristics for the source and drain junctions
- A junction diode breakdown with or without current limiting
- A dielectric constant of the gate dielectric as a model parameter
- .OPTION LIST now prints the total capacitances, instead of just the intrinsic capacitances for the BSIM4 (Level 54) MOSFET model

BSIM4.2.1 has the following improvements over BSIM4.2.0:

- A new **GISL** (Gate Induced Source Leakage) current component corresponds to the same current at the drain side (**GIDL**).
- The warning limits for effective channel length, channel width, and gate oxide thickness have been reduced to avoid unnecessary warnings if you use BSIM4 aggressively, beyond the desired model card application ranges.
- The **DELTOX** parameter in the MOS active element (M) models the relative variation on the trans conductance (oxide thickness) of the MOS in Monte Carlo analysis.
- **.OPTION LIST** can now print an element summary for the MOSFET Level=54 model

BSIM4 Model — Usage Notes: Parameter Range Limit

Simulation reports either a warning or a fatal error if BSIM3 version 3 parameters fall outside predefined ranges. These range limitations prevent (or at least warn of) potential numerical problems.

To control the maximum number of simulation warning messages printing to the output file, use:

```
.OPTION WARNLIMIT=#
```

In the preceding **.OPTION** statement, # is the maximum number of warning messages that simulation reports. The default **WARNLIMIT** value is 1. In some cases, simulation checks parameters only if you set the **PARMAMCHK=1** model parameter.

| Parameter | Limits | Comment |
|-----------|--------------------------|--|
| ACDE | < 0.1, > 1.6 warn | if (version < 4.29999) acde<0.4 warn |
| B1 | b1=-weff fatal | |
| CKAPPAD | < 0.02 warn and set 0.02 | if (version >= 4.299999 &&stiMod != 2) version < 4.299999 |
| CKAPPAS | < 0.02 warn and set 0.02 | if (version >= 4.299999 &&stiMod != 2) version < 4.299999 |
| CLC | < 0 fatal | |
| DELTA | < 0 fatal | |
| DROUT | < 0 fatal | |
| DSUB | < 0 fatal | |

Chapter 2: MOSFET Models

LEVEL 54: BSIM4 MOSFET Model

| Parameter | Limits | Comment |
|-----------|----------------------------------|---|
| DVT1 | < 0 fatal | |
| DVT1W | < 0 fatal | |
| GBMIN | < 1.0e-20 warn | |
| LINTNOI | > leff/2, fatal | if (version>=4.39999) |
| LPE0 | < -leff, fatal | |
| LPEB | < -leff, fatal | |
| MOIN | < 5.0, > 25 warn | |
| NDEP | <= 0 fatal | |
| NF | < 1 fatal | |
| NGATE | < 0,> 1.0e25 fatal | |
| NGCON | < 1 fatal | If ngcon !=1,2 warn and set 1 |
| NOFF | =0 warn and set 1; < 0.1 warn | if (version < 4.2999 stiMod=2) noff > 4 warn |
| NSUB | <= 0 fatal | |
| PCLM | <= 0 fatal | |
| PHIN | < -0.4 fatal | if (version>=4.4 phin <=0 fatal) |
| PSCBE2 | <= 0 fatal | |
| TOXREF | <= 0 fatal | |
| VOFFCV | < -0.5 warn | if (version<4.2999 stiMod=2) voffcv > 0.5 warn |
| W0 | w0=-weff fatal | |
| XJ | <= 0 fatal | |

If PARAMCHK=1 the following parameter limit range is added

| | | |
|----|---|--|
| A2 | < 0.01 warn, set 0.01; >1 .0 warn, set 1 and a1 set 0 | <ul style="list-style-type: none"> ■ If the total calculated A2 (including binnings) is smaller than 0.01, then it is set to 0.01. ■ If the total A2 is larger than 1, it is set to 1. |
|----|---|--|

| Parameter | Limits | Comment |
|-----------|-----------------------|---|
| B1 | b1+weff< 1e-7 warn | if (version>=4.39999) b1+weff<1e-9 warn |
| CDSC | < 0 warn | |
| CDSCD | < 0 warn | |
| CGBO | < 0 warn | if (version >4.4999) |
| CGDO | < 0 warn | |
| CGSO | < 0 warn | |
| DVT0 | < 0 warn | |
| ETA0 | < 0 warn | |
| KVSAT | < -1.0, > 1.0 fatal | |
| LAMBDA | > 1e-9 warn | if (version>=4.3) |
| LC | < 0 | if (version>= 4.3) |
| LEFF | <= 1e-9 warn | |
| LEFFCV | <= 1e-9 warn | |
| LODETA0 | <= 0 warn | if (version>= 4.4) |
| LODETA0 | <= 0 | |
| LODK2 | <= 0 warn | if (version>= 4.4) |
| LODK2 | <= 0 | |
| MJD | >= 0.99 warn | |
| MJS | >= 0.99 warn | |
| MJSWD | >= 0.99 warn | |
| MJSWGD | >= 0.99 warn | |
| MJSWGS | >= 0.99 warn | |
| MJSWS | >= 0.99 warn | |
| NDEP | <= 1e12, >= 1e21 warn | |

Chapter 2: MOSFET Models

LEVEL 54: BSIM4 MOSFET Model

| Parameter | Limits | Comment |
|-----------|-----------------------|------------------|
| NF | >1 fatal | if (stiMod == 2) |
| NFACTOR | < 0 warn | |
| NGATE | 0 <ngate <= 1e18 warn | |
| NIGBACC | <= 0 fatal | |
| NIGBINV | <= 0 fatal | |
| NIGC | <= 0 fatal | |
| NJD | < 0 warn | |
| NJS | < 0 warn | |
| NJTS | < 0 warn | |
| NJTSD | < 0 warn | |
| NJTSSW | < 0 warn | |
| NJTSSWD | < 0 warn | |
| NJTSSWG | < 0 warn | |
| NJTSSWGD | < 0 warn | |
| NSUB | <= 1e14, >= 1e21 warn | |
| NTNOI | < 0 warn | |
| PDIBL1 | < 0 warn | |
| PDIBL2 | < 0 warn | |
| PDITS | < 0 fatal | |
| PDITSL | < 0 fatal | |
| PIGCD | <= 0 fatal | |
| POXEDGE | <= 0 fatal | |
| PROUT | < 0 fatal | |
| PRWG | < 0 warn, set 0 | |

| Parameter | Limits | Comment |
|-----------|-------------------------------|---|
| RDS0 | < 0 warn, set 0 | |
| RDSW | < 0 warn, set 0 | |
| RDSWMIN | < 0 warn, set 0 | |
| RNOIA | < 0 warn | |
| RNOIB | < 0 warn | |
| RSHG | <= 0 warn | if (version >= 4.299999 && stlMod != 2) |
| SA | < 0 fatal | |
| SA0 | <= 0 fatal | |
| SB | < 0 fatal | |
| SB0 | <= 0 fatal | |
| SC | < 0 warn | if (wpemod=1) |
| SCA | < 0 warn | if (wpemod=1) |
| SCB | < 0 warn | if (wpemod=1) |
| SCC | < 0 warn | if (wpemod=1) |
| SCREF | < 0 warn | if (wpemod=1) |
| SD | < 0 fatal | If nf>1 |
| SL | < 1e-7 warn; < 0 fatal | |
| SW | < 1e-7 warn; < 0 fatal | |
| TNOB | < 0 warn | |
| TNOIA | < 0 warn | |
| TOXE | Toxe + Deltox < 1e-10 warn | |
| TOXM | < 1e-10 warn | |
| TOXP | Toxp + Deltox < 1e-10 warn | |

Chapter 2: MOSFET Models

LEVEL 54: BSIM4 MOSFET Model

| Parameter | Limits | Comment |
|-----------|--------------------|---|
| VSATTEMP | <1e3 warn | |
| VTL | < 6e4 warn | if (version>=4.3) |
| VTSD | < 0 warn | |
| VTSS | < 0 warn | |
| VTSSWD | < 0 warn | |
| VTSSWGD | < 0 warn | |
| VTSSWGS | < 0 warn | |
| VTSSWS | < 0 warn | |
| W0 | w0+weff< 1e-7 warn | if (version>=4.39999) w0+weff < 1e-9 warn |
| WEFF | <= 1e-9 warn | |
| WEFFCV | <= 1e-9 warn | |
| WLOD | < 0 fatal | |
| XN | < 3 | if (version>=4.3) |
| XRCRG1 | <=0 warn | if (version >= 4.299999 && stiMod != 2) |

BSIM4 Model — Usage Notes: TSMC Diode Model

HSPICE MOSFET Level 54 (BSIM4) supports a TSMC junction diode model. You can use this TSMC junction diode model to simulate the temperature dependence, source/body, and drain/body currents of a junction diode.

Note: For a complete description of this effect model, visit the official UCB BSIM web site:

<http://www-device.eecs.berkeley.edu/~bsim3/>

You can order either of these models directly from Taiwan Semiconductor Manufacturing Company (TSMC)—not from Synopsys. See the TSMC web site: <http://www.tsmc.com>

BSIM4 Model — Usage Notes: JUNCAP2 Model Support

HSPICE BSIM4 support for the juncap2 junction model is based on Philips JUNCAP2 model in BSIM4 version 4.2 and later. You use the flag JUNCAP=0 to

turn on the built-in BSIM4 default junction model. You can use JUNCAP=1 to switch to the Juncap1 model and JUNCAP=2 to access the Juncap2 model. The Juncap2 model has 2 versions, 200.0 and 200.1, which can be toggled using the JCAP2VERSION flag.

| Parameter | Unit | Default | Description |
|--------------|--------------------|-----------|--|
| JUNCAP | - | 0 | Flag to turn on juncap diode model, 1 for juncap1, 2 for juncap2 |
| JCAP2VERSION | - | 200.1 | Juncap2 model version (200.0, 200.1) |
| CBBTBOT | AV ³ | 1.00E-012 | Band-to-band tunneling pre-factor of bottom component |
| CBBTGAT | AV ⁻³ m | 1.00E-018 | Band-to-band tunneling pre-factor of gate-edge component |
| CBBTSTI | AV ⁻³ m | 1.00E-018 | Band-to-band tunneling pre-factor of STI-edge component |
| CJORBOT | F/m ² | 1.00E-003 | Zero-bias capacitance per unit-of-area of bottom component |
| CJORGAT | F/m ² | 1.00E-009 | Zero-bias capacitance per unit-of-length of gate-edge component |
| CJORSTI | F/m ² | 1.00E-009 | Zero-bias capacitance per unit-of-length of STI-edge component |
| CSRHBOT | A/m ² | 1.00E+002 | Shockley-Read-Hall pre-factor of bottom component |
| CSRHGAT | A/m ² | 1.00E-004 | Shockley-Read-Hall pre-factor of gate-edge component |
| CSRHSTI | A/m ² | 1.00E-004 | Shockley-Read-Hall pre-factor of STI-edge component |
| CTATBOT | A/m ³ | 1.00E+002 | Trap-assisted tunneling pre-factor of bottom component |
| CTATGAT | A/m ² | 1.00E-004 | Trap-assisted tunneling pre-factor of gate-edge component |
| CTATSTI | A/m ² | 1.00E-004 | Trap-assisted tunneling pre-factor of STI-edge component |
| FBBTRBOT | V/m | 1.00E+009 | Normalization field at the reference temperature for band-to-band tunneling of bottom component |
| FBBTRGAT | V/m | 1.00E+009 | Normalization field at the reference temperature for band-to-band tunneling of gate-edge component |
| FBBTRSTI | V/m | 1.00E+009 | Normalization field at the reference temperature for band-to-band tunneling of STI-edge component |

Chapter 2: MOSFET Models

LEVEL 54: BSIM4 MOSFET Model

| Parameter | Unit | Default | Description |
|------------|------------------|------------|---|
| IDSATRBOT | A/m ² | 1.00E-012 | Saturation current density at the reference temperature of bottom component |
| IDSATRGAT | A _m | 1.00E-018 | SATURATION current density at the reference temperature of gate-edge component |
| IDSATRSTI | A/m | 1.00E-018 | Saturation current density at the reference temperature of STI-edge component |
| IMAX | A | 1000 | Maximum current up to which forward current behaves exponentially |
| MEFFTATBOT | - | 0.25 | Effective mass (in units of m ₀) for trap-assisted tunneling of bottom component |
| MEFFTATGAT | - | 0.25 | Effective mass (in units of m ₀) for trap-assisted tunneling of gate-edge component |
| MEFFTATSTI | - | 0.25 | Effective mass (in units of m ₀) for trap-assisted tunneling of STI-edge component |
| PBOT | - | 0.5 | Grading coefficient of bottom component |
| PBRBOT | V | 4 | Breakdown onset tuning parameter of bottom component |
| PBRGA | V | 4 | Breakdown onset tuning parameter of gate-edge component |
| PBRSTI | V | 4 | Breakdown onset tuning parameter of STI-edge component |
| PGAT | - | 0.5 | Grading coefficient of gate-edge component |
| PHIGBOT | V | 1.16 | Zero-temperature bandgap voltage of bottom component |
| PHIGGAT | V | 1.16 | Zero-temperature bandgap voltage of gate-edge component |
| PHIGSTI | V | 1.16 | Zero-temperature bandgap voltage of STI-edge component |
| PSTI | - | 0.5 | Grading coefficient of STI-edge component |
| STFBBTBOT | 1/K | -1.00E-003 | Temperature scaling parameter for band-to-band tunneling of bottom component |
| STFBBTGAT | 1/K | -1.00E-003 | Temperature scaling parameter for band-to-band tunneling of gate-edge component |
| STFBBTSTI | 1/K | -1.00E-003 | Temperature scaling parameter for band-to-band tunneling of STI-edge component |

| Parameter | Unit | Default | Description |
|-----------|------|-----------|--|
| VBIRBOT | V | 1 | Built-in voltage at the reference temperature of bottom component |
| VBIRGAT | V | 1 | Built-in voltage at the reference temperature of gate-edge component |
| VBIRSTI | V | 1 | Built-in voltage at the reference temperature of TI-edge component |
| VBRBOT | V | 10 | Breakdown voltage of bottom component |
| VBRGAT | V | 10 | Breakdown voltage of gate-edge component |
| VBRSTI | V | 10 | Breakdown voltage of STI-edge component |
| XJUNGAT | m | 1.00E-007 | Junction depth of gate-edge component |
| XJUNSTI | m | 1.00E-007 | Junction depth of STI-edge component |

BSIM4 Model — Usage Notes: STI / LOD Parameters

HSPICE BSIM4 supports the full STI (Shallow Trench Isolation) or LOD (Length of Oxide Definition) induced mechanical stress-effect model (for version 4.3 or later), which was first released in the UCB BSIM4.3.0 model version. HSPICE BSIM4 turns on the simulation of this effect when the following conditions (consistent with those of the UCB BSIM4 model) are satisfied:

```
if (VERSION >=4.3)
{
  if ((SA > 0 and SB > 0 and NF==1) or ( SA > 0 and SB > 0 and (NF >1 and SD > 0 )))
  { UCB's STI/LOD model is turned on}
}
```

If VERSION>=4.3, the STI model is not dependent on STIMOD=0 or 1. In this case, the STI model is applied to the model similar to the UCB STI model. When parameter values that satisfy SA>0, SB>0, NF>1, and SD=0 are given in model cards, no evaluation of such effect is performed.

| Parameter | Unit | Default | Bin? | Description |
|----------------------------------|------|--------------------------------|------|--|
| STIMOD (Also instance parameter) | | 0.0 (V < 4.3) 1.0 (V >=4.3) | | STI model selector, which gives priority to the instance parameter. <ul style="list-style-type: none"> ■ 0: No STI effect. ■ 1: UCB's STI model ■ 2: TSMC's STI model |

Chapter 2: MOSFET Models

LEVEL 54: BSIM4 MOSFET Model

| Parameter | Unit | Default | Bin? | Description |
|-------------------------|------|---------|------|---|
| KU0 | M | 0.0 | No | Mobility degradation/enhancement coefficient for stress effect |
| KVSAT | M | 0.0 | No | Saturation velocity degradation/enhancement |
| | | | | parameter for stress effect. 1.0<=kvsat<=1.0 |
| KVTH0 | V*m | 0.0 | No | Threshold shift parameter for stress effect |
| LKU0 | | 0.0 | No | Length dependence of KU0 |
| LLODKU0 | | 0.0 | No | Length parameter for U0 stress effect, >0 |
| LLODVTH | | 0.0 | No | Length parameter for Vth stress effect, >0 |
| LODETA0 | M | 1.0 | No | ETA0 shift modification factor for stress effect, >0 |
| LODK2 | m | 1.0 | No | K2 shift modification factor for stress effect, >0 |
| PKVTH0 | | 0.0 | No | Cross-term dependence of KVTH0 |
| SA (instance parameter) | | 0.0 | | Distance between S/D diffusion edge to poly gate edge from one side. If not given, or, if (<=0), the stress effect is turned off. |
| SAREF | M | 1e-06 | No | Reference distance for SA, >0.0 |
| SB (instance parameter) | | 0.0 | | Distance between S/D diffusion edge to poly gate edge from the other side. If not given or, if (<=0), the stress effect is turned off |
| SBREF | M | 1e-06 | No | Reference distance for SB, >0.0 |
| SD (instance parameter) | | 0.0 | | Distance between neighboring fingers. For NF >1, If not given or (<=0), stress effect is turned off |
| STETA0 | | 0.0 | No | ETA0 shift factor related to VTH0 change |
| STK2 | | 0.0 | No | K2 shift factor related to VTh0 change |
| TKU0 | | 0.0 | No | Temperature coefficient of KU0 |
| WKU0 | | 0.0 | No | Width dependence of KU0 |

| Parameter | Unit | Default | Bin? | Description |
|-----------|------|---------|------|---|
| WKVTH0 | | 0.0 | No | Width dependence of KVTH0 |
| WLOD | M | 0.0 | No | Width parameter for stress effect |
| WLODKU0 | | 0.0 | No | Width parameter for U0 stress effect, >0 |
| WLODVTH | | 0.0 | No | Width parameter for Vth stress effect, >0 |

BSIM4 Model — Usage Notes: LMLT and WMLT Parameters

You can use `LMLT` and `WMLT` to shrink the length and width in memory design. The `LMLT` and `WMLT` parameters are unitless, and are used to scale (usually scale down) MOSFET drawn length and width (specified in BSIM4 MOSFET instance lines), respectively. This makes memory design and netlist creation quite convenient because most (if not all) memory circuits use the smallest feature sizes as the process capability improves, even within the same generation of CMOS technology.

The shrunken device length and width will then be further offset (by `XL` and `XW`, respectively) to the actual device size in lithography and etching process steps, and finally to the electrical size as a result of subsequent ion implementation and annealing steps.

| Name (Alias) | Default | Description |
|-------------------|---------|---------------------------------|
| <code>LMLT</code> | 1.0 | Channel length shrinking factor |
| <code>WMLT</code> | 1.0 | Device width shrinking factor |

Both `LMLT` and `WMLT` must be greater than 0; if not, simulation resets them to 1.0 (default) and issues a warning message.

To use these two parameters, add them in the model cards, without any other modifications. For example:

```
.model nmos nmos
+ level=54 lmlt=0.85 wmlt=0.9
```

- The drawn channel length (`L`) is multiplied by `LMLT`.
- The drawn channel width (`w`) is multiplied by `WMLT`,

BSIM4 evaluates the effective length and width, L_{eff} and W_{eff} , as:

Chapter 2: MOSFET Models

LEVEL 54: BSIM4 MOSFET Model

```
Leff=Lnew - 2.0 * dL  
Weff=Wnew - 2.0 * dW
```

L_{new} and W_{new} are evaluated as:

```
Lnew=L + XL  
Wnew=W + XW
```

dL and dW are evaluated with L_{new} and W_{new}:

```
T0=pow (Lnew, LLN)  
T1=pow (Wnew, LWN)  
dL=LINT + LL/T0 + LW / T1 + LWL / (T0*T1)  
T2=pow (Lnew, WLN)  
T3=pow (Wnew, WWN)  
dW=WINT + WL / T2 + WW / T3 + WWL / (T2*T3)
```

Similarly, the preceding equations determine the L_{dIc}, L_{dIcig}, L_{eff}CV, W_{dwc}, W_{dwcig}, W_{eff}CV, W_{eff}CJ, grgeltd, and W_{new} model variables and quantities.

When multiplied by the LMLT and WMLT parameters, L_{eff} and W_{eff} become:

```
Leff=Lnew' - 2.0 * dL  
Weff=Wnew' - 2.0 * dW
```

L_{new'} and W_{new'} are evaluated as:

```
Lnew'=L * LMLT + XL  
Wnew'=W * WMLT + XW
```

Similarly, dL, dW, L_{dIc}, L_{dIcig}, L_{eff}CV, W_{dwc}, W_{dwcig}, W_{eff}CV, W_{eff}CJ, and grgeltd are all evaluated from L_{new'} and W_{new'}.

BSIM4 Model — Usage Notes: HSPICE Junction Diode Model and ACM

BSIM4 now supports Area Calculation Method (ACM) similar to BSIM3 version 3 for the following models and corresponding ACM values:

- For the HSPICE junction model, specify ACM=0,1,2, or 3.
- For the Berkeley BSIM4 junction model, specify ACM=10,11,12, or 13.

For the junction current, junction capacitance, and parasitic resistance equations corresponding to ACM=0,1,2,3 see [MOSFET Diode Models](#).

JUNCAP Model Parameters:

| Parameter | Description |
|-----------|--------------------------|
| nf | Number of device fingers |

| Parameter | Description |
|-----------|--|
| min | Whether to minimize the number of drain or source diffusions for even-number fingered device |
| rdbd | Resistance connected between the internal drain-side body node and the external body node |
| rbsb | Resistance connected between the internal source-side body node and the external body node |
| rbpb | Resistance connected between the internal reference body node and the external body node |
| rbps | Resistance connected between the internal reference body node and the internal drain-side body node |
| rbpd | Resistance connected between the internal reference body node and the internal source-side body node |
| trnqsmod | Transient NQS model selector |
| acnqsmod | AC small-signal NQS model selector |
| rbodymod | Substrate resistance network model selector |
| rgatemod | Gate resistance model selector |
| geomod | Geometry-dependent parasitics model selector |
| rgeomod | Source/Drain diffusion resistance and contact model selector |

MOSFET Level 54 uses the generic MOSFET model parameters described in [Common MOSFET Model Parameters](#). It also uses the parameters described in this section, which apply only to MOSFET Level 54.

The simulation calculates Rd and Rs as follows:

$$\begin{aligned} \text{Rd}(\text{TEMP}) &= \text{Rd}(\text{TNOM}) * (1 + \text{TRD} * (\text{TEMP} - \text{TNOM})) \\ \text{Rs}(\text{TEMP}) &= \text{Rs}(\text{TNOM}) * (1 + \text{TRS} * (\text{TEMP} - \text{TNOM})) \end{aligned}$$

JUNCAP Instance Parameters:

| Parameter | Unit | Default | Description |
|-----------|------|---------|---|
| RDC | ohm | 0.0 | Drain contact resistance for the per-finger device |
| RSC | ohm | 0.0 | Source contact resistance for the per-finger device |

Chapter 2: MOSFET Models

LEVEL 54: BSIM4 MOSFET Model

| Parameter | Unit | Default | Description |
|--------------------|-----------|---------|---|
| DELVTO (DELVT0) | V | 0.0 | Shift in the zero-bias threshold voltage (VTH0) |
| MULU0 | | 1.0 | Low-field mobility (U0) multiplier |
| DELK1 | $V^{1/2}$ | | Shift in the body bias coefficient (K1) |
| DELNFCT | | 0.0 | Shift in subthreshold swing factor (NFACTOR) |

Model Selectors / Controllers:

| Parameter | Default | Bin | Description |
|-----------|---------------------------|-----|---|
| VERSION | 4.5 | NA | Model version number |
| BINUNIT | 1 | NA | Binning unit selector |
| PARAMCHK | 1 | NA | Switch for the parameter check |
| MOBMOD | 1 | NA | Mobility model selector |
| RDSMOD | 0 | NA | Bias-dependent source/drain resistance model selector |
| IGCMOD | 0 | NA | Gate-to-channel tunneling current model selector |
| IGBMOD | 0 | NA | Gate-to-substrate tunneling current model selector |
| CAPMOD | 2 | NA | Capacitance model selector |
| RGATEMOD | 0 (no gate resistance) | | Gate resistance model selector |
| RBODYMOD | 0 (network off) | NA | Substrate resistance network model selector |
| TRNQSMOD | 0 | NA | Transient NQS model selector |
| ACNQSMOD | 0 | NA | AC small-signal NQS model selector |
| FNOIMOD | 1 | NA | Flicker noise model selector |
| TNOIMOD | 0 | NA | Thermal noise model selector |
| DIOMOD | 1 | NA | Source/drain junction diode IV model selector |
| TEMPPMOD | 0 | NA | Temperature mode selector |

| Parameter | Default | Bin | Description |
|-----------|------------------------------------|-----|--|
| PERMOD | 1 | NA | PS/PD includes/excludes the gate-edge perimeter |
| GEOMOD | 0 (isolated) | NA | Geometry-dependent parasitics model selector |
| RGEOMOD | 0 (no S/D diffusion resistance) | NA | Source/drain diffusion resistance and contact model selector |
| WPEMOD | 0 | NA | Flag for WPE model (WPEMOD=1 to activate this model) |

Process Parameters:

| Parameter | Default | Bin | Description |
|----------------------------------|--------------------------|-----|---|
| EPSROX | 3.9 (SiO ₂) | No | Gate dielectric constant relative to vacuum |
| TOXE | 3.0e-9m | No | Electrical gate equivalent oxide thickness |
| TOXP | TOXE | No | Physical gate equivalent oxide thickness |
| TOXM | TOXE | No | Tox at which simulation extracts parameters |
| DTOX | 0.0m | No | Defined as (TOXE-TOXP) |
| XJ | 1.5e-7m | Yes | S/D junction depth |
| GAMMA1 (γ_1 in equation) | calculated ($V^{1/2}$) | Yes | Body-effect coefficient near the surface |
| GAMMA2 (γ_2 in equation) | calculated ($V^{1/2}$) | Yes | Body-effect coefficient in the bulk |
| NDEP | 1.7e17cm ⁻³ | Yes | Channel doping concentration at the depletion edge for the zero body bias |
| NSUB | 6.0e16cm ⁻³ | Yes | Substrate doping concentration |
| NGATE | 0.0cm ⁻³ | Yes | Poly Si gate doping concentration |
| NSD | 1.0e20cm ⁻³ | Yes | Source/drain doping concentration |
| VBX | calculated (v) | No | V_{bs} at which the depletion region width equals XT |
| XT | 1.55e-7m | Yes | Doping depth |

Chapter 2: MOSFET Models

LEVEL 54: BSIM4 MOSFET Model

| Parameter | Default | Bin | Description |
|-----------|---------------|-----|---------------------------------|
| RSH | 0.0ohm/square | No | Source/drain sheet resistance |
| RSHG | 0.1ohm/square | No | Gate electrode sheet resistance |

Basic Model Parameters:

| Parameter | Default | Bin | Description |
|--------------------------|-------------------------|-----|--|
| A0 | 1.0 | Yes | Coefficient of the channel-length dependence of the bulk charge effect |
| A1 | 0.0V ⁻¹ | Yes | First non-saturation effect parameter |
| A2 | 1.0 | Yes | Second non-saturation factor |
| AGS | 0.0V ⁻¹ | Yes | Coefficient of the V _{gs} dependence of the bulk charge effect |
| B0 | 0.0m | Yes | Bulk charge effect coefficient for the channel width |
| B1 | 0.0m | Yes | Bulk charge effect width offset |
| CDSC | 2.4e-4F/m ² | Yes | Coupling capacitance between the source/drain and the channel |
| CDSCB | 0.0F/(Vm ²) | Yes | Body-bias sensitivity of CDSC |
| CDSCD | 0.0(F/Vm ²) | Yes | Drain-bias sensitivity of DCSC |
| CIT | 0.0F/m ² | Yes | Interface trap capacitance |
| DELTA δ (in equation) | 0.01V | Yes | Parameter for DC V _{dself} |
| DROUT | 0.56 | Yes | Channel-length dependence of the DIBL effect on Rout |
| DSUB | DROUT | Yes | DIBL coefficient exponent in the subthreshold region |
| DVT0 | 2.2 | Yes | First coefficient of the short-channel effect on V _{th} |
| DVT0W | 0.0 | Yes | First coefficient of the narrow width effect on V _{th} for a small channel length |

| Parameter | Default | Bin | Description |
|-----------|-------------------------|-----|--|
| DVT1 | 0.53 | Yes | Second coefficient of the short-channel effect on V_{th} |
| DVT1W | $5.3e6m^{-1}$ | Yes | Second coefficient of the narrow width effect on V_{th} for a small channel length |
| DVT2 | $-0.032V^{-1}$ | Yes | Body-bias coefficient of the short-channel effect on V_{th} |
| DVT2W | $-0.032V^{-1}$ | Yes | Body-bias coefficient of narrow width effect for small channel length |
| DVTP0 | 0.0m | Yes | First coefficient of the drain-induced V_{th} shift due to long-channel pocket devices |
| DVTP1 | $0.0V^{-1}$ | Yes | First coefficient of the drain-induced V_{th} shift due to long-channel pocket devices |
| DWB | $0.0m/V^{1/2}$ | Yes | Coefficient of the body bias dependence of the Weff bias dependence |
| DWG | $0.0m/V$ | Yes | Coefficient of gate bias dependence of Weff |
| ETA0 | 0.08 | Yes | DIBL coefficient in the subthreshold region |
| ETAB | $-0.07V^{-1}$ | Yes | Body-bias coefficient for the DIBL effect for the subthreshold |
| EU | 1.67 (NMOS); 1.0 (PMOS) | No | Exponent for the mobility degradation of MOBMOD=2 |
| FPROUT | $0.0V/m^{0.5}$ | Yes | Effect of the pocket implant on Rout degradation |
| K1 | $0.5V^{1/2}$ | Yes | First-order body bias coefficient |
| K2 | 0.0 | Yes | Second-order body bias coefficient |
| K3 | 80.0 | Yes | Narrow width coefficient |
| K3B | $0.0V^{-1}$ | Yes | Body effect coefficient of K3 |
| KETA | $-0.047V^{-1}$ | Yes | Body-bias coefficient of the bulk charge effect |
| LINT | 0.0m | No | Channel-length offset parameter |
| LP | $1e-8(m)$ | Yes | Mobility channel length degradation of MOBMOD=2 |

Chapter 2: MOSFET Models

LEVEL 54: BSIM4 MOSFET Model

| Parameter | Default | Bin | Description |
|-----------|---|-----|--|
| LPE0 | 1.74e-7m | Yes | Lateral non-uniform doping parameter |
| LPEB | 0.0m | Yes | Lateral non-uniform doping effect on K1 |
| MINV | 0.0 | Yes | V_{gsteff} fitting parameter for the moderate inversion condition |
| NFACTOR | 1.0 | Yes | Subthreshold swing factor |
| PCLM | 1.3 | Yes | Channel-length modulation parameter |
| PDIBLC1 | 0.39 | Yes | Parameter for the DIBL effect on Rout |
| PDIBLC2 | 0.0086 | Yes | Parameter for the DIBL effect on Rout |
| PDIBLCB | 0.0V ⁻¹ | Yes | Body bias coefficient of the DIBL effect on Rout |
| PDITS | 0.0V ⁻¹ | Yes | Impact of the drain-induced V_{th} shift on Rout |
| PDITSD | 0.0V ⁻¹ | Yes | V_{ds} dependence of the drain-induced V_{th} shift for Rout |
| PDITSL | 0.0m ⁻¹ | No | Channel-length dependence of the drain-induced V_{th} shift for Rout |
| PHIN | 0.0V | Yes | Non-uniform vertical doping effect on the surface potential |
| PSCBE1 | 4.24e8V/m | Yes | First substrate current induced body-effect parameter |
| PSCBE2 | 1.0e-5m/V | Yes | Second substrate current induced body-effect parameter |
| PVAG | 0.0 | Yes | Gate-bias dependence of Early voltage |
| U0 | 0.067m ² /(Vs) (NMOS); 0.025 m ² /(Vs) (PMOS) | Yes | Low-field mobility |
| UA | 1.0e-9m/V for MOBMOD=0 and 1; 1.0e-15m/V for MOBMOD=2 | Yes | Coefficient of the first-order mobility degradation due to the vertical field |
| UB | 1.0e-19m ² /V2 | Yes | Coefficient of the second-order mobility degradation due to the vertical field |

| Parameter | Default | Bin | Description |
|--------------|---|-----|---|
| UC | -0.0465V ⁻¹ for MOB-MOD=1; -0.0465e-9 m/V ² for MOBMOD=0 and 2 | Yes | Coefficient of the mobility degradation due to the body-bias effect |
| UD | 1e14(1/m ²) | Yes | Mobility coulomb scattering coefficient |
| UP | 0(1/m ²) | Yes | Mobility channel length coefficient |
| VBM | -3.0V | Yes | Maximum applied body bias in the VTH0 calculation |
| VFB | -1.0V | Yes | Flat-band voltage (PHIN) |
| VOFF | -0.08V | Yes | Offset voltage in subthreshold region for large W and L |
| VOFFL | 0.0mV | No | Channel-length dependence of VOFF |
| VSAT | 8.0e4m/s | Yes | Saturation velocity |
| VTH0 or VTHO | 0.7V (NMOS) -0.7V (PMOS) | Yes | Long-channel threshold voltage at V _{bs} =0 |
| W0 | 2.5e-6m | Yes | Narrow width parameter |
| WINT | 0.0m | No | Channel-width offset parameter |

Asymmetric and Bias-Dependent Rds Model Parameters:

| Parameter | Default | Bin | Description |
|-----------|-----------------|-----|---|
| PRWB | 0.0V-0.5 | Yes | Body-bias dependence of the LDD resistance |
| PRWG | 1.0V-1 | Yes | Gate-bias dependence of the LDD resistance |
| RDSW | 200.0 ohm(μm)WR | Yes | Zero bias LLD resistance per unit width for RDSMOD=0 |
| RDSWMIN | 0.0 ohm(μm)WR | No | LDD resistance per unit width at high V _{gs} and zero V _{bs} for RDSMOD=0 |
| RDW | 100.0 ohm(μm)WR | Yes | Zero bias lightly-doped drain resistance R _d (v) per unit width for RDSMOD=1 |
| RSW | 100.0 ohm(μm)WR | Yes | Zero bias lightly-doped source resistance R _s (V) per unit width for RDSMOD=1 |

Chapter 2: MOSFET Models

LEVEL 54: BSIM4 MOSFET Model

| Parameter | Default | Bin | Description |
|-----------|----------------------------|-----|--|
| RSPWMIN | 0.0 ohm(μm)WR | No | Lightly-doped source resistance per unit width at high V_{gs} and zero V_{bs} for RDSMOD=1 |
| WR | 1.0 | Yes | Channel-width dependence of the LDD resistance |
| NRS | 1.0 | No | Number of source diffusion squares |
| NRD | 1.0 | No | Number of drain diffusion squares |

Impact Ionization Current Model Parameters:

| Parameter | Default | Bin | Description |
|-----------|---------|-----|--|
| ALPHA0 | 0.0Am/V | Yes | First parameter of the impact ionization current |
| ALPHA1 | 0.0A/V | Yes | I _{sub} parameter for length scaling |
| BETA0 | 30.0V | Yes | Second parameter for the impact ionization current |

Gate-Induced Drain Leakage Model Parameters:

| Parameter | Default | Bin | Description |
|-----------|----------|-----|---|
| AGIDL | 0.0ohm | Yes | Pre-exponential coefficient for GIDL |
| AGISL | 0.0 | Yes | Pre-exponential coefficient for GISL |
| BGIDL | 2.3e9V/m | Yes | Exponential coefficient for GIDL |
| BGISL | 2.3e9V/m | Yes | Exponential coefficient for GISL |
| CGIDL | 0.5V3 | Yes | Parameter for the body-bias effect on GIDL |
| EGIDL | 0.8V | Yes | Fitting parameter for band bending for GIDL |
| EGISL | 0.8V | Yes | Fitting parameter for Band bending |

Gate Dielectric Tunneling Current Model Parameters:

| Parameter | Default | Bin | Description |
|-----------|-----------------------------------|-----|-------------------------------|
| AIGS | 1.36e-2(NMOS) and 9.8e-3(PMOS) | Yes | Parameter for I _{gs} |

| Parameter | Default | Bin | Description |
|-----------|--|-----|--|
| AIGBACC | $0.43 (F_s^2/g)^{0.5} m^{-1}$ | Yes | Parameter for I_{gb} in the accumulation |
| AIGBINV | $0.35 (F_s^2/g)^{0.5} m^{-1}$ | Yes | Parameter for I_{gb} in the inversion |
| AIGC | 0.054 (NMOS) and 0.31 (PMOS) $(F_s^2/g)^{0.5} m^{-1}$ | Yes | Parameter for I_{gcs} and I_{gcd} |
| AIGD | 1.36e-2(NMOS) and 9.8e-3(PMOS) | Yes | Parameter for I_{gd} |
| AIGSD | 0.43 (NMOS) and 0.31 (PMOS) $(F_s^2/g)^{0.5} m^{-1}$ | Yes | Parameter for I_{gs} and I_{gd} |
| BIGBACC | $0.054 (F_s^2/g)^{0.5} m^{-1} V^{-1}$ | Yes | Parameter for I_{gb} in the accumulation |
| BIGBINV | $0.03 (F_s^2/g)^{0.5} m^{-1} V^{-1}$ | Yes | Parameter for I_{gb} in the inversion |
| BIGC | 0.054 (NMOS) and 0.024 (PMOS) $(F_s^2/g)^{0.5} m^{-1} V^{-1}$ | Yes | Parameter for I_{gcs} and I_{gcd} |
| BIGD | 1.71e-3(NMOS) and 7.59e-4(PMOS) | Yes | Parameter for I_{gd} |
| BIGS | 1.71e-3(NMOS) and 7.59e-4(PMOS) | Yes | Parameter for I_{gs} |
| BIGSD | 0.054 (NMOS) 0.024 (PMOS) $(F_s^2/g)^{0.5} m^{-1} V^{-1}$ | Yes | Parameter for I_{gs} and I_{gd} |
| CIGBACC | $0.075 V^{-1}$ | Yes | Parameter for I_{gb} in the accumulation |
| CIGBINV | $0.0006 V^{-1}$ | Yes | Parameter for I_{gb} in the inversion |
| CIGC | 0.075 (NMOS) and 0.03(PMOS) V^{-1} | Yes | Parameter for I_{gcs} and I_{gcd} |
| CIGD | 0.075(NMOS) and 0.03(PMOS) | Yes | Parameter for I_{gd} |

Chapter 2: MOSFET Models
LEVEL 54: BSIM4 MOSFET Model

| Parameter | Default | Bin | Description |
|-----------|---------------------------------------|-----|---|
| CIGS | 0.075(NMOS) and 0.03(PMOS) | Yes | Parameter for I_{gs} |
| CIGSD | 0.075 (NMOS) and 0.03 (PMOS) V^{-1} | Yes | Parameter for I_{gs} and I_{gd} |
| DLCIG | LINT | Yes | Source/drain overlap length for I_{gs} and I_{gd} |
| EIGBINV | 1.1V | Yes | Parameter for I_{gb} in the inversion |
| NIGBACC | 1.0 | Yes | Parameter for I_{gb} in the accumulation |
| NIGBINV | 3.0 | Yes | Parameter for I_{gb} in the inversion |
| NIGC | 1.0 | Yes | Parameter for I_{gcs} , I_{gcd} , I_{gs} and I_{gd} |
| NTOX | 1.0 | Yes | Exponent for the gate oxide ratio |
| PIGCD | 1.0 | Yes | V_{ds} dependence of I_{gcs} and I_{gcd} |
| POXEDGE | 1.0 | Yes | Factor for the gate oxide thickness in the source/drain overlap regions |
| TOXREF | 3.0e-9m | No | Nominal gate oxide thickness for the gate dielectric tunneling current model only |
| VFBSDOFF | 0.0V | Yes | Flatband voltage offset parameter |

Charge/Capacitance Model Parameters:

| Parameter | Default | Bin | Description |
|-----------|------------------|-----|---|
| ACDE | 1.0m/V | Yes | Exponential coefficient for the charge thickness in CAPMOD=2 for the accumulation and depletion regions |
| CF | calculated (F/m) | Yes | Fringing field capacitance |
| CGBO | 0.0 (F/m) | No | Gate-bulk overlap capacitance per unit channel length |
| CGDL | 0.0F/m | Yes | Overlap capacitance between gate and lightly-doped source region |
| CGDO | calculated (F/m) | No | Non LDD region drain-gate overlap capacitance per unit channel width |

| Parameter | Default | Bin | Description |
|-----------|------------------|-----|---|
| CGSL | 0.0F/m | Yes | Overlap capacitance between the gate and the lightly-doped source region |
| CGSO | calculated (F/m) | No | Non LDD region source-gate overlap capacitance per unit channel width |
| CKAPPAD | CKAPPAS | Yes | Coefficient of bias-dependent overlap capacitance for the drain side |
| CKAPPAS | 0.6V | Yes | Coefficient of the bias-dependent overlap capacitance for the source side |
| CLC | 1.0e-7m | Yes | Constant term for the short channel model |
| CLE | 0.6 | Yes | Exponential term for the short channel model |
| DLC | LINT (m) | No | Channel-length offset parameter for the CV model |
| DWC | WINT (m) | No | Channel-width offset parameter for the CV model |
| MOIN | 15.0 | Yes | Coefficient for the gate-bias dependent surface potential |
| NOFF | 1.0 | Yes | CV parameter in $V_{gsteff,CV}$ for weak to strong inversion |
| VFBCV | -1.0V | Yes | Flat-band voltage parameter (for CAPMOD=0 only) |
| VOFFCV | 0.0V | Yes | CV parameter in $V_{gsteff,CV}$ for weak to strong inversion |
| XPART | 0.0 | No | Charge partition parameter |

High-Speed / RF Model Parameters:

| Parameter | Default | Bin | Description |
|-----------|------------|-----|--|
| GBMIN | 1.0e-12mho | No | Conductance in parallel with each of the five substrate resistances to avoid potential numerical instability due to an unreasonably large substrate resistance |
| RBDB | 50.0 ohm | No | Resistance between dbNode and dbNode |
| RBDBX0 | 100 ohms | No | Scaling pre-factor for RBDBX |
| RBDBY0 | 100 ohms | No | Scaling pre-factor for RBDBY |
| RBPB | 50.0 ohm | No | Resistance between bNodePrime and bNode |
| RBPBX0 | 100 ohms | No | Scaling pre-factor for RBPBX |

Chapter 2: MOSFET Models

LEVEL 54: BSIM4 MOSFET Model

| Parameter | Default | Bin | Description |
|-----------|----------|-----|---|
| RBPBXL | 0.0 | No | Length Scaling parameter for RBPBX |
| RBPBXNF | 0.0 | No | Number of fingers Scaling parameter for RBPBX |
| RBPBXW | 0.0 | No | Width Scaling parameter for RBPBX |
| RBPBY0 | 100 ohms | No | Scaling pre-factor for RBPBY |
| RBPBYL | 0.0 | No | Length Scaling parameter for RBPBY |
| RBPBYNF | 0.0 | No | Number of fingers Scaling parameter for RBPBY |
| RBPBYW | 0.0 | No | Width Scaling parameter for RBPBY |
| RBPD | 50.0 ohm | No | Resistance between bNodePrime and dbNode |
| RBPD0 | 50 ohms | No | Scaling pre-factor for RBPD |
| RBPDL | 0.0 | No | Length Scaling parameter for RBPD |
| RBPDNF | 0.0 | No | Number of fingers Scaling parameter for RBPD |
| RBPDW | 0.0 | No | Width Scaling parameter for RBPD |
| RBPS | 50.0 ohm | No | Resistance between bNodePrime and sbNode |
| RBPS0 | 50 ohms | No | Scaling pre-factor for RBPS |
| RBPSL | 0.0 | No | Length Scaling parameter for RBPS |
| RBPSNF | 0.0 | No | Number of fingers Scaling parameter for RBPS |
| RBPSW | 0.0 | No | Width Scaling parameter for RBPS |
| RBSB | 50.0 ohm | No | Resistance between sbNode and bNode |
| RBSBX0 | 100 ohms | No | Scaling pre-factor for RBSBX |
| RBSBY0 | 100 ohms | No | Scaling pre-factor for RBSBY |
| RBSDBXL | 0.0 | 0.0 | Length Scaling parameter for RBSBX and RBDBX |
| RBSDBXNF | 0.0 | No | Number of fingers Scaling parameter for RBSBX and RBDBX |
| RBSDBXW | 0.0 | No | Width Scaling parameter for RBSBX and RBDBX |
| RBSDBYL | 0.0 | No | Length Scaling parameter for RBSBY and RBDBY |

| Parameter | Default | Bin | Description |
|------------------|----------------|------------|--|
| RBSDBYNF | 0.0 | No | Number of fingers Scaling parameter for RBSBY and RBDBY |
| RBSDBYW | 0.0 | No | Width Scaling parameter for RBSBY and RBDBY |
| XRCRG1 | 12.0 | Yes | Parameter for the distributed channel-resistance effect for both intrinsic-input resistance and charge-deficit NQS models |
| XRCRG2 | 1.0 | Yes | Parameter to account for the excess channel diffusion resistance for both intrinsic input resistance and charge-deficit NQS models |

Flicker and Thermal Noise Model Parameters:

| Parameter | Default | Bin | Description |
|------------------|---|------------|---|
| AF | 1.0 | No | Flicker noise exponent |
| EF | 1.0 | No | Flicker noise frequency exponent |
| EM | 4.1e7V/m | No | Saturation field |
| KF | 0.0 A ^{2-EF} s ^{1-EF} | No | Flicker noise coefficient |
| NOIA | 6.25e41 (eV) ⁻¹ s ^{1-EF} m ⁻³ for NMOS; 6.188e40 (eV) ⁻¹ s ^{1-EF} m ⁻³ for PMOS | No | Flicker noise parameter A |
| NOIB | 3.125e26 (eV) ⁻¹ s ^{1-EF} m ⁻¹ for NMOS; 1.5e25 (eV) ⁻¹ s ^{1-EF} m ⁻¹ for PMOS | No | Flicker noise parameter B |
| NOIC | 8.75 (eV) ⁻¹ s ^{1-EF} m | No | Flicker noise parameter C |
| NTNOI | 1.0 | No | Noise factor for short-channel devices for TNOIMOD=0 only |
| TNOIA | 1.5 | No | Coefficient of the channel-length dependence of the total channel thermal noise |
| TNOIB | 3.5 | No | Channel-length dependence parameter for partitioning the channel thermal noise |

Layout-Dependent Parasitics Model Parameters:

| Parameter | Default | Bin | Description |
|-----------|------------------|-----|--|
| DMCG | 0.0m | No | Distance from the S/D contact center to the gate edge |
| DMCGT | 0.0m | No | DMCG of the test structures |
| DMCI | DMCG | No | Distance from the S/D contact center to the isolation edge in the channel-length direction |
| DMDG | 0.0m | No | Same as DMCG, but for merged devices only |
| DWJ | DWC (in CVmodel) | No | Offset of the S/D junction width |
| MIN | 0 | No | Minimize the number of drain or source diffusions for even-number fingered device |
| NF | 1 | No | Number of device figures |
| NGCON | 1 | No | Number of gate contacts |
| XGL | 0.0m | No | Offset of the gate length due to variations in patterning |
| XGW | 0.0m | No | Distance from the gate contact to the channel edge |

Asymmetric Source/Drain Junction Diode Model Parameters:

| Parameter | Default | Bin | Description |
|-----------|-----------------------------|-----|--|
| BVD | BVD=BVS | No | Breakdown voltage |
| BVS | BVS=10.0V | No | Breakdown voltage |
| CJD | CJD=CJS | No | Bottom junction capacitance per unit area at zero bias |
| CJS | CJS=5.0e-4 F/m ² | No | Bottom junction capacitance per unit area at zero bias |
| CJSWD | CJSWD=CJSWS | No | Isolation-edge sidewall junction capacitance per unit length |
| CJSWGD | CJSWGD=CJSWS | No | Gate-edge sidewall junction capacitance per unit length |
| CJSWGS | CJSWGS=CJSWS | No | Gate-edge sidewall junction capacitance per unit length |

| Parameter | Default | Bin | Description |
|------------------|----------------------------|------------|--|
| CJSWS | CJSWS=5.0e-10 F/m | No | Isolation-edge sidewall junction capacitance per unit length |
| IJTHDFWD | IJTHDFWD= IJTHSFWD | No | Limiting current in the forward bias region |
| IJTHDREV | IJTHDREV= IJTHSREV | No | Limiting current in the reverse bias region |
| IJTHSFWD | IJTHSFWD=0.1A | No | Limiting current in the forward bias region |
| IJTHSREV | IJTHSREV=0.1A | No | Limiting current in the reverse bias region |
| JSD | JSD=JSS | No | Bottom junction reverse saturation current density |
| JSS | JSS=1.0e-4A/m ² | No | Bottom junction reverse saturation current density |
| JSWD | JSWD=JSWS | No | Isolation-edge sidewall reverse saturation current density |
| JSWGD | JSWGD=JSWGS | No | Gate-edge sidewall reverse saturation current density |
| JSWGS | JSWGS=0.0A/m | No | Gate-edge sidewall reverse saturation current density |
| JSWS | JSWS=0.0A/m | No | Isolation-edge sidewall reverse saturation current density |
| MJD | MJD=MJS | No | Bottom junction capacitance grading coefficient |
| MJS | MJS=0.5 | No | Bottom junction capacitance grading coefficient |
| MJSWD | MJSWD=MJSWS | No | Isolation-edge sidewall junction capacitance grading coefficient |
| MJSWGD | MJSWGD=MJSWS | No | Gate-edge sidewall junction capacitance grading coefficient |
| MJSWGS | MJSWGS=MJSWS | No | Gate-edge sidewall junction capacitance grading coefficient |
| MJSWS | MJSWS=0.33 | No | Isolation-edge sidewall junction capacitance grading coefficient |
| PBD | PBD=PBS | No | Bottom junction built-in potential |
| PBS | PBS=1.0V | No | Bottom junction built-in potential |
| PBSWD | PBSWD=PBSWS | No | Isolation-edge sidewall junction built-in potential |

Chapter 2: MOSFET Models
LEVEL 54: BSIM4 MOSFET Model

| Parameter | Default | Bin | Description |
|-----------|--------------|-----|---|
| PBSWGD | PBSWGD=PBSWS | No | Gate-edge sidewall junction built-in potential |
| PBSWGS | PBSWGS=PBSWS | No | Gate-edge sidewall junction built-in potential |
| PBSWS | PBSWS=1.0V | No | Isolation-edge sidewall junction built-in potential |
| XJBVD | XJBVD=XJBVS | No | Fitting parameter for the diode breakdown |
| XJBVS | XJBVS=1.0 | No | Fitting parameter for the diode breakdown |

Temperature Dependence Parameters:

| Parameter | Default | Bin | Description |
|-----------|----------------------|-----|--|
| AT | 3.3e4m/s | Yes | Temperature coefficient for the saturation velocity |
| KT1 | -0.11V | Yes | Temperature coefficient for the threshold voltage |
| KT1L | 0.0Vm | Yes | Channel length dependence of the temperature coefficient for the threshold voltage |
| KT2 | 0.022 | Yes | Body-bias coefficient of the V_{th} temperature effect |
| NJS, NJD | NJS=1.0; NJD=NJS | No | Emission coefficients of junction for the source and drain junctions |
| PRT | 0.0ohm-m | Yes | Temperature coefficient for Rdsw |
| TCJ | 0.0K ⁻¹ | No | Temperature coefficient of CJ |
| TCJSW | 0.0K ⁻¹ | No | Temperature coefficient of CJSW |
| TCJSWG | 0.0K ⁻¹ | No | Temperature coefficient of CJSWG |
| TNOM | 27° X | No | Temperature at which simulation extracts parameters |
| TPB | 0.0V/K | No | Temperature coefficient of PB |
| TPBSW | 0.0V/K | No | Temperature coefficient of PBSW |
| TPBSWG | 0.0V/K | No | Temperature coefficient of PBSWG |
| TRD | 0.0 1K ⁻¹ | No | Temperature coefficient for the drain diffusion and the Rd contact resistances. |

| Parameter | Default | Bin | Description |
|-------------|--|-----|--|
| TRS | 0.0 1/K | No | Temperature coefficient for the source diffusion and the Rs contact resistances. |
| TVFBSDOFF | 0.0K ⁻¹ | Yes | Temperature coefficient of VFBSDOFF |
| TVOFF | 0.0K ⁻¹ | Yes | Temperature coefficient of VOFF |
| UA1 | 1.0e-9m/V | Yes | Temperature coefficient for UA |
| UB1 | -1.0e-18 (m/V ²) | Yes | Temperature coefficient for UB |
| UC1 | 0.056/V ⁻¹ for MOBMOD=1; 0.056e-9m/V ² for MOBMOD=0 and 2 | Yes | Temperature coefficient for UC |
| UD1 | 0.0(1/m) ² | Yes | Temperature coefficient for UD |
| UTE | -1.5 | Yes | Mobility temperature exponent |
| XTIS, XTIID | XTIS=3.0; XTID=XTIS | No | Junction current temperature exponents for the source and drain junctions |

Well Proximity Effect Parameters:

| Parameter | Default | Bin | Description |
|-----------|---------|-----|--|
| K2WE | 0.0 | Yes | K2 shift factor for well proximity effect |
| KU0WE | 0.0 | Yes | Mobility degradation factor for well proximity effect |
| KVTH0WE | 0.0 | Yes | Threshold shift factor for well proximity effect |
| SC | 0.0[m] | No | Distance to a single well edge |
| SCA | 0.0 | No | Integral of the first distribution function for scattered well dopant |
| SCB | 0.0 | No | Integral of the second distribution function for scattered well dopant |
| SCC | 0.0 | No | Integral of the third distribution function for scattered well dopant |
| SCREF | 1e-6[m] | No | Reference distance to calculate SCA, SCB, and SCC |
| WEB | 0.0 | No | Coefficient for SCB |
| WEC | 0.0 | No | Coefficient for SCC |

dW and dL Parameters:

| Parameter | Default | Bin | Description |
|-----------|-------------------|-----|--|
| LL | 0.0mLLN | No | Coefficient of the length dependence for the length offset |
| LLC | LL | No | Coefficient of the length dependence for the CV channel length offset |
| LLN | 1.0 | No | Power of the length dependence for the length offset |
| LW | 0.0mLWN | No | Coefficient of the width dependence for the length offset |
| LWC | LW | No | Coefficient of the width dependence for the CV channel length offset |
| LWL | 0.0 mLWN+LLN | No | Coefficient of the length and width cross term dependence for the length offset |
| LWLC | LWL | No | Coefficient of the length and width cross-term dependence for the CV channel length offset |
| LWN | 1.0 | No | Power of the width dependence, length offset |
| WL | 0.0 $\mu\Omega$ N | No | Coefficient of the length dependence of the width offset |
| WLC | WL | No | Coefficient of the length dependence for the CV channel width offset |
| WLN | 1.0 | No | Power of the length dependence of the width offset |
| WW | 0.0mWWN | No | Coefficient of the width dependence of the width offset |
| WWC | WW | No | Coefficient of the width dependence for the CV channel width offset |
| WWL | 0.0 mWWN+WLN | No | Coefficient of the length and width cross term dependence for the width offset |
| WWLC | WWL | No | Coefficient of the length and width cross-term dependence for the CV channel width offset |
| WWN | 1.0 | No | Power of the width dependence of the width offset |

Range Parameters for Model Application:

| Parameter | Default | Binnable | Description |
|-----------|-----------|----------|------------------------|
| LMIN | 0.0 μ | No | Minimum channel length |

| Parameter | Default | Binnable | Description |
|-----------|---------|----------|------------------------|
| LMAX | 1.0m | No | Maximum channel length |
| WMIN | 0.0m | No | Minimum channel width |
| WMAX | 1.0m | No | Maximum channel width |

BSIM4 MOSFET Model — Version Updates

This section covers the following topics:

- [BSIM4 Model Version 4.7 Updates](#)
- [BSIM4 Model Version 4.6.6 Updates](#)
- [BSIM4 Model Version 4.6.5 Updates](#)
- [BSIM4 Model Version 4.6.3 Updates](#)
- [BSIM4 Model Version 4.6.2 Updates](#)
- [BSIM4 Model Version 4.6.1 Updates](#)
- [BSIM4 Model Version 4.6 Updates](#)
- [BSIM4 Model Version 4.5 Updates](#)

BSIM4 Model Version 4.7 Updates

Compared with version 4.6.6, the following changes were made:

- Removed tnoiMod=2 in BSIM4.6.6, changing tnoiMod=3 in BSIM4.6.6 to tnoiMod=2 in BSIM4.7
- Implemented GF's DIBL/Rout model in mtrlMmod=0 as well (it was implemented in mtrlMod=1 only in BSIM4.6.6)
- Added compatibility mode between mtrlMod=0 and 1 (in this mode, mtrlMod=0 with k=3.9 is the same in IV and CV as mtrlMod=1)

BSIM4 Model Version 4.6.6 Updates

Compared with BSIM4.6.5, several new features were added.

- Enhancement of GIDL/GISL Model
 - GIDLMOD=1 is introduced to decouple Vd from Vg through new parameters RGIDL, KGIDL and FGIDL (same for GISL)
 - Binnable parameters RGIDL, KGIDL, FGIDL are introduced with new Mod selector, gidlMod=1

Chapter 2: MOSFET Models

LEVEL 54: BSIM4 MOSFET Model

- Enhancement of DIBL/Rout Model
 - Existing DIBL/Rout model in BSIMSOI is enhanced with an additional term, DVTP5, to better capture the Vds effect in long channel device.
 - The model is implemented with Binnable parameters DVTP2, DVTP3, DVTP4, and DVTP5.
- Temperature Dependence of Sub-threshold Leakage Current
 - Improved formulations to capture temperature dependence of Leakage Current
 - Enhanced temperature dependence model has been implemented with new Binnable parameters TNFACTOR, TETA0, TVOFFCV.
- Enhanced Thermal Noise Model for BSIM4
 - tnoiMod=2 is introduced
 1. Drain and gate noise follows tnoiMod=1
 2. A new expression is used for the correlation coefficient.
 - Introduced tnoiMod=3, with New expressions for drain noise (S_{id}), induced gate noise (S_{ig}) and correlation coefficient (c)
 - Frequency-dependent formula implemented for tnoiMod=2 and tnoiMod=3 ensures that the gate noise never exceeds the drain noise.
- Additional big fixes.

BSIM4 Model Version 4.6.5 Updates

In the prior version, source and drain diode current showed unphysical and high values for $Aseff=Pseff=Adeff=Pdeff=0$, although it correctly predicts positive values of $Aseff$, $Pseff$, $Adeff$, and $Pdeff$.

In version 4.6.5:

- If $Aseff$, $Pseff$, $Adeff$, $Pdeff$ are negative, their values are set to '0'.
- For $Aseff$ and $Pseff= 0$, the source side diode is turned off by setting SourceSaturationCurrent=0.0
- For $Adeff$ and $Pdeff= 0$, the drain side diode is turned off by setting DrainSaturationCurrent=0.0.

BSIM4 Model Version 4.6.3 Updates

The only change in BSIM4.6.3 compared with BSIM4.6.2 was the refinement of the calculation below.

```
pParam->BSIM4litl = sqrt(3.0 * 3.9 / epsrox * pParam->BSIM4xj
* tox)
```

BSIM4 Model Version 4.6.2 Updates

The v. 4.6.2 release added the following features and bug fixes:

- Mobility model (mobMod=3) added to enhance the modeling of Coulombic scattering in the high-k/metal gate transistors.
- Trap assisted tunneling (TAT) has been improved to include the width dependence. A new model parameter JTWEFF is introduced and set to zero to maintain the backward compatibility.
- Bug fixes include:
 - Output Conductance Model: VASCBE: A division by zero bug in the output conductance calculation is fixed.
 - Thermal Noise Model (tnoiMod=0): The scaling factor NF is added to the equivalent resistance Rds/NF.
 - Negative Thermal Noise (tnoiMod=1) The noise spectral density will not be negative now.
 - Source/Drain Bulk Junction Capacitance: The source/drain bulk junction capacitance will not be discontinuous when Vbs/Vbd is zero. The S/D junction sidewall capacitance along the isolation edge is set to zero if they are negative.
 - Derivative Issue in Capacitance Model (capMod=0): An error in the derivative calculation of dVgs_eff_dVg has been fixed.
 - Toxp Calculation (mtrlMod=1): The physical oxide thickness should be lay-out independent.
 - Source/Drain Resistance: A division by zero bug in the Rend calculation is fixed.
 - Typo of SC: SCA is a typo of SC in b4.c
 - Drain/Body Breakdown Voltage: The reset value of drain/body breakdown voltage will not cause non-convergence now. Some other similar bugs have also been fixed.

BSIM4 Model Version 4.6.1 Updates

Compared with BSIM4.6.0, several new features are added in this version.

- New material model is introduced for the predictive modeling of Non-SiO₂ insulator, Non-Poly Silicon gate and Non-silicon channel. The following new parameters are added:
 - MTRLMOD: New material model selector
 - PHIG, EPSRGATE: non-poly silicon gate parameters
 - EOT, VDDEOT: non-SiO₂ gate dielectric
 - EASUB, EPSRSUB, NI0SUB, BG0SUB, TBGASUB, TBGBSUB, ADOS, BDOS: Non-silicon channel parameters
- Mobility model (MOBMOD = 0 and MOBMOD = 1) has been improved through predictive modeling of vertical electric field. The improved mobility model is selected through MTRLMOD = 1 for backward compatibility.
- GIDL/GISL models are improved through an improved definition of flatband voltages at S/D ends. The improved GISL/GIDL model is selected through MTRLMOD = 1 for backward compatibility.
- The Poly-depletion model is modified to account for new gate and gate-insulator materials.
- C-V model has been improved by adding a new VgsteffCV definition through CVCHARGEMOD = 1. Six new parameters have been added: CVCHARGEMOD, MINVCV, LMINVCV, WMINCV, PMINVCV and VOFFCVL
- The following bugs have been fixed:
 - An error in the derivative calculation of dVdseffCV_dVb has been fixed for CAPMOD = 1 and CAPMOD = 2 in b4ld.c
 - The warning limits for NOFF and VOFFCV have been removed from b4check.c.

BSIM4 Model Version 4.6 Updates

The current HSPICE release supports BSIM version 4.6.0, including the following features:

- The IGISL and IGIDL modules have independent model parameters (as opposed to v. 4.5, in which the GIDL and GISL leakage current modules shared the parameter set).
- The parameters for the source and drain side junction diode current due to the trap-assisted tunneling current in space-change region are fully separated.
- The parameters for the gate tunneling current in the S/D overlap diffusion regions (I_{gs}/I_{gd}) are separated.

In addition three bug fixes are implemented in this version.

- The implementation of coulomb scattering in mobility model has been changed to avoid the non-monotonicity in drain current as a function of gate voltage. Also the default value of parameter has been changed to 0.
- The accuracy of $R_{gateMod} = 2$ has been improved by accounting correctly the contribution from R_{gate} to overall noise. The change has been made in b4noi.c
- The default value for the model parameter V_{FB} was missing. The default value of the parameter V_{FB} has been now set to -1.0V in b4set.c

BSIM4 Model Version 4.5 Updates

In July 2005, Berkeley released BSIM4 Version 4.5 includes the following features:

- The gate resistance parameters X_{GW} and N_{GCON} are now available as both model and instance parameters.
- Four modes are added or enhanced:
 - $RBODYMOD=2$: substrate resistance model that is scalable with channel length, channel width and number fingers
 - $IGCMOD=2$: implements full BSIM4 Vth model into IGC enables accurate predictions of IGC V_{bs} dependence
 - $TEMPMOD=2$: enhances TEMPMOD so $V_{th}(DITS)$ and gate tunneling models are functions of nominal temperature and adds the temperature dependence of zero-bias flat-band voltage
 - $WPEMOD=1$: adds a new well-proximity effect model developed by CMC.

Chapter 2: MOSFET Models

LEVEL 54: BSIM4 MOSFET Model

- Adds a new mobility model that accounts for Coulomb scattering effect as well as the channel length dependence of mobility due to heavy halo-doping.
- Adds additional temperature dependence of model parameters VOFF and VFBSDOFF.
- A fatal error message is issued when a model parameter VTSS, VTSD, VTSSWS, or VTSSWGD is negative. A warning message was issued previously.
- A warning message is issued if model parameter CGBO is negative. In which case, CGBO is set to 0.
- Fixed bugs in BSIM 4.4.

Note: BSIM4 Version 4.5 officially supports instance parameter DELVTO, which is used to represent threshold variations. This parameter has been supported in HSPICE since the 2002.12 version.

See also:

[.OPTION VER_CONTROL](#)
[.OPTION MODPARCHK](#)
[.OPTION PHD](#) for the PHD flow that can generally help large case HSPICE DC OP convergence for BSIM4 test cases.

Other Noise Sources Modeled in BSIM4 Model Version 4.5:

BSIM4 models the thermal noise due to the substrate, electrode gate, and source/drain resistances. Shot noise due to various gate tunneling components is modeled as well.

HSPICE can print out rg, rbps, rbpd, rpbp, rbsb, rbdb, igs, igd, igb noise information. You can add the following noise parameters to the model card.

| Output Parameters | turns on... |
|-------------------|------------------------------|
| + rgatemod=1 | the rg noise output |
| + rbodymod=1 | the rbps, rpbp noise output |
| + igbmod=1 | the igb noise output |
| + igcmod=1 | the igs and igd noise output |

| Output Parameters | turns on... |
|--|--------------------------------|
| + rbsbx0=1 rbsby0=1 rbdbx0=1 rbdby0=1 rbodymod=1 | the rbsb and rbdb noise output |

BSIM4 MOSFET Model — Output Templates

For a list of output template parameters in the MOSFET models, and which parameters this model supports, see [MOSFET Output Templates](#).

LEVEL 55: EPFL-EKV MOSFET Model

The EPFL-EKV MOSFET model is a scalable and compact simulation model built on fundamental physical properties of the MOS structure. This model is dedicated to the design and simulation of low-voltage, low-current analog, and mixed analog-digital circuits using submicron CMOS technologies.

- The intrinsic part of the MOSFET includes the equations and parameters used to simulate the EPFL-EKV MOSFET model.
- The extrinsic part of the MOSFET model includes series resistances of the source and drain diffusions, junction currents, and capacitances.

This section covers the following topics:

- [EPFL-EKV MOSFET Model — Single Equation Model](#)
- [EPFL-EKV MOSFET Model — Effects Modeled](#)
- [EPFL-EKV MOSFET Model — Coherence of Static and Dynamic Models](#)
- [EPFL-EKV MOSFET Model — Bulk Reference and Symmetry](#)
- [EPFL-EKV MOSFET Model — EKV Intrinsic Model Parameters](#)
- [EPFL-EKV MOSFET Model — Static Intrinsic Model Equations](#)
- [EPFL-EKV MOSFET Model — Quasi-static Model Equations](#)
- [EPFL-EKV MOSFET Model — Intrinsic Noise Model Equations](#)
- [EPFL-EKV MOSFET Model — Operating Point Information](#)
- [EPFL-EKV MOSFET Model — Estimation and Limits of Static Intrinsic Model Parameters](#)
- [EPFL-EKV MOSFET Model Updates](#)

EPFL-EKV MOSFET Model — Single Equation Model

The EPFL-EKV MOSFET model is a *single expression*, which preserves continuity of first-order and higher-order derivatives with respect to any terminal voltage in the entire range of validity of the model. This section describes the analytical expressions of first-order derivatives as transconductances and transcapacitances, you can use them in simulation.

EPFL-EKV MOSFET Model — Effects Modeled

The EPFL-EKV MOSFET model version 2.6 models the following physical effects:

- Basic geometrical and process-related aspects, such as oxide thickness, junction depth, and effective channel length and width.
- Effects of the doping profile.
- Substrate effect.
- Modeling of weak, moderate, and strong inversion behavior.
- Modeling of mobility effects due to vertical and lateral fields, and velocity saturation.
- Short-channel effects, such as channel-length modulation (CLM), source and drain charge-sharing (including for narrow channel widths), and the reverse short channel effect (RSCE).
- Modeling of the substrate current due to impact ionization.
- Quasi-static charge-based dynamic model.
- Thermal and flicker noise modeling.
- Short-distance geometry-dependent and bias-dependent device matching.

EPFL-EKV MOSFET Model — Coherence of Static and Dynamic Models

Simulation derives all aspects of the static, the quasi-static, and the non-quasi-static (NQS) dynamic and noise models, from the normalized transconductance-to-current ratio. These expressions use symmetric normalized forward and reverse currents.

- For quasi-static dynamic operations, you can use a charge-based model for the node charges and trans-capacitances or a simpler capacitances model.
- The dynamic model, including the time constant for the NQS model, is described in symmetrical terms of the forward and reverse normalized currents.

The charge formulation also expresses the effective mobility dependence of a local field.

EPFL-EKV MOSFET Model — Bulk Reference and Symmetry

Voltages are all referred to the local substrate:

$$V_G = V_{GB} \quad \text{Intrinsic gate-to-bulk voltage}$$

$$V_S = V_{SB} \quad \text{Intrinsic source-to-bulk voltage}$$

$$V_D = V_{DB} \quad \text{Intrinsic drain-to-bulk voltage}$$

V_S and V_D are the intrinsic source and drain voltages so the voltage drop over the extrinsic resistive elements must already be accounted for externally.

V_D is the electrical drain voltage, where $V_D > V_S$. Bulk reference handles the model symmetrically with respect to source and drain. This symmetry is inherent in common MOS technologies (excluding non-symmetric source-drain layouts).

Note: Intrinsic model equations are presented for an N-channel MOSFET. P-channel MOSFETs are dealt with as pseudo-N-channel. That is, simulation reverses the polarity of the voltages (V_G , V_S , V_D , V_{FB} , V_{TO} , and V_{CV}) before computing the P-channel current, which has a negative sign. No other distinctions are made between N-channel and P-channel, except the η factor for calculating the effective mobility.

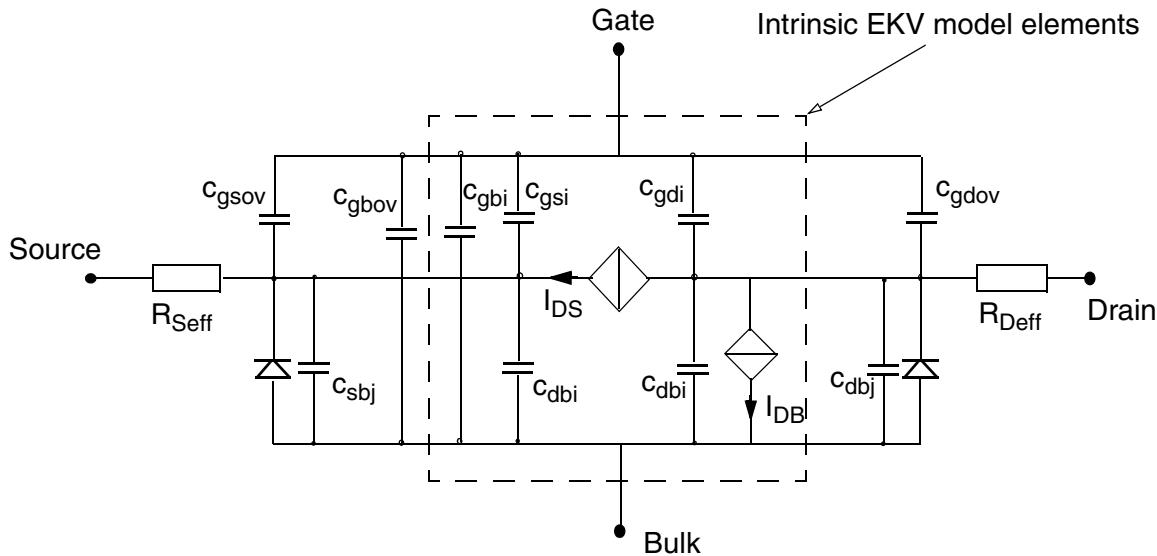


Figure 13 Level 55 Equivalent Circuit

The following table represents the intrinsic and extrinsic elements of the MOS transistor. For quasi-static dynamic operation, this figure shows only the intrinsic capacitances from the simpler capacitances model. However, you can also use a charge-based transcapacitances model in simulation.

| Name | Unit | Default | Description |
|---------|------|---------|---------------------------------|
| L | m | - | Channel length |
| W | m | - | Channel width |
| M or NP | - | 1.0 | Parallel multiple device number |
| N or NS | - | 1.0 | Series multiple device number |

EPFL-EKV MOSFET Model — EKV Intrinsic Model Parameters

| Name | Unit | Default | Range | Description |
|------------------|------------------|---------|-------|--------------------------------------|
| COX ¹ | F/m ² | 0.7e-3 | - | Gate oxide capacitance per unit area |

Chapter 2: MOSFET Models

LEVEL 55: EPFL-EKV MOSFET Model

| Name | Unit | Default | Range | Description |
|-----------------|------|---------|--------|---------------------------|
| DL | m | 0 | - | Channel length correction |
| DW ² | m | 0 | - | Channel width correction |
| XJ | m | 0.1e-6 | 1.0e-9 | Junction depth |

1. This model can calculate the default value of COX as a function of TOX.
2. DL and DW parameters are usually negative; see the effective length and width calculation.

| Name | Unit | Default ¹ | Range | Description |
|------------------|------------------|----------------------|------------|--------------------------------|
| E0 (EO) | V/m | 1.0e12 | $\geq 1E5$ | Mobility reduction coefficient |
| GAMMA | \sqrt{V} | 1.0 | ≥ 0 | Body effect parameter |
| KP | A/V ² | 50.0e-6 | - | Transconductance parameter |
| PHI | V | 0.7 | ≥ 0.1 | Bulk Fermi potential (*2) |
| UCRIT | V/m | 2.0e6 | $\geq 1E5$ | Longitudinal critical field |
| VTO ² | V | 0.5 | - | Long-channel threshold voltage |

1. This model can calculate the default values of VTO, GAMMA, PHI, and KP as a function of TOX, NSUB, UO, and VFB for statistical circuit simulation.
2. As VG, VTO also references the bulk.

| Name | Unit ¹ | Default | Range | Description |
|--------------------|-----------------------|---------|----------|--------------------------------|
| NSUB ² | cm ⁻³ | - | ≥ 0 | Channel doping |
| UO ³ | cm ² /(Vs) | - | ≥ 0 | Low-field mobility |
| THETA ⁴ | 1/V | 0 | ≥ 0 | Mobility reduction coefficient |
| TOX ⁵ | m | - | ≥ 0 | Oxide thickness |
| VFB ⁶ | V | - | - | Flat-band voltage |
| VMAX ⁷ | m/s | - | ≥ 0 | Saturation velocity |

1. In this example, cm is the basic unit for NSUB and UO. TOX and VMAX are in m .
2. Optional parameter for the dependence of GAMMA on COX, and for calculating PHI.
3. Optional parameter for the dependence of KP on COX.
4. Optional parameter for mobility reduction due to the vertical field.
5. Optional parameter for calculating COX.
6. Optional parameter for calculating VTO as a function of COX, GAMMA, or PHI.
7. Optional parameter for calculating UCRIT.

The preceding parameters accommodate the scaling behavior of the process and basic intrinsic model parameters, and statistical circuit simulation.

Simulation uses the TOX, NSUB, VFB, UO, and VMAX parameters only if you did not specify COX, GAMMA, PHI, VTO, KP, or UCRIT. You can also use a simpler mobility reduction model, due to the vertical field. Simulation uses the THETA mobility reduction coefficient only if you did not specify E0.

| Name | Unit | Default | Range | Description |
|--------|------|---------|----------|--|
| LAMBDA | - | 0.5 | ≥ 0 | Depletion length coefficient (channel length modulation) |
| LETA | - | 0.1 | - | Short-channel effect coefficient |
| WETA | - | 0.25 | - | Narrow-channel effect coefficient |

| Name | Unit | Default | Range | Description |
|---------|-----------------------|---------|---------------|--|
| LK | m | 0.29e-6 | $\geq 1.0e-8$ | Reverse short channel effect characteristic length |
| Q0 (QO) | A · s/ m ² | 0 | - | Reverse short channel effect peak charge density |

| Name | Unit | Default | Range | Description |
|------|------|---------|--------------|---|
| IBA | 1/m | 0 | - | First impact ionization coefficient |
| IBB | V/m | 3.0e8 | $\geq 1.0e8$ | Second impact ionization coefficient |
| IBN | - | 1.0 | ≥ 0.1 | Saturation voltage factor for impact ionization |

Chapter 2: MOSFET Models

LEVEL 55: EPFL-EKV MOSFET Model

| Name | Unit | Default | Description |
|------|------|---------|--|
| BEX | - | -1.5 | Mobility temperature exponent |
| IBBT | 1/K | 9.0e-4 | Temperature coefficient for IBB |
| TCV | V/K | 1.0e-3 | Threshold voltage temperature coefficient |
| UCEX | - | 0.8 | Longitudinal critical field temperature exponent |

| Name | Unit | Default | Description |
|--------|-------------|---------|---|
| AGAMMA | \sqrt{Vm} | 0 | Area related body effect mismatch parameter |
| AKP | m | 0 | Area related gain mismatch parameter |
| AVTO | Vm | 0^1 | Area related threshold voltage mismatch parameter |

1. Only DEV values apply to the statistical matching parameters (AVTO, AGAMMA, AKP) for Monte-Carlo type simulations. Default is 1E-6 for all three parameters in some implementations to allow sensitivity analysis of the matching parameters. Do not specify LOT for AVTO, AGAMMA, or AKP.

| Name | Unit | Default | Description |
|------|-------|---------|---------------------------|
| AF | - | 1 | Flicker noise exponent |
| KF | $^-1$ | 0 | Flicker noise coefficient |

1. The unit for KF might depend on the flicker noise model that you select, if these options are available.

| Name | Unit | Default | Description |
|---------------------|------|---------|--|
| NQS ¹ | - | 0 | Non-Quasi-Static (NQS) operation switch |
| XQC ² | - | 0.4 | Charge/capacitance model selector |
| SATLIM ³ | - | exp(4) | Ratio defining the i_f/i_s saturation limit. |

1. NQS=1 switches Non-Quasi-Static operation on, default is off (the NQS model option might not be available in all implementations).

2. Selects either the charges/transcapacitances (default) or the capacitances-only model. $XQC=0.4$: charges/transcapacitances model; $XQC=1$: capacitances only model. (the XQC model option might not be available in all implementations).
3. Only used for operating point information. (the SATLIM option might not be available in all implementations).

EPFL-EKV MOSFET Model — Static Intrinsic Model Equations

This section covers the following topics:

- EPFL-EKV MOSFET Model — Basic Definitions
- EPFL-EKV MOSFET Model — Parameter Preprocessing: Handling of Model Parameters for P-Channel MOSFETs
- EPFL-EKV MOSFET Model — Parameter Preprocessing: Initializing Intrinsic Parameters
- EPFL-EKV MOSFET Model — Parameter Preprocessing: Default Values and Parameter Ranges
- EPFL-EKV MOSFET Model — Parameter Preprocessing: Intrinsic Parameters Temperature Dependence
- EPFL-EKV MOSFET Model — Bulk Referenced Intrinsic Voltages
- EPFL-EKV MOSFET Model — Effective Channel Length and Width
- EPFL-EKV MOSFET Model — Short Distance Matching
- EPFL-EKV MOSFET Model — Reverse Short-channel Effect (RSCE)
- EPFL-EKV MOSFET Model — Effective Gate Voltage Including RSCE
- EPFL-EKV MOSFET Model — Effective substrate factor including charge-sharing for short and narrow channels
- EPFL-EKV MOSFET Model — Pinch-off Voltage Including Short-Channel and Narrow-Channel Effects
- EPFL-EKV MOSFET Model — Slope Factor
- EPFL-EKV MOSFET Model — Large Signal Interpolation Function
- EPFL-EKV MOSFET Model — Forward Normalized Current
- EPFL-EKV MOSFET Model — Velocity Saturation Voltage

Chapter 2: MOSFET Models

LEVEL 55: EPFL-EKV MOSFET Model

- EPFL-EKV MOSFET Model — Drain-to-source Saturation Voltage for Reverse Normalized Current
- EPFL-EKV MOSFET Model — Channel-length Modulation
- EPFL-EKV MOSFET Model — Equivalent Channel Length Including Channel-length Modulation and Velocity Saturation
- EPFL-EKV MOSFET Model — Reverse Normalized Current
- EPFL-EKV MOSFET Model — Transconductance Factor and Mobility Reduction Due to Vertical Field
- EPFL-EKV MOSFET Model — Simple Mobility Reduction Model
- EPFL-EKV MOSFET Model — Specific Current
- EPFL-EKV MOSFET Model — Drain-to-source Current
- EPFL-EKV MOSFET Model — Transconductances
- EPFL-EKV MOSFET Model — Impact Ionization Current

EPFL-EKV MOSFET Model — Basic Definitions

$$\epsilon_{si} = SCALE \cdot 1.045 \times 10^{-12} [F/m] \quad \text{Permittivity of silicon}$$

$$\epsilon_{ox} = SCALE \cdot 34.5 \times 10^{-12} [F/m] \quad \text{Permittivity of silicon dioxide}$$

$$q = 1.602 \times 10^{-19} [C] \quad \text{Magnitude of electron charge}$$

$$k = 1.3807 \times 10^{-23} [JK^{-1}] \quad \text{Boltzmann constant}$$

$$T_{ref} = 300.15 [K] \quad \text{Reference temperature}$$

$$T_{nom} [K] \quad \text{Nominal temperature of model parameters}$$

$$T [K] \quad \text{Model simulation temperature}$$

$$V_t(T) = \frac{k \cdot T}{q} \quad \text{Thermal voltage}$$

$$E_g(T) = \left(1.16 - 0.000702 \cdot \frac{T^2}{T + 1108} \right) [eV] \quad \text{Energy gap}$$

$$n_i(T) = 1.45 \times 10^{16} \cdot \left(\frac{T}{T_{ref}} \right) \cdot \exp \left(\frac{E_g(T_{ref})}{2 \cdot V_t(T_{ref})} - \frac{E_g(T)}{2 \cdot V_t(T)} \right) [m^{-3}] \quad \text{Intrinsic carrier concentration}$$

EPFL-EKV MOSFET Model — Parameter Preprocessing: Handling of Model Parameters for P-Channel MOSFETs

For P-channel devices, simulation reverses the sign of VFB, VTO, and TCV before processing. Therefore, VTO and TCV are usually positive and VFB is usually negative for N-channel, and vice versa for P-channel MOSFETs.

EPFL-EKV MOSFET Model — Parameter Preprocessing: Initializing Intrinsic Parameters

The basic intrinsic model parameters are related to the fundamental process parameters as in early SPICE models:

COX → TOX
 GAMMA and PHI → NSUB
 VTO → VFB
 KP → JO
 UCRIT → XMAX

For statistical circuit simulation, you should introduce parameter variations on the level of the latter parameters. You can also use these dependencies to analyze device scaling and to obtain parameter sets from other MOSFET models. Therefore, you can use the following relations:

If you do not specify COX, simulation initializes it as:

$$COX = \begin{cases} \varepsilon_{ox} / TOX & \text{for: } TOX > 0 \\ \text{default} & \text{otherwise} \end{cases}$$

If you do not specify GAMMA, simulation initializes it as:

$$GAMMA = \begin{cases} \frac{\sqrt{2q\varepsilon_{si} \cdot (NSUB \cdot 10^6)}}{COX} & \text{for: } NSUB > 0 \\ \text{default} & \text{otherwise} \end{cases}$$

If you do not specify PHI, simulation initializes it as:

$$PHI = \begin{cases} 2V_t(T_{nom}) \cdot \ln\left(\frac{NSUB \cdot 10^6}{n_i(T_{nom})}\right) & \text{for: } NSUB > 0 \\ \text{default} & \text{otherwise} \end{cases}$$

If you do not specify VTO, simulation initializes it as:

Chapter 2: MOSFET Models

LEVEL 55: EPFL-EKV MOSFET Model

$$VTO = \begin{cases} VFB + PHI + GAMMA \cdot \sqrt{PHI} & \text{if you specify VFB} \\ default & \text{otherwise} \end{cases}$$

If you do not specify `DP`, simulation initializes it as:

$$KP = \begin{cases} (UO \cdot 10^{-4}) \cdot COX & \text{for: } UO > 0 \\ default & \text{otherwise} \end{cases}$$

If you do not specify `UCRIT`, simulation initializes it as:

$$UCRIT = \begin{cases} VMAX / (UO \cdot 10^{-4}) & \text{for: } VMAX > 0, UO > 0 \\ default & \text{otherwise} \end{cases}$$

If you do not specify `E0`, simulation uses a simplified mobility model with the `THETA` parameter:

$$E0 = \begin{cases} 0 & \text{if you specify THETA} \\ default & \text{otherwise} \end{cases}$$

Note: The `E0` value is zero, indicating to use the simplified mobility model is used in conjunction with `THETA`, instead of the standard mobility model.

Optional parameters might not be available in all implementations.

EPFL-EKV MOSFET Model — Parameter Preprocessing: Default Values and Parameter Ranges

If you do not define a specific model parameters, simulation either initializes it according to the above relations, or sets it to its default value. Certain parameters restrict their numerical range to avoid numerical problems, such as divisions by zero. If you specify a parameter value outside the specified range (see the range column in the parameter tables), then simulation sets its value to the closest acceptable value.

EPFL-EKV MOSFET Model — Parameter Preprocessing: Intrinsic Parameters Temperature Dependence

$$VTO(T) = VTO - TCV \cdot (T - T_{nom})$$

$$KP(T) = KP \cdot \left(\frac{T}{T_{nom}} \right)^{BEX}$$

$$UCRIT(T) = UCRIT \cdot \left(\frac{T}{T_{nom}}\right)^{UCEX}$$

$$PHI(T) = PHI \cdot \frac{T}{T_{nom}} - 3 \cdot V_t \cdot \ln\left(\frac{T}{T_{nom}}\right) - E_g(T_{nom}) \cdot \frac{T}{T_{nom}} + E_g(T)$$

$$IBB(T) = IBB \cdot [1.0 + IBBT \cdot (T - T_{nom})]$$

EPFL-EKV MOSFET Model — Bulk Referenced Intrinsic Voltages

Simulation refers all voltages to the local substrate (see [EPFL-EKV MOSFET Model — Bulk Reference and Symmetry](#)):

$$V_G = V_{GB} = V_{GS} - V_{BS} \quad \text{Intrinsic gate-to-bulk voltage}$$

$$V_S = V_{SB} = -V_{BS} \quad \text{Intrinsic source-to-bulk voltage}$$

$$V_D = V_{DB} = V_{DS} - V_{BS} \quad \text{Intrinsic drain-to-bulk voltage}$$

For P-channel devices, simulation inverts all signs before processing.

EPFL-EKV MOSFET Model — Effective Channel Length and Width

$$W_{eff} = W + DW$$

$$L_{eff} = L + DL$$

Note: Unlike the convention in other MOSFET models, DL and DW usually permit a negative value due to the above definition.

EPFL-EKV MOSFET Model — Short Distance Matching

The inverse of the square root of the transistor area usually suitably describes a random mismatch between two transistors with an identical layout and close to each other. The following relationships have been adopted:

$$VTO_a = VTO + \frac{AVTO}{\sqrt{NP \cdot W_{eff} \cdot NS \cdot L_{eff}}}$$

$$KP_a = KP \cdot \left(1 + \frac{AKP}{\sqrt{NP \cdot W_{eff} \cdot NS \cdot L_{eff}}}\right)$$

$$GAMMA_a = GAMMA + \frac{AGAMMA}{\sqrt{NP \cdot W_{eff} \cdot NS \cdot L_{eff}}}$$

Chapter 2: MOSFET Models

LEVEL 55: EPFL-EKV MOSFET Model

These model equations apply only in Monte-Carlo and sensitivity simulations. Because negative values for both KP_a and $GAMMA_a$ are not physically meaningful, simulation clips them at zero.

EPFL-EKV MOSFET Model — Reverse Short-channel Effect (RSCE)

$$C_\varepsilon = 4 \cdot (22 \times 10^{-3})^2 \quad C_A = 0.028$$

$$\xi = C_A \cdot \left(10 \cdot \frac{L_{eff}}{LK} - 1 \right)$$

$$\Delta V_{RSCE} = \frac{2 \cdot Q0}{COX} \cdot \frac{1}{\left[1 + \frac{1}{2} \cdot (\xi + \sqrt{\xi^2 + C_\varepsilon}) \right]^2}$$

EPFL-EKV MOSFET Model — Effective Gate Voltage Including RSCE

$$V'_G = V_G - VTO_a - \Delta V_{RSCE} + PHI + GAMMA_a \sqrt{PHI}$$

EPFL-EKV MOSFET Model — Effective substrate factor including charge-sharing for short and narrow channels

Pinch-off voltage for narrow-channel effect:

$$V_{P0} = \begin{cases} V'_G - PHI - GAMMA_a \left(\sqrt{V'_G + \left(\frac{GAMMA_a}{2} \right)^2} - \frac{GAMMA_a}{2} \right) & \text{for: } V'_G > 0 \\ -PHI & \text{for: } V'_G \leq 0 \end{cases}$$

Effective substrate factor accounting for charge-sharing:

$$V'_{S(D)} = \frac{1}{2} \cdot [V_{S(D)} + PHI + \sqrt{(V_{S(D)} + PHI)^2 + (4V_t)^2}]$$

Note: This equation prevents a negative value in the square roots argument in the subsequent code.

$$\gamma^\circ = GAMMA_a - \frac{\varepsilon_{si}}{COX} \cdot \left[\frac{LETA}{L_{eff}} \cdot (\sqrt{V'_S} + \sqrt{V'_D}) - \frac{3 \cdot WETA}{W_{eff}} \cdot \sqrt{V_{P0} + PHI} \right]$$

$$\gamma' = \frac{1}{2} \cdot (\gamma^\circ + \sqrt{\gamma^\circ^2 + 0.1 \cdot V_t})$$

Note: This equation prevents the effective substrate factor from becoming negative.

EPFL-EKV MOSFET Model — Pinch-off Voltage Including Short-Channel and Narrow-Channel Effects

$$V_P = \begin{cases} V_G' - PHI - \gamma' \cdot \left(\sqrt{V_G' + \left(\frac{\gamma'}{2} \right)^2} - \frac{\gamma'}{2} \right) & \text{for: } V_G' > 0 \\ -PHI & \text{for: } V_G' \leq 0 \end{cases}$$

Note: The pinch-off voltage accounts for channel doping effects, such as the threshold voltage and the substrate effect.

For long-channel devices, V_p is a function of gate voltage; for short-channel devices, it also becomes a function of the source and drain voltage due to the charge-sharing effect.

EPFL-EKV MOSFET Model — Slope Factor

$$n = 1 + \frac{GAMMA_a}{2 \cdot \sqrt{V_P + PHI + 4V_t}}$$

Note: The slope factor (or body effect factor) is primarily a function of the gate voltage, and links to the weak inversion slope.

EPFL-EKV MOSFET Model — Large Signal Interpolation Function

$F(v)$ is the large-signal interpolation function, relating normalized currents to normalized voltages. A simple and accurate expression for the transconductance-to-current ratio consistently formulates:

- The static large-signal interpolation function.
- The dynamic model for the intrinsic charges (and capacitances).
- The intrinsic time constant and the thermal noise model for the whole range of current, from weak to strong inversion.

$$\frac{g_{ms} \cdot V_t}{I_{DS}} = \frac{1}{\sqrt{0.25 + i} + 0.5}$$

Large-signal interpolation function:

$$y = \sqrt{0.25 + i} - 0.5$$

$$v = 2y + \ln(y)$$

You cannot analytically invert this equation. However, you can use a Newton-Raphson iterative scheme to invert this equation. Currently, this model uses a simplified algorithm that avoids iteration, leading to a continuous expression for the large signal interpolation function.

The (inverted) large signal interpolation function has the following asymptotes in strong and weak inversion:

$$F(v) = \begin{cases} (v/2)^2 & \text{for: } v \gg 0 \\ \exp(v) & \text{for: } v \ll 0 \end{cases}$$

EPFL-EKV MOSFET Model — Forward Normalized Current

$$i_f = F\left[\frac{V_P - V_S}{V_t}\right]$$

EPFL-EKV MOSFET Model — Velocity Saturation Voltage

$$V_C = UCRIT \cdot NS \cdot L_{eff}$$

Note: This equation accounts for the NS multiple series device number:

$$V_{DSS} = V_C \cdot \left[\sqrt{\frac{1}{4} + \frac{V_t}{V_C} \cdot \sqrt{i_f}} - \frac{1}{2} \right]$$

Note: The V_{DSS} variable is half the value of the actual saturation voltage.

EPFL-EKV MOSFET Model — Drain-to-source Saturation Voltage for Reverse Normalized Current

$$V_{DSS}' = V_C \cdot \left[\sqrt{\frac{1}{4} + \frac{V_t}{V_C} \cdot \left(\sqrt{i_f} - \frac{3}{4} \cdot \ln(i_f) \right)} - \frac{1}{2} \right] + V_t \cdot \left[\ln\left(\frac{V_C}{2V_t}\right) - 0.6 \right]$$

EPFL-EKV MOSFET Model — Channel-length Modulation

$$\Delta V = 4 \cdot V_t \cdot \sqrt{LAMBDA \cdot \left(\sqrt{i_f} - \frac{V_{DSS}}{V_t} \right) + \frac{1}{64}}$$

$$V_{ds} = \frac{V_D - V_S}{2}$$

$$V_{ip} = \sqrt{V_{DSS}^2 + \Delta V^2} - \sqrt{(V_{ds} - V_{DSS})^2 + \Delta V^2}$$

$$L_C = \sqrt{\frac{\epsilon_{si}}{COX} \cdot XJ}$$

$$\Delta L = LAMBDA \cdot L_C \cdot \ln\left(1 + \frac{V_{ds} - V_{ip}}{L_C \cdot UCRIT}\right)$$

EPFL-EKV MOSFET Model — Equivalent Channel Length Including Channel-length Modulation and Velocity Saturation

$$L' = NS \cdot L_{eff} - \Delta L + \frac{V_{ds} + V_{ip}}{UCRIT}$$

$$L_{min} = NS \cdot L_{eff} / 10$$

Note: These equations also account for the NS multiple series device number.

$$L_{eq} = \frac{1}{2} \cdot (L' + \sqrt{L'^2 + L_{min}^2})$$

Note: This equation prevents the equivalent channel length from becoming zero or negative.

EPFL-EKV MOSFET Model — Reverse Normalized Current

Reverse normalized current:

$$i_r' = F \left[\frac{V_P - V_{ds} - V_S - \sqrt{V_{DSS}'^2 + \Delta V^2} + \sqrt{(V_{ds} - V_{DSS}')^2 + \Delta V^2}}{V_t} \right]$$

Reverse normalized current for the mobility model, intrinsic charges/capacitances, the thermal noise model, and the NQS time-constant:

$$i_r = F \left[\frac{V_P - V_D}{V_t} \right]$$

EPFL-EKV MOSFET Model — Transconductance Factor and Mobility Reduction Due to Vertical Field

$$\beta_0 = KP_a \cdot \frac{NP \cdot W_{eff}}{L_{eq}}$$

Chapter 2: MOSFET Models

LEVEL 55: EPFL-EKV MOSFET Model

Note: The NP (or M) device parameter returns accurate results for simulating parallel devices. Using NS (or N) for series devices is only approximate.

L_{eq} accounts for multiple NS series device numbers.

$$\eta = \begin{cases} 1/2 & \text{for NMOS} \\ 1/3 & \text{for PMOS} \end{cases}$$

$$q_{B0} = GAMMA_a \cdot \sqrt{PHI}$$

$$\beta_0' = \beta_0 \cdot \left(1 + \frac{COX}{E0 \cdot \epsilon_{si}} \cdot q_{B0} \right)$$

$$\beta = \frac{\beta_0'}{1 + \frac{COX}{E0 \cdot \epsilon_{si}} \cdot V_t \cdot |q_B + \eta \cdot q_I|}$$

For the definition of the q_B normalized depletion and the q_I inversion charges refer to the [EPFL-EKV Model — Quasi-static Model: Dynamic Model for the Intrinsic Node Charges - Normalized Intrinsic Node Charges](#). Use β_0' to ensure that

$$\beta \approx \beta_0$$

when

$$q_I \ll q_B$$

. The formulation of β arises from the integration of the local effective field as a function of depletion and inversion charge densities along the channel. You do not need to specify the substrate bias dependency, because the model includes the depletion charge.

Note: The resulting mobility expression also depends on V_{DS} .

EPFL-EKV MOSFET Model — Simple Mobility Reduction Model

For compatibility with the former EKV model versions (before v2.6), you can choose the simpler mobility reduction model, which uses the THETA parameter.

If you do *not* specify the E0 model parameter (see [EPFL-EKV MOSFET Model — Static Intrinsic Model Equations](#)), simulation uses the simpler mobility model:

$$V'_P = \frac{1}{2} \cdot (V_P + \sqrt{V_P^2 + 2V_t^2})$$

$$\beta = \frac{\beta_0}{1 + THETA \cdot V'_P}$$

EPFL-EKV MOSFET Model — Specific Current

$$I_S = 2 \cdot n \cdot \beta \cdot V_t^2$$

EPFL-EKV MOSFET Model — Drain-to-source Current

$$I_{DS} = I_S \cdot (i_f - i'_r)$$

For P-channel devices, I_{DS} has a negative sign.

This drain current expression is a single equation, valid in all operating regions:

- weak, moderate and strong inversion
- non-saturation
- saturation

This current is therefore not only continuous among all of these regions, but also continuously derivable.

EPFL-EKV MOSFET Model — Transconductances

Simulation derives the transconductances from the drain current:

$$g_{mg} \equiv \frac{\partial I_{DS}}{\partial V_G} \quad g_{ms} \equiv -\frac{\partial I_{DS}}{\partial V_S} \quad g_{md} \equiv \frac{\partial I_{DS}}{\partial V_{DS}}$$

In the following relationships, the source for the derivatives is a reference:

$$g_m \equiv \frac{\partial I_{DS}}{\partial V_{GS}} = g_{mg} \quad g_{mbs} \equiv \frac{\partial I_{DS}}{\partial V_{BS}} = g_{ms} - g_{mg} - g_{md} \quad g_{ds} \equiv \frac{\partial I_{DS}}{\partial V_{DS}} = g_{md}$$

This model includes the analytic derivatives.

EPFL-EKV MOSFET Model — Impact Ionization Current

$$V_{ib} = V_D - V_S - IBN \cdot 2 \cdot V_{DSS}$$

$$I_{DB} = \begin{cases} I_{DS} \cdot \frac{IBA}{IBB} \cdot V_{ib} \cdot \exp\left(\frac{-IBB \cdot L_C}{V_{ib}}\right) & \text{for: } V_{ib} > 0 \\ 0 & \text{for: } V_{ib} \leq 0 \end{cases}$$

Note: The factor 2 in the v_{ib} expression accounts for the fact that the numerical value of V_{DSS} is half of the actual saturation voltage. The substrate current is a component of the total extrinsic drain current, flowing from the drain to the bulk. This model therefore expresses the total drain current as

$$I_D = I_{DS} + I_{DB}$$

Note: The substrate current therefore also affects the total extrinsic conductances, especially the drain conductance.

EPFL-EKV MOSFET Model — Quasi-static Model Equations

MOSFET Level 55 includes both a charge-based model for transcapacitances, allowing charge-conservation during transient analysis, you can select a simpler capacitances-based model instead.

Note: The charges model is symmetrical in terms of the forward and reverse normalized currents—that is, the model is symmetrical for both the drain and source sides.

The pinch-off voltage in the dynamic model provides the short-channel effects (such as charge-sharing and reverse short-channel effects).

This section covers the following topics:

- [EPFL-EKV Model — Quasi-static Model: Dynamic Model for the Intrinsic Node Charges](#)
- [EPFL-EKV Model — Quasi-static Model: Dynamic Model for the Intrinsic Node Charges - Normalized Intrinsic Node Charges](#)
- [EPFL-EKV Model — Quasi-static Model: Dynamic Model for the Intrinsic Node Charges - Total Charges](#)
- [EPFL-EKV Model — Quasi-static Model: Intrinsic Capacitances - Transcapacitances](#)
- [EPFL-EKV Model — Quasi-static Model: Intrinsic Capacitances - Normalized Intrinsic Capacitances](#)
- [EPFL-EKV Model — Quasi-static Model: Intrinsic Capacitances - Total Intrinsic Capacitances](#)

EPFL-EKV Model — Quasi-static Model: Dynamic Model for the Intrinsic Node Charges

$$n_q = 1 + \frac{GAMMA_a}{2 \cdot \sqrt{V_p + PHI + 10^{-6}}}$$

EPFL-EKV Model — Quasi-static Model: Dynamic Model for the Intrinsic Node Charges - Normalized Intrinsic Node Charges

$$x_f = \sqrt{\frac{1}{4} + i_f}$$

$$x_r = \sqrt{\frac{1}{4} + i_r}$$

$$q_D = -n_q \cdot \left(\frac{4}{15} \cdot \frac{3x_r^3 + 6x_r^2 x_f + 4x_r x_f^2 + 2x_f^3}{(x_f + x_r)^2} - \frac{1}{2} \right)$$

$$q_S = -n_q \cdot \left(\frac{4}{15} \cdot \frac{3x_f^3 + 6x_f^2 x_r + 4x_f x_r^2 + 2x_r^3}{(x_f + x_r)^2} - \frac{1}{2} \right)$$

$$q_I = q_S + q_D = -n_q \cdot \left(\frac{4}{3} \cdot \frac{x_f^2 + x_f x_r + x_r^2}{x_f + x_r} - 1 \right)$$

$$q_B = \begin{cases} (-GAMMA_a \cdot \sqrt{V_p + PHI + 10^{-6}}) \cdot \frac{1}{V_t} - \left(\frac{n_q - 1}{n_q} \right) \cdot q_I & \text{for: } V'_G > 0 \\ -V'_G \cdot \frac{1}{V_t} & \text{for: } V'_G \leq 0 \end{cases}$$

$$q_G = -q_I - q_{OX} - q_B$$

q_{OX} is a fixed oxide charge, which simulation assumes is zero. The preceding equations express the charge conservation among the four nodes of the transistor.

EPFL-EKV Model — Quasi-static Model: Dynamic Model for the Intrinsic Node Charges - Total Charges

$$C_{ox} = COX \cdot NP \cdot W_{eff} \cdot NS \cdot L_{eff}$$

Chapter 2: MOSFET Models

LEVEL 55: EPFL-EKV MOSFET Model

$$Q_{(I, B, D, S, G)} = C_{ox} \cdot V_t \cdot q_{(I, B, D, S, G)}$$

EPFL-EKV Model — Quasi-static Model: Intrinsic Capacitances - Transcapacitances

Simulation derives the intrinsic capacitances from the node charges for the terminal voltages:

$$C_{xy} = \pm \frac{\partial}{\partial V_y} (Q_x) \quad x, y = G, D, S, B$$

The preceding equation uses the positive sign if $x=y$ or the negative sign otherwise. This equation produces simple, continuous analytical expressions for all transcapacitances in terms of the x_f pinch-off voltage, the x_r slope factor, and derivatives thereof, from weak to strong inversion, and from non-saturation to saturation.

EPFL-EKV Model — Quasi-static Model: Intrinsic Capacitances - Normalized Intrinsic Capacitances

Set $XQC=1$ to select a simplified capacitive dynamic model that uses the five intrinsic capacitances corresponding to the [Level 55 Equivalent Circuit](#). This model ignores the slight bias dependence of the n slope factor. The result is the following simple set of functions:

$$c_{gs} = \frac{2}{3} \cdot \left(1 - \frac{x_r^2 + x_r + \frac{1}{2}x_f}{(x_f + x_r)^2} \right)$$

$$c_{gd} = \frac{2}{3} \cdot \left(1 - \frac{x_f^2 + x_f + \frac{1}{2}x_r}{(x_f + x_r)^2} \right)$$

$$c_{gb} = \left(\frac{n_q - 1}{n_q} \right) \cdot (1 - c_{gs} - c_{gd})$$

$$c_{sb} = (n_q - 1) \cdot c_{gs}$$

$$c_{db} = (n_q - 1) \cdot c_{gd}$$

EPFL-EKV Model — Quasi-static Model: Intrinsic Capacitances - Total Intrinsic Capacitances

$$C_{(gs, gd, gb, sb, db)} = C_{ox} \cdot c_{(gs, gd, gb, sb, db)}$$

EPFL-EKV MOSFET Model — Intrinsic Noise Model Equations

The I_{NDS} current source models the noise between the intrinsic source and the drain. This noise includes a thermal noise component and a flicker noise component, and has the following Power Spectral Density (PSD):

$$S_{INDS} = S_{thermal} + S_{flicker}$$

This section covers the following topics:

- [EPFL-EKV Model — Intrinsic Noise Model: Thermal Noise](#)
- [EPFL-EKV Model — Intrinsic Noise Model: Flicker Noise](#)

EPFL-EKV Model — Intrinsic Noise Model: Thermal Noise

The following equation calculates the PSD thermal noise component:

$$S_{thermal} = 4kT \cdot \frac{\mu_{eff}}{(NS \cdot L_{eff})^2} \cdot |Q_I| = 4kT \cdot \beta \cdot |q_I|$$

The preceding thermal noise expression is valid in all regions of operation, including for small V_{DS} .

EPFL-EKV Model — Intrinsic Noise Model: Flicker Noise

The following equation calculates the PSD flicker noise component:

$$S_{flicker} = \frac{KF \cdot g_{mg}^2}{NP \cdot W_{eff} \cdot NS \cdot L_{eff} \cdot COX \cdot f^{AF}}$$

In some implementations, you can select different expressions.

EPFL-EKV MOSFET Model — Operating Point Information

At operating points, the following information displays to help in circuit design.

This section covers the following topics:

- [EPFL-EKV Model — Operating Point: Numerical values of model internal variables](#)
- [EPFL-EKV Model — Operating Point: Transconductance efficiency factor](#)

Chapter 2: MOSFET Models

LEVEL 55: EPFL-EKV MOSFET Model

- EPFL-EKV Model — Operating Point: Early voltage
- EPFL-EKV Model — Operating Point: Overdrive voltage
- EPFL-EKV Model — Operating Point: SPICE-like threshold voltage
- EPFL-EKV Model — Operating Point: Saturation voltage
- EPFL-EKV Model — Operating Point: Saturation / non-saturation flag

EPFL-EKV Model — Operating Point: Numerical values of model internal variables

The following are the intrinsic charges and capacitances:

$$V_G, V_S, V_D, I_{DS}, I_{DB}, g_{mg}, g_{ms}, g_{mbs}, g_{md}, V_P, n, \beta, IS, if, ir', t, t0.$$

EPFL-EKV Model — Operating Point: Transconductance efficiency factor

$$tef = g_{ms} \cdot V_t / I_{DS}$$

EPFL-EKV Model — Operating Point: Early voltage

$$VM = I_{DS} / g_{md}$$

EPFL-EKV Model — Operating Point: Overdrive voltage

$$n \cdot (V_P - V_S) \approx V_G - VTO_a - n \cdot V_S$$

For P-channel devices, $n \cdot (V_P - V_S)$ has a negative sign.

EPFL-EKV Model — Operating Point: SPICE-like threshold voltage

$$VTH = VTO_a + \Delta V_{RSCE} + \gamma' \cdot \sqrt{V'_S} - GAMMA_a \cdot \sqrt{PHI}$$

This expression is the SPICE-like threshold voltage (the source). It also accounts for charge-sharing and reverse short-channel effects on the threshold voltage.

For P-channel devices, VTH has a negative sign.

EPFL-EKV Model — Operating Point: Saturation voltage

$$VDSAT = 2V_{DSS} + 4V_t$$

For P-channel devices, $VDSAT$ has a negative sign.

EPFL-EKV Model — Operating Point: Saturation / non-saturation flag

'SAT' or '1' for $\frac{i_f}{i_r} > SATLIM$

'LIN' or '0' for $\frac{i_f}{i_r} \leq SATLIM$

Note: Some simulators implement the operating point differently (some information might not be available).

EPFL-EKV MOSFET Model — Estimation and Limits of Static Intrinsic Model Parameters

If you do not have access to a parameter extraction facility, simulation can roughly estimate the EKV intrinsic model parameters from the SPICE Level 2/3 parameters as indicated in the following table. Pay attention to the units of the parameters. This estimation method generally returns reasonable results.

Nevertheless, be aware that the underlying modeling in SPICE Level 2/3 and in the EKV model is not the same, even if the names and the function of several parameters are similar. Therefore, it is preferred if parameter extraction is made directly from measurements.

Lower and upper limits indicated in the table should give an idea on the order of magnitude of the parameters but do not necessarily correspond to physically meaningful limits, nor to the range specified in the parameter tables. These limits may be helpful for obtaining physically meaningful parameter sets when using nonlinear optimization techniques to extract EKV model parameters.

| Name | Unit | Default | Example | Lower | Upper | Estimation ¹ |
|-------|------------------|---------|------------------------|-----------------------|----------------------|---|
| COX | F/m ² | 0.7E-3 | 3.45E-3 | - | - | ϵ_{ox}/TOX |
| DL | m | 0 | -0.15*L _{min} | -0.5*L _{min} | 0.5*L _{min} | X _L - 2 · LD |
| DW | m | 0 | -0.1*W _{min} | -0.5*W _{min} | 0.5*W _{min} | X _W - 2 · WD |
| E0 | V/m | 1.0E12 | 200E6 | 0.1 / (0.4 · TOX) | 0.2 / (THETA · TOX) | |
| GAMMA | \sqrt{V} | 1.0 | 0.7 | 0 | 2 | $\sqrt{2q\epsilon_{si} \cdot NSUB / COX}$ |

Chapter 2: MOSFET Models

LEVEL 55: EPFL-EKV MOSFET Model

| Name | Unit | Default | Example | Lower | Upper | Estimation ¹ |
|------------------|-------------------|---------|---------|---------|-------|-----------------------------|
| IBA | 1/m | 0.0 | 2.0E8 | 0.0 | 5.0E8 | ALPHA · VCR/ L_C |
| IBB | V/m | 3.0E8 | 2.0E8 | 1.8E8 | 4.0E8 | VCR/ L_C |
| IBN | - | 1.0 | 0.6 | 0.4 | 1.0 | - |
| KP | A/V ² | 50E-6 | 150E-6 | 10E-6 | - | UO · COX |
| LAMBDA | - | 0.5 | 0.8 | 0 | 3 | - |
| LETA | - | 0.1 | 0.3 | 0 | 2 | - |
| LK | m | 0.29E-6 | 0.4E-6 | 0.05E-6 | 2E-6 | - |
| PHI ² | V | 0.7 | 0.5 | 0.3 | 2 | $2V_t \cdot \ln(NSUB/ n_i)$ |
| Q0 | As/m ² | 0.0 | 230E-6 | 0 | - | - |
| UCRIT | V/m | 2.0E6 | 2.3E6 | 1.0E6 | 25E6 | VMAX/UO |
| VTO | V | 0.5 | 0.7 | 0 | 2 | VTO |
| WETA | - | 0.25 | 0.2 | 0 | 2 | - |
| XJ | m | 0.1E-6 | 0.15E-6 | 0.01E-6 | 1E-6 | XJ |

1. Also compare with optional process parameters.

2. The minimum value of PHI also determines the minimum value of the pinch-off voltage. Due to the intrinsic temperature dependence of PHI, higher temperatures use a lower value, which limits the range of simulation for small currents.

$$\epsilon_{ox} = 0.0345E-9 \text{ F/m} \quad q = 1.609E-19 \text{ C} \quad k = 1.381E-23 \text{ J/K} \quad L_c = \sqrt{\epsilon_{si} \cdot XJ / COX}$$

$$\epsilon_{si} = 0.104E-9 \text{ F/m} \quad n_i = 1.45E16 \text{ m}^{-3} \quad V_t = kT/q = 0.0259 \text{ V (at room temperature)}$$

Note: Parameters in this table use m (meter) as the length unit. L_{min} is the minimum drawn length of transistors. W_{min} is the minimum drawn width of transistors. Example values are shown for enhancement N-channel devices.

EPFL-EKV MOSFET Model Updates

Synopsys has made several improvements to the original EKV v2.6 MOSFET model. Wherever possible, these enhancements maintain backward compatibility with previous versions.

This section covers the following topics:

- [EPFL-EKV Model Updates](#)
- [EPFL-EKV Model Corrections](#)

EPFL-EKV Model Updates

| Update | Description | Consequence |
|-----------------------|---|---|
| Revision I, Sep 1997 | The narrow channel effect on the substrate factor was revised to improve the transcapacitances behavior. The narrow channel effect is no longer a function of the v_s source voltage, but of the v_p pinch-off voltage. | The WETA and DW narrow channel effect parameters require different numerical values to achieve the same effect. |
| Revision II, Jul 1998 | Intrinsic Time Constant: Simulation calculates the τ_0 intrinsic time constant as a function of the effective β factor (including vertical field dependent mobility and short-channel effects), instead of the maximum mobility using the K_P parameter. Thermal noise: Simulation calculates the S_{thermal} thermal noise power spectral density as a function of the effective β factor (including vertical field dependent mobility and short-channel effects), instead of the maximum mobility using the K_P parameter. | The NQS time constant has an additional gate voltage dependence, resulting in more conservative (lower) estimation of the NQS time constant at high V_G , and additional dependence on short-channel effects. S_{thermal} has an additional gate voltage and short-channel effect dependence. |
| | Optional process parameters to calculate electrical intrinsic parameters: This option calculates the electrical parameters as a function of the optional parameters: COX— τ_{OX} GAMMA and PHI— N_{SUB} VTO— V_{FB} KP— U_O UCRIT— V_{MAX} cm is the length unit for the N_{SUB} and U_O parameters. | These parameters accommodate scaling behavior and allow meaningful statistical circuit simulation, due to de-correlation of physical effects. If you use these optional parameters, this version is compatible with former revisions, except for the default calculation of the parameters. |

Chapter 2: MOSFET Models

LEVEL 55: EPFL-EKV MOSFET Model

| Update | Description | Consequence |
|--------|---|---|
| | Optional simplified mobility model: The simple mobility model used in former model versions by using the THETA parameter, was reinstated as an option. | This mobility model simplifies adaptation from earlier model versions to the current version. |
| | Parameter synonyms: You can use E0 and Q0 as synonyms for the EO and QO parameters. | This option accommodates some simulators that use only alphabetic characters. |
| | Operating point information: This enhancement models the analytical expression for the SPICE-like VTH threshold voltage in the operating point information to include the charge-sharing and reverse short-channel effects. This option modifies the analytical expression for the VDSAT saturation voltage in the operating point information so it has a non-zero value in weak inversion. | This enhancement improves design information. |

EPFL-EKV Model Corrections

| Correction | Description |
|-------------------------|---|
| EPFL R11, March, 1999 | Equation 45, Equation 53, Equation 54, and Equation 58 were corrected for multiple series device behavior by using the NS parameter. |
| EPFL R12, July 30, 1999 | EPFL released the following corrections: <ol style="list-style-type: none">1. 99/07/30 mb (r12) corrected dGAMMAprime_dVG (narrow channel). An error in the analytical model derivatives of the GAMMAprime variable affected the transconductances and transcapacitances.2. 99/07/30 mb (r12) prevents PHI from being smaller than 0.2, both at init and after updating the temperature. For some CMOS technologies, PHI parameter values are as low as 400mV, required to account for particular process details. If you increase the temperature from room temperature, PHI decreases due to its built-in temperature dependence. As a result, PHI attains very low values or even becomes negative when it reaches 100degC. For the model to function at these temperatures, PHI has a lower limit of 200mV. The usual range for this parameter is well above this value (600mV to 1V).3. 99/06/28 mb (r12) fixed COX/KP initialization (rg).4. 99/05/04 mb (r12) completed parameter initialization for XQC, DL, and DW, and removed IBC and ibc (cd). |

LEVEL 57: BSIM3 SOI Model

The UC Berkeley SOI model (BSIM3SOI) supports Fully Depleted (FD), Partially Depleted (PD), and Dynamically Depleted (DD) SOI devices of which BSIM3PD2.0.1 for PD SOI devices is Synopsys MOSFET Level 57. For a description of this model, see the *BSIM3PD2.0 MOSFET MODEL User's Manual*.

Level 57 uses the UCB Version 2.2.3 model, which includes a separate set of the geometry-dependence parameters (`LLC`, `LWC`, `LWLC`, `WLC`, `WWC`, and `WWL`) to calculate $L_{eff}CV$ and $W_{eff}CV$.

Level 57 also includes a new Full-Depletion (FD) module (`soiMod=1`). This module provides a better fit to FD SOI devices. As `soiMod=0` (default), the model is identical to previous BSIMSOI PD models. This module also includes gate to channel/drain/source tunneling currents and overlap components.

See also: [.OPTION VER_CONTROL](#)

The following enhancements to the BSIMSOI PD version were made starting in the BSIMSOI 3.0 version:

- If the self-heating model is on, simulation calculates the channel surface potential.
- NDIF includes parameter Compared with BSIM4.6.1, several new features are added in this version.
- An error in the derivative calculation of dV_{gs_eff}/dV_g has been fixed.
- The reset value of drain/body breakdown voltage will not cause non-convergence now. Some other similar bugs have also been fixed.
- The DELTOX parameter in the MOS active element (M) models the relative variation on the trans conductance (oxide thickness) of the MOS in Monte Carlo analysis.

The following sections discuss these topics:

- [BSIM3 SOI Model — General Syntax](#)
- [BSIM3 SOI Model Parameters](#)
- [BSIM3 SOI Model — Range Limit Parameters](#)
- [BSIM3 SOI Model — Version Updates](#)

Chapter 2: MOSFET Models

LEVEL 57: BSIM3 SOI Model

- [BSIM3 SOI Model — PD Version Updates](#)
- [BSIM3 SOI Model — Output Templates](#)

BSIM3 SOI Model — General Syntax

Syntax:

```
Mxxx nd ng ns ne [np] [nb] [nT] mname [L=val] [W=val]
+ [M=val] [NRD=val] [AD=val] [AS=val] [PD=val] [PS=val]
+ [NRS=val] [NRB=val] [RTH0=val] [NBC=val]
+ [NSEG=val] [PDBCP=val] [PSBCP=val] [AGBCP=val]
+ [AEBCP=val] [VBSUSR=val] [DELTOX=val] [TNODEOUT]
+ [off] [FRBODY] [BJTOFF=val] [IC=Vds, Vgs, Vbs, Ves]
+ [SOIMOD=val] [SOIQ0=val] [MULID0=val]
```

| Parameter | Description |
|-----------|---|
| AD | Drain diffusion area. Overrides .OPTION DEFAD statement. Default=DEFAD. |
| AEBCP | Parasitic body-to-substrate overlap area for the body contact. |
| AGBCP | Parasitic gate-to-body overlap area for the body contact. |
| AS | Source diffusion area. Overrides .OPTION DEFAS statement. Default=DEFAS. |
| BJTOFF | Turning off BJT if equal to 1. |
| CTH0 | Thermal capacitance per unit width: <ul style="list-style-type: none">▪ If you do not specify CTH0, simulation extracts it from the model card.▪ If you specify CTH0, it overrides CTH0 in the model card. |
| DELTOX | Shift in gate oxide thickness (TOX). That is, the difference between the electrical and physical gate oxide/insulator thicknesses. |
| FRBODY | Coefficient of the distributed body resistance effects. Default=1.0 |
| IC | Initial guess in the order (drain, front gate, internal body, back gate, external voltage). (ignores Vps for 4-terminal devices) Use these only if you specify UIC in the .TRAN statement. The .IC statement overrides it. |
| L | SOI MOSFET channel length in meters. This parameter overrides DEFL in an OPTIONS statement. Default=DEFL with a maximum of 0.1m. |
| M | Multiplier to simulate multiple SOI MOSFETs in parallel. The M setting affects all channel widths, diode leakages, capacitances, and resistances. Default=1. |
| mname | MOSFET model name reference. |

| Parameter | Description |
|-----------|--|
| Mxxx | SOI MOSFET element name. Must begin with M, followed by up to 1023 alphanumeric characters. |
| nb | Internal body node name or number. |
| NBC | Number of body contact isolation edge. |
| nd | Drain terminal node name or number. |
| ne | Back gate (or substrate) node name or number. |
| ng | Front gate node name or number. |
| np | External body contact node name or number. |
| NRB | Number of squares for the body series resistance. |
| NRD | NRD (Number of squares of drain diffusion for resistance calculations) overrides .OPTION DEFNRD. For nonCMI models such as BSIM3 etc... Default=DEFNRD, if you set ACM=0 or 1 model parameter. Default=0.0, if you set ACM=2 or 3 For CMI models such as BSIM4 etc... Default=1.0 |
| NRS | NRS (Number of squares of source diffusion for resistance calculations) overrides .OPTION DEFNRS. For nonCMI models such as BSIM3 etc... Default=DEFNRS, if you set ACM=0 or 1 model parameter. Default=0.0, if you set ACM=2 or 3 For CMI models such as BSIM4 etc... Default=1.0 |
| ns | Source terminal node name or number. |
| NSEG | Number of segments for partitioning the channel width. |
| nT | Temperature node name or number. |
| OFF | Sets the initial condition of the element to OFF in DC analysis. |
| PD | Drain junction perimeter, including channel edge. Overrides .OPTION DEFPD. |
| PDBCP | Parasitic perimeter length for the body contact at the drain side. |
| PS | Source junction perimeter including channel edge. Overrides .OPTION DEFPS. |
| PSBCP | Parasitic perimeter length for the body contact at the source side. |

Chapter 2: MOSFET Models

LEVEL 57: BSIM3 SOI Model

| Parameter | Description |
|-----------|--|
| RTH0 | Thermal resistance per unit width: <ul style="list-style-type: none">▪ If you do not specify RTH0, simulation extracts it from the model card.▪ If you specify RTH0, it overrides RTH0 in the model card. |
| SOIMOD | SOI model selector <ul style="list-style-type: none">▪ If SOIMOD is not specified, it's extracted from the model card.▪ If SOIMOD is specified, it overrides SOIMOD in the model card. |
| SOIQ0 | Floating body charge initialization. This parameter is set for the BQI algorithm of a floating body node. |
| TNODEOUT | Temperature node flag indicating the use of the T node. |
| VBSUSR | Optional initial Drain/Body Breakdown Voltage of Vbs that you specify for transient analysis. |
| W | MOSFET channel width in meters. This parameter overrides DEFW in an OPTIONS statement. Default=DEFW. |
| MULID0 | Scaling factor of drain current, the default is 1.0. |

- If you do not set TNODEOUT, you can specify four nodes for a device to float the body. Specifying five nodes implies that the fifth node is the external body contact node with a body resistance between the internal and external terminals. This configuration applies to a distributed body resistance simulation.
- If you set TNODEOUT, simulation interprets the last node as the temperature node. You can specify five nodes to float the device. Specifying six nodes implies body contact. Seven nodes is a body-contacted case with an accessible internal body node. You can use the temperature node to simulate thermal coupling.

BSIM3 SOI Model Parameters

This section covers the following topics:

- [BSIM3 SOI Model — Control Parameters](#)
- [BSIM3 SOI Model — Process Parameters](#)
- [BSIM3 SOI Model — DC Parameters](#)
- [BSIM3 SOI Model — AC and Capacitance Parameters](#)

- [BSIM3 SOI Model — Temperature Parameters](#)
- [BSIM3 SOI Model — Avalanche Impact Ionization Parameters](#)
- [BSIM3 SOI Model — Notes](#)

BSIM3 SOI Model — Control Parameters

| Parameter | Unit | Default | Description |
|-----------|------|---------|---|
| CAPMOD | - | 2 | Flag for the short channel capacitance model |
| MOBMOD | - | 1 | Mobility model selector |
| NOIMOD | - | 1 | Flag for the noise model |
| SHMOD | - | 0 | Flag for self-heating: 0 - no self-heating 1 - self-heating |

BSIM3 SOI Model — Process Parameters

| Parameter | Unit | Default | Description |
|---------------------------|-------------------|---------|---|
| DTOXCV (capmod=3 only) | | | Difference between the electrical and physical gate oxide thicknesses, due to the effects of the gate poly-depletion and the finite channel charge layer thickness. |
| NCH | 1/cm ³ | 1.7e17 | Channel doping concentration |
| NGATE | 1/cm ³ | 0 | Poly gate doping concentration |
| NSUB | 1/cm ³ | 6.0e16 | Substrate doping concentration |
| TBOX | m | 3.0e-7 | Buried oxide thickness |
| TOX | m | 1.0e-8 | Gate oxide thickness |
| TSI | m | 1.0e-7 | Silicon film thickness |
| XJ | m | - | S/D junction depth |

Chapter 2: MOSFET Models

LEVEL 57: BSIM3 SOI Model

BSIM3 SOI Model — DC Parameters

| Parameter | Unit | Default | Description |
|-----------|------------------|---------|--|
| A0 | - | 1.0 | Bulk charge effect coefficient for the channel length |
| A1 | 1/V | 0.0 | First non-saturation effect parameter |
| A2 | - | 1.0 | Second non-saturation effect parameter |
| AELY | V/m | 0 | Channel length dependency of the early voltage for the bipolar current |
| AGIDL | 1/W | 0.0 | GIDL constant |
| AGS | 1/V | 0.0 | Gate bias coefficient of A_{bulk} |
| AHLI | - | 0 | High-level injection parameter for the bipolar current |
| ALPHA0 | m/V | 0.0 | First parameter of the impact ionization current |
| B0 | m | 0.0 | Bulk charge effect coefficient for the channel width |
| B1 | m | 0.0 | Bulk charge effect width offset |
| BETA0 | 1/V | 0.0 | First V_{ds} dependence parameter of the impact ionization current |
| BETA1 | - | 0.0 | Second V_{ds} dependence parameter of the impact ionization current |
| BETA2 | V | 0.1 | Third V_{ds} dependence parameter of the impact ionization current |
| BGIDL | V/m | 0.0 | GIDL exponential coefficient |
| CDSC | F/m ² | 2.4e-4 | Drain/source to the channel coupling capacitance |
| CDSCB | F/m ² | 0 | Body-bias sensitivity of cdsc |
| CDSCD | F/m ² | 0 | Drain-bias sensitivity of cdsc |
| CIT | F/m ² | 0.0 | Interface trap capacitance |
| DELTA | - | 0.01 | Effective V_{ds} parameter |
| DROUT | - | 0.56 | L dependence coefficient of the DIBL correction parameter in Rout |

| Parameter | Unit | Default | Description |
|------------------|--------------------|----------------|--|
| DSUB | - | 0.56 | DIBL coefficient exponent |
| DVT0 | - | 2.2 | First coefficient of the short-channel effect on Vth |
| DVT0W | - | 0 | First coefficient of the narrow width effect on Vth for a small channel length |
| DVT1 | - | 0.53 | Second coefficient of the short-channel effect on Vth |
| DVT1W | - | 5.3e6 | Second coefficient of the narrow width effect on Vth for a small channel length |
| DVT2 | 1/V | -0.032 | Body-bias coefficient of the short-channel effect on Vth |
| DVT2W | 1/V | -0.032 | Body-bias coefficient of the narrow width effect on Vth for a small channel length |
| DWB | m/V ^{1/2} | 0.0 | Coefficient of the substrate body bias dependence of Weff |
| DWBC | m | 0.0 | Width offset for the body contact isolation edge |
| DWG | m/V | 0.0 | Coefficient of the gate dependence of Weff |
| ESATI | V/m | 1.e7 | Saturation channel electric field for the impact ionization current |
| ETA0 | - | 0.08 | DIBL coefficient in the subthreshold region |
| ETAB | 1/V | -0.07 | Body-bias coefficient for the DIBL effect in the subthreshold region |
| FBJTII | - | 0.0 | Fraction of the bipolar current affecting the impact ionization |
| ISBJT | A/m ² | 1.0e-6 | BJT injection saturation current |
| ISDIF | A/m ² | 0 | Body to source/drain injection saturation current |
| ISREC | A/m ² | 1.0e-5 | Recombination in the depletion saturation current |
| ISTUN | A/m ² | 0.0 | Reverse tunneling saturation current |
| K1 | V ^{1/2} | 0.6 | First-order body effect coefficient |
| K1W1 | m | 0 | First-order effect width dependent parameter |
| K1W2 | m | 0 | Second-order effect width dependent parameter |

Chapter 2: MOSFET Models

LEVEL 57: BSIM3 SOI Model

| Parameter | Unit | Default | Description |
|-----------|------|---------|--|
| K2 | - | 0 | Second-order body effect coefficient |
| K3 | - | 0 | Narrow coefficient |
| K3B | 1/V | 0 | Body effect coefficient of k3 |
| KB1 | - | 1 | Backgate body charge coefficient |
| KETA | 1/V | -0.6 | Body-bias coefficient of the bulk charge effect |
| KETAS | V | 0.0 | Surface potential adjustment for the bulk charge effect |
| LBJT0 | m | 0.2e-6 | Reference channel length for the bipolar current |
| LII | - | 0 | Channel length dependence parameter for the impact ionization current |
| LINT | m | 0.0 | Length offset fitting parameter from I-V without bias |
| LN | m | 2.0e-6 | Electron/hole diffusion length |
| NBJT | - | 1 | Power coefficient of the channel length dependency for the bipolar current |
| NDIODE | - | 1.0 | Diode non-ideality factor |
| NFACTOR | - | 1 | Subthreshold swing factor |
| NGIDL | V | 1.2 | GIDL V_{ds} enhancement coefficient |
| NLX | m | 1.74e-7 | Lateral non-uniform doping parameter |
| NRECF0 | - | 2.0 | Recombination non-ideality factor at the forward bias |
| NRECR0 | - | 10 | Recombination non-ideality factor at the reversed bias |
| NTUN | - | 10.0 | Reverse tunneling non-ideality factor |
| PCLM | - | 1.3 | Channel length modulation parameter |
| PDIBLC1 | - | 0.39 | Correction parameter for the DIBL effect of the first output resistance |
| PDIBLC2 | - | 0.0086 | Correction parameter for the DIBL effect of the second output resistance |
| PRWB | 1/V1 | 0 | Body effect coefficient of Rds _w |

| Parameter | Unit | Default | Description |
|-----------|---|----------------------|---|
| PRWG | 1/V1/2 | 0 | Gate-bias effect coefficient of Rdsw |
| PVAG | - | 0.0 | Gate dependence of the Early voltage |
| RBODY | ohm/m2 | 0.0 | Intrinsic body contact sheet resistance |
| RBSH | ohm/m2 | 0.0 | Extrinsic body contact sheet resistance |
| RDSW | $\Omega^* \mu\text{m}^{\text{wr}}$ | 100 | Parasitic resistance per unit width |
| RSH | ohm/square | 0.0 | Source/drain sheet resistance in ohm per square |
| SII0 | 1/V | 0.5 | First V_{gs} dependence parameter for the impact ionization current |
| SII1 | 1/V | 0.1 | Second V_{gs} dependence parameter for the impact ionization current |
| SII2 | 1/V | 0 | Third V_{gs} dependence parameter for the impact ionization current |
| SIID | 1/V | 0 | V_{ds} dependence parameter of the drain saturation voltage for the impact ionization current |
| TII | - | 0 | Temperature dependence parameter for the impact ionization current |
| U0 | $\text{cm}^2/(\text{V}\cdot\text{sec})$ | NMOS-670 PMOS-250 | Mobility at Temp=Tnom |
| UA | m/V | 2.25e-9 | First-order mobility degradation coefficient |
| UB | (m/V) ² | 5.87e-19 | Second-order mobility degradation coefficient |
| UC | 1/V | -0.0465 | Body-effect of the mobility degradation coefficient |
| VABJT | V | 10 | Early voltage for the bipolar current |
| VDSATII0 | V | 0.9 | Nominal drain saturation voltage at threshold for the impact ionization current |
| VECB | v | 0.026v | Electron tunneling from the conduction band |
| VEVB | v | 0.075v | Electron tunneling from the valence band |

Chapter 2: MOSFET Models

LEVEL 57: BSIM3 SOI Model

| Parameter | Unit | Default | Description |
|-----------|-------|-----------------------|---|
| voff | v | -0.08 | Offset voltage in the subthreshold region for large W and L |
| Vrec0 | V | 0.0 | Voltage dependent parameter for the recombination current |
| vsat | m/sec | 8e4 | Saturation velocity at Temp=Tnom |
| vth0 | v | NMOS 0.7 PMOS -0.7 | Threshold voltage @ Vbs=0 for a long, wide device |
| Vtun0 | V | 0.0 | Voltage dependent parameter for the tunneling current |
| w0 | m | 0 | Narrow width parameter |
| wint | m | 0.0 | Width offset fitting parameter from I-V without bias |
| wr | - | 1 | Width offset from Weff for the Rds calculation |

BSIM3 SOI Model — AC and Capacitance Parameters

| Parameter | Unit | Default | Description |
|-----------|------------------|------------|---|
| ACDE | m/V | 1.0 | Exponential coefficient for the charge thickness in the CapMod=3 for the accumulation and depletion regions |
| ASD | V | 0.3 | Smoothing parameter for the source/drain bottom diffusion |
| CF | F/m | cal. | Fringing field capacitance of the gate-to-source/drain |
| CGDL | F/m | 0.0 | Overlap capacitance for the lightly-doped drain-gate region |
| CGDO | F/m | 0 | Non LDD region drain-gate overlap capacitance per channel length |
| CGEO | F/m | 0 | Gate substrate overlap capacitance per unit channel length |
| CGSL | F/m | 0.0 | Overlap capacitance for the lightly-doped source-gate region |
| CGSO | F/m | calculated | Non LDD region source-gate overlap capacitance per channel length |
| CJSWG | F/m ² | 1.e-10 | Source/drain (gate side) sidewall junction capacitance per unit width (normalized to 100nm Tsi) |
| CKAPPA | F/m | 0.6 | Coefficient for the fringing field capacitance for the overlap capacitance in the lightly-doped region |

| Parameter | Unit | Default | Description |
|-----------|--------|---------|---|
| CLC | m | 0.1e-7 | Constant term for the short-channel model |
| CLE | - | 0.0 | Exponential term for the short-channel model |
| CSDESW | F/m | 0.0 | Fringing capacitance per unit length for the source/drain sidewall |
| CSDMIN | V | cal. | Minimum capacitance for the source/drain bottom diffusion |
| DELVT | V | 0.0 | Threshold voltage adjustment for C-V |
| DLBG | m | 0 | Length offset fitting parameter for the backgate charge |
| DLC | m | lint | Length offset fitting parameter for the gate charge |
| DLCB | m | lint | Length offset fitting parameter for the body charge |
| DWC | m | wint | Width offset fitting parameter from C-V |
| FBODY | - | 1.0 | Scaling factor for the body charge |
| LDIF0 | - | 1 | Channel length dependency coefficient of the diffusion cap. |
| MJSWG | V | 0.5 | Grading coefficient of the source/drain (gate side) sidewall junction capacitance |
| MOIN | V1/2 | 15.0 | Coefficient for the gate-bias dependent surface potential |
| NDIF | - | -1 | Power coefficient of the channel length dependency for the diffusion capacitance |
| PBSWG | V | 0.7 | Built-in potential of the source/drain (gate side) sidewall junction capacitance |
| TT | second | 1ps | Diffusion capacitance transit time coefficient |
| VSDFB | V | cal. | Flatband voltage for the source/drain bottom diffusion capacitance |
| VSDTH | V | cal. | Threshold voltage for the source/drain bottom diffusion capacitance |
| XPART | - | 0 | Charge partitioning rate flag |

Chapter 2: MOSFET Models

LEVEL 57: BSIM3 SOI Model

BSIM3 SOI Model — Temperature Parameters

| Parameter | Unit | Default | Description |
|-----------|--------------------|-----------|--|
| AT | m/sec | 3.3e4 | Temperature coefficient for U_a |
| CTH0 | (W*S)/m°C | 0 | Normalized thermal capacity |
| KT1 | V | -0.11 | Temperature coefficient for the threshold voltage |
| KT2 | - | 0.022 | Body-bias coefficient of the threshold voltage temperature effect |
| KTIL | V*m | 0 | Channel length dependence of the temperature coefficient for the threshold voltage |
| NTRECF | - | 0 | Temperature coefficient for N_{ref} |
| NTRECR | - | 0 | Temperature coefficient for N_{recr} |
| PRT | $\Omega_{-\mu m}$ | 0 | Temperature coefficient for R_{dsW} |
| RTH0 | m°C/W | 0 | Normalized thermal resistance |
| TCJSWG | 1/K | 0 | Temperature coefficient of C_{jswg} |
| TNOM | °C | 25 | Temperature at which simulation expects parameters |
| TPBSWG | V/K | 0 | Temperature coefficient of P_{bswg} |
| UA1 | m/V | 4.31e-9 | Temperature coefficient for U_a |
| UB1 | (m/V) ² | -7.61e-18 | Temperature coefficient for U_b |
| UC1 | 1/V | -0.056 | Temperature coefficient for U_c |
| UTE | - | -1.5 | Mobility temperature exponent |
| XBJT | - | 1 | Power dependence of j_{bjt} on the temperature |
| XDIF | - | XBJT | Power dependence of j_{dif} on the temperature |
| XREC | - | 1 | Power dependence of j_{rec} on the temperature |
| XTUN | - | 0 | Power dependence of j_{tun} on the temperature |

BSIM3 SOI Model — Avalanche Impact Ionization Parameters

The following parameters improve the BSIM3SOI model to address parasitic BJT-induced avalanche impact ionization current.

| Parameter | Unit | Default | Description | Notes |
|-----------|------|-----------------------|--|-----------------------------|
| ABJTII | - | 0.0 | Exponent factor for avalanche current | - |
| CBJTII | m/V | 0.0 | Length scaling parameter for II BJT part | - |
| EBJTII | 1/V | 0.0 | Impact ionization parameter for BJT part | - |
| IIMOD | - | 0 (original II model) | Impact ionization model selector | =1 selects the new II model |
| MBJTII | - | 0.4 | Internal B-C grading coefficient | - |
| TVBCI | - | 0.0 | Temperature coefficient for VBCI | - |
| VBCI | V | 0.7 | Internal B-C built-in potential | - |

BSIM3 SOI Model — Notes

- BSIMPD2.01 supports capmod=2 and 3 only. It does not support capmod=0 and 1.
- Modern SOI technology commonly uses source/drain extension or LDD. The source/drain junction depth (X_j) can be different from the silicon film thickness (T_{Si}). By default, if you do not specify X_j , simulation sets it to T_{Si} . X_j cannot be greater than T_{Si} .
- BSIMPD refers the substrate to the silicon below the buried oxide (not to the well region in BSIM3) to calculate the backgate flatband voltage (V_{fb}) and the parameters related to the source/drain diffusion bottom capacitance (V_{sdth} , V_{sdfb} , C_{sdmin}).
 - Positive nsub means the same type of doping as the body.
 - Negative nsub means the opposite type of doping.
- New W0FLK Parameter:
The following equation models the SPICE2 flicker noise current density, used in both UCB SOI code and the Synopsys Level=57 MOSFET model for noiMod=1 and 4:

Chapter 2: MOSFET Models

LEVEL 57: BSIM3 SOI Model

$$S_{id,f} [A^2/Hz] = K_F * I_{ds}^{AF} / (C_{ox} * L_{eff}^2 * f^{EF}) \quad \text{--- (1)}$$

However, if A_F is not equal to unity, it does not scale properly with W_{eff} , because I_{ds} is approximately proportional to W_{eff} . Also, without the HSPICE multiplicity factor (M factor) in equation (1), this model cannot simulate multiple transistors in parallel.

To solve these problems, HSPICE 2002.2 added a W_{0FLK} (width normalizing) parameter, and corrects equation (1) as:

$$M * K_F * [(W_{eff}/W_{0FLK}) (1-A_F)] * I_{ds}^{AF} / (C_{ox} * L_{eff}^2 * f^{EF}) \quad \text{--- (2)}$$

The default value of W_{0FLK} is -1.0 to switch off the new width-scaling model. The unit is in meters.

The next equation handles the flicker noise model ($noimod=1$ & 4), depending on whether you specify W_{0FLK} .

If $W_{0FLK} <= 0.0$ (the default case), then the flicker noise model of $noiMod=1$ and 4 uses this equation for backward compatibility.

$$\begin{aligned} & M * K_F * I_{ds}^{AF} / (C_{ox} * L_{eff}^2 * f^{EF}) \quad \text{--- (3)} \\ & \text{ELSE} \\ & \quad M * K_F * [(W_{eff}/W_{0FLK})^{(1-A_F)}] * I_{ds}^{AF} / (C_{ox} * L_{eff}^2 * f^{EF}) \end{aligned}$$

BSIM3 SOI Model — Range Limit Parameters

Simulation reports either a warning or a fatal error if BSIM3 version 3 parameters fall outside predefined ranges. These range limitations prevent (or at least warn of) potential numerical problems.

To control the maximum number of simulation warning messages printing to the output file, use:

```
.OPTION WARNLIMIT=#
```

In the preceding .OPTION statement, # is the maximum number of warning messages that simulation reports. The default `WARNLIMIT`

The source/drain bulk junction capacitance will not be discontinuous when V_{bs}/V_{bd} is zero. The S/D junction sidewall capacitance along the isolation edge is set to zero if they are negative.

value is 1. In some cases, simulation checks parameters only if you set the PARMAMCHK=1 model parameter.

| Parameter | Limits | Comment |
|-----------|-----------------------|--|
| ACDE | < 0.1, > 1.6 warn | if (2.2299 < version < 3.1099) acde < 0.4 warn |
| B1 | b1+weff =0 fatal | |
| CLC | < 0 fatal | |
| DELTA | < 0 fatal | |
| DROUT | < 0 fatal | |
| DSUB | < 0 fatal | |
| DVT1 | < 0 fatal | |
| DVT1W | < 0 fatal | |
| MOIN | < 5, > 25 warn | |
| MOINFD | < 5.0 warn | if (version > 2.9999) |
| NGATE | < 0, > 1e25 fatal | |
| NLX | < -leff fatal | |
| NOFF | =0 warn, set 1.0 | If (version>3.1999) < 0.1, > 4.0 warn |
| NPEAK | <= 0 fatal | |
| PCLM | <= 0 fatal | |
| TBOX | <= 0 fatal | |
| TOX | tox+deltox < 0 fatal | |
| TOXM | toxm+deltox < 0 fatal | |
| U0 | <= 0 fatal | |
| VSAT | <= 0 fatal | |
| W0 | w0+weff =0 fatal | |

if paramchk=1 following parameter limit range is added

Chapter 2: MOSFET Models

LEVEL 57: BSIM3 SOI Model

| Parameter | Limits | Comment |
|-----------|-------------------|---------------------------------------|
| A2 | < 0.01, > 1 warn | |
| ACDE | < 0.4, > 1.6 warn | if (version > 3.1099) acde < 0.1 warn |
| AELY | < 0 warn | |
| AGIDL | < 0 warn | |
| AHLI | < 0 warn | |
| ALPHAGB1 | < 0 warn | |
| ALPHAGB2 | < 0 warn | |
| ASD | < 0 warn | |
| B1 | b1+weff<1e-7 warn | |
| BETA0 | < 0 warn | |
| BETA1 | < 0 warn | |
| BETA2 | < warn | |
| BETAGB1 | < 0 warn | |
| BGIDL | < 0 warn | |
| CAPMOD | < 2 warn | |
| CDSC | < 0 warn | |
| CDSCD | < 0 warn | |
| CGDOI | < 0 warn | |
| CGEO | < 0 warn | |
| CGSOI | < 0 warn | |
| CSDESW | < 0 warn | |
| CSDMIN | < 0 warn | |
| CTH0 | <0 warn | |
| DELTAVOX | <= 0 warn | |

| Parameter | Limits | Comment |
|-----------|----------------|------------------------|
| DLBG | < 0 warn | |
| DVT0 | < 0 warn | |
| DWBC | < 0 warn | |
| EBG | < 0 warn | |
| ESATII | < 0 warn | Should be within (0,1) |
| ETA0 | <0 warn | |
| FBJTII | < 0 warn | |
| ISBJT | < 0 warn | |
| ISDIF | < 0 warn | |
| ISREC | < 0 warn | |
| ISTUN | < 0 warn | |
| K1W1 | < 0 warn | |
| K1W2 | < 0 warn | |
| KETAS | < 0 warn | |
| LEFF | <= 5e-8 warn | |
| LEFFCV | <= 5e-8 warn | |
| LII | < 0 warn | |
| MOIN | < 5, > 25 warn | |
| NBJT | < 0 warn | |
| NDIF | < 0 warn | if (version <= 2.9999) |
| NDIODE | < 0 warn | |
| NECB | < 0 warn | |
| NEVB | < 0 warn | |
| NFACTOR | < 0 warn | |

Chapter 2: MOSFET Models

LEVEL 57: BSIM3 SOI Model

| Parameter | Limits | Comment |
|-----------|-----------------------------------|-----------------------|
| NGATE | $0 < \text{ngate} \leq 1e18$ warn | |
| NGIDL | < 0 warn | |
| NIGC | ≤ 0 fatal | if (version > 2.9999) |
| NLX | < 0 warn | |
| NPEAK | $\leq 1e15, \geq 1e21$ warn | |
| NSUB | $\geq 1e21$ warn | |
| NTOX | < 0 warn | |
| NTRECF | < 0 warn | |
| NTRED | < 0 warn | |
| NTUN | < 0 warn | |
| PDIBL1 | < 0 warn | |
| PDIBL2 | < 0 warn | |
| PIGCD | ≤ 0 fatal | if (version > 2.9999) |
| POXEDGE | ≤ 0 fatal | if (version > 2.9999) |
| RBODY | < 0 warn | |
| RBODY | < 0 warn | |
| RBSH | < 0 warn | |
| RBSH | < 0 warn | |
| RDS0 | $> 0, < 0.001$ warn | |
| RDSW | < 0 warn | |
| RHALO | < 0 warn | |
| RTH0 | < 0 warn | |
| SII1 | < 0 warn | |
| SII2 | < 0 warn | |

| Parameter | Limits | Comment |
|-----------|---------------------|------------------------|
| SIID | < 0 warn | |
| TCJSWG | < 0 warn | if (version <= 2.9999) |
| TII | < 0 warn | |
| TOX | tox+deltox < 0 warn | |
| TOXQM | <= 0 warn | |
| TOXTREF | < 0 warn | |
| TPBSWG | < 0 warn | if (version <= 2.9999) |
| TT | < 0 warn | |
| VECB | < 0 warn | |
| VEVB | < 0 warn | |
| VGB1 | < 0 warn | |
| VGB2 | < 0 warn | |
| VOXH | < 0 warn | |
| VREC0 | < 0 warn | |
| VSATTEMP | < 1e3 warn | |
| VTUN0 | < 0 warn | |
| W0 | w0+weff < 1e-7 warn | |
| WEFF | <= 1e-7 warn | |
| WEFFCV | <= 1e-7 warn | |
| WTH0 | < 0 warn | |
| XJ | > tsi warn | |

BSIM3 SOI Model — Version Updates

This section covers the following topics:

- [BSIM3 SOI Version 3.2 Updates](#)
- [BSIM3 SOI Version 3.1 Updates](#)

BSIM3 SOI Version 3.2 Updates

The model selector, SoiMod, is an instance parameter and a model parameter. SoiMod will determine the operation of BSIMSOI.

If SoiMod=0 (default), the model equation is identical to the BSIMPD equation.

If SoiMod=1 (unified model for PD&FD) or SoiMod=2 (ideal FD), the following equations (FD module) are added on top of BSIMPD.

$$V_{bs0} = \frac{C_{Si}}{C_{Si} + C_{BOX}} \cdot \left(phi - \frac{qN_{ch}(1 + N_{LX}/L_{eff})}{2\varepsilon_{Si}} \cdot T_{Si}^2 + V_{nonideal} + \Delta V_{DIBL} \right) + \eta_e \frac{C_{BOX}}{C_{Si} + C_{BOX}} \cdot (V_{es} - V_{FBb})$$

where $C_{Si} = \frac{\varepsilon_{Si}}{T_{Si}}$, $C_{BOX} = \frac{\varepsilon_{OX}}{T_{BOX}}$, $C_{OX} = \frac{\varepsilon_{OX}}{T_{OX}}$

$$\Delta V_{DIBL} = D_{vbd0} \left(\exp\left(-D_{vbd1} \frac{L_{eff}}{2l}\right) + 2 \exp\left(-D_{vbd1} \frac{L_{eff}}{l}\right) \right) \cdot (V_{bi} - 2\Phi_B)$$

$$\eta_e = K_{1b} - K_{2b} \cdot \left(\exp\left(-D_{k2b} \frac{L_{eff}}{2l}\right) + 2 \exp\left(-D_{k2b} \frac{L_{eff}}{l}\right) \right)$$

$$phi = phi_{ON} - \frac{C_{OX}}{C_{OX} + (C_{Si}^{-1} + C_{BOX}^{-1})^{-1}} \cdot N_{OFF,FD} V_t \cdot \ln\left(1 + \exp\left(\frac{V_{th,FD} - V_{gs_eff} - V_{OFF,FD}}{N_{OFF,FD} V_t}\right)\right)$$

$$phi_{ON} = 2\Phi_B + V_t \ln\left(1 + \frac{V_{gsteff,FD} (V_{gsteff,FD} + 2K1\sqrt{2\Phi_B})}{M_{on,FD} \cdot K1 \cdot V_t^2}\right),$$

$$V_{gsteff,FD} = N_{OFF,FD} V_t \cdot \ln\left(1 + \exp\left(\frac{V_{gs_eff} - V_{th,FD} - V_{OFF,FD}}{N_{OFF,FD} V_t}\right)\right)$$

Here N_{ch} is the channel doping concentration. N_{LX} is the lateral non-uniform doping coefficient to account for the lateral non-uniform doping effect. V_{FBb} is

the backgate flatband voltage. $V_{th,FD}$ is the threshold voltage at $V_{bs}=V_{bs0}(\phi=2\Phi_B)$. V_t is thermal voltage. K_1 is the body effect coefficient.

If SoiMod=1, the lower bound of V_{bs} (SPICE solution) is set to V_{bs0} . If SoiMod=2, V_{bs} is pinned at V_{bs0} . Notice that there is no body node and body leakage/charge calculation in SoiMod=2.

The zero field body potential that will determine the transistor threshold voltage, V_{bsmos} , is then calculated by

$$V_{bsmos} = V_{bs} - \frac{C_{Si}}{2qN_{ch}T_{Si}}(V_{bs0}(T_{OX} \rightarrow \infty) - V_{bs})^2 \text{ if } V_{bs} \leq V_{bs0}(T_{OX} \rightarrow \infty) \\ = V_{bs} \text{ else}$$

The subsequent clamping of V_{bsmos} will use the same equation that was utilized in BSIMPD. You can download the BSIMPD manual at:

<http://www-device.eecs.Berkeley.edu/~bsimsoi>

If SoiMod=3 is specified, BSIMSOI will select the operation mode for the user based on the estimated value of V_{bs0} at $\phi=2\Phi_B$ (bias independent), V_{bs0t} :

- If $V_{bs0t} > V_{bs0fd}$, BSIMSOI will be in the ideal FD mode (SoiMod=2).
- If $V_{bs0t} < V_{bs0pd}$, BSIMSOI will be in the BSIMPD mode (SoiMod=0).

Otherwise, BSIMSOI will be operated under SoiMod=1.

Notice that both V_{bs0fd} and V_{bs0pd} are model parameters.

A new model parameter, T_{OXM} , is introduced to represent the T_{OX} dependence for the model parameters K_1 and K_2 (compatible to BSIM3 version 3.2).

A new model parameter, N_{OFF} , is introduced in $V_{gsteff,cv}$ to adjust the CV curve around the threshold (compatible to BSIM3 version 3.2).

This section covers the following topics:

- Chapter 2, BSIM3 SOI Version 3.2 Updates — Noise Model
- Chapter 2, BSIM3 SOI Version 3.2 Updates — Simple and Unified Flicker Noise Models
- Chapter 2, BSIM3 SOI Version 3.2 Updates — Thermal Noise Models
- Chapter 2, BSIM3 SOI Version 3.2 Updates — Model Parameters

BSIM3 SOI Version 3.2 Updates — Noise Model

The BSIMSOI3.2 version implements a flicker noise and thermal noise model compatible with BSIM4. In addition, the new noise model includes gate tunneling-induced shot noise and thermal noise due to gate electrode resistance. (1) Flicker noise models

Note: For output noise parameters, see [Chapter 6, MOSFET Noise Models.](#)

BSIM3 SOI Version 3.2 Updates — Simple and Unified Flicker Noise Models

BSIMSOI3.2 provides two flicker noise models. When the model selector fnoiMod is set to 0, a simple flicker noise model which is convenient for hand calculation is invoked. A unified physical flicker noise model, which is the default model, will be used if fnoiMod=1. These two modes come from BSIMSOI3.1, but the unified model has many improvements. For instance, it is now smooth over all bias regions and considers the bulk charge effect.

- fnoiMOD = 0 (simple model)

$$S_{id}(f) = \frac{K_f I_{ds}^{af}}{C_{ox} L_{eff}^2 f^{ef}}$$

The noise density is:

- fnoiMOD = 1 (unified model)

The physical mechanism for the flicker noise is trapping/de-trapping related charge fluctuation in oxide traps, which results in fluctuations of both mobile carrier numbers and mobility in the channel. The unified flicker noise model captures this physical process.

The noise density in inversion region is given by:

$$S_{id,inv}(f) = \frac{k_B T q^2 \mu_{eff} I_{ds}}{C_{ox} L_{eff}^2 A_{bulk} f^{ef} \cdot 10^{10}} \left(NOLA \log \left(\frac{N_0 + N^*}{N_l + N^*} \right) + NOIB(N_0 - N_l) + \frac{NOIC}{2} (N_0^2 - N_l^2) \right) \\ + \frac{k_B T I_{ds}^2 \Delta L_{clm}}{W_{eff} L_{eff}^2 f^{ef} \cdot 10^{10}} \frac{NOLA + NOIB \cdot N_l + NOIC \cdot N_l^2}{(N_l + N^*)^2}$$

where μ_{eff} is the effective mobility at the given bias condition, and L_{eff} and W_{eff} are the effective length and width, respectively. The parameter N_0 is the charge density at the source side given by:

$$N_0 = \frac{C_{ox}V_{gsteff}}{q}$$

The parameter N_1 is the charge density at the source side given by:

$$N_1 = \frac{C_{ox}V_{gsteff}}{q} \left(1 - \frac{A_{bulk}V_{dseff}}{V_{gsteff} + 2V_t} \right)$$

N^* is given by:

$$N^* = K_B T \cdot \frac{(C_{ox} + C_d + CIT)}{q_2}$$

where CIT is a model parameter from DC IV and C_d is the depletion capacitance. ΔL_{clm} is the channel length reduction due to channel length modulation and given by:

$$\Delta L_{clm} = Litl \cdot \log \frac{\frac{V_{ds} - V_{dseff}}{Litl} + EM}{E_{sat}}$$

$$E_{sat} = \frac{2VSAT}{\mu_{eff}}$$

In the subthreshold region, the noise density is written as:

$$S_{id, subVt}(f) = \frac{NOIA \cdot k_B T \cdot I_{ds}^2}{W_{eff} L_{eff} f^{EF_N^* 2} \cdot 10^{10}}$$

The total flicker noise density is:

$$S_{id}(f) = \frac{S_{id, inv}(f) \times S_{id, insubvt}(f)}{S_{id, inv}(f) + S_{id, insubvt}(f)}$$

BSIM3 SOI Version 3.2 Updates — Thermal Noise Models

There are two channel thermal noise models in BSIMSOI3.2 version. One is the charge based model (default) similar to that used in BSIMSOI3.1. The other is the holistic model. These two models can be selected through the model selector tnoiMod.

- tnoiMod = 0 (charge based)

The noise current is given by:

Chapter 2: MOSFET Models

LEVEL 57: BSIM3 SOI Model

$$\overline{i_d^2} = \frac{4k_B T \Delta f}{L_{eff}^2} \cdot NT NOI, \\ R_{ds} + \frac{\mu_{eff} |Q_{inv}|}{\overline{i_d^2}}$$

where R_{ds} is the source/drain resistance, and the parameter $NT NOI$ is introduced from more accurate fitting of short-channel devices. Q_{inv} is the inversion channel charge computed from the capacitance models.

- $troiMod = 1$ (holistic)

In this thermal noise model, all the short-channel effects and velocity saturation effects incorporated in the IV model are automatically included, hence the name “holistic thermal noise model.” In addition, the amplification of the channel thermal noise through G_m and G_{mbs} as well as the induced-gate noise with partial correlation to the channel thermal noise are all captured in the new “noise partition” model.

The noise voltage source partitioned to the source side is given by:

$$\overline{v_d^2} = 4k_B T \cdot \theta_{moi}^2 \cdot \frac{V_{ds eff} \Delta f}{I_{ds}}$$

and the noise current source put in the channel region with gate and body amplification is given by:

$$\overline{i_d^2} = 4k_B T \frac{V_{ds eff} \Delta f}{I_{ds}} [G_{ds} + \beta_{moi} \cdot (G_m + G_{mbs})]^2 - \overline{v_d^2} \cdot (G_m + G_{ds} + G_{mbs})^2$$

where

$$\theta_{moi} = RNOIB \left[1 + TNOIB \cdot L_{eff} \left(\frac{V_{gsteff}}{E_{sat} L_{eff}} \right)^2 \right]$$

$$\beta_{moi} = RNOIA \left[1 + TNOIA \cdot L_{eff} \left(\frac{V_{gsteff}}{E_{sat} L_{eff}} \right)^2 \right]$$

BSIM3 SOI Version 3.2 Updates — Model Parameters

| Symbols Used in Equation | Symbol used in SPICE | Description | Unit | Default |
|--------------------------|----------------------|--|------|-----------------|
| SoiMod | SoiMod | SOI model selector (instance) SoiMOD=0 BSIMPD SoiMOD=1 Unified model for PD & FD SoiMod=2 ideal FD SoiMod=3 Auto selection by SIMSOI | - | 0 |
| T _{OXM} | toxm | Gate oxide thickness used in extraction | μ | T _{ox} |
| N _{OFF} | noff | CV parameter for V _{gesteff,cv} | - | 1.0 |
| V _{bs0fd} | vbs0fd | Upper bound of built-in potential lowering for ideal FD operation | V | 0.0 |
| V _{bs0fd} | vbs0fd | Lowering bound of built- in potential lowering for ideal FD operation | V | 0.5 |
| fnoiMod | fnoiMod | Flicker noise model selector | - | 1 |
| troiMod | tnoiMod | Thermal noise model selector | - | 0 |
| NTNOI | ntnoi | Noise factor for short-channel devices for TNOIMOD=0 only | - | 1.0 |
| TNOIA | tnoia | Coefficient of channel-length dependence of total channel thermal noise | - | 1.5 |
| TNOIB | tnoib | Channel-length dependence parameter for channel thermal noise partitioning | - | 3.5 |
| RNOIA | rnoia | Thermal noise parameter | | 0.577 |
| RNOIB | rnoib | Thermal noise parameter | | 0.37 |

BSIM3 SOI Version 3.1 Updates

In addition to BSIMSOI3.0, the MOSFET Level 57 model also supports the UCB BSIMSOI3.1 model version, which includes the following new features that are not available in BSMISOI3.0.

This section covers the following topics:

- [BSIM3 SOI Version 3.1 Updates — Ideal Full-Depletion \(FD\) Modeling](#)
- [BSIM3 SOI Version 3.1 Updates — Gate Resistance Modeling](#)

Chapter 2: MOSFET Models

LEVEL 57: BSIM3 SOI Model

- [BSIM3 SOI Version 3.1 Updates — Gate Resistance Equivalent Circuit](#)
- [BSIM3 SOI Version 3.1 Updates — Enhanced Binning Capability](#)

BSIM3 SOI Version 3.1 Updates — Ideal Full-Depletion (FD) Modeling

BSIMSOI3.0 supports the modeling of these two families of SOI MOSFETs with a SOIMOD switching model flag.

- SOIMOD=0 for partially depleted devices (PD).
- SOIMOD=1 for devices that tend to operate in a mixed mode of PD and FD.

V3.1 also provides an ideal full-depletion (FD) module (SOIMOD=2), not available in V3.0 to model FD SOI devices that literally exhibit no floating-body behavior. As in BSIMSOI3.0, the default SOIMOD value is 0 for BSIMSOI3.1.

The following physical modeling components, related to the internal SOI body node, are critical for accurately modeling PD SOI devices, but are not needed for the ideal FD module. Thus, for the ideal FD module, HSPICE ignores these components, which makes SOI MOSFET modeling much easier than for PD devices, or non-ideal FD devices.

- Source/Drain to body diode currents
- Source-Body-Drain parasitic BJT currents
- Impact ionization currents
- Gate-body direct currents
- Body-related capacitances.

BSIM3 SOI Version 3.1 Updates — Gate Resistance Modeling

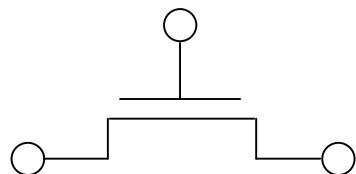
BSIMSOI3.1 uses the same gate resistance models as in the BSIM4 model with four options for various gate-resistance modeling topologies.

| Name | Unit | Default | Bin | Description |
|----------|--------|---------|-----|--|
| NGCON | - | - | N | Number of gate contacts |
| RGATEMOD | - | 0 | N | Gate resistance model selector <ul style="list-style-type: none">■ RGATEMOD=0: No gate resistance■ RGATEMOD=1: Constant gate resistance■ RGATEMOD=2: Rii model with variable resistance■ RGATEMOD=3: Rii model with two nodes |
| RSHG | Ohm/Sq | 0.1 | N | Gate electrode sheet resistance |
| XGL | m | 0 | N | Offset of the gate length due to variations in patterning |

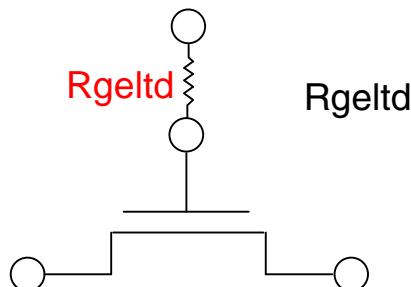
| Name | Unit | Default | Bin | Description |
|--------|------|---------|-----|---|
| XGW | m | 0 | N | Distance from the gate contact to the channel edge in the W direction |
| XRCRG1 | - | 12 | Y | Parameter for distributed channel-resistance effect for intrinsic input resistance |
| XRCRG2 | - | 1 | Y | Parameter to account for the excess channel diffusion resistance for intrinsic input resistance |

BSIM3 SOI Version 3.1 Updates — Gate Resistance Equivalent Circuit

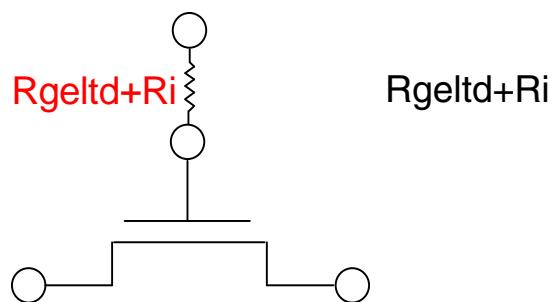
RGATEMOD=0: No gate resistance (default)



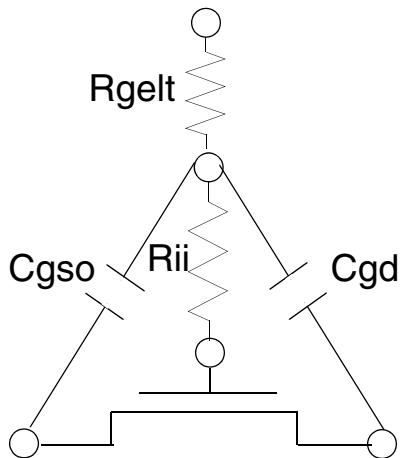
RGATEMOD=1: Constant gate resistance



RGATEMOD=2: variable resistance with Rii model



RGATEMOD=3: Rii model with two nodes



Rgeltd: (Poly) gate electrode resistance, bias independent.

Rii: Intrinsic input gate resistance, reflected to the gate from the intrinsic channel region. It is bias-dependent and a first-order non-quasi static model for RF and rapid transient MOSFET operations.

BSIM3 SOI Version 3.1 Updates — Enhanced Binning Capability

Model parameters for the following components are now binnable for better accuracy and scalability:

- Junction depth
- Gate-tunneling current
- Temperature dependence of threshold voltage, mobility, saturation velocity, parasitic resistance, and diode currents.

Bug Fixes:

The BSIMSOI3.1 from UC Berkeley fixes the following bugs in the BSIMSOI3.0 model:

- The model now takes NSEG into account when calculating the gate-channel tunneling current.
- The GMIN connecting gate and drain is now multiplied by 1e-6 to reduce false leakage current.
- A swapping error in the source/drain overlap capacitance stamping.
- The bulk charge effect coefficient (A_{bulkCV}) is now corrected for Q_{inv} and its derivatives in CAPMOD=2 .

BSIM3 SOI Model — PD Version Updates

- BSIM PD version 2.2 enhances the model flexibility and accuracy from PD version 2.0, and the following are its major features.
 - Gate-body tunneling (substrate current) enhances the model accuracy.
 - Body contact resistance improves the modeling accuracy.
 - Binning enhances the model flexibility.
- BSIM PD version 2.21 updates the PD version 2.2 for bug fixes and S/D swapping for the gate current components.
- BSIM PD version 2.22 updates the 2.21 version for bug fixes and enhancements. The major features include:
 - FRBODY instance parameter
 - Improved temperature dependence of the gate direct tunneling model
 - Two new model parameters, VEVB and VECB
 - UC Berkeley code no longer supports the NECB and NEVB model parameters. Version 2.22 accepts these parameters for backwards compatibility, but they have no effect.
- .OPTION LIST prints an element summary for the MOSFET Level=57 model.

| Element | Description |
|---------|--|
| bjtoff | BJT on/off flag (Turn off BJT if equal to 1) |
| rth0 | Thermal Resistance per unit width |
| cth0 | Thermal Capacitance per unit width |
| nrb | Number of squares for the body series resistance |
| frbody | Coefficient of the distributed body resistance effects |
| nbc | Number of body contact isolation edge |
| nseg | Number of segments for channel width partitioning |
| pdbc | Parasitic perimeter length for the body contact at the drain side |
| psdbc | Parasitic perimeter length for the body contact at the source side |

Chapter 2: MOSFET Models

LEVEL 57: BSIM3 SOI Model

| Element | Description |
|---------|---|
| agbcp | Parasitic gate-to-body overlap area for the body contact |
| aebcp | Parasitic body-to-substrate overlap area for the body contact |
| vbsusr | Optional initial value of Vbs, which you specify for transient analysis |

- BSIM PD version 2.23 includes several bug fixes and enhancements from version 2.2.
 - Adds geometric dependency in CV delta L and delta W .
 - Fixes a gate-body-tunneling residue problem in the low-bias region.
 - Provides an additional parameter (dtoxcv) in CAPMOD=3 for flexibility
 - Other bug fixes

Using BSIM3 SOI PD Model

To use BSIM3-SOI PD versions 2.0, 2.2, 2.21, or 2.22 in simulation, apply the VERSION model parameter. For example:

- Invokes PD2.0 if VERSION=2.0
- Invokes PD2.2 and PD2.21 if VERSION=2.2
- Invokes PD2.22 if VERSION=2.22
- Invokes PD2.23 if VERSION=2.23.

For gate-body tunneling, set the IGMOD model parameter to 1.

Example:

```
mckt drain gate source bulk nch L=10e-6 W=10e-6
.model nch nmos Level=57 igmod=1 version=2.2
+ tnom=27 tox=4.5e-09 tsi=.0000001 tbox=8e-08
+ mobmod=0 capmod=2 shmod=0 paramchk=0
+ wint=0 lint=-2e-08 vth0=.42 k1=.49
+ k2=.1 k3=0 k3b=2.2 nlx=2e-7
+ dvt0=10 dvt1=.55 dvt2=-1.4 dvt0w=0
+ dvt1w=0 dvt2w=0 nch=4.7e+17 nsub=-1e+15
+ ngate=1e+20 agidl=1E-15 bgidl=1E9 ngidl=1.1
+ ndiode=1.13 ntun=14.0 nrecf0=2.5 nrecr0=4
+ vrec0=1.2 ntrecf=.1 ntrecr=.2 isbjt=1E-4
+ isdif=1E-5 istun=2E-5 isrec=4E-2 xbjt=.9
+ xdif=.9 xrec=.9 xtun=0.01 ahli=1e-9
+ lbjt0=0.2e-6 ln=2e-6 nbjt=.8 ndif=-1
+ aely=1e8 vabjt=0 u0=352 ua=1.3e-11
+ ub=1.7e-18 uc=-4e-10 w0=1.16e-06 ags=.25
+ A1=0 A2=1 b0=.01 b1=10
+ rdsw=0 prwg=0 prwb=-.2 wr=1
+ rbody=1E0 rbsh=0.0 a0=1.4 keta=0.1
+ ketas=0.2 vsat=135000 dwg=0 dwb=0
+ alpha0=1e-8 beta0=0 beta1=0.05 beta2=0.07
+ vdsatii0=.8 esatii=1e7 voff=-.14 nfactor=.7
+ cdsc=.00002 cdscb=0 cdscd=0 cit=0
+ pclm=2.9 pvag=12 pdiblc1=.18 pdiblc2=.004
+ pdiblcb=-.234 drout=.2 delta=.01 eta0=.05
+ etab=0 dsub=.2 rth0=.005 clc=.0000001
+ cle=.6 cf=1e-20 ckappa=.6 cgdl=1e-20
+ cgsl=1e-20 kt1=-.3 kt1l=0 kt2=.022
+ ute=-1.5 ua1=4.31e-09 ub1=-7.61e-18 uc1=-5.6e-11
+ prt=760 at=22400 cgso=1e-10 cgdo=1e-10
+ cjswg=1e-12 tt=3e-10 asd=0.3 csdesw=1e-12
+ tcjswg=1e-4 mjswg=.5 pbswg=1
```

BSIM3 SOI Model — Output Templates

For a list of output template parameters in the MOSFET models, and which parameters this model supports, see [MOSFET Output Templates](#).

LEVEL 58: UFSOI MOSFET Model

University of Florida SOI includes non-fully depleted (NFD) and fully depleted (FD) SOI models (a dynamic mode must not operate between NFD and FD) that separately describe two main types of SOI devices. The UFSOI version 4.5F model is Level 58 in the Synopsys MOSFET models.

Some processes use an external contact to the body of the device. The Synopsys MOSFET model supports only a 4-terminal device, which includes drain, front gate, source, and back gate (or substrate). The additional body contact is currently not supported so it floats.

The effects of parasitic diodes in SOI are different from those in the bulk MOSFET. The SOI model does not include the MOSFET *junction* model (ACM), developed for bulk MOSFETs.

The general syntax for MOSFET Level 58 in a netlist is:

```
Mxxx nd ngf ns [ngb] mname [L=val] [W=val] [M=val]
+ [AD=val] [AS=val] [PD=val] [PS=val] [NRD=val]
+ [NRS=val] [NRB=val] [RTH=val] [CTH=val] [off]
+ [IC=Vds, Vgfs, VGbs]
```

In the preceding syntax, angle brackets denote optional parameters. The arguments are identical to those for the BSIM3-SOI model, but the thermal resistance and capacitance have different names.

Table 1 Thermal Resistance and Capacitance Names

| Name | Description |
|------|--|
| CTH | Thermal capacitance, unit in $\text{W} \cdot \text{s} \cdot \text{K}^{-1}$, default is 0.0. |
| RTH | Thermal resistance, unit in $\text{K} \cdot \text{W}^{-1}$, default is 0.0. |

Note: Following are some important notes:

- The default value for channel length (L) and width (W) is 1.0e-6.
- The present version supports only 4 nodes (only floating-body devices). AB is typically zero; specify it accordingly.

- If you activate the self-heating option (on the model line), RTH and CTH define the thermal impedance of the device. Typical values are 5e3 (for RTH) and 1e-12 (for CTH), but these can vary widely from one device to another.
- For M>1, you must specify W, AD, AS, NRD, NRS, NRB, PDJ, PSJ, RTH, and CTH per gate finger.
- The initial condition (IC) is in the following order: V_{ds} drain voltage, V_{gfs} front gate voltage, and V_{bgs} back gate voltage.

This section covers the following topics:

- [UFSOI Model — FDSOI Parameters](#)
- [UFSOI Model — NFDSOI Parameters](#)
- [UFSOI MOSFET Model Template](#)

UFSOI Model — FDSOI Parameters

The following tables describe Level 58 model parameters for the fully depleted (FD) SOI, including parameter names, descriptions, units, defaults, and typical notes.

This section covers the following topics:

- [FDSOI Flag Parameters](#)
- [FDSOI Structural Parameters](#)
- [FDSOI Electrical Parameters](#)
- [FDSOI Optional Parameters](#)

FDSOI Flag Parameters

| Parameter | Unit | Default | Typical Value | Description |
|-----------|------|---------|---------------|--|
| Level | - | - | - | Level 57 for UFSOI |
| NFDMOD | - | 0 | 0 | Model selector (0: FD) |
| BJT | - | 1 | 1 | Parasitic bipolar flag (0: off; 1: on) |

Chapter 2: MOSFET Models
 LEVEL 58: UFSOI MOSFET Model

| Parameter | Unit | Default | Typical Value | Description |
|-----------|------|---------|---------------|--|
| SELFT | - | 0 | 0 | Self-heating flag: <ul style="list-style-type: none"> ■ 0: no self-heating ■ 1: approximate model ■ 2: full self-heating |
| TPG | - | 1 | - | Type of gate polysilicon: <ul style="list-style-type: none"> ■ +1: opposite to body ■ -1: same as body |
| TPS | - | -1 | - | Type of substrate: <ul style="list-style-type: none"> ■ +1: opposite to body ■ -1: same as body |

FDSOI Structural Parameters

| Parameter | Unit | Default | Typical Value | Description |
|-----------|------|---------|-------------------|---|
| DL | m | 0.0 | (0.05-0.15)x10-6 | Channel-length reduction |
| DW | m | 0.0 | (0.1-0.5)x10-6 | Channel-width reduction |
| LLDD | m | 0.0 | (0.05-0.2)x10-6 | LDD/LDS region length (0 for no LDD) |
| NBODY | cm-3 | 5.0e16 | 1017 -1018 | Film (body) doping density |
| NDS | cm-3 | 5.0e19 | 1019 -1020 | Source/drain doping density |
| NGATE | cm-3 | 0.0 | 1019 -1020 | Poly-gate doping density (0 for no poly-gate depletion) |
| NLDD | cm-3 | 5.0e19 | 1x1019 | LDD/LDS doping density (>1e19: LDD/LDS treated as D/S extensions) |
| NSUB | cm-3 | 1.0e15 | 1015 -1017 | Substrate doping density |
| TB | m | 0.1e-6 | (30-100) x10-9 | Film (body) thickness |

| Parameter | Unit | Default | Typical Value | Description |
|-----------|------|---------|---------------------------|----------------------------|
| TOXB | m | 0.5e-6 | (80-400)x10 ⁻⁹ | Back-gate oxide thickness |
| TOXF | m | 1.0e-8 | (3-8)x10 ⁻⁹ | Front-gate oxide thickness |

FDSOI Electrical Parameters

| Parameter | Unit | Default | Typical Value | Description |
|-----------|---------------------|---------|--|---|
| ALPHA | cm ⁻¹ | 0.0 | 2.45x10 ⁶ | Impact-ionization coefficient (0 for no impact ionization) |
| BETA | V· cm ⁻¹ | 0.0 | 1.92x10 ⁶ | Impact-ionization exponential factor (0 for no impact ionization) |
| BGIDL | V· cm ⁻¹ | 0.0 | (4-8)x10 ⁹ | Exponential factor for gate-induced drain leakage (0 for no GIDL) |
| CGFBO | F· m ⁻¹ | 0.0 | 0.0 | Gate-body overlap capacitance |
| CGFDO | F· m ⁻¹ | 0.0 | 1x10 ⁻¹⁰ | Gate-drain overlap capacitance |
| CGFSO | F· m ⁻¹ | 0.0 | 1x10 ⁻¹⁰ | Gate-source overlap capacitance |
| FNA | - | 1.0 | 0.5-2 | Flicker noise exponent |
| FNK | F· A | 0.0 | 0-10 ⁻² | Flicker noise coefficient |
| GAMMA | - | 0.3 | 0.3-1.0 | BOX fringing field weighting factor |
| JRO | A· m ⁻¹ | 1.0e-10 | 10 ⁻¹¹ -10 ⁻⁹ | Body-source/drain junction recombination current coefficient |
| KAPPA | - | 0.5 | 0.5-1.0 | BOX fringing field weighting factor |
| LDIFF | m | 1.0e-7 | (0.1-0.5)x10 ⁻⁶ | Effective diffusion length in source/drain |

Chapter 2: MOSFET Models
LEVEL 58: UFSOI MOSFET Model

| Parameter | Unit | Default | Typical Value | Description |
|-----------|---|----------|---------------------------------|--|
| M | - | 2.0 | 1.0-2.0 | Body-source/drain junction recombination ideality factor |
| NQFB | cm ⁻² | 0.0 | ~ 1011 | Back oxide fixed charge (normalized) |
| NQFF | cm ⁻² | 0.0 | ~ 1010 | Front oxide fixed charge (normalized) |
| NQFSW | cm ⁻² | 0.0 | ~ ± 1012 | Effective sidewall fixed charge (0 for no narrow-width effect) |
| NSB | cm ⁻² . eV-1 | 0.0 | ~ 1011 | Back surface state density |
| NSF | cm ⁻² . eV-1 | 0.0 | ~1010 | Front surface state density |
| QM | - | 0.0 -0.5 | | Energy quantization parameter (0 for no quantization) |
| RD | ohm· m | 0.0 | 200-1000 | Specific drain parasitic resistance |
| RHOB | ohm/sq. | 0.0 | 30x103 | Body sheet resistance |
| RS | ohm· m | 0.0 | 200-1000 | Specific source parasitic resistance |
| SEFF | cm· s-1 | 1.0e5 | (0.5-5)x105 | Effective recombination velocity in source/drain |
| THETA | cm· V-1 | 7.0e2 | (0.1-3)x10-6 | Mobility degradation coefficient |
| UO | cm ² . V ⁻¹ . s-1 | 7.0e2 | 200-700 (nMOS) 70-400 (pMOS) | Low-field mobility |
| VSAT | cm· s-1 | 1.0e-6 | (0.5-1)x10 | Carrier saturated drift velocity |

FDSOI Optional Parameters

| Parameter | Unit | Default | Typical Value | Description |
|-----------|------|---------|---------------|---|
| BFACT | - | 0.3 | 0.1-0.5 | V _{DS} averaging factor for mobility degradation |

| Parameter | Unit | Default | Typical Value | Description |
|-----------|---------|---------|-----------------------|---|
| FVBJT | - | 0.0 | 0-1 | BJT current directional partitioning factor (0 for lateral 1D flow) |
| RHOSD | ohm/sq. | 0.0 | 50 | Source/drain sheet resistance |
| TAUO | s | calc. | 10-7 -10-5 | Carrier lifetime in lightly doped regions |
| VFBB | V | calc. | - | Back-gate flatband voltage |
| VFBF | V | calc. | -1 (nMOS) 1 (pMOS) | Front-gate flatband voltage |
| WKB | V | calc. | - | Back-gate work function difference |
| WKF | V | calc. | ~ VFBF | Front-gate work function difference |

UFSOI Model — NFDSOI Parameters

The following tables describe the Level 58 model parameters for non fully depleted (NFD) SOI, including parameter names, descriptions, units, defaults, and typical notes.

This section covers the following topics:

- [NFDSOI Flag Parameters](#)
- [NFDSOI Structural Parameters](#)
- [NFDSOI Electrical Parameters](#)
- [NFDSOI Optional Parameters](#)

NFDSOI Flag Parameters

| Parameter | Unit | Default | Typical Value | Description |
|-----------|------|---------|---------------|--|
| Level | - | - | - | Level 57 for UFSOI |
| BJT | - | 1 | 1 | Parasitic bipolar flag: ■ 0: off ■ 1: on |
| NFDMOD | - | 0 | - | Model selector (1: NFD) |

Chapter 2: MOSFET Models

LEVEL 58: UFSOI MOSFET Model

| Parameter | Unit | Default | Typical Value | Description |
|-----------|------|---------|---------------|--|
| SELFT | - | 0 | 0 | Self-heating flag: ■ 0: no self-heating ■ 1: approximate model ■ 2: full self-heating |
| TPG | - | 1 | 1 | Type of gate polysilicon ■ +1: opposite to body ■ -1: same as body |
| TPS | - | -1 | -1 | Type of substrate ■ +1: opposite to body ■ -1: same as body) |

NFDSOI Structural Parameters

| Parameter | Unit | Default | Typical Value | Description |
|-----------|------|---------|------------------|--|
| DL | m | 0.0 | (0.05-0.15)x10-6 | Channel-length reduction |
| DW | m | 0.0 | (0.1-0.5)x10-6 | Channel-width reduction |
| LLDD | m | 0.0 | (0.05-0.2)x10-6 | LDD/LDS region length (0 for no LDD) |
| LRSC | m | 0.0 | ~0.1x10-6 | Characteristic length for reverse short-channel effect (0 for no RSCE) |
| NBH | cm-3 | 5.0e17 | 1019 -1020 | Halo doping density |
| NBL | cm-3 | 5.0e16 | 1017 -1018 | Low body doping density |
| NDS | cm-3 | 5.0e19 | 1019 -1020 | Source/drain doping density |
| NGATE | cm-3 | 0.0 | 1019 -1020 | Poly-gate doping density (0 for no poly-gate depletion) |
| NHALO | cm-3 | - | ~1018 | Halo doping density |

| Parameter | Unit | Default | Typical Value | Description |
|-----------|------|---------|---------------|--|
| NLDD | cm-3 | 5.0e19 | 1x1019 | LDD/LDS doping density (>1e19: LDD/LDS treated as D/S extensions) |
| NSUB | cm-3 | 1.0e15 | 1015 -1017 | Substrate doping density |
| TB | m | 0.1e-6 | (30-100)x10-9 | Film (body) thickness |
| TF | m | 0.2e-6 | (3-8)x10-9 | Silicon film thickness |
| THALO | m | 0.0 | - | Halo thickness (0 for no halo) |
| TOXB | m | 0.5e-6 | (80-400)x10-9 | Back-gate oxide thickness |
| TOXF | m | 1.0e-8 | (3-8)x10-9 | Front-gate oxide thickness |

NFDSOI Electrical Parameters

| Parameter | Unit | Default | Typical Value | Description |
|-----------|---------|---------|---------------|---|
| ALPHA | cm-1 | 0.0 | 2.45x106 | Impact-ionization coefficient (0 for no impact ionization) |
| BETA | V· cm-1 | 0.0 | 1.92x106 | Impact-ionization exponential factor (0 for no impact ionization) |
| BGIDL | V· cm-1 | 0.0 | (4-8)x109 | Exponential factor for gate-induced drain leakage (0 for no GIDL) |
| CGFBO | F· m-1 | 0.0 | 0.0 | Gate-body overlap capacitance |
| CGFDO | F· m-1 | 0.0 | 1x10-10 | Gate-drain overlap capacitance |
| CGFSO | F· m-1 | 0.0 | 1x10-10 | Gate-source overlap capacitance |
| FNA | - | 1.0 | 0.5-2 | Flicker noise exponent |
| FNK | F· A | 0.0 | 0-10-2 | Flicker noise coefficient |

Chapter 2: MOSFET Models

LEVEL 58: UFSOI MOSFET Model

| Parameter | Unit | Default | Typical Value | Description |
|-----------|---|----------|---------------------------------------|--|
| JRO | A· m-1 | 1.0e-10 | 10-11 -10-9 | Body-source/drain junction recombination current coefficient |
| LDIFF | m | 1.0e-7 | (0.1-0.5)x10-6 | Effective diffusion length in source/drain |
| M | - | 2.0 | 1.0-2.0 | Body-source/drain junction recombination ideality factor |
| NQFB | cm ⁻² | 0.0 | ~ 10 ¹¹ | Back oxide fixed charge (normalized) |
| NQFF | cm ⁻² | 0.0 | ~ 10 ¹⁰ | Front oxide fixed charge (normalized) |
| NQFSW | cm ⁻² | 0.0 | ~ ± 10 ¹² | Effective sidewall fixed charge (0 for no narrow-width effect) |
| NTR | cm ⁻³ | 0.0 | 10 ¹⁴ -10 ¹⁵ | Effective trap density for trap-assisted junction tunneling (0 for no tunneling) |
| QM | - | 0.0 -0.5 | | Energy quantization parameter (0 for no quantization) |
| RD | ohm· m | 0.0 | 200-1000 | Specific drain parasitic resistance |
| RHOB | ohm/sq. | 0.0 | 30x10 ³ | Body sheet resistance |
| RS | ohm· m | 0.0 | 200-1000 | Specific source parasitic resistance |
| SEFF | cm· s-1 | 1.0e5 | (0.5-5)x10 ⁵ | Effective recombination velocity in source/drain |
| THETA | cm· V-1 | 7.0e2 | (0.1-3)x10 ⁻⁶ | Mobility degradation coefficient |
| UO | cm ² . V ⁻¹ . s ⁻¹ | 7.0e2 | 200-700 (nMOS) 70-400 (pMOS) | Low-field mobility |

| Parameter | Unit | Default | Typical Value | Description |
|-----------|---------------------|---------|---------------|----------------------------------|
| VSAT | cm· s ⁻¹ | 1.0e-6 | (0.5-1)x10 | Carrier saturated drift velocity |

NFDSOI Optional Parameters

| Parameter | Unit | Default | Typical Value | Description |
|-----------|---------|---------|---------------------------------------|---|
| VFBF | V | calc. | -1 (nMOS) 1 (pMOS) | Front-gate flatband voltage |
| VFBB | V | calc. | - | Back-gate flatband voltage |
| WKF | V | calc. | ~ VFBF | Front-gate work function difference |
| WKB | V | calc. | - | Back-gate work function difference |
| TAUO | s | calc. | 10 ⁻⁷ -10 ⁻⁵ | Carrier lifetime in lightly doped regions |
| BFACT | - | 0.3 | 0.1-0.5 | V_{DS} -averaging factor for mobility degradation |
| FVBJT | - | 0.0 | 0-1 | BJT current directional partitioning factor (0 for lateral 1D flow) |
| RHOSD | ohm/sq. | 0.0 | 50 | Source/drain sheet resistance |

Note: Following are some important notes:

- The model line must include LEVEL=58 and NFDMOD=0 for FD, or NFDMOD=1 for NFD devices.
- Specifying VFBF turns off the narrow-width effect defined by NQFSW (which can be positive or negative) and the reverse short-channel effect defined by LRSCE (and NBH or NHALO if specified); the latter effect is also turned off if you specify WKF.
- For floating-body devices, CGFBO is small; you should set it to 0.

Chapter 2: MOSFET Models

LEVEL 58: UFSOI MOSFET Model

- `JRO` and `SEFF` influence the gain of the BJT, but `LDIFF` affects only bipolar charge storage in the source/drain. If you specify `THALO`, then `NBH` and `NHALO` also influence the BJT gain.
- Loosely correlate the `TAUO` value with `JRO` in accord with basic pn-junction recombination/generation properties. Its default value is based on `JRO`, which is appropriate for short L; for long L, body generation predominates over that in the junctions so specify `TAUO`.
- The non-local impact-ionization model is physical so do not arbitrarily vary its parameters.
- The `LDD` option intensifies the model so set `LLDD` to 0 for large-scale circuit simulation, and add the unbiased `LDD` resistance to `RD`; this simplification stops if you specify `NLDD > 1e19`.

UFSOI MOSFET Model Template

For a list of output template parameters in the MOSFET models, and which parameters this model supports, see [MOSFET Output Templates](#).

LEVEL 59: BSIM3 SOI FD Model

The UC Berkeley SOI (BSIM3-SOI) Fully Depleted (FD) model is Level 59 in the Synopsys MOSFET models. For a description of this model, see the *BSIM3SOI FD2.1 MOSFET MODEL User Manual*, at:

<http://www-device.eecs.berkeley.edu/~bsim3soi>

The following sections discuss these topics:

- [BSIM3 SOI FD Model — General Syntax](#)
 - [BSIM3 SOI FD Model Parameters](#)
 - [BSIM3 SOI FD Model — Template Output](#)
-

BSIM3 SOI FD Model — General Syntax

Syntax:

```
Mxxx nd ng ns ne [np] mname [L=val]
+ [W=val] [M=val] [AD=val] [AS=val] [PD=val] [PS=val]
+ [NRD=val] [NRS=val] [NRB=val] [RTH0=val] [CTH0=val]
+ [off] [BJTOff=val] [IC=Vds, Vgs, Vbs, Ves, Vps]
```

| Parameter | Description |
|-----------|--|
| Mxxx | SOI MOSFET element name. Must begin with M, followed by up to 1023 alphanumeric characters. |
| nd | Drain terminal node name or number. |
| ng | Front gate node name or number. |
| ns | Source terminal node name or number. |
| ne | Back gate (or substrate) node name or number. |
| np | Optional external body contact node name or number. |
| mname | MOSFET model name reference. |
| L | SOI MOSFET channel length in meters. This parameter overrides DEFL in an OPTIONS statement. Default=DEFL with a maximum of 0.1m. |
| W | MOSFET channel width in meters. This parameter overrides DEFW in an OPTIONS statement. Default=DEFW. |

Chapter 2: MOSFET Models

LEVEL 59: BSIM3 SOI FD Model

| Parameter | Description |
|-----------|--|
| M | Multiplier to simulate multiple SOI MOSFETs in parallel. The M setting affects all channel widths, diode leakages, capacitances, and resistances. Default=1. |
| AD | Drain diffusion area. Overrides DEFAD in the OPTIONS statement. Default=DEFAD. |
| AS | Source diffusion area. Overrides DEFAS in the OPTIONS statement. Default=DEFAS. |
| PD | Perimeter of the drain junction, including the channel edge. Overrides DEFPD in the OPTIONS statement. |
| PS | Perimeter of the source junction, including the channel edge. Overrides DEFPS in the OPTIONS statement. |
| NRD | Number of squares of drain diffusion for the drain series resistance. Overrides DEFNRD in the OPTIONS statement. |
| NRS | Number of squares of source diffusion for the source series resistance. Overrides DEFNRS in the OPTIONS statement. |
| NRB | Number of squares for the body series resistance. |
| RTH0 | Thermal resistance per unit width: <ul style="list-style-type: none">■ If you do not specify RTH0, simulation extracts it from the model card.■ If you specify RTH0, it overrides RTH0 in the model card. |
| CTH0 | Thermal capacitance per unit width <ul style="list-style-type: none">■ If you do not specify CTH0, simulation extracts it from the model card.■ If you specify CTH0, it overrides CTH0 in the model card. |
| OFF | Sets the initial condition to OFF for this element in DC analysis. |
| BJTOFF | Turns off BJT if equal to 1. |
| IC | Initial guess in the order (drain, front gate, internal body, back gate, external voltage). (ignores Vps in a 4-terminal device) Simulation uses these settings if you specify UIC in the .TRAN statement. The .IC statement overrides them. |

BSIM3 SOI FD Model Parameters

This section covers the following topics:

- [BSIM3 SOI FD Model — Control Parameters](#)
- [BSIM3 SOI FD Model — Process Parameters](#)
- [BSIM3 SOI FD Model — DC Parameters](#)

- [BSIM3 SOI FD Model — AC and Capacitance Parameters](#)
- [BSIM3 SOI FD Model — Temperature Parameters](#)

BSIM3 SOI FD Model — Control Parameters

| Parameter | Unit | Default | Description |
|-----------|------|---------|---|
| CAPMOD | - | 2 | Flag for the short channel capacitance model |
| Level | - | - | Level 59 for BSIM3SOI |
| MOBMOD | - | 1 | Mobility model selector |
| NOIMOD | - | 1 | Flag for the Noise model |
| SHMOD | - | 0 | Flag for self-heating: ■ 0=no self-heating ■ 1=self-heating |

BSIM3 SOI FD Model — Process Parameters

| Parameter | Unit | Default | Description |
|-----------|-------------------|---------|--------------------------------|
| NCH | 1/cm ³ | 1.7e17 | Channel doping concentration |
| NGATE | 1/cm ³ | 0 | Poly gate doping concentration |
| NSUB | 1/cm ³ | 6.0e16 | Substrate doping concentration |
| TBOX | m | 3.0e-7 | Buried oxide thickness |
| TOX | m | 1.0e-8 | Gate oxide thickness |
| TSI | m | 1.0e-17 | Silicon film thickness |

BSIM3 SOI FD Model — DC Parameters

| Parameter | Unit | Default | Description |
|-----------|------|---------|---|
| A0 | - | 1.0 | Bulk charge effect coefficient for the channel length |
| A1 | 1/V | 0.0 | First non-saturation effect parameter |
| A2 | - | 1.0 | Second non-saturation effect parameter |

Chapter 2: MOSFET Models
 LEVEL 59: BSIM3 SOI FD Model

| Parameter | Unit | Default | Description |
|-----------|------------------|---------|--|
| ABP | - | 1.0 | Coefficient of A_{beff} dependency on V_{gst} |
| ADICE0 | - | 1 | DICE bulk charge factor |
| AGIDL | 1/W | 0.0 | GIDL constant |
| AGS | 1/V | 0.0 | Gate bias coefficient of A_{bulk} |
| All | 1/V | 0.0 | First Vdsatii parameter for the Leff dependence |
| ALPHA0 | m/V | 0.0 | First parameter of the impact ionization current |
| ALPHA1 | 1/V | 1.0 | Second parameter of the impact ionization current |
| B0 | m | 0.0 | Bulk charge effect coefficient for the channel width |
| B1 | m | 0.0 | Width offset for the bulk charge effect |
| BGIDL | V/m | 0.0 | GIDL exponential coefficient |
| BII | m/V | 0.0 | Second Vdsatii parameter for the Leff dependence |
| CDSC | F/m ² | 2.4e-4 | Drain/source to the channel coupling capacitance |
| CDSCB | F/m ² | 0 | Body-bias sensitivity of cdsc |
| CDSCD | F/m ² | 0 | Drain-bias sensitivity of cdsc |
| CII | - | 0.0 | First Vdsatii parameter for the V_{ds} dependence |
| CIT | F/m ² | 0.0 | Interface trap capacitance |
| DELP | V | 0.02 | Constant for limiting V_{bseff} to the surface potential |
| DELTA | - | 0.01 | Effective V_{ds} parameter |
| DII | V | -1.0 | Second Vdsatii parameter for the V_{ds} dependence |
| DROUT | - | 0.56 | L dependence coefficient of the DIBL correction parameter in R_{out} |
| DSUB | - | 0.56 | DIBL coefficient exponent |
| DVBD0 | V | 0 | First coefficient of the V_{ds} 0 dependency on Leff |

| Parameter | Unit | Default | Description |
|-----------|-------------|---------|---|
| DVBD1 | V | 0 | Second coefficient of the V_{ds} 0 dependency on L_{eff} |
| DVT0 | - | 2.2 | First coefficient of the short-channel effect on V_{th} |
| DVT0W | - | 0 | First coefficient of the narrow-width effect on V_{th} for a small channel length |
| DVT1 | - | 0.53 | Second coefficient of the short-channel effect on V_{th} |
| DVT1W | - | 5.3e6 | Second coefficient of the narrow-width effect on V_{th} for a small channel length |
| DVT2 | 1/V | -0.032 | Body-bias coefficient of the short-channel effect on V_{th} |
| DVT2W | 1/V | -0.032 | Body-bias coefficient of the narrow width effect on V_{th} for small channel length |
| DWB | $m/V^{1/2}$ | 0.0 | Coefficient of the substrate body bias dependence for W_{eff} |
| DWG | m/V | 0.0 | Coefficient of the gate dependence for W_{eff} |
| EDL | m | 2e-6 | Electron diffusion length |
| ETA0 | - | 0.08 | DIBL coefficient in the subthreshold region |
| ETAB | 1/V | -0.07 | Body-bias coefficient for the DIBL effect in the subthreshold region |
| ISBJT | A/m^2 | 1.0e-6 | BJT injection saturation current |
| ISDIF | A/m^2 | 0 | Body to source/drain injection saturation current |
| ISREC | A/m^2 | 1.0e-5 | Recombination in the depletion saturation current |
| ISTUN | A/m^2 | 0.0 | Reverse tunneling saturation current |
| K1 | $V^{1/2}$ | 0.6 | Coefficient for the first-order body effect |
| K2 | - | 0 | Coefficient for the second-order body effect |
| K3 | - | 0 | Narrow coefficient |
| K3B | 1/V | 0 | Body-effect coefficient of k3 |
| KB1 | - | 1 | Coefficient of the V_{bs} 0 dependency on V_{gbs} |

Chapter 2: MOSFET Models

LEVEL 59: BSIM3 SOI FD Model

| Parameter | Unit | Default | Description |
|-----------|---------------------------|----------------------|--|
| KB3 | - | 1 | Coefficient of the V_{bs0} dependency on V_{gs} at subthreshold region |
| KBJT1 | m/V | 0 | Parasitic bipolar Early effect coefficient |
| KETA | m | -0.6 | Body-bias coefficient of the bulk charge effect |
| LINT | m | 0.0 | Length-offset fitting parameter from I-V without bias |
| MXC | - | -0.9 | Fitting parameter for calculating A_{beff} |
| NDIODE | - | 1.0 | Diode non-ideality factor |
| NFACTOR | - | 1 | Subthreshold swing factor |
| NGIDL | V | 1.2 | GIDL V_{ds} enhancement coefficient |
| NLX | m | 1.74e-7 | Lateral non-uniform doping parameter |
| NTUN | - | 10.0 | Reverse tunneling non-ideality factor |
| PCLM | - | 1.3 | Channel length modulation parameter |
| PDIBL1 | - | 0.39 | First correction parameter for the DIBL effect of the output resistance |
| PDIBL2 | - | 0.0086 | Second correction parameter for the DIBL effect of the output resistance |
| PRWB | 1/V ¹ | 0 | Body effect coefficient of R_{dsW} |
| PRWG | 1/V ^{1/2} | 0 | Gate bias effect coefficient of R_{dsW} |
| PVAG | | 0.0 | Gate dependence of the Early voltage |
| RBODY | ohm/m ² | 0.0 | Intrinsic body contact sheet resistance |
| RBSH | ohm/m ² | 0.0 | Extrinsic body contact sheet resistance |
| RDSW | $\Omega \cdot \mu m^{wr}$ | 100 | Parasitic resistance per unit width |
| RSH | ohm/square | 0.0 | Source/drain sheet resistance in ohm per square |
| U0 | cm ² /(V·sec) | NMOS-670 PMOS-250 | Mobility at Temp=Tnom |

| Parameter | Unit | Default | Description |
|-----------|--------------------|-----------------------|--|
| UA | m/V | 2.25e-9 | First-order coefficient for mobility degradation |
| UB | (m/V) ² | 5.87e-19 | Second-order coefficient for mobility degradation |
| UC | 1/V | -0.0465 | Body-effect coefficient for mobility degradation |
| VBSA | V | 0 | Transition body voltage offset |
| VOFF | v | -0.08 | Offset voltage in the subthreshold region for large W and L values |
| VSAT | m/sec | 8e4 | Saturation velocity at Temp=Tnom |
| VTH0 | v | NMOS 0.7 PMOS -0.7 | Threshold voltage @ Vbs=0 for a long, wide device |
| W0 | m | 0 | Narrow width parameter |
| WINT | m | 0.0 | Width offset fitting parameter from I-V without bias |
| WR | - | 1 | Width offset from Weff for calculating R _{ds} |

BSIM3 SOI FD Model — AC and Capacitance Parameters

| Parameter | Unit | Default | Description |
|-----------|------------------|------------|--|
| ASD | V | 0.3 | Smoothing parameter for the source/drain bottom diffusion |
| CF | F/m | cal. | Gate to source/drain fringing field capacitance |
| CGDL | F/m | 0.0 | Lightly-doped drain-gate region overlap capacitance |
| CGDO | F/m | calculated | Non-LDD region drain-gate overlap capacitance per channel length |
| CGEO | F/m | 0.0 | Gate-substrate overlap capacitance per channel length |
| CGSL | F/m | 0.0 | Lightly-doped source-gate region overlap capacitance |
| CGSO | F/m | calculated | Non-LDD region source-gate overlap capacitance per channel length |
| CJSWG | F/m ² | 1.e-10 | Source/drain (gate side) sidewall junction capacitance per unit width (normalized to 100nm Ts) |
| CKAPPA | F/m | 0.6 | Coefficient for lightly-doped region overlap capacitance fringing field capacitance |

Chapter 2: MOSFET Models
 LEVEL 59: BSIM3 SOI FD Model

| Parameter | Unit | Default | Description |
|-----------|--------|---------|---|
| CLC | m | 0.1e-7 | Constant term for the short channel model |
| CLE | - | 0.0 | Exponential term for the short channel model |
| CSDESCW | F/m | 0.0 | Source/drain sidewall fringing capacitance per unit length |
| CSDMIN | V | cal. | Source/drain bottom diffusion minimum capacitance |
| DLC | m | lint | Length offset fitting parameter for the gate charge |
| DWC | m | wint | Width offset fitting parameter from C-V |
| MJSWG | V | 0.5 | Source/drain (gate side) sidewall junction capacitance grading coefficient |
| PBSWG | V | 0.7 | Built-in potential for the source/drain (gate side) sidewall junction capacitance |
| TT | second | 1ps | Diffusion capacitance transit time coefficient |
| VSDFB | V | cal. | Flatband voltage for the source/drain bottom diffusion capacitance |
| VSDTH | V | cal. | Threshold voltage for the source/drain bottom diffusion capacitance |

BSIM3 SOI FD Model — Temperature Parameters

| Parameter | Unit | Default | Description |
|-----------|--------------|---------|--|
| XPART | - | 0 | Charge partitioning rate flag |
| AT | m/sec | 3.3e4 | Temperature coefficient for U_a |
| CTH0 | (W*S)/m°C | 0 | Normalized thermal capacity |
| KT1 | V | -0.11 | Temperature coefficient for the threshold voltage |
| KT2 | - | 0.022 | Body-bias coefficient for the temperature effect of the threshold voltage |
| KTIL | V*m | 0 | Channel length dependence of the temperature coefficient for the threshold voltage |
| PRT | Ω -um | 0 | Temperature coefficient for R_{dsw} |

| Parameter | Unit | Default | Description |
|-----------|--------------------|-----------|--|
| RTH0 | m°C/W | 0 | Normalized thermal resistance |
| TNOM | °C | 25 | Temperature at which simulation expects parameters |
| UA1 | m/V | 4.31e-9 | Temperature coefficient for U_a |
| UB1 | (m/V) ² | -7.61e-18 | Temperature coefficient for U_b |
| UC1 | 1/V | -0.056 | Temperature coefficient for U_c |
| UTE | - | -1.5 | Mobility temperature exponent |
| XBJT | - | 1 | Power dependence of j_{bjt} on the temperature |
| XDIF | - | XBJT | Power dependence of j_{dif} on the temperature |
| XREC | - | 1 | Power dependence of j_{rec} on the temperature |
| XTUN | - | 0 | Power dependence of j_{tun} on the temperature |

Note: BSIM3 SOI FD refers the substrate to the silicon below the buried oxide, not to the well region in BSIM3. It calculates the backgate flatband voltage (V_{fbb}) and the parameters related to the bottom capacitance of the source/drain diffusion (V_{sdth} , V_{sdfb} , C_{sdmin}).

- Positive nsub means the same type of doping as the body.
- Negative nsub means opposite type of doping.

BSIM3 SOI FD Model — Template Output

For a list of output template parameters in the MOSFET models, and which parameters this model supports, see [MOSFET Output Templates](#).

LEVEL 60: BSIM3 SOI DD Model

The UC Berkeley SOI model (BSIM3 SOI) supports Fully Depleted (FD), Partially Depleted (PD), and Dynamically Depleted (DD) SOI devices. BSIM3 DD V2.2 for DD SOI devices is Level 60 in the Synopsys MOSFET models. For a description of this model, see the *BSIM3DD2.1 MOSFET MODEL User's Manual*, at <http://www-device.eecs.berkeley.edu/~bsim3>

BSIM3 DD V2.1 includes many advanced concepts for dynamic and continuous transition between PD and FD operation. These concepts are collectively named Dynamic Depletion.

The following sections discuss these topics:

- [BSIM3 SOI DD Model — Features](#)
 - [BSIM3 SOI DD Model — General Syntax](#)
 - [BSIM3 SOI DD Model Parameters](#)
-

BSIM3 SOI DD Model — Features

- Simulation applies dynamic depletion to both I-V and C-V. Tbox and Tsi continuously scale the charge and drain current.
- Supports external body bias and backgate bias; a total of 6 nodes.
- Real floating body simulation in both I-V and C-V. Diode and C-V formulation properly bind the body potential.
- Improved self-heating.
- Improved impact ionization current model.
- Various diode leakage components and parasitic bipolar current.
- Depletion charge model (EBCI) for better accuracy in predicting capacitive coupling. The BSIM3 version 3 based model is also improved.
- Dynamic depletion can suit different requirements for SOI technologies.
- Single I-V expression as in BSIM3 version 3.1 to assure continuities of I_{ds} , G_{ds} , G_m and their derivatives for all bias conditions.

BSIM3 SOI DD Model — General Syntax

Syntax:

```
Mxxx nd ng ns ne [np] mname [L=val] [W=val] [M=val]
+ [AD=val] [AS=val] [PD=val] [PS=val] [NRD=val] [NRS=val]
+ [NRB=val] [RTHO=val] [CTHO=val] [off] [BJToff=val]
+ [IC=Vds, Vgs, Vbs, Ves, Vps] [SOIQ0=val]
```

| Parameter | Description |
|-----------|--|
| Mxxx | SOI MOSFET element name. Must begin with M, followed by up to 1023 alphanumeric characters. |
| nd | Drain terminal node name or number. |
| ng | Front gate node name or number. |
| ns | Source terminal node name or number. |
| ne | Back gate (or Substrate) node name or number. |
| np | External body contact node name or number. |
| mname | MOSFET model name reference. |
| L | SOI MOSFET channel length in meters. This parameter overrides DEFL in an .OPTION statement. Default=DEFL with a maximum of 0.1m. |
| W | SOI MOSFET channel width in meters. This parameter overrides DEFW in an .OPTION statement. Default=DEFW with a maximum of 0.1m. |
| M | Multiplier to simulate multiple SOI MOSFETs in parallel. The M setting affects all channel widths, diode leakages, capacitances, and resistances. Default=1. |
| AD | Drain diffusion area. Overrides DEFAD in the .OPTION statement: Default=DEFAD |
| AS | Source diffusion area. Overrides DEFAS in the .OPTION statement: Default=DEFAS |
| PD | Perimeter of the drain junction, including the channel edge. Overrides DEFAD in the .OPTION statement. |
| PS | Perimeter of the source junction, including the channel edge. Overrides DEFAS in the .OPTION statement. |
| NRD | Number of squares of the drain diffusion for the drain series resistance. Overrides DEFNRD in the .OPTION statement. |

Chapter 2: MOSFET Models

LEVEL 60: BSIM3 SOI DD Model

| Parameter | Description |
|-----------|--|
| NRS | Number of squares of the source diffusion for the source series resistance. Overrides DEFNRS in the .OPTION statement. |
| NRB | Number of squares for the body series resistance. |
| RDC | Additional drain resistance due to the contact resistance in units of ohms. This value overrides the RDC setting in the model specification. Default=0.0. |
| RSC | Additional source resistance due to the contact resistance in units of ohms. This value overrides the RDC setting in the model specification. Default=0.0. |
| RTHO | Thermal resistance per unit width: <ul style="list-style-type: none">■ If you do not specify RTHO, simulation extracts it from the model card.■ If you specify RTHO, it overrides RTHO in the model card. |
| CTHO | Thermal capacitance per unit width: <ul style="list-style-type: none">■ If you do not specify CTHO, simulation extracts it from the model card.■ If you specify CTHO, it overrides CTHO in the model card. |
| OFF | Sets the initial condition to OFF for this element in DC analysis. |
| BJTOFF | Turns off BJT if equal to 1. |
| IC | Initial guess in the order (drain, front gate, internal body, back gate, external voltage). Simulation ignores Vps in a 4-terminal device. Use these settings if you specify UIC in the .TRAN statement. The .IC statement overrides it. |
| SOIQ0 | Floating body charge initialization. This parameter is set for the BQI algorithm of a floating body node. |

BSIM3 SOI DD Model Parameters

This section covers the following topics:

- [BSIM3 SOI DD Model — Control Parameters](#)
- [BSIM3 SOI DD Model — Process Parameters](#)
- [BSIM3 SOI DD Model — DC Parameters](#)
- [BSIM3 SOI DD Model — AC and Capacitance Parameters](#)
- [BSIM3 SOI DD Model — Temperature Parameters](#)
- [BSIM3 SOI DD Model — Notes](#)

BSIM3 SOI DD Model — Control Parameters

| SPICE Symbol | Description | Unit | Default | Notes |
|--------------|--|------|---------|-------|
| CAPMOD | Flag for the short channel capacitance model | - | 2 | nl-1 |
| MOBMOD | Mobility model selector | - | 1 | - |
| NOIMOD | Flag for the noise model | - | 1 | - |
| SHMOD | Flag for self-heating | - | 0 | |
| | ■ 0=no self-heating ■ 1=self-heating | | | |

For more information on the Notes, see [BSIM3 SOI DD Model — Notes](#) section.

BSIM3 SOI DD Model — Process Parameters

| SPICE Symbol | Description | Unit | Default | Notes |
|--------------|--------------------------------|-------------------|----------------------|-------|
| NCH | Channel doping concentration | 1/cm ³ | 1.7x10 ¹⁷ | - |
| NGATE | Poly gate doping concentration | 1/cm ³ | 0 | - |
| NSUB | Substrate doping concentration | 1/cm ³ | 6x10 ¹⁶ | nl-2 |
| TBOX | Buried oxide thickness | m | 3x10 ⁻⁷ | - |
| TOX | Gate oxide thickness | m | 1x10 ⁻⁸ | - |
| TSI | Silicon film thickness | m | 10 ⁻⁷ | - |

For more information on the Notes, see [BSIM3 SOI DD Model — Notes](#) section.

BSIM3 SOI DD Model — DC Parameters

| SPICE Symbol | Description | Unit | Default | Notes |
|--------------|---|------|-------------------------|-------|
| vth0 | Threshold voltage @ V _{bs} =0 for the long and wide device | V | 0.7 for N -0.7 for P | nl-3 |
| A0 | Bulk charge effect coefficient for the channel length | - | 1.0 | - |

Chapter 2: MOSFET Models

LEVEL 60: BSIM3 SOI DD Model

| SPICE Symbol | Description | Unit | Default | Notes |
|---------------------|--|------------------|----------------|--------------|
| A1 | First non-saturation effect parameter | 1/V | 0.0 | - |
| A2 | Second non-saturation effect parameter | 0 | 1.0 | - |
| ABP | Coefficient of the A_{beff} dependency on V_{gst} | - | 1.0 | - |
| ADICE0 | DICE bulk charge factor | - | 1 | - |
| AGIDL | GIDL constant | $\Omega\cdot 1$ | 0.0 | - |
| AGS | Gate bias coefficient of A_{bulk} | 1/V | 0.0 | - |
| All | First V_{dsatii} parameter for the L_{eff} dependence | 1/V | 0.0 | - |
| ALPHA0 | First parameter of the impact ionization current | m/V | 0.0 | - |
| ALPHA1 | Second parameter of the impact ionization current | 1/V | 1.0 | - |
| B0 | Bulk charge effect coefficient for the channel width | m | 0.0 | - |
| B1 | Bulk charge effect width offset | m | 0.0 | - |
| BETA0 | Third parameter of the impact ionization current | V | 30 | - |
| BGIDL | GIDL exponential coefficient | V/m | 0.0 | - |
| BII | Second V_{dsatii} parameter for the L_{eff} dependence | m/V | 0.0 | - |
| CDSC | Drain/Source to the channel coupling capacitance | F/m ² | 2.4e-4 | - |
| CDSCB | Body-bias sensitivity of Cdsc | F/m ² | 0 | - |
| CDSCD | Drain-bias sensitivity of Cdsc | F/m ² | 0 | - |
| CII | First V_{dsatii} parameter for the V_{ds} dependence | - | 0.0 | - |
| CIT | Interface trap capacitance | F/m ² | 0.0 | - |
| DELP | Constant for limiting V_{bseff} to f_s | V | 0.02 | - |
| DELTA | Effective V_{ds} parameter | - | 0.01 | - |

| SPICE Symbol | Description | Unit | Default | Notes |
|---------------------|--|--------------------|----------------|--------------|
| DII | Second Vdsatii parameter for the Vds dependence | V | -1.0 | - |
| DROUT | L dependence coefficient of the DIBL correction parameter in Rout | - | 0.56 | - |
| DSUB | DIBL coefficient exponent | - | 0.56 | - |
| DVBD0 | First coefficient of Vbs0, Leff dependency | V | 0 | - |
| DVBD1 | Second coefficient of Vbs0, Leff dependency | V | 0 | - |
| DVT0 | First coefficient of the short-channel effect on Vth | - | 2.2 | - |
| DVT0W | First coefficient of the narrow-width effect on Vth for a small channel length | - | 0 | - |
| DVT1 | Second coefficient of the short-channel Vth effect | - | 0.53 | - |
| DVT1W | Second coefficient of the narrow-width effect on Vth for a small channel length | - | 5.3e6 | - |
| DVT2 | Body-bias coefficient of the short-channel Vth effect | 1/V | -0.032 | - |
| DVT2W | Body-bias coefficient of the narrow-width effect on Vth for a small channel length | 1/V | -0.032 | - |
| DWB | Coefficient, substrate body bias dependence, Weff | m/V ^{1/2} | 0.0 | |
| DWG | Coefficient of the gate dependence of Weff | m/V | 0.0 | |
| EDL | Electron diffusion length | m | 2e-6 | - |
| ETA0 | DIBL coefficient in the subthreshold region | - | 0.08 | - |
| ETAB | Body-bias coefficient for subthreshold DIBL effect | 1/V | -0.07 | - |
| ISBJT | BJT injection saturation current | A/m ² | 1e-6 | - |
| ISDIF | Body to source/drain injection saturation current | A/m ² | 0.0 | - |
| ISREC | Recombination in the depletion saturation current | A/m ² | 1e-5 | - |

Chapter 2: MOSFET Models

LEVEL 60: BSIM3 SOI DD Model

| SPICE Symbol | Description | Unit | Default | Notes |
|---------------------|--|--------------------|----------------|--------------|
| ISTUN | Reverse tunneling saturation current | A/m ² | 0.0 | - |
| K1 | First order body effect coefficient | V ^{1/2} | 0.5 | - |
| K2 | Second order body-effect coefficient | - | 0 | - |
| K3 | Narrow width coefficient | - | 0 | - |
| K3B | Body-effect coefficient of k3 | 1/V | 0 | - |
| KB1 | Coefficient of V _{bs0} dependency on V _{es} | - | 1 | - |
| KBJT1 | Parasitic bipolar early effect coefficient | m/V | 0 | - |
| KETA | Body-bias coefficient of the bulk charge effect | m | -0.6 | - |
| LINT | Length offset fitting parameter of I-V without bias | m | 0.0 | - |
| MXC | Fitting parameter for calculating A _{beff} | - | -0.9 | - |
| NDIODE | Diode non-ideality factor | - | 1.0 | - |
| NFACTOR | Subthreshold swing factor | - | 1 | - |
| NGIDL | GIDL V _{ds} enhancement coefficient | V | 1.2 | - |
| NLX | Lateral non-uniform doping parameter | m | 1.74e-7 | - |
| NTUN | Reverse tunneling non-ideality factor | - | 10.0 | - |
| PCLM | Channel length modulation parameter | - | 1.3 | - |
| PDIBL1 | Correction parameter for the DIBL effect of the first output resistance | - | .39 | - |
| PDIBL2 | Correction parameter for the DIBL effect of the second output resistance | - | 0.086 | - |
| PRWB | Body-effect coefficient of R _{dsw} | 1/V | 0 | - |
| PRWG | Gate bias effect coefficient of R _{dsw} | 1/V ^{1/2} | 0 | - |
| PVAG | Gate dependence of the Early voltage | - | 0.0 | - |
| RBODY | Intrinsic body contact sheet resistance | ohm/m ² | 0.0 | - |
| RBSH | Extrinsic body contact sheet resistance | ohm/m ² | 0.0 | - |

| SPICE Symbol | Description | Unit | Default | Notes |
|--------------|--|---|---------|-------|
| RDSW | Parasitic resistance per unit width | $\Omega \cdot \text{mm}^{\text{Wr}}$ | 100 | - |
| RSH | Source drain sheet resistance in ohm per square | Ω/square | 0.0 | - |
| U0 | Mobility at Temp=Tnom | $\text{cm}^2/(\text{V}\cdot\text{sec})$ | 670 | - |
| | ■ NMOSFET | | 250 | |
| | ■ PMOSFET | | | |
| UA | First-order mobility degradation coefficient | m/V | 2.25e-9 | - |
| UB | Second-order mobility degradation coefficient | $(\text{m/V})^2$ | 5.9e-19 | - |
| UC | Body-effect of the mobility degradation coefficient | 1/V | -0.0465 | - |
| VBSA | Transition body voltage offset | V | 0 | - |
| VOFF | Offset voltage in the subthreshold region for large W and L values | V | -0.08 | - |
| VSAT | Saturation velocity at Temp=Tnom | m/sec | 8e4 | - |
| W0 | Narrow width parameter | m | 0 | - |
| WINT | Width offset fitting parameter of I-V without bias | m | 0.0 | - |
| WR | Width offset from Weff for calculating Rds | - | 1 | - |

For more information on the Notes, see [BSIM3 SOI DD Model — Notes](#) section.

BSIM3 SOI DD Model — AC and Capacitance Parameters

| SPICE Symbol | Description | Unit | Default | Notes |
|--------------|--|------|------------|-------|
| ASD | Smoothing parameter for the source/drain bottom diffusion | - | 0.3 | - |
| CGD1 | Overlap capacitance for the lightly-doped drain-gate region | F/m | 0.0 | - |
| CGDO | Non-LDD region drain-gate overlap capacitance per channel length | F/m | calculated | nC-2 |
| CGEO | Gate substrate overlap capacitance per unit channel length | F/m | 0.0 | - |

Chapter 2: MOSFET Models

LEVEL 60: BSIM3 SOI DD Model

| SPICE Symbol | Description | Unit | Default | Notes |
|---------------------|---|------------------|----------------------|--------------|
| CGS1 | Overlap capacitance for the lightly-doped source-gate region | F/m | 0.0 | - |
| CGSO | Non-LDD region source-gate overlap capacitance per channel length | F/m | calculated | nC-1 |
| CJSWG | Source/Drain (gate side) sidewall junction | F/m ² | 1e-10 | - |
| | Capacitance per unit width (normalized to 100nm T _{Si}) | | | |
| CKAPPA | Coefficient of the fringing field capacitance for the overlap capacitance in the lightly-doped region | F/m | 0.6 | - |
| CSDESW | Source/drain sidewall fringing capacitance per unit length | F/m | 0.0 | - |
| CSDMIN | Minimum capacitance of the source/drain bottom diffusion | V | calculated | nC-5 |
| MJSWG | Grading coefficient for the Source/Drain (gate side) sidewall junction capacitance | V | 0.5 | - |
| PBSWG | Built-in potential for the Source/Drain (gate side) sidewall junction capacitance | V | .7 | - |
| TT | Coefficient for the diffusion capacitance transit time | second | 1ps | - |
| VSDFB | Flatband voltage for the source/drain bottom diffusion capacitance | V | calculated | nC-3 |
| VSDTH | Threshold voltage for the source/drain bottom diffusion capacitance | V | calculated | nC-4 |
| XPART | Charge partitioning rate flag | - | 0 | |
| CF | Fringing field capacitance for the gate-to-source/ drain | F/m | calculated | nC-6 |
| CLC | Constant term for the short-channel mode | m | 0.1x10 ⁻⁷ | - |
| CLE | Exponential term for the short-channel mode | none | 0.0 | - |
| DLC | Length offset fitting parameter from C-V | m | lint | - |
| DWC | Width offset fitting parameter from C-V | m | wint | - |

For more information on the Notes, see [BSIM3 SOI DD Model — Notes](#) section.

BSIM3 SOI DD Model — Temperature Parameters

| SPICE Symbol | Description | Unit | Default | Notes |
|--------------|--|--------------------|-----------|-------|
| AT | Temperature coefficient for the saturation velocity | m/sec | 3.3e4 | - |
| CTH0 | Normalized thermal capacity | (W*S)/m°C | 0 | - |
| KT1 | Temperature coefficient for the threshold voltage | V | -0.11 | - |
| KT11 | Channel length dependence of the temperature coefficient for the threshold voltage | V*m | 0.0 | - |
| KT2 | Body-bias coefficient of the V_{th} temperature effect | none | 0.022 | - |
| PRT | Temperature coefficient for R_{dsw} | $\Omega\cdot\mu m$ | 0 | - |
| RTH0 | Normalized thermal resistance | moC/W | 0 | - |
| TNOM | Temperature at which simulation expects parameters | °C | 27 | - |
| UA1 | Temperature coefficient for U_a | m/V | 4.31e-9 | - |
| UB1 | Temperature coefficient for U_b | $(m/V)^2$ | -7.61e-18 | - |
| UC1 | Temperature coefficient for U_c | 1/V | -.056 | nT-1 |
| UTE | Mobility temperature exponent | none | -1.5 | - |
| XBJT | Power dependence of j_{bjt} on the temperature | none | 2 | - |
| XDIF | Power dependence of j_{dif} on the temperature | none | 2 | - |
| XREC | Power dependence of j_{rec} on the temperature | none | 20 | - |
| XTUN | Power dependence of j_{tun} on the temperature | none | 0 | - |

For more information on the Notes, see [BSIM3 SOI DD Model — Notes](#) section.

Chapter 2: MOSFET Models

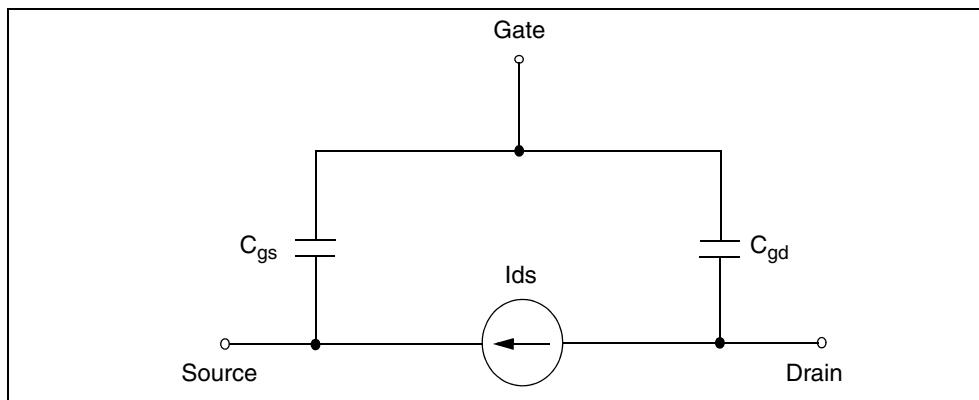
LEVEL 60: BSIM3 SOI DD Model

BSIM3 SOI DD Model — Notes

| Note | Explanation |
|------|---|
| nl-1 | <i>Capmod 0 and 1 do not calculate the dynamic depletion. Therefore, ddMod does not work with capmod.</i> |
| nl-2 | BSIMSOI refers to a substrate of the silicon below the buried oxide, not the well region in BSIM3. It calculates the backgate flatband voltage (V_{fb}) and the parameters related to the source/drain diffusion bottom capacitance (V_{sdth} , V_{sdfb} , C_{sdmin}). <ul style="list-style-type: none"> ■ Positive n_{sub} is the same type of doping as the body. ■ Negative n_{sub} is the opposite type of doping. |
| nC-1 | If you do not specify cgs_0 , simulation calculates it: <ul style="list-style-type: none"> ■ if you specify dlc greater than 0, then $cgs_0=pl=(dlc*cox)-cgs_1$ ■ if the previously-calculated $cgs_0 < 0$, then $cgs_0=0$ ■ else $cgs_0=0.6*Tsi*cox$ |
| nC-2 | Calculates C_{gdo} similar to C_{sdo} |
| nC-3 | If n_{sub} is positive, then: |
| | $V_{sdfb} = -\frac{kT}{q} \log\left(\frac{10^{20} \cdot n_{sub}}{n_i \cdot n_i}\right) - 0.3 \text{ else } V_{sdfb} = -\frac{kT}{q} \log\left(\frac{10^{20}}{n_{sub}}\right) + 0.3$ |
| nC-4 | If n_{sub} is positive, then: |
| | $\phi_{sd} = 2\frac{kT}{q} \log\left(\frac{n_{sub}}{n_i}\right), \Upsilon_{sd} = \frac{5.753 \times 10^{-12} \sqrt{n_{sub}}}{C_{box}} \quad V_{sdth} = V_{sdfb} + \phi_{sd} + \Upsilon_{sd} \sqrt{\phi_{sd}}$ else: $\phi_{sd} = 2\frac{kT}{q} \log\left(-\frac{n_{sub}}{n_i}\right), \Upsilon_{sd} = \frac{5.753 \times 10^{-12} \sqrt{-n_{sub}}}{C_{box}} \quad V_{sdth} = V_{sdfb} - \phi_{sd} - \Upsilon_{sd} \sqrt{\phi_{sd}}$ |
| nC-5 | $X_{sddep} = \sqrt{\frac{2\epsilon_{si}\phi_{sd}}{q[n_{sub} \cdot 10^6]}}, C_{sddep} = \frac{\epsilon_{si}}{X_{sddep}}, C_{sdmin} = \frac{C_{sddep}C_{box}}{C_{sddep} + C_{box}}$ |
| nC-6 | If you do not specify cf , then simulation calculates it: |
| | $CF = \frac{2\epsilon_{ox}}{\pi} 1n \left(1 + \frac{4 \times 10^{-7}}{T_{ox}} \right)$ |
| nT-1 | For $mobmod=1$ and 2 , the unit is m/V^2 . Default is $-5.6E-11$. For $mobmod=3$, the unit is $1/V$ and the default is -0.056 . |

LEVEL 61: RPI a-Si TFT Model

This is a Synopsys MOSFET model which is based on the AIM-SPICE MOS15 amorphous silicon (a-Si) thin-film transistor (TFT) model, developed by Rensselaer Polytechnic Institute.



This section covers the following topics:

- [RPI a-Si TFT Model Features](#)
- [Using RPI a-Si TFT Model with Synopsys Simulators](#)
- [RPI a-Si TFT Model Parameters](#)
- [RPI a-Si TFT Model Equations](#)

RPI a-Si TFT Model Features

Features of the AIM-SPICE MOS15 a-Si TFT model include:

- Modified charge control model; induced charge trapped in localized states
- Above threshold includes:
 - Field effect mobility becoming a function of gate bias
 - Band mobility dominated by lattice scattering
- Below threshold includes:
 - Fermi level located in deep localized states
 - Relate position of Fermi level, including the deep DOS, back to the gate bias

- Empirical expression for current at large negative gate biases for hole-induced leakage current
 - Applies interpolation techniques to equations to unify the model
-

Using RPI a-Si TFT Model with Synopsys Simulators

To simulate using the AIM-SPICE MOS15 a-Si TFT model:

1. Set Level=61 to identify the model as the AIM-SPICE MOS15 a-Si TFT model.
2. The default value for L is 100 μm , and the default value for W is 100 μm .
3. Level 61 is a 3-terminal model. This model does not include a bulk node; therefore simulation does not append parasitic drain-bulk or source-build diodes are appended to the model. You can specify a fourth node, but it does not affect simulation results.
4. The default room temperature is 25°C in Synopsys circuit simulators, but is 27°C in most other simulators. When comparing to other simulators, use .TEMP 27 or .OPTION TNOM=27 to set the simulation temperature to 27 in the netlist.

The following is an example of how Level 61 modifies the Synopsys MOSFET model and element statement.

```
mckt drain gate source nch L=10e-6 W=10e-6
.MODEL nch nmos Level=61
+ alphasat=0.6 cgdo=0.0 cgso=0.0 def0=0.6
+ delta=5.0 el=0.35 emu=0.06 eps=11
+ epsi=7.4 gamma=0.4 gmin=1e23 iol=3e-14
+ kasat=0.006 kvt=-0.036 lambda=0.0008 m=2.5
+ muband=0.001 rd=0.0 rs=0.0 sima0=1e-14
+ tnom=27 tox=1.0e-7 v0=0.12 vaa=7.5e3
+ vdsl=7 vfb=-3 vgs1=7 vmin=0.3 vto=0.0
```

RPI a-Si TFT Model Parameters

| Name | Unit | Default | Description |
|----------|----------------------|---------|---|
| ALPHASAT | - | 0.6 | Saturation modulation parameter |
| CGDO | F/m | 0.0 | Gate-drain overlap capacitance per meter channel width |
| CGSO | F/m | 0.0 | Gate-source overlap capacitance per meter channel width |
| DEF0 | eV | 0.6 | Dark Fermi level position |
| DELTA | - | 5 | Transition width parameter |
| EL | eV | 0.35 | Activation energy of the hole leakage current |
| EMU | eV | 0.06 | Field effect mobility activation energy |
| EPS | - | 11 | Relative dielectric constant of the substrate |
| EPSI | - | 7.4 | Relative dielectric constant of the gate insulator |
| GAMMA | - | 0.4 | Power law mobility parameter |
| GMIN | m ⁻³ eV-1 | 1E23 | Minimum density of deep states |
| IOL | A | 3E-14 | Zero-bias leakage current parameter |
| KASAT | 1°X | 0.006 | Temperature coefficient of ALPHASAT |
| KVT | V°X | -0.036 | Threshold voltage temperature coefficient |
| LAMBDA | 1/V | 0.0008 | Output conductance parameter |
| M | - | 2.5 | Knee shape parameter |
| MUBAND | m ² /Vs | 0.001 | Conduction band mobility |
| RD | m | 0.0 | Drain resistance |
| RS | m | 0.0 | Source resistance |
| SIGMA0 | A | 1E-14 | Minimum leakage current parameter |
| TNOM | oC | 25 | Parameter measurement temperature |
| TOX | m | 1E-7 | Thin-oxide thickness |

| Name | Unit | Default | Description |
|------|------|---------|--|
| V0 | V | 0.12 | Characteristic voltage for deep states |
| VAA | V | 7.5E3 | Characteristic voltage for field effect mobility |
| VDSL | V | 7 | Hole leakage current drain voltage parameter |
| VFB | V | -3 | Flat band voltage |
| VGSL | V | 7 | Hole leakage current gate voltage parameter |
| VMIN | V | 0.3 | Convergence parameter |
| VTO | V | 0.0 | Zero-bias threshold voltage |

RPI a-Si TFT Model Equations

This section covers the following topics:

- [RPI a-Si TFT Model — Drain Current](#)
- [RPI a-Si TFT Model — Temperature Dependence](#)
- [RPI a-Si TFT Model — Capacitance](#)

RPI a-Si TFT Model — Drain Current

$$I_{ds} = I_{leakage} + I_{ab}, \quad I_{ab} = g_{ch} V_{dse} (1 + LAMBDA \cdot V_{ds})$$

$$V_{dse} = \frac{V_{ds}}{\left[1 + (V_{ds}/V_{sate})^M\right]^{1/M}}$$

$$V_{sate} = \alpha_{sat} V_{gte}$$

$$g_{ch} = \frac{g_{chi}}{1 + g_{chi}(RS + RD)}, \quad g_{chi} = qn_s W \cdot MUBAND / L$$

$$n_s = \frac{n_{sa} n_{sb}}{n_{sa} + n_{sb}}$$

$$n_{sa} = \frac{EPSI \cdot V_{gte}}{(q \cdot TOX)} \cdot \left(\frac{V_{gte}}{V_{aat}} \right)^{GAMMA}$$

$$n_{sb} = n_{so} \left(\frac{t_m}{TOX} \frac{V_{gfbe} EPSI}{V_0 EPS} \right)^{\frac{2 \cdot V_0}{V_e}}$$

$$n_{so} = N_c t_m \frac{V_e}{V_0} \exp\left(-\frac{DEF0}{V_{th}}\right), N_c = 3.0 \cdot 10^{25} m^{-3}$$

$$V_e = \frac{2 \cdot V_0 \cdot V_{tho}}{2 \cdot V_0 - V_{th}}, t_m = \sqrt{\frac{EPS}{2q \cdot GMIN}}$$

$$V_{gte} = \frac{VMIN}{2} \left[1 + \frac{V_{gt}}{VMIN} + \sqrt{DELTA^2 + \left(\frac{V_{gt}}{VMIN} - 1 \right)^2} \right]$$

$$V_{gt} = V_{gs} - V_T$$

$$V_{gfbe} = \frac{VMIN}{2} \left[1 + \frac{V_{gfb}}{VMIN} + \sqrt{DELTA^2 + \left(\frac{V_{gfb}}{VMIN} - 1 \right)^2} \right]$$

$$V_{gfb} = V_{gs} - VFB, I_{leakage} = I_{hl} + I_{min}$$

$$I_{hl} = IOL \left[\exp\left(\frac{V_{ds}}{VDSL}\right) - 1 \right] \exp\left(-\frac{V_{gs}}{VGSL}\right) \exp\left[\frac{EL}{q} \left(\frac{1}{V_{tho}} - \frac{1}{V_{th}} \right)\right]$$

$$I_{min} = SIGMA0 \cdot V_{ds}$$

RPI a-Si TFT Model — Temperature Dependence

$$V_{tho} = k_B \cdot TNOM / q, V_{th} = k_B \cdot (TEMP) / q$$

$$V_{aat} = VAA \exp\left[\frac{EMU}{q \cdot GAMMA} \left(\frac{1}{V_{th}} - \frac{1}{V_{tho}} \right)\right]$$

$$V_T = VTO + KVT(TEMP - TNOM)$$

$$\alpha_{sat} = ALPHASAT + KASAT(TEMP - TNOM)$$

RPI a-Si TFT Model — Capacitance

$$C_{gs} = C_f + \frac{2}{3} C_{gc} \left[1 - \left(\frac{V_{sate} - V_{dse}}{2V_{sate} - V_{dse}} \right)^2 \right]$$

Chapter 2: MOSFET Models

LEVEL 61: RPI a-Si TFT Model

$$C_{gd} = C_f + \frac{2}{3}C_{gc} \left[1 - \left(\frac{V_{sate}}{2V_{sate} - V_{dse}} \right)^2 \right]$$

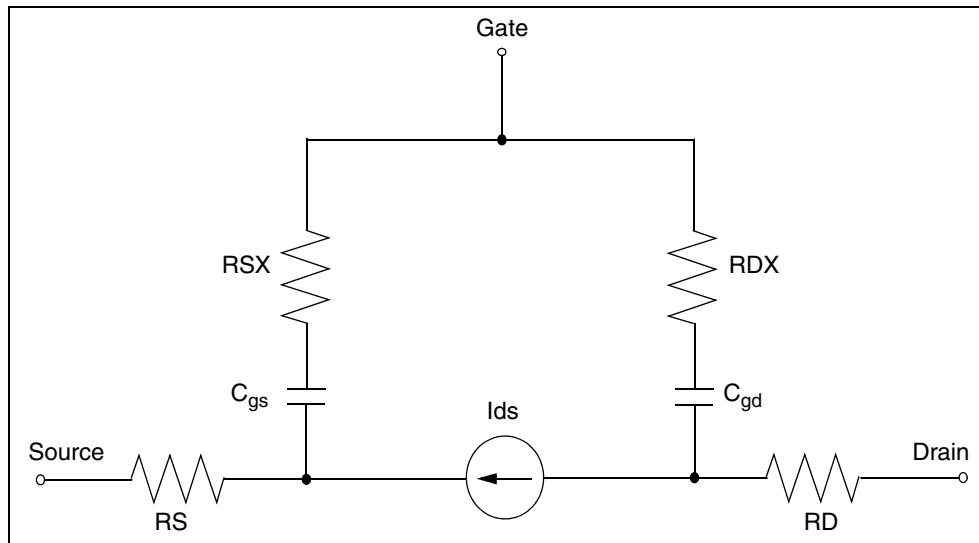
$$C_f = 0.5 \cdot EPS \cdot W, \quad \left(C_{gs} = q \frac{dn_{sc}}{dV_{gs}} \right)$$

$$n_{sc} = \frac{n_{sac} n_{sbc}}{n_{sac} + n_{sbc}}, \quad \left(n_{sa} = \frac{EPSI \cdot V_{gte}}{(q \cdot TOX)} \cdot \left(\frac{V_{gte}}{V_{aat}} \right)^{GAMMA} \right)$$

$$n_{sbc} = n_{sb}$$

LEVEL 62: RPI Poli-Si TFT Model

This is an AIM-SPICE MOS16 poly-silicon (Poli-Si) thin-film transistor (TFT) model, developed by Rensselaer Polytechnic Institute. This model is supported by HPP.



The following topics are discussed in the next sections.

- [RPI Poli-Si TFT Model Features](#)
- [Using RPI Poli-Si TFT Model with Synopsys Simulators](#)
- [RPI Poli-Si TFT Model Parameters](#)
- [RPI Poli-Si TFT Model Equations](#)
- [RPI Poli-Si TFT Model Version 2 Equations](#)

RPI Poli-Si TFT Model Features

Features of the AIM-SPICE MOS16 Poli-Si TFT model include:

- A design based on the crystalline MOSFET model
- Field effect mobility that becomes a function of the gate bias
- Effective mobility that accounts for trap states:
 - For low V_{gs} , it is the power law

Chapter 2: MOSFET Models

LEVEL 62: RPI Poli-Si TFT Model

- For high V_{GS} , it is the constant
- Reverse bias drain current function of the electric field near the drain and the temperature
- A design independent of the channel length
- A unified DC model that includes all four regimes for channel lengths down to 4 μm :
 - Leakage (thermionic emission)
 - Subthreshold (diffusion-like model)
 - Above threshold (c-Si-like with mFet)
 - Kink (impact ionization with feedback)
- An AC model accurately reproduces the C_{gc} frequency dispersion
- Automatic scaling of model parameters that accurately model a wide range of device geometries

Using RPI Poli-Si TFT Model with Synopsys Simulators

To simulate using the AIM-SPICE MOS16 Poli-Si TFT model:

1. Set `LEVEL=62` to identify the model as the AIM-SPICE MOS16 Poli-Si TFT model.
2. The default value for `L` is 100 μm , and the default value for `W` is 100 μm .
3. Level 62 is a 3-terminal model. This model does not include a bulk node; therefore, simulation does not append a parasitic drain-bulk or source-bulk diode to the model. You can specify a fourth node, but it does not affect the simulation results.
4. The default room temperature is 25°C in Synopsys circuit simulators, but is 27°C in most other simulators. When comparing to other simulators, use `.TEMP 27` or `.OPTION TNOM=27` to set the simulation temperature to 27°C in the netlist.

The following is an example of how Level 62 modifies a MOSFET device model and element statement:

```
mckt drain gate source nch L=10e-6 W=10e-6
.MODEL nch nmox Level=62
+ asat=1 at=3e-8 blk=0.001 bt=0.0 cgdo=0.0
+ cgso=0.0 dasat=0.0 dd=1.4e-7 delta=4.0
+ dg=2.0e-7 dmul=0.0 dvt=0.0 dvto=0.0 eb=0.68
+ eta=7 etac0=7 etac00=0 i0=6.0 i00=150
+ lasat=0 lkink=19e-6 mc=3.0 mk=1.3 mmu=3.0
+ mu0=100 mul=0.0022 mus=1.0 rd=0.0 rdx=0.0
+ rs=0.0 rsx=0.0 tnom=27 tox=1.0e-7 vfb=-0.1
+ vkink=9.1 von=0.0 vto=0.0
```

RPI Poli-Si TFT Model Parameters

This section covers the following topics:

- [RPI Poli-Si TFT Model — General Parameters](#)
- [RPI Poli-Si TFT Model — Version 2 Parameters](#)
- [RPI Poli-Si TFT Model — Self-heating Parameters](#)
- [RPI Poli-Si TFT Model — ACM Parameters for Drain and Source Resistance Calculus Specific to HSPICE](#)

RPI Poli-Si TFT Model — General Parameters

| Name | Unit | Default | Description |
|--------|-------|---------|---|
| ASAT | - | 1 | Proportionality constant of Vsat |
| AT | m/V | 3E-8 | DIBL parameter 1 |
| BLK | - | 0.001 | Leakage barrier lowering constant |
| BT | m · V | 1.9E-6 | DIBL parameter 2 |
| CAPMOD | - | 0 | Model capacitance selector (zero recommended) |
| CGDO | F/m | 0 | Gate-drain overlap capacitance per meter channel width |
| CGSO | F/m | 0 | Gate-source overlap capacitance per meter channel width |
| DASAT | 1/°C | 0 | Temperature coefficient of ASAT |
| DD | m | 1400 Å | Vds field constant |
| DELTA | - | 4.0 | Transition width parameter |

Chapter 2: MOSFET Models

LEVEL 62: RPI Poli-Si TFT Model

| Name | Unit | Default | Description |
|--------|---------------------------------|---------|---|
| DG | m | 2000 Å | Vgs field constant |
| DMU1 | $\chi\mu^2/\varsigma \propto C$ | 0 | Temperature coefficient of MU1 |
| DVT | V | 0 | The difference between VON and the threshold voltage |
| DVTO | V/ $^{\circ}$ C | 0 | Temperature coefficient of VTO |
| EB | eV | 0.68 | Barrier height of the diode |
| EPS | - | 11.7 | Constant of the substrate (default user-specifiable) |
| EPSI | - | 3.9 | Constant of the gate insulator (deflt. user-specifiable) |
| ETA | - | 7 | Subthreshold ideality factor |
| ETAC0 | - | ETA | Capacitance subthreshold ideality factor at zero-drain bias |
| ETAC00 | 1/V | 0 | Capacitance subthreshold coefficient of the drain bias |
| I0 | A/m | 6.0 | Leakage scaling constant |
| I00 | A/m | 150 | Reverse diode saturation current |
| KSS | - | 0 | Small signal parameter (zero is recommended) |
| LASAT | M | 0 | Coefficient for length dependence of ASAT |
| LKINK | M | 19E-6 | Kink effect constant |
| MC | - | 3.0 | Capacitance knee shape parameter |
| MK | - | 1.3 | Kink effect exponent |
| MMU | - | 3.0 | Low field mobility exponent |
| MU0 | cm ² /Vs | 100 | High field mobility |
| MU1 | cm ² /Vs | 0.0022 | Low field mobility parameter |
| MUS | cm ² /Vs | 1.0 | Subthreshold mobility |
| RD | μ | 0 | Drain resistance |
| RDX | Ω | 0 | Resistance in series with C_{gd} |

| Name | Unit | Default | Description |
|----------------|--------------------|---------|---|
| RS | μ | 0 | Source resistance |
| RSX | Ω | 0 | Resistance in series with C_{gs} |
| TNOM | $^{\circ}\text{C}$ | 25 | Parameter measurement temperature |
| TOX | m | 1e-7 | Thin-oxide thickness |
| V0 | V | 0.12 | Characteristic voltage for deep states |
| VFB | V | -0.1 | Flat band voltage |
| VKINK | V | 9.1 | Kink effect voltage |
| VON | V | 0 | On-voltage |
| VSI | V | 2.0 | vgs dependence parameter |
| VST | V | 2.0 | vgs dependence parameter |
| VTO | V | 0 | Zero-bias threshold voltage |
| ZEROC | - | 0 | Flag for capacitance calculations in capmod=1 <ul style="list-style-type: none"> ■ capmod=1: set the 0 capacitance value ■ capmod=0: calculation capacitance |
| XL | m | 0 | Length bias accounts for the masking and etching effects |
| XW | m | 0 | Width bias accounts for the masking and etching effects |
| LMLT | - | 1 | Length shrink factor |
| WMLT | - | 1 | Width shrink factor |
| COMPATIBLE=0 1 | - | 0 | <ul style="list-style-type: none"> ■ COMPATIBLE=0: HSPICE implementation of AIM-SPICE MOS 16 RPI TFT model. ■ COMPATIBLE=1: Enables compatibility to a commonly-used TFT model by the industry. |

RPI Poli-Si TFT Model — Version 2 Parameters

| Name | Unit | Default | Description |
|---------|------|---------|----------------------------|
| VERSION | - | 1 | 1=Version 1 2=Version 2 |

Chapter 2: MOSFET Models

LEVEL 62: RPI Poli-Si TFT Model

| Name | Unit | Default | Description |
|----------|------|--|---|
| DIBLMOD | - | 1 | DIBL model selector |
| INTDSNOD | - | 1 if VERSION=1 0 if VERSION=2 | Extrinsic series resistance mode selector: 0 - uses internal approximation for drain and source resistances 1 – uses drain and source resistances as extrinsic elements |
| ISUBMOD | - | 0 | Channel length modulation selector: 0 – uses LAMBDA 1 – uses LS and VP |
| LAMBDA | 1/V | | Channel length modulation parameter |
| LME | m | 0 | ME length dependence parameter |
| LMU0 | m | 0 | MU0 length dependence parameter |
| LMU1 | m | 0 | MU1 length dependence parameter |
| LS | - | 3.50E-008 | Channel length modulation parameter |
| ME (MS) | - | 2.5 | Long channel saturation transition parameter |
| META | - | 1 | ETA floating-body parameter |
| MSS | - | 1.5 | Vdse transition parameter |
| THETA | M/V | 0 | Mobility degradation parameter |
| VMAX | m/s | 4.00E+004 | Saturation velocity |
| VP | V | 0.2 | Channel length modulation parameter |
| VSIGMA | V | VSI, if specified 0.2, otherwise | VGS dependence parameter |
| VSIGMA | V | VSI, if specified, 0.2 otherwise | VGS dependence parameter |
| VSIGMAT | V | VST, if specified 1.7, otherwise | VGS dependence parameter |
| VSIGMAT | V | VST, if specified, 1.7 otherwise | VGS dependence parameter |

RPI Poli-Si TFT Model — Self-heating Parameters

| Name | Unit | Default | Description |
|-------|-----------|-----------|---|
| CTH0 | (W*S)/m°C | 1.00E-005 | Thermal capacitance per unit width |
| RTH0 | m°C/W | 0 | Thermal resistance per unit width |
| SHMOD | - | 0 | Self-heating flag |
| WTH0 | m | 0 | Width offset for thermal resistance and capacitance scaling |

RPI Poli-Si TFT Model — ACM Parameters for Drain and Source Resistance Calculus Specific to HSPICE

| Name | Unit | Default | Description |
|------|--------|---------|--|
| ACM | - | - | Area calculation method |
| HDIF | m | 0 | Length of heavily doped diffusion |
| LD | m | 0 | Lateral diffusion into channel from source and drain diffusion |
| LDIF | m | 0 | Length of heavily doped region adjacent to gate |
| RDC | ohm | 0 | Additional drain resistance due to contact |
| RSC | ohm | 0 | Additional source resistance due to contact |
| RSH | ohm/sq | 0 | Drain and source diffusion sheet resistance |
| WD | m | 0 | Lateral diffusion into channel from bulk along width |

Note: Source and drain resistances are calculated similarly to other HSPICE MOSFET models, which are based on the value of ACM.

RPI Poli-Si TFT Model Equations

This section covers the following topics:

- [RPI Poli-Si TFT Model — Drain Current: Total Current](#)
- [RPI Poli-Si TFT Model — Drain Current: Subthreshold Current](#)
- [RPI Poli-Si TFT Model — Drain Current: Subthreshold Leakage Current](#)

Chapter 2: MOSFET Models

LEVEL 62: RPI Poli-Si TFT Model

- RPI Poli-Si TFT Model — Drain Current: Impact Ionization Effect
- RPI Poli-Si TFT Model — Threshold Voltage
- RPI Poli-Si TFT Model — Temperature Dependence
- RPI Poli-Si TFT Model — Capacitance: CAPMOD=0
- RPI Poli-Si TFT Model — Capacitance: CAPMOD=1
- RPI Poli-Si TFT Model — Geometry Effect
- RPI Poli-Si TFT Model — Self Heating

RPI Poli-Si TFT Model — Drain Current: Total Current

$$I_{ds} = \frac{I_a \cdot I_{sub}}{I_a + I_{sub}} \cdot (1 + I_{kink}) + I_{leak}$$

RPI Poli-Si TFT Model — Drain Current: Subthreshold Current

The following is the expression for the subthreshold current:

$$I_{sub} = MUS \cdot C_{ox} \frac{W}{L} V_{sth}^2 \exp\left(\frac{V_{GT}}{V_{sth}}\right) \left[1 - \exp\left(-\frac{V_{DS}}{V_{sth}}\right) \right]$$

$$I_{sub} = MUS \cdot C_{ox} \cdot \frac{W_{eff}}{L_{eff}} \cdot V_{sth}^2 \cdot \exp\left(\frac{V_{GT}}{V_{sth}}\right) \cdot \left(1 - \exp\left(-\frac{V_{DS}}{V_{sth}}\right) \right)$$

$$C_{OX} = \frac{\epsilon_i}{T_{OX}}, \quad V_{sth} = ETA \cdot V_{th}, \quad V_{th} = \frac{k_B \cdot TEMP}{q}$$

$$V_{GT} = V_{GS} - V_{Teff}$$

$$V_{Teff} = V_{TX} - \frac{AT \cdot V_{DS}^2 + BT}{L_{eff} \cdot \left(1 + \exp\left(\frac{V_{GS} - VST - VTX}{VSI}\right) \right)}$$

In the preceding equations, $\epsilon\tau$ is the dielectric constant of the oxide, and k_B is the Boltzmanns constant.

Above the $V_{GT} > 0$ threshold, the following equation calculates the conduction current:

$$I_a = \frac{\mu_{FET} \cdot C_{OX} \cdot W_{eff}}{L_{eff}} \left(V_{GTE} \cdot V_{DS} - \frac{V_{DS}^2}{2 \cdot \alpha_{sat}} \right) \text{ for } V_{DS} \leq \alpha_{sat} V_{GTE}$$

$$\frac{\mu_{FET} \cdot C_{OX} \cdot W_{eff} \cdot V_{GTE}^2 \cdot \alpha_{sat}}{2 \cdot L_{eff}} \quad \text{for } V_{DS} > \alpha_{sat} V_{GTE}$$

$$\frac{1}{\mu_{FET}} = \frac{1}{MUO} + \frac{1}{\mu_1 \cdot \left(\frac{2 \cdot V_{GTE}}{V_{sth}} \right)^{MMU}}$$

$$V_{GTE} = V_{sth} \cdot \left[1 + \frac{V_{GT}}{2 \cdot V_{sth}} + \sqrt{DELTA^2 + \left(\frac{V_{GT}}{2 \cdot V_{sth}} - 1 \right)^2} \right]$$

RPI Poli-Si TFT Model — Drain Current: Subthreshold Leakage Current

Subthreshold leakage current is the result of the thermionic field emission of carriers through the grain boundary trap states as described in the following equations.

$$I_{leak} = IO \cdot W_{eff} \cdot \left[\exp \left(\frac{q \cdot BLK \cdot V_{DS}}{k \cdot T} \right) - 1 \right] \cdot (X_{TFE} + X_{TE}) + I_{diode}$$

$$X_{TFE} = \frac{X_{TFE, lo} \cdot X_{TFE, hi}}{X_{TFE, lo} + X_{TFE, hi}}$$

The following equations calculate values for the preceding equations:

$$X_{TE} = \exp(-W_C)$$

$$W_C = \frac{E_C - E_t}{k \cdot T} = \frac{0.55eV}{k \cdot T}$$

$$X_{TFE, lo} = \frac{4\sqrt{\pi}}{3} \cdot f \cdot \exp \left(\frac{4}{27} \cdot f^2 - W_c \right) \text{ for } f \leq f_{lo}$$

$$X_{TFE, lo}(f_{lo}) \cdot \exp \left[\left(\frac{1}{f_{lo}} + \frac{8}{27} \cdot f_{lo} \right) \cdot (f - f_{lo}) \right] \text{ for } f > f_{lo}$$

Chapter 2: MOSFET Models

LEVEL 62: RPI Poli-Si TFT Model

$$X_{TFE,hi} = \frac{2W_c}{3} \cdot \exp\left(1 - \frac{2W_c}{3}\right) \quad \text{for } f > f_{hi}$$

$$\left(1 - \frac{3\sqrt{W_c}}{2 \cdot f}\right)^{-1} \exp\left[\frac{-W_c^{3/2}}{f}\right] \quad \text{for } f \geq f_{hi}$$

$$f_{hi} = 3 \cdot \left(\frac{W_c^{3/2}}{2W_c - 3}\right)$$

$$f = \frac{F_{min}}{2} \left[1 + \frac{F_f}{F_{min}} + \sqrt{DELTA^2 + \left(\frac{F_f}{F_{min}} - 1\right)^2} \right]$$

$$F_{min} = 1 e^{-4}$$

$$X_{TFE,lo}(f_{lo}) = \frac{2\sqrt{4\pi}}{3} \cdot f_{lo} \cdot \exp\left(\frac{4}{27}f_{lo}^2 - W_c\right)$$

$$F_f = \left(\frac{V_{DS}}{DD} - \frac{V_{GS} - VFB}{DG}\right)$$

$$F_{fo} = (k \cdot T)^{3/2} \cdot \left(\frac{4}{3} \cdot \frac{2\pi\sqrt{2m^*}}{q \cdot h}\right)$$

$$m^* = 0.27 \cdot m_0$$

$$f_{lo} = \frac{3}{2} \cdot (\sqrt{W_c + 1} - 1)$$

$$I_{diode} = IOO \cdot W_{eff} \cdot \exp\left(-\frac{EB}{k \cdot T}\right) \left[1 - \exp\left(-\frac{q \cdot V_{DS}}{k \cdot T}\right)\right]$$

RPI Poli-Si TFT Model — Drain Current: Impact Ionization Effect

$V_{GT} > 0$ very large drain biases include the kink effect. Level 62 models this effect as impact ionization in a narrow region near the drain, and adds the I_{kink} impact ionization current to the drain current. The expression is:

$$I_{kink} = A_{kinkt} \cdot (V_{DS} - V_{DSE}) \cdot \exp\left(-\frac{VKINK}{V_{DS} - V_{DSE}}\right)$$

$$A_{kinkt} = \frac{1}{VKINK} \left(\frac{LKINK}{L_{eff}} \right)^{MK}$$

$$V_{DSE} = \frac{V_{DS}}{\left(1 + \left(\frac{V_{DS}}{V_{DSAT}}\right)^3\right)^{1/3}} - V_{th}$$

$$V_{DSAT} = \alpha_{sat} \cdot V_{GTE}$$

RPI Poli-Si TFT Model — Threshold Voltage

If you do not specify VTO, then VT=VON-DVT. Otherwise, VT=VTO.

RPI Poli-Si TFT Model — Temperature Dependence

$$V_{TX} = V_T - DVTO \cdot (TEMP - TNOM)$$

$$\mu_1 = MU1 + DMU1 \cdot (TEMP - TNOM)$$

$$\alpha_{sat} = ASAT - \frac{LASAT}{L_{eff}} - DASAT \cdot (TEMP - TNOM)$$

RPI Poli-Si TFT Model — Capacitance: CAPMOD=0

$$C_{gs} = C_f + \frac{2}{3} \cdot C_{gcs} \cdot \left[1 - \left(\frac{V_{DSAT} - V_{DSEX}}{2V_{DSAT} - V_{DSEX}} \right)^2 \right]$$

$$C_{gd} = C_f + \frac{2}{3} \cdot C_{gcd} \cdot \left[1 - \left(\frac{V_{DSAT}}{2V_{DSAT} - V_{DSEX}} \right)^2 \right]$$

$$C_f = 0.5 \cdot EPS \cdot W_{eff}$$

$$C_{gcd} = \frac{C_{ox}}{1 + \eta_{cd} \cdot \exp\left(-\frac{V_{GTX}}{\eta_{cd} \cdot V_{th}}\right)}$$

$$C_{gcs} = \frac{C_{ox}}{1 + ETAC0 \cdot \exp\left(-\frac{V_{GTX}}{ETAC0 \cdot V_{th}}\right)}$$

Chapter 2: MOSFET Models

LEVEL 62: RPI Poli-Si TFT Model

$$C_{OX} = \frac{W_{eff} \cdot L_{eff} \cdot \epsilon_i}{T_{OX}}, \quad \eta_{ed} = ETAC0 + ETAC00 \cdot V_{DSEX}$$

$$V_{DSEX} = \frac{V_{DS}}{\left[1 + \left(\frac{V_{DS}}{V_{DSAT}}\right)^{MC}\right]^{\frac{1}{MC}}}$$

$$V_{GTX} = V_{GS} - V_{TX}$$

RPI Poli-Si TFT Model — Capacitance: CAPMOD=1

If ZEROC equals 1:

$$V_{gst} = V_{GS} - V_{TX}$$

$$Phi = 0.6$$

$$V_{gst} < \frac{-phi}{2} \quad C_{gs} = C_{gd} = 0$$

$$\frac{-phi}{2} \leq V_{gst} < 0 \quad C_{gs} = \frac{4 \cdot V_{gst} \cdot C_{OX}}{3 \cdot Phi} + \frac{2 \cdot C_{OX}}{3}, \quad C_{gd} = 0$$

$$V_{gst} \geq 0 \quad \begin{cases} V_{DS} \geq V_{DSAT} & C_{gs} = \frac{2C_{OX}}{3}, \quad C_{gd} = 0 \\ V_{DS} < V_{DSAT} & C_{gd} = \frac{2}{3} \cdot C_{OX} \cdot \left[1 - \left(\frac{V_{DSAT}}{2(V_{DSAT} - V_{DSEX})}\right)^2\right] \\ & C_{gs} = \frac{2}{3} \cdot C_{OX} \cdot \left[1 - \left(\frac{V_{DSAT} - V_{DSE}}{2(V_{DSAT} - V_{DSEX})}\right)^2\right] \end{cases}$$

$$C_{OX} = \frac{\epsilon_i \cdot W_{eff} \cdot L_{eff}}{T_{OX}}, \quad V_{DSEX} = \frac{V_{DS}}{\left[1 + \left(\frac{V_{DS}}{V_{DSAT}}\right)^{MC}\right]^{\frac{1}{MC}}}$$

RPI Poli-Si TFT Model — Geometry Effect

$$W_{eff} = W + XW$$

$$L_{eff} = L + XL$$

RPI Poli-Si TFT Model — Self Heating

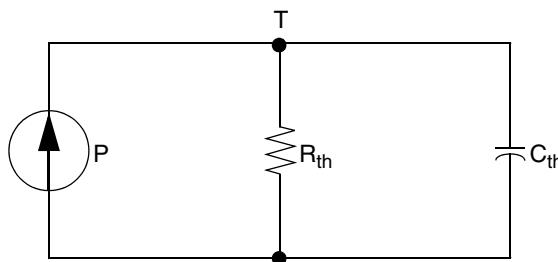
Self heating is turned on if self-heating parameters SHMOD=1 and RTH0 > 0.

SHMOD and RTH0 are also instance parameters. They override the corresponding model parameters.

The effective thermal resistance and capacitance equations and equivalent circuit are:

$$R_{th} = \frac{RTH0}{W_{eff} + WTH0_{eff}}$$

$$C_{th} = CTH0 \cdot (W_{eff} + WTH0_{eff})$$



RPI Poli-Si TFT Model Version 2 Equations

The RPI TFT poly-Si Version 2 model is available in HSPICE. Invoke the model by setting the VERSION parameter to 2.

This section covers the following topics:

- [RPI Poli-Si TFT Model — Version 2 Equations: Threshold Voltage and V_{GS} - V_T](#)
- [RPI Poli-Si TFT Model — Version 2 Equations: Mobility](#)
- [RPI Poli-Si TFT Model — Version 2 Equations: Channel Conductance](#)
- [RPI Poli-Si TFT Model — Version 2 Equations: Saturation Voltage and Effective V_{ds}](#)
- [RPI Poli-Si TFT Model — Version 2 Equations: Drain Current](#)

Chapter 2: MOSFET Models

LEVEL 62: RPI Poli-Si TFT Model

- RPI Poli-Si TFT Model — Version 2 Equations: Total Drain Current, including Kink Effect and Leakage
- RPI Poli-Si TFT Model — Version 2 Equations: Additional Geometry Scaling
- RPI Poli-Si TFT Model — Version 2 Equations: Temperature Dependence

RPI Poli-Si TFT Model — Version 2 Equations: Threshold Voltage and V_{GS}

- V_T

$$V_{Teff} = V_{TX} - \Delta V_{T, DIBL}$$

$$\text{If DIBLMOD} = 0, \text{ then } \Delta V_{T, DIBL} = \frac{AT \cdot V_{DS}^2 + BT}{L_{eff}}$$

else, if DIBLMOD = 1, then

$$\Delta V_{T, DIBL} = \frac{AT \cdot V_{DS}^2 + BT}{L_{eff} \cdot \left[1 + \exp\left(\frac{V_{GS} - VSIGMAT - V_{TX}}{VSIGMA}\right) \right]}$$

otherwise

$$\Delta V_{T, DIBL} = \frac{AT \cdot V_{DS}^2}{L_{eff} \cdot \left[1 + \exp\left(\frac{V_{GS} - VSIGMAT - V_{TX}}{VSIGMA}\right) \right]} + \frac{BT}{L_{eff}}$$

$$V_{GT} = V_{GS} - V_{Teff}$$

$$V_{GTE} = ETA \cdot V_{th} \cdot \left[1 + \frac{V_{GT}}{2 \cdot ETA \cdot V_{th}} + \sqrt{DELTA^2 + \left(\frac{V_{GT}}{2 \cdot ETA \cdot V_{th}} - 1 \right)^2} \right]$$

$$V_{th} = \frac{k_B \cdot TEMP}{q}$$

RPI Poli-Si TFT Model — Version 2 Equations: Mobility

$$\Delta V_{T, DIBL} = \frac{AT \cdot V_{DS}^2}{L_{eff} \cdot \left[1 + \exp\left(\frac{V_{GS} - VSIGMAT - V_{TX}}{VSIGMA}\right) \right]} + \frac{BT}{L_{eff}}$$

$$\mu_{eff} = MUS + \frac{\mu_{FET}}{1 + \frac{THETA}{T_{OX}} \cdot V_{GTE}}$$

$$\frac{1}{\mu_{FET}} = \frac{1}{\mu_0} + \frac{1}{\mu_1 \cdot \left(\frac{2 \cdot V_{GTE}}{\eta \cdot V_{th}} \right)^{MMU}}$$

$$\eta = \frac{ETA}{1 + META \cdot \frac{ETA - 1}{ETA} \cdot r_{i1}}$$

$$r_{i1} = \frac{i_1}{1 + i_1}$$

$$i_1 = \left(\frac{LKINK}{L_{eff}} \right)^{MKINK} \cdot \frac{W_{eff}}{L_{eff}} \cdot \frac{V_{DS} - V_{DSE}}{VKINK} \cdot \exp \left(- \frac{VKINK}{V_{DS} - V_{DSE}} \right)$$

$$V_{DSE} = \frac{V_{DS}}{\left[1 + \left(\frac{V_{DS}}{V_{GTE}} \right)^{MSS} \right]^{MSS}} - V_{th}$$

RPI Poli-Si TFT Model — Version 2 Equations: Channel Conductance

$$g_{ch} = \frac{g_{chi}}{1 + g_{chi} \cdot (R_D + R_S)}, g_{chi} = q \cdot n_s \cdot \mu_{eff} \cdot \frac{W_{eff}}{L_{eff}}$$

$$n_s = \frac{C_{OX} \cdot ETA \cdot V_{TH}}{q} \cdot \log \left[1 + \frac{1}{2} \cdot \exp \left(\frac{V_{GT}}{\eta \cdot V_{th}} \right) \right], C_{OX} = \frac{\epsilon_i}{T_{OX}}$$

RPI Poli-Si TFT Model — Version 2 Equations: Saturation Voltage and Effective V_{ds}

$$V_L = \frac{VMAX_L}{\mu_{eff}}$$

$$I_{sat} = \frac{g_{chi} \cdot V_{GTE}}{1 + \frac{V_{GTE}}{V_L} + g_{chi} \cdot R_S + \sqrt{1 + 2 \cdot g_{chi} \cdot R_S + \left(1 + \frac{V_{GTE}}{V_L} \right)^2}}$$

Chapter 2: MOSFET Models

LEVEL 62: RPI Poli-Si TFT Model

$$V_{Dsat} = \frac{I_{sat}}{g_{ch}}$$

$$I_{choo} = g_{ch} \cdot V_{DS} \cdot \frac{(1 + \lambda \cdot V_{DS})}{\left[1 + \left(\frac{V_{DS}}{V_{Dsat}}\right)^{ME_L}\right]^{\frac{1}{ME_L}}}$$

If ISUBMOD=1, then $\lambda = 0$

otherwise $\lambda = LAMBDA$

$$q_s = q \cdot \left(n_s - I_{choo} \cdot \frac{C_{OX} \cdot R_d}{q} \right)$$

$$V_{satnew} = \frac{2 \cdot VMAX_L \cdot q_s}{q_s \cdot \mu_{eff} + 2 \cdot VMAX_L \cdot \frac{C_{OX}}{\alpha_{SAT}}}$$

$$V_{DS0} = V_{DS} - I_{choo} \cdot (R_D + R_S)$$

$$V_{DSEnew} = \frac{V_{DS0}}{\left[1 + \left(\frac{V_{DS0}}{V_{satnew}}\right)^{MSS}\right]^{\frac{1}{MSS}}} - V_{th}$$

RPI Poli-Si TFT Model — Version 2 Equations: Drain Current

If ISUBMOD = 0, then $I_{dp} = I_{choo}$

otherwise

$$I_{dp} = \frac{I_{choo}}{1 - \frac{\Delta_L}{L_{eff}}}, \quad \Delta_L = \frac{LS \cdot \log\left(1 + \frac{V_{DS0} - V_{DSEnew}}{VP}\right)}{1 + \frac{V_{DSEnew}}{VP} + C_{OX} \cdot \mu_{eff} \cdot R_s \cdot \frac{W_{eff}}{L_{eff}}},$$

RPI Poli-Si TFT Model — Version 2 Equations: Total Drain Current, including Kink Effect and Leakage

$$m = \left(\frac{LKINK}{L_{eff}} \right)^{MKINK} \cdot \frac{V_{DS} - V_{DSEnew}}{VKINK} \cdot \exp\left(-\frac{VKINK}{V_{DS} - V_{DSEnew}}\right)$$

$$I_{ds} = I_{dp} \cdot (1 + m) + I_{leak}$$

The subthreshold leakage current equation is the same as for VERSION=1.

RPI Poli-Si TFT Model — Version 2 Equations: Additional Geometry Scaling

$$\mu_0 = MU0 \cdot \left[1 + \left(\frac{LMU0}{L_{eff}} \right)^2 \right]$$

$$\mu_{1L} = MU1 \cdot \left[1 - \left(\frac{LMU1}{L_{eff}} \right)^2 \right]$$

$$ME_L = ME \cdot \left[1 - \left(\frac{LME}{L_{eff}} \right)^2 \right]$$

RPI Poli-Si TFT Model — Version 2 Equations: Temperature Dependence

$$V_{TX} = VTO - DVTO \cdot (TEMP - TNOM)$$

$$\mu_1 = \mu_{1L} + DMU1 \cdot (TEMP - TNOM)$$

$$\alpha_{sat} = ASAT - \frac{LASAT}{L_{eff}} - DASAT \cdot (TEMP - TNOM)$$

LEVEL 63: Philips MOS11 Model

The Philips MOS Model 11, Level 1101 and 1102, are available as Level 63 in the Synopsys MOSFET models.

Philips MOS Model 11, Level 1102, is an updated version of Level 1101. It uses slightly different equations than Level 1101. The surface potential is calculated iteratively using a second-order Newton-Raphson procedure, resulting in a more accurate description of the surface potential. It includes two types of geometrical scaling rules: physical rules and binning rules. You use the `BINFLAG` parameter to select these rules.

The parasitic diode model includes the Philips JUNCAP Parasitic Diode Model.

The implementation history of the Philips MOS Model 11 is as follows:

| Level | Implementation Description |
|--------|--|
| 1102.1 | <ul style="list-style-type: none">▪ Default of NT (noise parameter) changed from 1.656e-20 to 1.624e-20▪ Bug in noise equation for induced gate noise fixed.▪ Maximum temperature limiting for self-heating implemented. |
| 1102 | <ul style="list-style-type: none">▪ Iterative solution of surface potential.▪ More accurate, physics-based implementation of velocity saturation effects.▪ More accurate, physics-based equations for thermal noise, induced gate noise, and their correlations.▪ Self-heating implemented.▪ Temperature dependence parameter of the thermal resistance, <code>ATH</code>, added.▪ Internal variable <code>VDBt</code> was simplified, which results in a more physical description for $V_{DS} < 0$.▪ Definition of starting condition of surface potential Ψ_s and Y_{ov} rewritten to increase numerical efficiency and to avoid possible floating-point exceptions. |
| 1101.6 | <ul style="list-style-type: none">▪ Default value of NT (noise parameter) changed from 1.656e-20 to 1.624e-20.▪ Handling of low limit of internal variable, G_{mob}, simplified.▪ Maximum temperature limiting for self-heating implemented. |
| 1101.5 | Added temperature dependence parameter of the thermal resistance (<code>ATH</code>). |
| 1101.4 | Improved thermal noise density. |
| 1101.2 | Self-heating implementation. |

This section covers the following topics:

- [Using the Philips MOS11 Model](#)
 - [Philips MOS11 Model Parameters](#)
 - [Philips MOS11 Model Examples](#)
-

Using the Philips MOS11 Model

To use the Philips MOS11 model:

1. Set LEVEL=63 to identify the model as Philips MOS Model 11.
2. Set the MOS11 version:
 - Set VERSION=1102.1 (default) to identify the model as Level 1102.1
 - Set VERSION=1102.0 to identify the model as Level 1102.0
 - Set VERSION=1101.6 to identify the model as Level 1101.6
 - Set VERSION=1101.5 to identify the model as Level 1101.5
 - Set VERSION=1101.4 to identify the model as Level 1101.4
 - Set VERSION=1101.2 to identify the model as Level 1101.2
 - Set VERSION=1101.1 to identify the model as Level 1101.1
 - Set VERSION=1101.0 to identify the model as Level 1101.0
 - Set VERSION=1100.3 to identify the model as Level 1100.3
 - Set VERSION=1100.2 to identify the model as Level 1100.2
 - Set VERSION=1100.1 to identify the model as Level 1100.1
 - Set VERSION=1100.0 to identify the model as Level 1100.0
3. Set the flag for binned model:
 - Set BINFLAG=0 (default) to select the physical geometry scaling rules.
 - Set BINFLAG=1 to select the binning geometry scaling rules.
4. The existing version is internally switched for backward compatibility as follows:
 - VERSION=11010 switched to VERSION=1101.1 and BINFLAG=0
 - VERSION=11011 switched to VERSION=1101.1 and BINFLAG=1
5. Set the flag for self-heating:

Chapter 2: MOSFET Models

LEVEL 63: Philips MOS11 Model

- Set `SHMOD=0` (default) to select no self-heating.
 - Set `SHMOD=1` to select self-heating.
6. The default room temperature is 25°C in Synopsys circuit simulators, but is 27°C in most other simulators. When comparing to other simulators, use `.TEMP 27` or `.OPTION TNOM=27` to set the simulation temperature to 27 in the netlist.
 7. The set of model parameters should always include the `TR` model reference temperature which corresponds to `TREF` in other levels in the Synopsys MOSFET model levels. The default for `TR` is 21.0 to match the Philips simulator.
 8. This model has its own charge-based capacitance model. This model ignores the `CAPOP` parameter, which selects different capacitance models.
 9. This model uses analytical derivatives for the conductances. This model ignores the `DERIV` parameter, which selects the finite difference method.
 10. You can use `DTEMP` with this model to increase the temperature of individual elements, relative to the circuit temperature. Set `DTEMP` on the element line.
 11. Because the defaults are non-zero, you should set *every* Level 63 model parameter in the Model Parameters table in the `.MODEL` statement.
 12. The general syntax for the MOSFET element is the same as the other standard MOSFET models, other than `PS` and `PD`. In Level 63, `PS` and `PD` are the length of the sidewall of the source/drain, which is not under the gate.
 13. Philips MOS11 has its own `LMIN` parameter, which has a different definition from that of HSPICE. To avoid the conflict with `LMIN` in simulation, Synopsys changed the `LMIN` parameter in the Level 63 MOSFET model to `LLMIN`.

Philips MOS11 Model Parameters

This section covers the following topics:

- [Philips MOS11 Model — Control, Geometry, and Self-Heating Parameters](#)
- [Philips MOS11 Model — Physical Geometry Scaling](#)
- [Philips MOS11 Model — Binning Geometry Scaling](#)
- [Philips MOS11 Model — JUNCAP Parameters](#)

Philips MOS11 Model — Control, Geometry, and Self-Heating Parameters

| Name (Alias) | Description | Units | NMOS | PMOS |
|--------------|--|-------|--------|--------|
| LEVEL | Level of this model | - | 63 | 63 |
| VERSION | Version of this model | | 1102.1 | 1102.1 |
| BINFLAG | Flag for binned model <ul style="list-style-type: none">■ 0: physical model■ 1: binned model | - | 0 | 0 |
| ATH | Temperature coefficient of thermal resistance | - | 0 | 0 |
| CTH | Thermal capacitance | J/K- | 3e-9 | 3e-9 |
| DTA | Temperature offset of the device | °C | 0 | 0 |
| LAP | Effective channel length reduction per side, due to the lateral diffusion of source/drain dopant ions | m | 4e-8 | 4e-8 |
| LER | Effective channel length, reference transistor | m | 1e-6 | 1e-6 |
| LVAR | Difference between the actual and programmed poly silicon gate length | m | 0 | 0 |
| RTH | Thermal resistance | K/W | 300 | 300 |
| SHMOD | Flag for self-heating <ul style="list-style-type: none">■ 0: no self-heating■ 1: self-heating | - | 0 | 0 |
| TR | Temperature at which simulation determines the reference transistor parameters | °C | 21 | 21 |
| WER | Effective channel width, reference transistor | m | 1e-5 | 1e-5 |
| WOT | Effective reduction of the channel width per side due to the lateral diffusion of the channel stop dopant ions | m | 0 | 0 |
| WVAR | Difference between the actual and programmed field oxide opening | m | 0 | 0 |

Philips MOS11 Model — Physical Geometry Scaling

| Name (Alias) | Description | Units | NMOS | PMOS |
|---------------------|--|------------------|----------|---------|
| A1R | Weak-avalanche current factor for reference transistor at reference temperature | - | 6 | 6 |
| A2R | Exponent of the weak-avalanche current for the reference transistor | V | 38 | 38 |
| A3R | Drain-source voltage factor, above which weak-avalanche occurs for reference transistor | - | 1 | 1 |
| AGIDL | Gain factor for gate-induced drain leakage current for a channel width of 1 um | AV ⁻³ | 0 | 0 |
| ALPEXP | Exponent of the length dependence of α | - | 1 | 1 |
| ALPR | Factor of the channel length modulation for the reference transistor | - | 1e-2 | 1e-2 |
| BACC | Probability factor for intrinsic gate tunneling current in accumulation | V | 48 | 48 |
| BETSQ | Gain factor for an infinite square transistor at the reference temperature | AV ⁻² | 3.709e-4 | 1.15e-4 |
| BGIDL | Probability factor for gate-induced drain leakage current at the reference temperature | V | 41.0 | 41.0 |
| BINV | Probability factor for intrinsic gate tunneling current in inversion | V | 48 | 87.5 |
| CGIDL | Factor for the lateral field dependence of the gate-induced drain leakage current | - | 0 | 0 |
| COL | Gate overlap capacitance per unit channel length | F | 3.2e-16 | 3.2e-16 |
| ETABETR (ETABET) | Exponent of the temperature dependence of the gain factor | - | 1.3 | 0.5 |
| ETAMOBR | Effective field parameter, depletion/ inversion charge dependence for reference transistor | - | 1.4 | 3 |
| ETAPH | Exponent of the temperature dependence of θ_{sr} for the reference temperature | - | 1.35 | 3.75 |
| ETAR | Exponent of temperature dependence of θ_R | - | 0.95 | 0.4 |
| ETASAT | Exponent of temperature dependence of θ_{sat} | - | 1.04 | 0.86 |

| Name (Alias) | Description | Units | NMOS | PMOS |
|--------------|---|---------------------------------|----------|----------|
| ETASR | Exponent of temperature dependence of θ_{sr} | - | 0.65 | 0.5 |
| FBET1 | Relative mobility decrease due to first lateral profile | - | 0 | 0 |
| FBET2 | Relative mobility decrease due to second lateral profile | - | 0 | 0 |
| GATENOISE | In/exclusion flag of induced gate thermal noise | - | 0 | 0 |
| IGACCR | Gain factor for intrinsic gate tunneling current in accumulation for reference transistor | AV ⁻² | 0 | 0 |
| IGINVR | Gain factor for intrinsic gate tunneling current in inversion for reference transistor | AV ⁻² | 0 | 0 |
| IGOVR | Gain factor for Source/Drain overlap tunneling current for reference transistor | AV ⁻² | 0 | 0 |
| KOR | Body-effect factor for the reference transistor | V ^{1/2} | 0.5 | 0.5 |
| KOV | Body-effect factor for the Source/Drain overlap extensions | V ^{1/2} | 2.5 | 2.5 |
| KPINV | Inverse of the body-effect factor, poly-silicon gate | V ^{-1/2} | 0 | 0 |
| LLMIN | Minimum effective channel length in technology, calculates smoothing factor m | M | 1.5e-7 | 1.5e-7 |
| LP1 | Characteristic length of first lateral profile | m | 8e-7 | 8e-7 |
| LP2 | Characteristic length of second lateral profile | M | 8e-7 | 8e-7 |
| MOEXP | Exponent of the length dependence of m_0 | - | 1.34 | 1.34 |
| MOO | Parameter for short-channel subthreshold slop | | 0 | 0 |
| MOR | Parameter for short-channel subthreshold slope for the reference transistor | - | 0 | 0 |
| NFAR | First coefficient of the flicker noise for the reference transistor | V ⁻¹ m ⁻⁴ | 1.573e23 | 3.825e24 |
| NFBR | Second coefficient of the flicker noise for the reference transistor | V ⁻¹ m ⁻² | 4.752e9 | 1.015e9 |
| NFCR | Third coefficient of the flicker noise for the reference transistor | V ⁻¹ | 0 | 7.3e-8 |

Chapter 2: MOSFET Models

LEVEL 63: Philips MOS11 Model

| Name (Alias) | Description | Units | NMOS | PMOS |
|--------------|---|-------------------|-----------|-----------|
| NT | Thermal noise coefficient at the actual temperature | J | 1.624e-20 | 1.624e-20 |
| NU (NUR) | Exponent of field dependence, mobility model minus 1 (such as v-1) at reference temperature | - | 2 | 2 |
| NUEXP | Exponent of the temperature dependence of parameter v | - | 5.25 | 3.23 |
| PHIBR | Surface potential at the onset of strong inversion at the reference temperature | V | 0.95 | 0.95 |
| SDIBLEXP | Exponent of length dependence of ϕ_{DIBL} | - | 1.35 | 1.35 |
| SDIBLO | Drain-induced barrier-lowering parameter for the reference transistor | V ^{-1/2} | 1e-4 | 1e-4 |
| SL2KO | Second coefficient of the length dependence of k_0 | - | 0 | 0 |
| SL2PHIB | Second coefficient of length dependence of ϕ_B | - | 0 | 0 |
| SLA1 | Coefficient of the length dependence of a^1 | - | 0 | 0 |
| SLA2 | Coefficient of the length dependence of a^2 | - | 0 | 0 |
| SLA3 | Coefficient of the length dependence of a^3 | - | 0 | 0 |
| SLALP | Coefficient of the length dependence of α | - | 1 | 1 |
| SLETABET | Length dependence coefficient of β_R | - | 0 | 0 |
| SLKO | Coefficient of the length dependence of k_0 | - | 0 | 0 |
| SLPHIB | Coefficient of the length dependence of ϕ_B | - | 0 | 0 |
| SLSSF | Length dependence coefficient of α_{sf} | - | 1.0 | 1.0 |
| SLTHESAT | Length dependence coefficient of θ_{sat} | - | 1 | 1 |
| SSFR | Static feedback parameter, reference transistor | V ^{-1/2} | 6.25e-3 | 6.25e-3 |
| STA1 | Temperature dependence coefficient of a^1 | K ⁻¹ | 0 | 0 |
| STBGIDL | Coefficient of the temperature dependence of B_{GIDL} | VK ⁻¹ | -3.638e-4 | -3.638e-4 |

| Name (Alias) | Description | Units | NMOS | PMOS |
|--------------|--|------------------|---------|---------|
| STETAMOB | Temperature dependence coefficient of η_{mob} | K ⁻¹ | 0 | 0 |
| STPHIB | Temperature dependence coefficient of ϕ_B | VK ⁻¹ | -8.5e-4 | -8.5e-4 |
| STVFB | Temperature dependence coefficient of V_{FB} | V/K | 5e-4 | 5e-4 |
| SWA1 | Coefficient of the width dependence of a^1 | - | 0 | 0 |
| SWA2 | Coefficient of the width dependence of a^2 | - | 0 | 0 |
| SWA3 | Coefficient of the width dependence of a^3 | - | 0 | 0 |
| SWALP | Coefficient of the width dependence of α | - | 0 | 0 |
| SWETAMOB | Width dependence coefficient of η_{mob} | - | 0 | 0 |
| SWKO | Coefficient of the width dependence of k_0 | - | 0 | 0 |
| SWPHIB | Coefficient of the width dependence of ϕ_B | - | 0 | 0 |
| SWSSF | Coefficient of the width dependence of α_{sf} | - | 0 | 0 |
| SWTHEPH | Coefficient of the width dependence of θ_{sr} | - | 0 | 0 |
| SWTHER | Coefficient of the width dependence of θ_R | - | 0 | 0 |
| SWTHESAT | Width dependence coefficient of θ_{sat} | - | 0 | 0 |
| SWTHESR | Coefficient of the width dependence of θ_{sr} | - | 0 | 0 |
| SWTHETH | Coefficient of the width dependence of θ_{TH} | - | 0 | 0 |
| THEPHR | Coefficient of the mobility reduction due to phonon scattering for the reference transistor at the reference temperature | V ⁻¹ | 1.29e-2 | 1e-3 |
| THER1 | Numerator of gate voltage dependent part of series resistance for reference transistor | V | 0 | 0 |
| THER2 | Denominator of gate voltage dependent part of series resistance for the reference transistor | V | 1 | 1 |
| THERR | Series resistance coefficient for reference transistor at reference temperature | V ⁻¹ | 0.155 | 0.08 |

Chapter 2: MOSFET Models

LEVEL 63: Philips MOS11 Model

| Name (Alias) | Description | Units | NMOS | PMOS |
|--------------|---|-----------------|--------|--------|
| THESATEXP | Exponent of length dependence of θ_{sat} | - | 1 | 1 |
| THESATR | Velocity saturation parameter due to optical/acoustic phonon scattering for the reference transistor at the reference temperature | V ⁻¹ | 0.5 | 0.2 |
| THESRR | Mobility reduction coefficient, due to surface roughness scattering for reference transistor at reference temperature | V ⁻¹ | 0.4 | 0.73 |
| THETHEXP | Exponent of the length dependence of θ_{TH} | - | 1 | 1 |
| THETHR | Coefficient of self-heating for the reference transistor at the reference temperature | V ⁻³ | 1e-3 | 0.5e-3 |
| TOX | Thickness of the gate oxide layer | M | 3.2e-9 | 3.2e-9 |
| VFBOV | Flat-band voltage for the Source/Drain overlap extensions | V | 0 | 0 |
| VFBR (VFB) | Flat-band voltage for the reference transistor at the reference temperature | V | -1.05 | -1.05 |
| VP | Characteristic voltage of the channel length modulation | V | 5e-2 | 5e-2 |

Philips MOS11 Model — Binning Geometry Scaling

| Name (Alias) | Description | Units | NMOS | PMOS |
|--------------|---|-------------------|-----------|-----------|
| GATENOISE | Inclusion/exclusion flag of the induced gate thermal noise | - | 0 | 0 |
| KOV | Body-effect factor for the source/drain overlap extensions | V ^{1/2} | 2.5 | 2.5 |
| KPINV | Inverse of body-effect factor, poly-silicon gate | V ^{-1/2} | 0 | 0 |
| NT | Coefficient for the thermal noise at the reference temperature | J | 1.656e-20 | 1.656e-20 |
| NU | Exponent of the field dependence of the mobility model at the reference temperature | - | 2 | 2 |
| PLA1 | Coefficient for the length-dependent part of a^1 | - | 0 | 0 |
| PLA2 | Coefficient for the length-dependent part of a^2 | V | 0 | 0 |

| Name (Alias) | Description | Units | NMOS | PMOS |
|--------------|---|----------------|------|------|
| PLA3 | Coefficient for the length-dependent part of a^3 | - | 0 | 0 |
| PLAGIDL | Coefficient for the length dependence of A_{GIDL} | AV^{-3} | 0 | 0 |
| PLALP | Coefficient for the length-dependent part of α | - | 0 | 0 |
| PLBACC | Coefficient for the length-dependent part of B_{ACC} | V | 0 | 0 |
| PLBET | Coefficient for the length dependent of β | AV^{-2} | 0 | 0 |
| PLBGIDL | Coefficient for the length dependence of B_{GIDL} | V | 0 | 0 |
| PLBINV | Coefficient for the length-dependent part of I_{GINV} | V | 0 | 0 |
| PLCGDO | Coefficient for the length-dependent part of C_{GDO} | F | 0 | 0 |
| PLCGIDL | Coefficient for the length dependence of C_{GIDL} | | 0 | 0 |
| PLCGSO | Coefficient for the length-dependent part of C_{GSO} | F | 0 | 0 |
| PLCOX | Coefficient for the length-dependent part of C_{OX} | F | 0 | 0 |
| PLETAMOB | Coefficient, length-dependent n_{mob} part | - | 0 | 0 |
| PLIGACC | Coefficient for the length-dependent part of I_{GACC} | AV^{-2} | 0 | 0 |
| PLIGINV | Coefficient for the length-dependent part of I_{GINV} | AV^{-2} | 0 | 0 |
| PLIGOV | Coefficient for the length-dependent part of I_{GOV} | AV^{-2} | 0 | 0 |
| PLKO | Coefficient for the length dependent of k_0 | $V^{1/2}$ | 0 | 0 |
| PLMEXP | Coefficient for the length-dependent part of $1/m$ | - | 0 | 0 |
| PLMO | Coefficient for the length-dependent part of m_0 | - | 0 | 0 |
| PLNFA | Coefficient for the length-dependent part of N_{FA} | $V^{-1}m^{-4}$ | 0 | 0 |
| PLNFB | Coefficient for the length-dependent part of N_{FB} | $V^{-1}m^{-2}$ | 0 | 0 |
| PLNFC | Coefficient for the length-dependent part of N_{FC} | V^{-1} | 0 | 0 |
| PLPHIB | Coefficient for the length dependent of Φ_B | V | 0 | 0 |

Chapter 2: MOSFET Models

LEVEL 63: Philips MOS11 Model

| Name (Alias) | Description | Units | NMOS | PMOS |
|--------------|--|-------------------|------|------|
| PLSDIBL | Coefficient for the length-dependent part of σ_{dibl} | V ^{-1/2} | 0 | 0 |
| PLSSF | Coefficient for the length-dependent part of σ_{sf} | V ^{-1/2} | 0 | 0 |
| PLTA1 | Coefficient for the length-dependent part of $S_T:a^1$ | K ⁻¹ | 0 | 0 |
| PLTBGIDL | Coefficient for the length dependence of $S_T:B_{GIDL}$ | VK ⁻¹ | 0 | 0 |
| PLTETABET | Coefficient for the length-dependent part of $\tau\beta$ | - | 0 | 0 |
| PLTETAMOB | Coefficient for the length-dependent part of η_{bh} | K ⁻¹ | 0 | 0 |
| PLTETAPH | Coefficient for the length-dependent part of η_{bh} | - | 0 | 0 |
| PLTETAR | Coefficient for the length-dependent part of η_R | - | 0 | 0 |
| PLTETASAT | Coefficient for the length-dependent part of η_{sat} | - | 0 | 0 |
| PLTETASR | Coefficient for the length-dependent part of η_{sr} | - | 0 | 0 |
| PLTHEPH | Coefficient for the length dependent of θ_{ph} | V ⁻¹ | 0 | 0 |
| PLTHER | Coefficient for the length-dependent part of θ_R | V ⁻¹ | 0 | 0 |
| PLTHESAT | Coefficient for length-dependent part of θ_{sat} | V ⁻¹ | 0 | 0 |
| PLTHESR | Coefficient for the length dependent part of θ_{sr} | V ⁻¹ | 0 | 0 |
| PLTHETH | Coefficient for the length-dependent part of θ_{TH} | V ⁻³ | 0 | 0 |
| PLTNUEXP | Coefficient for the length-dependent part of v_{exp} | - | 0 | 0 |
| PLTPHIB | Coefficient for the length-dependent part of $ST;\phi_B$ | VK ⁻¹ | 0 | 0 |
| PLTVFB | Coefficient for the length-dependent part of $ST;V_{FB}$ | VK ⁻¹ | 0 | 0 |
| PLWA1 | Coefficient for the length times width a ¹ dependent part | - | 0 | 0 |
| PLWA2 | Coefficient of the length times width a ² dependent part | V | 0 | 0 |

| Name (Alias) | Description | Units | NMOS | PMOS |
|--------------|---|-----------|------|------|
| PLWA3 | Coefficient for the length times width a^3 dependent part | - | 0 | 0 |
| PLWAGIDL | Coefficient for the width over length dependence of A_{GIDL} | AV^{-3} | 0 | 0 |
| PLWALP | Coefficient for the length times width dependent part of α | - | 0 | 0 |
| PLWBACC | Coefficient for the length times width dependent part of B_{ACC} | V | 0 | 0 |
| PLWBET | Coefficient, width over length dependent of β | AV^{-2} | 0 | 0 |
| PLWBGIDL | Coefficient for the length times width dependence of B_{GIDL} | V | 0 | 0 |
| PLWBINV | Coefficient for the length times width dependent part of I_{GINV} | V | 0 | 0 |
| PLWCGDO | Coefficient for the width over length dependent part of C_{GDO} | F | 0 | 0 |
| PLWCGIDL | Coefficient for the length times width dependence of C_{GIDL} | | 0 | 0 |
| PLWCGSO | Coefficient for the width over length dependent part of C_{GSO} | F | 0 | 0 |
| PLWCOX | Coefficient for the length times width dependent part of C_{OX} | F | 0 | 0 |
| PLWETAMOB | Coefficient, length times width dependent n_{mob} part | - | 0 | 0 |
| PLWHEPH | Coefficient, length times width, θ_{ph} dependent | V^{-1} | 0 | 0 |
| PLWIGACC | Coefficient for the length times width dependent part of I_{GACC} | AV^{-2} | 0 | 0 |
| PLWIGINV | Coefficient for the length times width dependent part of I_{GINV} | AV^{-2} | 0 | 0 |
| PLWIGOV | Coefficient for the width over length dependent part of I_{GOV} | AV^{-2} | 0 | 0 |
| PLWKO | Coefficient, length times width k_0 dependent | $V^{1/2}$ | 0 | 0 |

Chapter 2: MOSFET Models

LEVEL 63: Philips MOS11 Model

| Name (Alias) | Description | Units | NMOS | PMOS |
|--------------|---|----------------|------|------|
| PLWMEXP | Coefficient of the length times width 1/m dependent part | - | 0 | 0 |
| PLWMO | Coefficient for the length times width m_0 dependent part | - | 0 | 0 |
| PLWNFA | Coefficient for the length times width dependent part of N_{FA} | $V^{-1}m^{-4}$ | 0 | 0 |
| PLWNFB | Coefficient for the length times width dependent part of N_{FB} | $V^{-1}m^{-2}$ | 0 | 0 |
| PLWNFC | Coefficient for the length times width dependent part of N_{FC} | V^{-1} | 0 | 0 |
| PLWPHIB | Coefficient, length times width Φ_B dependent | V | 0 | 0 |
| PLWSDIBL | Coefficient, length times width dependent of σ_{dibl} | $V^{-1/2}$ | 0 | 0 |
| PLWSSF | Coefficient for the length times width σ_{sf} dependent part | $V^{-1/2}$ | 0 | 0 |
| PLWTA1 | Coefficient for the length times width dependent part of $S_T:a^1$ | K^{-1} | 0 | 0 |
| PLWTBGIDL | Coefficient for the length times width dependence of $S_T:B_{GIDL}$ | VK^{-1} | 0 | 0 |
| PLWTETABET | Coefficient for the length times width η_{br} dependent part | - | 0 | 0 |
| PLWTETAMOB | Coefficient for the length times width dependent part of η_{bh} | K^{-1} | 0 | 0 |
| PLWTETAPH | Coefficient for the length times width η_{ph} dependent part | - | 0 | 0 |
| PLWTETAR | Coefficient for the length times width dependent part of η_R | - | 0 | 0 |
| PLWTETASAT | Coefficient for the length times width dependent part of η_{sat} | - | 0 | 0 |
| PLWTETASR | Coefficient for the length times width dependent part of η_{br} | - | 0 | 0 |

| Name (Alias) | Description | Units | NMOS | PMOS |
|--------------|---|------------------|-----------|-----------|
| PLWTHER | Coefficient, length times width θR dependent | V ⁻¹ | 0 | 0 |
| PLWTHESAT | Coefficient, length times width θ_{sat} dependent | V ⁻¹ | 0 | 0 |
| PLWTHESR | Coefficient, length times width, θ_{sr} dependent | V ⁻¹ | 0 | 0 |
| PLWTHETH | Coefficient for the length times width θ_{TH} dependent part | V ⁻³ | 0 | 0 |
| PLWTNUEXP | Coefficient fore the length times width dependent part of v_{exp} | - | 0 | 0 |
| PLWTPHIB | Coefficient for the length times width dependent part of ST; ϕ_B | VK ⁻¹ | 0 | 0 |
| PLWTVFB | Coefficient for the length times width dependent part of ST; V_{FB} | VK ⁻¹ | 0 | 0 |
| POA1 | Coefficient of the geometry-independent a^1 part | - | 6.022 | 6.858 |
| POA2 | Coefficient for the geometry-independent a^2 part | V | 3.802e1 | 5.732e1 |
| POA3 | Coefficient of the geometry-independent a^3 part | - | 6.407e-1 | 4.254e-1 |
| POAGIDL | Coefficient for the geometry-independent part of A_{GIDL} | AV ⁻³ | 0 | 0 |
| POALP | Coefficient for the geometry-independent part of α | - | 2.5e-2 | 2.5e-2 |
| POBACC | Coefficient for the geometry-independent part of B_{ACC} | V | 48 | 48 |
| POBET | Coefficient, geometry independent β part | AV ⁻² | 1.922e-3 | 3.814e-4 |
| POBGIDL | Coefficient for the geometry independent part of B_{GIDL} | V | 41.0 | 41.0 |
| POBINV | Coefficient for the geometry-independent part of I_{GINV} | V | 48 | 87.5 |
| POCGDO | Coefficient for the geometry-independent C_{GDO} part | F | 6.392e-15 | 6.358e-15 |
| POCGIDL | Coefficient for the geometry independent part of C_{GIDL} | | 0 | 0 |

Chapter 2: MOSFET Models

LEVEL 63: Philips MOS11 Model

| Name (Alias) | Description | Units | NMOS | PMOS |
|--------------|---|---------------------------------|-----------|-----------|
| POCGSO | Coefficient for the geometry-independent part of C_{GSO} | F | 6.392e-15 | 6.358e-15 |
| POCOX | Coefficient for the geometry-independent C_{OX} part | F | 2.98e-14 | 2.717e-14 |
| POETAMOB | Coefficient, geometry independent η_{mob} part | - | 1.40 | 3 |
| POIGACC | Coefficient for the geometry-independent part of I_{GACC} | AV ⁻² | 0 | 0 |
| POIGINV | Coefficient for the geometry-independent part of I_{GINV} | AV ⁻² | 0 | 0 |
| POIGOV | Coefficient for the geometry-independent part of I_{GOV} | AV ⁻² | 0 | 0 |
| POKO | Coefficient, geometry independent k_0 part | V ^{1/2} | 0.5 | 0.5 |
| POMEXP | Coefficient for the geometry-independent 1/m part | - | 0.2 | 0.2 |
| POMO | Coefficient for the geometry-independent part of m_0 | - | 0 | 0 |
| PONFA | Coefficient for the geometry-independent N_{FA} part | V ⁻¹ m ⁻⁴ | 8.323e22 | 1.90e22 |
| PONFB | Coefficient for the geometry-independent N_{FB} part | V ⁻¹ m ⁻² | 2.514e7 | 5.043e6 |
| PONFC | Coefficient for the geometry-independent N_{FC} part | V ⁻¹ | 0 | 3.627e-10 |
| POPHIB | Coefficient, geometry independent Φ_B part | V | 0.950 | 0.950 |
| POSDBL | Coefficient for the geometry-independent part of C_{dbl} | V ^{-1/2} | 8.53e-4 | 3.551e-5 |
| POSSF | Coefficient for the geometry-independent part of α_{sf} | V ^{-1/2} | 1.2e-2 | 1.0e-2 |
| POTA1 | Coefficient for the geometry-independent $S_T:a^1$ part | K ⁻¹ | 0 | 0 |
| POTBGIDL | Coefficient for the geometry independent part of $S_T:B_{GIDL}$ | VK ⁻¹ | -3.638e-4 | -3.638e-4 |

| Name (Alias) | Description | Units | NMOS | PMOS |
|--------------|---|-----------|----------|----------|
| POTETABET | Coefficient for the geometry-independent part of τ_B | - | 1.30 | 0.5 |
| POTETAMOB | Coefficient for the geometry-independent part of $ST;\eta_{ph}$ | K^{-1} | 0 | 0 |
| POTETAPH | Coefficient for the geometry-independent η_{ph} part | - | 1.35 | 3.75 |
| POTETAR | Coefficient for the geometry-independent η_R part | - | 0.95 | 0.4 |
| POTETASAT | Coefficient for the geometry-independent part of η_{sat} | - | 1.04 | 0.86 |
| POTETASR | Coefficient for the geometry-independent τ_{sr} part | - | 0.65 | 0.5 |
| POTHEPH | Coefficient, geometry independent θ_{ph} part | V^{-1} | 1.290e-2 | 1.0e-3 |
| POTHER | Coefficient for the geometry-independent part of θ_R | V^{-1} | 8.12e-2 | 7.9e-2 |
| POTHESAT | Coefficient for the geometry-independent part of θ_{sat} | V^{-1} | 2.513e-1 | 1.728e-1 |
| POTHESR | Coefficient, geometry independent θ_{sr} part | V^{-1} | 3.562e-1 | 7.30e-1 |
| POTHETH | Coefficient for the geometry-independent part of θ_{TH} | V^{-3} | 1.0e-5 | 0 |
| POTNUEXP | Coefficient for the geometry-independent v_{exp} part | - | 5.25 | 3.23 |
| POTPHIB | Coefficient for the geometry-independent part of $ST;\phi_B$ | VK^{-1} | -8.5e-4 | -8.5e-4 |
| POTVFB | Coefficient for the geometry-independent part of $ST;V_{FB}$ | VK^{-1} | 5.0e-4 | 5.0e-4 |
| PWA1 | Coefficient for the width-dependent part of a^1 | - | 0 | 0 |
| PWA2 | Coefficient for the width-dependent part of a^2 | V | 0 | 0 |
| PWA3 | Coefficient for the width-dependent part of a^3 | - | 0 | 0 |
| PWAGIDL | Coefficient for the width dependence of A_{GIDL} | AV^{-3} | 0 | 0 |
| PWALP | Coefficient for the width-dependent part of α | - | 0 | 0 |

Chapter 2: MOSFET Models

LEVEL 63: Philips MOS11 Model

| Name (Alias) | Description | Units | NMOS | PMOS |
|--------------|---|----------------|------|------|
| PWBACC | Coefficient for the width-dependent part of B_{ACC} | V | 0 | 0 |
| PWBET | Coefficient for the width dependent of β | AV^{-2} | 0 | 0 |
| PWBGIDL | Coefficient for the width dependence of B_{GIDL} | V | 0 | 0 |
| PWBINV | Coefficient for the width-dependent part of I_{GINV} | V | 0 | 0 |
| PWCGDO | Coefficient for the width dependent part of C_{GDO} | F | 0 | 0 |
| PWCgidl | Coefficient for the width dependence of C_{GIDL} | | 0 | 0 |
| PWCgso | Coefficient for the width-dependent part of C_{GSO} | F | 0 | 0 |
| PWCOX | Coefficient for the width-dependent part of C_{OX} | F | 0 | 0 |
| PWETAMOB | Coefficient, width-dependent n_{mob} part | - | 0 | 0 |
| PWIGACC | Coefficient for the width-dependent part of I_{GACC} | AV^{-2} | 0 | 0 |
| PWIGINV | Coefficient for the width-dependent part of I_{GINV} | AV^{-2} | 0 | 0 |
| PWIGOV | Coefficient for the width-dependent part of I_{GOV} | AV^{-2} | 0 | 0 |
| PWKO | Coefficient for the width dependent of k_0 | $V^{1/2}$ | 0 | 0 |
| PWMEXP | Coefficient for the width dependent part of $1/m$ | - | 0 | 0 |
| PWMO | Coefficient for the width-dependent part of m_0 | - | 0 | 0 |
| PWNFA | Coefficient for the width-dependent part of N_{FA} | $V^{-1}m^{-4}$ | 0 | 0 |
| PWNFB | Coefficient for the width-dependent part of N_{FB} | $V^{-1}m^{-2}$ | 0 | 0 |
| PWNFC | Coefficient for the width-dependent part of N_{FC} | V^{-1} | 0 | 0 |
| PWPhib | Coefficient for the width dependent of Φ_B | V | 0 | 0 |
| PWSDIBL | Coefficient for the width-dependent part of σ_{dibl} | $V^{-1/2}$ | 0 | 0 |
| PWSSF | Coefficient for the width-dependent part of σ_{sf} | $V^{-1/2}$ | 0 | 0 |
| PWTA1 | Coefficient for the width-dependent part of $S_T:a^1$ | K^{-1} | 0 | 0 |

| Name (Alias) | Description | Units | NMOS | PMOS |
|--------------|--|------------------|--------|--------|
| PWTBGIDL | Coefficient for the width dependence of $S_T; B_{GIDL}$ | VK ⁻¹ | 0 | 0 |
| PWTETABET | Coefficient for the width-dependent part of $\eta\beta$ | - | 0 | 0 |
| PWTETAMOB | Coefficient for the width-dependent part of η_{ph} | K ⁻¹ | 0 | 0 |
| PWTETAPH | Coefficient for the width-dependent part of η_{ph} | - | 0 | 0 |
| PWTETAR | Coefficient for the width-dependent part of η_R | - | 0 | 0 |
| PWTETASAT | Coefficient for the width-dependent part of η_{sat} | - | 0 | 0 |
| PWTETASR | Coefficient for the width-dependent part of η_{sr} | - | 0 | 0 |
| PWTHEPH | Coefficient for the width dependent of θ_{ph} | V ⁻¹ | 0 | 0 |
| PWTHER | Coefficient for the width dependent part of θ_R | V ⁻¹ | 0 | 0 |
| PWTHESAT | Coefficient for the width-dependent part of θ_{sat} | V ⁻¹ | 0 | 0 |
| PWTHESR | Coefficient for the width dependent part of θ_{sr} | V ⁻¹ | 0 | 0 |
| PWTHETH | Coefficient for the width-dependent part of θ_{TH} | V-3 | 0 | 0 |
| PWTNUEXP | Coefficient for the width-dependent part of v_{exp} | - | 0 | 0 |
| PWTPHIB | Coefficient for the width-dependent part of $ST; \phi_B$ | VK ⁻¹ | 0 | 0 |
| PWTVFBI | Coefficient for the width-dependent part of $ST; V_{FB}$ | VK ⁻¹ | 0 | 0 |
| THER1 | Numerator of the gate voltage dependent part of the series resistance for all transistors in bin | V | 0 | 0 |
| THER2 | Denominator of the gate voltage dependent part of the series resistance for all transistors in the bin | V | 1.0 | 1.0 |
| TOX | Thickness of the gate oxide layer | m | 3.2e-9 | 3.2e-9 |
| VFB | Flat-band voltage for the reference transistor at the reference temperature | V | -1.05 | -1.05 |
| VFBOV | Flatband voltage for the source/drain overlap extensions | V | 0 | 0 |

Chapter 2: MOSFET Models

LEVEL 63: Philips MOS11 Model

| Name (Alias) | Description | Units | NMOS | PMOS |
|--------------|---|-------|------|------|
| VP | Characteristic voltage of the channel length modulation | V | 5e-2 | 5e-2 |

Philips MOS11 Model — JUNCAP Parameters

| Name | Description | Units | Default |
|-------|--|------------------|---------|
| CJBR | Bottom junction capacitance at $V=V_R$ | Fm ⁻² | 1e-12 |
| CJGR | Gate edge junction capacitance at $V=V_R$ | Fm ⁻¹ | 1e-12 |
| CJSR | Sidewall junction capacitance at $V=V_R$ | Fm ⁻¹ | 1e-12 |
| DTA | Temperature offset of the JUNCAP element with respect to T_A | °C | 0 |
| JSDBR | Bottom saturation-current density due to diffusion from back contact | Am ⁻² | 1e-03 |
| JSDGR | Gate edge saturation-current density due to back-contact diffusion | Am ⁻¹ | 1e-03 |
| JSDSR | Sidewall saturation-current density due to back-contact diffusion | Am ⁻¹ | 1e-03 |
| JSGBR | Bottom saturation-current density due to generating an electron hole at $V=V_R$ | Am ⁻² | 1e-03 |
| JSGGR | Gate edge saturation-current density due to generating an electron hole at $V=V_R$ | Am ⁻¹ | 1e-03 |
| JSGSR | Sidewall saturation-current density due to generating an electron hole at $V=V_R$ | Am ⁻¹ | 1e-03 |
| NB | Emission coefficient of the bottom forward current | - | 1 |
| NG | Emission coefficient of the gate edge forward current | - | 1 |
| NS | Emission coefficient of the sidewall forward current | - | 1 |
| PB | Bottom junction grading coefficient | - | 0.4 |
| PG | Gate edge junction grading coefficient | - | 0.4 |
| PS | Sidewall junction grading coefficient | - | 0.4 |
| VDBR | Diffusion voltage of the bottom junction at $T=T_R$ | V | 1 |
| VDGR | Diffusion voltage of the gate-edge junction at $T=T_R$ | V | 1 |

| Name | Description | Units | Default |
|------|--|-------|---------|
| VDSR | Diffusion voltage of the sidewall junction at T=T _R | V | 1 |
| VR | Voltage at which simulation determines parameters | V | 0 |

Note: All symbols refer to “Unclassified Report NL-UR 2001/813”.

Philips MOS11 Model Examples

Following are some examples of the Philips MOS11 Model implementation:

Example 1

```
.model nch nmos level=63
+ VERSION=1100
+ LER=1E-06 WER=1E-05 LAP=-1.864E-08
+ TR=21 VFBR=-1.038 SLPHIB=-1.024E-08
+ SL2PHIB=1.428E-14 KOR=5.763E-01 SLKO=2.649E-08
+ SL2KO=-1.737E-14 KPINV=2.2E-01 PHIBR=0.85
+ BETSQ=1.201E-04 ETABET=1.3 FBET1=-3.741000E-01
+ LP1=2.806E-06 LP2=1E-10 THESATEXP=2
+ THESRR=7.109E-01 THEPHR=1E-03 TOX=3.2E-09
+ ETAPH=1.75E+00 ETAMOBR=2.825 NUR=1
+ NUEXP=3.228 THERR=1.267E-01 ETAR=0.4
+ THER2=1 THESATR=6.931E-02 SLTHESAT=1
+ ETASAT=8.753E-01 SSFR=2.304E-03 VP=5E-02
+ SLSSF=1.002E-06 ALPR=1.062E-02 SLALP=9.957E-01
+ ALPEXP=1.039 THETHR=2.413E-03 THETHEXP=1
+ SDIBLO=1.06E-06 SDIBLEXP=6.756 LLMIN=2E-07
+ MOR=1.05E-03 MOEXP=3.146
+ A1R=9.938E+04 STA1=9.3E-02 SLA1=-2.805E-03
+ A2R=4.047E+01 SLA2=1E-15
+ A3R=7.54E-01 SLA3=-8.705E-08
+ COL=3.2E-10
+ NTR=1.6237E-20 NFAR=1 NFBR=0
+ NFCR=0 GATENOISE=0
+ CJBR=1.347E-3 CJSR=0.183E-9 CJGR=0.374E-9
+ JSDBR=0.027E-6 JSDSR=0.040E-12 JSDGR=0.100E-12
+ VR=0.000
+ JSGBR=1.900E-6 JSGSR=78.000E-12 JSGGR=54.000E-12
+ VB=20.000
+ VDBR=0.828 VDSR=0.593 VDGR=0.500
+ PB=0.394 PS=0.171 PG=0.193
+ NB=1.000 NS=1.000 NG=1.000
```

Chapter 2: MOSFET Models

LEVEL 63: Philips MOS11 Model

Example 2

```
.model nch nmos level=63
+ VERSION=11010
+ LVAR=0.000000E+00
+ LAP=-1.864000E-08 WVAR=0.000000E+00 WOT=0.000000E+00
+ TR=2.100000E+01 VFB=-1.038000E+00 STVFB=0.000000E+00
+ SLPHIB=-1.024000E-08 SL2PHIB=1.428000E-14 SWPHIB=0.000000E+00
+ KOR=5.763000E-01 SLKO=2.649000E-08 SL2KO=-1.737000E-14
+ SWKO=0.000000E+00 KPINV=2.200000E-01 PHIBR=8.500000E-01
+ BETSQ=1.201000E-04 ETABETR=1.300000E+00 FBET1=-3.741000E-01
+ LP1=2.806000E-06 FBET2=0.000000E+00 LP2=1.000000E-10
+ THESRR=7.109000E-01 SWTHESR=0.000000E+00 THEPHR=1.000000E-03
+ ETAPH=1.750000E+00 SWTHEPH=0.000000E+00 ETAMOBR=2.825000E+00
+ STETAMOB=0.000000E+00 SWETAMOB=0.000000E+00 NU=1.000000E+00
+ NUEXP=3.228000E+00 THERR=1.267000E-01 ETAR=4.000000E-01
+ SWTHER=0.000000E+00 THER1=0.000000E+00 THER2=1.000000E+00
+ THESATR=6.931000E-02 SLTHESAT=1.000000E+00
THESATEXP=2.000000E+00
+ ETASAT=8.753000E-01 SWTHESAT=0.000000E+00 SSFR=2.304000E-03
+ SLSSF=1.002000E-06 SWSSF=0.000000E+00 ALPR=1.062000E-02
+ SLALP=9.957000E-01 ALPEXP=1.039000E+00 SWALP=0.000000E+00
+ VP=5.000000E-02 THETHR=2.413000E-03 THETHEXP=1.000000E+00
+ SWTHETH=0.000000E+00 SDIBLO=1.060000E-06 SDIBLEXP=6.756000E+00
+ MOR=1.050000E-03 MOEXP=3.146000E+00 LLMIN=2.000000E-07
+ A1R=9.938000E+04 STA1=9.300000E-02 SLA1=-2.805000E-03
+ SWA1=0.000000E+00 A2R=4.047000E+01 SLA2=1.000000E-15
+ SWA2=0.000000E+00 A3R=7.540000E-01 SLA3=-8.705000E-08
+ SWA3=0.000000E+00 TOX=3.200000E-09 COL=3.200000E-10
+ NT=1.623700E-20 NFAR=1.000000E-00 NFBR=0.000000E+00
+ NFCR=0.000000E+00 GATENOISE =0.00000E-00 DTA=0.000000E-00
```

Example 3

```
.model nch nmos level=63
+ LEVEL =63
+ VERSION=11011
+ LVAR=0 LAP=4.0E-08 WVAR=0.0 WOT=0.0 TR=21 VFB=-0.105E+01
+ POKO=0.5 PLKO=0.0 PWKO=0.0 PLWKO=0.0 KPINV=0.0
+ POPHIB=0.95 PLPHIB=0.0 PWPHIB=0.0 POBET=1.922E-03
+ POTHESR=3.562E-01 POTHEPH=1.29E-02 POETAMOB=1.4 POTHER=8.120E-02
+ THER1=0.0 THER2=0.1E+01 POTHESAT=0.2513 POTHETH =1.0E-5
+ POSDIBL=8.530E-4 POSSF=1.2E-2 POALP=2.5E-2 VP=5.0E-2
+ POMEXP=0.2 POA1=6.022 POA2=38.02 POA3=0.6407
+ POBINV=48 POBACC=48 KOV=2.5 TOX=3.2E-09
+ POCOX=2.980E-14 POCGDO=6.392E-15 POCGSO=6.392E-15
+ NT=1.656E-20 PONFA=8.323E+22 PONFB=2.514E+7
+ POTVFB=5.0E-4 POTPHIB=-8.5E-4
+ POTETABET=1.30 POTETASR=0.65 POTETAPH=1.350 NU=2.0
```

Chapter 2: MOSFET Models
LEVEL 63: Philips MOS11 Model

+ POTNUEXP=5.25 POTETAR=0.95 POTETASAT=1.040

LEVEL 64: STARC HiSIM MOSFET Model

HiSIM (Hiroshima-university STARC IGFET Model) is a publicly-available MOSFET model for circuit simulation. It uses drift-diffusion approximation, and a channel-surface-potential description. You can model all MOSFET characteristics closely, based on their physical origins by using fewer model parameters (about 90 model parameters); each parameter set is sufficient for all gate lengths. These model parameters are directly related to the MOSFET physics that a simulator can easily extract according to its physical meanings.

The STARC HiSIM model is Level 64 in the Synopsys MOSFET models. To use this model, specify:

```
M1 drain gate source bulk NCH w=4u l=1u  
.MODEL NCH NMOS LEVEL=64
```

Since the STARC HiSIM1.1.0 release, the Synopsys version of the HiSIM model has included a VERSION number parameter to facilitate backward compatibility. Starting in the 2003.03 release, Synopsys uses the STARC version control mechanism so you must enter an integer for the VERSION model parameter. For example, to specify HiSIM version 1.0.0, set the VERSION model parameter to 100. If you do not set the VERSION parameter, simulation issues a warning and automatically sets this parameter to 100.

You can set the VERSION value to:

- 100, 101, 102 (HiSIM1.0.* series)
- 110, 111, 112 (HiSIM1.1.* series)
- 120 (HiSIM1.2.*)

To turn off the model effects, use the following settings:

- Short-Channel Effect SC1=SC2=SC3=0
- Reverse-Short-Channel Effect LP=0
- Quantum-Mechanical Effect QME1=QME2=QME3=0
- Poly-Depletion Effect PGD1=PGD2=PGD3=0
- Channel-Length Modulation CLM1=CLM2=CLM3=0
- Narrow-Channel Effect WFC=MUEPH2=0

This section covers the following topics:

- [STARC HiSIM Model Parameters](#)
-

STARC HiSIM Model Parameters

This section covers the following topics:

- [STARC HiSIM Model — Model Selectors](#)
- [STARC HiSIM Model — Technological Parameters](#)
- [STARC HiSIM Model — Temperature Dependence Parameters](#)
- [STARC HiSIM Model — Quantum Effect Parameters](#)
- [STARC HiSIM Model — Poly Depletion Parameters](#)
- [STARC HiSIM Model — Short Channel Parameters](#)
- [STARC HiSIM Model — Narrow Channel Parameters](#)
- [STARC HiSIM Model — Mobility Parameters](#)
- [STARC HiSIM Model — Channel Length Modulation Parameters](#)
- [STARC HiSIM Model — Substrate Current Parameters](#)
- [STARC HiSIM Model — Current Parameters](#)
- [STARC HiSIM Model — GIDL Current Parameters](#)
- [STARC HiSIM Model — 1/f Noise Parameters](#)
- [STARC HiSIM Model — Conserving Symmetry at \$V_{ds}=0\$ for Short-Channel MOSFETS](#)
- [STARC HiSIM Model — MOS Diode](#)
- [STARC HiSIM Model — Subthreshold Swing](#)
- [STARC HiSIM Model — Parameter Version Defaults](#)

STARC HiSIM Model — Model Selectors

| Parameter | Default | Description |
|-----------|---------|----------------------|
| LEVEL | 64 | Model selector |
| VERSION | 100 | Model version number |

Chapter 2: MOSFET Models

LEVEL 64: STARC HiSIM MOSFET Model

| Parameter | Default | Description |
|-----------|---------|--|
| CORSRD | 0(no) | Flag. Indicates whether to include the Rs and Rd contact resistors, and whether to solve equations iteratively. CORSRD=1(yes) |
| COGIDL | 0 | Selects the gate induced drain leakage (GIDL) current model. <ul style="list-style-type: none">■ COGIDL=0 (yes)■ COGIDL=1 (no) VERSION < 111 does not support this model. |
| COIIGS | 0 | Selects the gate tunneling current model. <ul style="list-style-type: none">■ COIIGS=0 (yes),■ COIIGS=1 (no) VERSION < 111 does not support this model. |
| COISTI | 0 | Selects the shallow-trench-isolation (STI) leakage current. <ul style="list-style-type: none">■ COISTI=0 (no)■ COISTI=1 (yes), only if VERSION \geq 110. |
| COISUB | 0 | Substrate current model selector. <ul style="list-style-type: none">■ for VERSION < 110, COISUB=0 (yes),■ otherwise, COISUB=1 (no) |
| CONOIS | 0 | 1/f noise model selector. <ul style="list-style-type: none">■ CONOIS=0 (no)■ CONOIS=1 (yes) |
| COOVLP | 0 | Overlap capacitance model selector. <ul style="list-style-type: none">■ COOVLP=-1, constant value■ COOVLP=0, approximating the field linear reduction■ COOVLP=1, considering the lateral impurity profile. |

| Parameter | Default | Description |
|-----------|---------|---|
| NOISE | 5 | <p>Channel thermal and flicker noises combination selector.</p> <ul style="list-style-type: none"> ▪ NOISE=1 Channel thermal noise=SPICE2 model Flicker noise=SPICE2 model ▪ NOISE=2 Channel thermal noise=HiSIM1 model for the BSIM3 model Flicker noise=HiSIM1 model ▪ NOISE=3 Channel thermal noise=SPICE2 model Flicker noise=HiSIM1 model ▪ NOISE=4 Channel thermal noise=HiSIM1 model for the BSIM3 model Flicker noise=SPICE2 model ▪ NOISE=5 Channel thermal noise=NONE Flicker noise=HiSIM1 model |

STARC HiSIM Model — Technological Parameters

| Parameter | Default | Description |
|-----------|--------------|---|
| LP | 0.0m | Pocket penetration length |
| NSUBC | 5.94e+17cm-3 | Substrate-impurity concentration |
| NSUBP | 5.94e+17cm-3 | Maxim pocket concentration |
| RD | 0.0ohm*m | Drain-contact resistance |
| RS | 0.0ohm*m | Source-contact resistance |
| TOX | 3.6e-9m | Oxide thickness |
| TPOLY | 0.0m | Height of the gate poly-Si |
| VFBC | -0.722729V | Flat-band voltage |
| XJ | 0.0m | Junction depth (if VERSION < 110) |
| XLD | 0.0m | Gate-overlap length |
| XPOLYD | 0.0m | Difference between the gate-poly and the design lengths |
| XQY | 0.0m | Distance from the drain junction to the maximum electric field point (if VERSION ≥ 110) |
| XWD | 0.0m | Gate-overlap width |

Chapter 2: MOSFET Models

LEVEL 64: STARC HiSIM MOSFET Model

STARC HiSIM Model — Temperature Dependence Parameters

| Parameter | Default | Description |
|-----------|--------------------------|-------------------|
| BGTM1 | 9.03e-5eVK ⁻¹ | Bandgap narrowing |
| BGTM2 | 3.05e-7eVK-2 | Bandgap narrowing |

STARC HiSIM Model — Quantum Effect Parameters

| Parameter | Default | Description |
|-----------|---------|---|
| QME1 | 0.0mV | Coefficient for the quantum mechanical effect |
| QME2 | 0.0V | Coefficient for the quantum mechanical effect |
| QME3 | 0.0m | Coefficient for the quantum mechanical effect |

STARC HiSIM Model — Poly Depletion Parameters

| Parameter | Default | Description |
|-----------|---------|---|
| PGD1 | 0.0V | Strength of the poly depletion |
| PGD2 | 0.0V | Threshold voltage of the poly depletion |
| PGD3 | 0.0 | V_{ds} dependence of the poly depletion |

STARC HiSIM Model — Short Channel Parameters

| Parameter | Default | Description |
|-----------|----------------------|---|
| PARL1 | 1.0 | Strength of the lateral-electric-field gradient |
| PARL2 | 2.2e-8m | Depletion width of the channel/contact junction |
| SC1 | 13.5V ⁻¹ | Short-channel coefficient 1 |
| SC2 | 1.8V-2 | Short-channel coefficient 2 |
| SC3 | 0.0V ⁻² m | Short-channel coefficient 3 |
| SCP1 | 0.0V ⁻¹ | Short-channel coefficient 1 for the pocket |

| Parameter | Default | Description |
|-----------|----------------------|--|
| SCP2 | 0.0V-2 | Short-channel coefficient 2 for the pocket |
| SCP3 | 0.0V ⁻² m | Short-channel coefficient 3 for the pocket |

STARC HiSIM Model — Narrow Channel Parameters

| Parameter | Default | Description |
|-----------|------------------------|---|
| WFC | 0.0m*F/cm ² | Voltage reduction |
| MUEPH2 | 0.0 | Mobility reduction |
| NSTI | 0.0cm ⁻³ | Substrate-impurity concentration at the shallow-trench-isolation (STI) edge, if VERSION ≥ 110 |
| W0 | 0.0log(cm) | Minimum gate width |
| WSTI | 0.0m | Width of the high-field region at the shallow-trench-isolation (STI), if VERSION ≥ 110 |
| WVTHSC | 0.0 | Short-channel effect at the shallow-trench-isolation (STI) edge, if VERSION ≥ 110 |

STARC HiSIM Model — Mobility Parameters

| Parameter | Default | Description |
|-----------|--------------------------|---|
| BB | 2.0(NMOS) 1.0(PMOS) | High-field-mobility degradation |
| MUECB0 | 300.0cm ² /Vs | Coulomb scattering |
| MUECB1 | 30.0cm ² /Vs | Coulomb scattering |
| MUEPH0 | 0.295 | Phonon scattering |
| MUEPH1 | 1.0e7 | Phonon scattering |
| MUESR0 | 1.0 | Surface-roughness scattering |
| MUESR1 | 7.0e8 | Surface-roughness scattering |
| MUETMP | 0.0 | Temperature dependence of phonon scattering |
| NDEP | 1.0 | Coefficient of the effective-electric field |

Chapter 2: MOSFET Models

LEVEL 64: STARC HiSIM MOSFET Model

| Parameter | Default | Description |
|-----------|--|---|
| NINV | 0.5 | Coefficient of the effective-electric field |
| NINVD | 0.0V ⁻¹ | Modification of NINV |
| RPOCK1 | 0.0V ² *m ^{1/2} /A | Resistance coefficient caused by the potential barrier |
| RPOCK2 | 0.0V | Resistance coefficient caused by the potential barrier |
| RPOCP1 | 0.0 | Resistance coefficient caused by the potential barrier, if VERSION ≥ 110 |
| RPOCP2 | 0.0 | Resistance coefficient caused by the potential barrier, if VERSION ≥ 110 |
| VDS0 | 0.05V | Drain voltage for extracting low-field mobility |
| VMAX | 1.0e7cm/s | Maximum saturation velocity |
| VOVER | 0.0 | Velocity overshoot effect |
| VOVERP | 0.0 | L _{gate} dependence of the velocity overshoot |

STARC HiSIM Model — Channel Length Modulation Parameters

| Parameter | Default | Description |
|-----------|---------|--|
| CLM1 | 0.3 | Hardness coefficient of the channel/contact junction |
| CLM2 | 0.0 | Coefficient for the Q _B contribution |
| CLM3 | 0.0 | Coefficient for the Q _I contribution |

STARC HiSIM Model — Substrate Current Parameters

| Parameter | Default | Description |
|-----------|--------------------|---------------------------------|
| SUB1 | 0.0V ⁻¹ | Substrate current coefficient 1 |
| SUB2 | -70.0 | Substrate current coefficient 2 |
| SUB3 | 1.0 | Substrate current coefficient 3 |

STARC HiSIM Model — Current Parameters

| Parameter | Default | Description |
|-----------|---------------------------|----------------------------|
| GLEAK1 | 0.0A*V ^{-3/2} /C | Gate current coefficient 1 |
| GLEAK2 | 0.0 | Gate current coefficient 2 |
| GLEAK3 | 0.0 | Gate current coefficient 3 |

STARC HiSIM Model — GIDL Current Parameters

| Parameter | Default | Description |
|-----------|-----------------------------|----------------------------|
| GIDL1 | 0.0A*m*V ^{-3/2} /C | GIDL current coefficient 1 |
| GIDL2 | 0.0V ^{-1/2} /cm | GIDL current coefficient 2 |
| GIDL3 | 0.0 | GIDL current coefficient 3 |

STARC HiSIM Model — 1/f Noise Parameters

| Parameter | Default | Description |
|-----------|----------------------|--|
| AF | 1.0 | SPICE2 flicker noise exponent |
| CIT | 0.0F/cm ² | Capacitance caused by the interface trapped carriers |
| EF | 0.0 | SPICE2 flicker noise frequency exponent |
| KF | 0.0 | SPICE2 flicker noise coefficient |
| NFALP | 2.0e-15 | Contribution of the mobility fluctuation |
| NFTRP | 1.0e11 | Ratio of trap density to the attenuation coefficient |

STARC HiSIM Model — Conserving Symmetry at V_{ds}=0 for Short-Channel MOSFETS

| Parameter | Default | Description |
|-----------|---------|-----------------------------------|
| PZADD0 | 1.0e-3V | Symmetry conservation coefficient |
| VZADD0 | 1.0e-2V | Symmetry conservation coefficient |

Chapter 2: MOSFET Models

LEVEL 64: STARC HiSIM MOSFET Model

STARC HiSIM Model — MOS Diode

| Parameter | Default | Description |
|-----------|------------------------------|--|
| CJ | 8.397247e-04Fm ⁻² | Bottom junction capacitance per unit area at zero bias |
| CJSW | 5.0e-10Fm ⁻¹ | Source/drain sidewall junction capacitance per unit area at zero bias |
| CJSWG | 5.0e-10Fm ⁻¹ | Source/drain gate sidewall junction capacitance per unit area at zero bias |
| JSO | 1.0e-4Am ⁻² | Saturation current density |
| JSOSW | 0.0Am ⁻¹ | Sidewall saturation current density |
| MJ | 0.5 | Bottom junction capacitance grading coefficient |
| MJSW | 0.33 | Source/drain sidewall junction capacitance grading coefficient |
| MJSWG | 0.33 | Source/drain gate sidewall junction capacitance grading coefficient |
| NJ | 1.0 | Emission coefficient |
| NJSW | 1.0 | Sidewall emission coefficient |
| PB | 1.0V | Bottom junction build-in potential |
| PBSW | 1.0V | Source/drain sidewall junction build-in potential |
| PBSWG | 1.0V | Source/drain gate sidewall junction build-in potential |
| VDIFFJ | 0.5V | Diode threshold voltage between source/drain and substrate |
| XTI | 3.0 | Junction current temperature exponent coefficient |

STARC HiSIM Model — Subthreshold Swing

| Parameter | Default | Description |
|-----------|---------|---|
| PTHROU | 0.0 | Correction for steep subthreshold swing |

Note: Model parameter defaults in the above tables are valid only for versions 100 and 110. For other versions, please refer to the following table:

STARC HiSIM Model — Parameter Version Defaults

| Parameter | Version=100, 110 | Others |
|-----------|------------------|--|
| BGTM1 | 9.03e-5 | 90.25e-6 |
| BGTM2 | 3.05e-7 | 100.0e-9 |
| CJ | 8.397247e-04 | 5.0e-04 |
| CLM1 | 0.3 | 0.7 |
| CLM2 | 0.0 | 2.0 |
| CLM3 | 0.0 | 1.0 |
| GIDL1 | 0.0 | 5.0e-3 for HiSIM101, 5.0e-6 for others |
| GIDL2 | 0.0 | 1.0e+6 |
| GIDL3 | 0.0 | 0.3 |
| GLEAK1 | 0.0 | 0.01e+6 for HiSIM101, 10.0e+3 for others |
| GLEAK2 | 0.0 | 20.0e+6 |
| GLEAK3 | 0.0 | 0.3 |
| LP | 0.0 | 15.0e-9 |
| MUEPH0 | 0.295 | 0.300 |
| MUEPH1 | 1.00e+7 | 25.0e+3 |
| MUESR0 | 1.0 | 2.0 |
| MUESR1 | 7.00e+8 | 2.0e+15 |
| MUETMP | 0.0 | 1.5 |
| NFALP | 2.00e-15 | 1.0e-16 |
| NFTRP | 100.0e+9 | 10.0e+9 |

Chapter 2: MOSFET Models

LEVEL 64: STARC HiSIM MOSFET Model

| Parameter | Version=100, 110 | Others |
|-----------|------------------|-----------|
| NINVD | 0.0 | 1.0e-9 |
| NSUBC | 5.94e+17 | 1.0e+17 |
| NSUBP | 5.94e+17 | 1.0e+17 |
| PARL2 | 2.20e-8 | 1.0e+17 |
| PGD1 | 0.0 | 0.01 |
| PGD2 | 0.0 | 1.0 |
| PGD3 | 0.0 | 0.8 |
| PZADD0 | 1.0e-3 | 5.0e-3 |
| QME1 | 0.0 | 40.0e-12 |
| QME2 | 0.0 | 300.0e-12 |
| RD | 0.0 | 80.0e-6 |
| RPOCK1 | 0.0 | 0.01 |
| RPOCK2 | 0.0 | 0.1 |
| RPOCP1 | 0.0 | 1.0 |
| RS | 0.0 | 80.0e-6 |
| SC1 | 13.5 | 0.0 |
| SC2 | 1.8 | 0.0 |
| SUB1 | 0.0 | 10.0 |
| SUB2 | -70.0 | 20.0 |
| SUB3 | 1.0 | 0.8 |
| TOX | 3.60e-9 | 5.0e-9 |
| VFBC | -0.722729 | -1.0 |
| VMAX | 1.00e+7 | 7.00e+6 |
| VOVER | 0.0 | 0.01 |

| Parameter | Version=100, 110 | Others |
|-----------|------------------|--------|
| VOVERP | 0.0 | 0.1 |

LEVEL 65: SSIMSOI Model

Level 65 is a surface-potential, charge-based, and partially depleted SOI MOSFET model developed by Motorola semiconductor.

The following sections discuss these topics:

- [Using SSIMSOI Model with HSPICE](#)
 - [SSIMSOI Model — General Syntax](#)
 - [SSIMSOI Model Parameters](#)
-

Using SSIMSOI Model with HSPICE

To simulate using the SSIMSOI model:

1. Set LEVEL=65 to identify the model as the SSIMSOI model.
2. Set the correct simulator room temperature.

The default room temperature is 25°C in Synopsys circuit simulators, but is 27°C in most other simulators. When comparing to other simulators, use TEMP 27 or .OPTION TNOM=27 to set the simulation temperature to 27°C in the netlist.

3. Set DTEMP on the element line.

You can use DTEMP with this model to increase the temperature of individual elements, relative to the circuit temperature. If you do not specify DTEMP, simulation extracts TRISE from the model card. If you do specify DTEMP, it overrides TRISE in the model card.

SSIMSOI Model — General Syntax

Syntax:

```
Mxxx nd ng ns ne [np] mname [L=val] [W=val]  
+ [M=val] [AD=val] [AS=val] [PD=val] [PS=val]  
+ [BODYTYPE=val] [IGATE=val] [AB=val] [PB=val] [LXB=val]  
+ [WXB=val] [LPE=val] [DTEMP=val]
```

For more information on parameters, see the [SSIMSOI Model Parameters](#) section.

SSIMSOI Model Parameters

This section covers the following topics:

- [SSIMSOI Model — General Parameters](#)
- [SSIMSOI Model — Intrinsic Parameters \(Geometry Modifiers and Threshold Voltage\)](#)
- [SSIMSOI Model — Intrinsic Parameters \(Mobility and Saturation, Output Conductance\)](#)
- [SSIMSOI Model — Parasitic Parameters](#)

SSIMSOI Model — General Parameters

| Parameter | Description |
|-----------|--|
| Mxxx | SSIMSOI element name. Must begin with M, followed by up to 1023 alphanumeric characters. |
| nd | Drain terminal node name or number. |
| ng | Front gate node name or number. |
| ns | Source terminal node name or number. |
| ne | Back gate (or Substrate) node name or number. |
| np | External body contact node name or number. |
| mname | SSIMSOI model name reference. |
| L | SSIMSOI channel length in meters. Default is 5.0 um. |
| W | SSIMSOI channel width in meters. Default is 5.0 um. |
| M | Multiplier to simulate multiple SSIMSOIs in parallel. Default=1. |
| AD | Drain diffusion area. Default=0. |
| AS | Source diffusion area. Default=0. |
| PD | Drain diffusion perimeter. Default=0. |
| PS | Source diffusion perimeter. Default=0. |
| BODYTYPE | Flag to choose floating(0) or Tgate(2). Default=0. |
| IGATE | Flag to turn on/off(0/1) gate current calculations. Default=1. |

Chapter 2: MOSFET Models

LEVEL 65: SSIMSOI Model

| Parameter | Description |
|-----------|---|
| AB | Body diffusion area. Default=0. |
| PB | Body diffusion perimeter (Body Contacted). Default=0. |
| LXB | Extrinsic Gate Length (Body Contacted). Default=0. |
| WXB | Extrinsic Gate Width (Body Contacted). Default=0. |
| LPE | Flag to turn on/off lpe-related parasitics. |
| DTEMP | Increases the temperature. |

SSIMSOI Model — Intrinsic Parameters (Geometry Modifiers and Threshold Voltage)

| Name | Parameter | Units | Default |
|-------|---------------------------------------|--------|---------|
| ABIAS | Width modifier | micron | 0 |
| CS1LE | Exponent for I-dependence of n1 | | -1 |
| CS1LL | I-dependence parameter of n1 | | 0 |
| CS1WE | | | -1 |
| CS1WL | | | 0 |
| CS2LE | | | -1 |
| CS2LL | | | 0 |
| CS2WE | | | -1 |
| CS2WL | | | 0 |
| DBIAS | Diffusion resistor processing bias | micron | 0 |
| DIBLE | | | -2 |
| DIBLL | | | 0 |
| DLICV | Length modified for capacitance model | micron | 0 |
| DPHII | Norm. error in phi at extro. Vth0 | | 0 |

| Name | Parameter | Units | Default |
|---------|---|---------------------|---------|
| GP1 | Bulk charge coefficient | | 1.744 |
| GP2 | I-dependence parameter of n2 | | 0.8364 |
| LG2CT | Distance from contact to poly edge | micron | 1.0 |
| LLDD | Ldd spacer width | micron | 0 |
| N1 | Surface region doping density | 1/cm ³ | 5.0e16 |
| N2 | Bulk region doping density | 1/cm ³ | 2.0e16 |
| NFS | Fast surface state density | 1/V-cm ² | 0 |
| NG | Poly gate doping density | 1/cm ³ | |
| NGF | Gate oxide fixed charge density | 1/cm ² | 0 |
| ODIF | Outdiffusion of s/d under gate | micron | 0 |
| ODIFS | Outdiffusion of s under gate (asymmetric) | micron | oidf |
| PBIAS | Length modifier (use with odif) | micron | 0 |
| SHRINK | Exponent for I-dependence of n2 | | 0 |
| SHRINK2 | W-dependence parameter of n1 | | 0 |
| TBOX | Back oxide thickness. | Angstro m | 250 |
| TCV | Temperature coefficient of threshold voltage. | 1/K | 0 |
| TCVFB | Temperature coefficient of flatband voltage | 1/K | |
| TOX | Gate oxide thickness. | Angstro m | 250 |
| TSI | Silicon film thickness. | cm | 0.2e-4 |
| VFB | Reference (large) MOSFET flatband voltage | v | calc |
| VFBLE | Exponent for length dependence of vth0 | | -1 |
| VFBLL | Length dependence parameter of vth0 | | 0 |

Chapter 2: MOSFET Models

LEVEL 65: SSIMSOI Model

| Name | Parameter | Units | Default |
|-------|--|--------|---------------------------|
| VFBWE | Exponent for width dependence of vth0 | | -1 |
| VFBWL | Width dependence parameter of vth0 | | 0 |
| VTH0 | Linear region vth, reference (large) MOSFET, Vbs=0 | v | 0.8 (nmos) -0.8 (pmos) |
| WBRK | Depth of surface region | micron | 0.2 |

SSIMSOI Model — Intrinsic Parameters (Mobility and Saturation, Output Conductance)

| Name | Parameter | Units | Default |
|--------|--|--------------------------|--------------------------|
| UBREF | Mobility parameter | cm ² /V-s | 700 (nmos) 300 (pmos) |
| UBRED | Mobility field reduction factor | (cm/V) ^{egvexp} | 100 |
| EAVFAC | Effective field coefficient | | 0.5 |
| EAVFWL | Width dependence of eavfac | | 0.0 |
| EAVFWE | Exponent of width dependence of eavfac | | -2.0 |
| EAVEXP | Exponent of mobility field function | | 1.0 |
| UBVDS | Drain dependence of eff. field | | 0.5 |
| VSAT | Channel carrier saturation velocity | cm/sec | 1.0e-7 |
| ESAT0 | Vsat divisor, velocity field model | | 2 |
| ESAT1 | Divisor, carrier velocity at sat. | | 1 |
| LC00 | Mult. For channel length modulation | | 0.2 |
| LC01 | Length dependence of lc00 | 1/micron | 0 |
| LC1 | Bias dependence of channel length modulation | 1/V | 0 |
| WLMOD | Mult. for channel width modulation | | 0 |
| DV2 | Par. for lin/sat transition region | | 0.05 |

| Name | Parameter | Units | Default |
|------|-------------------------------|-------|---------|
| DV3 | Length dependence of dv2 | | 0 |
| EXB | Temperature exponent of ubref | | 1.5 |

SSIMSOI Model — Parasitic Parameters

| Name | Parameter | Units | Default |
|--------|---|----------|---------|
| AF | Flicker noise exponent | | 1.0 |
| AIMP0 | Impact ionization parameter | | 0 |
| AIMPL | Length dependence of aimp0 | micron | 0 |
| AIMPT | Temperature dependence of aimp0 | 1/K | 0 |
| AIMPW | Width dependence of aimp0 | micron | 0 |
| BIMP0 | Exponent for impact ionization | 1/V | 28.0 |
| BIMP2 | Width dependence of bimp0 | micron | 0 |
| BIMPL | Length dependence of bimp0 | micron | 0 |
| CCC | Contact-to-contact capacitance | F/micron | 0 |
| CCCR | Ccc error in RCE netlists | F/micron | 0 |
| CCP | Contact-to-poly capacitance | F/micron | 0 |
| CCPR | Ccp error in RCE netlist | F/micron | 0 |
| CCX | Contact-to-soisub capacitance | F/micron | 0 |
| CEXP | Flicker noise cox exponent | | 1.0 |
| CFR | Gate to S/D fringing capacitance | F/micron | 0 |
| CFRB | Gate to body overlap capacitance | F/micron | 0 |
| CFRBOX | Back-gate to S/D fringing capacitance | F/micron | 0 |
| CFRS | Gate to s-fringing capacitance (asymmetrical) | F/micron | cfr |
| CJCH | S/D zero-bias junction channel-side capacitance | F/m | 0.0 |

Chapter 2: MOSFET Models

LEVEL 65: SSIMSOI Model

| Name | Parameter | Units | Default |
|--------------|---|----------------|------------|
| CPX | Poly-to-soisub capacitance | F/micron | 0 |
| FEXP | Flicker noise frequency exponent | | 1.0 |
| FOC | Bias dependence of overlap capacitance | | 1.0 |
| FSAT1 | Bias dependence of impact ionization | 1/V | 0 |
| GIDLA | GIDL pre-exponential parameter | A/m | (off) |
| GIDLB | GIDL exponential parameter | m/V | 3.0e9 |
| GIDLC | GIDL bulk-dependence parameter | V ³ | 8.0 |
| GIDLE | GIDL bandgap | V | calculated |
| GIDLت | GIDL temperature-dependence parameter | | calculated |
| GISLA | GISL pre-exponential parameter | A/m | gidla |
| GISLB | GISL exponential parameter | m/V | gidlb |
| GISLC | GISL bulk-dependence parameter | V ³ | gidlc |
| GISLE | GISL bandgap | V | gidle |
| GISLT | GISL temperature-dependence parameter | | gidlt |
| GTUNDELTO_X | Intrinsic region delta tox (electrical vs physical) | angstrom | (off) |
| GTUNDTOXO_VL | S/D overlap region delta tox (electrical vs physical) | angstrom | (off) |
| GTUNECBA | ECB fitting parameter | | 0.6 |
| GTUNECBB | ECB barrier height | V | 3.1 |
| GTUNECBBO | ECB barrier height | V | 3.1 |
| GTUNECBM | ECB effective mass | | 0.4 |
| GTUNEVBA | EVB fitting parameter | | 0.4 |
| GTUNEVBB | EVB barrier height | V | 4.2 |
| GTUNEVBB0 | EVB barrier height | V | 3.1 |

| Name | Parameter | Units | Default |
|--------------|---|-------------------|------------|
| GTUNEVBEG | EVB energy bandgap | V | 1.12 |
| GTUNEVBM | EVB effective mass | | 0.32 |
| GTUNHVBA | HVB fitting parameter | | 1.0 |
| GTUNHVBB | HVB barrier height | V | 4.5 |
| GTUNHVBBO | HVB barrier height | V | 4.5 |
| GTUNHVBM | HWB effective mass | | 0.3 |
| GTUNSTOXO VL | S overlap region delta tox (asymmetric) | angstrom | gundtoxovl |
| GTUNWDEP | Accumulation 2-D fringing parameter | micron | 0 |
| JGO | S/D diode SCR generation coefficient | A/cm ² | 0 |
| JGOLE | Exponent for I-dependence for jgo | | 0 |
| JGOLL | I-dependence parameter for jgo | | 0 |
| JGOS | S diode SCR generation coefficient (asymmetrical) | A/cm ² | jgo |
| JGOSLE | Exponent for I-dependence for jgo | | jgole |
| JGOSLL | I-dependence parameter for jgo | | jgoll |
| JGOST | Temperature adjustment coefficient for jgo | | jgot |
| JGOSWE | Exponent for w-dependence for jgo | | jgowe |
| JGOSWL | W-dependence parameter for jgo | | jgowl |
| JGOT | Temperature adjustment coefficient for jgo | | 0 |
| JGOWE | Exponent for w-dependence for jgo | | 0 |
| JGOWL | Exponent for I-dependence for jgo | | 0 |
| JRO | S/D diode SCR recombination coef | A/cm ² | 1e6 |
| JROLE | Exponent for I-dependence for jro | | 0 |
| JROLL | I-dependence parameter for jro | | 0 |

Chapter 2: MOSFET Models

LEVEL 65: SSIMSOI Model

| Name | Parameter | Units | Default |
|---------|--|-------------------|------------|
| JROS | S diode SCT recombination coefficient (asymmetrical) | A/cm ² | jro |
| JROSLE | Exponent for I-dependence for jro | | jrole |
| JROSLL | I-dependence parameter for jro | | jroll |
| JROST | Temperature adjustment coefficient for jro | | jrot |
| JROSWE | Exponent for w-dependence for jro | | jrowe |
| JROSWL | W-dependence parameter for jro | | jrowl |
| JROT | Temperature adjustment coefficient for jro | | calculated |
| JROWE | Exponent for w-dependence for jro | | 0 |
| JROWL | W-dependence parameter for jro | | 0 |
| KF | Flicker noise coefficient | | 0.0 |
| M | S/D diode recombination slope factor | | 2.0 |
| MG | S/D diode generation slope factor | | 2.0 |
| MGS | S diode generation slope factor | | mg |
| MICH | S/D junction channel-side grading coefficient | | 0.5 |
| MS | S diode recombination slope factor (asymmetrical) | | m |
| NBIT | Effective doping parameter for I-bit | | 1.0 |
| NDIF | Effective doping parameter for Q-diffusion | | 1.0 |
| NLEV | Flicker noise equation level | | 0 |
| ODIFACT | S/D active diffusion | micron | 0 |
| ODIFBC | Body contact diffusion | micron | 0 |
| ONKINK | Voltage adjustment for onset of the kink | V | 0 |
| PBCH | S/D junction channel-side built-in pot. | V | 0.8 |
| RSHBODY | Sheet res. of intrinsic body | ohm/sq | 3000 |

| Name | Parameter | Units | Default |
|----------------|--|--------|------------|
| RSHBODYEX T | Sheet res. of extrinsic body | ohm/sq | 3000 |
| RSHMIN | Sheet res. of s/d-gate overlap | ohm/sq | 0 |
| RSHMINS | Sheet res. of s-gate overlap (asymmetrical) | ohm/sq | rshmin |
| RSHPLS | Sheet res. of heavily doped S/D | ohm/sq | 0 |
| SEFF | S/D diode QNR recombination velocity | cm/s | 1e5 |
| SEFFL | I-dependence parameter for seff | | 0 |
| SEFFLE | Exponent for I-dependence for seff | | 0 |
| SEFFS | S diode QNR recombination velocity (asymmetrical) | cm/s | seff |
| SEFFSLE | Exponent for dependence for seffs | | seffle |
| SEFFSLL | I-dependence parameter for seffs | | seffll |
| SEFFST | Temperature adjustment coefficient for seffs | | sefft |
| SEFFSWE | Exponent for w-dependence for seffs | | seffwe |
| SEFFSWL | W-dependence parameter for seffs | | seffwl |
| SEFFT | Temperature adjustment coefficient for seff | | 0 |
| SEFFWE | Exponent for w-dependence for seff | | 0 |
| SEFFWL | W-dependence parameter for seff | | 0 |
| TCBODY | Temperature coefficient for rshbody and rshbodyext | 1/K | 0 |
| TCMIN | Temperature coefficient for rshmin | 1/K | 0 |
| TCMINS | Temperature coefficient for rshims (asymmetrical) | 1/K | tcmin |
| TCPLS | Temperature coefficient for rshpls | 1/K | 0 |
| TCPPBCH | S/D temperature coefficient for pbch | V/K | calculated |
| VOC | Bias dependence of overlap capacitance | V | 0 |
| WFR | Additional contact width | micron | 0 |

LEVEL 66: HSPICE HVMOS Model

The HSPICE Level 66 model is Synopsys proprietary model for high-voltage CMOS integrated circuits design and simulation. It is accurate in modeling the high-voltage device physics and robust in SPICE simulation. It is designed for various high-voltage CMOS processes, technology nodes, and device structures, including both widely-employed LDMOS (Laterally Diffused MOS) and EDMOS (Extended Drain MOS) transistors that may have any field plate oxide layer which helps the drain engineering. In addition, applications can be whole power management ICs such as switch power supply controllers, flash memory, hot-swap chips, and chips used in the automotive and medical industries.

This HSPICE HVMOS model has been widely adopted for production by many semiconductor companies and major foundries.

The model has been developed based on BSIM4, with high accuracy in geometrical, bias, and temperature scaling. It explicitly and accurately considers the following physical effects: independent bias-dependent drain/source resistances, quasi-saturation, self-heating, Gm fall-off in the saturation region, symmetric and asymmetrical source and drain structures, and many other high-voltage operation-related unique device behaviors.

This section covers the following topics:

- [HSPICE HVMOS Model — General Syntax](#)
- [HSPICE HVMOS Model Parameters](#)

HSPICE HVMOS Model — General Syntax

Syntax:

```
Mxxx nd ng ns [nb] mname [L=val] [W=val] [M=val]
+ [AD=val] [AS=val] [PD=val] [PS=val]
+ [RGATEMOD=val] [RBODYMOD=val]
+ [ACNQSMOD=val] [GEOMOD=val] [RGEOMOD=val]
+ [TRNQSMOD=val] [SA=val] [SB=val] [SD=val] [SHMOD=val]
+ [NRS=val] [NRD=val] [RBPB=val] [RBPD=val]
+ [RBPS=val] [RBSB=val]
+ [MIN=val] [RDC=val] [RSC=val] [DELVTO=val]
+ [MULU0=val] [DELK1=val]
+ [DELTOX=val] [OFF] [IC=Vds, Vgs, Vbs]
+ [WNFLAG=val]
```

HSPICE HVMOS Model Parameters

The following list only presents the HSPICE proprietary model parameters, while the rest are the same as [LEVEL 54: BSIM4 MOSFET Model](#).

| Parameter | Description |
|-----------|--|
| ACNQSMOD | AC small-signal NQS model selector. |
| AD | Drain diffusion area. |
| AS | Source diffusion area. |
| DELK1 | Shift in body bias coefficient (K1). |
| DELNFCT | Shift in subthreshold swing factor (NFACTOR). |
| DELTOX | Shift in gate electrical and physical oxide thickness (TOXE and TOXP). That is, the difference between the electrical and physical gate oxide/insulator thicknesses. |
| DELVTO | Shift in the VTH0 zero-bias threshold voltage. |
| GEOMOD | Geometry-dependent parasitics model selector—specifies how the end S/D diffusions connect. |
| IC | Initial guess in the order |
| L | MOSFET channel length in meters. |
| MIN | Whether to minimize the number of drain or source diffusions for even-number fingered device. |
| MNAME | MOSFET model name reference. |
| MULU0 | Low-field mobility (U_0) multiplier. |
| NB | Bulk terminal node name. |
| ND | Drain terminal node name. |
| NF | Number of device fingers. |
| NG | Gate terminal node name. |
| NRD | Number of drain diffusion squares. |

Chapter 2: MOSFET Models
 LEVEL 66: HSPICE HVMOS Model

| Parameter | Description |
|-----------|--|
| NRS | Number of source diffusion squares. |
| NS | Source terminal node name. |
| OFF | Sets the initial condition to OFF in DC analysis. |
| PD | Perimeter of the drain junction: <ul style="list-style-type: none"> ▪ If PERMOD=0, it excludes the gate edge. ▪ Otherwise, it includes the gate edge. |
| PS | Perimeter of the source junction: <ul style="list-style-type: none"> ▪ If PERMOD=0, it excludes the gate edge. ▪ Otherwise, it includes the gate edge. |
| RBDB | Resistance connected between dbNode and bNode. |
| RBODYMOD | Substrate resistance network model selector. |
| RBPB | Resistance connected between bNodePrime and bNode. |
| RBPD | Resistance connected between bNodePrime and dbNode. |
| RBPS | Resistance connected between bNodePrime and sbNode. |
| RBSB | Resistance connected between sbNode and bNode. |
| RDC | Drain contact resistance for per-finger device. |
| RGATEMOD | Gate resistance model selector. |
| RGEOMOD | Source/drain diffusion resistance and contact model selector—specifies the end S/D contact type: point wide or merged) and how to compute the S/D parasitics resistance. |
| RSC | Source contact resistance for per-finger device. |
| TRNQSMOD | Transient NQS model selector. |
| SHMOD | Self-heating model selector. |
| W | MOSFET channel width in meters. |
| WNFLAG | Turn on to select bin model based on width per NF for multi-finger devices. |

LEVEL 68: STARC HiSIM2 MOSFET Model

HiSIM (Hiroshima University/STARC IGFET Model) is the first complete surface-potential-based MOSFET model for circuit simulation. The most important advantage of the surface-potential-based modeling is the unified description of device characteristics for all bias conditions. The physical reliability of the drift-diffusion approximation has been proved by 2-D device simulations with channel lengths below 0.1um.

Note: HiSIM2 source code, and all copyrights, trade secrets or other intellectual property rights and the source code in its entirety, is owned by Hiroshima University and STARC.

To obtain analytical solutions for describing device performances, the charge sheet approximation of the inversion layer with zero thickness has been introduced. Together with the gradual-channel approximation all device characteristics are then described analytically by the channel-surface potentials at the source side and at the drain side. These surface potentials are functions of applied voltages on the four MOSFET terminals; the gate voltage Vg, the drain voltage Vd, the bulk voltage Vb and the reference potential of the source Vs. This is the long-channel basis of the HiSIM model, and extensions of the model approximations are done for advanced technologies. All newly appearing phenomena such as short-channel and reverse-short-channel effects are included in the surface potential calculations causing modifications resulting from the features of these advanced technologies.

The section covers the following topics:

- [STARC HiSIM2 Model — General Syntax \(All Versions\)](#)
- [STARC HiSIM2 Model Parameters](#)
- [STARC HiSIM2 Model Instance Parameters](#)
- [STARC HiSIM2 Model Updates](#)

STARC HiSIM2 Model — General Syntax (All Versions)

The following lists and describes the HiSIM Level 68 general parameters.

```
Mxxx nd ng ns [nb] mname [L=val] [W=val] [M=val]
+ [AD=val] [AS=val] [PD=val] [PS=val]
+ [NRS=val] [NRD=val] [XGW=val] [XGL=val]
```

Chapter 2: MOSFET Models

LEVEL 68: STARC HiSIM2 MOSFET Model

```
+ [RDC=val] [RSC=val]
+ [NF=val] [NGCON=val] [RBPB=val] [RBPD=val]
+ [RBPS=val] [RBDB=val] [RBSB=val] [SA=val]
+ [SB=val] [SD=val] [TEMP=val] [DTEMP=val]
+ [NSUBCDFM=val]

.MODEL MNAME N(P)MOS LEVEL=68 VERSION=240.0
+ [CORSRD=val] [COVLP=val] [COISUB=val]
+ [COIIGS=val] [COGIDL=val] [COISTI=val]
+ [COADOV=val] [CONQS=val] [CORG=val] [CORBNET=val]
+ [COFLICK=val] [COTHRML=val] [COIGN=val] [COIPRV=val]
+ [COPPRV=val] [CODFM=val]
+ . . .
```

STARC HiSIM2 Model Parameters

This section lists the STARC HiSIM2 MOSFET Model parameters:

- STARC HiSIM2 Model — General Parameters
- STARC HiSIM2 Model — Basic Device Parameters
- STARC HiSIM2 Model — Velocity Parameters
- STARC HiSIM2 Model — Quantum-Mechanical Effect Parameters
- STARC HiSIM2 Model — Poly-Silicon Gate Depletion Effect Parameters
- STARC HiSIM2 Model — Short Channel Effect Parameters
- STARC HiSIM2 Model — Channel-Length Modulation Parameters
- STARC HiSIM2 Model — Narrow Channel Effect Parameters
- STARC HiSIM2 Model — Small Size Effect Parameters
- STARC HiSIM2 Model — Substrate Current Parameters
- STARC HiSIM2 Model — Impact- Ionization Induced Bulk Potential Change Parameters
- STARC HiSIM2 Model — Gate Leakage Current Parameters
- STARC HiSIM2 Model — GIDL Current Parameters
- STARC HiSIM2 Model — Conservation of Symmetry at $V_{ds}=0$ for Short-Channel MOSFETs
- STARC HiSIM2 Model — Smoothing Coefficient Between Linear and Saturation Region

- STARC HiSIM2 Model — Source / Bulk and Drain / Bulk Diode Parameters
- STARC HiSIM2 Model — 1/f Noise Parameters
- STARC HiSIM2 Model — DFM Support Parameters
- STARC HiSIM2 Model — Non-Quasi-Static (NQS) Parameters
- STARC HiSIM2 Model — Capacitance Parameters
- STARC HiSIM2 Model — Parasitic Resistance Parameters
- STARC HiSIM2 Model — Binning Model Parameters

STARC HiSIM2 Model — General Parameters

| Description | Flag |
|--|---|
| Contact resistances R_s and R_d | CORSRD=0: No (default) CORSRD=1 & RS/RD ≠ 0: Yes, as internal resistances of HiSIM CORSRD=2 & RD ≠ 0: Yes, simple analytical formulation CORSRD=-1 & RS/RD ≠ 0: Yes, as external resistances of HiSIM |
| Overlap capacitance model | COOVLP=0: Constant overlap capacitance, either given LOVER plus CGSO/CGDO or LOVER only COOVLP=1: Bias dependent overlap capacitance (default: yes). Selecting a model either by defining NOVER value or not |
| Overlap capacitance for COOVLP=1 and NOVER ≠ 0 | COQOVSM=0: Analytically solved without inversion condition COQOVSM=1: Iteratively solved (default) COQOVSM=2: Analytically solved with inversion condition |
| Substrate current I_{sub} | COISUB=0: No (default) COISUB=1: Yes |
| Gate current I_{gate} | COIIGS=0: No (default) COIIGS=1: Yes |
| GIDL current I_{GIDL} | COGIDL=0: No (default) COGIDL=1: Yes |
| STI leakage current $I_{ds,STI}$ | COISTI=0: No (default) COISTI=1: Yes |

Chapter 2: MOSFET Models

LEVEL 68: STARC HiSIM2 MOSFET Model

| Description | Flag |
|--|--|
| Lateral field induced and overlap charges/capacitances are added to intrinsic ones | COADOV=0: No COADOV=1: Yes (default) |
| Non-quasi-static mode | CONQS=0: No (default) CONQS=1: Yes |
| Gate-contact resistance is included (This flag can also be given as an instance parameter) | CORG=0: No (default) CORG=1: Yes |
| Substrate resistance network is invoked (This flag can also be given as an instance parameter) | CORBNET=0: No (default) CORBNET=1: Yes |
| 1/f noise is calculated | COFLICK=0: No (default) COFLICK=1: Yes |
| Thermal noise is calculated | COTHRML=0: No (default) COTHRML=1: Yes |
| Induced gate and cross correlation noise are calculated | COIGN=0 COTHRML=0: No (default) COIGN=1 & COTHRML=1: Yes |
| Previous I_{ds} is used as an initial value for calculating source/drain resistance effect (R_s and/or $R_d \neq 0$) | COIPRV=0: No COIPRV=1: Yes (default) |
| Previous ϕ_S is used as an initial value for the iteration | COPPRV=0: No COPPRV=1: Yes (default) |
| Parameter variations for the DFM support are considered | CODFM=0: No (default) CODFM=1: Yes |
| Accurate calculation of the capacitance reciprocity is performed | CORECIP=0: No CORECIP=1: Yes (default) |
| Lateral-Field-Induced Charge is considered. | COQY=0: No (default) COQY=1: Yes |

STARC HiSIM2 Model — Basic Device Parameters

| Parameter | Description |
|-----------|--------------------------|
| TOX | Physical oxide thickness |

* indicates minor parameters, and ** indicates minor parameters for special cases.

| Parameter | Description |
|-----------|---|
| XL | Difference between real and drawn gate length |
| XW | Difference between real and drawn gate width |
| XLD | Gate-overlap length |
| XWD | Gate-overlap width |
| TPOLY | Height of the gate poly-Si for fringing capacitance |
| LL | Coefficient of gate length modification |
| LLD | Coefficient of gate length modification |
| LLN | Coefficient of gate length modification |
| WL | Coefficient of gate width modification |
| WLD | Coefficient of gate width modification |
| WLN | Coefficient of gate width modification |
| NSUBC | Substrate-impurity concentration |
| NSUBP | Maximum pocket concentration |
| LP | Pocket penetration length |
| *NPEXT | Maximum concentration of pocket tail |
| *LPEXT | Extension length of pocket tail |
| VFBC | Flat-band voltage |
| VFBCL | Channel length dependence of flat-band voltage |
| VFBCLP | Channel length dependence of flat-band voltage |
| VBI | Built-in potential |
| KAPPA | Dielectric constant for gate dielectric |
| EG0 | Bandgap |
| BGTMPI | Temperature dependence of bandgap |

* indicates minor parameters, and ** indicates minor parameters for special cases.

Chapter 2: MOSFET Models

LEVEL 68: STARC HiSIM2 MOSFET Model

| Parameter | Description |
|-----------|---|
| BGTM2 | Temperature dependence of bandgap |
| TNOM | Temperature selected as a nominal temperature value |

* indicates minor parameters, and ** indicates minor parameters for special cases.

STARC HiSIM2 Model — Velocity Parameters

| Parameter | Description |
|-----------|---|
| VMAX | Saturation velocity |
| VOVER | Velocity overshoot effect |
| VOVERP | L_{eff} dependence of velocity overshoot |
| *VTMP | Temperature dependence of the saturation velocity |

* indicates minor parameters, and ** indicates minor parameters for special cases.

STARC HiSIM2 Model — Quantum-Mechanical Effect Parameters

| Parameter | Description |
|-----------|--|
| QME1 | V_{gs} dependence of quantum mechanical effect |
| QME2 | V_{gs} dependence of quantum mechanical effect |
| QME3 | Minimum T_{ox} modification |

STARC HiSIM2 Model — Poly-Silicon Gate Depletion Effect Parameters

| Parameter | Description |
|-----------|--|
| PGD1 | Strength of poly-depletion effect |
| PGD2 | Threshold voltage of poly-depletion effect |
| *PGD4 | L_{gate} dependence of poly-depletion effect |

* indicates minor parameters, and ** indicates minor parameters for special cases.

STARC HiSIM2 Model — Short Channel Effect Parameters

| Parameter | Description |
|------------------|---|
| PARL2 | Depletion width of channel/contact junction |
| SC1 | Magnitude of short-channel effect |
| SC2 | V_{ds} dependence of short-channel effect |
| *SC3 | V_{bs} dependence of short-channel effect |
| *SC3VBS | For diminishing of impurity gradient |
| **SC4 | Coupling of V_{ds} and V_{bs} dependence |
| SCP1 | Magnitude of short-channel effect due to pocket |
| SCP2 | V_{ds} dependence of short-channel due to pocket |
| *SCP3 | V_{bs} dependence of short-channel effect due to pocket |
| *SCP21 | Short-channel-effect modification for small V_{ds} |
| *SCP22 | Short-channel-effect modification for small V_{ds} |
| *BS1 | Body-coefficient modification by impurity profile |
| *BS2 | Body-coefficient modification by impurity profile |
| *PTL | Strength of punch-through effect |
| *PTLP | Channel-length dependence of punch-through effect |
| *PTP | Strength of punch-through effect |
| *PT2 | V_{ds} dependence of punch-through effect |
| *PT4 | V_{bs} dependence of punch-through effect |
| *PT4P | V_{bs} dependence of punch-through effect |
| *GDL | Strength of high-field effect |
| *GDLP | Channel-length dependence of high-field effect |

*** indicates minor parameters, and ** indicates minor parameters for special cases.**

Chapter 2: MOSFET Models

LEVEL 68: STARC HiSIM2 MOSFET Model

| Parameter | Description |
|-----------|---|
| *GDLD | Channel-length dependence of high-field effect |
| *NSUBPL | Starting channel length of NSUBP reduction |
| *NSUBPFAC | Minimum factor of reduction |
| *NSUBPDLT | Delta for smoothness of the NSUBPFAC model |

* indicates minor parameters, and ** indicates minor parameters for special cases.

STARC HiSIM2 Model — Mobility Model Parameters

| Parameter | Description |
|-----------|---|
| MUECB0 | Coulomb scattering |
| MUECB0LP | Length dependence of Coulomb scattering |
| MUECB1 | Coulomb scattering |
| MUECB1LP | Length dependence of Coulomb scattering |
| MUEPH0 | Phonon scattering |
| MUEPH1 | Phonon scattering |
| MUETMP | Temperature dependence of phonon scattering |
| *MUEPHL | Length dependence of phonon mobility reduction |
| *MUEPLP | Length dependence of phonon mobility reduction |
| *MUEPLD | Length dependence of phonon mobility reduction |
| **MUEPHL2 | Length dependence of phonon mobility reduction |
| **MUEPLP2 | Length dependence of phonon mobility reduction |
| MUESR0 | Surface-roughness scattering |
| MUESR1 | Surface-roughness scattering |
| *MUESRL | Length dependence of surface roughness mobility reduction |

* indicates minor parameters, and ** indicates minor parameters for special cases.

| Parameter | Description |
|------------------|---|
| *MUESLP | Length dependence of surface roughness mobility reduction |
| *MUEPHS | Mobility modification due to small size |
| *MUEPSP | Mobility modification due to small size |
| NDEP | Depletion charge contribution on effective-electric field |
| *NDEPL | Modification of Q_B contribution for short-channel case |
| *NDEPLP | Modification of Q_B contribution for short-channel case |
| NINV | Inversion charge contribution on effective-electric field |
| *NINVD | Reduced resistance effect for small V_{ds} |
| BB | High-field-mobility degradation |

* indicates minor parameters, and ** indicates minor parameters for special cases.

STARC HiSIM2 Model — Channel-Length Modulation Parameters

| Parameter | Description |
|------------------|--|
| CLM1 | Hardness coefficient of channel/contact junction |
| CLM2 | Coefficient for Q_B contribution |
| CLM3 | Coefficient for Q_I contribution |
| *CLM4 | No more used |
| *CLM5 | Effect of pocket implantation |
| *CLM6 | Effect of pocket implantation |

* indicates minor parameters, and ** indicates minor parameters for special cases.

Chapter 2: MOSFET Models

LEVEL 68: STARC HiSIM2 MOSFET Model

STARC HiSIM2 Model — Narrow Channel Effect Parameters

| Parameter | Description |
|------------|--|
| WFC | Threshold voltage change due to capacitance change |
| *WVTH0 | Threshold voltage shift |
| **NSUBCW | Modification of substrate concentration for narrow width |
| **NSUBCWP | Modification of substrate concentration for narrow width |
| **NSUBCW2 | Modification of substrate concentration for narrow width |
| **NSUBCWP2 | Modification of substrate concentration for narrow width |
| **NSUBCMAX | Upper limit of substrate concentration for narrow width |
| *NSUBPW | Modification of pocket concentration for narrow width |
| *NSUBPWP | Modification of pocket concentration for narrow width |
| *NPEXTW | Modification of expansion concentration for narrow width |
| *NPEXTWP | Modification of expansion concentration for narrow width |
| *MUEPHW | Width dependence of phonon mobility reduction |
| *MUEPWP | Width dependence of phonon mobility reduction |
| *MUEPWD | Width dependence of phonon mobility reduction |
| **MUEPHW2 | Phonon related mobility reduction |
| **MUEPWP2 | Phonon related mobility reduction |
| *MUESRW | Change of surface roughness related mobility |
| *MUESWP | Change of surface roughness related mobility |
| *NDEPW | Modification of universal mobility for narrow width |
| *NDEPWP | Modification of universal mobility for narrow width |
| *VTHSTI | Threshold voltage shift due to STI |
| *VDSTI | V_{ds} dependence of STI subthreshold |

* indicates minor parameters, and ** indicates minor parameters for special cases.

| Parameter | Description |
|------------------|--|
| *SCSTI1 | The same effect as SC1 but at STI edge |
| *SCSTI2 | The same effect as SC2 but at STI edge |
| NSTI | Substrate-impurity concentration at the STI edge |
| **NSTIL | Length dependence of STI impurity concentration |
| **NSTILP | Length dependence of STI impurity concentration |
| WSTI | Width of the high-field region at STI edge |
| *WSTIL | Channel-length dependence of WSTI |
| *WSTILP | Channel-length dependence of WSTI |
| *WSTIW | Channel-width dependence of WSTI |
| *WSTIWP | Channel-width dependence of WSTI |
| WL1 | Threshold voltage shift of STI leakage due to small size effect |
| WL1P | Threshold voltage shift of STI leakage due to small size effect |
| NSUCPSTI1 | Channel concentration change due to diffusion-region length between gate and STI |
| NSUBCSTI2 | Channel concentration change due to diffusion-region length between gate and STI |
| NSUBCSTI3 | Channel concentration change due to diffusion-region length between gate and STI |
| NSUBPSTI1 | Pocket concentration change due to diffusion-region length between gate and STI |
| NSUBPSTI2 | Pocket concentration change due to diffusion-region length between gate and STI |
| NSUBPSTI3 | Pocket concentration change due to diffusion-region length between gate and STI |
| MUESTI1 | Mobility change due to diffusion-region length between gate and STI |
| MUESTI2 | Mobility change due to diffusion-region length between gate and STI |
| MUESTI3 | Mobility change due to diffusion-region length between gate and STI |
| SAREF | Reference length of diffusion between gate and STI |
| SBREF | Reference length of diffusion between gate and STI |

*** indicates minor parameters, and ** indicates minor parameters for special cases.**

Chapter 2: MOSFET Models

LEVEL 68: STARC HiSIM2 MOSFET Model

STARC HiSIM2 Model — Small Size Effect Parameters

| Parameter | Description |
|-----------|--|
| WL2 | Threshold voltage shift due to small size effect |
| WL2P | Threshold voltage shift due to small size effect |
| *MUEPHS | Mobility modification due to small size |
| *MUEPSP | Mobility modification due to small size |
| *VOVERS | Modification of maximum velocity due to small size |
| *VOVERSP | Modification of maximum velocity due to small size |

* indicates minor parameters, and ** indicates minor parameters for special cases.

STARC HiSIM2 Model — Substrate Current Parameters

| Parameter | Description |
|-----------|---|
| SUB1 | Substrate current coefficient of magnitude |
| SUB1L | L_{gate} dependence SUB1 |
| SUB1LP | L_{gate} dependence SUB1 |
| SUB2 | Substrate current coefficient of exponential term |
| SUB2L | L_{gate} dependence of SUB2 |
| SVDS | Substrate current dependence on V_{ds} |
| SLG | Substrate current dependence on L_{gate} |
| SLGL | Substrate current dependence on L_{gate} |
| SLGLP | Substrate current dependence on L_{gate} |
| SVBS | Substrate current dependence on V_{bs} |
| SVBSL | L_{gate} dependence of SVBS |

* indicates minor parameters, and ** indicates minor parameters for special cases.

| Parameter | Description |
|-----------|--|
| SVBSLP | L_{gate} dependence of SVBS |
| SVGS | Substrate current dependence on V_{gs} |
| SVGSL | L_{gate} dependence of SVGS |
| SVGSLP | L_{gate} dependence of SVGS |
| SVGSW | W_{gate} dependence of SVGS |
| SVGSPW | W_{gate} dependence of SVGS |

* indicates minor parameters, and ** indicates minor parameters for special cases.

STARC HiSIM2 Model — Impact-Ionization Induced Bulk Potential Change Parameters

| Parameter | Description |
|-----------|---|
| IBPC1 | Impact-ionization induced bulk potential change |
| IBPC2 | Impact-ionization induced bulk potential change |

STARC HiSIM2 Model — Gate Leakage Current Parameters

| Parameter | Description |
|-----------|---|
| GLEAK1 | Gate to channel current coefficient |
| GLEAK2 | Gate to channel current coefficient |
| GLEAK3 | Gate to channel current coefficient |
| GLEAK4 | Gate to channel current coefficient |
| *GLEAK5 | Gate to channel current coefficient (short channel correction) |
| *GLEAK6 | Gate to channel current coefficient (V_{ds} dependence correction) |
| *GLEAK7 | Gate to channel current coefficient (gate length and width dependence correction) |
| EGIG | Temperature dependence of gate leakage |

* indicates minor parameters, and ** indicates minor parameters for special cases.

Chapter 2: MOSFET Models

LEVEL 68: STARC HiSIM2 MOSFET Model

| Parameter | Description |
|-----------|--|
| IGTEMP2 | Temperature dependence of gate leakage |
| IGTEMP3 | Temperature dependence of gate leakage |
| GLKSD1 | Gate to source/drain current coefficient |
| GLKSD2 | Gate to source/drain current coefficient |
| GLKSD3 | Gate to source/drain current coefficient |
| GLKB1 | Gate to bulk current coefficient |
| GLKB2 | Gate to bulk current coefficient |
| GLKB3 | Flat-bans shift for gate to bulk current |

* indicates minor parameters, and ** indicates minor parameters for special cases.

STARC HiSIM2 Model — GIDL Current Parameters

| Parameter | Description |
|-----------|---------------------------------------|
| GIDL1 | Magnitude of GIDL |
| GIDL2 | Field dependence of GIDL |
| GIDL3 | V_{ds} dependence of GIDL |
| *GIDL4 | Threshold of V_{ds} dependence |
| *GIDL5 | Correction of high-field contribution |
| *GIDL6 | V_{bs} dependence of GIDL |
| *GIDL7 | Correction of high-field contribution |

* indicates minor parameters, and ** indicates minor parameters for special cases.

STARC HiSIM2 Model — Conservation of Symmetry at $V_{ds}=0$ for Short-Channel MOSFETs

| Parameter | Description |
|-----------|-----------------------------------|
| VZADD0 | Symmetry conservation coefficient |

| Parameter | Description |
|-----------|-----------------------------------|
| PZADD0 | Symmetry conservation coefficient |

STARC HiSIM2 Model — Smoothing Coefficient Between Linear and Saturation Region

| Parameter | Description |
|-----------|--|
| *DDLTMAX | Smoothing coefficient for Vds |
| *DDLTSLP | L_{gate} dependence of smoothing coefficient |
| *DDLTICT | L_{gate} dependence of smoothing coefficient |

* indicates minor parameters, and ** indicates minor parameters for special cases.

STARC HiSIM2 Model — Source / Bulk and Drain / Bulk Diode Parameters

| Parameter | Description |
|-----------|--|
| JS0 | Saturation current density |
| JS0SW | Sidewall saturation current density |
| NJ | Emission coefficient |
| NJSW | Sidewall emission coefficient |
| XTI | Temperature coefficient for forward current densities |
| XTI2 | Temperature coefficient for reverse current densities |
| DIVX | Reverse current coefficient |
| CTEMP | Temperature coefficient of reverse currents |
| CISB | Reverse biased saturation current |
| CISBK | Reverse biased saturation current (at low temperature) |
| CVB | Bias dependence coefficient of CISB |
| CVBK | Bias dependence coefficient of CISB (at low temperature) |
| CJ | Bottom junction capacitance per unit area at zero bias |

Chapter 2: MOSFET Models

LEVEL 68: STARC HiSIM2 MOSFET Model

| Parameter | Description |
|-------------------|--|
| CJSW | Source/drain sidewall junction cap. grading coefficient per unit length at zero bias |
| CJSWG | Source/drain sidewall junction capacitance per unit length at zero bias |
| MJ | Bottom junction capacitance grading coefficient |
| MJSW | Source/drain sidewall junction capacitance grading coefficient |
| MJSWG | Source/drain gate sidewall junction capacitance grading coefficient |
| PB | Bottom junction build-in potential |
| PBSW | Source/drain sidewall junction build-in potential |
| PBSWG | Source/drain gate sidewall junction build-in potential |
| VDIFFJ | Diode threshold voltage between source/drain and substrate |
| TCJB _D | Temperature dependence of drain-side diode capacitance |
| TCJBDSW | Temperature dependence of drain-side diode capacitance |
| TCJBDSWG | Temperature dependence of drain-side diode capacitance |
| TCJB _S | Temperature dependence of source-side diode capacitance |
| TCJBSSW | Temperature dependence of source-side diode capacitance |
| TCJBSSWG | Temperature dependence of source-side diode capacitance |

STARC HiSIM2 Model — 1/f Noise Parameters

| Parameter | Description |
|-----------|--|
| NFALP | Contribution of the mobility fluctuation |
| NFTRP | Ratio of trap density to attenuation coefficient |
| *CIT | Capacitance caused by the interface trapped carriers |
| FALPH | Power of f describing deviation of 1/f |

* indicates minor parameters, and ** indicates minor parameters for special cases.

STARC HiSIM2 Model — DFM Support Parameters

| Parameter | Description |
|-----------|---|
| MPHDFM | Mobility dependence on NSUBC due to μ_{phonon} |

STARC HiSIM2 Model — Non-Quasi-Static (NQS) Parameters

| Parameter | Description |
|-----------|---|
| DLY1 | Coefficient for delay due to diffusion of carriers |
| DLY2 | Coefficient for delay due to conduction of carriers |
| DLY3 | Coefficient for RC delay of bulk carriers |

STARC HiSIM2 Model — Capacitance Parameters

| Parameter | Description |
|-----------|--|
| XQY | Distance from drain junction to maximum electric field point |
| *XQY1 | V_{bs} dependence of Q_y |
| *XQY2 | L_{gate} dependence of Q_y |
| QYRAT | Partitioning ratio of Q_y between source and drain |
| LOVER | Overlap length |
| NOVER | Impurity concentration in overlap region |
| VFBOVER | Flat-band voltage in overlap region |
| OVSLP | Coefficient for overlap capacitance |
| OVMAG | Coefficient for overlap capacitance |
| CGSO | Gate-to-source overlap capacitance |
| CGDO | Gate-to-drain overlap capacitance |
| CGBO | Gate-to-bulk overlap capacitance |

* indicates minor parameters, and ** indicates minor parameters for special cases.

Chapter 2: MOSFET Models

LEVEL 68: STARC HiSIM2 MOSFET Model

STARC HiSIM2 Model — Parasitic Resistance Parameters

| Parameter | Description |
|-----------|---|
| RS | Source-contact resistance in LDD region |
| RD | Drain-contact resistance in LDD region |
| RSH | Source/drain sheet resistance |
| RSHG | Gate sheet resistance |
| GBMIN | Substrate resistance network |
| RBPB | Substrate resistance network |
| RBPD | Substrate resistance network |
| RBPS | Substrate resistance network |
| RBDB | Substrate resistance network |
| RBSB | Substrate resistance network |

STARC HiSIM2 Model — Binning Model Parameters

| Parameter | Description |
|-----------|-------------------------------------|
| LBINN | Power of L_{drawn} dependence |
| WBINN | Power of W_{drawn} dependence |
| LMAX | Maximum length of L_{drawn} valid |
| LMIN | Minimum length of L_{drawn} valid |
| WMAX | Maximum length of W_{drawn} valid |
| WMIN | Minimum length of W_{drawn} valid |

The complete binning criteria is as follows:

$$\begin{aligned}L_{MIN} + XLREF &\leq L + XL < LMAX + XLREF \\ W_{MIN} + XWREF &\leq W + XW < WMAX + XWREF\end{aligned}$$

If you do not specify $XLREF$, the simulation sets it to XL .

If you do not specify $XWREF$, the simulation sets it to XW .

STARC HiSIM2 Model Instance Parameters

| Parameter | Description |
|--------------------------------|--|
| L | Gate length (L_{gate}) |
| W | Gate width (W_{gate}) |
| Diode | |
| AD | Junction area of the drain contact |
| AS | Junction area of the source contact |
| PD | Junction periphery of the drain contact |
| PS | Junction periphery of the source contact |
| Source/Drain Resistance | |
| NRD | Number of drain squares |
| NRS | Number of source squares |
| RDC | Additional drain resistance due to contact |
| RSC | Additional source resistance due to contact |
| Gate Resistance | |
| NF | Number of gate fingers |
| NGCON | Number of gate contacts |
| XGL | Offset of the gate length |
| XGW | Distance from the gate contact to the channel edge |
| Substrate Network | |
| RBDB | Substrate resistance network |
| RPB | Substrate resistance network |
| RBPD | Substrate resistance network |
| RBPS | Substrate resistance network |

Chapter 2: MOSFET Models

LEVEL 68: STARC HiSIM2 MOSFET Model

| Parameter | Description |
|-------------------------------|---|
| RBSB | Substrate resistance network |
| Length of Diffusion | |
| SA | Length of diffusion between gate and STI |
| SB | Length of diffusion between gate and STI |
| SD | Length of diffusion between gate and gate |
| Temperature | |
| TEMP | Device temperature (T) |
| DTEMP | Device temperature change |
| Design for Manufacture | |
| NSUBCDFM | Substrate impurity concentration |

STARC HiSIM2 Model Updates

This section provides the HiSIM2 model version updates:

- [HiSIM 2.7.0 Updates](#)
- [HiSIM 2.6.1 Updates](#)
- [HiSIM 2.6.0 Updates](#)
- [HiSIM 2.5.1 Updates](#)
- [HiSIM 2.5.0 Updates](#)
- [HiSIM 2.4.3 Updates](#)
- [HiSIM 2.4.2 Updates](#)
- [HiSIM 2.4.1 Updates](#)
- [HiSIM 240SC2 Updates](#)

HiSIM 2.7.0 Updates

The following is a summary of bug fixes and enhancements from version 2.6.1 to 2.7.0 per the HiSIM-STARC release notes.

1. Unit Conversion from CGS to MKS
 - In this release, the source code for model evaluation was converted from CKS units to MKS units.
2. Model description changes (Refer to *HiSim-STARC User's Manual for detailed information*).
 - Suppression of error messages from the range check when new model flag COERRREP is set to 0.
 - Improvement of GIDL current model with new model parameters GIDL6 and GIDL7.
 - Improvement of STI effect model with new model parameters NSUBCSTI1, NSUBCSTI2, and NSUBCSTI3.
 - Introduction of gate length dependence for VFBC with new model parameters VFBCL and VFBCLP.
 - Improvement of smoothness of the NSUBPFAC model with new model parameters NSUBPDLT.
 - Invalidation of the NSUBPFAC model when NSUBPFAC=1.
 - Range check of model parameters NSUBPFAC and NSUBPDLT:

| Parameter | Min | Max | Default | Remarks |
|-----------|-------|-----|---------|------------------|
| NSUBPFAC | 0.2 | 1.0 | 1.0 | Rest with range. |
| NSUBPDLT | 1E-50 | 0.1 | 0.01 | Rest with range. |

3. Bug fixes:
 - Calculation of MUEPH1 when CODFM=1.
 - Reset of SC4 value when CORECIP=1.
 - Calculation of some derivatives.
 - Floating point exception in the smoothing functions.
 - High-field effect model with model parameter GDLD.
 - Code improvements of Fn_POW and Fn_SZ functions for higher exception robustness.

Chapter 2: MOSFET Models

LEVEL 68: STARC HiSIM2 MOSFET Model

For details, refer to the official Hiroshima University HiSIM2 release website:
<http://home.hiroshima-u.ac.jp/usdl/HiSIM2/C-Code/protect.cgi>

HiSIM 2.6.1 Updates

The following is a summary of bug fixes and enhancements from version 2.6.0 to 2.6.1 per the HiSIM-STARC release notes.

The following bugs were fixed in this release:

- Missing initialization of NSUBC, NSUBP and MUEPH1 in the `hsm2temp.c` for repeating simulation.
- Unit converting in the `hsm2temp.c`.
- Condition for generating of the internal drain node and gate node.
- Derivative calculations in the **Qover** model code (C code only).
- Floating point exception in the **QME** model code.
- Floating point exception in the smoothing functions.
- Maximum gate width for the range check when model parameter `NF != 1`.

For details, refer to the official Hiroshima University HiSIM2 release website:
<http://home.hiroshima-u.ac.jp/usdl/HiSIM2/C-Code/protect.cgi>

HiSIM 2.6.0 Updates

The following is a summary of bug fixes and enhancements from version 2.5.1 to 2.6.0 per the HiSIM-STARC release notes.

1. Model description changes (Refer to *HiSim-STARC User's Manual for detailed information*).
 - Introduction of the Well Proximity Effect (WPE) model with new model parameters WEB, WEC, NSUBCWPE, NSUBPWPE, and NPEXTWPE.
 - New instance parameters: SCA, SCB, and SCC.
 - Improvement of the overlap capacitance model.
 - Activation of Induced Gate Noise model for the C code.
2. Other changes:
 - New guideline for the VZADD0 setting. See *User's Manual*.
 - Default value change for instance parameters NRD and NRS.

For details, refer to the official Hiroshima University HiSIM2 release website:
<http://home.hiroshima-u.ac.jp/usdl/HiSIM2/C-Code/protect.cgi>

HiSIM 2.5.1 Updates

The following is a summary of bug fixes and enhancements from version 2.5.0 to 2.5.1 per the HiSIM-STARC release notes. See the *HiSIM2.5.1 User's Manual* for full details.

1. Update information of HiSIM_2.5.1-Beta-5 from HiSIM_2.5.1-Beta4
 - a. Bug fix in the modeling of the short-channel effect induced by the pocket implantation
 - b. Bug fix in the modeling of the gate leakage currents
 - c. Change of default values for model flags and parameters as follows:

| Parameter | Default |
|-----------|---------|
| VZADD0 | 20E-3 |
| PZADD0 | 20E-3 |

$$M_{Coulomb0} = MUECB0 \cdot \left(\frac{L_{gate} \cdot 10^6}{1\mu m} \right)^{MUECB0LP}$$

Introduction of a channel length dependence for the screening effect of the Coulomb scattering with new model parameters MUECB0LP and MUECB1LP.

$$M_{Coulomb1} = MUECB1 \cdot \left(\frac{L_{gate} \cdot 10^6}{1\mu m} \right)^{MUECB1LP}$$

- d. Change of Min / Max values for model parameter as follows:

| Parameter | Min | Max |
|-----------|----------|----------|
| VOVER | 0 | 50 |
| VMAX | 1.00E+05 | 2.00E+07 |
| VTMP | -5 | 1 |
| MUESR1 | 1.00E+13 | 1.00E+16 |
| SC3VBS | -3 | 0 |

Chapter 2: MOSFET Models

LEVEL 68: STARC HiSIM2 MOSFET Model

Note: Previously (up to beta 4) SC3VBS is not treated as a model parameter. The default value of SC3VBS is now set to zero, which was -2.5 previously.

2. Introduction of range check for NDEPW and NDEPWP.
3. Removal of warning for SC3.
4. Removal of initial jump when COPPRV flag set to 1.
5. Improvement of the overlap capacitance model.
6. Removal of the warning message for channel length modulation in hsm2eval.c.
7. Removal of unnecessary comments in source code.

For details, refer to the official Hiroshima University HiSIM2 release website:
<http://home.hiroshima-u.ac.jp/usdl/HiSIM2/C-Code/protect.cgi>

HiSIM 2.5.0 Updates

The following is a summary of bug fixes and enhancements from version 2.4.3 to 2.5.0 per the HiSim-STARC release notes.

1. A new highly accurate intrinsic capacitance model is added, which is controlled by new model parameter CORECIP (default=0). In addition, if CORECIP=1 is set and an overlap capacitance is added with COADOV=1, it is recommended to give a non-zero NOVER value. For Igb calculation, model parameter values must preserve that VFBC+GLKB3 <= 0.
2. Changed some smoothing parameter values for better fitting.
3. Fixed bugs related to poly-depletion model.
4. Removed negative-capacitance clamping.
5. Fixed several bugs related to QM effects.
6. Added reverse-mode treatment for IGISL and IGIDL.
7. Fixed bugs related to derivative calculations.

HiSIM 2.4.3 Updates

The following summarizes the bug fixes and changes from HiSIM 2.4.2 to 2.4.3 per the HiSim-STARC release note.

1. A bug in hsm2temp was fixed.
2. Bugs of the Vbsz dependence were fixed.
3. Improved capacitance characteristics.

HiSIM 2.4.2 Updates

The following is a summary of bug fixes and changes over version 2.4.1 per the HiSim-STARC release note.

1. The calculation of Taub for NQS model was corrected.
2. The avoidance of zero division.
3. The deletion of the unnecessary sentence.
4. Bug fix of asymmetrical Qover model.
5. The initial setting of GLPART1 was missed.
6. The default value of model parameter ‘VERSION’ was corrected.
7. The calculation of the induced gate noise with M factor != 1 was corrected.
8. The calculation of Igate model was corrected.
9. Changes to the default model parameters as follows:
 - GLKSD2 1e-2
 - GLKSD3 -1e-2
 - FN1 0.0
 - FN2 0.0
 - FVBS 0.0

HiSIM 2.4.1 Updates

The following is a summary of updates and changes from HiSIM 240-SC2 to HiSIM 2.4.1:

1. Induced Gate Noise model: bug fix to avoid division by zero and use of uninitialized values.
2. Impact-ionization-induced Bulk Potential Change model: bug fix of derivatives when **CORSRD = 1**.
3. Bug fix of numerical calculation for surface potentials.
4. The W and/or L dependence of the gate resistance model was discontinuous.
5. Bug fix to avoid division by zero if **DLY1 = 0** and **DLY2 = 0** in **NQS** model.
6. Improved capacitance reciprocity in **AC** analysis.
7. Fixed the inconsistency result of **AC** analysis and **TR** analysis in **NQS** model.

Chapter 2: MOSFET Models

LEVEL 68: STARC HiSIM2 MOSFET Model

8. Bug fix of sign of the parasitic capacitances for the small-signal **NQS** model.
9. Bug fix of handling the multiplication factor **M**.
10. Bug fix of handling the number of gate fingers **NF**.
11. The thermal noise and flicker noise were incorrect in some cases.
12. The temperature specification with an instance parameter **TEMP** was invalid.
13. The **M * NF** was multiplied twice for output values like **gigds** and **gigss**.
14. Bug fix of extrapolation when Vbse less than 10.5 V.
15. Changed the minimum and maximum values of the model parameters **CVB**, **CVBK** and **DDLMAX**.
16. The parameter **SVBSLP**, **SVGSW** and **SVGSWP** were not declared in hsm2mask.
17. Bug fix to avoid the negative **Cgb**.
18. Improvements and bug fixes of the overlap charge model.
19. Bug fix to avoid division by zero in calculation of **Vdx2**.
20. The temperature dependence of the noise value was incorrect.
21. Deleted the unnecessary '#ifdef' statements in hsm2acld.c.
22. Initialize the pyABb_i for **AC-NQS** model.
23. Fixed the gate partitioning model for **Igate**.
24. If **GLPART1 != 0.5**, the option calculating explicitly is selected.

For the full release note for the HiSIM 2.4.1, go to:

<http://www.starc.jp/other/contactus-e.html>

HiSIM 240SC2 Updates

The following changes and fixed issues are implemented in the SC2 release:

- Multiplication factor #M is introduced.
- Bugs in the derivatives of Ps0 in the accumulation zone.
- Bugs in the derivatives of T10 in Igate model.
- Bug in Vdsat output for users (caused by Qover model).
- ISBS2-related bugs in the junction-diode-current model.

- Default values for NSTI and EGIG were wrong. NSTI = 0.0 changed to NSTI = 5.0e17, EGIG = 1.1 changed to EGIG = 0.0
- Coding bug in the DFM model.

Changed Parameters:

- Removed Parameter: SCSTI3
- Replaced Parameters: CLM4 (replaced for DDLTMAX, DDLTICT and DDLTSLP), #LOD (replaced for #SA, #SB, #SD, SAREF and SBREF)
- Renamed Parameter: IGTEMP1 changed to EGIG

| Parameter | Unit | Min | Default | Max | Description |
|--|------------------|--------|---------|--------|--|
| Unit/default value modified parameters | | | | | |
| GIDL4 | V | // | 0.0 | // | Threshold of Vds dependence. |
| LOVER | // | // | 30e-9 | // | Overlap length. |
| NSTI | cm-3 | // | 5.0e17 | // | Substrate-impurity concentration at STI edge. |
| PGD1 | // | // | 0.0 | // | Strength of poly-Si gate depletion. |
| RD | $\Omega \cdot m$ | // | // | // | Drain-contact resistance in LDD region |
| RS | $\Omega \cdot m$ | // | // | // | Source-contact resistance in LDD region |
| VBI | // | // | 1.1 | 1.2 | Built-in potential. |
| Added model flag | | | | | |
| CODFM | None | 0 | 0 | 1 | Flag for DFM support. |
| Added parameters | | | | | |
| #M | None | | 1.0 | | Multiplication factor |
| #NSUBCDFM | None | 1.0e16 | None | 1.0e19 | NSUBC as an instance parameter for DFM support |
| #SA | m | | 0 | | Distance from STI edge to Gate edge |

The // mark indicates values not changed from HiSIM2.3.1-SC2. The # mark indicates instance parameters.

Chapter 2: MOSFET Models

LEVEL 68: STARC HiSIM2 MOSFET Model

| Parameter | Unit | Min | Default | Max | Description |
|-----------|--------------------------|------|---------|------|--|
| #SB | m | | 0 | | Distance from STI edge to Gate edge |
| #SD | m | | 0 | | Distance from Gate edge to Gate edge |
| DDLTICT | None | -3.0 | 10.0 | 20.0 | Lgate dependence of smoothing coeff. |
| DDLTMX | None | 0.0 | 10.0 | 20.0 | Smoothing coefficient for Vds |
| DDLTSLP | 1 / (μm) | 0.0 | 0.0 | 20.0 | Lgate dependence of smoothing coeff. |
| GLKB3 | V | | 0.0 | | Flat-band shift for gate to bulk current |
| MPHDFM | None | -3.0 | -0.3 | 3.0 | NSUBC dependence of μ_{phonon} for DFM support |
| NDEPL | None | | 0.0 | | Modification of Qb contribution for short-channel case |
| NDEPLP | None | | 1.0 | | Modification of Qb contribution for short-channel case |
| NOVER | cm-3 | | 0.0 | | Impurity concentration in overlap region |
| SAREF | m | | 1e-6 | | Reference distance from STI edge to Gate edge |
| SBREF | m | | 1e-6 | | Reference distance from STI edge to Gate edge |
| VDSTI | None | | 0.0 | | Vds dependence of STI subthreshold |
| VFBOVER | V | | -0.5 | | Flat-band voltage in overlap region |
| WSTIW | μm^{WSTIWP} | | 0.0 | | Channel-width dependence of WSTI |
| WSTIWP | None | | 1.0 | | Channel-width dependence of WSTI |
| XL | m | | 0.0 | | Gate length offset due to mask/etch effect |
| XQY1 | $F \cdot \mu m^{QXY2-1}$ | | 0.0 | | Vbs dependence of Qy |

The // mark indicates values not changed from HiSIM2.3.1-SC2. The # mark indicates instance parameters.

| Parameter | Unit | Min | Default | Max | Description |
|-----------|------|-----|---------|-----|---|
| XQY2 | None | | 2.0 | | Lgate dependence of Qy |
| XW | m | | 0.0 | | Gate width offset due to mask/etch effect |

The // mark indicates values not changed from HiSIM2.3.1-SC2. The # mark indicates instance parameters.

6 + 74 × 3 = 228 binning parameters are added in addition to the above parameters.

HiSIM 2.3.1 Updates

The STARC HiSIM2 is Level 68 in the Synopsys MOSFET models. HiSIM2.3.1 is an improved version that resolved many issues of previous releases.

HiSIM version 2.3.1 provides:

- Improved Linear Region Modeling
- Improved Small Size Model
- Improved I_{sub} Model
- Inclusion of Induced Gate Noise
- Support for DFM (Interface to Instance Parameters)

LEVEL 69: PSP Model

The PSP model is a compact MOSFET model intended for digital, analog, and RF designs. It has been jointly developed by the Pennsylvania State University and Philips Research. The roots of this model lie in both SP (Penn State) and MOS Model 11 (Philips).

It is a surface-potential based MOS model containing all relevant physical effects (mobility reduction, velocity saturation, DIBL, gate current, lateral doping gradient effects, STI stress, and so forth), to model present-day and upcoming deep-submicron bulk CMOS technologies. The JUNCAP2 source/drain junction model is an integrated part of PSP.

For a full description of the PSP models, see <http://pspmodel.asu.edu/>.

The following sections discuss these topics:

- [PSP Model Features](#)
 - [PSP Model Updates](#)
 - [Using PSP Model in HSPICE](#)
 - [PSP 103.1 Model Parameters](#)
 - [PSP 103.1 Instance Parameters](#)
 - [PSP Model — Output Templates](#)
-

PSP Model Features

The PSP general features of this model are:

- Physical surface-potential-based formulation in both intrinsic and extrinsic model modules
- Physical and accurate description of the accumulation region
- Inclusion of all relevant small-geometry effects
- Modeling of the halo implant effects, including the output conductance degradation in long devices
- Coulomb scattering and non-universality in the mobility model
- Non-singular velocity-field relation enabling the modeling of RF distortions, including inter-modulation effects
- Complete Gummel symmetry

- Mid-point bias linearization enabling accurate modeling of the ration-based circuits (for example, R2R circuits)
- Quantum-mechanical corrections
- Correction for the polysilicon depletion effects
- Gate-induced drain leakage (GIDL) and gate-induced source leakage current (GISL) model
- Surface-potential-based noise model including channel thermal noise, flicker noise, and channel-induced gate noise
- Advanced junction model, including trap-assisted tunneling, band-to-band tunneling, and avalanche breakdown
- Spline-collocation-based non-quasi-static (NQS) model, including all terminal currents
- Stress model (based on BSIM4 version)

PSP Model Updates

This section provides the PSP100 model version updates:

- [PSP 103.1 Model Updates](#)
- [PSP103.0 Model Updates](#)
- [PSP102.3 Model Updates](#)
- [PSP102.2 Model Updates](#)
- [PSP102.1 Model Updates](#)
- [PSP102.0 Model Updates](#)
- [PSP101.0 Model Updates](#)
- [PSP100.1 Model Updates](#)

PSP 103.1 Model Updates

The following updates were made in PSP v103.1:

- Added external sheet resistance `RSHD` for drain diffusion (used when `SWJUNASYM = 1`).
- Bug-fix and minor implementation change in NUD-model.
- Minor bug-fix in conditional for SP-calculation of overlap areas.

PSP103.0 Model Updates

The PSP103 model is NOT completely backward-compatible with PSP102.3.

The main changes are:

- Global, local and binning models are unified. When `SWGEO = 1` (default) the global model is used. When `SWGEO = 0` the local model is selected. The binning model is invoked if `SWGEO` is set to 2.
- Added non-uniform doping (NUD) model. The model can be invoked on by setting `SWNUD = 1` or 2. When `SWNUD = 1`, a separate surface potential calculation is carried out and the NUD model does not affect the CV results. This avoids non-reciprocal capacitances. When `SWNUD = 2`, the extra surface potential calculation is skipped and this may result in non-reciprocal capacitances.
- Added related model parameters `GFACNUDO`, `GFACNUDL`, `GFACNUDLEXP`, `GFACNUDW`, `GFACNUDLW`, `VSBNUDO` and `DVSBNUDO` to global, `GFACNUD`, `VSBNUD` and `DVSBNUD` to local and `POGFACNUD`, `PLGFACNUD`, `PWGFACTUD`, `PLWGFACTUD`, `POVSBNUD` and `PODVSBNUD` to binning models.
- Added Vth-adjustment model for CV. It can be turned on by setting `SWDELVTAC = 1`. Note that this requires extra computation of surface potentials. Added related model parameters `FACNEFFACO`, `FACNEFFACL`, `FACNEFFACW`, `FACNEFFACLW`, `DELVTACO`, `DELVTACL`, `DELVTACLEXP`, `DELVTACW` and `DELVTACLW` to global, `FACNEFFAC` and `DELVTAC` to local and `POFACNEFFAC`, `PLFACNEFFAC`, `PWFACNEFFAC`, `PLWFACNEFFAC`, `PODELVTAC`, `PLDELVTAC`, `PWDELVTAC` and `PLWDELVTAC` to binning model.
- Added external diffusion resistances to source and drain.
- Added instance parameters `NRS` and `NRD`; added model parameters `RSH` to global and binning, `RSE` and `RDE` to local model.
- Modified the geometrical scaling rules of following parameters: `VFB`, `STVFB`, `DPHIB`, `STBET`, and `STTHESAT`.
- Modified the binning rule of `BETN`.
- Removed the effect of `FETA` from `CV`.
- Some minor bug-fixes and implementation changes.

PSP102.3 Model Updates

PSP 102.3 is backward compatible with PSP 102.2. The main changes are:

- Added asymmetric junction model for the drain-bulk junction. The new junction parameters have a suffix “D” added to their names. When SWJUNASYM = 1 the original parameters are used for the sourcebulk junction and the new parameters are used for drain-bulk junction. When SWJUNASYM = 0 the original junction parameters are used for both sourcebulk and drain-bulk junctions as in symmetric case, and the new junction parameters are neglected.
- Added asymmetric models for the overlap region of the drain side. These include:
 - Added related model parameters TOXOVDO, LOVD and NOVDO to global, TOXOVD and NOVD to local and POTOXOVD, PONOVD, PLNOVD, PWNOVD and PLWNOVD to binning models.
 - Asymmetric GIDL/GISL model. Added related parameters AGIDLDW, BGIDLDO, STBGIDLDO and CGIDLDO to global, AGIDLD, BGIDLD, STBGIDLD and CGIDLD to local and POAGIDLD, PLAGIDLD, PWAGIDLD, PLWAGIDLD, POBGIDLD, POSTBGIDLD and POCGIDLD to binning models.
 - Asymmetric overlap gate current model. Added related parameters IGOVDW to global, IGOVD to local and POIGOVD, PLIGOVD, PWIGOVD and PLWIGOVD to binning models.
 - Asymmetric overlap capacitance model. Added related parameters CGOVD to local, POCGOVD, PLCGOVD, PWCGOVD and PLWCGOVD to binning models.
 - Asymmetric outer fringe capacitance model. Added related parameters CFRDW to global, CFRD to local and POCFRD, PLCFRD, PWCFRD and PLWCFRD to binning models.
- When SWJUNASYM = 1 the original parameters for the models listed above are used for the source side and the newly added parameters are used for the drain side. When SWJUNASYM = 0 the original parameters are used for both source and drain sides and the new parameters are ignored.
- Added EF (local), EFO (global) and POEF (binning) as flicker noise frequency exponent parameters.

Chapter 2: MOSFET Models

LEVEL 69: PSP Model

- Added noise parameters `LINTNOI` and `ALPNOI` to global model to increase the flexibility of the length scaling of the flicker noise.
- Some minor bug-fixes and implementation changes.

PSP102.2 Model Updates

The PSP102.2 model is backward-compatible with PSP102.1.

The main changes are:

- Added well proximity effect (WPE) model according to CMC's specification
- Added parameters `EPSROX` (local), `EPSROXO` (global), `POEPSROX` (binning) representing relative dielectric constant of gate oxide
- Added instance parameters `DELVTO` and `FACTUO` to local, global, and binning model
- Added `NF` support to global and binning model
- Extended stress model to support `NF`
- Added substrate resistance network and external gate resistance to PSP model besides `NQS` mode
- Added geometry scaling for gate resistance in global and binning models, resulting in additional model parameters `RSHG`, `RINT`, `DLSIL`, and `RVPOLY` and instance parameters `NGCON` and `XGW`
- Added JUNCAP2 Express as an optional alternative to the full JUNCAP2 model. Added related model parameters `SWJUNEXP`, `VJUNREF`, and `FJUNQ`, using model parameter `SWJUNEXP=1` to enable JUNCAP2 Express model
- Added “dummy” parameters `LMIN`, `LMAX`, `WMIN`, `WMAX` to binning model, which can be used as labels for the binning parameter sets
- Some minor bug fixes and minor implementation changes

PSP102.1 Model Updates

The PSP102.1 model is backward-compatible with PSP102.0.

The main changes include:

- Added clipping boundaries for `SWNQS`
- Made several minor changes and improvements in model implementation
- Solved bug in stress model
- Solved bug in JUNCAP2

PSP102.0 Model Updates

The PSP102.0 model is backward-compatible with PSP101.0 in all practical cases.

The most important changes include:

- The value for LG when SWJUNCAP=2 was corrected
- The clipping/limiting behavior of NP has been made more transparent
- A minor numerical issue was resolved
- The scaling rule for DPHIB is now correctly implemented

PSP101.0 Model Updates

The PSP101.0 model is *not* backward compatible with PSP100.1.

The most important changes include:

- A complete set of binning scaling rules was added as a phenomenological alternative to the physics-based geometrical scaling rules
- BSIM-like instance parameters AS, AD, PS and PD were added for the junction model
- To avoid confusion between zeros and “O”s, zeros no longer occur in parameter names. They have all been replaced by “O”s
- Some global parameter names have an additional “O” in their names in order to avoid duplicate names in the global and local model

PSP100.1 Model Updates

The PSP100.1 model is compatible with the PSP100 model. It improves performance by about a factor of 2, and adds a thermal noise coefficient (FNT) parameter. This parameter is used to add in thermal noise. Set FNT=1 (default) to turn on thermal noise. Set FNT=0 to turn off thermal noise.

Using PSP Model in HSPICE

The PSP model is Level 69 in the Synopsys MOSFET models. To use this model, specify:

```
M1 drain gate source bulk NCH w=4u l=1u
.MODEL NCH NMOS LEVEL=69
+ SWGEO =[0|1|2]
+ VERSION=num
```

Where,

- SWGEO=0: Local model
- SWGEO=1: Default, Global model
- SWGEO=2: Binning model
- VERSION=*num*: Specify version number of the PSP model

See Also

- [.OPTION VER_CONTROL](#)

PSP 103.1 Model Parameters

This section covers the following PSP model parameters:

- [PSP 103.1 Model — Basic Parameters](#)
- [PSP 103.1 Model — Switch Parameters](#)
- [PSP 103.1 Model — Labels for Binning Set](#)
- [PSP 103.1 Model — Process Parameters](#)
- [PSP 103.1 Model — DIBL Parameters](#)
- [PSP 103.1 Model — Mobility Parameters](#)
- [PSP 103.1 Model — Series Resistance Parameters](#)
- [PSP 103.1 Model — Velocity Saturation Parameters](#)
- [PSP 103.1 Model — Saturation Voltage Parameters](#)
- [PSP 103.1 Model — Channel Length Modulation \(CLM\) Parameters](#)
- [PSP 103.1 Model — Impact Ionization \(II\) Parameters](#)
- [PSP 103.1 Model — Gate Current Parameters](#)
- [PSP 103.1 Model — Gate-Induced Drain Leakage \(GIDL\) Parameters](#)
- [PSP 103.1 Model — Charge Model Parameters](#)
- [PSP 103.1 Model — Noise Model Parameters](#)
- [PSP 103.1 Model — Stress Model Parameters](#)
- [PSP 103.1 Model — Well Proximity Effect \(WPE\) Model Parameters](#)
- [PSP 103.1 Model — Source-bulk and Drain-bulk Junction Model Parameters](#)

- [PSP 103.1 Model — Parasitic Resistance Model Parameters](#)
- [PSP 103.1 Model — NQS Model Parameters](#)

PSP 103.1 Model — Basic Parameters

| Name | Unit | Default | Min. | Max. | Description | SWGEO ¹ |
|---------|------|---------|------|------|--|--------------------|
| VERSION | - | 103.11 | - | - | PSP version selection parameter | 0, 1, 2 |
| TYPE | - | 1 | -1 | - | Channel type parameter; 1: NMOS, -1: PMOS ¹ | 0, 1, 2 |
| TR | °C | 21 | -273 | - | Reference temperature | 0, 1, 2 |
| DTA | K | 0 | - | - | Temperature offset with respect to ambient circuit temperature | 0, 1, 2 |

1. *Indicates for which value of SWGEO the listed parameter is used.*

PSP 103.1 Model — Switch Parameters

| Name | Unit | Default | Min. | Max. | Description | SWGEO ¹ |
|-----------|------|---------|------|------|---|--------------------|
| SWGEO | - | 1 | 0 | 2 | Flag for geometrical model (0: local, 1:global, 2: binning) | 0, 1, 2 |
| SWIGATE | - | 0 | 0 | 1 | Flag for gate current (0: off) | 0, 1, 2 |
| SWIMPACT | - | 0 | 0 | 1 | Flag for impact ionization current (0: off) | |
| SWGIDL | - | 0 | 0 | 1 | Flag for GIDL/GISL current (0: off) | 0, 1, 2 |
| SWJUNCAP | - | 0 | 0 | 3 | Flag for JUNCAP (0: off) | 0, 1, 2 |
| SWJUNASYM | - | 0 | - | - | Flag for asymmetric junctions (0: off) | 0, 1, 2 |
| SWNUD | - | 0 | 0 | 2 | Flag for NUD-effect (0: off) | 0, 1, 2 |
| SWDELVTAC | - | 0 | 0 | 1 | Flag for separate charge calculation (0: off) | 0, 1, 2 |
| QMC | - | 1 | 0 | - | Quantum-mechanical correction factor | 0, 1, 2 |

1. *Indicates for which value of SWGEO the listed parameter is used.*

Chapter 2: MOSFET Models

LEVEL 69: PSP Model

PSP 103.1 Model — Labels for Binning Set

| Name | Unit | Default | Min. | Max. | Description | SWGEO ¹ |
|------|------|---------|------|------|--------------------------------------|--------------------|
| LMIN | m | 0 | - | - | Dummy parameter to label binning set | 2 |
| LMAX | m | 1 | - | - | Dummy parameter to label binning set | 2 |
| WMIN | m | 0 | - | - | Dummy parameter to label binning set | 2 |
| WMAX | m | 1 | - | - | Dummy parameter to label binning set | 2 |

1. Indicates for which value of SWGEO the listed parameter is used.

PSP 103.1 Model — Process Parameters

| Name | Unit | Default | Min. | Max. | Description | SWGEO ¹ |
|-------|------|---------|------|------|--|--------------------|
| LVARO | m | 0 | - | - | Geometry independent difference between actual and programmed poly-silicon gate length | 1, 2 |
| LVARL | - | 0 | - | - | Length dependence of ΔL_{PS} | 1, 2 |
| LVARW | - | 0 | - | - | Width dependence of ΔL_{PS} | 1, 2 |
| LAP | m | 0 | - | - | Effective channel length reduction per side due to lateral diffusion of source /drain dopant ions | 1, 2 |
| WVARO | m | 0 | - | - | Geometry independent difference between actual and programmed field-oxide opening | 1, 2 |
| WVARL | - | 0 | - | - | Length dependence of ΔW_{OD} | 1, 2 |
| WVARW | - | 0 | - | - | Width dependence of ΔW_{OD} | 1, 2 |
| WOT | m | 0 | - | - | Effective reduction of channel width per side due to lateral diffusion of channel-stop dopant ions | 1, 2 |
| DLQ | m | 0 | - | - | Effective channel length offset for CV | 1, 2 |
| DWQ | m | 0 | - | - | Effective channel width offset for CV | 1, 2 |
| VFB | V | -1 | - | - | Flat-band voltage at TR | 0 |

| Name | Unit | Default | Min. | Max. | Description | SWGEO ¹ |
|----------|------|-------------------|------------|------|--|--------------------|
| VFBO | V | -1 | - | - | Geometry-independent part | 1 |
| VFBL | V | 0 | - | - | Length dependence | 1 |
| VFBW | V | 0 | - | - | Width dependence | 1 |
| VFBLW | V | 0 | - | - | Area dependence | 1 |
| POVFB | V | -1 | - | - | Geometry independent part | 2 |
| PLVFB | V | 0 | - | - | Length dependence | 2 |
| PWVFB | V | 0 | - | - | Width dependence | 2 |
| PLWVFB | V | 0 | - | - | Length times width dependence | 2 |
| STVFB | V/K | $5 \cdot 10^{-4}$ | - | - | Temperature dependence of VFB | 0 |
| STVFBO | V/K | $5 \cdot 10^{-4}$ | - | - | Geometry-independent part | 1 |
| STVFBL | V/K | 0 | - | - | Length dependence | 1 |
| STVFBW | V/K | 0 | - | - | Width dependence | 1 |
| STVFBLW | V/K | 0 | - | - | Area dependence | 1 |
| POSTVFB | V/K | $5 \cdot 10^{-4}$ | - | - | Geometry independent part | 2 |
| PLSTVFB | V/K | 0 | - | - | Length dependence | 2 |
| PWSTVFB | V/K | 0 | - | - | Width dependence | 2 |
| PLWSTVFB | V/K | 0 | - | - | Length times width dependence | 2 |
| TOX | m | $2 \cdot 10^{-9}$ | 10^{-10} | - | Gate oxide thickness | 0 |
| TOXO | m | $2 \cdot 10^{-9}$ | 10^{-10} | - | Gate oxide thickness | 1 |
| POTOX | m | $2 \cdot 10^{-9}$ | - | - | Geometry independent part | 2 |
| EPSROX | - | 3.9 | 1 | - | Relative permittivity of gate dielectric | 0 |
| EPSROXO | - | 3.9 | 1 | - | Geometry independent part | 1 |
| POEPSROX | - | 3.9 | 1 | - | Geometry independent part | 2 |

Chapter 2: MOSFET Models

LEVEL 69: PSP Model

| Name | Unit | Default | Min. | Max. | Description | SWGEO ¹ |
|------------|-----------------|-------------|------------|-----------|---|--------------------|
| NEFF | m^{-3} | 5.10^{23} | 10^{20} | 10^{26} | Substrate doping | 0 |
| NSUBO | m^{-3} | 3.10^{23} | 10^{20} | - | Geometry independent substrate doping | 1 |
| NSUBW | - | 0 | - | - | Width dependence of substrate doping due to segregation | 1 |
| WSEG | m | 10^{-8} | 10^{-10} | - | Characteristic length for segregation of substrate doping | 1 |
| NPCK | m^{-3} | 10^{24} | 0 | - | Pocket doping level | 1 |
| NPCKW | - | 0 | - | - | Width dependence of NPCK due to segregation | 1 |
| WSEGP | m | 10^{-8} | 10^{-10} | - | Characteristic length for segregation of pocket doping | 1 |
| LPCK | m | 10^{-8} | 10^{-10} | - | Characteristic length for lateral doping profile | 1 |
| LPCKW | - | 0 | - | - | Width dependence of LPCK due to segregation | 1 |
| FOL1 | - | 0 | - | - | First order length dependence of short channel body-effect | 1 |
| FOL2 | - | 0 | - | - | Second order length dependence of short channel body-effect | 1 |
| PONEFF | m^{-3} | 5.10^{23} | - | - | Geometry independent part | 2 |
| PLNEFF | m^{-3} | 0 | - | - | Length dependence | 2 |
| PWNEFF | m^{-3} | 0 | - | - | Width dependence | 2 |
| PLWNEFF | m^{-3} | 0 | - | - | Length times width dependence | 2 |
| FACNEFFAC | - | 1 | 0 | - | Pre-factor for effective substrate doping in separate charge calculation when SWDELVTAC = 1 | 0 |
| FACNEFFACO | - | 1 | 0 | - | Geometry independent part | 1 |
| FACNEFFACL | - | 0 | - | - | Length dependence | 1 |

| Name | Unit | Default | Min. | Max. | Description | SWGEO ¹ |
|--------------|------|---------|------|------|--|--------------------|
| FACNEFFACW | - | 0 | - | - | Width dependence | 1 |
| FACNEFFACLW | - | 0 | - | - | Area dependence | 1 |
| POFACNEFFAC | - | 1 | - | - | Geometry independent part | 2 |
| PLFACNEFFAC | - | 0 | - | - | Length dependence | 2 |
| PWFACNEFFAC | - | 0 | - | - | Width dependence | 2 |
| PLWFACNEFFAC | - | 0 | - | - | Area dependence | 2 |
| GFACNUD | - | 1 | 0.01 | - | Body factor change due to NUD-effect | 0 |
| GFACNUDO | - | 1 | - | - | Geometry independent part | 1 |
| GFACNUDL | - | 0 | - | - | Length dependence | 1 |
| GFACNUDLEXP | - | 1 | - | - | Exponent for length dependence | 1 |
| GFACNUDW | - | 0 | - | - | Width dependence | 1 |
| GFACNUDLW | - | 0 | - | - | Area dependence | 1 |
| POGFACNUD | - | 1 | - | - | Geometry independent part | 2 |
| PLGFACNUD | - | 0 | - | - | Length dependence | 2 |
| PWGFACNUD | - | 0 | - | - | Width dependence | 2 |
| PLWGFACNUD | - | 0 | - | - | Area dependence | 2 |
| VSBNUD | V | 0 | 0 | - | Lower V_{SB} -value for NUD-effect | 0 |
| VSBNUDO | V | 0 | - | - | Geometry independent part | 1 |
| POVSBNUD | V | 0 | - | - | Geometry independent part | 2 |
| DVSBNUD | V | 1 | 0.1 | - | V_{SB} -range for NUD-effect | 0 |
| DVSBNUDO | V | 1 | - | - | Geometry independent part | 1 |
| PODVSBNUD | V | 1 | - | - | Geometry independent part | 2 |
| VNSUB | V | 0 | - | - | Effective doping bias-dependence parameter | 0 |

Chapter 2: MOSFET Models

LEVEL 69: PSP Model

| Name | Unit | Default | Min. | Max. | Description | SWGEO ¹ |
|-------------|----------|---------|-----------|------|--|--------------------|
| VNSUBO | V | 0 | - | - | Geometry independent part | 1 |
| POVNSUB | V | 0 | - | - | Geometry independent part | 2 |
| NSLP | V | 0.05 | 10^{-3} | - | Effective doping bias-dependence parameter | 0 |
| NSLPO | V | 0.05 | - | - | Geometry independent part | 1 |
| PONSLP | V | 0.05 | - | - | Geometry independent part | 2 |
| DNSUB | V^{-1} | 0 | 0 | 1 | Effective doping bias-dependence parameter | 0 |
| DNSUBO | V^{-1} | 0 | - | - | Geometry independent part | 1 |
| PODNSUB | V^{-1} | 0 | - | - | Geometry independent part | 2 |
| DPHIB | V | 0 | - | - | Offset of ϕ_B | 0 |
| DPHIBO | V | 0 | - | - | Geometry independent part | 1 |
| DPHIBL | V | 0 | - | - | Length dependence | 1 |
| DPHIBLEXP | - | 1 | - | - | Exponent for length dependence | 1 |
| DPHIBW | V | 0 | - | - | Exponent for length dependence | 1 |
| DPHIBLW | V | 0 | - | - | Area dependence | 1 |
| PODPHIB | V | 0 | - | - | Geometry independent part | 2 |
| PLDPHIB | V | 0 | - | - | Length dependence | 2 |
| PWDPHIB | V | 0 | - | - | Width dependence | 2 |
| PLWDPHIB | V | 0 | - | - | Length times width dependence | 2 |
| DELVTAC | V | 0 | - | - | Offset of ϕ_B in separate charge calculation when SWDELVTAC = 1 | 0 |
| DELVTACO | V | 0 | - | - | Geometry independent part | 1 |
| DELVTACL | - | 1 | - | - | Length dependence | 1 |
| DELVTACLEXP | V | 0 | - | - | Exponent for length dependence | 1 |

| Name | Unit | Default | Min. | Max. | Description | SWGEO ¹ |
|------------|-----------------|------------------|------|------|--------------------------------|--------------------|
| DELVTACW | V | 0 | - | - | Width dependence | 1 |
| DELVTACLW | V | 0 | - | - | Area dependence | 1 |
| PODELVTAC | V | 0 | - | - | Geometry independent part | 2 |
| PLDELVTAC | V | 0 | - | - | Length dependence | 2 |
| PWDELVTAC | V | 0 | - | - | Width dependence | 2 |
| PLWDELVTAC | V | 0 | - | - | Length times width dependence | 2 |
| NP | m ⁻³ | 10 ²⁶ | 0 | - | Gate poly-silicon doping | 0 |
| NPO | m ⁻³ | 10 ²⁶ | - | - | Geometry-independent part | 1 |
| NPL | - | 0 | - | - | Length dependence | 1 |
| PONP | m ⁻³ | 10 ²⁶ | - | - | Geometry independent part | 2 |
| PLNP | m ⁻³ | - | - | - | Length dependence | 2 |
| PWNP | m ⁻³ | - | - | - | Width dependence | 2 |
| PLWNP | m ⁻³ | - | - | - | Length times width dependence | 2 |
| CT | - | 0 | 0 | - | Interface states factor | 0 |
| CTO | - | 0 | - | - | Geometry-independent part | 1 |
| CTL | - | 0 | - | - | Length dependence | 1 |
| CTLEXP | - | 1 | - | - | Exponent for length dependence | 1 |
| CTW | - | 0 | - | - | Width dependence | 1 |
| CTLW | - | 0 | - | - | Area dependence | 1 |
| POCT | - | 0 | - | - | Geometry independent part | 2 |
| PLCT | - | 0 | - | - | Length dependence | 2 |
| PWCT | - | 0 | - | - | Width dependence | 2 |
| PLWCT | - | 0 | - | - | Length times width dependence | 2 |

Chapter 2: MOSFET Models

LEVEL 69: PSP Model

| Name | Unit | Default | Min. | Max. | Description | SWGEO ¹ |
|----------|-----------------|-------------------|------------|-----------|---|--------------------|
| TOXOV | m | $2 \cdot 10^{-9}$ | 10^{-10} | - | Overlap oxide thickness | 0 |
| TOXOVO | m | $2 \cdot 10^{-9}$ | 10^{-10} | - | Geometry independent part | 1 |
| POTOXOV | m | $2 \cdot 10^{-9}$ | - | - | Geometry independent part | 2 |
| TOXOVD | m | $2 \cdot 10^{-9}$ | 10^{-10} | - | Overlap oxide thickness for drain side | 0 |
| TOXOVD0 | m | $2 \cdot 10^{-9}$ | 10^{-10} | - | Geometry independent part | 1 |
| POTOXOVD | m | $2 \cdot 10^{-9}$ | - | - | Geometry independent part | 2 |
| LOV | m | 0 | 0 | - | Overlap length for overlap capacitance | 1 |
| LOVD | m | 0 | 0 | - | Overlap length for gate/drain overlap capacitance | 1 |
| NOV | m^{-3} | $5 \cdot 10^{25}$ | 10^{20} | 10^{27} | Effective doping of overlap region | 0 |
| NOVO | m^{-3} | $5 \cdot 10^{25}$ | - | - | Geometry independent part | 1 |
| PONOV | m^{-3} | $5 \cdot 10^{25}$ | - | - | Geometry independent part | 2 |
| PLNOV | m^{-3} | 0 | - | - | Length dependence | 2 |
| PWNOV | m^{-3} | 0 | - | - | Width dependence | 2 |
| PLWNOV | m^{-3} | 0 | - | - | Length times width dependence | 2 |
| NOVD | m^{-3} | $5 \cdot 10^{25}$ | 10^{20} | 10^{27} | Effective doping of overlap region for drain side | 0 |
| NOVDO | m^{-3} | $5 \cdot 10^{25}$ | - | - | Geometry independent part | 1 |
| PONOVD | m^{-3} | $5 \cdot 10^{25}$ | - | - | Geometry independent part | 2 |
| PLNOVD | m^{-3} | 0 | - | - | Length dependence | 2 |
| PWNOVD | m^{-3} | 0 | - | - | Width dependence | 2 |
| PLWNOVD | m^{-3} | 0 | - | - | Length times width dependence | 2 |

1. Indicates for which value of SWGEO the listed parameter is used.

PSP 103.1 Model — DIBL Parameters

| Name | Unit | Default | Min. | Max. | Description | SWGEO ¹ |
|--------|-----------------|---------|------|------|--------------------------------|--------------------|
| CF | - | 0 | 0 | - | DIBL parameter | 0 |
| CFL | - | 0 | - | - | Length dependence | 1 |
| CFLEXP | - | 2 | - | - | Exponent for length dependence | 1 |
| CFW | - | 0 | - | - | Width dependence | 1 |
| POCF | - | 0 | - | - | Geometry independent part | 2 |
| PLCF | - | 0 | - | - | Length dependence | 2 |
| PWCF | - | 0 | - | - | Width dependence | 2 |
| PLWCF | - | 0 | - | - | Length times width dependence | 2 |
| CFB | V ⁻¹ | 0 | 0 | 1 | Back-bias dependence of CF | 0 |
| CFBO | V ⁻¹ | 0 | - | - | Geometry independent part | 1 |
| POCFB | V ⁻¹ | 0 | - | - | Geometry independent part | 2 |

1. Indicates for which value of SWGEO the listed parameter is used.

PSP 103.1 Model — Mobility Parameters

| Name | Unit | Default | Min. | Max. | Description | SWGEO ¹ |
|--------|---------------------|--------------------|-------------------|------|---|--------------------|
| BETN | m ² /V/s | 7.10 ⁻² | 0 | - | Product of channel aspect ratio and zero-field mobility at TR | 0 |
| UO | m ² /V/s | 5.10 ⁻² | - | - | Zero-field mobility at TR | 1 |
| FBET1 | - | 0 | - | - | Relative mobility decrease due to first lateral profile | 1 |
| FBET1W | - | 0 | - | - | Width dependence of FBET1 | 1 |
| LP1 | m | 10 ⁻⁸ | 10 ⁻¹⁰ | - | Mobility-related characteristic length of first lateral profile | 1 |
| LP1W | - | 0 | - | - | Width dependence of LP1 | 1 |

Chapter 2: MOSFET Models

LEVEL 69: PSP Model

| Name | Unit | Default | Min. | Max. | Description | SWGEO ¹ |
|----------|------------------------------------|-------------------|------------|------|--|--------------------|
| FBET2 | - | 0 | - | - | Relative mobility decrease due to second lateral profile | 1 |
| LP2 | m | 10^{-8} | 10^{-10} | - | Mobility-related characteristic length of second lateral profile | 1 |
| BETW1 | - | 0 | - | - | First higher-order width scaling coefficient of BETN | 1 |
| BETW2 | - | 0 | - | - | Second higher-order width scaling coefficient of BETN | 1 |
| WBET | m | 10^{-9} | 10^{-10} | - | Characteristic width for width scaling of BETN | 1 |
| POBETN | $\text{m}^2/\text{V}\cdot\text{s}$ | $7 \cdot 10^{-2}$ | - | - | Geometry independent part | 2 |
| PLBETN | $\text{m}^2/\text{V}\cdot\text{s}$ | 0 | - | - | Length dependence | 2 |
| PWBETN | $\text{m}^2/\text{V}\cdot\text{s}$ | 0 | - | - | Width dependence | 2 |
| PLWBETN | $\text{m}^2/\text{V}\cdot\text{s}$ | 0 | - | - | Length times width dependence | 2 |
| STBET | 0 | 1 | - | - | Temperature dependence of BETN | 0 |
| STBETO | 0 | 1 | - | - | Geometry independent part | 1 |
| STBETL | 0 | 0 | - | - | Length dependence | 1 |
| STBETW | 0 | 0 | - | - | Width dependence | 1 |
| STBETLW | 0 | 0 | - | - | Area dependence | 1 |
| POSTBET | 0 | 1 | - | - | Geometry independent part | 2 |
| PLSTBET | 0 | 0 | - | - | Length dependence | 2 |
| PWSTBET | 0 | 0 | - | - | Width dependence | 2 |
| PLWSTBET | 0 | 0 | - | - | Length times width dependence | 2 |
| MUE | m/V | 0.5 | 0 | - | Mobility reduction coefficient at TR | 0 |
| MUEO | m/V | 0.5 | - | - | Geometry independent part | 1 |
| MUEW | - | 0 | - | - | Width dependence | 1 |

| Name | Unit | Default | Min. | Max. | Description | SWGEO ¹ |
|-----------|------|---------|------|------|------------------------------------|--------------------|
| POMUE | m/V | 0.5 | - | - | Geometry independent part | 2 |
| PLMUE | m/V | 0 | - | - | Length dependence | 2 |
| PWMUE | m/V | 0 | - | - | Width dependence | 2 |
| PLWMUE | m/V | 0 | - | - | Length times width dependence | 2 |
| STMUE | - | 0 | - | - | Temperature dependence of MUE | 0 |
| STMUEO | - | 0 | - | - | Geometry independent part | 1 |
| POSTMUE | - | 0 | - | - | Geometry independent part | 2 |
| THEMU | - | 1.5 | 0 | - | Mobility reduction exponent at TR | 0 |
| THEMUO | - | 1.5 | 0 | - | Geometry independent part | 1 |
| POTHEMU | - | 1.5 | - | - | Geometry independent part | 2 |
| STTHEMU | - | 1.5 | - | - | Temperature dependence of THEMU | 0 |
| STTHEMUO | - | 1.5 | - | - | Geometry independent part | 1 |
| POSTTHEMU | - | 1.5 | - | - | Geometry independent part | 2 |
| CS | - | 0 | 0 | - | Coulomb scattering parameter at TR | 0 |
| CSO | - | 0 | - | - | Geometry independent part | 1 |
| CSL | - | 0 | - | - | Length dependence | 1 |
| CSLEXP | - | 1 | - | - | Exponent for length dependence | 1 |
| CSW | - | 0 | - | - | Width dependence | 1 |
| CSLW | - | 0 | - | - | Area dependence | 1 |
| POCS | - | 0 | - | - | Geometry independent part | 2 |
| PLCS | - | 0 | - | - | Length dependence | 2 |
| PWCS | - | 0 | - | - | Width dependence | 2 |
| PLWCS | - | 0 | - | - | Length times width dependence | 2 |
| STCS | - | 0 | - | - | Temperature dependence of CS | 0 |

Chapter 2: MOSFET Models

LEVEL 69: PSP Model

| Name | Unit | Default | Min. | Max. | Description | SWGEO ¹ |
|----------|-----------------|---------|------|------|--------------------------------|--------------------|
| STCSO | - | 0 | - | - | Geometry independent part | 1 |
| POSTCS | - | 0 | - | - | Geometry independent part | 2 |
| XCOR | V ⁻¹ | 0 | 0 | - | Non-universality parameter | 0 |
| XCORO | V ⁻¹ | 0 | - | - | Geometry independent part | 1 |
| XCORL | - | 0 | - | - | Length dependence | 1 |
| XCORW | - | 0 | - | - | Width dependence | 1 |
| XCORLW | - | 0 | - | - | Area dependence | 1 |
| POXCOR | V ⁻¹ | 0 | - | - | Geometry independent part | 2 |
| PLXCOR | V ⁻¹ | 0 | - | - | Length dependence | 2 |
| PWXCOR | V ⁻¹ | 0 | - | - | Width dependence | 2 |
| PLWXCOR | V ⁻¹ | 0 | - | - | Length times width dependence | 2 |
| STXCOR | - | 0 | - | - | Temperature dependence of XCOR | 0 |
| STXCORO | - | 0 | - | - | Geometry independent part | 1 |
| POSTXCOR | - | 0 | - | - | Geometry independent part | 2 |
| FETA | - | 1 | 0 | - | Effective field parameter | 0 |
| FETAO | - | 1 | - | - | Geometry independent part | 1 |
| POFETA | - | 1 | - | - | Geometry independent part | 2 |

1. Indicates for which value of SWGEO the listed parameter is used.

PSP 103.1 Model — Series Resistance Parameters

| Name | Unit | Default | Min. | Max. | Description | SWGEO ¹ |
|------|----------|---------|------|------|---|--------------------|
| RS | Ω | 30 | 0 | - | Source/drain series resistance at TR | 0 |
| RSW1 | Ω | 50 | - | - | Source/drain series resistance for a channel width W_{EN} | 1 |

| Name | Unit | Default | Min. | Max. | Description | SWGEO ¹ |
|--------|----------|---------|------|------|-------------------------------|--------------------|
| RSW2 | - | 0 | - | - | Higher-order width scaling | 1 |
| PORS | Ω | 30 | - | - | Geometry independent part | 2 |
| PLRS | Ω | 0 | - | - | Length dependence | 2 |
| PWRS | Ω | 0 | - | - | Width dependence | 2 |
| PLWRS | Ω | 0 | - | - | Length times width dependence | 2 |
| STRS | - | 1 | - | - | Temperature dependence of RS | 0 |
| STRSO | - | 1 | - | - | Geometry dependent part | 1 |
| POSTRS | - | 1 | - | - | Geometry independent part | 2 |
| RSB | V^{-1} | 0 | -0.5 | - | Back-bias dependence of RS | 0 |
| RSBO | V^{-1} | 0 | - | - | Geometry independent part | 1 |
| PORSB | V^{-1} | 0 | - | - | Geometry independent part | 2 |
| RSG | V^{-1} | 0 | -0.5 | - | Gate-bias dependence of RS | 0 |
| RSGO | V^{-1} | 0 | - | - | Geometry independent part | 1 |
| PORSG | V^{-1} | 0 | - | - | Geometry independent part | 2 |

1. Indicates for which value of SWGEO the listed parameter is used.

PSP 103.1 Model — Velocity Saturation Parameters

| Name | Unit | Default | Min. | Max. | Description | SWGEO ¹ |
|------------|----------|---------|------|------|-------------------------------------|--------------------|
| THESAT | V^{-1} | 1 | 0 | - | Velocity saturation parameter at TR | 0 |
| THESATO | V^{-1} | 0 | - | - | Geometry independent part | 1 |
| THESATL | V^{-1} | 0.05 | - | - | Length dependence | 1 |
| THESATLEXP | - | 1 | - | - | Exponent for length dependence | 1 |
| THESATW | - | 0 | - | - | Width dependence | 1 |

Chapter 2: MOSFET Models

LEVEL 69: PSP Model

| Name | Unit | Default | Min. | Max. | Description | SWGEO ¹ |
|-------------|-----------------|---------|------|------|---|--------------------|
| THESATLW | - | 0 | - | - | Area dependence | 1 |
| POTHESAT | V ⁻¹ | 1 | - | - | Geometry independent part | 2 |
| PLTHESAT | V ⁻¹ | 0 | - | - | Length dependence | 2 |
| PWTHESAT | V ⁻¹ | 0 | - | - | Width dependence | 2 |
| PLWTHESAT | V ⁻¹ | 0 | - | - | Length times width dependence | 2 |
| STTHESAT | - | 1 | - | - | Temperature dependence of THESAT | 0 |
| STTHESATO | - | 1 | - | - | Geometry independent temperature dependence | 1 |
| STTHESATL | - | 0 | - | - | Length dependence | 1 |
| STTHESATW | - | 0 | - | - | Width dependence | 1 |
| STTHESATLW | - | 0 | - | - | Area dependence | 1 |
| POSTTHESAT | - | 1 | - | - | Geometry independent part | 2 |
| PLSTTHESAT | - | 0 | - | - | Length dependence | 2 |
| PWSTTHESAT | - | 0 | - | - | Width dependence | 2 |
| PLWSTTHESAT | - | 0 | - | - | Length times width dependence of temperature dependence | 2 |
| THESATB | V ⁻¹ | 0 | -0.5 | - | Back-bias dependence of velocity saturation | 0 |
| THESATBO | V ⁻¹ | 0 | - | - | Geometry independent part | 1 |
| POTHESATB | V ⁻¹ | 0 | - | - | Geometry independent part | 2 |
| PLTHESATB | V ⁻¹ | 0 | - | - | Length dependence | 2 |
| PWTHESATB | V ⁻¹ | 0 | - | - | Width dependence | 2 |
| PLWTHESATB | V ⁻¹ | 0 | - | - | Length times width dependence | 2 |
| THESATG | V ⁻¹ | 0 | -0.5 | - | Gate-bias dependence of velocity saturation | 0 |

| Name | Unit | Default | Min. | Max. | Description | SWGEO ¹ |
|------------|-----------------|---------|------|------|-------------------------------|--------------------|
| THESATGO | V ⁻¹ | 0 | - | - | Geometry independent part | 1 |
| THESATGO | V ⁻¹ | 0 | - | - | Geometry independent part | 2 |
| PLTHESATG | V ⁻¹ | 0 | - | - | Length dependence | 2 |
| PWTHESATG | V ⁻¹ | 0 | - | - | Width dependence | 2 |
| PLWTHESATG | V ⁻¹ | 0 | - | - | Length times width dependence | 2 |

1. Indicates for which value of SWGEO the listed parameter is used.

PSP 103.1 Model — Saturation Voltage Parameters

| Name | Unit | Default | Min. | Max. | Description | SWGEO ¹ |
|-------|------|---------|------|------|-------------------------------------|--------------------|
| AX | - | 3 | 2 | - | Linear/saturation transition factor | 0 |
| AXO | - | 18 | - | - | Geometry independent | 1 |
| AXL | - | 0.4 | 0 | - | Length dependence | 1 |
| POAX | - | 3 | - | - | Geometry independent part | 2 |
| PLAX | - | 0 | - | - | Length dependence | 2 |
| PWAX | - | 0 | - | - | Width dependence | 2 |
| PLWAX | - | 0 | - | - | Length times width dependence | 2 |

1. Indicates for which value of SWGEO the listed parameter is used.

PSP 103.1 Model — Channel Length Modulation (CLM) Parameters

| Name | Unit | Default | Min. | Max. | Description | SWGEO ¹ |
|---------|------|-------------------|------|------|--------------------------------|--------------------|
| ALP | - | 0.01 | 0 | - | CLM pre-factor | 0 |
| ALPL | - | $5 \cdot 10^{-4}$ | - | - | Length dependence | 1 |
| ALPLEXP | - | 1 | - | - | Exponent for length dependence | 1 |
| ALPW | - | 0 | - | - | Width dependence | 1 |

Chapter 2: MOSFET Models

LEVEL 69: PSP Model

| Name | Unit | Default | Min. | Max. | Description | SWGEO ¹ |
|----------|-----------------|---------|------|------|--|--------------------|
| POALP | - | 0.01 | - | - | Geometry independent part | 2 |
| PLALP | - | 0 | - | - | Length dependence | 2 |
| PWALP | - | 0 | - | - | Width dependence | 2 |
| PLWALP | - | 0 | - | - | Length times width dependence | 2 |
| ALP1 | V | 0 | 0 | - | CLM enhancement factor above threshold | 0 |
| ALP1L1 | V | 0 | - | - | Length dependence | 1 |
| ALP1LEXP | - | 0.5 | - | - | Exponent for length dependence | 1 |
| ALP1L2 | - | 0 | 0 | - | Second order length dependence | 1 |
| ALP1W | - | 0 | 0 | - | Width dependence | 1 |
| POALP1 | V | 0 | 0 | - | Geometry independent part | 2 |
| PLALP1 | V | 0 | 0 | - | Length dependence | 2 |
| PWALP1 | V | 0 | 0 | - | Width dependence | 2 |
| PLWALP1 | V | 0 | - | - | Length times width dependence | 2 |
| ALP2 | V ⁻¹ | 0 | 0 | - | CLM enhancement factor below threshold | 0 |
| ALP2L1 | V | 0 | - | - | Length dependence | 1 |
| ALP2LEXP | - | 0.5 | - | - | Exponent for length dependence | 1 |
| ALP2L2 | - | 0 | 0 | - | Second order length dependence | 1 |
| ALP2W | - | 0 | - | - | Width dependence | 1 |
| POALP2 | V ⁻¹ | 0 | - | - | Geometry independent part | 2 |
| PLALP2 | V ⁻¹ | 0 | - | - | Length dependence | 2 |
| PWALP2 | V ⁻¹ | 0 | - | - | Width dependence | 2 |
| PLWALP2 | V ⁻¹ | 0 | - | - | Length times width dependence | 2 |

| Name | Unit | Default | Min. | Max. | Description | SWGEO ¹ |
|------|------|---------|------------|------|--------------------------------------|--------------------|
| VP | V | 0.05 | 10^{-10} | - | CLM logarithmic dependence parameter | 0 |
| VPO | V | 0.05 | - | - | Geometry independent part | 1 |
| POVP | V | 0.05 | - | - | Geometry independent part | 2 |

1. Indicates for which value of SWGEO the listed parameter is used.

PSP 103.1 Model — Impact Ionization (II) Parameters

| Name | Unit | Default | Min. | Max. | Description | SWGEO ¹ |
|--------|------|---------|------|------|-------------------------------------|--------------------|
| A1 | - | 1 | 0 | - | Impact-ionization pre-factor | 0 |
| A1O | - | 1 | | - | Geometry independent part | 1 |
| A1L | - | 0 | | - | Length dependence | 1 |
| A1W | - | 0 | | - | Width dependence | 1 |
| POA1 | - | 1 | | - | Geometry independent part | 2 |
| PLA1 | - | 0 | | - | Length dependence | 2 |
| PWA1 | - | 0 | | - | Width dependence | 2 |
| PLWA1 | - | 0 | | - | Length times width dependence | 2 |
| A2 | V | 10 | 0 | - | Impact-ionization exponent at TR | 0 |
| A2O | V | 10 | - | - | Geometry independent part | 1 |
| POA2 | V | 10 | - | - | Geometry independent part | 2 |
| STA2 | V | 0 | - | - | Temperature dependence of A2 | 0 |
| STA2O | V | 0 | - | - | Geometry independent part | 1 |
| POSTA2 | V | 0 | - | - | Geometry independent part | 2 |
| A3 | - | 1 | 0 | - | Saturation-voltage dependence of II | 0 |
| A3O | - | 1 | - | - | Geometry independent part | 1 |
| A3L | - | 0 | - | - | Length dependence | 1 |

Chapter 2: MOSFET Models

LEVEL 69: PSP Model

| Name | Unit | Default | Min. | Max. | Description | SWGEO ¹ |
|-------|-------------------|---------|------|------|-------------------------------|--------------------|
| A3W | - | 0 | - | - | Width dependence | 1 |
| POA3 | - | 1 | - | - | Geometry independent part | 2 |
| PLA3 | - | 0 | - | - | Length dependence | 2 |
| PWA3 | - | 0 | - | - | Width dependence | 2 |
| PLWA3 | - | 0 | - | - | Length times width dependence | 2 |
| A4 | V ^{-1/2} | 0 | 0 | - | Back-bias dependence of II | 0 |
| A4O | V ^{-1/2} | 0 | - | - | Geometry independent part | 1 |
| A4L | - | 0 | - | - | Length dependence | 1 |
| A4W | - | 0 | - | - | Width dependence | 1 |
| POA4 | V ^{-1/2} | 0 | - | - | Geometry independent part | 2 |
| PLA4 | V ^{-1/2} | 0 | - | - | Length dependence | 2 |
| PWA4 | V ^{-1/2} | 0 | - | - | Width dependence | 2 |
| PLWA4 | V ^{-1/2} | 0 | - | - | Length times width dependence | 2 |

1. Indicates for which value of SWGEO the listed parameter is used.

PSP 103.1 Model — Gate Current Parameters

| Name | Unit | Default | Min. | Max. | Description | SWGEO ¹ |
|---------|------|---------|------|------|---|--------------------|
| GCO | - | 0 | -10 | 10 | Gate tunnelling energy adjustment | 0 |
| GCOO | - | 0 | - | - | Geometry independent part | 1 |
| POGCO | - | 0 | - | - | Geometry independent part | 2 |
| IGINV | A | 0 | 0 | - | Gate channel current pre-factor | 0 |
| IGINVLW | A | 0 | - | - | Gate channel current pre-factor for a channel area of $W_{EN} \cdot L_{EN}$ | 1 |
| POIGINV | A | 0 | - | - | Geometry independent part | 2 |

| Name | Unit | Default | Min. | Max. | Description | SWGEO ¹ |
|----------|------|-----------------------|------|------|--|--------------------|
| PLIGINV | A | 0 | - | - | Length dependence | 2 |
| PWIGINV | A | 0 | - | - | Width dependence | 2 |
| PLWIGINV | A | 0 | - | - | Length times width dependence | 2 |
| IGOV | A | 0 | 0 | - | Gate overlap current pre-factor | 0 |
| IGOVW | A | 0 | - | - | Gate overlap current pre-factor for a channel width of W_{EN} | 1 |
| POIGOV | A | 0 | - | - | Geometry independent part | 2 |
| PLIGOV | A | 0 | - | - | Length dependence | 2 |
| PWIGOV | A | 0 | - | - | Width dependence | 2 |
| PLWIGOV | A | 0 | - | - | Length times width dependence | 2 |
| IGOVD | A | 0 | 0 | - | Gate overlap current pre-factor for drain side | 0 |
| IGOVDW | A | 0 | - | - | Gate overlap current pre-factor for a channel width of W_{EN} for drain side | 1 |
| POIGOVD | A | 0 | - | - | Geometry independent part | 2 |
| PLIGOVD | A | 0 | - | - | Length dependence | 2 |
| PWIGOVD | A | 0 | - | - | Width dependence | 2 |
| PLWIGOVD | A | 0 | - | - | Length times width dependence | 2 |
| STIG | - | 2 | - | - | Temperature dependence of gate current | 0 |
| STIGO | - | 2 | - | - | Geometry independent part | 1 |
| POSTIG | - | 2 | - | - | Geometry independent part | 2 |
| GC2 | - | 0.375 | 0 | 10 | Gate current slope factor | 0 |
| GC2O | - | 0.375 | - | - | Geometry independent part | 1 |
| POGC2 | - | 3.75×10^{-1} | - | - | Geometry independent part | 2 |
| GC3 | - | 0.063 | -2 | 2 | Gate current curvature factor | 0 |

Chapter 2: MOSFET Models

LEVEL 69: PSP Model

| Name | Unit | Default | Min. | Max. | Description | SWGEO ¹ |
|--------|------|----------------------|------|------|---------------------------|--------------------|
| GC3O | - | 0.063 | - | - | Geometry independent part | 1 |
| POGC3 | - | 6.3×10^{-2} | - | - | Geometry independent part | 2 |
| CHIB | V | 3.1 | 1 | - | Tunnelling barrier height | 0 |
| CHIBO | V | 3.1 | - | - | Geometry independent part | 1 |
| POCHIB | V | 3.1 | - | - | Geometry independent part | 2 |

1. Indicates for which value of SWGEO the listed parameter is used.

PSP 103.1 Model — Gate-Induced Drain Leakage (GIDL) Parameters

| Name | Unit | Default | Min. | Max. | Description | SWGEO ¹ |
|-----------|------------------|---------|------|------|--------------------------------|--------------------|
| AGIDL | A/V ³ | 0 | 0 | - | GIDL pre-factor | 0 |
| AGIDLW | A/V ³ | 0 | - | - | Width dependence | 1 |
| POAGIDL | A/V ³ | 0 | - | - | Geometry independent part | 2 |
| PLAGIDL | A/V ³ | 0 | - | - | Length dependence | 2 |
| PWAGIDL | A/V ³ | 0 | - | - | Width dependence | 2 |
| PLWAGIDL | A/V ³ | 0 | - | - | Length times width dependence | 2 |
| AGIDLD | A/V ³ | 0 | 0 | - | GIDL pre-factor for drain side | 0 |
| AGIDLDW | A/V ³ | 0 | - | - | Width dependence | 1 |
| POAGIDLD | A/V ³ | 0 | - | - | Geometry independent part | 2 |
| PLAGIDLD | A/V ³ | 0 | - | - | Length dependence | 2 |
| PWAGIDLD | A/V ³ | 0 | - | - | Width dependence | 2 |
| PLWAGIDLD | A/V ³ | 0 | - | - | Length times width dependence | 2 |
| BGIDL | V | 41 | 0 | - | GIDL probability factor at TR | 0 |
| BGIDLO | V | 41 | - | - | Geometry independent part | 1 |

| Name | Unit | Default | Min. | Max. | Description | SWGEO ¹ |
|------------|------|---------|------|------|--|--------------------|
| POBGIDL | V | 41 | - | - | Geometry independent part | 2 |
| BGIDLD | V | 41 | 0 | - | GIDL probability factor at TR for drain side | 0 |
| BGIDLDO | V | 41 | - | - | Geometry independent part | 1 |
| POBgidLD | V | 41 | - | - | Geometry independent part | 2 |
| STBGIDL | V/K | 0 | - | - | Temperature dependence of BGIDL | 0 |
| STBGIDLO | V/K | 0 | - | - | Geometry independent part | 1 |
| POSTBGIDL | V/K | 0 | - | - | Geometry independent part | 2 |
| STBGIDLD | V/K | 0 | - | - | Temperature dependence of BGIDL for drain side | 0 |
| STBGIDLDO | V/K | 0 | - | - | Geometry independent part | 1 |
| POSTBGIDLD | V/K | 0 | - | - | Geometry independent part | 2 |
| CGIDL | - | 0 | - | - | Back-bias dependence of GIDL | 0 |
| CGIDLO | - | 0 | - | - | Geometry independent part | 1 |
| POCGIDL | - | 0 | - | - | Geometry independent part | 2 |
| CGIDLD | - | 0 | - | - | Back-bias dependence of GIDL for drain side | 0 |
| CGIDLDO | - | 0 | - | - | Geometry independent part | 1 |
| POCGIDLD | - | 0 | - | - | Geometry independent part | 2 |

1. Indicates for which value of SWGEO the listed parameter is used.

PSP 103.1 Model — Charge Model Parameters

| Name | Unit | Default | Min. | Max. | Description | SWGEO ¹ |
|-------|------|------------|------|------|---|--------------------|
| COX | F | 10^{-14} | 0 | - | Oxide capacitance for intrinsic channel | 0 |
| POCOX | F | 10^{-14} | - | - | Geometry independent part | 2 |
| PLCOX | F | 0 | - | - | Length dependence | 2 |

Chapter 2: MOSFET Models

LEVEL 69: PSP Model

| Name | Unit | Default | Min. | Max. | Description | SWGEO ¹ |
|----------|------|------------|------|------|--|--------------------|
| PWCOX | F | 0 | - | - | Width dependence | 2 |
| PLWCOX | F | 0 | - | - | Length times width dependence | 2 |
| CGOV | F | 10^{-15} | 0 | - | Oxide capacitance for gate–drain/source overlap | 0 |
| POCGOV | F | 10^{-15} | - | - | Geometry independent part | 2 |
| PLCGOV | F | 0 | - | - | Length dependence | 2 |
| PWCGOV | F | 0 | - | - | Width dependence | 2 |
| PLWCGOV | F | 0 | - | - | Length times width dependence | 2 |
| CGOVD | F | 10^{-15} | 0 | - | Oxide capacitance for gate–drain/source overlap for drain side | 0 |
| POCGOVD | F | 10^{-15} | - | - | Geometry independent part | 2 |
| PLCGOVD | F | 0 | - | - | Length dependence | 2 |
| PWCGOVD | F | 0 | - | - | Width dependence | 2 |
| PLWCGOVD | F | 0 | - | - | Length times width dependence | 2 |
| CGBOV | F | 0 | 0 | - | Oxide capacitance for gate–bulk overlap | 0 |
| CGBOVL | F | 0 | - | - | Oxide capacitance for gate–bulk overlap for a channel length of L_{EN} | 1 |
| POCGBOV | F | 0 | - | - | Geometry independent part | 2 |
| PLCGBOV | F | 0 | - | - | Length dependence | 2 |
| PWCGBOV | F | 0 | - | - | Width dependence | 2 |
| PLWCGBOV | F | 0 | - | - | Length times width dependence | 2 |
| CFR | F | 0 | - | - | Outer fringe capacitance | 0 |
| CFRW | F | 0 | 0 | - | Outer fringe capacitance for a channel width of W_{EN} | 1 |
| POCFR | F | 0 | - | - | Geometry independent part | 2 |

| Name | Unit | Default | Min. | Max. | Description | SWGEO ¹ |
|---------|------|---------|------|------|---|--------------------|
| PLCFR | F | 0 | - | - | Length dependence | 2 |
| PWCFR | F | 0 | - | - | Width dependence | 2 |
| PLWCFR | F | 0 | - | - | Length times width dependence | 2 |
| CFRD | F | 0 | 0 | - | Outer fringe capacitance for drain side | 0 |
| CFRDW | F | 0 | - | - | Outer fringe capacitance for a channel width of W_{EN} for drain side | 1 |
| POCFRD | F | 0 | - | - | Geometry independent part | 2 |
| PLCFRD | F | 0 | - | - | Length dependence | 2 |
| PWCFRD | F | 0 | - | - | Width dependence | 2 |
| PLWCFRD | F | 0 | - | - | Length times width dependence | 2 |

1. Indicates for which value of SWGEO the listed parameter is used.

PSP 103.1 Model — Noise Model Parameters

| Name | Unit | Default | Min. | Max. | Description | SWGEO ¹ |
|--------|---------------------------------|--------------------|------|------|--|--------------------|
| FNT | - | 1 | 0 | - | Thermal noise coefficient | 0 |
| FNTO | - | 1 | - | - | Geometry independent part | 1 |
| POFNT | - | 1 | - | - | Geometry independent part | 2 |
| NFA | V ⁻¹ /m ⁴ | 8.10 ²² | 0 | - | First coefficient of flicker noise | 0 |
| NFALW | V ⁻¹ /m ⁴ | 8.10 ²² | - | - | First coefficient of flicker noise for a channel area of $W_{EN} \cdot L_{EN}$ | 1 |
| PONFA | V ⁻¹ /m ⁴ | 8.10 ²² | - | - | Geometry independent part | 2 |
| PLNFA | V ⁻¹ /m ⁴ | 0 | - | - | Length dependence | 2 |
| PWNFA | V ⁻¹ /m ⁴ | 0 | - | - | Width dependence | 2 |
| PLWNFA | V ⁻¹ /m ⁴ | 0 | - | - | Length times width dependence | 2 |
| NFB | V ⁻¹ /m ² | 3.10 ⁷ | 0 | - | Second coefficient of flicker noise | 0 |

Chapter 2: MOSFET Models

LEVEL 69: PSP Model

| Name | Unit | Default | Min. | Max. | Description | SWGEO ¹ |
|---------|---------------------------------|-------------------|------|------|---|--------------------|
| NFBLW | V ⁻¹ /m ² | 3.10 ⁷ | - | - | Second coefficient of flicker noise for a channel area of $W_{EN} \cdot L_{EN}$ | 1 |
| PONFB | V ⁻¹ /m ² | 3.10 ⁷ | - | - | Geometry independent part | 2 |
| PLNFB | V ⁻¹ /m ² | 0 | - | - | Length dependence | 2 |
| PWNFB | V ⁻¹ /m ² | 0 | - | - | Width dependence | 2 |
| PLWNFB | V ⁻¹ /m ² | 0 | - | - | Length times width dependence | 2 |
| NFC | V ⁻¹ | 0 | 0 | - | Third coefficient of flicker noise | 0 |
| NFCLW | V ⁻¹ | 0 | - | - | Third coefficient of flicker noise for a channel area of $W_{EN} \cdot L_{EN}$ | 1 |
| PONFC | V ⁻¹ | 0 | - | - | Geometry independent part | 2 |
| PLNFC | V ⁻¹ | 0 | - | - | Length dependence | 2 |
| PWNFC | V ⁻¹ | 0 | - | - | Width dependence | 2 |
| PLWNFC | V ⁻¹ | 0 | - | - | Length times width dependence | 2 |
| EF | - | 1 | 0 | - | Flicker noise frequency exponent | 0 |
| EFO | - | 1 | - | - | Geometry independent part | 1 |
| POEF | - | 1 | - | - | Geometry independent part | 2 |
| LINTNOI | m | 0 | - | - | Length offset for flicker noise | 1 |
| ALPNOI | - | 2 | - | - | Exponent for length offset | 1 |

1. Indicates for which value of SWGEO the listed parameter is used.

PSP 103.1 Model — Stress Model Parameters

The PSP stress model parameters are derived from BSIM4.40 with as little modifications as possible. Parameter names have been copied, but are subjected to PSP conventions by replacing every zero by an 'O'.

Note: The STK2 and LODK2 parameters are not available in PSP. Except for these changes, stress parameters determined for BSIM can be directly applied in PSP.

The parameters listed in the following table are part of PSP global parameter set (both geometrical and binning).

| Name | Unit | Default | Min. | Max. | Description | SWGEO ¹ |
|---------|-----------------------|-----------|-----------|------|--|--------------------|
| SAREF | m | 10^{-6} | 10^{-9} | - | Reference distance between OD edge to Poly from one side | 1, 2 |
| SBREF | m | 10^{-6} | 10^{-9} | - | Reference distance between OD edge to Poly from other side | 1, 2 |
| WLOD | m | 0 | - | - | Width parameter | 1, 2 |
| KUO | m | 0 | - | - | Mobility degradation/enhancement coefficient | 1, 2 |
| KVSAT | m | 0 | -1 | 1 | Saturation velocity degradation/enhancement parameter | 1, 2 |
| TKUO | - | 0 | - | - | Temperature coefficient of KUO | 1, 2 |
| LKUO | $m^{LLODKUO}$ | 0 | - | - | Length dependence of KUO | 1, 2 |
| WKUO | $m^{WLODKUO}$ | 0 | - | - | Width dependence of KUO | 1, 2 |
| PKUO | $m^{LLODKUO+WLODKUO}$ | 0 | - | - | Cross-term dependence of KUO | 1, 2 |
| LLODKUO | - | 0 | 0 | - | Length parameter for mobility stress effect | 1, 2 |
| WLODKUO | - | 0 | 0 | - | Width parameter for mobility stress effect | 1, 2 |
| KVTHO | Vm | 0 | - | - | Threshold shift parameter | 1, 2 |
| LKVTHO | $m^{LLODVTH}$ | 0 | - | - | Length dependence of KVTHO | 1, 2 |
| WKVTHO | $m^{WLODVTH}$ | 0 | - | - | Width dependence of KVTHO | 1, 2 |
| PKVTHO | $m^{LLODVTH+WLODVTH}$ | 0 | - | - | Cross-term dependence of KVTHO | 1, 2 |
| LLODVTH | - | 0 | 0 | - | Length parameter for threshold voltage stress effect | 1, 2 |
| WLODVTH | - | 0 | 0 | - | Width parameter for threshold voltage stress effect | 1, 2 |
| STETAO | m | 0 | - | - | ETAO shift factor related to threshold voltage change | 1, 2 |

Chapter 2: MOSFET Models

LEVEL 69: PSP Model

| Name | Unit | Default | Min. | Max. | Description | SWGEO ¹ |
|---------|------|---------|------|------|--------------------------------|--------------------|
| LODETAO | - | 1 | 0 | - | ETAO shift modification factor | 1, 2 |

1. *Indicates for which value of SWGEO the listed parameter is used.*

PSP 103.1 Model — Well Proximity Effect (WPE) Model Parameters

The PSP WPE model parameters are derived from BSIM4.5.0 with as little modifications as possible. Parameter names have been copied, but are subjected to PSP conventions by replacing every zero by an ‘O’.

Note: The K2WE parameter are not available in PSP. Except for these changes, stress parameters determined for BSIM can be directly applied in PSP.

The parameters listed in the following table have both geometrical and binning rules included. You can use one of the following parameter sets depending on which scaling rule is selected.

| Name | Unit | Default | Min. | Max. | Description | SWGEO ¹ |
|------------|------|--------------------|------|------|--|--------------------|
| SCREF | m | 1.10 ⁻⁶ | 0 | - | Distance between OD-edge and well edge of a reference device | 1, 2 |
| WEB | - | 0 | - | - | Coefficient for SCB | 1, 2 |
| WEC | - | 0 | - | - | Coefficient for SCC | 1, 2 |
| KVTHOWEO | - | 0 | - | - | Geometry independent threshold shift parameter | 1 |
| KVTHOWEL | - | 0 | - | - | Length dependence | 1 |
| KVTHOWEW | - | 0 | - | - | Width dependence | 1 |
| KVTHOWELW | - | 0 | - | - | Area dependence | 1 |
| POKVTHOWE | - | 0 | - | - | Geometry independent part of threshold shift parameter | 2 |
| PLKVTHOWE | - | 0 | - | - | Length dependence | 2 |
| PWKVTHOWE | - | 0 | - | - | Width dependence | 2 |
| PLWKVTHOWE | - | 0 | - | - | Length times width dependence | 2 |

| Name | Unit | Default | Min. | Max. | Description | SWGEO ¹ |
|----------|------|---------|------|------|--|--------------------|
| KUOWEO | - | 0 | - | - | Geometry independent mobility degradation factor | 1 |
| KUOWEL | - | 0 | - | - | Length dependence | 1 |
| KUOWEW | - | 0 | - | - | Width dependence | 1 |
| KUOWELW | - | 0 | - | - | Area dependence | 1 |
| POKUOWE | - | 0 | - | - | Geometry independent part of mobility degradation factor | 2 |
| PLKUOWE | - | 0 | - | - | Length dependence | 2 |
| PWKUOWE | - | 0 | - | - | Width dependence | 2 |
| PLWKUOWE | - | 0 | - | - | Length times width dependence | 2 |

1. Indicates for which value of SWGEO the listed parameter is used.

PSP 103.1 Model — Source-bulk and Drain-bulk Junction Model Parameters

The PSP JUNCAP2 model parameters are part of both the global and the local parameter sets. You can use one of the following parameter sets depending on which scaling rule is selected:

| Name | Unit | Default | Min. | Max. | Description | SWJUNASYM ¹ |
|----------|------|---------|-------------------|------|---|------------------------|
| TRJ | °C | 21 | T _{min} | - | Reference temperature | 0, 1 |
| SWJUNEXP | - | 0 | 0 | 1 | Flag for JUNCAP2 Express; 0: full JUNCAP2 model, 1: Express model | 0, 1 |
| IMAX | A | 1000 | 10 ⁻¹² | - | Maximum current up to which forward current behaves exponentially | 0, 1 |

Capacitance Parameters

| | | | | | | |
|---------|------------------|------------------|-------------------|---|---|------|
| CJORBOT | F/m ² | 10 ⁻³ | 10 ⁻¹² | - | Zero-bias capacitance per unit-of-area of bottom component for source-bulk junction | 0, 1 |
| CJORSTI | F/m | 10 ⁻⁹ | 10 ⁻¹⁸ | - | Zero-bias capacitance per unit-of-length of STI-edge component for source-bulk junction | 0, 1 |

Chapter 2: MOSFET Models

LEVEL 69: PSP Model

| Name | Unit | Default | Min. | Max. | Description | SWJUNASYM ¹ |
|----------|------------------|-----------|--------------|------|---|------------------------|
| CJORGAT | F/m | 10^{-9} | 10^{-18} | - | Zero-bias capacitance per unit-of-length of gate-edge component for source-bulk junction | 0, 1 |
| VBIRBOT | V | 1 | $V_{bi,low}$ | - | Built-in voltage at the reference temperature of bottom component for source-bulk junction | 0, 1 |
| VBIRSTI | V | 1 | $V_{bi,low}$ | - | Built-in voltage at the reference temperature of STI-edge component for source-bulk junction | 0, 1 |
| VBIRGAT | V | 1 | $V_{bi,low}$ | - | Built-in voltage at the reference temperature of gate-edge component for source-bulk junction | 0, 1 |
| PBOT | - | 0.5 | 0.05 | 0.95 | Grading coefficient of bottom component for source-bulk junction | 0, 1 |
| PSTI | - | 0.5 | 0.05 | 0.95 | Grading coefficient of STI-edge component for source-bulk junction | 0, 1 |
| PGAT | - | 0.5 | 0.05 | 0.95 | Grading coefficient of gate-edge component for source-bulk junction | 0, 1 |
| CJORBOTD | F/m ² | 10^{-3} | 10^{-12} | - | Zero-bias capacitance per unit-of-area of bottom component for drain-bulk junction | 1 |
| CJORSTID | F/m | 10^{-9} | 10^{-18} | - | Zero-bias capacitance per unit-of-length of STI-edge component for drain-bulk junction | 1 |
| CJORGATD | F/m | 10^{-9} | 10^{-18} | - | Zero-bias capacitance per unit-of-length of gate-edge component for drain-bulk junction | 1 |
| VBIRBOTD | V | 1 | $V_{bi,low}$ | - | Built-in voltage at the reference temperature of bottom component for drain-bulk junction | 1 |
| VBIRSTID | V | 1 | $V_{bi,low}$ | - | Built-in voltage at the reference temperature of STI-edge component for drain-bulk junction | 1 |
| VBIRGATD | V | 1 | $V_{bi,low}$ | - | Built-in voltage at the reference temperature of gate-edge component for drain-bulk junction | 1 |

| Name | Unit | Default | Min. | Max. | Description | SWJUNASYM ¹ |
|---------------------------------|------------------|-------------------|------|------|---|------------------------|
| PBOTD | - | 0.5 | 0.05 | 0.95 | Grading coefficient of bottom component for drain-bulk junction | 1 |
| PSTID | - | 0.5 | 0.05 | 0.95 | Grading coefficient of STI-edge component for drain-bulk junction | 1 |
| PGATD | - | 0.5 | 0.05 | 0.95 | Grading coefficient of gate-edge component for drain-bulk junction | 1 |
| Ideal-Current Parameters | | | | | | |
| PHIGBOT | V | 1.16 | - | - | Zero-temperature band-gap voltage of bottom component for source-bulk junction | 0, 1 |
| PHIGSTI | V | 1.16 | - | - | Zero-temperature band-gap voltage of STI-edge component for source-bulk junction | 0, 1 |
| PHIGGAT | V | 1.16 | - | - | Zero-temperature band-gap voltage of gate-edge component for source-bulk junction | 0, 1 |
| IDSATRBOT | A/m ² | 10 ⁻¹² | 0 | - | Saturation current density at the reference temperature of bottom component for source-bulk junction | 0, 1 |
| IDSATRSTI | A/m | 10 ⁻¹⁸ | 0 | - | Saturation current density at the reference temperature of STI-edge component for source-bulk junction | 0, 1 |
| IDSATRGAT | A/m | 10 ⁻¹⁸ | 0 | - | Saturation current density at the reference temperature of gate-edge component for source-bulk junction | 0, 1 |
| PHIGBOTD | V | 1.16 | - | - | Zero-temperature band-gap voltage of bottom component for drain-bulk junction | 1 |
| PHIGSTID | V | 1.16 | - | - | Zero-temperature band-gap voltage of STI-edge component for drain-bulk junction | 1 |
| PHIGGATD | V | 1.16 | - | - | Zero-temperature band-gap voltage of gate-edge component for drain-bulk junction | 1 |
| IDSATRBOTD | A/m ² | 10 ⁻¹² | 0 | - | Saturation current density at the reference temperature of bottom component for drain-bulk junction | 1 |

Chapter 2: MOSFET Models

LEVEL 69: PSP Model

| Name | Unit | Default | Min. | Max. | Description | SWJUNASYM ¹ |
|--------------------------------------|------------------|------------|-----------|------|--|------------------------|
| IDSATRSTID | A/m | 10^{-18} | 0 | - | Saturation current density at the reference temperature of STI-edge component for drain-bulk junction | 1 |
| IDSATRGATD | A/m | 10^{-18} | 0 | - | Saturation current density at the reference temperature of gate-edge component for drain-bulk junction | 1 |
| Shockley-Read-Hall Parameters | | | | | | |
| CSRHBOT | A/m ³ | 10^2 | 0 | - | Shockley-Read-Hall pre-factor of bottom component for source-bulk junction | 0, 1 |
| CSRHSTI | A/m ² | 10^{-4} | 0 | - | Shockley-Read-Hall pre-factor of STI-edge component for source-bulk junction | 0, 1 |
| CSRHGAT | A/m ² | 10^{-4} | 0 | - | Shockley-Read-Hall pre-factor of gate-edge component for source-bulk junction | 0, 1 |
| XJUNSTI | m | 10^{-7} | 10^{-9} | - | Junction depth of STI-edge component for source-bulk junction | 0, 1 |
| XJUNGAT | m | 10^{-7} | 10^{-9} | - | Junction depth of gate-edge component for source-bulk junction | 0, 1 |
| CSRHBOTD | A/m ³ | 10^2 | 0 | - | Shockley-Read-Hall pre-factor of bottom component for drain-bulk junction | 1 |
| CSRHSTD | A/m ² | 10^{-4} | 0 | - | Shockley-Read-Hall pre-factor of STI-edge component for drain-bulk junction | 1 |
| CSRHGATD | A/m ² | 10^{-4} | 0 | - | Shockley-Read-Hall pre-factor of gate-edge component for drain-bulk junction | 1 |
| XJUNSTID | m | 10^{-7} | 10^{-9} | - | Junction depth of STI-edge component for drain-bulk junction | 1 |
| XJUNGATD | m | 10^{-7} | 10^{-9} | - | Junction depth of gate-edge component for drain-bulk junction | 1 |

Trap-assisted Tunneling Parameters

| Name | Unit | Default | Min. | Max. | Description | SWJUNASYM ¹ |
|-------------|------------------|------------------|------|------|---|------------------------|
| CTATBOT | A/m ³ | 10 ² | 0 | - | Trap-assisted tunneling pre-factor of bottom component for source-bulk junction | 0, 1 |
| CTATSTI | A/m ² | 10 ⁻⁴ | 0 | - | Trap-assisted tunneling pre-factor of STI-edge component for source-bulk junction | 0, 1 |
| CTATGAT | A/m ² | 10 ⁻⁴ | 0 | - | Trap-assisted tunneling pre-factor of gate-edge component for source-bulk junction | 0, 1 |
| MEFFTATBOT | - | 0.25 | 0.01 | - | Effective mass (in units of m_0) for trap-assisted tunneling of bottom component for source-bulk junction | 0, 1 |
| MEFFTATSTI | - | 0.25 | 0.01 | - | Effective mass (in units of m_0) for trap-assisted tunneling of STI-edge component for source-bulk junction | 0, 1 |
| MEFFTATGAT | - | 0.25 | 0.01 | - | Effective mass (in units of m_0) for trap-assisted tunneling of gate-edge component for source-bulk junction | 0, 1 |
| CTATBOTD | A/m ³ | 10 ² | 0 | - | Trap-assisted tunneling pre-factor of bottom component for drain-bulk junction | 1 |
| CTATSTID | A/m ² | 10 ⁻⁴ | 0 | - | Trap-assisted tunneling pre-factor of STI-edge component for drain-bulk junction | 1 |
| CTATGATD | A/m ² | 10 ⁻⁴ | 0 | - | Trap-assisted tunneling pre-factor of gate-edge component for drain-bulk junction | 1 |
| MEFFTATBOTD | - | 0.25 | 0.01 | - | Effective mass (in units of m_0) for trap-assisted tunneling of bottom component for drain-bulk junction | 1 |
| MEFFTATSTID | - | 0.25 | 0.01 | - | Effective mass (in units of m_0) for trap-assisted tunneling of STI-edge component for drain-bulk junction | 1 |
| MEFFTATGATD | - | 0.25 | 0.01 | - | Effective mass (in units of m_0) for trap-assisted tunneling of gate-edge component for drain-bulk junction | 1 |

Band-to-band Tunneling Parameters

Chapter 2: MOSFET Models

LEVEL 69: PSP Model

| Name | Unit | Default | Min. | Max. | Description | SWJUNASYM ¹ |
|-----------|--------------------|-------------------|------|------|---|------------------------|
| CBBTBOT | AV ⁻³ | 10 ⁻¹² | 0 | - | Band-to-band tunneling prefactor of bottom component for source-bulk junction | 0, 1 |
| CBBTSTI | AV ⁻³ m | 10 ⁻¹⁸ | 0 | - | Band-to-band tunneling prefactor of STI-edge component for source-bulk junction | 0, 1 |
| CBBTGAT | AV ⁻³ m | 10 ⁻¹⁸ | 0 | - | Band-to-band tunneling prefactor of gate-edge component for source-bulk junction | 0, 1 |
| FBBTRBOT | Vm ⁻¹ | 10 ⁹ | - | - | Normalization field at the reference temperature for band-to-band tunneling of bottom component for source-bulk junction | 0, 1 |
| FBBTRSTI | Vm ⁻¹ | 10 ⁹ | - | - | Normalization field at the reference temperature for band-to-band tunneling of STI-edge component for source-bulk junction | 0, 1 |
| FBBTRGAT | Vm ⁻¹ | 10 ⁹ | - | - | Normalization field at the reference temperature for band-to-band tunneling of gate-edge component for source-bulk junction | 0, 1 |
| STFBBTBOT | K ⁻¹ | -10 ⁻³ | - | - | Temperature scaling parameter for band-to-band tunneling of bottom component for source-bulk junction | 0, 1 |
| STFBBTSTI | K ⁻¹ | -10 ⁻³ | - | - | Temperature scaling parameter for band-to-band tunneling of STI-edge component for source-bulk junction | 0, 1 |
| STFBBTGAT | K ⁻¹ | -10 ⁻³ | - | - | Temperature scaling parameter for band-to-band tunneling of gate-edge component for source-bulk junction | 0, 1 |
| CBBTBOD | AV ⁻³ | 10 ⁻¹² | 0 | - | Band-to-band tunneling prefactor of bottom component for drain-bulk junction | 1 |
| CBBTSTD | AV ⁻³ m | 10 ⁻¹⁸ | 0 | - | Band-to-band tunneling prefactor of STI-edge component for drain-bulk junction | 1 |
| CBBTGATD | AV ⁻³ m | 10 ⁻¹⁸ | 0 | - | Band-to-band tunneling prefactor of gate-edge component for drain-bulk junction | 1 |

| Name | Unit | Default | Min. | Max. | Description | SWJUNASYM ¹ |
|------------|------------------|-------------------|------|------|--|------------------------|
| FBBTRBOTD | Vm ⁻¹ | 10 ⁹ | - | - | Normalization field at the reference temperature for band-to-band tunneling of bottom component for drain-bulk junction | 1 |
| FBBTRSTID | Vm ⁻¹ | 10 ⁹ | - | - | Normalization field at the reference temperature for band-to-band tunneling of STI-edge component for drain-bulk junction | 1 |
| FBBTRGATD | Vm ⁻¹ | 10 ⁹ | - | - | Normalization field at the reference temperature for band-to-band tunneling of gate-edge component for drain-bulk junction | 1 |
| STFBBTBOTD | K ⁻¹ | -10 ⁻³ | - | - | Temperature scaling parameter for band-to-band tunneling of bottom component for drain-bulk junction | 1 |
| STFBBTSTID | K ⁻¹ | -10 ⁻³ | - | - | Temperature scaling parameter for band-to-band tunneling of STI-edge component for drain-bulk junction | 1 |
| STFBBTGATD | K ⁻¹ | -10 ⁻³ | - | - | Temperature scaling parameter for band-to-band tunneling of gate-edge component for drain-bulk junction | 1 |

Avalanche and Breakdown Parameters

| | | | | | | |
|--------|---|----|-----|---|--|------|
| VBRBOT | V | 10 | 0.1 | - | Breakdown voltage of bottom component for source-bulk junction | 0, 1 |
| VBRSTI | V | 10 | 0.1 | - | Breakdown voltage of STI-edge component for source-bulk junction | 0, 1 |
| VBRGAT | V | 10 | 0.1 | - | Breakdown voltage of gate-edge component for source-bulk junction | 0, 1 |
| PBRBOT | V | 4 | 0.1 | - | Breakdown onset tuning parameter of bottom component for source-bulk junction | 0, 1 |
| PBRSTI | V | 4 | 0.1 | - | Breakdown onset tuning parameter of STI-edge component for source-bulk junction | 0, 1 |
| PBRGAT | V | 4 | 0.1 | - | Breakdown onset tuning parameter of gate-edge component for source-bulk junction | 0, 1 |

Chapter 2: MOSFET Models

LEVEL 69: PSP Model

| Name | Unit | Default | Min. | Max. | Description | SWJUNASYM ¹ |
|----------------------------------|------|---------|------|------|--|------------------------|
| VBRBOTD | V | 10 | 0.1 | - | Breakdown voltage of bottom component for drain-bulk junction | 1 |
| VBRSTID | V | 10 | 0.1 | - | Breakdown voltage of STI-edge component for drain-bulk junction | 1 |
| VBRGATD | V | 10 | 0.1 | - | Breakdown voltage of gate-edge component for drain-bulk junction | 1 |
| PBRBOTD | V | 4 | 0.1 | - | Breakdown onset tuning parameter of bottom component for drain-bulk junction | 1 |
| PBRSTID | V | 4 | 0.1 | - | Breakdown onset tuning parameter of STI-edge component for drain-bulk junction | 1 |
| PBRGATD | V | 4 | 0.1 | - | Breakdown onset tuning parameter of gate-edge component for drain-bulk junction | 1 |
| JUNCAP Express Parameters | | | | | | |
| VJUNREF | V | 2.5 | 0.5 | - | Typical maximum source-bulk junction voltage; usually about $2 \cdot V_{\text{sup}}$ | 0, 1 |
| FJUNQ | V | 0.03 | 0 | - | Fraction below which source-bulk junction capacitance components are neglected | 0, 1 |
| VJUNREFD | V | 2.5 | 0.5 | - | Typical maximum drain-bulk junction voltage; usually about $2 \cdot V_{\text{sup}}$ | 1 |
| FJUNQD | V | 0.03 | 0 | - | Fraction below which drain-bulk junction capacitance components are neglected | 1 |

1. Indicates for which value of SWJUNASYM the listed parameter is used.

PSP 103.1 Model — Parasitic Resistance Model Parameters

| Name | Unit | Default | Min. | Max. | Description | SWGEO ¹ |
|------|----------|---------|------|------|-----------------------------------|--------------------|
| RG | Ω | 0 | 0 | - | Gate resistance R_{gate} | 0 |
| RGO | Ω | 0 | - | - | Gate resistance R_{gate} | 1, 2 |

| Name | Unit | Default | Min. | Max. | Description | SWGEO ¹ |
|--------|--------------------|---------|------|------|--|--------------------|
| RINT | $\Omega \cdot m^2$ | 0 | 0 | - | Contact resistance between silicide and poly | 1, 2 |
| RVPOLY | $\Omega \cdot m^2$ | 0 | 0 | - | Vertical poly resistance | 1, 2 |
| RSHG | Ω / \square | 0 | 0 | - | Gate electrode diffusion sheet resistance | 1, 2 |
| DLSIL | m | 0 | - | - | Silicide extension over the physical gate length | 1, 2 |
| RSE | Ω | 0 | 0 | - | External source resistance | 0 |
| RDE | Ω | 0 | 0 | - | External drain resistance | 0 |
| RSH | Ω / \square | 0 | - | - | Sheet resistance of source diffusion | 1, 2 |
| RSHD | Ω / \square | 0 | - | - | Sheet resistance of drain diffusion | 1, 2 |
| RBULK | Ω | 0 | 0 | - | Bulk resistance R_{bulk} | 0 |
| RBULKO | Ω | 0 | - | - | Bulk resistance R_{bulk} | 1, 2 |
| RWELL | Ω | 0 | 0 | - | Well resistance R_{well} | 0 |
| RWELLO | Ω | 0 | - | - | Well resistance R_{well} | 1, 2 |
| RJUNS | Ω | 0 | 0 | - | Source-side bulk resistance R_{juns} | 0 |
| RJUNSO | Ω | 0 | - | - | Source-side bulk resistance R_{juns} | 1, 2 |
| RJUND | Ω | 0 | 0 | - | Drain-side bulk resistance R_{jund} | 0 |
| RJUNDO | Ω | 0 | - | - | Drain-side bulk resistance R_{jund} | 1, 2 |

1. Indicates for which value of SWGEO the listed parameter is used.

PSP 103.1 Model — NQS Model Parameters

| Name | Unit | Default | Min. | Max. | Description | SWGEO ¹ |
|-------|------|---------|------|------|---|--------------------|
| SWNQS | - | 0 | 0 | 9 | Switch for NQS effects / number of collocation points | 0, 1, 2 |
| MUNQS | - | 1 | 0 | - | Relative mobility for NQS modeling | 0 |

Chapter 2: MOSFET Models

LEVEL 69: PSP Model

| Name | Unit | Default | Min. | Max. | Description | SWGEO ¹ |
|--------|------|---------|------|------|------------------------------------|--------------------|
| MUNQSO | - | 1 | - | - | Relative mobility for NQS modeling | 1, 2 |

1. Indicates for which value of SWGEO the listed parameter is used.

PSP 103.1 Instance Parameters

| Name | Unit | Default | Min. | Max. | Description | SWGEO ¹ |
|----------|-------|-------------|-----------|------|---|--------------------|
| L | m | 10^{-6} | 10^{-9} | - | Drawn channel length | 1, 2 |
| W | m | 10^{-6} | 10^{-9} | - | Drawn channel width (total width) | 1, 2 |
| ABSOURCE | m^2 | 10^{-12} | 0 | - | Source junction area | 0, 1, 2 |
| LSSOURCE | m | 10^{-6} | 0 | - | STI-edge part of source junction perimeter | 0, 1, 2 |
| LGSOURCE | m | 10^{-6} | 0 | - | Gate-edge part of source junction perimeter | 0, 1, 2 |
| ABDRAIN | m^2 | 10^{-12} | 0 | - | Drain junction area | 0, 1, 2 |
| LSDRAIN | m | 10^{-6} | 0 | - | STI-edge part of drain junction perimeter | 0, 1, 2 |
| LGDRAIN | m | 10^{-6} | 0 | - | Gate-edge part of drain junction perimeter | 0, 1, 2 |
| AS | m^2 | 10^{-12} | 0 | - | Source junction area (alternative spec.) | 0, 1, 2 |
| PS | m | 10^{-6} | 0 | - | Source STI-edge perimeter (alternative spec.) | 0, 1, 2 |
| AD | m^2 | 10^{-12} | 0 | - | Drain junction area (alternative spec.) | 0, 1, 2 |
| PD | m | 10^{-6} | 0 | - | Drain STI-edge perimeter (alternative spec.) | 0, 1, 2 |
| JW | m | 1.10^{-6} | 0 | - | Junction width | 0 |
| DELVTO | V | 0 | - | - | Threshold voltage shift parameter | 0, 1, 2 |
| FACTUO | - | 1 | 0 | - | Zero-field mobility pre-factor | 0, 1, 2 |

| Name | Unit | Default | Min. | Max. | Description | SWGEO ¹ |
|-------|------|-----------|------|------|--|--------------------|
| SA | m | 0 | - | - | Distance between OD-edge and poly at source side | 1, 2 |
| SB | m | 0 | - | - | Distance between OD-edge and poly at drain side | 1, 2 |
| SD | m | 0 | - | - | Distance between neighboring fingers | 1, 2 |
| SCA | - | 0 | 0 | - | Integral of the first distribution function for scattered well dopant | 1, 2 |
| SCB | - | 0 | 0 | - | Integral of the second distribution function for scattered well dopant | 1, 2 |
| SCC | - | 0 | 0 | - | Integral of the third distribution function for scattered well dopant | 1, 2 |
| SC | m | 0 | - | - | Distance between OD edge and nearest well edge | 1, 2 |
| NRS | - | 0 | - | - | Number of squares of source diffusion | 1, 2 |
| NRD | - | 0 | - | - | Number of squares of drain diffusion | 1, 2 |
| NGCON | - | 1 | 1 | 2 | Number of gate contacts | 1, 2 |
| XGW | m | 10^{-7} | - | - | Distance from the gate contact to the channel edge | 1, 2 |
| NF | - | 1 | 1 | - | Number of fingers; internally rounded to the nearest integer | 1, 2 |
| MULT | - | 1 | 0 | - | Number of devices in parallel | 0, 1, 2 |

1. Indicates for which value of SWGEO the listed parameter is used.

PSP Model — Output Templates

The following output templates (and recommended templates) are available for use with PSP models. See also: [Additional Output Templates for PSP and Other Models](#).

| Name | Alias |
|-----------------|-------|
| Channel current | LX4 |

Chapter 2: MOSFET Models

LEVEL 69: PSP Model

| Name | Alias |
|----------------------|--|
| Diode current | LX5, LX6 |
| Junction capacitance | LX28, LX29 |
| I_{dd} | LX69 |
| I_{gidl} | LX70 |
| W_{eff}/L_{eff} | LX62, LX63 |
| Capacitance | LX82~LX87 (recommended, since they include intrinsic, overlap, and fringe capacitances), LX18~LX23 |

LEVEL 70: BSIMSOI4 Model

The UC Berkeley SOI model (BSIM SOI 4.0) addresses several issues in modeling sub-0.13 micron CMOS/SOI high-speed and RF circuit simulations. Many inputs from the Compact Model Council (CMC) meetings were incorporated into the model. This model is fully backward compatible with its previous 3.X versions. For a description of this model, see the *BSIMSOI4.0 MOSFET Model User's Manual* at http://www-device.eecs.berkeley.edu/bsim/?page=BSIMSOI_LR

The BSIMSOI4 model provides the following major improvements and additions over the BSIMSOIv3.2 model:

- A scalable stress effect model for process induced stress effect; device performance thus becomes a function of the active area geometry and the location of the device in the active area.
- An asymmetric current/capacitance model S/D diode and asymmetric S/D resistance.
- An improved GIDL model with BSIM4 GIDL compatibility.
- Noise model improvements, such as:
 - Improved width/length dependence on flicker noise
 - SPICE2 thermal noise model is introduced as `TNOIMOD=2` with parameter `NTNOI` that adjusts the magnitude of the noise density
 - Body contact resistance induced thermal noise
 - Thermal noise induced by the body resistance network
 - Shot noises induced by `Ibs` and `Ibd` separated
- A two resistance body resistance network introduced for RF simulation.
- Threshold voltage model enhancement, such as:
 - Long-channel DIBL effect model added
 - Channel-length dependence of body effect improved
- Drain-induced threshold shift (DITS) model introduced in output conductance.
- Improved model accuracy in moderate inversion region with BSIM4 compatible `Vgsteff`.
- Multi-finger device with instance parameter `NF`.

Chapter 2: MOSFET Models

LEVEL 70: BSIMSOI4 Model

- A new instance parameter `AGBCPD` to improve gate current for body contact.
- A new instance parameter `DELVTO` representing threshold voltage variation.
- Instance `FRBODY` is both an instance and a model parameter.

The following sections discuss these topics:

- [BSIMSOI4 Model — General Syntax](#)
- [BSIMSOI4 Model Parameters](#)
- [BSIMSOI4 Model — Parameter Range Limit](#)
- [BSIMSOI4 Model — Version Updates](#)

BSIMSOI4 Model — General Syntax

Syntax:

```
MXXX nd ng ns ne [np] [nb] [nT] mname [L=val] [W=val]
+ [M=val] [AD=val] [AS=val] [PD=val] [PS=val] [NRD=val]
+ [NRS=val] [NRB=val] [RTH0=val] [CTH0=val] [NBC=val]
+ [NSEG=val] [PDBCP=val] [PSBCP=val] [AGBCP=val] [AEBCP=val]
+ [VBSUSR=val] [DELTOX=val] [TNODEOUT] [off] [FRBODY=val]
+ [BJTOFF=val] [IC=vds, vgs, vbs, ves, vps] [dtemp=val]
+ [soimod=val] [rgatemod=val] [nf=val] [sa=val] [sb=val]
+ [sd=val] [rbdb=val] [rbsb=val] [delvto=val] [agbcpd=val]
+ [rbodymod=val] [mulu0=val] [SOIQ0=val]
+ [DELSVAT=val] [MULSVAT=val]
```

BSIMSOI4 Model Parameters

This section covers the following topics:

- [BSIMSOI4 Model — General Parameters](#)
- [BSIMSOI4 Model — Control Parameters](#)
- [BSIMSOI4 Model — Process Parameters](#)
- [BSIMSOI4 Model — DC Parameters](#)
- [BSIMSOI4 Model — Gate-to-body Tunneling Parameters](#)
- [BSIMSOI4 Model — AC and Capacitance Parameters](#)
- [BSIMSOI4 Model — Temperature Parameters](#)

- [BSIMSOI4 Model — Built-in Potential Lowering Model Parameters](#)
- [BSIMSOI4 Model — RF Model Parameters](#)
- [BSIMSOI4 Model — Noise Model Parameters](#)
- [BSIMSOI4 Model — Stress Model Parameters](#)

BSIMSOI4 Model — General Parameters

| Parameter | Description |
|------------------|---|
| Mxxx | SOI MOSFET element name. Must begin with M, followed by up to 1023 alphanumeric characters. |
| nd | Drain terminal node name or number. |
| ng | Front gate node name or number. |
| ns | Source terminal node name or number. |
| ne | Back gate (or Substrate) node name or number. |
| np | External body contact node name or number. If 'body node' is to be checked in a .biaschk command, use keyword 'np' as in the BSIM3 SOI model. |
| nb | Internal body node name or number. |
| nT | Temperature node name or number. |
| mname | SOI MOSFET model name reference. |
| L | SOI MOSFET channel length in meters. The default is 5e-6. |
| W | SOI MOSFET channel width in meters. The default is 5e-6. |
| M | Multiplier to simulate multiple SOI MOSFETs in parallel. The M setting affects all channel widths, diode leakages, capacitances, and resistances. The default is 1. |
| AD | Drain diffusion area. The default is 0. |
| AS | Source diffusion area. The default is 0. |
| PD | Perimeter of the drain junction, including the channel edge. The default is 0. |
| PS | Perimeter of the source junction, including the channel edge. The default is 0. |
| NRD | Number of squares of drain diffusion for the drain series resistance. The default is 1. |
| NRS | Number of squares of source diffusion for the source series resistance. The default is 1. |

Chapter 2: MOSFET Models

LEVEL 70: BSIMSOI4 Model

| Parameter | Description |
|-----------|--|
| NRB | Number of squares for the body series resistance. The default is 1. |
| FRBODY | Coefficient of the distributed body resistance effects. <ul style="list-style-type: none"> ▪ If FRBODY is not specified, it's extracted from the model card ▪ If FRBODY is specified, it overrides FRBODY in the model card |
| RTH0 | Thermal resistance per unit width. <ul style="list-style-type: none"> ▪ If RTH0 is not specified, it's extracted from the model card ▪ If RTH0 is specified, it overrides RTH0 in the model card |
| CTH0 | Thermal capacitance per unit width. <ul style="list-style-type: none"> ▪ If CTH0 is not specified, it's extracted from the model card ▪ If CTH0 is specified, it overrides RTH0 in the model card |
| NBC | Number of body contact isolation edge. The default is 0 |
| NSEG | Number of segments for partitioning the channel width. The default is 1 |
| PDBCP | Parasitic perimeter length for the body contact at the drain side. The default is 0 |
| PSBCP | Parasitic perimeter length for the body contact at the source side. The default is 0 |
| AGBCP | Parasitic gate-to-body overlap area for the body contact. The default is 0 |
| AEBCP | Parasitic body to substrate overlap area for the body contact. The default is 0 |
| VBSUSR | Optional initial value of Vbs that you specify for transient analysis. |
| DELTOX | Shift in gate oxide thickness (TOX), that is, the difference between the electrical and physical gate oxide/insulator thickness. The default is 0 |
| TNODEOUT | Temperature node flag indicating the use of the T node. If you do not set TNODEOUT, you can specify four nodes for a device to float the body. Specifying five nodes implies that the fifth node is the external body contact node with a body resistance between the internal and external terminals. This configuration applies to a distributed body resistance simulation. If you set TNODEOUT, simulation interprets the last node as the temperature node. You can specify five nodes to float the device. Specifying six nodes implies body contact. Seven nodes is a body-contacted case with a accessible internal body node. You can use the temperature node to simulate thermal coupling. |
| OFF | Sets the initial condition to OFF for this element in DC analysis. |
| BJTOFF | Turns off BJT if equal to 1. |
| IC | Initial guess in the order (drain, front gate, internal body, back gate, external voltage). Simulation ignores Vps in a 4-terminal device. Use these settings if you specify UIC in the .TRAN statement. The .IC statement overrides it. |

| Parameter | Description |
|-----------|---|
| DTEMP | Increase in temperature. The default is 0. |
| SOIMOD | SOI model selector. <ul style="list-style-type: none"> ▪ If SOIMOD is not specified, it's extracted from the model card ▪ If SOIMOD is specified, it overrides SOIMOD in the model card |
| RGATEMOD | Gate resistance model selector. <ul style="list-style-type: none"> ▪ If RGATEMOD is not specified, it's extracted from the model card ▪ If RGATEMOD is specified, it overrides RGATEMOD in the model card |
| NF | Number of fingers. The default is 1. |
| SA | Distance between OD edge to poly from one side. The default is 0. |
| SB | Distance between OD edge to poly from another side. The default is 0. |
| SD | Distance between neighboring fingers. The default is 0. |
| RBDB | Resistance between dbNode and bNode. <ul style="list-style-type: none"> ▪ If RBDB is not specified, it's extracted from the model card ▪ If RBDB is specified, it overrides RBDB in the model card |
| RBSB | Resistance between sbNode and bNode. <ul style="list-style-type: none"> ▪ If RBSB is not specified, it's extracted from the model card ▪ If RBSB is specified, it overrides RBSB in the model card |
| DELVTO | Zero bias threshold voltage variation. The default is 0. |
| AGBCPD | Parasitic gate to body overlap area for body contact in DC. The default is 0. |
| RBODYMOD | Body resistance model selector. <ul style="list-style-type: none"> ▪ If RBODYMOD is not specified, it's extracted from the model card ▪ If RBODYMOD is specified, it overrides RBODYMOD in the model card |
| MULU0 | Low-field mobility (U_0) multiplier($U_{0_eff} = MULU0 * U_0$), the default is 1.0 |
| SOIQ0 | Floating body charge initialization. This parameter is set for the BQI algorithm of a floating body node. |
| DELSVAT | Shift in Saturation velocity (VSAT). |
| MULSVAT | Scaling factor of Saturation velocity (VSAT), the default is 1.0. |

Chapter 2: MOSFET Models

LEVEL 70: BSIMSOI4 Model

BSIMSOI4 Model — Control Parameters

| Parameter | Description | Unit | Default |
|------------|---|------|---------|
| VERSION | Mode version number | - | 4.40 |
| BSOIUPDATE | Flag for fixing thermal noise NF issue in versions 4.0-4.3 <ul style="list-style-type: none">■ 0 = Does not fix noise NF issue■ 1 = Fixes noise NF issue | - | 0 |
| SOIMOD | SOI model selector (instance) <ul style="list-style-type: none">■ SoiMod=0: BSIMPD■ SoiMod=1: unified model for PD&FD■ SoiMod=2: ideal FD■ SoiMod=3: auto selection by BSIMSOI | - | 0 |
| SHMOD | Flag for self-heating <ul style="list-style-type: none">■ 0 - no self-heating■ 1 - self-heating | - | 0 |
| MOBMOD | Mobility model selector | - | 0 |
| CAPMOD | Flag for the short channel capacitance model | - | 1 |
| NOIMOD | Flag for Noise model | - | 2 |
| IGCMOD | Gate-to-channel tunneling current model selector | - | 1 |
| IGBMOD | Gate-to-body tunneling current model selector | - | 0 |
| RDSMOD | Bias-dependent source/drain resistance model selector | - | 0 |
| RGATEMOD | Flag for gate resistance model | - | 0 |
| RBODYMOD | Flag for body resistance model | - | 0 |
| FNOIMOD | Flicker noise model selector | - | 1 |
| TNOIMOD | Thermal noise model selector | - | 0 |
| MTRLMOD | New material model selector | - | 0 |
| VGSTCVMOD | VgsteffCV model selector | - | 0 |
| IIIMOD | Impact ionization current model selector | - | 0 |
| GIDLMOD | New GIDL/GISL model selector | - | 0 |

| Parameter | Description | Unit | Default |
|-----------|------------------------------------|------|---------|
| FDMOD | New δV_{bi} model selector | - | 0 |

BSIMSOI4 Model — Process Parameters

| Parameter | Description | Unit | Default |
|-----------|---|-------------------|----------------------|
| TSI | Silicon film thickness | m | 10^{-7} |
| TBOX | Buried oxide thickness | m | 3×10^{-7} |
| TOX | Gate oxide thickness | m | 1×10^{-8} |
| TOXM | Gate oxide thickness used in extraction | m | TOX |
| XJ | S/D junction depth | m | TSI |
| NCH | Channel doping concentration | 1/cm ³ | 1.7×10^{17} |
| NSUB | Substrate doping concentration | 1/cm ³ | 6×10^{16} |
| NGATE | Poly gate doping concentration | 1/cm ³ | 0 |
| EOT | Effective SiO ₂ thickness | nm | 10 |
| LEFFEOT | Effective length for extraction of EOT | um | 1 |
| WEFFEOT | Effective width for extraction of EOT | um | 10 |
| TEMPEOT | Temperature for extraction of EOT | K | 300.15 |

BSIMSOI4 Model — DC Parameters

| Parameter | Description | Unit | Default |
|-----------|---|------------------|---------|
| VTH0 | Threshold voltage @ $V_{bs}=0$ for long and wide device | - | 0.7 |
| K1 | First order body effect coefficient | V ^{1/2} | 0.6 |
| K1W1 | First body effect width dependent parameter | m | 0 |
| K1W2 | Second body effect width dependent parameter | m | 0 |
| K2 | Second order body effect coefficient | - | 0 |

Chapter 2: MOSFET Models

LEVEL 70: BSIMSOI4 Model

| Parameter | Description | Unit | Default |
|-----------|--|--------------------------|------------|
| K3 | Narrow width coefficient | - | 0 |
| K3B | Body effect coefficient of k3 | 1/V | 0 |
| KB1 | Backgate body charge coefficient | - | 1 |
| W0 | Narrow width parameter | m | 0 |
| LPE0/NLX | Lateral non-uniform doping parameter | m | 1.74e-7 |
| LPEB | Lateral non-uniform doping effect on K1 | m | 0.0 |
| DVT0 | First coefficient of short-channel effect on Vth | - | 2.2 |
| DVT1 | Second coefficient of short-channel effect on Vth | - | 0.53 |
| DVT2 | Body-bias coefficient of short-channel effect on Vth | 1/V | -0.032 |
| DVT0W | First coefficient of narrow width effect on Vth for small channel length | - | 0 |
| DVT1W | Second coefficient of narrow width effect on Vth for small channel length | - | 5.3e6 |
| DVT2W | Body-bias coefficient of narrow width effect on Vth for small channel length | 1/V | -0.032 |
| U0 | Mobility at Temp = T_{nom} ■ NMOSFET ■ PMOSFET | cm ² /(V·sec) | 670 250 |
| UA | First-order mobility degradation coefficient | m/V | 2.25e-9 |
| UB | Second-order mobility degradation coefficient | (m/V) ² | 5.9e-19 |
| UC | Body-effect of mobility degradation coefficient | 1/V | -.0465 |
| UD | Coulomb scattering factor of mobility | - | 0 |
| UCS | Mobility exponent factor in mobMod=4 | - | 0 |
| EU | Mobility exponent factor in mobMod=4 | - | 0 |
| VSAT | Saturation velocity at Temp= T_{nom} | m/sec | 8e4 |
| A0 | Bulk charge effect coefficient for channel length | - | 1.0 |

| Parameter | Description | Unit | Default |
|------------------|---|-----------------------------|----------------|
| AGS | Gate bias coefficient of A_{bulk} | 1/V | 0.0 |
| B0 | Bulk charge effect coefficient for channel width | m | 0.0 |
| B1 | Bulk charge effect width offset | m | 0.0 |
| KETA | Body-bias coefficient of bulk charge effect | V ⁻¹ | 0 |
| KETAS | Surface potential adjustment for bulk charge effect | V | 0 |
| A1 | First non-saturation effect parameter | 1/V | 0.0 |
| A2 | Second non-saturation effect parameter | 0 | 1.0 |
| RDSW | Parasitic resistance per unit width | $\Omega - \mu\text{m}^{Wr}$ | 100 |
| PRWB | Body effect coefficient of R_{dsW} | 1/V | 0 |
| PRWG | Gate bias effect coefficient of R_{dsW} | 1/V ^{1/2} | 0 |
| WR | Width offset from Weff for Rds calculation | - | 1 |
| NFACTOR | Subthreshold swing factor | - | 1 |
| WINT | Width offset fitting parameter from I-V without bias | m | 0.0 |
| LINT | Length offset fitting parameter from I-V without bias | m | 0.0 |
| DWG | Coefficient of W_{eff} 's gate dependence | m/V | 0.0 |
| DWB | Coefficient of W_{eff} 's substrate body bias dependence | m/V ^{1/2} | 0.0 |
| DWBC | Width offset for body contact isolation edge | m | 0.0 |
| VOFF | Offset voltage in the subthreshold region for large W and L | V | -0.08 |
| ETA0 | DIBL coefficient in subthreshold region | - | 0.08 |
| ETAB | Body-bias coefficient for the subthreshold DIBL effect | 1/V | -0.07 |
| DSUB | DIBL coefficient exponent | - | 0.56 |
| CIT | Interface trap capacitance | F/m ² | 0.0 |
| CDSC | Drain/Source to channel coupling capacitance | F/m ² | 2.4e-4 |

Chapter 2: MOSFET Models

LEVEL 70: BSIMSOI4 Model

| Parameter | Description | Unit | Default |
|-----------|---|------------------|---------|
| CDSCB | Body-bias sensitivity of C_{dsc} | F/m ² | 0 |
| CDSCD | Drain-bias sensitivity of C_{dsc} | F/m ² | 0 |
| PCLM | Channel length modulation parameter | - | 1.3 |
| PDIBL1 | First output resistance DIBL effect correction parameter | - | 0.39 |
| PDIBL2 | Second output resistance DIBL effect correction parameter | - | 0.086 |
| DROUT | L dependence coefficient of the DIBL correction parameter in Rout | - | 0.56 |
| PVAG | Gate dependence of Early voltage | - | 0.0 |
| DELTA | Effective V_{ds} parameter | - | 0.01 |
| ALPHA0 | The first parameter of impact ionization current | m/V | 0.0 |
| FBJTII | Fraction of bipolar current affecting the impact ionization | - | 0.0 |
| BETA0 | First V_{ds} dependent parameter of impact ionization current | V ⁻¹ | 0 |
| BETA1 | Second V_{ds} dependent parameter of impact ionization current | - | 0 |
| BETA2 | Third V_{ds} dependent parameter of impact ionization current | V | 0.1 |
| VDSATII0 | Nominal drain saturation voltage at threshold for impact ionization current | V | 0.9 |
| TII | Temperature dependent parameter for impact ionization current | - | 0 |
| LII | Channel length dependent parameter at threshold for impact ionization current | - | 0 |
| ESATII | Saturation channel electric field for impact ionization current | V/m | 1e7 |
| SII0 | First V_{gs} dependent parameter for impact ionization current | V ⁻¹ | 0.5 |

| Parameter | Description | Unit | Default |
|-------------|--|------------|---------|
| SII1 | Second V_{gs} dependent parameter for impact ionization current | V^{-1} | 0.1 |
| SII2 | Third V_{gs} dependent parameter for impact ionization current | - | 0 |
| SIID | V_{ds} dependent parameter of drain saturation voltage for impact ionization current | V^{-1} | 0 |
| ABJTII | Exponent factor for avalanche current | V^{-1} | 0 |
| CBJTII | Length scaling parameter for II BJT part | m | 0 |
| EBJTII | Impact ionization parameter for BJT part | - | 0 |
| MBJTII | Internal B-C grading coefficient | - | 0.4 |
| VBCI | Internal B-C built-in potential | V | 0 |
| AGIDL | Pre-exponential GIDL constant | Ω^1 | 0.0 |
| BGIDL | GIDL exponential coefficient | V/m | 2.3e9 |
| CGIDL | Parameter for body bias effect on GIDL | V^3 | 0.5 |
| EGIDL/NGIDL | Fitting parameter for band bending for GIDL | V | 1.2 |
| AGISL | Pre-exponential GISL constant | Ω^1 | 0.0 |
| BGISL | GISL exponential coefficient | V/m | 2.3e9 |
| CGISL | Parameter for body bias effect on GISL | V^3 | 0.5 |
| EGISL | Fitting parameter for band bending for GISL | V | 1.2 |
| RGIDL | V_{gs} -dependent parameter for GIDL when gidlMod = 1 | - | 1.0 |
| KGIDL | V_{ds} -dependent parameter for GIDL when gidlMod = 1 | V | 0.0 |
| FGIDL | V_{ds} -dependent parameter for GIDL when gidlMod = 1 | - | - |
| RGISL | V_{gs} -dependent parameter for GISL when gislMod = 1 | - | 1.0 |
| KGISL | V_{bs} -dependent parameter for GISL when gislMod = 1 | V | 0.0 |
| FGISL | V_{bs} -dependent parameter for GISL when gislMod = 1 | V | 0.0 |

Chapter 2: MOSFET Models

LEVEL 70: BSIMSOI4 Model

| Parameter | Description | Unit | Default |
|-----------|--|------------------|-----------------------------|
| NDIODE | Diode non-ideality factor for source | - | 1.0 |
| NDIODED | Diode non-ideality factor for drain | - | Default to its source value |
| NRECF0 | Recombination non-ideality factor at forward bias for source | - | 2.0 |
| NRECF0D | Recombination non-ideality factor at forward bias for drain | - | Default to its source value |
| NRECR0 | Recombination non-ideality factor at reversed bias for source | - | 10 |
| NRECR0D | Recombination non-ideality factor at reversed bias for drain | - | Default to its source value |
| ISBJT | BJT injection saturation current | A/m ² | 1e-6 |
| IDBJT | BJT injection saturation current | A/m ² | 1e-6 |
| ISDIF | Body to source/drain injection saturation current | A/m ² | 1e-7 |
| IDDIF | Body to source/drain injection saturation current | A/m ² | 1e-7 |
| ISREC | Recombination in depletion saturation current | A/m ² | 1e-5 |
| IDREC | Recombination in depletion saturation current | A/m ² | 1e-5 |
| ISTUN | Reverse tunneling saturation current | A/m ² | 0.0 |
| IDTUN | Reverse tunneling saturation current | A/m ² | 0.0 |
| LN | Electron/hole diffusion length | m | 2e-6 |
| VREC0 | Voltage dependent parameter for recombination current for source | V | 0 |
| VREC0D | Voltage dependent parameter for recombination current for drain | V | Default to its source value |
| VTUN0 | Voltage dependent parameter for tunneling current for source | V | 0 |

| Parameter | Description | Unit | Default |
|-----------|---|--|-----------------------------|
| VTUN0D | Voltage dependent parameter for tunneling current for drain | V | Default to its source value |
| NBJT | Power coefficient of channel length dependency for bipolar current | - | 1 |
| LBJT0 | Reference channel length for bipolar current | m | 0.20e-6 |
| VABJT | Early voltage for bipolar current | V | 10 |
| AELY | Channel length dependency of early voltage for bipolar current | V/m | 0 |
| AHLI | High level injection parameter for bipolar current for source | - | 0 |
| AHLID | High level injection parameter for bipolar current for drain | - | Default to its source value |
| RBODY | Intrinsic body contact sheet resistance | Ω / square | 0.0 |
| RBSH | Extrinsic body contact sheet resistance | Ω / square | 0.0 |
| RSH | Source drain sheet resistance in ohm per square | Ω / square | 0.0 |
| RHALO | Body halo sheet resistance | Ω / m | 1e15 |
| RSW | Zero bias lightly-doped source resistance per unit width for RDSENSMOD=1 | Ω (μm) ^{Wr} | 50 |
| RDW | Zero bias lightly-doped drain resistance per unit width for RDSENSMOD=1 | Ω (μm) ^{Wr} | 50 |
| RSWMIN | Lightly-doped source resistance per unit width at high V_{gs} and zero V_{bs} for RDSENSMOD=1 | Ω (μm) ^{Wr} | 0 |
| RDWMIN | Lightly-doped source resistance per unit width at high V_{gs} and zero V_{bs} for RDSENSMOD=1 | Ω (μm) ^{Wr} | 0 |
| DVTP0 | First parameter for Vth shift due to pocket | m | 0.0 |
| DVTP1 | Second parameter for Vth shift due to pocket | V^{-1} | 0.0 |
| DVTP2 | Third parameter for Vth shift due to pocket | V^{-1} | 0.0 |
| DVTP3 | Forth parameter for Vth shift due to pocket | V^{-1} | 0.0 |

Chapter 2: MOSFET Models

LEVEL 70: BSIMSOI4 Model

| Parameter | Description | Unit | Default |
|-----------|--|--------------------|---------|
| DVTP4 | Fifth parameter for Vth shift due to pocket | V ⁻¹ | 0.0 |
| PDITS | Coefficient for drain-induced Vth shifts | V ⁻¹ | 1e-20 |
| PDITSL | Length dependence of drain-induced Vth shifts | m ⁻¹ | 0 |
| PDITSD | Vds dependence of drain-induced Vth shifts | V ⁻¹ | 0 |
| FPROUT | Effect of pocket implant on rout degradation | V/m ^{0.5} | 0.0 |
| MINV | Vgsteff fitting parameter for moderate inversion | - | 0.0 |

BSIMSOI4 Model — Gate-to-body Tunneling Parameters

| Parameter | Description | Unit | Default |
|-----------|--|------------------|---------|
| IGMOD | Gate current model selector | - | 0 |
| TOXQM | Oxide thickness for I_{gb} calculation | m | Tox |
| NTOX | Power term of gate current | - | 1 |
| TOXREF | Target oxide thickness | m | 2.5e-9 |
| EBG | Effective bandgap in gate current calculation | V | 1.2 |
| ALPHAGB1 | First V_{ox} dependent parameter for gate current in inversion | 1/V | 0.35 |
| BETAGB1 | Second V_{ox} dependent parameter for gate current in inversion | 1/V ² | 0.03 |
| VGB1 | Third V_{ox} dependent parameter for gate current in inversion | V | 300 |
| VEVB | V_{aux} parameter for valence band electron tunneling | - | 0.075 |
| ALPHAGB2 | First V_{ox} dependent parameter for gate current in accumulation | 1/V | 0.43 |
| BETAGB2 | Second V_{ox} dependent parameter for gate current in accumulation | 1/V ² | 0.05 |
| VGB2 | Third V_{ox} dependent parameter for gate current in accumulation | V | 17 |

| Parameter | Description | Unit | Default |
|-----------|---|---------|---------|
| VECB | V_{aux} parameter for conduction band electron tunneling | - | 0.026 |
| AIGBCP2 | First V_{gp} dependent parameter for gate current in accumulation in AGBCP2 region | $1/V^2$ | 0.043 |
| BIGBCP2 | Second V_{gp} dependent parameter for gate current in accumulation in AGBCP2 region | $1/V^2$ | 0.0054 |
| CIGBCP2 | Third V_{gp} dependent parameter for gate current in accumulation in AGBCP2 region | $1/V^2$ | 0.0075 |

BSIMSOI4 Model — AC and Capacitance Parameters

| Parameter | Description | Unit | Default |
|-----------|---|---------|-----------------------------|
| XPART | Charge partitioning rate flag | - | - |
| CGSO | Non LDD region source-gate overlap capacitance per channel length | F/m | Calculated |
| CGDO | Non LDD region drain-gate overlap capacitance per channel length | F/m | Calculated |
| CGEO | Gate substrate overlap capacitance per unit channel length | F/m | 0.0 |
| CJSWG | Source (gate side) sidewall junction capacitance per unit width (normalized to 100nm T_{Si}) | F/m^2 | 1e-10 |
| CJSWGD | Drain (gate side) sidewall junction capacitance per unit width (normalized to 100nm T_{Si}) | F/m^2 | Default to its source value |
| PBSWG | Source (gate side) sidewall junction capacitance built-in potential | V | 0.7 |
| PBSWGD | Drain (gate side) sidewall junction capacitance built-in potential | V | Default to its source value |
| MJSWG | Source (gate side) sidewall junction capacitance grading coefficient | V | 0.5 |
| MJSWGD | Drain (gate side) sidewall junction capacitance grading coefficient | V | Default to its source value |
| TT | Diffusion capacitance transit time coefficient | Second | 1e-12 |

Chapter 2: MOSFET Models

LEVEL 70: BSIMSOI4 Model

| Parameter | Description | Unit | Default |
|-----------|--|------------------|------------|
| NDIF | Power coefficient of channel length dependency for diffusion capacitance | - | -1 |
| LDIF0 | Channel-length dependency coefficient of diffusion cap. | - | 1 |
| VSDFB | Source/drain bottom diffusion capacitance flatband voltage | V | Calculated |
| VSDTH | Source/drain bottom diffusion capacitance threshold voltage | V | Calculated |
| CSDMIN | Source/drain bottom diffusion minimum capacitance | V | Calculated |
| ASD | Source/drain bottom diffusion smoothing parameter | - | 0.3 |
| CSDESW | Source/drain sidewall fringing capacitance per unit length | F/m | 0.0 |
| CGSL | Light doped source-gate region overlap capacitance | F/m | 0.0 |
| CGDL | Light doped drain-gate region overlap capacitance | F/m | 0.0 |
| CKAPPA | Coefficient for lightly doped region overlap capacitance fringing field capacitance | F/m | 0.6 |
| CF | Gate to source/drain fringing field capacitance | F/m | Calculated |
| CLC | Constant term for the short channel model | m | 0.1x10-7 |
| CLE | Exponential term for the short channel model | None | 0.0 |
| DLC | Length offset fitting parameter for gate charge | m | lint |
| DLCB | Length offset fitting parameter for body charge | m | 0 |
| DLBG | Length offset fitting parameter for backgate charge | m | 0.0 |
| DWC | Width offset fitting parameter from C-V | m | wint |
| DELVT | Threshold voltage adjust for C-V | V | 0.0 |
| FBODY | Scaling factor for body charge | - | 1.0 |
| ACDE | Exponential coefficient for charge thickness in capMod=3 for accumulation and depletion regions | m/V | 1.0 |
| MOIN | Coefficient for the gate-bias dependent surface potential. | V ^{1/2} | 15.0 |

| Parameter | Description | Unit | Default |
|-----------|---|------|---------|
| CFRCOEFF | Sidewall fringe capacitance coefficient | - | 1 |

BSIMSOI4 Model — Temperature Parameters

| Parameter | Description | Unit | Default |
|-----------|--|--------------------|-----------------------------|
| TNOM | Temperature at which parameters are expected | °C | 27 |
| UTE | Mobility temperature exponent | None | -1.5 |
| KT1 | Temperature coefficient for threshold voltage | V | -0.11 |
| KT11 | Channel length dependence of the temperature coefficient for threshold voltage | V*m | 0.0 |
| KT2 | Body-bias coefficient of the V _{th} temperature effect | None | 0.022 |
| UA1 | Temperature coefficient for U _a | m/V | 4.31e-9 |
| UB1 | Temperature coefficient for U _b | (m/V) ² | -7.61e-18 |
| UC1 | Temperature coefficient for U _c | 1/V | -0.056 |
| AT | Temperature coefficient for saturation velocity | m/sec | 3.3e4 |
| TCJSWG | Temperature coefficient of C _{jswgs} | 1/K | 0 |
| TPBSWG | Temperature coefficient of P _{bswgs} | V/K | 0 |
| TCJSWGD | Temperature coefficient of C _{jswgd} | 1/K | Default to its source value |
| TPBSWGD | Temperature coefficient of P _{bswgd} | V/K | Default to its source value |
| CTH0 | Normalized thermal capacity | (W*sec)/ m°C | 1e-5 |
| PRT | Temperature coefficient for R _{dsw} | Ω - μm | 0 |
| RTH0 | Normalized thermal resistance | m°C/W | 0 |
| NTRECF | Temperature coefficient for N _{refcf} | - | 0 |

Chapter 2: MOSFET Models

LEVEL 70: BSIMSOI4 Model

| Parameter | Description | Unit | Default |
|-----------|--|------|---------|
| NTRECR | Temperature coefficient for N_{recr} | - | 0 |
| XBJT | Power dependence of j_{bjt} on temperature | - | 1 |
| XDIFS | Power dependence of j_{difs} on temperature | - | Xbjt |
| XRECS | Power dependence of j_{recs} on temperature | - | 1 |
| XTUNS | Power dependence of j_{tuns} on temperature | - | 0 |
| XDIFD | Power dependence of j_{difd} on temperature | - | Xbjt |
| XRECD | Power dependence of j_{recd} on temperature | - | 1 |
| XTUND | Power dependence of j_{tund} on temperature | - | 0 |
| WTH0 | Minimum width for thermal resistance calculation | m | 0 |
| TVBCI | Temperature coefficient for V_{bci} | - | 0 |

BSIMSOI4 Model — Built-in Potential Lowering Model Parameters

| Parameter | Description | Unit | Default |
|-----------|---|------|---------|
| SOIMOD | SOI model selector. <ul style="list-style-type: none"> ■ SoiMod=0: BSIMPD ■ SoiMod=1: unified model for PD&FD ■ SoiMod=2: ideal FD ■ SoiMod=3: auto selection by BSIMSO | - | 0 |
| VBSA | Offset voltage due to non-idealities | V | 0 |
| NOFFF | Smoothing parameter in FD module | - | 1 |
| VOFFF | Smoothing parameter in FD module | V | 0 |
| K1B | First backgate body effect parameter | - | 1 |
| K2B | Second backgate body effect parameter for short channel effect | - | 0 |
| DK2B | Third backgate body effect parameter for short channel effect | - | 0 |
| DVBD0 | First short channel effect parameter in FD module | - | 0 |

| Parameter | Description | Unit | Default |
|-----------|--|------|---------|
| DVBD1 | Second short channel effect parameter in FD module | - | 0 |
| MOINFD | Gate bias dependence coefficient of surface potential in FD module | - | 1e3 |
| VBS0PD | Upper bound of built-in potential lowering for BSIMPD operation | V | 0.0 |
| VBS0FD | Lowering bound of built-in potential lowering for ideal FD operation | V | 0.5 |

BSIMSOI4 Model — RF Model Parameters

| Parameter | Description | Unit | Default |
|-----------|---|----------|---------|
| RGATEMOD | Gate resistance model selector <ul style="list-style-type: none"> ■ rgatemod = 0 No gate resistance ■ rgatemod = 1 Constant gate resistance ■ rgatemod = 2 Rii model with variable resistance ■ rgatemod = 3 Rii model with two nodes | - | 0 |
| RBODYMOD | <ul style="list-style-type: none"> ■ RbodyMod=0 No body resistance model ■ RbodyMod=1 Two-resistor body resistance model | - | 0 |
| RSHG | Gate electrode sheet resistance | Ω/square | 0.1 |
| XRCRG1 | Parameter for distributed channel-resistance effect for intrinsic input resistance | - | 12.0 |
| XRCRG2 | Parameter to account for the excess channel diffusion resistance for intrinsic input resistance | - | 1.0 |
| NGCON | Number of gate contacts | - | 1 |
| XGW | Distance from the gate contact to the channel edge | m | 0.0 |
| XGL | Offset of the gate length due to variations in patterning | m | 0.0 |
| RBSB | Resistance between sbNode and bNode | Ω | 50.0 |
| RBDB | Resistance between dbNode and bNode | Ω | 50.0 |
| GBMIN | Conductance parallel with RBSB/RBDB | Ω | 1e-12 |

Chapter 2: MOSFET Models

LEVEL 70: BSIMSOI4 Model

BSIMSOI4 Model — Noise Model Parameters

| Parameter | Description | Unit | Default |
|-----------|--|------|---------|
| FNOIMOD | Flicker noise model selector | - | 1 |
| TNOIMOD | Thermal noise model selector | - | 0 |
| NTNOI | Noise factor for short-channel devices for TNOIMOD=0 or 2 | - | 1.0 |
| TNOIA | Coefficient of channel length dependence of total channel thermal noise | - | 1.5 |
| TNOIB | Channel length dependence parameter for channel thermal noise partitioning | - | 3.5 |
| RNOIA | Thermal noise parameter | - | 0.577 |
| RNOIB | Thermal noise parameter | - | 0.37 |
| W0FLK | Flicker noise width dependence parameter | - | -1 |
| BF | Flicker noise length dependence exponent | - | 2.0 |

BSIMSOI4 Model — Stress Model Parameters

| Parameter | Description | Unit | Default |
|-----------|---|------|---------|
| SA | Distance between OD edge to poly from one side | m | 0.0 |
| SB | Distance between OD edge to poly from another side | m | 0.0 |
| SD | Distance between neighboring fingers | m | 0.0 |
| SAREF | Reference distance between OD and edge to poly of one side | m | 1e-6 |
| SBREF | Reference distance between OD and edge to poly of another side | m | 1e-6 |
| WLOD | Width parameter for stress effect | M | 0.0 |
| KU0 | Mobility degradation/enhancement | M | 0.0 |
| KVSAT | Saturation velocity degradation/enhancement parameter for stress effect | M | 0.0 |
| TKU0 | Temperature coefficient of KU0 | - | 0.0 |
| LKU0 | Length dependence of KU0 | - | 0.0 |

| Parameter | Description | Unit | Default |
|-----------|--|------|---------|
| WKU0 | width dependence of KU0 | - | 0.0 |
| PKU0 | Cross-term dependence of KU0 | - | 0.0 |
| LLODKU0 | Length parameter for u0 stress effect | - | 0.0 |
| WLODKU0 | Width parameter for u0 stress effect | - | 0.0 |
| KVTH0 | Threshold shift parameter for stress effect | Vm | 0.0 |
| LKVTH0 | Length dependence of KVHT0 | - | 0.0 |
| WKVTH0 | Width dependence of KVHT0 | - | 0.0 |
| PKVTH0 | Cross term dependence of KVHT0 | - | 0.0 |
| LLODVTH | Length parameter for Vth stress effect | - | 0.0 |
| WLODVTH | Width parameter for Vth stress effect | - | 0.0 |
| STK2 | K2 shift factor related to Vth0 change | M | 0.0 |
| LODK2 | K2 shift modification factor for stress effect | - | 1.0 |
| STETA0 | Eta0 shift factor related to vth0 change | M | 0.0 |
| LODETA0 | Eta0 shift modification factor for stress effect | - | 1.0 |

BSIMSOI4 Model — Parameter Range Limit

Simulation reports either a warning or a fatal error if BSIMSOI4 parameters fall outside predefined ranges. These range limitations prevent (or at least warn of) potential numerical problems.

To control the maximum number of simulation warning messages printing to the output file, use:

```
.OPTION WARNLIMIT=#
```

In the preceding .OPTION statement, # is the maximum number of warning messages that simulation reports. The default `WARNLIMIT` value is 1. In some

Chapter 2: MOSFET Models

LEVEL 70: BSIMSOI4 Model

cases, simulation checks parameters only if you set the PARMAMCHK=1 model parameter.

| Parameter | Limit |
|-----------|-------------------|
| ACDE | < 0.1, > 1.6 warn |
| B1+WEFF | b1+weff = 0 fatal |
| CLC | < 0 fatal |
| DELTA | < 0 fatal |
| DROUT | < 0 fatal |
| DSUB | <0 fatal |
| DVT1 | < 0 fatal |
| DVT1W | < 0 fatal |
| FPROUT | < 0 fatal |
| KVSAT | < -1.0, >1.0 warn |
| LODETA0 | <= 0 warn |
| LODK2 | <= 0 warn |
| LPE0 | < -leff fatal |
| LPEB | < -leff fatal |
| MOIN | < 5, > 25 warn |
| MOINFD | < 5 warn |
| NF | < 1 fatal |
| NGATE | < 0, > 1e25 fatal |
| NOFF | < 0.1, > 4.0 warn |
| NPEAK | <= 0 fatal |
| PCLM | <=0 fatal |
| PD | < w warn |

| Parameter | Limit |
|-----------|------------------------|
| PDITS | < 0 fatal |
| PDITSL | < 0 fatal |
| PS | < w warn |
| SAREF | <= 0 fatal |
| SBREF | <= 0 fatal |
| TBOX | <= 0 fatal |
| TOX | tox+deltox <= 0 fatal |
| TOXM | toxm+deltox <= 0 fatal |
| U0 | <= 0 fatal |
| VSAT | <= 0 fatal |
| W0 | w0+weff =0 fatal |
| WLOD | < 0 warn |

If paramchk=1 following parameter limit range is added

| | |
|----------|---------------------|
| A2 | < 0.01, > 1 warn |
| AELY | < 0 warn |
| AHLI | < 0 warn |
| ALPHAGB1 | < 0 warn |
| ALPHAGB2 | < 0 warn |
| ASD | < 0 warn |
| B1 | b1+weff < 1e-7 warn |
| BELTAVOX | <= 0 warn |
| BETA0 | < 0 warn |
| BETA1 | < 0 warn |
| BETA2 | < 0 warn |

Chapter 2: MOSFET Models

LEVEL 70: BSIMSOI4 Model

| Parameter | Limit |
|-----------|----------|
| BETAGB1 | < 0 warn |
| BETAGB2 | < 0 warn |
| CDSC | < 0 warn |
| CDSCD | < 0 warn |
| CGDO | < 0 warn |
| CGEO | < 0 warn |
| CGSO | < 0 warn |
| CSDESW | < 0 warn |
| CSDMIN | < 0 warn |
| CTH0 | < 0 warn |
| DVT0 | < 0 warn |
| DWBC | < 0 warn |
| EBG | < 0 warn |
| ETA0 | < 0 warn |
| FBJTII | < 0 warn |
| IDBJT | < 0 warn |
| IDDIFF | < 0 warn |
| IDREC | < 0 warn |
| IDTUN | < 0 warn |
| ISBJT | < 0 warn |
| ISDIFF | < 0 warn |
| ISREC | < 0 warn |
| ISTUN | < 0 warn |
| K1W1 | < 0 warn |

| Parameter | Limit |
|-----------|------------------------|
| K1W2 | < 0 warn |
| KETAS | < 0 warn |
| LEFF | <= 5e-8 warn |
| LEFFCV | <= 5e-8 warn |
| LII | < 0 warn |
| LPE0 | < 0 warn |
| NBJT | < 0 warn |
| NDIODE | < 0 warn |
| NDIODED | < 0 warn |
| NFACTOR | < 0 warn |
| NGATE | < 1e18 warn |
| NIGC | <= 0 warn |
| NPEAK | <= 1e15, >= 1e21 warn |
| NSUB | <= -1e21, >= 1e21 warn |
| NTOX | < 0 warn |
| NTUN | < 0 warn |
| NTUND | < 0 warn |
| PDIBL1 | < 0 warn |
| PDIBL2 | < 0 warn |
| PIGCD | <= 0 warn |
| POXEDGE | <= 0 warn |
| RBODY | < 0 warn |
| RBSH | < 0 warn |
| RDS0 | < 0.001 warn |

Chapter 2: MOSFET Models

LEVEL 70: BSIMSOI4 Model

| Parameter | Limit |
|-----------|---------------------|
| RDSW | < warn |
| RHALO | < 0 warn |
| RTH0 | < 0 warn |
| SII1 | < 0 warn |
| SII2 | < 0 warn |
| SIID | < 0 warn |
| TII | < 0 warn |
| TOXQM | < 0 warn |
| TOXREF | < 0 warn |
| TT | < 0 warn |
| VECB | < 0 warn |
| VEVB | < 0 warn |
| VGB1 | < 0 warn |
| VGB2 | < warn |
| VOXH | < 0 warn |
| VREC0 | < 0 warn |
| VREC0D | < 0 warn |
| VSATTEMP | < 1e3 warn |
| VTUN0 | < 0 warn |
| VTUN0D | < 0 warn |
| W0 | w0+weff < 1e-7 warn |
| WEFF | <= 1e-7 warn |
| WEFFCV | <= 1e-7 warn |
| WTH0 | < 0 warn |

| Parameter | Limit |
|-----------|-------------------|
| ACDE | < 0.1, > 1.6 warn |
| AGIDL | < 0 warn |
| AHLID | < 0 warn |
| BGIDL | < 0 warn |
| CAPMOD | < 2 warn |
| CGIDL | < 0 warn |
| DLBG | < 0 warn |
| EGIDL | < 0 warn |
| ESATII | <= 0 warn |
| MOIN | < 5, > 25 warn |
| NTRECF | < 0 warn |
| NTRECR | < 0 warn |
| RBODY | < 0 warn |
| RBSH | < 0 warn |
| TCJSWG | < 0 warn |
| TCJSWGD | < 0 warn |
| TPBSWG | < 0 warn |
| TPBSWGD | < 0 warn |
| XJ | > tsi warn |

BSIMSOI4 Model — Version Updates

This section covers the following topics:

- [BSIMSOI4 Version 4.4 Update](#)
- [BSIMSOI4 Version 4.3.1 Update](#)

Chapter 2: MOSFET Models

LEVEL 70: BSIMSOI4 Model

- [BSIMSOI4 Version 4.3 and 4.2 Updates](#)
- [BSIMSOI4 Version 4.1 Update](#)

BSIMSOI4 Version 4.4 Update

The following changes were made for the BSIM4 version 4.4 release:

- Implemented a check on the physical thickness and doping level of the channel
- Enhanced sidewall fringe capacitance formulation.
- Bug fixes for derivative expressions in SOIMOD=1 and 2.

BSIMSOI4 Version 4.3.1 Update

In BSIMSOI4 version 4.3.1 the following updates are added:

1. The temperature derivative expressions are greatly improved.
2. Bug fixes related to mtrlMod=1 are incorporated.
3. Thermal noise NF issue is fixed in SOI4.3.1.

For a description of this model, see the *BSIMSOI4.3.1 MOSFET Model User's Manual* at <http://www-device.eecs.berkeley.edu/~bsimsoi/get.html>

BSIMSOI4 Version 4.3 and 4.2 Updates

In BSIMSOI4 versions 4.3 and 4.2, the following features were added:

1. Some bugs such as charge derivative issues are fixed in version 4.2.
2. The charge derivative issues in v4.2 and earlier versions are greatly improved in version 4.3.
3. Many expressions and derivatives are greatly improved in version 4.3, such as GISL.
4. A model parameter `BSOIUPDATE=0 | 1` has been added using a flag to control thermal noise nf fix for v. 4.3. Its default value is 0, providing "No fix" for backward compatibility. Setting `BSOIUPDATE=1` turns on the HSPICE thermal noise nf fix.

BSIMSOI4 Version 4.1 Update

In BSIMSOI4.1, the following features were added:

- A new material model (`mtrlMod`)
- Asymmetric GIDL/GISL model and new GIDL/GISL model (`gidlMod`)
- A new impact-ionization current model
- An improved Coulombic scattering model for high k/metal gate

- An improved body-contact model to characterize the opposite-type gate
- A new ΔV_{bi} model to simplify the parameter extraction
- A new $V_{gsteff}CV$ model for C-V, which is similar to V_{gsteff} in I-V
- A new gate current component in body contact region
- An improved DITS model with more flexibility and better fit

For a description of this model, see the *BSIMSOI4.1 MOSFET Model User's Manual* at <http://www-device.eecs.berkeley.edu/~bsimsoi/get.html>.

LEVEL 71: TFT Model

Thin-film transistor (TFT) process technology has been the industry mainstream technology of choice to implement various flat-panel display applications. While there exist many similarities in the electrical terminal characteristics between TFTs and their crystalline silicon counterparts, unique charge trapping/de-trapping and charge carrier transport mechanisms associated with the grains and grain boundaries in the channel region have led to significant technical challenges in TFT device modeling for accurate and scalable SPICE simulations.

The Level 71 TFT model is a unified model. It is used for polycrystalline silicon (p-si), but it is also applicable to amorphous silicon (a-si). The model has been developed based on BSIMSOI, with high accuracy in geometrical, bias, and temperature scaling. It explicitly and accurately considers the following physical effects: non-ideality of the subthreshold swing, quasi-saturation, bias-dependent source/drain resistance, kink in the saturation region, self heating, large leakage current, and many other related device behaviors.

This HSPICE TFT model is fully supported by Synopsys' parameter extraction tool, Aurora. For detail on usage, contact the Synopsys support teams.

The following sections discuss these topics:

- [TFT Model — General Syntax](#)
- [TFT Model Parameters](#)

TFT Model — General Syntax

Syntax:

```
Mxxx nd ng ns ne [np] [nb] [nT] mname [L=val]
+ [M=val] [AS=val] [PS=val] [NRD=val]
+ [NRS=val] [NRB=val] [CTH0=val]
+ [NSEG=val] [PDBCP=val] [PSBCP=val] [AGBCP=val]
+ [AEBCP=val] [DELTOX=val] [TNODEOUT]
+ [off] [FRBODY] [BJToff=val] [IC=Vds, Vgs, Vbs, Ves, Vps]
```

TFT Model Parameters

This section covers the following topics:

- [TFT Model — Argument Descriptions](#)
- [TFT Model — General Parameters](#)
- [TFT Model — Process Parameters](#)
- [TFT Model — DC Parameters](#)
- [TFT Model — AC and Capacitance Parameters](#)
- [TFT Model — Temperature Parameters](#)
- [TFT Model — Bias-Dependent Source \(Rs\) / Drain \(Rd\) Parameters](#)

TFT Model — Argument Descriptions

| Argument | Description |
|----------|--|
| Mxxx | TFT element name. Must begin with M, followed by up to 1023 alphanumeric characters. |
| nd | Drain terminal node name or number. |
| ng | Front gate node name or number. |
| ns | Source terminal node name or number. |
| ne | Back gate (or substrate) node name or number. |
| np | External body contact node name or number. |
| nb | Internal body node name or number. |
| nT | Temperature node name or number. |
| mname | MOSFET model name reference. |
| L | TFT channel length in meters. This parameter overrides DEFL in an OPTIONS statement. Default=DEFL with a maximum of 0.1m. |
| W | MOSFET channel width in meters. This parameter overrides DEFW in an OPTIONS statement. Default=DEFW. |
| M | Multiplier to simulate multiple TFT in parallel. The M setting affects all channel widths, diode leakages, capacitances, and resistances. Default=1. |
| AD | Drain diffusion area. Overrides .OPTION DEFAD statement. Default=DEFAD. |

Chapter 2: MOSFET Models

LEVEL 71: TFT Model

| Argument | Description |
|----------|---|
| AS | Source diffusion area. Overrides .OPTION DEFAS statement. Default=DEFAS. |
| PD | Drain junction perimeter, including channel edge. Overrides .OPTION DEFPD. |
| PS | Source junction perimeter including channel edge. Overrides .OPTION DEFPS. |
| NRD | Number of squares of drain diffusion for the drain series resistance. Overrides .OPTION DEFNRD. |
| NRS | Number of squares of source diffusion for the source series resistance. Overrides .OPTION DEFNRS. |
| NRB | Number of squares for the body series resistance. |
| FRBODY | Coefficient of the distributed body resistance effects. Default=1.0 |
| RTH0 | Thermal resistance per unit width: If you do not specify RTH0, simulation extracts it from the model card. If you specify RTH0, it overrides RTH0 in the model card. |
| CTH0 | Thermal capacitance per unit width: If you do not specify CTH0, simulation extracts it from the model card. If you specify CTH0, it overrides CTH0 in the model card. |
| NBC | Number of body contact isolation edge. |
| NSEG | Number of segments for partitioning the channel width. |
| PDBCP | Parasitic perimeter length for the body contact at the drain side. |
| PSBCP | Parasitic perimeter length for the body contact at the source side. |
| AGBCP | Parasitic gate-to-body overlap area for the body contact. |
| AEBCP | Parasitic body-to-substrate overlap area for the body contact. |
| VBSUSR | Optional initial Compared value of Vbs that you specify for transient analysis. |
| DELTOX | Shift in gate oxide thickness (TOX). That is, the difference between the electrical and physical gate oxide/insulator thicknesses. |
| TNODEOUT | Temperature node flag indicating the use of the T node. ¹ See footnote below. |

| Argument | Description |
|----------|--|
| OFF | Sets the initial condition of the element to OFF in DC analysis. |
| BJTOFF | Turning off BJT if equal to 1. |
| IC | Initial guess in the order (drain, front gate, internal body, back gate, external voltage). (ignores Vps for 4-terminal devices) Use these only if you specify UIC in the .TRAN statement. The .IC statement overrides it. |

1. If you do not set TNODEOUT, you can specify 3 nodes for a device to float the body. Specifying 4 nodes implies that the 4th node is the external body contact node with a body resistance between the internal and external terminals. This configuration applies to a distributed body resistance simulation.
 If you set TNODEOUT, simulation interprets the last node as the temperature node. You can specify 4 nodes to float the device. Specifying 5 nodes implies body contact. 6 nodes is a body-contacted case with an accessible internal body node. You can use the temperature node to simulate thermal coupling.

TFT Model — General Parameters

| Parameter | Unit | Default | Description |
|-----------|------|---------|---|
| MOBMOD | - | 1 | Mobility model selector |
| NOIMOD | - | 1 | Flag for the noise model |
| SHMOD | - | 0 | Flag for self-heating: <ul style="list-style-type: none"> ■ 0=no self-heating ■ 1=self-heating |
| TFTMOD | - | 0 | Flag for the transistor operation mode: <ul style="list-style-type: none"> ■ 0=partially depleted ■ 1=dynamic depleted ■ 2=partially depleted |

TFT Model — Process Parameters

| Parameter | Unit | Default | Description |
|-----------|-------------------|---------|---|
| DTOXCV | | | Difference between the electrical and physical gate oxide thicknesses, due to the effects of the gate poly depletion and the finite channel charge layer thickness. |
| NCH | 1/cm ³ | 1e15 | Channel doping concentration |
| NGATE | 1/cm ³ | 0 | Poly gate doping concentration |

Chapter 2: MOSFET Models

LEVEL 71: TFT Model

| Parameter | Unit | Default | Description |
|-----------|-------------------|---------|--------------------------------|
| NSUB | 1/cm ³ | 6.0e16 | Substrate doping concentration |
| TOX | m | 4.5e-8 | Gate oxide thickness |
| TSI | m | 1.0e-8 | Silicon film thickness |

TFT Model — DC Parameters

| Parameter | Unit | Default | Description |
|-----------|------------------|---------|--|
| A0 | - | 2.5 | Bulk charge effect coefficient for the channel length |
| A1 | 1/V | 0.68 | First non-saturation effect parameter |
| A2 | - | 0.18 | Second non-saturation effect parameter |
| AELY | V/m | -0.1 | Channel length dependency of the early voltage for the bipolar current |
| AGIDL | 1/W | 1e-7 | GIDL constant |
| AGS | 1/V | 0.15 | Gate bias coefficient of Abulk |
| AHLI | - | 0.1 | High-level injection parameter for the bipolar current |
| ALPHA0 | m/V | 1e-12 | First parameter of the impact ionization current |
| B0 | m | 4.5e-8 | Bulk charge effect coefficient for the channel width |
| B1 | m | 1e-7 | Bulk charge effect width offset |
| BETA0 | 1/V | 40 | First Vds dependence parameter of the impact ionization current |
| BETA1 | - | 5 | Second Vds dependence parameter of the impact ionization current |
| BETA2 | V | 0 | Third Vds dependence parameter of the impact ionization current |
| BETAG | - | 3 | Gate induced grain boundary barrier lowering coefficient |
| BGIDL | V/m | 9.5e9 | GIDL exponential coefficient |
| CDSC | F/m ² | -1e-3 | Drain/source to the channel coupling capacitance |

| Parameter | Unit | Default | Description |
|-----------|--------------------|---------|--|
| CDSCB | F/m ² | 0 | Body-bias sensitivity of cdsc |
| CDSCD | F/m ² | 1e-3 | Drain-bias sensitivity of cdsc |
| CGIDL | - | 3.7e-2 | Body voltage factor for gidl |
| CIT | F/m ² | 0.0 | Interface trap capacitance |
| DELTA | - | 2.3 | Effective Vds parameter |
| DGIDL | - | 2.5 | Electric field exponent factor for gidl |
| DROUT | - | 0.2 | L dependence coefficient of the DIBL correction parameter in Rout |
| DSUB | - | 5 | DIBL coefficient exponent |
| DVT0 | - | 0 | First coefficient of the short-channel effect on Vth |
| DVT0W | - | 0 | First coefficient of the narrow width effect on Vth for a small channel length |
| DVT1 | - | 1 | Second coefficient of the short-channel effect on Vth |
| DVT1W | - | 5.3e6 | Second coefficient of the narrow width effect on Vth for a small channel length |
| DVT2 | 1/V | -0.032 | Body-bias coefficient of the short-channel effect on Vth |
| DVT2W | 1/V | -0.032 | Body-bias coefficient of the narrow width effect on Vth for a small channel length |
| DWB | m/V ^{1/2} | 0.0 | Coefficient of the substrate body bias dependence of Weff |
| DWBC | m | 0.0 | Width offset for the body contact isolation edge |
| DWG | m/V | 2.3e-8 | Coefficient of the gate dependence of Weff |
| ESATI | V/m | 1.e7 | Saturation channel electric field for the impact ionization current |
| ETA0 | - | 0 | DIBL coefficient in the subthreshold region |
| ETAB | 1/V | -0.07 | Body-bias coefficient for the DIBL effect in the subthreshold region |
| FBJTII | - | 0.0 | Fraction of the bipolar current affecting the impact ionization |

Chapter 2: MOSFET Models

LEVEL 71: TFT Model

| Parameter | Unit | Default | Description |
|-----------|------------------|---------|--|
| GGIDL | - | 6e-1 | Gate voltage coefficient for gidl |
| ISBJT | A/m ² | 1.4e-7 | BJT injection saturation current |
| ISDIF | A/m ² | 5e-5 | Body to source/drain injection saturation current |
| ISREC | A/m ² | 1.0e-5 | Recombination in the depletion saturation current |
| ISTUN | A/m ² | 0.0 | Reverse tunneling saturation current |
| K1 | V ^{1/2} | 0.35 | First-order body effect coefficient |
| K1W1 | m | 0 | First-order effect width dependent parameter |
| K1W2 | m | 0 | Second-order effect width dependent parameter |
| K2 | - | -2e-2 | Second-order body effect coefficient |
| K3 | - | 6e-4 | Narrow coefficient |
| K3B | 1/V | 0 | Body effect coefficient of k3 |
| KB1 | - | 1 | Backgate body charge coefficient |
| KETA | 1/V | -4.6e-2 | Body-bias coefficient of the bulk charge effect |
| KETAS | V | 0.0 | Surface potential adjustment for the bulk charge effect |
| KG | - | 1 | Offset voltage for gate induced grain boundary barrier lowering |
| LBJT0 | m | 1.3e-7 | Reference channel length for the bipolar current |
| LII | - | 2.8e-6 | Channel length dependence parameter for the impact ionization current |
| LINT | m | 0.0 | Length offset fitting parameter from I-V without bias |
| LGB1 | - | 1e-2 | Grain boundary factor inducing effective channel length decrease |
| LGB2 | - | 7e-4 | Depletion near grain boundary inducing effective channel length decrease |
| LGB3 | - | 2e-2 | Gate voltage factor for effective channel length |
| LN | m | 1.8e-6 | Electron/hole diffusion length |

| Parameter | Unit | Default | Description |
|-----------|--------------------|---------|--|
| NBJT | - | 1.3 | Power coefficient of the channel length dependency for the bipolar current |
| NDIO | - | 0.5 | Diode non-ideality factor |
| NLN | - | 2 | Channel length exponent for amplification coefficient of parasitic BJT |
| NFACTOR | - | 20 | Subthreshold swing factor |
| NGIDL | V | -22 | GIDL Vds enhancement coefficient |
| NLX | m | 1.5e-6 | Lateral non-uniform doping parameter |
| NRECF0 | - | 2.0 | Recombination non-ideality factor at the forward bias |
| NRECR0 | - | 10 | Recombination non-ideality factor at the reversed bias |
| NTUN | - | 10.0 | Reverse tunneling non-ideality factor |
| PCLM | - | 9e-4 | Channel length modulation parameter |
| PDIBLC1 | - | 1 | Correction parameter for the DIBL effect of the first output resistance |
| PDIBLC2 | - | 1.5e-3 | Correction parameter for the DIBL effect of the second output resistance |
| PRWB | 1/V | -7.7e-7 | 0 |
| PRWG | 1/V ^{1/2} | -1e-2 | Gate-bias effect coefficient of Rds _w |
| PVAG | - | 5.6e2 | Gate dependence of the Early voltage |
| RBODY | ohm/m ² | 0.0 | Intrinsic body contact sheet resistance |
| RBSH | ohm/m ² | 0.0 | Extrinsic body contact sheet resistance |
| RDSW | ohm/m ² | 7e4 | Parasitic resistance per unit width |
| RSH | ohm/ square | 0.0 | Source/drain sheet resistance in ohm per square |
| SII0 | 1/V | 0.37 | First V _{gs} dependence parameter for the impact ionization current |

Chapter 2: MOSFET Models

LEVEL 71: TFT Model

| Parameter | Unit | Default | Description |
|-----------|--------------------------|------------------------|--|
| SII1 | 1/V | 0.08 | Second Vgs dependence parameter for the impact ionization current |
| SII2 | 1/V | 0.08 | Third Vgs dependence parameter for the impact ionization current |
| SIID | 1/V | 5e-3 | Vds dependence parameter of the drain saturation voltage for the impact ionization current |
| TII | - | 0 | Temperature dependence parameter for the impact ionization current |
| U0 | cm ² /(V-sec) | NMOS-600 PMOS-200 | Mobility at Temp=Tnom |
| UA | m/V | 9.6e-9 | First-order mobility degradation coefficient |
| UB | (m/V) ² | 1e-21 | Second-order mobility degradation coefficient |
| UC | 1/V | -4e-11 | Body-effect of the mobility degradation coefficient |
| UG | m ² /(V-sec) | 9e-2 | Grain boundary barrier scattering mobility at Temp=Tnom |
| VABJT | V | 10 | Early voltage for the bipolar current |
| VDSATII0 | V | 0.6 | Nominal drain saturation voltage at threshold for the impact ionization current |
| VECB | v | 0.026v | Electron tunneling from the conduction band |
| VEVB | v | 0.075v | Electron tunneling from the valence band |
| VOFF | v | -0.6 | Offset voltage in the subthreshold region for large W and L values |
| VREC0 | V | 0.0 | Voltage dependent parameter for the recombination current |
| VSAT | m/sec | 5e5 | Saturation velocity at Temp=Tnom |
| VTH0 | v | NMOS 0.7 PMOS - 0.7 | Threshold voltage @ Vbs=0 for a long, wide device |
| VTUN0 | V | 0.0 | Voltage dependent parameter for the tunneling current |
| W0 | m | 2.5e-5 | Narrow width parameter |

| Parameter | Unit | Default | Description |
|-----------|------|---------|--|
| WINT | m | 0.0 | Width offset fitting parameter from I-V without bias |
| WR | - | 0.8 | Width offset from Weff for the Rds calculation |

TFT Model — AC and Capacitance Parameters

| Parameter | Unit | Default | Description |
|-----------|------------------|---------|---|
| ACDE | m/V | 1.0 | Exponential coefficient for the charge thickness in the CapMod=3 for the accumulation and depletion regions |
| ASD | V | 0.3 | Smoothing parameter for the source/drain bottom diffusion |
| CF | F/m | cal. | Fringing field capacitance of the gate-to-source/drain |
| CGDL | F/m | 0.0 | Overlap capacitance for the lightly-doped drain-gate region |
| CGDO | F/m | 0 | Non LDD region drain-gate overlap capacitance per channel length |
| CGEO | F/m 0 | Gate | Substrate overlap capacitance per unit channel length |
| CGSL | F/m | 0.0 | Overlap capacitance for the lightly-doped source-gate region |
| CGSO | F/m | cal. | Calculated Non LDD region source-gate overlap capacitance per channel length |
| CJSWG | F/m ² | 1.e-10 | Source/drain (gate side) sidewall junction capacitance per unit width (normalized to 100nm Ts) |
| CKAPPA | F/m | 0.6 | Coefficient for the fringing field capacitance for the overlap capacitance in the lightly-doped region |
| CLC | m | 0.1e-7 | Constant term for the short-channel model |
| CLE | - | 0.0 | Exponential term for the short-channel model |
| CSDESCW | F/m | 0.0 | Fringing capacitance per unit length for the source/drain sidewall |
| CSDMIN | V | cal. | Minimum capacitance for the source/drain bottom diffusion |
| DELVT | V | 0.0 | Threshold voltage adjustment for C-V |
| DLBG | m | 0 | Length offset fitting parameter for the backgate charge |
| DLC | m | lint | Length offset fitting parameter for the gate charge |

Chapter 2: MOSFET Models

LEVEL 71: TFT Model

| Parameter | Unit | Default | Description |
|-----------|------------------|---------|---|
| DLCB | m | lint | Length offset fitting parameter for the body charge |
| DWC | m | wint | Width offset fitting parameter from C-V |
| FBODY | - | 1.0 | Scaling factor for the body charge |
| LDIF0 | - | 1 | Channel length dependency coefficient of the diffusion cap. |
| MJSWG | V | 0.5 | Grading coefficient of the source/drain (gate side) sidewall junction capacitance |
| MOIN | V ^{1/2} | 15.0 | Coefficient for the gate-bias dependent surface potential |
| NDIF | - | -1 | Power coefficient of the channel length dependency for the diffusion capacitance |
| PBSWG | V | 0.7 | Built-in potential of the source/drain (gate side) sidewall junction capacitance |
| TT | second | 1ps | Diffusion capacitance transit time coefficient |
| VSDFB | V | cal. | Flatband voltage for the source/drain bottom diffusion capacitance |
| VSDTH | V | cal. | Threshold voltage for the source/drain bottom diffusion capacitance |
| XPART | - | 0 | Charge partitioning rate flag |

TFT Model — Temperature Parameters

| Parameter | Unit | Default | Description |
|-----------|-----------|---------|--|
| AT | m/sec | 3.3e4 | Temperature coefficient for Ua |
| CTH0 | (W*S)/m°C | 0 | Normalized thermal capacity |
| KT1 | V | -0.11 | Temperature coefficient for the threshold voltage |
| KT2 | - | 0.022 | Body-bias coefficient of the threshold voltage temperature effect |
| KTIL | V*m | 0 | Channel length dependence of the temperature coefficient for the threshold voltage |
| NTRECF | - | 0 | Temperature coefficient for Nrecf |

| Parameter | Unit | Default | Description |
|-----------|------------------|--------------|--|
| NTRECR | - | 0 | Temperature coefficient for Nrecr |
| PRT | $\Omega - \mu m$ | 0 | Temperature coefficient for Rdsw |
| RTH0 | $m^\circ C/W$ | 0 | Normalized thermal resistance |
| TCJSWG | 1/K | 0 | Temperature coefficient of Cjswg |
| TNOM | $^\circ C$ | 25 | Temperature at which simulation expects parameters |
| TPBSWG | V/K | 0 | Temperature coefficient of Pbswg |
| UA1 | m/V | 4.31e-9 | Temperature coefficient for Ua |
| UB1 | $(m/V)^2$ | -7.61e-18 | Temperature coefficient for Ub |
| UC1 | 1/V | -0.056 | Temperature coefficient for Uc |
| UTE | - | -1.5 | Mobility temperature exponent |
| XBJT | - | 1 | Power dependence of jbjt on the temperature |
| XDIF | - | Same as XBJT | Power dependence of jdif on the temperature |
| XREC | - | 1 | Power dependence of jrec on the temperature |
| XTUN | - | 0 | Power dependence of jtun on the temperature |

TFT Model — Bias-Dependent Source (Rs) / Drain (Rd) Parameters

| Parameter | Unit | Default | Description |
|-----------|------------------|---------|--|
| CRD | Same as crs | | Coefficient of Rd due to gate and external drain bias |
| CRS | | 1.0 | Coefficient of Rs due to gate and external source bias |
| DELTAVGD | Same as deltavgs | | Smoothing parameter for RD dependence on VGD |
| DELTAVGS | - | 1.0e-4 | Smoothing parameter for RS dependence on VGS |
| ERDD | Same as erss | | External drain voltage dependent parameter in PRWDD |
| ERDG1 | Same as ersg1 | | Gate-bias dependent parameter in PRWGD |

Chapter 2: MOSFET Models

LEVEL 71: TFT Model

| Parameter | Unit | Default | Description |
|-----------|---------------|---------|---|
| ERDG2 | Same as ersg2 | | Gate-bias dependent parameter in PRWDD |
| ERSG1 | - | 1.0 | Gate-bias dependent parameter in PRWGS |
| ERSG2 | - | 1.0 | Gate-bias dependent parameter in PRWSS |
| ERSS | - | 1.0 | External source voltage dependent parameter in PRWSS |
| PRWBS | V^-0.5 | 0.0 | Body-bias dependence of LDD resistance in source side |
| PRWDB | Same as prwbs | | Body-bias dependence of LDD resistance in drain side |
| PRWDD | Same as prwss | | External drain-bias and gate-bias dependence of LDD resistance in drain side |
| PRWGD | Same as prwgs | | Gate-bias dependence of LDD resistance in drain side |
| PRWGS | V^-1 | 1.0 | Gate-bias dependence of LDD resistance in source side |
| PRWSS | V^-1 | 1.0 | External source-bias and gate-bias dependence of LDD resistance in source side |
| RDW | ohm(um)^wr | 100.0 | Zero bias lightly-doped drain resistance Rd(V) per unit width for RDMOD=1 |
| RDWMIN | ohm(um)^wr | 0.0 | Lightly-doped drain resistance per unit width at high Vgs and zero Vbs for RDMOD=1 |
| RDWMIN0 | Ohm | 0.0 | Drain resistance constant component |
| RSW | ohm(um)^wr | 100.0 | Zero bias lightly-doped source resistance Rs(V) per unit width for RSMOD=1 |
| RSWMIN | ohm(um)^wr | 0.0 | Lightly-doped source resistance per unit width at high Vgs and zero Vbs for RSMOD=1 |
| RSWMIN0 | Ohm | 0.0 | Source resistance constant component |
| WR | - | 0.0 | Width dependence exponent of lightly-doped source and drain resistance |

LEVEL 72: BSIM-CMG MOSFET Model

The BSIM-CMG model is a compact model to describe the behavior of multiple-gate MOSFET devices. There are two sub-modules for this HSPICE built-in model:

- SOIMG module for the BSIM-CMG SOI model
- BULKMG module for the BSIM-CMG BULK model

This model captures all important multi-gate transistor behaviors. The solution of Poisson's equation includes volume inversion; hence the subsequent I-V formulation automatically captures the volume inversion effect. Analysis of the electrostatic potential in the body of CMG MOSFETs provides the model equation for short channel effects (SCE). The short channel model also captures the extra electrostatic control from the top gate (tri-gate) or top/bottom gates (omega-gate or all-around-gate). The SCE model predicts the threshold (V_t) roll-off, drain-induced-barrier lowering (DIBL) and subthreshold slope degradation in close agreement with 2-D device simulation results.

Included in the model are other important effects such as: mobility degradation, multiple surface-orientations, velocity saturation, velocity overshoot, series resistance, channel length modulation, quantum mechanical effects, poly depletion, gate tunneling current, gate-induced-drain-leakage, and parasitic capacitance models.

Note: With version 105, the model name was renamed as BSIMMG; later it was changed back to BSIM-CMG with version 105.03.

See also: [Output Templates for BSIM-CMG, Level 72](#).

The following sections discuss these topics:

- [BSIM-CMG Model — General Syntax](#)
- [BSIM-CMG Model — Version Updates](#)
- [BSIM-CMG Model Parameters \(Version >= 105\)](#)
- [BSIM-CMG Model Parameters \(Version < 105\)](#)
- [BSIM-CMG Model \(Version=105.03\) — WPE Model Support](#)
- [BSIM-CMG Model — Deactivating Model Equations](#)
- [BSIM-CMG Model — Searching Models as Function of NFIN and L](#)

Chapter 2: MOSFET Models

LEVEL 72: BSIM-CMG MOSFET Model

- [BSIM-CMG Model — Binning Calculation](#)
 - [BSIM-CMG Model — Additional Operating Point Outputs](#)
-

BSIM-CMG Model — General Syntax

Syntax:

```
Mxxx nd ng ns [nb] mname [L=val] [M=val]
.model mname n(p)mos LEVEL=72 VERSION=val ...
```

Level 72 is the BSIM-CMG model in HSPICE. Before BSIM-CMG102, the model parameter TECHMOD=0 (default) was used for the BSIM-CMG BULK model and TECHMOD=1 for the BSIM-CMG SOI model. With BSIMCMG102, and going forward, use model parameter BULKMOD=1 (default) for the BSIM-CMG BULK model and BULKMOD=0 for the BSIM-CMG SOI model.

For example, to use the BSIM-CMG model in HSPICE, specify:

```
M1 drain gate source NCH L=1u
```

For the BSIM-CMG BULK model, specify NCH as:

```
.MODEL NCH NMOS LEVEL=72 VERSION=1.01 TECHMOD=0
.MODEL NCH NMOS LEVEL=72 VERSION=102 BULKMOD=1
```

For the BSIM-CMG SOI model, specify NCH as:

```
.MODEL NCH NMOS LEVEL=72 VERSION=1.01 TECHMOD=1
.MODEL NCH NMOS LEVEL=72 VERSION=102 BULKMOD=0
```

BSIM-CMG Model — Version Updates

This section covers the following topics:

- [BSIM-CMG 107.0 Updates](#)
- [BSIM-CMG 106.1.0 Updates](#)
- [BSIM-CMG 106 Updates](#)
- [BSIM-CMG 105.04 Updates](#)
- [BSIM-CMG 105.031 Updates](#)
- [BSIM-CMG 105.03 Updates](#)
- [BSIMMG 105 Updates](#)

- [BSIM-CMG 104.1](#)
- [BSIM-CMG 104.0](#)
- [BSIM-CMG 103 Updates](#)

BSIM-CMG 107.0 Updates

BSIM-CMG 107.0 implemented the following features:

- Long channel DIBL (also called Drain-Induced V_{th} Shift or DITS) was added and new parameters DVTP0 and DVTP1 were introduced.
- Average charge weighing factor was added through the new parameter CHARGEWF.
- Length scaling of SCE and SS were de-coupled and the new binnable parameter DVT1SS was introduced.
- A linear length scaling equation for PHIG was added.
- New NFIN scaling equations and parameters were added for the following parameters: PHIG, CDSC, CDSCD, CDSCDR, NBODY, VSAT, VSAT1, VSAT1R, U0.
- Temperature dependence on ETA0 and ETA0R was added.
- The default values of COVS and COVD were at the unrealistic value of 25 pF. The default values were set to zero.
- For CGEOMOD=1 only, CGEO1SW=1 now enables the parameters COVS, COVD, CGSP, and CGDP to be in F per fin per gate-finger per unit channel width. The default value of GEO1SW switch is zero.
- To be consistent with SOI, RTH and CTH equations in the self-heating sub-model were updated.
- The initial guess for the surface potential calculation was improved. The model is now infinitely scalable with respect to TFIN and NBODY without any clamping on NBODY.
- Unused model parameters NINTNOI and PINTNOI were removed.
- Minor updates in the technical manual including equations 3.332 and 3.334; the equations were updated in manual to be consistent with the code.
- Fix several bugs.

Chapter 2: MOSFET Models

LEVEL 72: BSIM-CMG MOSFET Model

BSIM-CMG 106.1.0 Updates

BSIM-CMG 106.1.0 implemented the following features:

- Two different expressions are adopted for $V_{fb\text{sd}}$ for Poly and Metal Gate, respectively.
- For gate current model, in order to decouple the oxide thickness used in I-V model (through the gate current) and C-V model and facilitate the model tuning, a new parameter, TOXG, is introduced and used in the gate tunneling current model. The default value of TOXG is equal to TOXP.
- For gate-induced source and drain leakage (GIDL/GISL), the model now retains zero current at zero bias and it is smooth with respect to bias. For BULKMOD=1, the singularity in the denominator of body-bias factor, $V_{de}^3 / (CGIDL + V_{de}^3)$, was removed and for $V_{de} > 0$ the GIDL is zero. Similar fixes were applied to GISL model.
- For temperature dependence of body effect model, lateral NUD model, and non-saturation effect model, the model parameters K1, K1SAT, K0, K0SI, A1, and A2 now have linear temperature dependency. For example, $K1_t = K1_i + K11_i * (T - TNOM)$.
- Modify temperature and length dependence of impact ionization current for iimod=2.
- Current (I_S) clamping in accumulation, I_{min} is now a model parameter with the default value of $1.0E-15$.
- Built-in $\cosh()$ overflow is added.
- Improve gate resistance model.
- NQSMOD=3 was disabled.
- The definitions of the physical intrinsic capacitances, CEDI and CEEI, were corrected.
- Threshold voltage definition is added.
- Fixed many bugs.

BSIM-CMG 106 Updates

BSIM-CMG 106 implemented the following features:

- Removed some unused source codes.
- Used built-in hyperbolic functions instead of macros.

- Added more significant digits to definition of electronic charge.
- Fixed some bugs.

BSIM-CMG 105.04 Updates

BSIM-CMG 105.04 implemented the following features:

1. GIDL Current Model modified. New parameter PGIDL/PGISL introduced and model retains zero current at zero bias.
2. Gate Current Model modified:
 - a. Default values of BIGBINV, AIGBACC, BIGBACC, NIGBACC were changed
 - b. Gate-to-Channel Current, Igcs/Igcd. Partition function implemented with parameter PIGCD (Binned).
3. Modification to the CLM Model:
 - a. Fixed discontinuity in implementation at PCLMG=0 for CLM Model
 - b. CLM Model for I-V Modified. Parameter VASAT removed. The old equation was known to cause unphysical “wiggles.”
4. ETAMOB binning corrected and linear temperature dependence added with new parameter EMOBT.
5. Velocity Saturation Model for better Id, sat and Gm, sat fitting.
6. Parameters DELTAVSAT, DVTSHIFT and KT1 are now binned.
7. DTEMP handle has been implemented.
8. CGEOMOD=0 case, removing QM effects in Fringe Caps.
9. Drain to Source Fringe Cap now available for all CGEOMOD.
10. Introduced DLCACC parameter for accumulation region capacitance (CAPMOD=1 and BULKMOD=1).
11. Velocity Saturation Model for Short Channel C-V introduced. New parameters VSATCV (binned) added.
12. CLM Model for C-V modified:
 - a. MclmCV factor simplified. Parameters VASATCV and PCLMGCV removed.
 - b. Corrected the wrong implementation of in the charge equations.
13. Added relevant equations for Short Channel CV.

Chapter 2: MOSFET Models

LEVEL 72: BSIM-CMG MOSFET Model

14. Parameter NFIN has been converted from integer to real to enable optimization.
15. Gate to Substrate Overlap cap scalability corrected. New parameter CGBN introduced.
16. Temperature Dependence for Subthreshold Swing enhanced with new parameter TSS (binned).
17. RDSMOD=1 is enhanced to capture quasi-saturation / current crowding for high voltage devices. New parameters RSDR, RDDR, PRSDR, PRDDR are introduced and new equations are added. Temperature dependence through TRSDR and TRDDR parameters.
18. Asymmetric Model - ASYMMOD Switch:
 - a. To model highly asymmetric devices, seven parameters in the model are identified and their reverse mode equivalents are created, such as CDSCDR, ETA0R, PDIBL1R, PTWGR, VSAT1R, RSDRR, and RDDRR.
 - b. Additionally, parameter PRWG is split into PRWGS and PRWDG for source and drain side in RDSMOD=1. However for RDSMOD=0, PRWGS takes over and replaces PRWG. PRWDG is not used.
19. Junction capacitance equations have been changed. The transition from standard junction capacitance equation to linear cap does not happen at $V_{es}=0$ / $V_{ed}=0$ (like BSIM4), but at $V_{es} = 0.9 * V_{bi}$ (built-in voltage of diode). This moves discontinuity in second derivative of capacitance far into forward bias where the device does not usually operate.
20. New parameters PHIBE, K1, K1ST, K1SAT are introduced for body Effect in BULKMOD=1.
21. Added more significant digits to definition of electronic charge from $1.6e-19$ to $1.60219e-19$ (Coulombs).
22. Quantum Mechanical Effects:
 - a. Introduced new parameter QMTCENCVA (binned) to replace QMTCENCV for the accumulation region capacitance.
 - b. Some bug fixes for variable 'Tcen' calculations in both inversion and accumulation region.
23. Introduced Non-saturation effect with new parameters A1 and A2. To be used to improve $I_{d,sat}$ and $G_{m,sat}$ fitting.
24. Lateral NUD Model introduced to create IV-CV Vth shift.
25. Fixed many bugs.

BSIM-CMG 105.031 Updates

BSIM-CMG 105.031 implemented the following features:

1. GIDL Current model modified for zero current at zero bias. This update introduced the equation around parameter CGIDL/CGISL (binned) from BSIM4 for BULKMOD=1. For BULKMOD=0, CGIDL/CGISL parameters are not used.
2. Gate Current Model (igcs/igcd, igs/igd) has been modified. Partition function implemented with parameter PIGCD (Binned).
3. Removed CLM effect in Charge model due to faulty implementation.
4. Fixed discontinuity in implementation at PCLMG=0 for CLM model.

BSIM-CMG 105.03 Updates

BSIM-CMG 105.03 implemented the following features.

1. Restored the name BSIM-CMG from its change to BSIMMG (see [BSIMMG 105 Updates](#))
2. Added PCLMG, VASAT, and ETAMOB to the list of binnable parameters
3. Introduced DLBIN, an 'L' offset parameter for binning.
4. Introduced the DVTSHIFT parameter as a handle to create Vth shift.
5. This release replaces all older mobility models with a single new mobility model. The new mobility model uses UA, EU, UD, and UCS parameters from MOBMOD=0 of 105.02 release.
6. This version adds a New Velocity Saturation (Ion degradation) model. Parameters VSAT1 (binned) and DELTAVSAT replace the old parameter THETASAT. This is a backward *incompatible* change In BSIMMG105 alpha2.
7. Changed the RDSMOD=0 implementation for better accuracy.
8. Modified the CLM Model to prevent cross-correlation of binning parameters.
9. Added an Igb accumulation component for IGBMOD=1.
10. Changed the Vds asymmetric function for better higher order derivative predictability.

Chapter 2: MOSFET Models

LEVEL 72: BSIM-CMG MOSFET Model

BSIMMG 105 Updates

BSIMMG v.105 implemented the following features.

1. Implemented the new geometry-dependent FinFET source/drain resistance model `RGEOMOD=1` for the purpose of variability modeling.
2. Implemented a new geometry-dependent FinFET outer fringe capacitance model `CGEOMOD=1` for the purpose of variability modeling.
3. Implemented a bias-dependent overlap capacitance model (adapted from BSIM4).
4. SOI multi-gate devices (`BULKMOD=0`) now support 4 terminals only.
5. Changed the formulation for current degradation due to velocity saturation in the linear region.
6. Changed the definitions of `AS`, `AD`, `PS`, `PD` for consistency with BSIM4: `ASEO`, `ADEO`, `PSEO`, `PDEO` now refers to the total source/drain area or perimeter rather than the per-finger value. `AS` is separated into a junction portion only for bulk multi-gate (`ASEJ`, `PSEJ`) and a oxide portion (`ASEO`, `PSEO`). `AD` is separated into `ADEJ`, `PDEJ`, `ADEO` and `PDEO`.
7. Implemented Source/drain to substrate capacitance for both `BULKMOD=0, 1`, controlled by parameters `ASEO`, `ADEO`, `PSEO`, `PDEO`, and `CSDESW`.
8. The model now distinguishes `toxe` (electrical oxide thickness) and `toxp` (physical oxide thickness). `DEOT` is a new parameter that represents the oxide-equivalent thickness of the inversion layer. For backward compatibility with BSIM-CMG 104, set `DEOT=0`.
9. New I-V and C-V model.
10. QM Model changes: `Weff/Toxeff` equations changed and correct version introduced. Introduced model parameters `QMTCENIV` and `QMTCENCV` (quasi-switches) to independently turn on/off `Weff` correction for IV and CV, and `coxeff` correction for CV.
11. Accumulation Capacitance added. `CAPMOD=1` turns on additional Surface potential computation required and stamps accumulation charge too. Currently allowed only for `BULKMOD=1` case.
12. Added gate sidewall junction capacitances and currents.
13. Separated `GMOD` into `IGBMOD` and `IGCMOD`
14. Renamed BSIMCMG to BSIMMG.
15. Added `Igb` for SOI multi-gate devices (`BULKMOD=0`). (Previously, `Igb` was only calculated for bulk multi-gate devices.)

16. Added BSIM4 style NQS model. `NQSMOD=2`.
17. Added New Charge segmentation based NQS model. `NQSMOD=3`.
18. Fixed many bugs.

BSIM-CMG 104.1

BSIM-CMG 104.1 implemented the following features:

1. Asymmetric DIBL parameters supported.
2. Bulk-Charge is made bias independent through correct implementation.
3. `CLMMOD=1` case replaced with newer model.
4. Many bug fixes were implemented.

BSIM-CMG 104.0

BSIM-CMG 104 implemented the following features:

1. Channel length modulation model `CLMMOD=1` is added based on the BSIM4 formulation.
2. Instance parameters `NRS` and `NRD` and associated equations are added based on the BSIM4 formulation.
3. The equations associated with parameter `PVAG` are modified to provide more flexibility for output conductance fitting.
4. Added a New Impact Ionization Current Model and Model Switch `IIMOD`; BSIM4 based `Iii` model into `IIMOD=1` block and BSIM SOI based `Iii` model into `IIMOD=2` block.
5. Improved the Gate Electrode Resistance Model; introduced new parameters `RGEXT` and `RGFIN` and removed parameter `RGELTD`.
6. Changed the Internal Resistance formula.
7. Implemented many bug fixes.

BSIM-CMG 103 Updates

BSIM-CMG 103 implemented the following features:

1. This release supports a Cylindrical gate geometry through `GEOMOD = 3` with an associated short channel scale length and quantum effects model.
2. The existing I-V has been enhanced to model Poly-depletion accurately.
3. Self-heating is now supported with addition of a Temperature node.

Chapter 2: MOSFET Models

LEVEL 72: BSIM-CMG MOSFET Model

4. Junction Capacitance and Junction Current equations were revamped with source-drain asymmetry supported. The asymmetry is now also in GIDL/ GISL currents.
5. Length-dependent equations have been added for a Global Parameter Extraction without binning.
6. SHMOD, RGATEMOD, NQSMOD and RDMSMOD also control the number of internal nodes for faster simulations.
7. Many bug fixes were implemented.

BSIM-CMG Model Parameters (Version >= 105)

Note: The name BSIMMMG is the same as BSIM-CMG and refers to the same model; from version 105.03 the model name (BSIMMMG) was reverted to BSIM-CMG, its original name.

This section covers the following topics:

- [BSIM-CMG Model \(Version>=105\) — Instance Parameters](#)
- [BSIM-CMG Model \(Version>=105\) — Control and Process Parameters](#)
- [BSIM-CMG Model \(Version>=105\) — Basic Model Parameters](#)
- [BSIM-CMG Model \(Version>=105\) — Geometry Dependent Parasitic Parameters](#)
- [BSIM-CMG Model \(Version>=105\) — Temperature Dependent and Self-Heating Parameters](#)

BSIM-CMG Model (Version>=105) — Instance Parameters

Note: Binnable parameters are marked as ^(b). Instance parameters which are also model parameters are marked as ^(m).

| Parameter | Unit | Default | Min | Max | Description |
|---------------------|----------------|---------|-----|-----|--|
| ADEJ ^(m) | m ² | 0 | 0 | - | Drain junction area (all fingers; for bulk MuGFETs, BULKMOD = 1) |
| ADEO ^(m) | m ² | 0 | 0 | - | Drain to substrate overlap area through oxide (all fingers) |

| Parameter | Unit | Default | Min | Max | Description |
|-----------------------|----------------------------|---------|------|-----|---|
| ASEJ ^(m) | m ² | 0 | 0 | - | Source junction area (all fingers; for bulk MuGFETs, BULKMOD = 1) |
| ASEO ^(m) | m ² | 0 | 0 | - | Source to substrate overlap area through oxide (all fingers) |
| CDSP ^(m) | F | 0 | 0 | - | Constant drain to source fringe capacitance (for CGEOMOD = 1) |
| CGDP ^(m) | F | 0 | 0 | - | Constant gate to drain fringe capacitance (for CGEOMOD = 1) |
| CGSP ^(m) | F | 0 | 0 | - | Constant gate to source fringe capacitance (for CGEOMOD = 1) |
| COVS ^(m) | For F/m, see CGEO1SW | 0 | 0 | - | Constant gate to source overlap capacitance (for CGEOMOD = 1) |
| COVD ^(m) | For F/m, see CGEO1SW | 0 | 0 | - | Constant gate to drain overlap capacitance (for CGEOMOD = 1) |
| D ^(m) | m | 40n | 1n | - | Diameter of cylinder (for GEOMOD = 3) |
| FPITCH ^(m) | m | 80n | TFIN | - | Fin pitch |
| L ^(m) | m | 30n | 1n | - | Designed gate length |
| LRSD ^(m) | m | L | 0 | - | Length of the source/drain |
| NF | - | 1 | 1 | - | Number of fingers |
| NFIN ^(m) | - | 1 | >0 | - | Number of fins per finger |
| NGCON ^(m) | - | 1 | 1 | 2 | Number of gate contacts |
| NRD ^(m) | - | 0 | 0 | - | Number of drain diffusion squares (for RGEOMOD = 0) |
| NRS ^(m) | - | 0 | 0 | - | Number of source diffusion squares (for RGEOMOD = 0) |
| PDEO ^(m) | m | 0 | 0 | - | Perimeter of drain to substrate overlap region through oxide (all fingers) |
| PSEO ^(m) | m | 0 | 0 | - | Perimeter of source to substrate overlap region through oxide (all fingers) |

Chapter 2: MOSFET Models

LEVEL 72: BSIM-CMG MOSFET Model

| Parameter | Unit | Default | Min | Max | Description |
|---------------------|----------|---------|-----|-----|--|
| PDEJ ^(m) | m | 0 | 0 | - | Drain junction perimeter (all fingers; for bulk MuGFETs, BULKMOD = 1) |
| PSEJ(m) | m | 0 | 0 | - | Source junction perimeter (all fingers; for bulk MuGFETs, BULKMOD = 1) |
| RDC | Ω | 0 | - | - | Drain contact resistance for per-finger device |
| RSC | Ω | 0 | - | - | Source contact resistance for per-finger device |
| TFIN ^(m) | m | 15n | 1n | - | Body (fin) thickness |

BSIM-CMG Model (Version>=105) — Control and Process Parameters

| Parameter | Unit | Default | Min | Max | Description |
|-----------|------|---------|------|------|---|
| VERSION | - | 106.1 | - | - | Model version number |
| DEVTYPE | - | NMOS | PMOS | NMOS | NMOS=1, PMOS=0 |
| ASYMMOD | - | 0 | 0 | 1 | Asymmetric I-V model selector 0 = turn off, reverse mode parameters ignored, 1 = turn on |
| BULKMOD | - | 0 | 0 | 1 | Substrate model selector. 0 = multi-gate on SOI substrate, 1 = multi-gate on bulk substrate |
| CGEO1SW | - | 0 | 0 | 1 | For CGEOMOD=1 only, GEO1SW=1 enables the parameters COVS, COVD, CGSP, and CGDP to be in F per n, per gate-finger, per unit channel width. |
| COREMOD | - | 0 | 0 | 1 | Simplified surface potential solution; 0=Turn off, 1= Turn on (lightly-doped or undoped) |
| GEOMOD | - | 1 | 0 | 3 | Structure selector; 0=double gate, 1=triple gate, 2=quadruple gate, 3=cylindrical gate |
| MOBMOD | - | 0 | 0 | 1 | Mobility model selector 0 = BSIM-based, 1 = PSP-based |
| RDSMOD | - | 0 | 0 | 1 | Bias-dependent source/drain resistance model selector (controls <i>si</i> and <i>di</i> nodes); 0 = internal, 1 = external |

| Parameter | Unit | Default | Min | Max | Description |
|-----------|------|---------|-----|-----|--|
| IGCMOD | - | 0 | 0 | 1 | Model selector for I_{gc} , I_{gs} , and I_{gd} ; 1=turn on, 0=turn off |
| IGBMOD | - | 0 | 0 | 1 | Model selector for I_{gb} ; 1=turn on, 0=turn off |
| GIDLMOD | - | 0 | 0 | | GIDL/GISL current switcher; 1=on, 0=off |
| IIMOD | - | 0 | | | Impact ionization model switch; 0 = OFF, 1 =BSIM4 based, 2 = BSIMSOI based |
| NQSMOD | - | 0 | 0 | 1 | NQS gate resistor and gi node switcher; 1=on, 0=off |
| SHMOD | - | 0 | 0 | 1 | Self-heating and T node switcher; 1=on, 0=off |
| RGATEMOD | - | 0 | | 1 | Gate electrode resistor and ge node switcher; 1=on, 0=off |
| RGEOMOD | - | 0 | 0 | 1 | Bias independent parasitic resistance model selector |
| CGEOMOD | - | 0 | 0 | 2 | Parasitic capacitance model selector; 1=on, 0=off |
| CAPMOD | - | 0 | 0 | 1 | accumulation region capacitance model selector; 0=no accumulation capacitance, 1=accumulation capacitance included |
| BG0SUB | eV | 1.12 | - | - | Band gap of the channel material at 300.15K |
| DELTAW | m | 0.0 | - | - | Reduction of effective width due to shape of fin |
| DELTAWCV | m | 0.0 | - | - | CV reduction of effective width due to shape of fin |
| DLC | m | 0.0 | - | - | Length reduction parameter for CV (dopant diffusion effect) |
| DLCACC | m | 0.0 | - | - | Length reduction parameter for CV in accumulation region (BULKMOD =1; CAPMOD = 1) |
| EASUB | eV | 4.05 | 0 | - | Electron affinity of the substrate material |

Chapter 2: MOSFET Models

LEVEL 72: BSIM-CMG MOSFET Model

| Parameter | Unit | Default | Min | Max | Description |
|----------------------|---------------|---------|------|------|---|
| EOT | m | 1.0n | 0.1n | - | SiO_2 equivalent gate dielectric thickness (including inversion layer thickness) |
| EOTBOX | m | 140n | 1n | - | SiO_2 equivalent buried oxide thickness |
| EPSROX | - | 3.9 | 1 | 0 | Relative dielectric constant of the gate insulator |
| EPSRSUB | - | 11.9 | 1 | - | Relative dielectric constant of the channel material |
| FECH | - | 1.0 | 0 | - | End-channel factor, for different orientation/shape; mobility difference between the side channel and the top channel is handled by this parameter. |
| FECHCV | - | 1.0 | 0 | - | CV end-channel factor, for different orientation/shape; (Mobility difference between the side channel and the top channel is handled by this parameter) |
| HFIN | m | 30n | 1n | - | Fin height; instance parameter, also |
| LINT | m | 0.0 | - | - | Length reduction parameter (dopant diffusion effect) |
| LL | $m^{(LLN+1)}$ | 0.0 | - | - | Length reduction parameter (dopant diffusion effect) |
| LLC | $m^{(LLN+1)}$ | 0.0 | - | - | Length reduction parameter for CV (dopant diffusion effect) |
| LLN | - | 1.0 | - | - | Length reduction parameter (dopant diffusion effect) |
| NBODY ^(b) | m^{-3} | 1e22 | 1e18 | 5e24 | Channel doping concentration; model currently supports NBODY < $5 \times 10^{24} m^{-3}$; for larger values use BSIM4 or BSIM4SOI |
| NC0SUB | m^{-3} | 2.86e25 | - | - | Conduction band density of states at 300.15K |
| NGATE ^(b) | m^{-3} | 0 | - | - | Parameter for Poly Gate doping; =0 for metal gate; Set NGATE = 0 for metal gates |
| NI0SUB | m^{-3} | 1.1e16 | - | - | Intrinsic carrier concentration of channel at 300.15K |

| Parameter | Unit | Default | Min | Max | Description |
|---------------------|------------------|---------|------|------|--|
| NSD | m ⁻³ | 2e26 | 2e25 | 1e27 | S/D doping concentration |
| PHIG ^(b) | eV | 4.61 | 0 | - | Work function of gate |
| TOXP | m | 1.2n | 0.1n | - | Physical oxide thickness |
| XL | m | 0 | - | - | L offset for channel length due to mask/etch effect |
| Imin | A/m ² | 1E-15 | - | - | Parameter for voltage clamping for inversion region calculation in accumulation. |

BSIM-CMG Model (Version>=105) — Basic Model Parameters

Note: Binnable parameters are marked with ^(b).

| Name | Unit | Default | Min | Max | Description |
|------------------------|---------------------------------|-----------|-----|-----|--|
| A1 ^(b) | V ⁻² | 0.0 | - | - | Non-saturation effect parameter in strong inversion region |
| A2 ^(b) | V ⁻¹ | 0.0 | - | - | Non-saturation effect parameter in moderate inversion region |
| AGIDL ^(b) | Ω^1 | 6.055e-12 | - | - | Pre-exponential coefficient for GIDL |
| AGISL ^(b) | Ω^1 | AGIDL | - | - | Pre-exponential coefficient for GISL |
| AIGBACC ^(b) | $(Fs^2 / g)^{0.5} m^{-1}$ | 1.36e-2 | - | - | Parameter for lgb in accumulation |
| AIGBINV ^(b) | $(Fs^2 / g)^{0.5} m^{-1}$ | 1.11e-2 | - | - | Parameter for lgb in inversion |
| AIGC ^(b) | $(Fs^2 / g)^{0.5} m^{-1}$ | 1.36e-2 | - | - | Parameter for lgc in inversion |
| AIGD ^(b) | $(Fs^2 / g)^{0.5} m^{-1}$ | 1.36e2 | - | - | Parameter for lgd in inversion |
| AIGEN ^(b) | m ⁻³ V ⁻¹ | 0.0 | - | - | Parameter for R/G current (Experimental) |
| AIGS ^(b) | $(Fs^2 / g)^{0.5} m^{-1}$ | 1.36e2 | - | - | Parameter for lgs in inversion |

Chapter 2: MOSFET Models

LEVEL 72: BSIM-CMG MOSFET Model

| Name | Unit | Default | Min | Max | Description |
|--------------------------------------|----------------------------------|---------|-----|-----|--|
| ALPHA0 ^(b) | $m \cdot V^{-1}$ | 0.0 | - | - | First parameter of I _{II} (IIMOD=1) |
| ALPHA1 ^(b) | V ⁻¹ | 0.0 | - | - | L scaling parameter of I _{II} (IIMOD=1) |
| ALPHAI _{II} ^(b) | - | 0.0 | - | - | Pre-exponential constant for I _{II} (IIMOD=2) |
| BETA0 ^(b) | V ⁻¹ | 0.0 | - | - | V _{DS} dependent parameter of I _{II} (IIMOD=1) |
| BETAI _{II} 0 ^(b) | V ⁻¹ | 0.0 | - | - | V _{DS} dependent parameter of I _{II} (IIMOD=2) |
| BETAI _{II} 1 ^(b) | - | 0.0 | - | - | V _{DS} dependent parameter of I _{II} (IIMOD=2) |
| BETAI _{II} 2 ^(b) | V | 0.1 | - | - | V _{DS} dependent parameter of I _{II} (IIMOD=2) |
| BGIDL ^(b) | V/m | 0.3e9 | - | - | Exponential coefficient for GIDL |
| BGISL ^(b) | V/m | BGIDL | | | Exponential coefficient for GISL |
| BIGBACC ^(b) | $(Fs^2 / g)^{0.5} m^{-1} V^{-1}$ | 1.71e-3 | - | - | Parameter for Ig _b in accumulation |
| BIGBINV ^(b) | $(Fs^2 / g)^{0.5} m^{-1} V^{-1}$ | 9.49e-4 | - | - | Parameter for Ig _b in inversion |
| BIGC ^(b) | $(Fs^2 / g)^{0.5} m^{-1} V^{-1}$ | 1.71e-3 | - | - | Parameter for Ig _c in inversion |
| BIGS ^(b) | $(Fs^2 / g)^{0.5} m^{-1} V^{-1}$ | 1.71e-3 | - | - | Parameter for Ig _s in inversion |
| BIGD ^(b) | $(Fs^2 / g)^{0.5} m^{-1} V^{-1}$ | BIGS | - | - | Parameter for Ig _d in inversion |
| BIGEN ^(b) | $m^{-3} V^{-3}$ | 0.0 | | - | Parameter for R/G current (Experimental) |
| BVD | V | BVS | | | Drain diode breakdown voltage |
| BVS | V | 10.0 | | | Source diode breakdown voltage |
| CDSC ^(b) | F/m ² | 7e-3 | 0.0 | - | Coupling capacitance between S/D and channel |

| Name | Unit | Default | Min | Max | Description |
|----------------------|------------------|------------|-------|-----|--|
| CDSCD ^(b) | F/m ² | 7e-3 | 0.0 | - | Drain-bias sensitivity of CDSC |
| CDSCDN1 | - | 0 | -0.08 | - | NFIN dependence of CDSCD |
| CDSCDN2 | - | 1e5 | 1e-5 | - | NFIN dependence of CDSCD |
| CDSCDRN1 | - | CDSCDN1 | -0.08 | - | NFIN dependence of CDSCDR |
| CDSCDRN2 | - | CDSCDN2 | 1e-5 | - | NFIN dependence of CDSCDR |
| CDSCN1 | - | 0 | -0.08 | - | NFIN dependence of CDSC |
| CDSCN2 | - | 1e5 | 1e-5 | - | NFIN dependence of CDSC |
| CFD ^(b) | F/m | CFS | 0.0 | - | Drain-side outer fringe cap (for CGEOMOD = 0) |
| CFS ^(b) | F/m | 2.5e-11 | 0.0 | - | Source-side outer fringe cap (for parasitic capacitance calculation) |
| CGBN | F/m | 0 | 0.0 | - | Gate-substrate overlap capacitance per unit channel length per finger per fin |
| CGBO | F/m | 0 | 0.0 | - | Gate-substrate overlap capacitance per unit channel length per finger per gate contact |
| CGDL ^(b) | F/m | CGSL | 0.0 | - | Overlap capacitance between gate and lightly-doped drain region (for CGEOMOD = 0, 2) |
| CGDO | F/m | calculated | 0.0 | - | Non LDD region drain-gate overlap capacitance per unit channel width (for CGEOMOD = 0, 2) |
| CGIDL ^(b) | V ³ | 0.2 | - | - | Parameter for body bias effect of GIDL |
| CGSL ^(b) | F/m | 0 | 0.0 | - | Overlap capacitance between gate and lightly-doped source region (for CGEOMOD = 0, 2) |
| CGSO | F/m | calculated | 0.0 | - | Non LDD region source-gate overlap capacitance per unit channel width (for CGEOMOD = 0, 2) |

Chapter 2: MOSFET Models

LEVEL 72: BSIM-CMG MOSFET Model

| Name | Unit | Default | Min | Max | Description |
|------------------------|------------------|---------|------|-----|--|
| CHARGEWF | - | 0 | -1 | 1 | Average channel charge weighting (sampling) factor, +1: source-side, 0: middle, -1: drain-side |
| CIGBACC ^(b) | V ⁻¹ | 7.5e-2 | - | - | Parameter for lgb in accumulation |
| CIGBINV ^(b) | V ⁻¹ | 6.00e-3 | - | - | Parameter for lgb in inversion (BULKMOD only) |
| CIGC ^(b) | V ⁻¹ | 0.075 | - | - | Parameter for lgc in inversion |
| CIGD ^(b) | V ⁻¹ | CIGD | - | - | Parameter for lgd in inversion |
| CIGS ^(b) | V ⁻¹ | 0.075 | - | - | Parameter for lgs in inversion |
| CIT ^(b) | F/m ² | 0.0 | - | - | Parameter for interface trap |
| CJD | F/m ² | CJS | 0.0 | - | Unit area drain-side junction capacitance at zero bias |
| CJS | F/m ² | 0.0005 | 0.0 | - | Unit area source-side junction capacitance at zero bias |
| CJSWD | F/m | CJSWS | 0.0 | - | Unit length sidewall junction capacitance at zero bias (drain-side) |
| CJSWS | F/m | 5.0e-10 | 0.0 | - | Unit length sidewall junction capacitance at zero bias (source-side) |
| CJSWGD | F/m | CJSWS1 | 0.0 | - | Unit length gate sidewall junction capacitance at zero bias (drain-side) |
| CJSWGS | F/m | 0.0 | 0.0 | - | Unit length gate sidewall junction capacitance at zero bias (source-side) |
| CKAPPAD ^(b) | V | CKAPPAS | 0.02 | - | Coefficient of bias-dependent overlap capacitance for the drain side (for CGEOMOD = 0, 2) |
| CKAPPAS ^(b) | V | 0.6 | 0.02 | - | Coefficient of bias-dependent overlap capacitance for source side (for CGEOMOD = 0, 2) |

| Name | Unit | Default | Min | Max | Description |
|--------------------------|------|---------|------|-----|--|
| COVD ^(b) | F/m | COVS | 0.0 | - | Constant gate-to-drain overlap cap (for CGEOMOD = 1) |
| COVS ^(b) | F/m | 0 | 0.0 | - | Constant gate-to-source overlap cap (for CGEOMOD = 1) |
| CSDESW | F/m | 0 | 0.0 | - | Source/drain sidewall fringing capacitance per unit length |
| DELTAVSAT ^(b) | - | 1.0 | 0.01 | - | Velocity saturation parameter in the linear region |
| DELVFBACC | V | 0.0 | - | - | Additional V_{fb} shift required for accumulation region |
| DLCIGD | m | DLCIGS | - | - | Delta L for IgD model |
| DLCIGS | m | 0 | - | - | Delta L for IgS model |
| DROUT ^(b) | | 1.06 | >0.0 | - | L dependence of DIBL effect on Rout |
| DSUB ^(b) | - | 1.06 | >0 | - | DIBL exponent coefficient |
| DVT0 ^(b) | - | 0.0 | 0.0 | - | SCE coefficient |
| DVT1 ^(b) | - | 0.60 | >0 | - | SCE exponent coefficient |
| DVTP0 | - | 0 | - | - | Coefficient for Drain-Induced Vth Shift (DITS) |
| DVTP1 | - | 0 | - | - | DITS exponent coefficient |
| DVTSHIFT | V | 0.0 | 0.0 | - | Additional Vth shift handle |
| DVT1SS ^(b) | - | DVT1 | >0 | - | Subthreshold Swing exponent coefficient |
| EF | - | 1.0 | >0.0 | 2.0 | Flicker noise frequency exponent |
| EGIDL ^(b) | V | 0.2 | - | - | Band bending parameter for GIDL |
| EGISL ^(b) | V | EGIDL | - | - | Band bending parameter for GISL |

Chapter 2: MOSFET Models

LEVEL 72: BSIM-CMG MOSFET Model

| Name | Unit | Default | Min | Max | Description |
|------------------------|------------------|----------|---------------------|-----|---|
| EIGBINV ^(b) | V | 1.1 | - | - | Parameter for lgb in inversion (BULKMOD only) |
| EM | V/m | 4.1e7 | - | - | Flicker noise parameter |
| EOTACC | m | EOT | 0.1n | - | $S_i O_2$ equivalent gate dielectric thickness for accumulation region |
| ESATII ^(b) | V/m | 1.0e7 | - | - | Saturation channel E-Field for lii (IMOD=2) |
| ETA0 ^(b) | - | 0.60 | 0.0 | - | DIBL coefficient |
| ETAMOB ^(b) | - | 2.0 | - | - | Effective field parameter |
| ETAQM | - | 0.54 | - | - | Body-charge coefficient for QM charge centroid |
| EU ^(b) | cm/MV | 0.3 | >0.0 | - | Phonon / surface roughness scattering parameter |
| IJTHSREV | A | 0.1 | 10 I _{sbs} | - | Reverse source diode breakdown limiting current |
| IJTHDFWD | A | IJTHSFWD | 10 I _{sbs} | - | Forward drain diode breakdown limiting current |
| IJTHSFWD | A | 0.1 | 10 I _{sbs} | - | Forward source diode breakdown limiting current |
| IJTHDREV | A | IJTHSREV | | | Reverse drain diode breakdown limiting current |
| JSD | A/m ² | JSS | 0.0 | - | Bottom drain junction reverse saturation current density |
| JSS | A/m ² | 1.0e-4 | 0.0 | - | Bottom source junction reverse saturation current density |
| JSWD | A/m | JSWS | 0.0 | - | Unit length reverse saturation current for isolation-edge sidewall drain junction |
| JSWGD | A/m | JSWGS | 0.0 | - | Unit length reverse saturation current for isolation-edge sidewall drain junction |

Chapter 2: MOSFET Models
LEVEL 72: BSIM-CMG MOSFET Model

| Name | Unit | Default | Min | Max | Description |
|-----------------------|-------------------|---------|------------|-------------|--|
| JSWGS | A/m | 0 | 0.0 | - | Unit length reverse saturation current for isolation-edge sidewall source junction |
| JSWS | A/m | 0 | 0.0 | - | Unit length reverse saturation current for isolation-edge sidewall source junction |
| JTSD | A/m ² | JTSS | 0.0 | - | Bottom drain junction trap-assisted saturation current density |
| JTSS | A/m ² | 1.0e-4 | 0.0 | - | Bottom source junction trap-assisted saturation current density |
| K0(b) | V | 0.0 | - | - | Lateral NUD parameter |
| K0SI(b) | - | 1.0 | >0 | - | Correction factor for strong inversion/gm |
| K1 ^(b) | V ^{1/2} | 1.0 | 0.0 | - | Body-effect coefficient for subthreshold region |
| K1SAT | V ^{-1/2} | 0.0 | 0.0 | - | Body-effect coefficient for saturation region |
| K1RSCE ^(b) | V ^{1/2} | 0.0 | - | - | Pre-factor for reverse short channel effect |
| KSATIV ^(b) | - | 1.0 | - | - | Parameter for long channel V _{dsat} |
| LII ^(b) | V -m | 0.5e-9 | - | - | Channel length dependent parameter of lii (IIMOD=2) |
| LINTIGEN | m | 0.0 | - | $L_{eff}/2$ | L_{int} offset for R/G current |
| LINTNOI | m | 0.0 | - | $L_{eff}/2$ | L_{int} offset for flicker noise calculation |
| LPA | - | 1.0 | - | - | Mobility L power coefficient |
| LPE0 ^(b) | m | 5e-9 | $-L_{eff}$ | - | Equivalent length of pocket region zero bias |
| MEXP ^(b) | - | 4 | 2 | - | Smoothing function factor for V _{dsat} |

Chapter 2: MOSFET Models

LEVEL 72: BSIM-CMG MOSFET Model

| Name | Unit | Default | Min | Max | Description |
|------------------------|--|----------|-------|-----|--|
| MJD | - | MJS | - | - | Drain bottom junction capacitance grading coefficient |
| MJS | - | 0.5 | - | - | Source bottom junction capacitance grading coefficient |
| MJSWGD | - | MJSWGS | - | - | Gate-edge sidewall junction capacitance grading coefficient (drain-side) |
| MJSWGS | - | MJSWS | - | - | Gate-edge sidewall junction capacitance grading coefficient (source-side) |
| MJSWS | - | 0.33 | | | Isolation-edge sidewall junction capacitance grading coefficient (source-side) |
| MJSWD | - | MJSWS | - | - | Isolation-edge sidewall junction capacitance grading coefficient (drain-side) |
| NBODYN1 | - | 0 | -0.08 | - | NFIN dependence of NBODY |
| NBODYN2 | - | 1e5 | 1e-5 | - | NFIN dependence of NBODY |
| NIGBACC ^(b) | - | 1.0 | >0.0 | - | Parameter for lgb in accumulation |
| NIGBINV ^(b) | - | 3.0 | > 0.0 | - | Parameter for lgb in inversion (BULKMOD only) |
| NIGC ^(b) | - | 1.0 | >0 | - | Parameter for lgc in inversion |
| NJS | - | 1.0 | 0.0 | - | Source junction emission coefficient |
| NJD | - | NJS | 0.0 | - | Drain junction emission coefficient |
| NJTS | - | 20 | 0.0 | - | Non-ideality factor for JTSS |
| NOIA | eV ⁻¹ s ^{1-EF} m ⁻³ | 6.250e39 | - | - | Flicker noise parameter |
| NOIB | eV ⁻¹ s ^{1-EF} m ⁻¹ | 3.125e24 | - | - | Flicker noise parameter |
| NOIC | eV ⁻¹ s ^{1-EF} m | 8.750e7 | - | - | Flicker noise parameter |

| Name | Unit | Default | Min | Max | Description |
|------------------------|------|---------|------|-----|---|
| NSEG | - | 5 | 4 | 10 | Number of channel segments for NQSMOD=3 |
| NTGEN ^(b) | - | 1.0 | >0.0 | - | Parameter for R/G current (Experimental) |
| NTNOI | - | 1.0 | 0.0 | - | Thermal noise parameter |
| NTOX ^(b) | - | 1.0 | - | - | Exponent for gate oxide ratio |
| PBD | V | PBS | 0.01 | - | Bottom junction built-in potential (drain-side) |
| PBS | V | 1.0 | 0.01 | - | Bottom junction built-in potential (source-side) |
| PBSWD | V | PBSWS | 0.0 | - | Isolation-edge sidewall junction built-in potential (drain-side) |
| PBSWGD | V | PBSWGS | 0.01 | - | Gate-edge sidewall junction built-in potential (drain-side) |
| PBSWGS | V | PBSWS | 0.01 | - | Gate-edge sidewall junction built-in potential (source-side) |
| PBSWS | V | 1.0 | 0.01 | - | Isolation-edge sidewall junction built-in potential (source-side) |
| PCLM ^(b) | - | 0.013 | - | - | Channel length modulation (CLM) parameter |
| PCLMCV ^(b) | - | 0.013 | >0.0 | - | Channel length modulation (CLM) parameter for C-V |
| PCLMG(b) | - | 0 | - | - | Gate bias dependent parameter for channel length modulation (CLM) |
| PDIBL1 ^(b) | - | 1.30 | 0.0 | - | Parameter for DIBL effect on Rout in forward mode |
| PDIBL1R ^(b) | - | 2e-4 | 0.0 | - | Parameter for DIBL effect on Rout in reverse mode |
| PDIBL2 ^(b) | - | 2e-4 | 0.0 | - | Parameter for DIBL effect on Rout |
| PGIDL ^(b) | - | 1.0 | - | - | Exponent of electric field for GIDL |

Chapter 2: MOSFET Models

LEVEL 72: BSIM-CMG MOSFET Model

| Name | Unit | Default | Min | Max | Description |
|------------------------|-----------------|---------|-------|-----|---|
| PGISL ^(b) | - | 1.0 | - | - | Exponent of electric field for GISL |
| PHIBE ^(b) | V | 0.7 | 0.2 | 1.2 | Body-effect voltage parameter |
| PHIGL | eV=m | 0 | - | - | Length dependence of gate work function |
| PHIGN1 | - | 0 | -0.08 | - | NFIN dependence of PHIG |
| PHIGN2 | - | 1e5 | 1e-5 | - | NFIN dependence of PHIG |
| PHIN ^(b) | V | 0.05 | - | - | Nonuniform vertical doping effect on surface potential |
| PIGCD ^(b) | - | 1.0 | >0.0 | - | Vds dependence of Igcs and Igcd |
| POXEDGE ^(b) | - | 1 | >0.0 | - | Factor for the gate edge Tox |
| PQM | - | 0.66 | - | - | Fitting parameter for QM charge centroid (inversion) |
| PQMACC | - | 0.66 | - | - | Fitting parameter for QM charge centroid (accumulation) |
| PRWGS ^(b) | V ⁻¹ | 0.0 | 0.0 | - | Source side quasi-saturation parameter |
| PRWGD ^(b) | V ⁻¹ | PRWGS | 0.0 | - | Drain side quasi-saturation parameter |
| PSAT(b) | - | 2.0 | 2.0 | - | Exponent for field for velocity saturation |
| PTWG ^(b) | V ⁻² | 0.0 | - | - | Correction factor for velocity saturation in forward mode |
| PTWGR ^(b) | V ⁻² | 0.0 | - | - | Correction factor for velocity saturation in reverse mode |
| PVAG ^(b) | - | 1.0 | - | - | Vgs dependence on early voltage |
| QM0 | V | 1e-3 | >0 | - | Normalization parameter for QM charge centroid (inversion) |
| QM0ACC | V | 1e-3 | >0 | - | Normalization parameter for QM charge centroid (accumulation) |

| Name | Unit | Default | Min | Max | Description |
|--------------------------|-----------------------|---------|-----|-----|--|
| QMFACTOR ^(b) | - | 0.0 | - | - | Pre-factor for QM V_{th} shift correction |
| QMTCENCV(b) | - | 0.0 | - | - | Pre-factor/switch for QM effective width and oxide thickness correction for CV |
| QMTCENCVA ^(b) | - | 0.0 | - | - | Pre-factor/switch for QM effective width and oxide thickness correction for accumulation region CV |
| QMTCENIV(b) | - | 0.0 | - | - | Pre-factor/switch for QM effective width correction for IV |
| RDSWMIN | $\Omega - \mu_m^{WR}$ | 0.0 | - | - | RDSMOD = 0 S/D extension resistance per unit width at high V_{gs} |
| RDSW ^(b) | $\Omega - \mu_m^{WR}$ | 40 | 0.0 | - | RDSMOD = 0 zero bias S/D extension resistance per unit width |
| RDWMIN | $\Omega - \mu_m^{WR}$ | 0.0 | 0.0 | - | RDSMOD = 1 drain extension resistance per unit width at high V_{gs} |
| RDW ^(b) | $\Omega - \mu_m^{WR}$ | 50 | 0.0 | - | RDSMOD = 1 zero bias drain extension resistance per unit width |
| RSW ^(b) | $\Omega - \mu_m^{WR}$ | 50 | 0.0 | - | RDSMOD = 1 zero bias source extension resistance per unit width |
| RSWMIN | $\Omega - \mu_m^{WR}$ | 0.0 | 0.0 | - | RDSMOD = 1 source extension resistance per unit width at high V_{gs} |
| RSDR | V^{-PRSDR} | 0.0 | 0.0 | - | RDSMOD = 1 source side drift resistance parameter in forward mode |
| RSDRR | V^{-PRSDR} | RSDR | 0.0 | | RDSMOD = 1 drain side drift resistance parameter in reverse mode |
| PRSDR | - | 1.0 | 0.0 | - | RDSMOD = 1 drain side drift resistance parameter in forward mode |

Chapter 2: MOSFET Models

LEVEL 72: BSIM-CMG MOSFET Model

| Name | Unit | Default | Min | Max | Description |
|---------------------|-----------------|---------|--------|-----|--|
| PRDDR | - | PRSDDR | - | - | RDSMOD = 1 drain side drift resistance parameter in reverse mode |
| RGFIN | Ω | 1.0e-3 | 1.0e-3 | - | Effective gate electrode resistance per fin per finger |
| RGEXT | Ω | 0.0 | 0.0 | - | Effective gate electrode external resistance (Experimental) |
| RSHD | Ω | RSHS | 0.0 | - | Drain-side sheet resistance |
| RSHS | Ω | 0.0 | 0.0 | - | Source-side sheet resistance |
| SII0 ^(b) | V^{-1} | 0.5 | - | - | Vgs dependent parameter of Iii (IIMOD=2) |
| SII1 ^(b) | - | 0.1 | - | - | Vgs dependent parameter of Iii (IIMOD=2) |
| SII2 ^(b) | V | 0.0 | - | - | Vgs dependent parameter of Iii (IIMOD=2) |
| SIID ^(b) | V | 0.0 | - | - | Vds dependent parameter of Iii (IIMOD=2) |
| TETA0 | $1/K$ | 0.0 | - | - | Temperature dependence of DIBL coefficient |
| TETA0R | $1/K$ | 0.0 | - | - | Temperature dependence of Reverse-mode DIBL coefficient |
| TOXREF | m | 1.2nm | > 0.0 | - | Nominal gate oxide thickness for gate tunneling current |
| U0 ^(b) | $m^2/V \cdot s$ | 3e-2 | - | - | Low field mobility |
| U0N1 | - | 0 | -0.08 | - | NFIN dependence of U0 |
| U0N2 | - | 1e5 | 1e-5 | - | NFIN dependence of U0 |
| UA ^(b) | $(cm/MV)^{EU}$ | 0.3 | >0.0 | - | Phonon / surface roughness scattering parameter |
| UCS ^(b) | - | 1.0 | >0.0 | - | Coulombic scattering parameter (Experimental) |

Chapter 2: MOSFET Models
LEVEL 72: BSIM-CMG MOSFET Model

| Name | Unit | Default | Min | Max | Description |
|-----------------------|---------------|---------|--------------------------|-----|--|
| UD ^(b) | cm/MV | 0.0 | >0.0 | - | Coulombic scattering parameter (Experimental) |
| UP ^(b) | μm^{LPA} | 0.0 | - | - | Mobility L coefficient |
| VSAT ^(b) | m/s | 85000 | - | - | Saturation velocity for the saturation region |
| VSAT1 ^(b) | m/s | VSAT | - | - | Saturation velocity for the linear region in forward mode |
| VSAT1N1 | - | 0 | -0.08 | - | NFIN dependence of VSAT1 |
| VSAT1N2 | - | 1e5 | 1e-5 | - | NFIN dependence of VSAT1 |
| VSATN1 | - | 0 | -0.08 | - | NFIN dependence of VSAT |
| VSATN2 | - | 1e5 | 1e-5 | - | NFIN dependence of VSAT |
| VSAT1R ^(b) | m/s | VSAT1 | - | - | Saturation velocity for the linear region in reverse mode |
| VSAT1RN1 | - | VSAT1N1 | -0.08 | - | NFIN dependence of VSAT1R |
| VSAT1RN2 | - | VSAT1N2 | 1e-5 | - | NFIN dependence of VSAT1R |
| VSATCV ^(b) | m/s | VSAT | - | - | Saturation velocity for the capacitance model |
| WR ^(b) | - | 1.0 | - | - | W dependence parameter of S/D extension resistance |
| XJBVD | - | XJBVS | - | - | Fitting parameter for source diode breakdown current |
| XJBVS | - | 1.0 | - | - | Fitting parameter for source diode breakdown current |
| XRCRG1 ^(b) | | 12.0 | 0.0 or $\geq 10^{-3}$ | - | Parameter for non quasi-static gate resistance (NQSMOD=1) and NQSMOD=2 |
| XRCRG2 ^(b) | - | 1.0 | - | - | Parameter for non quasi-static gate resistance (NQSMOD=1) and NQSMOD=2 |
| ALPHAI0(b) | $m.V^{-1}$ | 0.0 | - | - | First parameter of Iii (IIMOD=2) |

Chapter 2: MOSFET Models

LEVEL 72: BSIM-CMG MOSFET Model

| Name | Unit | Default | Min | Max | Description |
|----------------------------|-----------------|-----------------------|------|-----|---|
| ALPHAI1(b) | V ⁻¹ | 0.0 | - | - | L scaling parameter of I _{II} (IIMOD=2) |
| TOXG | m | TOXP | >0.0 | - | Oxide thickness for gate current model. |
| K1SI(b) | - | K0SI | >0 | - | Correction factor for strong inversion used in M _{ob} |
| PSATCV ^(b) | - | PSAT | 2.0 | - | Exponent for field for velocity saturation for the capacitance model. |
| DELTAVSATCV ^(b) | - | DELTAVSA _T | 0.01 | - | Velocity saturation parameter in the linear region for the capacitance model. |

BSIM-CMG Model (Version>=105) — Geometry Dependent Parasitic Parameters

| Name | Unit | Default | Min | Max | Description |
|-----------|-----------------|---------|--------------------|-----|--|
| ARSDEND | m ² | 0 | 0 | - | Extra raised source/drain cross sectional area at the two ends of the FinFET |
| ASILIEND | m ² | 0 | 0 | - | Extra silicide cross sectional area at the two ends of the FinFET |
| CGEOA | - | 1.0 | - | - | Fitting parameter for CGEOMOD=2 |
| CGEOB | m ⁻¹ | 0 | - | - | Fitting parameter for CGEOMOD=2 |
| CGEOC | m ⁻¹ | 0 | - | - | Fitting parameter for CGEOMOD=2 |
| CGEOD | m ⁻¹ | 0 | - | - | Fitting parameter for CGEOMOD=2 |
| CGEOE | - | 1.0 | - | - | Fitting parameter for CGEOMOD=2 |
| CRATIO | - | 0.5 | 0 | 1 | Ratio of the corner area filled with silicon to the total corner area |
| DELTAPRSD | m | 0.0 | FPICT _H | - | Change in silicon/silicide interface length due to non-rectangular epi |
| EPSRSP | - | 3.9 | 1 | - | Relative dielectric constant of the gate sidewall spacer material |

| Name | Unit | Default | Min | Max | Description |
|---------|-----------------------|--------------------|-----------|-----------|--|
| HEPI | m | 10n | - | - | Height of the raised source/drain on top of the fin |
| LDG | m | 5n | 0 | - | Lateral diffusion gradient in the fin extension region |
| LSP | m | 0.2(L+XL) | 0 | - | Thickness of the gate sidewall spacer |
| NSDE | m^{-3} | 2×10^{25} | 10^{25} | 10^{26} | Active doping concentration at the channel edge |
| PRSDEND | m | 0 | 0 | - | Extra silicon/silicide interface perimeter at the two ends of the FinFET |
| RGEOA | - | 1.0 | - | - | Fitting parameter for RGEOMOD=1 |
| RGEOB | m^{-1} | 0 | - | - | Fitting parameter for RGEOMOD=1 |
| RGEOC | m^{-1} | 0 | - | - | Fitting parameter for RGEOMOD=1 |
| RGEOD | m^{-1} | 0 | - | - | Fitting parameter for RGEOMOD=1 |
| RGEOE | m^{-1} | 0 | - | - | Fitting parameter for RGEOMOD=1 |
| RHOC | $\Omega - \text{m}^2$ | 10^{-18} | 10^{-9} | | Contact resistivity at the silicon/silicide interface |
| RHOEXT | $\Omega - \text{m}$ | RHORSD | 0 | - | Average resistivity of silicon in the fin extension region |
| RHORSD | $\Omega - \text{m}$ | calculated | 0 | - | Average resistivity of silicon in the raised source/drain region |
| SDTERM | - | 0 | 0 | 1 | Indicator of whether the source/drain are terminated with silicide |
| TGATE | m | 30n | 0 | - | Gate height on top of the hard mask |
| TMASK | m | 30n | 0 | - | Height of the hard mask on top of the fin |
| TSILI | m | 10n | - | - | Thickness of the silicide on top of the raised source/drain |

BSIM-CMG Model (Version>=105) — Temperature Dependent and Self-Heating Parameters

| Name | Unit | Default | Min | Max | Description |
|----------------------|------------|---------|-----|-----|--|
| AT ^(b) | 1/K | 0.005 | - | - | Saturation velocity temperature coefficient |
| CTH0 | J/K | 1.0e-5 | 0.0 | - | Thermal capacitance for self-heating calculation |
| EMOBT ^(b) | - | 0.0 | - | - | Temperature Coefficient of ETAMOB |
| IGT ^(b) | - | 2.5 | - | - | Gate current temperature coefficient |
| IIT ^(b) | - | -0.5 | - | - | Impact ionization temperature coefficient(IIMOD=1) |
| KT1 | V | 0.0 | - | - | V _{th} temperature coefficient |
| KT1L | V · m | 0.0 | - | - | V _{th} temperature coefficient |
| PRT ^(b) | 1/K | 0.001 | - | - | Series resistance temperature coefficient |
| PTWGT ^(b) | 1/K | 0.004 | - | - | PTWG temperature coefficient |
| RTH0 | K/W | 0.01 | 0.0 | - | Thermal resistance for self-heating calculation |
| TBGASUB | (eV)/ (°K) | 7.02e-4 | - | - | Bandgap temperature coefficient |
| TBGBSUB | °K | 1108.0 | - | - | Bandgap temperature coefficient |
| TCJ | 1/K | 0.0 | - | - | Temperature coefficient for CJS/CJD |
| TCJSW | 1/K | 0.0 | - | - | Temperature coefficient for CJSWS1/CJDWD1 |
| TCJSWG | 1/K | 0.0 | - | - | Temperature coefficient for CJSWGS/CJSWGD |
| TGIDL ^(b) | 1/K | -0.003 | - | - | GISL/GIDL temperature coefficient |
| TII ^(b) | - | 0.0 | - | - | Impact ionization temperature coefficient(IIMOD=2) |

| Name | Unit | Default | Min | Max | Description |
|----------------------|------|-----------|-----|-----|--|
| TMEXP ^(b) | 1/K | 0 | - | - | Temperature coefficient for V_{dseff} smoothing |
| TNOM | °C | 27 | 0.0 | - | Temperature at which the model is extracted in Celsius |
| TPB | 1/K | 0.0 | - | - | Temperature coefficient for PBS/PBD |
| TPBSW | 1/K | 0.0 | - | - | Temperature coefficient for PBSWS/PBDWD |
| TBSWG | 1/K | 0.0 | - | - | Temperature coefficient for PBSWGS/PBSWGD |
| TRSDR ^(b) | 1/K | 0.0 | - | - | Source side drift resistance temperature coefficient |
| TRDDR ^(b) | 1/K | 0.0 | - | - | Drain side drift resistance temperature coefficient |
| TSS ^(b) | 1/K | 0.0 | - | - | Subthreshold swing temperature coefficient |
| UA1 ^(b) | - | 1.032e-3 | - | - | Mobility temperature coefficient for UA |
| UC1(b) | - | 0.056e-9 | - | - | Mobility temperature coefficient for UC |
| UCSTE ^(b) | - | -4.775e-3 | - | - | Mobility temperature coefficient |
| UD1 ^(b) | - | 0.0 | - | - | Mobility (MOBMOD=0) temperature coefficient (Experimental) |
| UTE ^(b) | - | 0.0 | - | - | Mobility temperature coefficient |
| UTL ^(b) | - | -1.5e-3 | - | - | Mobility temperature coefficient |
| WTH0 | m | 0.0 | 0.0 | - | Width-dependence coefficient for self-heating calculation |
| XTIS | - | 3.0 | - | - | Source junction current temperature exponent |
| XTID | - | XTIS | - | - | Drain junction current temperature exponent |

Chapter 2: MOSFET Models

LEVEL 72: BSIM-CMG MOSFET Model

| Name | Unit | Default | Min | Max | Description |
|--------------------------|---|---------|-----|-----|---|
| ALPHAIIO1 ^(b) | $\text{m.V}^{-1}/\text{K}$ | 0.0 | - | - | Temperature dependence of ALPHAIIO |
| ALPHAI11 ^(b) | V^{-1}/K | 0.0 | - | - | Temperature dependence of ALPHAI1 |
| ALPHA01 ^(b) | $\text{m.V}^{-1}/\text{K}$ | 0.0 | - | - | Temperature dependence of ALPHA0 |
| ALPHA11 ^(b) | V^{-1}/K | 0.0 | - | - | Temperature dependence of ALPHA1 |
| AIGBINV1 ^(b) | $(\text{F s}^2/\text{g})^{0.5}\text{m}^{-1}/\text{K}$ | 0.0 | - | - | Temperature dependence of AIGBINV |
| AIGBACC1 ^(b) | $(\text{F s}^2/\text{g})^{0.5}\text{m}^{-1}/\text{K}$ | 0.0 | - | - | Temperature dependence of AIGBACC |
| AIGC1 ^(b) | $(\text{F s}^2/\text{g})^{0.5}\text{m}^{-1}/\text{K}$ | 0.0 | - | - | Temperature dependence of AIGC |
| AIGS1 ^(b) | $(\text{F s}^2/\text{g})^{0.5}\text{m}^{-1}/\text{K}$ | 0.0 | - | - | Temperature dependence of AIGS |
| AIGD1 ^(b) | $(\text{F s}^2/\text{g})^{0.5}\text{m}^{-1}/\text{K}$ | 0.0 | - | - | Temperature dependence of AIGD |
| A11 ^(b) | V^{-2}/K | 0.0 | - | - | Temperature dependence of non-saturation effect parameter for strong inversion region |
| A21 ^(b) | V^{-1}/K | 0.0 | - | - | Temperature dependence of non-saturation effect parameter for moderate inversion region |
| K01 ^(b) | V/K | 0.0 | - | - | Temperature dependence of K0 |
| K0SI1 ^(b) | $1/\text{K}$ | 0.0 | - | - | Temperature dependence of K0SI |
| K11 ^(b) | $\text{V}^{-1/2}/\text{K}$ | 0.0 | - | - | Temperature dependence of K1 |
| K1SI1 ^(b) | $1/\text{K}$ | 0.0 | - | - | Temperature dependence of K1SI |
| K1SAT1 ^(b) | $\text{V}^{-1/2}/\text{K}$ | 0.0 | - | - | Temperature dependence of K1SAT |

BSIM-CMG Model (Version>=105) — Variability Modeling Parameters

| Name | Unit | Default | Min | Max | Description |
|-------------------------|--------------------|------------|-------------------|------------------|--|
| DTEMP | K | 0.0 | - | - | Device temperature shift handle |
| DELVTRAND | V | 0.0 | - | - | Threshold voltage shift handle |
| U0MULT | - | 1.0 | - | - | Multiplier to mobility (or more precisely divides D _{mob} , D _{mobs}) |
| IDS0MULT | - | 1.0 | - | - | Multiplier to source-drain channel current |
| TFIN ⁽ⁱ⁾ | m | 15n | 1n | | Body (fin) thickness |
| FPICTH ⁽ⁱ⁾ | m | 80n | TFIN | - | Fin Pitch |
| XL ^(mod) | m | 0 | - | - | L offset for channel length due to mask/etch effect |
| NBODY ^(mod) | m ⁻³ | 1e22 | 1e18 | 5e24 | Channel (body) doping concentration |
| EOT ^(mod) | m | 1.0n | 0.1n | - | <i>SiO</i> 2 equivalent gate dielectric thickness (including inversion layer thickness) |
| TOXP ^(mod) | m | 1.2n | 0.1n | - | Physical oxide thickness |
| RSHS ^(mod) | Ω | 0.0 | 0.0 | - | Source-side sheet resistance |
| RSHD ^(mod) | Ω | RSHS | 0.0 | - | Drain-side sheet resistance |
| RHOC ^(mod) | $\Omega \cdot m^2$ | 1p | 10 ⁻¹⁸ | 10 ⁻⁹ | Contact resistivity at the silicon / silicide interface |
| RHORSD ^(mod) | $\Omega \cdot m$ | Calculated | - | - | Average resistivity of silicon in the raised source/drain region |
| RHOEXT ^(mod) | $\Omega \cdot m$ | RHORSD | - | - | Average resistivity of silicon in the fin extension region |

BSIM-CMG Model Parameters (Version < 105)

This section covers the following topics:

- [BSIM-CMG Model \(Version<105\) — Instance Parameters](#)
- [BSIM-CMG Model \(Version<105\) — Control and Process Parameters](#)
- [BSIM-CMG Model \(Version<105\) — Basic Parameters](#)
- [BSIM-CMG Model \(Version<105\) — Temperature Dependence and Self-Heating Parameters](#)

BSIM-CMG Model (Version<105) — Instance Parameters

Note: Binnable parameters are marked as ^(b). Instance parameters which are also model parameters are marked as ^(m).

| Parameter | Unit | Default | Description |
|---------------------|----------------|---------|---|
| AD ^(m) | m ² | 0 | Drain area |
| AS ^(m) | m ² | 0 | Source area |
| CDSP ^(m) | F | 0 | Constant drain to source fringe capacitance |
| CGDP ^(m) | F | 0 | Constant gate to drain fringe capacitance |
| CGSP ^(m) | F | 0 | Constant gate to source fringe capacitance |
| D ^(m) | m | 40e-9 | Diameter of cylinder |
| L ^(m) | m | 30e-9 | Channel length |
| NF | - | 1 | Number of fingers |
| NFIN ^(m) | - | 10 | Number of fins per finger |
| NRD | - | 0 | Number of drain diffusion squares |
| NRS | - | 0 | Number of source diffusion squares |
| PD1 ^(m) | m | 0 | 1st part of the drain perimeter |
| PD2 ^(m) | m | 0 | 2nd part of the drain perimeter |

| Parameter | Unit | Default | Description |
|---------------------|----------|---------|--|
| PS1 ^(m) | m | 0 | 1st part of the source perimeter |
| PS2 ^(m) | m | 0 | 2nd part of the source perimeter |
| RDC | Ω | 0 | Source contact resistance for per-finger device (after v.104) |
| RSC | Ω | 0 | Source contact resistance for per-finger device (after v.104) |
| TFIN ^(m) | m | 15e-9 | Fin (channel) thickness; currently supports TFIN < 50x ¹⁰⁻⁹ m; for larger values use BSIM4 or BSIM4SOI. |

BSIM-CMG Model (Version<105) — Control and Process Parameters

| Parameter | Unit | Default | Description |
|-----------|------|---------|--|
| BULKMOD | - | 1 | BULK/SOI model selector (Version102 and later) In Verilog-A the number of terminals cannot be controlled by a model parameter. If you are running the Verilog-A version of this model, select the bulk or SOI module by running bulkmg.va or soimg.va |
| CGEOMOD | - | 0 | Geometry-dependent parasitic capacitance model selector; 1=on, 0=off |
| CLMMOD | - | 0 | Model selector for channel length modulation |
| COREMOD | - | 0 | Simplified surface potential solution; 0=off, 1= on (lightly-doped or undoped) |
| GEOMOD | - | 1 | Structure selector; 0=double gate, 1=triple gate, 2=quadruple gate, 3=cylindrical gate |
| GIDLMOD | - | 0 | GIDL/GISL current switch; 1=on, 0=off |
| IGMOD | - | 0 | Gate current switch; 1=on, 0=off |
| IIMOD | - | 0 | Impact ionization model switch; 0 = OFF, 1 =BSIM4 based, 2 = BSIMSOI based |
| MOBMOD | - | 0 | Mobility model selector 0 = BSIM-based, 1 = PSP-based |
| NQSMOD | - | 0 | NQS gate resistor switch; 1=on, 0=off |
| RDSMOD | - | 0 | Source/drain resistance selector; 0 = internal, 1 =external |
| RGATEMOD | - | 0 | Gate electrode resistor switcher; 1=on, 0=off |

Chapter 2: MOSFET Models

LEVEL 72: BSIM-CMG MOSFET Model

| Parameter | Unit | Default | Description |
|----------------------|---------------|---------|--|
| SHMOD | - | 0 | Self-heating switch; 1=on, 0=off |
| DEVTYPE | | NMOS | NMOS=1, PMOS=0 |
| BG0SUB | eV | 1.12 | Band gap of the channel material at 300.15K |
| DELTAW | m | 0.0 | Reduction of effective width due to shape of fin |
| DELTAWCV | m | 0.0 | CV reduction of effective width due to shape of fin |
| DLBIN | m | 0.0 | Length reduction parameter for binning |
| DLC | m | 0.0 | Channel length reduction parameter for CV |
| DLCACC | m | 0.0 | Length reduction parameter for CV in accumulation region (BULKMOD =1;CAPMOD = 1) |
| EASUB | eV | 4.05 | Electron affinity of the substrate material |
| EOT | m | 0.9e-9 | Effective gate dielectric thickness relative to SIO2 |
| EPSROX | - | 3.9 | Relative dielectric constant of the gate insulator |
| EPSRSUB | - | 11.9 | Relative dielectric constant of the channel material |
| FECH | - | 1.0 | End-channel factor, for different orientation/shape; this parameter handles the mobility difference between the side channel and the top channel |
| FECHCV | - | 1.0 | CV end-channel factor, for different orientation/shape |
| HFIN | m | 35e-9 | Fin height; instance parameter, also |
| LINT | m | 0.0 | Channel length reduction parameter |
| LL | $m^{(LLN+1)}$ | 0.0 | Channel length reduction parameter |
| LLC | $m^{(LLN+1)}$ | 0.0 | Channel length reduction parameter for CV |
| LLN | - | 1.0 | Channel length reduction parameter |
| NBODY ^(b) | m^{-3} | 1e22 | Channel doping concentration; model currently supports NBODY < $5 \times 10^{24} m^{-3}$; for larger values use BSIM4 or BSIM4SOI |
| NC0SUB | m^{-3} | 2.86e25 | Conduction band density of states at 300.15K |

| Parameter | Unit | Default | Description |
|----------------------|----------|---------|---|
| NGATE ^(b) | m^{-3} | 0 | Parameter for Poly Gate doping; =0 for metal gate |
| NI0SUB | m^{-3} | 1.1e16 | Intrinsic carrier concentration of channel at 300.15K |
| PHIG ^(b) | eV | 4.61 | Work function of gate |
| XL | m | -5e-9 | L offset for channel length due to mask/etch effect |

BSIM-CMG Model (Version<105) — Basic Parameters

| Name | Unit | Default | Min | Max | Description |
|------------------------|---------------------------|---------|-----|-----|--|
| A1(b) | V ⁻¹ | 0.0 | - | - | Non-saturation effect parameter in strong inversion region |
| A2(b) | V ⁻² | 0.0 | - | 1 | Non-saturation effect parameter in moderate inversion region |
| AGIDL ^(b) | Ω^{-1} | 6.055 | - | - | Pre-exponential coefficient for GIDL |
| AGISL ^(b) | Ω^{-1} | AIGDL | - | - | Pre-exponential coefficient for GISL |
| AIGBINV ^(b) | $(Fs^2 / g)^{0.5} m^{-1}$ | 1.11e-2 | - | - | Parameter for lgb in inversion |
| AIGC ^(b) | $(Fs^2 / g)^{0.5} m^{-1}$ | 1.36e-2 | - | - | Parameter for lgc in inversion |
| AIGD ^(b) | $(Fs^2 / g)^{0.5} m^{-1}$ | 1.36e2 | - | - | Parameter for lgd in inversion |
| AIGS ^(b) | $(Fs^2 / g)^{0.5} m^{-1}$ | 1.36e2 | - | - | Parameter for lgs in inversion |
| ALP ^(b) | - | 0.013 | - | - | CLMMOD = 0 Channel Length Modulation (CLM) pre-factor |
| ALPHA0 ^(b) | $m \cdot V^{-1}$ | 0.0 | - | - | First parameter of lii |
| ALPHA1 ^(b) | V ⁻¹ | 0.0 | - | - | L scaling parameter of lii |
| ALPHAI ^(b) | - | 0.0 | - | - | Pre-exponential constant for lii (IMOD=2) |
| BETA0 ^(b) | V ⁻¹ | 0.0 | - | - | Vds dependent parameter of lii |

Chapter 2: MOSFET Models

LEVEL 72: BSIM-CMG MOSFET Model

| Name | Unit | Default | Min | Max | Description |
|------------------------|----------------------------------|---------|-----|-----|---|
| BETAII0 ^(b) | V ⁻¹ | 0.0 | - | - | Vds dependent parameter of Iii (IIMOD=2) |
| BETAII1 ^(b) | - | 0.0 | - | - | Vds dependent parameter of Iii (IIMOD=2) |
| BETAII2 ^(b) | V | 0.0 | - | - | Vds dependent parameter of Iii (IIMOD=2) |
| BGIDL ^(b) | V/m | 0.3e9 | - | - | Exponential coefficient for GIDL |
| BGISL ^(b) | V/m | BIGDL | | | Band bending parameter for GISL |
| BIGBINV ^(b) | $(Fs^2 / g)^{0.5} m^{-1} V^{-1}$ | 9.49e-4 | - | - | Parameter for Ig _b in inversion (BULKMOD only) |
| BIGC ^(b) | $(Fs^2 / g)^{0.5} m^{-1} V^{-1}$ | 1.71e-3 | - | - | Parameter for Ig _c in inversion |
| BIGD ^(b) | $(Fs^2 / g)^{0.5} m^{-1} V^{-1}$ | 1.71e-3 | - | - | Parameter for Ig _d in inversion |
| BIGS ^(b) | $(Fs^2 / g)^{0.5} m^{-1} V^{-1}$ | 1.71e-3 | - | - | Parameter for Ig _s in inversion |
| BVD | V | BVS | | | Drain diode breakdown voltage |
| BVS | V | 10.0 | | | Source diode breakdown voltage |
| CDSC ^(b) | F/m ² | 7e-3 | 0.0 | - | Coupling capacitance between S/D and channel |
| CDSCD ^(b) | F/m ² | 7e-3 | 0.0 | - | Drain-bias sensitivity of CDSC |
| CDSCDR ^(b) | F/m ² | CDSCD | 0.0 | | Reverse mode drain-bias sensitivity of CDSC |
| CFD ^(b) | F/m | CFS | 0.0 | - | Drain-side outer fringe cap (for parasitic capacitance calculation) |
| CFS ^(b) | F/m | 2.5e-11 | 0.0 | - | Source-side outer fringe cap (for parasitic capacitance calculation) |
| CGBN | F/m | 0 | 0.0 | - | Gate-substrate overlap capacitance per unit channel length per finger per fin |
| CIGBINV ^(b) | V ⁻¹ | 6.00e-3 | - | - | Parameter for Ig _b in inversion (BULKMOD only) |

| Name | Unit | Default | Min | Max | Description |
|---------------------|------------------|---------|------|-----|---|
| CIGC ^(b) | V ⁻¹ | 0.075 | - | - | Parameter for Ig _c in inversion |
| CIGD ^(b) | V ⁻¹ | 0.075 | - | - | Parameter for Ig _d in inversion |
| CIGS ^(b) | V ⁻¹ | 0.075 | - | - | Parameter for Ig _s in inversion |
| CIT ^(b) | F/m ² | 0 | - | - | Parameter for interface trap |
| CJD | F/m ² | CJS | 0.0 | - | Unit area drain-side junction capacitance at zero bias |
| CJS | F/m ² | 0.003 | 0.0 | - | Unit area source-side junction capacitance at zero bias |
| CJSWD1 | F/m | CJSWS1 | 0.0 | - | 1st unit length drain-side sidewall junction capacitance at zero bias |
| CJSWD2 | F/m | CJSWS1 | 0.0 | - | 2nd unit length drain-side sidewall junction capacitance at zero bias |
| CJSWS1 | F/m | 3.0e-10 | 0.0 | - | 1st unit length source-side sidewall junction capacitance at zero bias |
| CJSWS2 | F/m | 3.0e-10 | 0.0 | - | 2nd unit length source-side sidewall junction capacitance at zero bias |
| COVD ^(b) | F | COVS | 0.0 | - | Constant gate-to-drain overlap cap (for parasitic capacitance calculation) |
| COVS ^(b) | F | 2.5e-11 | 0.0 | - | Constant gate-to-source overlap cap (for parasitic capacitance calculation) |
| CS ^(b) | - | 0.0 | >0.0 | - | Coulombic scattering parameter |
| DLCIGD | m | DLCIGS | - | - | Delta L for Ig _d model |
| DLCIGS | m | 0 | - | - | Delta L for Ig _s model |
| DROUT | | 1.06 | >0.0 | - | 0.56 |
| DSUB ^(b) | - | 1.06 | >0 | - | DIBL exponent coefficient |
| DVT0 ^(b) | - | 0.0 | 0.0 | - | SCE coefficient |
| DVT1 ^(b) | - | 0.60 | >0 | - | SCE exponent coefficient |

Chapter 2: MOSFET Models

LEVEL 72: BSIM-CMG MOSFET Model

| Name | Unit | Default | Min | Max | Description |
|------------------------|------------------|--------------|------------------------|-----|---|
| EGIDL ^(b) | V | 0.2 | | | Band bending parameter for GIDL |
| EGISL ^(b) | V | EGIDL | - | - | Pre-exponential coefficient for GISL |
| EIGBINV ^(b) | V | 1.1 | - | - | Parameter for Ig _b in inversion (BULKMOD only) |
| ESATII ^(b) | V/m | 1.0e7 | - | - | Saturation channel E-Field for I _{ii} (IIMOD=2) |
| ETA0 ^(b) | - | 0.60 | 0.0 | - | DIBL coefficient |
| ETA0R ^(b) | | ETA0 | 0.0 | | Reverse mode DIBL coefficient |
| ETAMOB ^(b) | - | 2.0 | - | - | Effective field parameter |
| EU ^(b) | cm/MV | 2.5 | >0.0 | - | MOBMOD = 0 phonon / surface roughness scattering |
| IJTHDFWD | A | IJTHSFW D | 10 I _{sbs} | - | Forward drain diode breakdown limiting current |
| IJTHDREV | A | IJTHSRE V | | | Reverse drain diode breakdown limiting current |
| IJTHSFWD | A | 0.1 | 10 I _{sbs} | - | Forward source diode breakdown limiting current |
| IJTHSREV | A | 0.1 | 10 I _{sbs} | - | Reverse source diode breakdown limiting current |
| JSD | A/m ² | JSS | 0.0 | - | Bottom drain junction reverse saturation current density |
| JSS | A/m ² | 1.0e-4 | 0.0 | - | Bottom source junction reverse saturation current density |
| JSWD1 | A/m | JSWS1 | 0.0 | 0.0 | Unit length reverse saturation current for 1st sidewall drain junction |
| JSWD2 | A/m | JSWS2 | 0.0 | 0.0 | Unit length reverse saturation current for 2nd sidewall drain junction |
| JSWS1 | A/m | 0 | 0.0 | 0.0 | Unit length reverse saturation current for 1st sidewall source junction |

| Name | Unit | Default | Min | Max | Description |
|-----------------------|-------------------|---------|-------|-----|---|
| JSWS2 | A/m | JSWS1 | 0.0 | 0.0 | Unit length reverse saturation current for 2nd sidewall source junction |
| K1RSCE ^(b) | V ^{1/2} | 0.0 | - | - | Pre-factor for reverse short channel effect |
| K0(b) | V | - | 0.0 | - | Lateral NUD parameter |
| K0SI(b) | - | 1.0 | >0 | - | Correction factor for strong inversion/gm |
| K1(b) | V ^{1/2} | 1.0 | 0.0 | - | Body-effect coefficient for subthreshold region |
| K1SAT(b) | V ^{-1/2} | 0.0 | - | - | Body-effect coefficient for saturation region |
| KSATIV ^(b) | - | 1.3 | - | - | Parameter for reverse short channel effect |
| LII ^(b) | V -m | 0.5e-9 | - | - | Channel length dependent parameter of lii (IIMOD=2) |
| LOVD ^(b) | m | LOVS | 0.0 | - | Gate-to-drain overlap length (for parasitic capacitance calculation) |
| LOVS ^{b)} | m | 1.0e-9 | 0.0 | - | Gate-to-source overlap length (for parasitic capacitance calculation) |
| LPA | - | 1.0 | - | - | Mobility L power coefficient |
| LPE0 ^(b) | m | 5e-9 | -Leff | - | Equivalent length of pocket region zero bias |
| MEXP ^(b) | - | 4 | 2 | - | Smoothing function factor for Vdsat |
| MJD | - | MJS | - | - | Drain bottom junction capacitance grading coefficient |
| MJS | - | 0.5 | - | - | Source bottom junction capacitance grading coefficient |
| MJSWD1 | - | MJSWS1 | - | - | 2nd drain sidewall junction capacitance grading coefficient |
| MJSWD2 | - | MJSWS2 | - | - | 2nd drain sidewall junction capacitance grading coefficient |

Chapter 2: MOSFET Models

LEVEL 72: BSIM-CMG MOSFET Model

| Name | Unit | Default | Min | Max | Description |
|------------------------|-----------------|---------|-------|-----|--|
| MJSWS1 | - | 0.33 | | | 1st source sidewall junction capacitance grading coefficient |
| MJSWS2 | - | MJSWS1 | - | - | 2nd source sidewall junction capacitance grading coefficient |
| MUE ^(b) | cm/MV | 1.2 | >0.0 | - | MOBMOD=1 Mobility reduction coefficient |
| NIGBINV ^(b) | - | 3.0 | > 0.0 | - | Parameter for Ig _b in inversion (BULKMOD only) |
| NIGC ^(b) | - | 1 | >0 | - | Parameter for Ig _c in inversion |
| NJD | - | NJS | 0.0 | - | Drain junction emission coefficient |
| NJS | - | 1.0 | 0.0 | - | Source junction emission coefficient |
| NSD ^(b) | m ⁻³ | 2e26 | - | - | S/D doping concentration |
| NTOX(b) | - | 1.0 | - | - | Nominal gate oxide thickness for Gate tunneling current |
| PBD | V | PBS | 0.01 | - | Unit area drain-side junction capacitance at zero bias |
| PBS | V | 1.0 | 0.01 | - | Unit area source-side junction capacitance at zero bias |
| PBSWD1 | V | PBSWS1 | 0.0 | - | Built-in potential for 1st drain-side sidewall junction capacitance |
| PBSWD2 | V | PBSWS2 | 0.01 | - | Built-in potential for 2nd drain-side sidewall junction capacitance |
| PBSWS1 | V | 1.0 | 0.01 | - | Built-in potential for 1st source-side sidewall junction capacitance |
| PBSWS2 | V | PBSWS1 | 0.01 | - | Built-in potential for 2nd source-side sidewall junction capacitance |
| PCLM ^(b) | - | 0.013 | - | - | CLMMOD = 1 Channel Length Modulation parameter |
| PCLMG | - | 0 | - | - | CLMMOD = 1 Gate bias dependent parameter for channel Length Modulation (CLM) |
| PDIBL1(b) | - | 1.30 | 0.0 | - | Parameter for DIBL effect on Rout |

| Name | Unit | Default | Min | Max | Description |
|--------------------------|-----------------------|---------|-----|-----|--|
| PDIBL2(b) | - | 2e-4 | 0.0 | - | Parameter for DIBL effect on Rout |
| PDIBL1R(b) | - | PDIBL1 | 0.0 | - | Parameter for DIBL effect on Rout in reverse mode |
| PGIDL(b) | - | 1.0 | - | - | Exponent of electric field for GIDL |
| PGISL(b) | - | 1.0 | - | - | Exponent of electric field for GISL |
| PHIBE ^(b) | V | 0.7 | 0.2 | 1.2 | Body-effect voltage parameter |
| PHIN ^(b) | V | 0.05 | - | - | Nonuniform vertical doping effect on surface potential |
| POXEDGE ^(b) | - | 1 | >0 | - | Factor for the gate edge Tox |
| PRWG ^(b) | V ⁻¹ | 0.0 | 0.0 | - | Gate bias dependence of S/D extension resistance |
| PRWGS ^(b) | V ⁻¹ | 0.0 | 0.0 | - | Source side quasi-saturation parameter |
| PRWGD ^(b) | V ⁻¹ | PRWGS | 0.0 | - | Drain side quasi-saturation parameter |
| PSAT ^(b) | - | 2.0 | 2.0 | - | Exponent for field for velocity saturation |
| PTWG ^(b) | V ⁻² | 0.0 | - | - | Correction factor for velocity saturation |
| PTWGR(b) | V ⁻² | PTWG | - | - | Correction factor for velocity saturation in reverse mode |
| PVAG ^(b) | - | 1.0 | - | - | V _{gs} dependence on early voltage |
| QMFACTOR ^(b) | - | 0.0 | - | - | Pre-factor for QM correction |
| QMTCENCVA ^(b) | - | 0.0 | - | - | Pre-factor/switch for QM effective width and oxide thickness correction for accumulation region CV |
| RDSW ^(b) | $\Omega - \mu_m^{WR}$ | 40 | 0.0 | - | RDSMOD = 0 zero bias S/D extension resistance per unit width |
| RDSWMIN | $\Omega - \mu_m^{WR}$ | 0.0 | - | - | RDSMOD = 0 S/D extension resistance per unit width at high V _{gs} |
| RDW ^(b) | $\Omega - \mu_m^{WR}$ | 50 | 0.0 | - | RDSMOD = 1 zero bias drain extension resistance per unit width |

Chapter 2: MOSFET Models

LEVEL 72: BSIM-CMG MOSFET Model

| Name | Unit | Default | Min | Max | Description |
|---------------------|-----------------------|---------|--------|-----|--|
| RDWMIN | $\Omega - \mu_m^{WR}$ | 0.0 | 0.0 | - | RDSMOD = 1 drain extension resistance per unit width at high V_{gs} |
| RSDR | $V^{-PRS DR}$ | RSDR | 0.0 | - | RDSMOD = 1 source side drift resistance parameter in forward mode |
| RDDRR | $V^{-PR DDR}$ | RDDR | 0.0 | - | RDSMOD = 1 source side drift resistance parameter in reverse mode |
| RDDR | $V^{-PR DDR}$ | RSDR | 0.0 | - | RDSMOD = 1 drain side drift resistance parameter in forward mode |
| RDDRR | $V^{-PR DDR}$ | RDDR | 0.0 | 0.0 | RDSMOD = 1 drain side drift resistance parameter in reverse mode |
| PRS DR | - | 1.0 | 0.0 | - | RDSMOD = 1 drain side drift resistance parameter in forward mode |
| PR DDR | - | PRS DR | 0.0 | - | RDSMOD = 1 drain side drift resistance parameter in reverse mode |
| RGEXT | Ω | 0.0 | 0.0 | - | Effective gate electrode external resistance (Experimental) |
| RGFIN | Ω | 1.0e-3 | 1.0e-3 | - | Effective gate electrode resistance per n per finger |
| RSHD | Ω | RSHS | 0.0 | - | Drain-side sheet resistance |
| RSHS | Ω | 0.0 | 0.0 | - | Source-side sheet resistance |
| RSW ^(b) | $\Omega - \mu_m^{WR}$ | 50 | 0.0 | - | RDSMOD = 1 zero bias source extension resistance per unit width |
| RSWMIN | $\Omega - \mu_m^{WR}$ | 0.0 | 0.0 | - | RDSMOD = 1 source extension resistance per unit width at high V_{gs} |
| SII0 ^(b) | V^{-1} | 0.0 | - | - | V_{gs} dependent parameter of Iii (IIMOD=2) |
| SII1 ^(b) | - | 0.0 | - | - | V_{gs} dependent parameter of Iii (IIMOD=2) |
| SII2 ^(b) | V | 0.0 | - | - | V_{gs} dependent parameter of Iii (IIMOD=2) |
| SIID ^(b) | V | 0.0 | - | - | V_{ds} dependent parameter of Iii (IIMOD=2) |

| Name | Unit | Default | Min | Max | Description |
|-------------------------|---|---------|------|-----|---|
| THETAMU | - | 1.0 | >0.0 | - | MOBMOD = 1 mobility reduction exponent |
| THETASAT ^(b) | V ⁻¹ | 2.0 | - | - | Velocity saturation parameter |
| TOXREF | m | 12nm | >0.0 | - | Nominal gate oxide thickness for Gate tunneling current |
| U0 ^(b) | m ² /V-s | 6e-2 | - | - | Low field mobility |
| UA ^(b) | (cm/MV) ^{EU} | 0.3 | >0.0 | - | MOBMOD = 0 phonon / surface roughness scattering |
| UC ^(b) | $\left(1.0e - 6 \cdot \frac{cm}{MV^2}\right)^{RU1.0}$ | | >0.0 | - | Body effect coefficient for mobility (BULKMOD=1) |
| UCS ^(b) | - | 1.0 | >0.0 | - | MOBMOD = 0 Coulombic scattering (Experimental) |
| UD ^(b) | cm/MV | 0.0 | >0.0 | - | MOBMOD = 0 Coulombic scattering (Experimental) |
| UP ^(b) | μm^{LPA} | 0.0 | - | - | Mobility L coefficient |
| VASAT | V | 0.2 | - | - | CLMMOD = 1 Channel Length Modulation (CLM) parameter |
| VP | V | 0.0 | - | - | CLMMOD = 0 CLM log dependence parameter |
| VSAT | m/s | 85000 | - | - | Saturation velocity |
| VSATCV(b) | m/s | VSAT | - | - | Saturation velocity for the capacitance model |
| VSAT1R(b) | m/s | VSAT1 | - | - | Saturation velocity for the linear region in reverse mode |
| WR ^(b) | - | 1.0 | - | - | W dependence parameter of S/D extension resistance |

BSIM-CMG Model (Version<105) — Temperature Dependence and Self-Heating Parameters

| Name | Unit | Default | Min | Max | Description |
|----------------------|-----------------------|---------|-----|-----|--|
| AT ^(b) | 1/ ($^{\circ}K$) | 0.005 | - | - | Saturation velocity temperature coefficient |
| CTH0 | J/K | 1.0e-5 | 0.0 | - | Thermal capacitance for self-heating calculation |
| EMOBT(b) | - | 0.0 | - | - | Temperature Coefficient of ETAMOB |
| IGT ^(b) | - | 2.5 | - | - | Gate current temperature coefficient |
| IIT ^(b) | - | -0.5 | - | - | Impact ionization temperature coefficient(IIMOD=1) |
| KT1 | V | -0.3 | - | - | V_{th} temperature coefficient |
| KT1L | V . m | 0.0 | - | - | V_{th} temperature coefficient |
| PRT ^(b) | - | 0.001 | - | - | Series resistance temperature coefficient |
| PTWGT ^(b) | 1/ ($^{\circ}K$) | 0.004 | - | - | PTWG temperature coefficient |
| RTH0 | K/W | 0.01 | 0.0 | - | Thermal resistance for self-heating calculation |
| STCS | - | 0.0 | - | - | Mobility (MOBMOD=1) temperature coefficient |
| STMUE | - | 0.0 | - | - | Mobility (MOBMOD=1) temperature coefficient |
| STTHETAMU | - | 1.5 | - | - | Mobility (MOBMOD=0) temperature coefficient |
| STTHETASAT | - | 1.0 | - | - | Saturation velocity temperature coefficient |
| TBGASUB | (eV)/ ($^{\circ}K$) | 7.02e-4 | - | - | Bandgap temperature coefficient |
| TBGBSUB | $^{\circ}K$ | 1108.0 | - | - | Bandgap temperature coefficient |
| TCJ | 1/ ($^{\circ}K$) | 0.0 | - | - | Temperature coefficient for cjs/cjd |

| Name | Unit | Default | Min | Max | Description |
|----------------------|--------------------|-----------|-----|-----|--|
| TCJSW1 | 1/ ($^{\circ}K$) | 0.0 | - | - | Temperature coefficient for cjsws1/cjdw1 |
| TCJSW2 | 1/ ($^{\circ}K$) | 0.0 | - | - | Temperature coefficient for cjsws2/cjdw2 |
| TGIDL ^(b) | 1/ ($^{\circ}K$) | -0.003 | - | - | GISL/GIDL temperature coefficient |
| TII ^(b) | - | 0.0 | - | - | Impact ionization temperature coefficient(IIMOD=2) |
| TMEXP ^(b) | 1/ ($^{\circ}K$) | 0 | - | - | Temperature coefficient for $V_{ds eff}$ smoothing |
| TNOM | $^{\circ}C$ | 27 | 0.0 | - | Temperature at which the model is extracted (in Celsius) |
| TPB | 1/ ($^{\circ}K$) | 0.0 | - | - | Temperature coefficient for pbs/pbd |
| TPBSW1 | 1/ ($^{\circ}K$) | 0.0 | - | - | Temperature coefficient for pbsws1/pbdw1 |
| TPBSW2 | 1/ ($^{\circ}K$) | 0.0 | - | - | Temperature coefficient for pbsws2/pbdw2 |
| TSS(b) | 1/K | 0.0 | - | - | Subthreshold swing temperature coefficient |
| TRSDR(b) | 1/K | 0.0 | | | Source side drift resistance temperature coefficient |
| TRDDR(b) | 1/K | TRSDR | - | - | Drain side drift resistance temperature coefficient |
| UA1 ^(b) | - | -1.1 | - | - | Mobility (MOBMOD=0) temperature coefficient |
| UC1(b) | - | 0.056e-9 | - | - | Mobility temperature coefficient for UC |
| UCSTE ^(b) | - | -4.775e-3 | - | - | Mobility (MOBMOD=0) temperature coefficient (Experimental) |
| UD1 ^(b) | - | 0.0 | - | - | Mobility (MOBMOD=0) temperature coefficient (Experimental) |
| UTE ^(b) | - | -1.4 | - | - | Mobility temperature coefficient |

Chapter 2: MOSFET Models

LEVEL 72: BSIM-CMG MOSFET Model

| Name | Unit | Default | Min | Max | Description |
|------|------|---------|-----|-----|---|
| WTH0 | m | 0.0 | 0.0 | - | Width-dependence coefficient for self-heating calculation |
| XTID | - | XTIS | - | - | Source junction current temperature exponent |
| XTIS | - | 3.0 | - | - | Drain junction current temperature exponent |

BSIM-CMG Model (Version=105.03) — WPE Model Support

This section covers the following topics:

- [BSIM-CMG Model \(Version=105.03\) — WPE Model Parameters](#)
- [BSIM-CMG Model \(Version=105.03\) — WPE Instance Parameters](#)

BSIM-CMG Model (Version=105.03) — WPE Model Parameters

| Parameter | Default | Min | Max | Bin | Description |
|-----------|---------|-----|-----|-----|---|
| WPEMOD | 0 | 0 | 1 | No | Flag for WPE model (WPEMOD=1 to activate this model) |
| K2WE | 0.0 | - | - | Yes | Threshold shift factor for well-proximity effect |
| KU0WE | 0.0 | - | - | Yes | K2 shift factor for well-proximity effect |
| KVTH0WE | 0.0 | - | - | Yes | Threshold shift factor for well-proximity effect |
| NK2WE | 0.0 | - | - | Yes | K2 shift factor for well-proximity effect |
| NKU0WE | 0.0 | - | - | Yes | Mobility degradation factor for well-proximity effect |
| NKVTH0WE | 0.0 | - | - | Yes | Threshold shift factor for well-proximity effect |
| PK2WE | 0.0 | - | - | Yes | K2 shift factor for well-proximity effect |
| PKU0WE | 0.0 | - | - | | Mobility degradation factor for well-proximity effect |
| PKVTH0WE | 0.0 | - | - | Yes | Threshold shift factor for well-proximity effect |
| SCREF | 1.0e-6 | 0.0 | - | No | Reference distance to calculate SCA, SCB, and SCC (unit: m) |

| Parameter | Default | Min | Max | Bin | Description |
|-----------|---------|-----|-----|-----|---------------------|
| WEB | 0.0 | - | - | No | Coefficient for SCB |
| WEC | 0.0 | - | - | No | Coefficient for SCC |

BSIM-CMG Model (Version=105.03) — WPE Instance Parameters

| Parameter | Default | Min | Max | Description |
|-----------|---------|-----|-----|--|
| SC | 0.0 | 0.0 | - | Distance to a single well edge (unit: m) |
| SCA | 0.0 | 0.0 | - | Integral of the first distribution function for scattered well dopant |
| SCB | 0.0 | 0.0 | - | Integral of the second distribution function for scattered well dopant |
| SCC | 0.0 | 0.0 | - | Integral of the third distribution function for scattered well dopant |

BSIM-CMG Model — Deactivating Model Equations

The following are the parameter settings to turn-off BSIM-CMG model equations:

| Parameter | Description |
|---------------------------------------|---|
| CDSC=0 | Subthreshold slope degradation |
| CDSCD=0 | |
| CIT=0 | |
| ETA0=0 | Drain induced barrier lowering |
| DVT0=0 | V _t roll-off (at low drain bias) |
| K1RSCE=0 | Reverse short channel effect |
| QMFACTOR=0 | Quantum effect |
| QMTCENIV=0 | |
| QMTCENCV=0 | |
| UA=0 | Mobility degradation due to vertical field & Coulomb scattering |
| EU=1 (to prevent 0 to the 0'th power) | |
| UD=0 | |

Chapter 2: MOSFET Models

LEVEL 72: BSIM-CMG MOSFET Model

| Parameter | Description |
|-------------|--|
| RGEOMOD=0 | Source drain resistance |
| RSHS=0 | |
| RSHD=0 | |
| RDSMOD=0 | |
| RDSWMIN=0 | |
| RDSW=0 | |
| ASYMMOD=0 | Asymmetry Model |
| KSATIV=1000 | Drain saturation voltage |
| VSAT=1e9 | |
| NGATE=0 | Polysilicon Depletion |
| PCLM=0 | Channel Length Modulation |
| THETASAT=0 | Effect of velocity saturation in the linear region |
| PDIBL1=0 | Output conductance due to DIBL |
| PDIBL2=0 | |
| CGEOMOD=0 | Parasitic Capacitance |
| CFS=0 | |
| CFD=0 | |
| CGSO=0 | |
| CGDO=0 | |
| CSDESW=0 | |
| CGBO=0 | |
| ASEO=0 | |
| ADEO=0 | |
| IIMOD=0 | Impact Ionization |
| IGBMOD=0 | Gate Current |
| IGCMOD=0 | |
| GIDLMOD=0 | GIDL Current |
| NQSMOD=0 | NQS Gate Resistance |
| XRCRG1=0 | |

| Parameter | Description |
|------------|---------------------------|
| NOIA=0 | Flicker Noise |
| NOIB=0 | |
| NOIC=0 | |
| NTNOI=0 | Thermal Noise |
| SHMOD=0 | Self-heating |
| RGATEMOD=0 | Gate electrode resistance |

BSIM-CMG Model — Searching Models as Function of NFIN and L

BSIM-CMG uses NFIN and L (Length) to determine model bins. The automatic model selection program searches a data file for a MOSFET model where the NFIN and L are within the range specified in the MOSFET element statement. The simulation then uses this model statement. Note that NFIN, NFINMAX, and NFINMIN are double type numbers for bin selection.

The algorithm for automatic model selection based on NFIN and L is the same as conventional MOSFET.

To search a data file for MOSFET models within a specified range of NFIN and L:

- Provide a root extension for the model reference name (in the .MODEL statement).
- Use the model geometric range parameters (LMIN, LMAX, NFINMIN, and NFINMAX). These model parameters define the range of physical length and NFIN dimensions to which the MOSFET model applies.

BSIM-CMG Model — Binning Calculation

For a given L, NFIN, each model parameter $PARAM_i$ is calculated as a function of PARAM, a length-dependent term, LPARAM, a number of fins per finger (NFIN) dependent term, NPARAM, and a product $L \times NFIN$ term, PPARAM:

Chapter 2: MOSFET Models

LEVEL 72: BSIM-CMG MOSFET Model

$$PARAM_i = PARAM + \frac{10^{-6}}{L_{eff} + DLBIN} \cdot LPARAM + \frac{1.0}{NFIN} \cdot NPARAM + \frac{10^{-6}}{NFIN(L_{eff} + DLBIN)} \cdot PPARAM$$

For the list of binnable parameters, please refer to [BSIM-CMG Model Parameters \(Version >= 105\)](#).

BSIM-CMG Model — Additional Operating Point Outputs

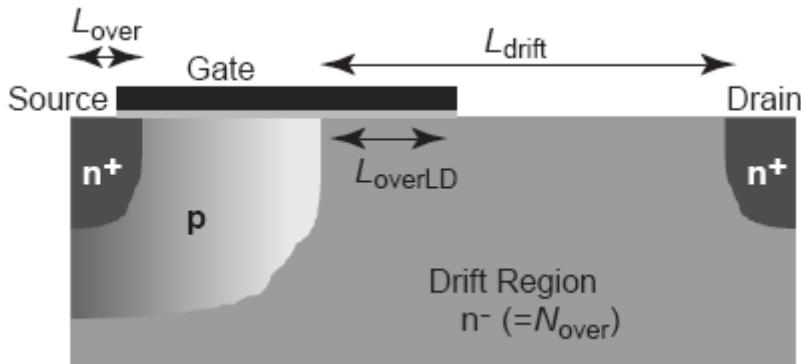
BSIM-CMG additional operating point outputs are available in BSIM-CMG version 105.03 or later. These additional operating point outputs include total capacitances and intrinsic capacitances. Additional operating point information is printed out when setting option `ext_op=1` (Default is 0).

| Name | Descriptions |
|-------|-------------------------------------|
| CGB | Total gate-to-bulk capacitance |
| CDG | Total drain-to-gate capacitance |
| CDS | Total drain-to-source capacitance |
| CDB | Total drain-to-bulk capacitance |
| CSD | Total source-to-drain capacitance |
| CSG | Total source-to-gate capacitance |
| CSB | Total source-to-bulk capacitance |
| CBD | Total bulk-to-drain capacitance |
| CBG | Total bulk-to-gate capacitance |
| CBS | Total bulk-to-source capacitance |
| CGGBO | Intrinsic gate capacitance |
| CGDBO | Intrinsic gate-to-drain capacitance |

| Name | Descriptions |
|-------|---------------------------------------|
| CGSBO | Intrinsic gate-to-source capacitance |
| CGBBO | Intrinsic gate-to-bulk capacitance |
| CSGBO | Intrinsic source-to-gate capacitance |
| CSDBO | Intrinsic source-to-drain capacitance |
| CSSBO | Intrinsic source capacitance |
| CSBBO | Intrinsic source-to-bulk capacitance |
| CDGBO | Intrinsic drain-to-gate capacitance |
| CDDBO | Intrinsic drain capacitance |
| CDSBO | Intrinsic drain-to-source capacitance |
| CDBBO | Intrinsic drain-to-bulk capacitance |
| CBGBO | Intrinsic bulk-to-gate capacitance |
| CBDBO | Intrinsic bulk-to-drain capacitance |
| CBSBO | Intrinsic bulk-to-source capacitance |
| CBBBO | Intrinsic bulk capacitance |

LEVEL 73: HiSIM_HV Model

HiSIM (Hiroshima University STARC IGFET Model) is the first complete surface-potential-based MOSFET model for circuit simulation based on the drift-diffusion theory, which was originally developed by Pao and Sah. The model has been extended for power MOSFETs by considering the resistance effect explicitly, which is named HiSIM_HV. There are two types of structures commonly used for high voltage applications. One is the asymmetrical laterally diffused structure called LDMOS and the other is originally the symmetrical structure, which we distinguish by referring to it as HVMOS. However, the asymmetrical HVMOS structure is also possible. HiSIM_HV is valid for modeling all these structure types. The most important features of LDMOS/HVMOS devices, different from the conventional MOSFET, originate from the drift region introduced to achieve the sustainability of high voltages. By varying the length and the dopant concentration of the drift region, various devices with various operating bias conditions are realized for the LDMOS structure:



Note: HSPICE currently supports Version 2.1.0 and earlier. When running this model with HSPICE Precision Parallel (HPP) the simulator automatically resets the version to the compatible one for the HPP technology and issues a warning message.

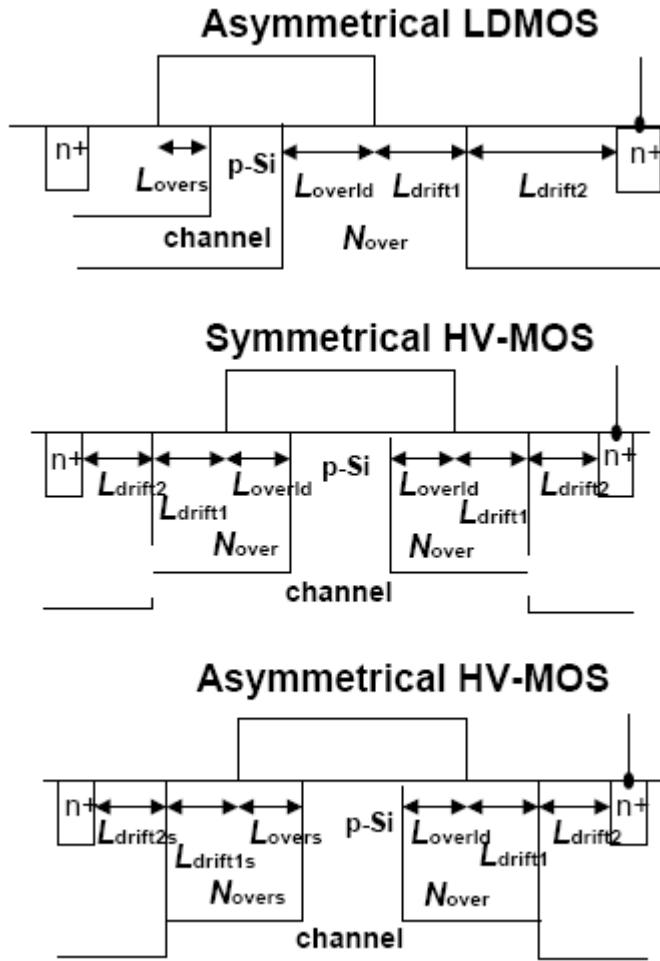


Figure 14 Device parameters in HiSIM_HV

To make the structural definition easy, the flag COSYM is introduced as shown in [Figure 15 on page 660](#). COSYM=0 refers to the asymmetrical LDMOS, and all structural parameters have to be determined independently. COSYM=1 refers to symmetrical/asymmetrical HVMOS. If parameter values of the source side are given, they are activated. If they are not given, parameter values of the drain side are copied to the source side automatically.

Chapter 2: MOSFET Models

LEVEL 73: HiSIM_HV Model

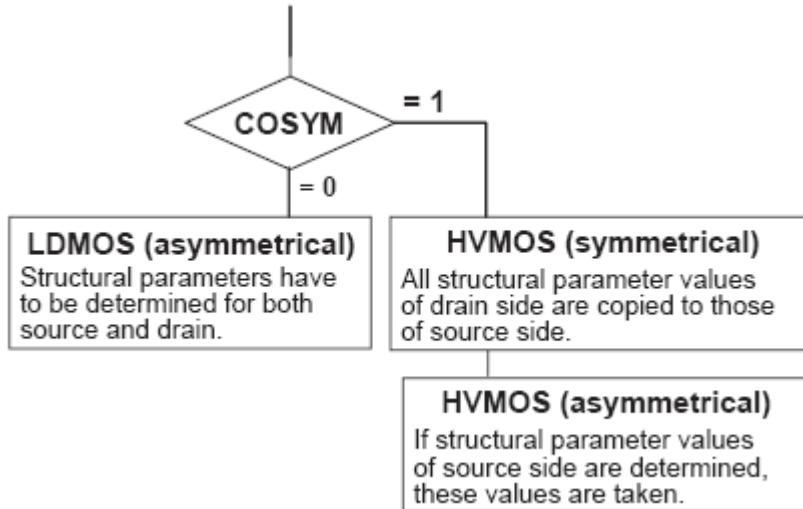


Figure 15 COSYM flag usage: =0 for LDMOS, =1 for HVMOS

Table 2 summarizes the structural parameters to be determined. If the overlap length LOVER is determined instead of LOVERS, then LOVER is taken for LOVERS. Model parameters for resistances at the source side and the drain side are distinguished by RS and RD for the asymmetrical HVMOS.

Table 2 HiSIM HV 1.2.0 model parameters introduced

| Flag | Structure | Source | Drain |
|---------|--------------------|--|---|
| COSYM=0 | LDMOS | LOVERS RS | LOVERLD LDRIFT1S LDRIFT2S NOVERS RD |
| COSYM=1 | Symmetrical HVMOS | - | LOVERLD LDRIFT1 LDRIFT2 NOVER RD |
| COSYM=1 | Asymmetrical HVMOS | LOVERS LDRIFT1S LDRIFT2S NOVERS RS | LOVERLD LDRIFT1S LDRIFT2S NOVERS RD |

The currently supported version includes the substrate node V_{sub} as schematically shown in [Figure 16 on page 661](#), where model parameters DDRIFT and NSUBSUB are newly introduced for Ddrift and Nsubsub, respectively. The node inclusion is done by selecting Flag COSUBNODE=0 as the 5th node.

For details and usage, and current parameters, contact the Synopsys support team.

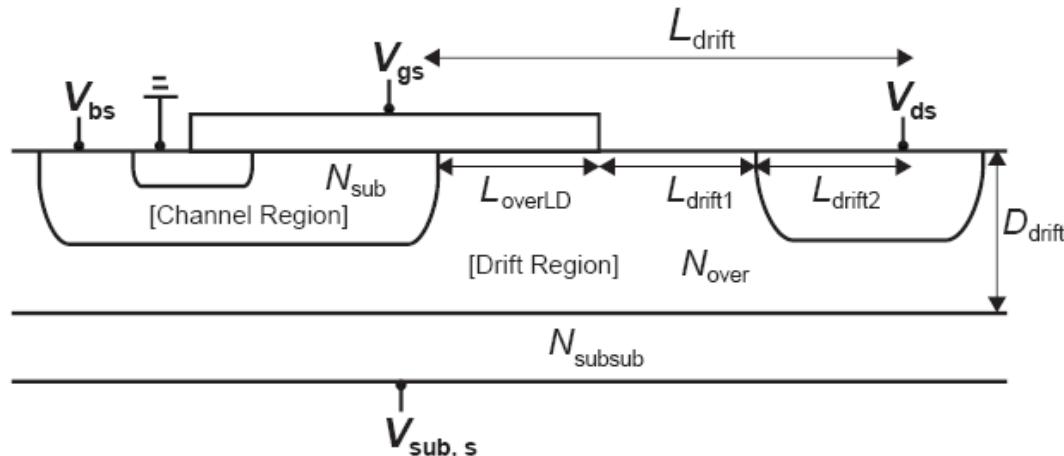


Figure 16 Schematic of a LDMOS with the substrate node V_{sub,s}

Note: HiSIM-LDMOS source code, and all copyrights, trade secrets or other intellectual property rights in and to the source code in its entirety, is owned by Hiroshima University and STARC.

This section covers the following topics:

- [HiSIM_HV Model — General Syntax](#)
- [HiSIM_HV Model Parameters](#)
- [HiSIM_HV Model Updates](#)
- [HiSIM_HV Model — Template Output](#)

HiSIM_HV Model — General Syntax

The following lists and describes the HiSIM_HV Level 73 general parameters.

```
Mxxx nd ng ns [nb] [nsub] [nth] mname [L=val] [W=val] [M=val]
+ [AD=val] [AS=val] [PD=val] [PS=val]
```

Chapter 2: MOSFET Models

LEVEL 73: HiSIM_HV Model

```
+ [NRS=val] [NRD=val] [XGW=val] [XGL=val]
+ [NF=val] [NGCON=val] [RBPB=val] [RBPD=val]
+ [RBPS=val] [SA=val] [SB=val] [SD=val] [DTEMP=val]
+ [NSUBCDFM=val] [SUBLD1=val] [SUBLD2=val]
+ [LDRIFT1=val] [LDRIFT2=val] [LDSRIFT1S=val] [LDRIFT2S=val]
+ [LOVER=val] [LOVERLD=val] [LOVERS=val]
+ [COSELFHEAT=val] [COSUBNODE=val]
```

Notes for Mxxx Card

- nd, ng, ns, nb: drain, gate, source, and bulk node, respectively
- nsub: substrate node
- nth: thermal node
- The square brackets “[]” indicate optional content which may be omitted.
- If 5 nodes are specified and COSUBNODE=0, the 5th node is nth.
 - If 5 nodes are specified and COSUBNODE=1, the 5th node is nsub.
 - The following table shows the effects when 6 nodes are specified for a specific version of HiSIM_HV model:

| Version | Effect |
|-------------------------|--|
| HiSIM_HV 1.2.4 or 2.1.0 | If COSUBNODE=0, HSPICE issues an error in parser. If COSUBNODE=1, the 5th node is nsub and 6th node is nth. |
| Earlier | The 5th node is nsub and the 6th node is nth no matter COSUBNODE is 0 1. |

- COSUBNODE is a new instance parameter and at the same time is recognized as a model parameter for the specification and the recognition of the node order.
- Originally COSELFHEAT was treated as a model parameter as other flags. It is additionally recognized as an instance parameter.
- See [HiSIM_HV Model Parameters](#) for model options and descriptions.

HiSIM_HV Model Parameters

This section covers the following topics:

- [HiSIM_HV Model — General Parameters](#)
- [HiSIM_HV Model — Control Option Flags](#)

HiSIM_HV Model — General Parameters

| Parameter | Default | Description |
|--------------------------------|-----------------------|--|
| L | $2.0\mu m$ | Gate length (L_{gate}) |
| W | $5.0\mu m$ | Gate width (W_{gate}) |
| Diode | | |
| AD | 0.0 | Area of drain junction |
| AS | 0.0 | Area of source junction |
| PD | 0.0 | Perimeter of drain junction |
| PS | 0.0 | Perimeter of source junction |
| Source/Drain Resistance | | |
| NRS | 1.0 | Number of source squares |
| NRD | 1.0 | Number of drain squares |
| Gate Resistance | | |
| M | 1.0 | Multiplication factor |
| NF | 1.0 | Number of gate fingers |
| NGCON | 1.0 | Number of gate contacts |
| XGL | 0.0 | Offset of the gate length |
| XGW | 0.0 | Distance from the gate contact to the channel edge |
| Substrate Network | | |
| RBPB | Model parameter value | Substrate Resistance Network |
| RBPD | Model parameter value | Substrate Resistance Network |
| RBPS | Model parameter value | Substrate Resistance Network |

Chapter 2: MOSFET Models

LEVEL 73: HiSIM_HV Model

| Parameter | Default | Description |
|-------------------------------------|-----------------------|---|
| RBDB | | Obsolete |
| RBSB | | Obsolete |
| Length of Diffusion | | |
| SA | 0.0 | Length of diffusion between gate and STI |
| SB | 0.0 | Length of diffusion between gate and STI |
| SD | 0.0 | Length of diffusion between gate and gate |
| Temperature | | |
| DTEMP | 0.0 | Device temperature change |
| SHEMAX | 500 | Limiter for the temperature increase due to the self-heating effect |
| Design for Manufacturability | | |
| NSUBCDFM | 0.0 | Substrate impurity concentration |
| Substrate Current | | |
| SUBLD1 | Model parameter value | Substrate current induced in L_{drift} |
| SUBLD2 | Model parameter value | Substrate current induced in L_{drift} |
| Resistance | | |
| LDRIFT1 | 0.0 | Length of lightly doped drift region |
| LDRIFT2 | $1.0 \mu m$ | Length of heavily doped drift region |
| LDRIFT1S | 0.0 | Length of lightly doped drift region in source side |
| LDRIFT2S | $1.0 \mu m$ | Length of heavily doped drift region in source side |
| Overlap | | |
| LOVER | 0.0 | Length of overlap region in source side for LDMOS |

| Parameter | Default | Description |
|------------|-----------------------|---|
| LOVERLD | Model parameter value | Length of overlap region in drain side |
| LOVERS | Model parameter value | Length of overlap region in source side for HVMOS |
| COSELFHEAT | Model parameter value | Flag to switch on the self-heating effect |
| COSUBNODE | Model parameter value | Flag for selection of the 5th node |

HiSIM_HV Model — Control Option Flags

| Description | Flag |
|---|--|
| Selects asymmetrical (LDMOS) or HVMOS structure | <ul style="list-style-type: none"> ■ COSYM = 0: asymmetrical LDMOS (default) ■ COSYM = 1: symmetrical and asymmetrical HVMOS |
| Include contact resistances Rs and Rd | <ul style="list-style-type: none"> ■ CORSRD= 0: no ■ CORSRD = 1 & $RS/ RD \neq 0$: yes, as internal resistance nodes ■ CORSD=2 & $RS/ RD \neq 0$: yes, analytical description ■ CORSD=3 & $RS/ RD \neq 0$: yes, both internal nodes and analytical description (default) ■ CORSRD = -1 & $RS/ RD \neq 0$: yes, as external resistance nodes |
| Adds overlap charges/capacitances to intrinsic ones | <ul style="list-style-type: none"> ■ COADOV = 0: no ■ COADOV = 1: yes (default) |
| Selects bias-dependent overlap capacitance model at drain side | <ul style="list-style-type: none"> ■ COOVL = 0: constant overlap capacitance ■ COOVL = 1: yes (default) including constant values as option |
| Selects bias-dependent overlap capacitance model at source side | <ul style="list-style-type: none"> ■ COOVLPS = 0: constant overlap capacitance ■ COOVLPS = 1: yes (default) including constant values as option |
| Selects method for calculating potential in overlap region | <ul style="list-style-type: none"> ■ COQOVSM = 0: analytical equation excluding inversion charge ■ COQOVSM = 1: iterative solution (default) ■ COQOVSM = 2: analytical equation including inversion charge |

Chapter 2: MOSFET Models

LEVEL 73: HiSIM_HV Model

| Description | Flag |
|--|---|
| Considers self-heating effect | <ul style="list-style-type: none"> ■ COSELFHEAT = 0: no (default) ■ COSELFHEAT = 1: yes |
| Calculates substrate current I_{sub} | <ul style="list-style-type: none"> ■ COISUB = 0: no (default) ■ COISUB = 1: yes |
| Calculates gate current I_{gate} | <ul style="list-style-type: none"> ■ COIIGS = 0: no (default) ■ COIIGS = 1: yes |
| Calculates GIDL current I_{GIDL} | <ul style="list-style-type: none"> ■ COGIDL = 0: no (default) ■ COGIDL = 1: yes |
| Calculates STI leakage current $I_{ds,STI}$ | <ul style="list-style-type: none"> ■ COISTI = 0: no (default) ■ COISTI = 1: yes |
| Invokes non-quasi-static | <ul style="list-style-type: none"> ■ CONQS = 0: no (default) ■ CONQS = 1: yes |
| Includes gate-contact resistance | <ul style="list-style-type: none"> ■ CORG = 0: no (default) ■ CORG = 1: yes |
| Invokes substrate resistance network | <ul style="list-style-type: none"> ■ CORBNET = 0: no (default) ■ CORBNET = 1: yes |
| Calculates 1/f noise | <ul style="list-style-type: none"> ■ COFLICK = 0: no (default) ■ COFLICK = 1: yes |
| Calculates thermal noise | <ul style="list-style-type: none"> ■ COTHRML = 0: no (default) ■ COTHRML = 1: yes |
| Calculates induced-gate and cross-correlation noise | <ul style="list-style-type: none"> ■ COIGN = 0 & COTHRML = 0: no (default) ■ COIGN = 1 & COTHRML = 1: yes |
| Uses previous $_S$ for the iteration | <ul style="list-style-type: none"> ■ COPPRV = 0: no ■ COPPRV = 1: yes (default) |
| Considers parameter variations for DFM support | <ul style="list-style-type: none"> ■ CODFM = 0: no (default) ■ CODFM = 1: yes |
| Uses previous I_{ds} is used for calculating source/drain resistance effect <i>(RSand or RD ≠ 0)</i> : This flag is deactivated. | <ul style="list-style-type: none"> ■ COIPRV = 0: no ■ COIPRV = 1: yes (default) |

| Description | Flag | | | | |
|--|---|----------------|-----------|--------------|--|
| Selects temperature dependence of models | $R_{d0,temp}$ | $R_{dvd,temp}$ | V_{max} | N_{invd} | |
| | ■ COTEMP=0 T T0 and backward compatible) | T0 | T0 | T0 (default) | |
| | ■ COTEMP=1 T0 T0 | T0 | T0 | T0 | |
| | ■ COTEMP=2 T T T T | T | T | T | |
| | ■ COTEMP=3 T T T0 T0 | T0 | T0 | T0 | |
| | where T includes the temperature increase by the self-heating effect and T0 omits it. | | | | |
| Selects the 5th node | ■ COSUBNODE = 0: the 5th node is the thermal node. ■ COSUBNODE = 1: the 5th node is the Vsub node. | | | | |
| Selects the Ldrift | ■ COLDRIIFT = 0: Ldrift includes LOVER (default & backward compatible) ■ COLDRIIFT = 1: without LOVER. | | | | |
| Selection for output message whether model parameter is within recommended range | ■ COERRREP = 0: no message is given. ■ COERRREP = 1: range check result is given (default). | | | | |

HiSIM_HV Model Updates

This section covers the following topics:

- [HiSIM_HV Version 2.1.0 Updates](#)
- [HiSIM_HV Version 2.0.1 Updates](#)
- [HiSIM_HV Version 2.0.0 Updates](#)
- [HiSIM_HV Version 1.2.4 Updates](#)
- [HiSIM_HV Version 1.2.3 Updates](#)
- [HiSIM_HV Version 1.2.1 Updates](#)
- [HiSIM_HV Version 1.1.2 Updates](#)
- [HiSIM_HV Version 1.0.1 and 1.0.2 Updates](#)
- [HiSIM-LDMOS 100 Updates](#)

HiSIM_HV Version 2.1.0 Updates

The following are the highlights of the HiSIM_HV version 2.1.0 upgrade:

1. Changed model descriptions:

- Degradation of the mobility in the drift region with new model parameter RDRBB.

Chapter 2: MOSFET Models

LEVEL 73: HiSIM_HV Model

- Additional overlap capacitance with new model parameter QOVADD.
 - Improved smoothness of drift resistance at $V_{DS}=0$.
2. Changed default/min/max values of model parameters NOVER, NOVERS, SCP1, SC1, FN1, NSTI, RDRMAX, RDRQOVER, QME1, and QME2 in the source code.
 3. Changed range check method of model parameter VFBC.
 4. Bug fixes:
 - Range check of CGSO, CGDO, CGBO, NSUBCDFM, SUB2L, and SC4.
 - Calculation of the derivatives.
 - Temperature dependence of the output parameter VON for the threshold voltage.
 - Removal of unnecessary code.
 - Removal of the function FABS (Verilog-A code only).
 - NF dependence of RD, RDVD, RD23, and RTH.
 - Removal of unused variables.
 - Calculation of the temperature derivatives.
 - Temperature dependence of the output parameter Vth.
 - Error check of the 6th node.
 - Inconsistency between Verilog-A code and C-code.
 - Calculation of the output parameter Vdsat.
 - Redundant calculations of the temperature variables.
 - Duplicated output of error message.

HiSIM_HV Version 2.0.1 Updates

The following are the highlights of the HiSIM_HV version 2.0.1 upgrade:

Bug Fixes:

- Missing initialization of NSUBC, NSUBP and MUEPH1 in the hsmhvtemp.c for repeating simulation.
- Reference voltage (**Vbs -> Vbse**) in the Qover model used when model parameter CVDSOVER != 0.
- Derivative calculations with respect to temperature (C code only).

- Maximum gate width for the range check when instance parameter `NF != 1`.
- Derivative calculations in the `Qover` model code (`hsmhveval_qover.h`) (C code only).
- Floating point exception in the `QME` model code.
- Floating point exception in the smoothing functions.
- Floating point exception when model parameters `RDVDL << 0` and `RD23L << 0`.
- Floating point exception when model flag/parameters `COSUBNODE != 0`, `COSYM=0` and `NOVER * (NSUBSUB+NOVER) = 0`.
- Floating point exception when model flag `CORDRIFT=1` and model parameter `RDRDJUNC = 0`.
- Derivative calculations when model parameter `COSUBNODE = 1` (C code only).
- Different maximum values of model parameters `RSH` and `RSHG` from User's Manual.
- Inactivated model parameter `RSH` and instance parameter `NRS` when model flag `CORDRIFT = 1`.
- Incorrect clamping of the `Vbs` when `Vbs > 0` (Verilog-A code only).
- Incorrect minimum resistance value `RMIN` (Verilog-A code only).
- Incorrect gate resistance definition when model flag `CORG = 1` and model parameters `RSHG > 0` (Verilog-A code only).

HiSIM_HV 2.0.1 — Junction Diode Model Parameters

Following are the junction diode model parameters:

- `sbdb_dio`: [General Junction Diode Parameters](#)
- `t_cap_dio`: [Temperature Dependence of Junction Capacitance Parameters](#)
- `d_dio`: [Drain Diode Parameters](#)

Chapter 2: MOSFET Models

LEVEL 73: HiSIM_HV Model

- `s_dio`: Source Diode Parameters
- `g_sbdb_dio`, `g_d_dio`, `g_s_dio`: Geometry Dependence of Diode Parameters

Table 3 General Junction Diode Parameters

| Name | Default | Unit | Description |
|-------|---------|------------------|---|
| JS0 | 0.5E-6 | A/m ² | Saturation current density |
| JS0SW | 0.0 | A/m | Side wall saturation current density |
| NJ | 1.0 | - | Emission coefficient |
| NJSW | 1.0 | | Sidewall emission coefficient |
| XTI | 2.0 | - | Junction current temperature exponent coefficient |
| CJ | 5.0E-04 | F/m ² | Bottom junction capacitance per unit area at zero bias |
| CJSW | 5.0E-10 | F/m | Source/drain sidewall junction capacitance grading coefficient per unit length at zero bias |
| CJSWG | 5.0E-10 | F/m | Source/drain gate sidewall junction capacitance per unit length at zero bias |
| MJ | 5.0E-0 | | Bottom junction capacitance grading coefficient |
| MJSW | 0.33E0 | | Source/drain sidewall junction capacitance grading coefficient |
| MJSWG | 0.33E0 | | Source/drain gate sidewall junction capacitance grading coefficient |
| PB | 1.0E0 | V | Bottom junction build-in potential |
| PBSW | 1.0E0 | V | Source/drain sidewall junction build-in potential |
| PBSWG | 1.0E0 | V | Source/drain gate sidewall junction build-in potential |
| XTI2 | 0.0E0 | - | Temperature coefficient |
| CISB | 0.0E0 | - | Reverse bias saturation current |
| CVB | 0.0E0 | - | Bias dependence coefficient of cisb |
| CTEMP | 0.0E0 | - | Temperature coefficient |

Table 3 General Junction Diode Parameters

| Name | Default | Unit | Description |
|--------|---------|------|--|
| CISBK | 0.0E0 | A | Reverse bias saturation current |
| CVBK | CVB | - | Inactivated by CVB |
| DIVX | 0.0E0 | | [1/V] |
| VDIFFJ | 0.6E-3 | V | Threshold voltage for S/D junction diode |

Table 4 Temperature Dependence of Junction Capacitance Parameters

| Name | Default | Unit | Description |
|----------|---------|------|---------------------------------|
| TCJBD | 0.0 | | Temperature dependence of cjbd |
| TCJBS | 0.0 | | Temperature dependence of cjbs |
| TCJBDSW | 0.0 | | Temperature dependence of cjbds |
| TCJBSSW | 0.0 | | Temperature dependence of cjbss |
| TCJBDSWG | 0.0 | | Temperature dependence of cjbds |
| TCJBSSWG | 0.0 | | Temperature dependence of cjbss |

Table 5 Drain Diode Parameters

| Name | Default | Unit | Description |
|--------|---------|------------------|---|
| JS0D | JS0 | A/m ² | Saturation current density for drain junction |
| JS0SWD | JS0SW | A/m | Side wall saturation current density for drain junction |
| NJD | NJ | - | Emission coefficient for drain junction |
| NJSWD | NJSW | | Sidewall emission coefficient for drain junction |
| XTID | XTI | - | Junction current temperature exponent coefficient for drain junction |
| CJD | CJ | F/m ² | Bottom junction capacitance per unit area at zero bias for drain junction |
| CJSWD | CJSW | F/m | Sidewall junction capacitance grading coefficient per unit length at zero bias for drain junction |

Chapter 2: MOSFET Models

LEVEL 73: HiSIM_HV Model

Table 5 Drain Diode Parameters

| Name | Default | Unit | Description |
|---------|---------|------|--|
| CJSWGD | CJSWG | F/m | Gate sidewall junction capacitance per unit length at zero bias for drain junction |
| MJD | MJ | | Bottom junction capacitance grading coefficient for drain junction |
| MJSWD | MJSW | | Sidewall junction capacitance grading coefficient for drain junction |
| MJSWGD | MJSWG | | Gate sidewall junction capacitance grading coefficient for drain junction |
| PBD | PB | V | Bottom junction build-in potential for drain junction |
| PBSWD | PBSW | V | Sidewall junction build-in potential for drain junction |
| PBSWGD | PBSWG | V | Gate sidewall junction build-in potential for drain junction |
| XTI2D | XTI2 | - | Temperature coefficient for drain junction |
| CISBD | CISB | - | Reverse bias saturation current for drain junction |
| CVBD | CVB | - | Bias dependence coefficient of cisb for drain junction |
| CTEMPD | CTEMP | - | Temperature coefficient for drain junction |
| CISBKD | CISBK | A | Reverse bias saturation current for drain junction |
| DIVXD | DIVX | 1/V | Reverse coefficient coefficient for drain junction |
| VDIFFJD | VDIFFJ | V | Threshold voltage for junction diode for drain junction |

Table 6 Source Diode Parameters

| Name | Default | Unit | Description |
|--------|---------|-------|--|
| JS0S | JS0D | A/m^2 | Saturation current density for source junction |
| JS0SWS | JS0SWD | A/m | Side wall saturation current density for source junction |
| NJS | NJD | - | Emission coefficient for source junction |

Table 6 Source Diode Parameters

| Name | Default | Unit | Description |
|---------|---------|------------------|--|
| NJSWS | NJSWD | | Sidewall emission coefficient for source junction |
| XTIS | XTID | - | Junction current temperature exponent coefficient for source junction |
| CJS | CJD | F/m ² | Bottom junction capacitance per unit area at zero bias for source junction |
| CJSWS | CJSWD | F/m | Sidewall junction capacitance grading coefficient per unit length at zero bias for source junction |
| CJSWGS | CJSWGD | F/m | Gate sidewall junction capacitance per unit length at zero bias for source junction |
| MJS | MJD | | Bottom junction capacitance grading coefficient for source junction |
| MJSWS | MJSWD | | Sidewall junction capacitance grading coefficient for source junction |
| MJSWGS | MJSWGD | | Gate sidewall junction capacitance grading coefficient for source junction |
| PBS | PBD | V | Bottom junction build-in potential for source junction |
| PBSWS | PBSWD | V | Sidewall junction build-in potential for source junction |
| PBSWGS | PBSWGD | V | Gate sidewall junction build-in potential for source junction |
| XTI2S | XTI2D | - | Temperature coefficient for source junction |
| CISBS | CISBD | - | Reverse bias saturation current for source junction |
| CVBS | CVBD | - | Bias dependence coefficient of cisb for source junction |
| CTEMPS | CTEMPD | - | Temperature coefficient for source junction |
| CISBKS | CISBKD | A | Reverse bias saturation current for source junction |
| DIVXS | DIVXD | 1/V | Reverse coefficient coefficient for source junction |
| VDIFFJS | VDIFFJD | V | Threshold voltage for junction diode for source junction |

Chapter 2: MOSFET Models

LEVEL 73: HiSIM_HV Model

Table 7 *Geometry Dependence of Diode Parameters*

| Name | Default | Unit | Description |
|-------------|----------------|-------------|------------------------------|
| LJS0 | 0.0 | | Length dependence of js0 |
| LJS0SW | 0.0 | | Length dependence of js0sw |
| LNJ | 0.0 | | Length dependence of nj |
| LCISBK | 0.0 | | Length dependence of cisbk |
| LVDIFFJ | 0.0 | | Length dependence of vdiffj |
| LJS0D | LJS0 | | Length dependence of js0d |
| LJS0SWD | LJS0SW | | Length dependence of js0swd |
| LNJD | LNJ | | Length dependence of njd |
| LCISBKD | LCISBK | | Length dependence of cisbkd |
| LVDIFFJD | LVDIFFJ | | Length dependence of vdiffjd |
| LJS0S | LJS0D | | Length dependence of js0s |
| LJS0SWS | LJS0SWD | | Length dependence of js0sws |
| LNJS | LNJD | | Length dependence of njs |
| LCISBKS | LCISBKD | | Length dependence of cisbks |
| LVDIFFJS | LVDIFFJD | | Length dependence of vdiffjs |
| WJS0 | 0.0 | | Width dependence of js0 |
| WJS0SW | 0.0 | | Width dependence of js0sw |
| WNJ | 0.0 | | Width dependence of nj |
| WCISBK | 0.0 | | Width dependence of cisbk |
| WVDIFFJ | 0.0 | | Width dependence of vdiffj |
| WJS0D | WJS0 | | Wength dependence of js0d |
| WJS0SWD | WJS0SW | | Wength dependence of js0swd |
| WNJD | WNJ | | Wength dependence of njd |

Table 7 Geometry Dependence of Diode Parameters

| Name | Default | Unit | Description |
|----------|----------|------|----------------------------------|
| WCISBKD | WCISBK | | Wength dependence of cisbkd |
| WVDIFFJD | WVDIFFJ | | Wength dependence of vdiffjd |
| WJS0S | WJS0D | | Wength dependence of js0s |
| WJS0SWS | WJS0SWD | | Wength dependence of js0sws |
| WNJS | WNJD | | Wength dependence of njs |
| WCISBKS | WCISBKD | | Wength dependence of cisbks |
| WVDIFFJS | WVDIFFJD | | Wength dependence of vdiffjs |
| PJS0 | 0.0 | | Cross-term dependence of js0 |
| PJS0SW | 0.0 | | Cross-term dependence of js0sw |
| PNJ | 0.0 | | Cross-term dependence of nj |
| PCISBK | 0.0 | | Cross-term dependence of cisbk |
| PVDIFFJ | 0.0 | | Cross-term dependence of vdiffj |
| PJS0D | PJS0 | | Cross-term dependence of js0d |
| PJS0SWD | PJS0SW | | Cross-term dependence of js0swd |
| PNJD | PNJ | | Cross-term dependence of njd |
| PCISBKD | PCISBK | | Cross-term dependence of cisbkd |
| PVDIFFJD | PVDIFFJ | | Cross-term dependence of vdiffjd |
| PJS0S | PJS0D | | Cross-term dependence of js0s |
| PJS0SWS | PJS0SWD | | Cross-term dependence of js0sws |
| PNJS | PNJD | | Cross-term dependence of njs |
| PCISBKS | PCISBKD | | Cross-term dependence of cisbks |
| PVDIFFJS | PVDIFFJD | | Cross-term dependence of vdiffjs |

HiSIM_HV Version 2.0.0 Updates

The following are the highlights of the HiSIM_HV version 2.0.0 upgrade:

1. Improvements of fitting capability (Refer to the *HiSIM HV 2.0.0 User's Manual* for detailed description).
 - Length dependence of `Rdrift` with new model parameters `RDRVMAXL`, `RDRVMAXLP`, `RDRMUEL`, and `RDRMUEL`.
 - Addition of overlap charge to the carrier concentration of the drift region with new model parameter `RDRQOVER`.
 - Modification of `Rdrift` for improved small `Vds` fitting with introduction of new model parameters `RDRLOWVD1` and `RDRLOWVD2`.
 - Increase of upper limitation for `Rdrift` from 50000 Ohm to 500000 Ohm.
2. Bug Fixes:
 - Floating-point exception for large drain voltage when `COQOVSM=2`.
 - Incorrect recognition of the 5th terminal connected to ground (0) when `COSUBNODE=0`.
 - Removal the unnecessary program statements.

Note: The HiSIM_HV 2.0.0 model does not currently support Template output.

HiSIM_HV Version 1.2.4 Updates

The following are the highlights of the HiSIM_HV version 1.2.4 upgrade:

Bug fixes:

- Incorrectly Referencing `Total W` Instead of `W per Finger`.
- Derivative calculations with respect to temperature (C code only).
- Convergence and `Flg_subNode` setting.

HiSIM_HV Version 1.2.3 Updates

The following are the highlights of the HiSIM_HV version 1.2.3 upgrade:

Bug fixes:

- Missing initialization of `NSUBC`, `NSUBP`, and `MUEPH1` in the `hsmhvtemp.c` for repeating simulation.
- Inaccurate overlap capacitance when model parameter `CVDSOVER !=0`.

- Reference voltage ($V_{BS} \rightarrow V_{BSE}$) in the Q_{OVER} model used when model parameter $CVDSOVER != 0$.
- Derivative calculations with respect to temperature (C code only).
- Maximum gate width for the range check when model parameter $NF != 1$.
- Derivative calculations in the Q_{OVER} model code (`hsmhveval_qover.h`) (C code only).
- Floating point exception in the Q_{ME} model code.
- Floating point exception in the smoothing functions.
- Floating point exception when model parameters $RDVDL << 0$ and $RD23 << 0$.
- Floating point exception when model flag/parameters $COSUBNODE != 0$, $COSYM=0$, and $NOVER^* (NSUBSUB+NOVER) = 0$.
- Different default value of some model parameters from User Manual.
- Different minimum value and/or the maximum value of some model parameters from User Manual.
- Incorrect clamping of the V_{BS} when $V_{BS} > 0$ (Verilog-A code only).
- Incorrect minimum resistance value $RMIN$ (Verilog-A code only).
- Incorrect gate resistance definition when model flag $CORG=1$ and model parameter $RSHG > 0$ (Verilog-A code only).

HiSIM_HV Version 1.2.1 Updates

The following are the highlights of the HiSIM_HV version 1.2.1 upgrade:

1. Improvements in the lateral-field-induced charge (Q_Y) model.
2. Improvements in the overlap capacitance (Q_{OVER}) model. New options are provided to calculate Q_{OVER} . These options are selected by the flag $COQOVSM$:
 - $COQOVSM=0$: Q_{OVER} is calculated with an analytical equation excluding the inversion charge.
 - $COQOVSM=1$: Q_{OVER} is calculated with an iterative procedure including the inversion charge (Default).
 - $COQOVSM=2$: Q_{OVER} is calculated with an analytical equation including the inversion charge (HiSIM_HV 1.1.1 original).
3. A limiter for the temperature increase due to the self-heating effect is introduced by the model parameter $SHEMAX$ (Default=500).

Chapter 2: MOSFET Models

LEVEL 73: HiSIM_HV Model

4. The V_{bs} clamping (add temperature dependence to V_{bs_max}) is changed to fix a discontinuity in C_{dd}-V_{ds} at T=125.
5. Fixed derivative calculation.
6. Fixed typo in model ask function for parameter PB.
7. Fixed calculation of the drift resistance when COSYM=0 and the V_{sub} node connected to 0.

HiSIM_HV Version 1.1.2 Updates

The following are the highlights of the HiSIM_HV version 1.1.2 upgrade:

- Improvements in the lateral-field-induced charge (Q_y) model
- Improvements in the overlap capacitance (Q_{over}) model
- New options are provided to calculate Q_{over}. These options are selected by the flag COQOVSM:
 - COQOVSM=0 : Q_{over} is calculated with an analytical equation excluding the inversion charge.
 - COQOVSM=1 : Q_{over} is calculated with an iterative procedure including the inversion charge (Default)
 - COQOVSM=2 : Q_{over} is calculated with an analytical equation including the inversion charge (HiSIM_HV 1.1.1 original).
- A limiter for the temperature increase due to the self-heating effect is introduced by the model parameter SHEMAX (Default=500).
- The V_{bs} clamping (add temperature dependence to V_{bs_max}) is changed to fix a discontinuity in C_{dd}-V_{ds} at T=125
- Derivative calculation in the IBPC model
- Derivative calculation in the I_{sub} model: missing I_{sub}_dVdse
- Floating-point exception issue in the I_{sub} model
- Floating-point exception issue in the Vdseff calculation
- Floating-point exception issue for RD23
- Ra model
- Parameter handling with COSYM
- Small resistance cases: introduction of Res_min
- Improvement of the drain-side surface potential (Ps1) iteration

- Pds clippings
- Typo in model ask function for parameter PB

HiSIM_HV Version 1.0.1 and 1.0.2 Updates

HSPICE supports HiSIM_HV version 1.0.1 and 1.0.2 to address the need for accurate modeling of high-voltage MOSFETs, Hiroshima University and STARC developed the HISIM-HVMOS model as an extension to the IGFET model. The HVMOS model focuses on symmetrical structure while the HiSIM-LDMOS model is used for asymmetrical structures. According to the *HiSIM_HV User Guide*: the most important advantage of the surface-potential-based modeling is the unified description of device characteristics for all bias conditions. The physical reliability of the drift-diffusion theory has been proved by 2-D device simulations with channel lengths even down to below 0.1 μm . To obtain analytical solutions for describing device performances, the charge sheet approximation of the inversion layer with zero thickness has been introduced. Together with the gradual-channel approximation all device characteristics are then described analytically by the channel-surface potentials at the source side (S0) and at the drain side (SL) (see [Figure 17](#)).

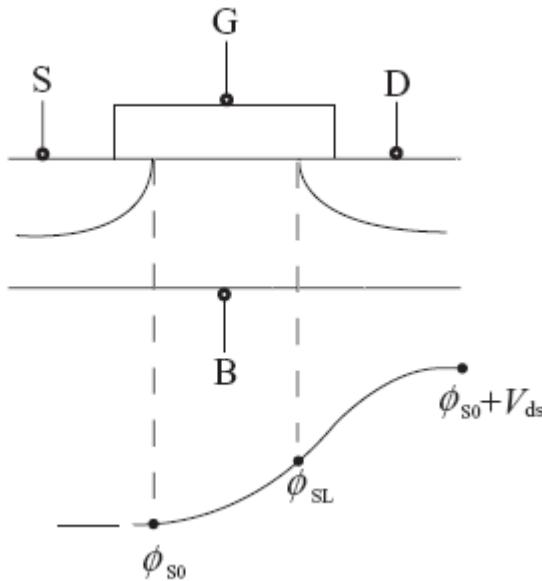


Figure 17 Schematic of the surface potential distribution in the channel

These surface potentials are functions of applied voltages on the four terminals: the gate voltage V_g , the drain voltage V_d , the bulk voltage V_b and the reference potential of the source V_s . The resistance in the contact region causing

potential drops also affects the surface potential values. Since the surface potentials are implicit functions of the applied voltages, model-internal iteration procedures are introduced only for calculating ϕ_{S0} , and ϕ_{SL} is calculated in addition to the global iteration of the circuit simulator.

The potential $\phi_s(\Delta L)$ is calculated with ϕ_{S0} , ϕ_{SL} , and V_{ds} together with a fitting parameter.

The most important features of LDMOS/HVMOS devices, different from the conventional MOSFET, originate from the drift region introduced to achieve the sustainability of high voltages. By varying the length as well as the dopant concentration of the drift region, various devices with various operating bias conditions are realized. In many cases, the drift region acts as the resistance for the current flow and also induces additional charge, which causes the especially unique features of the LDMOS capacitances. Thus, accurate modeling of the drift region is the main task of HiSIM-LDMOS/HV.

For the LDMOS/HVMOS devices the iterative solution is only one possible to model the specific features of this device accurately, because the resistance effect in the drift region is dependent on the bias condition as well as the detailed geometrical LDMOS/HVMOS structure. The basic modeling method is taken over from the HiSIM2 model for advanced MOSFETs, and additional equations for capturing the drift-region effects are included. Since the overlap length is relatively long for LDMOS/HVMOS, accurate surface potential calculation for the overlap region as a function of applied voltages is also necessary for accurate prediction of the high-voltage MOS capacitances.

HiSIM-LDMOS 100 Updates

The following changes were made in the HiSIM-LDMOS 100 model as reported in the SC1 through SC3 release notes provided by Hiroshima University/STARC.

- SC1:
 - Self-heating effect Temperature node is handled as an internal node.
 - The model parameter RD26 was deleted, and the smoothing parameter was fixed to a constant value.
 - Qover Overlap Capacitance: The model description of Qover was changed from external bias to internal bias.
 - The charge-partitioning scheme with model parameters QOVRAT1 and QOVRAT2 was deactivated.

- The new model parameter RD26 was introduced to fit transition characteristics at depletion and/or inversion.
- SC2:
 - The self-heating effect (`COSELFHEAT=1`) was stabilized for HSPICE. The temperature node can be treated either as an external or internal node.
 - The NF dependability in the drift resistance model was removed for improved accuracy.
- SC3:
 - The self-heating effect became applicable for AC analysis
 - Introduction of drift-length (`LDRIFT`) dependence of the drift resistance.
 - Introduction of model parameters `RDTEMP1` and `RDTEMP2` for temperature dependent drift resistance.

Extension to LDMOS and HVMOS: To facilitate the structural definition, the `COSYM` flag was introduced with HiSIM-HV1.0.0. **`COSYM=0`** refers to the asymmetrical LDMOS, and all drain-side and source-side parameters of the drain side are copied to the source side. **`COSYM=1`** refers to symmetrical HVMOS, and all parameters have to be determined independently. HiSIM_HV considers the length of the drift region L_{drift} , the overlap length L_{over} , and the impurity concentration of the drift region N_{over} explicitly. In the HVMOS case, the parameter values for the drain side have to be determined, and are copied to the source side automatically. If parameters are not determined, default values are taken.

HiSIM_HV Model — Template Output

HSPICE supports parameter template output for all existing versions, HiSIM-HVMOS 1.00, 1.01, 1.02, 1.10, 1.11, 1.12, 1.20, 1.21, 1.23, 2.00, 2.01, and 2.10. See [Output Templates for HiSIM_HV, Level=73](#).

LEVEL 74: MOS Model 20 Model

MOS Model 20 (MM20) is a compact MOSFET model developed by NXP, intended for analog circuit simulation in high-voltage MOS technologies. MOS Model 20 describes the electrical behavior of the region under the thin gate oxide of a high-voltage MOS device, similar to a Lateral Double-diffused MOS (LDMOS) device or an extended-drain MOSFET. It combines the MOSFET-operation of the channel region with that of the drift region under the thin gate oxide in a high-voltage MOS device. As such, MOS Model 20 is aimed as a successor of the combination of MOS Model 9 (MM9) for the channel region in series with MOS Model 31 (MM31) for the drift region under the thin gate oxide, in macro models of various high-voltage MOS devices. MOS Model 20 has especially been developed to improve the convergence behavior during simulation, by having the voltage at the transition from the channel region to the drift region calculated inside the model itself.

Please check following URL from NXP for original MOS Model 20 release and documentation.

http://www.nxp.com/models/hv_models/model20/

The following sections discuss these topics:

- [MOS Model 20 Model — General Syntax](#)
 - [MOS Model 20 Model — Instances and Parameters](#)
-

MOS Model 20 Model — General Syntax

Mxxxxx drain gate source bulk *mname* W=*val* Wd=*val* ...

MOS Model 20 Model — Instances and Parameters

JUNCAP 200.2 is supported in HSPICE MOS Model 20 as an alternative to the MOSFET junction diode model. You can use model parameter, JUNCAPMOD=1, to invoke Juncap200.2.

This section covers the following topics:

- [MOS Model 20 — Instance Parameters](#)
- [MOS Model 20 — Geometrical Parameters](#)
- [MOS Model 20 — Electrical Parameters](#)

MOS Model 20 — Instance Parameters

| Name | Unit | Default | Description |
|------|------|---------|-----------------------------------|
| W | m | 2E-5 | Drawn width of the channel region |
| WD | m | 2E-5 | Drawn width of the drift region |
| MULT | | 1 | Number of devices in parallel |

MOS Model 20 — Geometrical Parameters

| Name | Unit | Default | Description |
|-----------|------------------|----------|---|
| LEVEL | | 74 | HSPICE model level as 74 for MOS Model 20 |
| VERSION | | 2002.2 | VERSION 2002.2 is the default version number to define NXP model level 2002 |
| GEOMOD | | 1 | GEOMOD is used as a switch between geometrical model and electrical model, 0 for geometrical model and 1 for electrical model |
| JUNCAPMOD | | 0 | JUNCAPMOD as a switch of juncap200.2 model effective, 0 for off and 1 for on |
| A1CHR | | 15 | Factor of channel weak avalanche current, at reference temperature |
| A1DRR | | 15 | Factor of drift weak avalanche current, at reference temperature |
| A2CH | V | 73 | Exponent of weak avalanche current, related to channel |
| A2DR | V | 73 | Exponent of weak avalanche current, related to drift |
| A3CH | | 0.8 | Factor of the internal drain-source voltage, above which channel weak avalanche occurs |
| A3DR | | 0.8 | Factor of the internal drain-source voltage, above which drift weak avalanche occurs |
| ALP | | 0.002 | Factor for channel length modulation |
| ATH | | 0 | Temperature coefficient of the thermal resistance |
| BETACCW | A/V ² | 7.00E-05 | Gain factor of drift region of 1 um wide, at reference temperature |
| BETW | A/V ² | 7.00E-05 | Gain factor of a channel region of 1 um wide, at reference temperature |

Chapter 2: MOSFET Models

LEVEL 74: MOS Model 20 Model

| Name | Unit | Default | Description |
|-----------|--------------------|----------|---|
| CGDOW | F | 0 | Gate-to-drain overlap capacitance for a drift region of 1 um wide |
| CGSOW | F | 0 | Gate-to-source overlap capacitance for a drift region of 1 um wide |
| COXDW | F | 7.5E-16 | Oxide capacitance for an intrinsic drift region of 1 um wide |
| COXW | F | 7.5E-16 | Oxide capacitance for an intrinsic channel region of 1 um wide |
| CTH | J/K | 3.00E-09 | Thermal capacitance |
| DTA | K | 0 | Temperature offset to the ambient temperature |
| ETABET | | 1.6 | Temperature scaling exponent for BET |
| ETABETACC | | 1.5 | Temperature scaling exponent for BETACC |
| ETARD | | 1.5 | Temperature scaling exponent for RD |
| ETATHE3 | | 1 | Temperature scaling exponent for THE3 |
| ETATHE3D | | 1 | Temperature scaling exponent for THE3D |
| KODR | V ^(1/2) | 1 | Body factor of the drift region of an infinitely wide transistor |
| KOR | V ^(1/2) | 1.6 | Body factor of the channel region of an infinitely wide transistor |
| LAMD | | 0.2 | Quotient of the depletion layer thickness to the effective thickness of the drift region at VSB = 0 V |
| MEXP | | 2 | Smoothing factor for transition from linear to saturation regime |
| MEXPD | | 2 | Smoothing factor for transition from linear to quasi-saturation regime |
| MO | V | 0 | Parameter for the (short-channel) sub-threshold slope |
| MSDIBL | | 3 | Exponent for the drain-induced barrier lowering dependence on the backgate bias |
| NFAW | $V^{-1m^{-4}}$ | 1.4E+25 | First coefficient of flicker noise for a channel region of 1 um wide |
| NFBW | $V^{-1m^{-2}}$ | 2.00E+08 | Second coefficient of flicker noise for a channel region of 1 um wide |

| Name | Unit | Default | Description |
|---------|---------------------|-----------|--|
| NFCW | V ⁻¹ | 0 | Third coefficient of flicker noise for a channel region of 1 um wide |
| NT | J | 1.645E-20 | Coefficient of thermal noise, at reference temperature |
| PHIB | V | 0.86 | Surface potential at the onset of strong inversion in the channel region, at reference temperature |
| PHIBD | V | 0.78 | Surface potential at the onset of strong inversion in the drift region, at reference temperature |
| RDW | Ohm | 4000 | On-resistance of a drift region of 1 um wide, at reference temperature |
| RTH | K/W | 300 | Thermal resistance |
| SDIBL | V ^(-1/2) | 0.001 | Factor for drain-induced barrier lowering |
| SHMOD | | 0 | SHMOD is used as a switch of self-heating effect, 0 for off and 1 for on |
| SSF | V ^(-1/2) | 1E-12 | Factor for static feedback |
| STA1CH | K ⁻¹ | 0 | Temperature scaling coefficient for A1CH |
| STA1DR | K ⁻¹ | 0 | Temperature scaling coefficient for A1DR |
| STPHIB | V/K | -0.0012 | Temperature scaling coefficient for PHIB |
| STPHIBD | V/K | -0.0012 | Temperature scaling coefficient for PHIBD |
| STVFB | V/K | 0 | Temperature scaling coefficient for VFB |
| STVFBD | V/K | 0 | Temperature scaling coefficient for the flatband voltage of the drift region |
| SWA1CH | | 0 | Width scaling coefficient for A1CH |
| SWA1DR | | 0 | Width scaling coefficient for A1DR |
| SWKO | | 0 | Width scaling coefficient for KO |
| SWKOD | | 0 | Width scaling coefficient for the body factor of the drift region |
| SWTHE1 | | 0 | Width scaling coefficient for THE1 |
| SWTHE2 | | 0 | Width scaling coefficient for THE2 |

Chapter 2: MOSFET Models

LEVEL 74: MOS Model 20 Model

| Name | Unit | Default | Description |
|---------|---------------------|----------|--|
| SWTHE3 | | 0 | Width scaling coefficient for THE3 |
| SWTHE3D | | 0 | Width scaling coefficient for THE3D |
| THE1ACC | V ⁻¹ | 0.02 | Mobility reduction coefficient in the drift region due to the vertical electrical field caused by accumulation |
| THE1R | V ⁻¹ | 0.09 | Mobility reduction coefficient of infinitely wide transistor, due to vertical strong-inversion field in a channel region |
| THE2R | V ^(-1/2) | 0.03 | Mobility reduction coefficient for VSB > 0 of an infinitely wide transistor, due to vertical depletion field in channel region |
| THE3DR | V ⁻¹ | 0 | Mobility reduction coefficient in a channel region of an infinitely wide transistor due to velocity saturation |
| THE3R | V ⁻¹ | 0.4 | Mobility reduction coefficient in a channel region of an infinitely wide transistor due to velocity saturation |
| TOX | m | 3.80E-08 | Thickness of the oxide above the channel region |
| TREF | deg.C | 25 | Reference temperature |
| VFB | V | -1 | Flatband voltage of the channel region, at reference temperature |
| VFBD | V | -0.1 | Flatband voltage of the drift region, at reference temperature |
| VP | V | 0.05 | Characteristic voltage of channel length modulation |
| WDVAR | m | 0 | Width offset of the drift region |
| WVAR | m | 0 | Width offset of the channel region |

MOS Model 20 — Electrical Parameters

| Name | Unit | Default | Description |
|-----------|------|---------|---|
| VERSION | | 2002.2 | VERSION 2002.2 is the default version number to define NXP model level 2002 |
| GEOMOD | | 1 | GEOMOD is used as a switch between geometrical model and electrical model, 0 for geometrical model and 1 for electrical model |
| JUNCAPMOD | | 0 | JUNCAPMOD as a switch of juncap200.2 model effective, 0 for off and 1 for on |

| Name | Unit | Default | Description |
|-----------|------------------|----------|--|
| TYPE | | 1 | TYPE=1 NMOS;TYPE=-1 PMOS |
| A1CH | | 15 | Factor of channel weak avalanche current, at reference temperature |
| A1DR | | 15 | Factor of drift weak avalanche current, at reference temperature |
| A2CH | V | 73 | Exponent of weak avalanche current, related to channel |
| A2DR | V | 73 | Exponent of weak avalanche current, related to drift |
| A3CH | | 0.8 | Factor of the internal drain-source voltage, above which channel weak avalanche occurs |
| A3DR | | 0.8 | Factor of the internal drain-source voltage, above which drift weak avalanche occurs |
| ALP | | 0.002 | Factor for channel length modulation |
| ATH | | 0 | Temperature coefficient of the thermal resistance |
| BET | A/V ² | 7.00E-05 | Gain factor of a channel region, at reference temperature |
| BETACC | A/V ² | 7.00E-05 | Gain factor of drift region of 1 um wide, at reference temperature |
| CGDO | F | 0 | Gate-to-drain overlap capacitance for a drift region |
| CGSO | F | 0 | Gate-to-source overlap capacitance for a drift region |
| COX | F | 15E-15 | Oxide capacitance for an intrinsic channel region |
| COXD | F | 15E-15 | Oxide capacitance for an intrinsic drift region |
| CTH | J/K | 3.00E-09 | Thermal capacitance |
| DTA | K | 0 | Temperature offset to the ambient temperature |
| ETABET | | 1.6 | Temperature scaling exponent for BET |
| ETABETACC | | 1.5 | Temperature scaling exponent for BETACC |
| ETARD | | 1.5 | Temperature scaling exponent for RD |
| ETATHE3 | | 1 | Temperature scaling exponent for THE3 |
| ETATHE3D | | 1 | Temperature scaling exponent for THE3D |

Chapter 2: MOSFET Models

LEVEL 74: MOS Model 20 Model

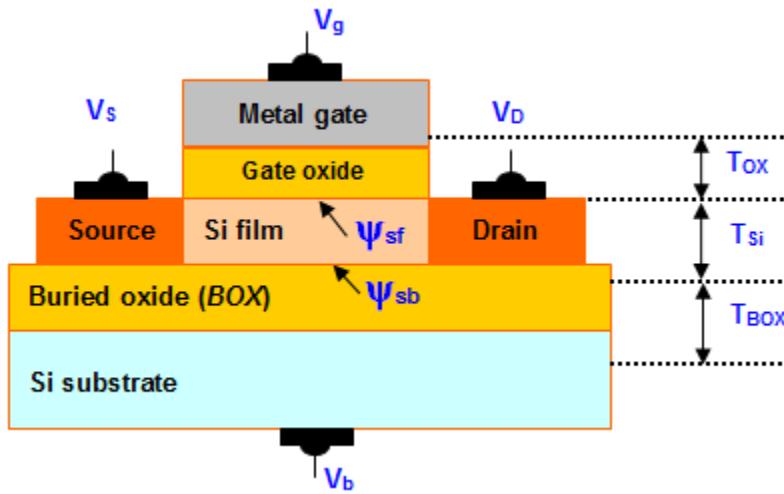
| Name | Unit | Default | Description |
|--------|----------------|-----------|--|
| KO | $V^{(1/2)}$ | 1.6 | Body factor of the channel region |
| KOD | $V^{(1/2)}$ | 1 | Body factor of the drift region |
| LAMD | | 0.2 | Quotient of the depletion layer thickness to the effective thickness of the drift region at $V_{SB} = 0$ V |
| MEXP | | 2 | Smoothing factor for transition from linear to saturation regime |
| MEXPD | | 2 | Smoothing factor for transition from linear to quasi-saturation regime |
| MO | V | 0 | Parameter for the (short-channel) sub-threshold slope |
| MSDIBL | | 3 | Exponent for the drain-induced barrier lowering dependence on the backgate bias |
| NFA | $V^{-1m^{-4}}$ | 7.0E+23 | First coefficient of flicker noise for a channel region |
| NFB | $V^{-1m^{-2}}$ | 1.0E+07 | Second coefficient of flicker noise for a channel region |
| NFC | V^{-1} | 0 | Third coefficient of flicker noise for a channel region |
| NT | J | 1.645E-20 | Coefficient of thermal noise, at reference temperature |
| PHIB | V | 0.86 | Surface potential at the onset of strong inversion in the channel region, at reference temperature |
| PHIBD | V | 0.78 | Surface potential at the onset of strong inversion in the drift region, at reference temperature |
| RD | Ohm | 200 | On-resistance of a drift region, at reference temperature |
| RTH | K/W | 300 | Thermal resistance |
| SDIBL | $V^{(-1/2)}$ | 0.001 | Factor for drain-induced barrier lowering |
| SHMOD | | 0 | SHMOD is used as a switch of self-heating effect, 0 for off and 1 for on |
| SSF | $V^{(-1/2)}$ | 1E-12 | Factor for static feedback |
| STA1CH | K^{-1} | 0 | Temperature scaling coefficient for A1CH |

| Name | Unit | Default | Description |
|---------|---------------------|----------|--|
| STA1DR | K ⁻¹ | 0 | Temperature scaling coefficient for A1DR |
| STPHIB | V/K | -0.0012 | Temperature scaling coefficient for PHIB |
| STPHIBD | V/K | -0.0012 | Temperature scaling coefficient for PHIBD |
| STVFB | V/K | 0 | Temperature scaling coefficient for VFB |
| STVFBD | V/K | 0 | Temperature scaling coefficient for the flatband voltage of the drift region |
| THE1 | V ⁻¹ | 0.09 | Mobility reduction coefficient due to vertical strong-inversion field in a channel region |
| THE1ACC | V ⁻¹ | 0.02 | Mobility reduction coefficient in the drift region due to the vertical electrical field caused by accumulation |
| THE2 | V ^(-1/2) | 0.03 | Mobility reduction coefficient for VSB > 0, due to vertical depletion field in channel region |
| THE3 | V ⁻¹ | 0.4 | Mobility reduction coefficient in a channel region due to velocity saturation |
| THE3D | V ⁻¹ | 0 | Mobility reduction coefficient in a channel region due to velocity saturation |
| TOX | m | 3.80E-08 | Thickness of the oxide above the channel region |
| TREF | deg.C | 25 | Reference temperature |
| VFB | V | -1 | Flatband voltage of the channel region, at reference temperature |
| VFBD | V | -0.1 | Flatband voltage of the drift region, at reference temperature |
| VP | V | 0.05 | Characteristic voltage of channel length modulation |

LEVEL 76: LETI-UTSOI MOSFET Model

The *UTSOI* [11] model developed by CEA-LETI is a surface-potential based model dedicated to Planar Ultra-Thin SOI MOSFET device. Similarly *PSP* [12] is a surface-potential model dedicated to Planar MOSFET on Bulk Silicon.

The UTSOI model has been designed to be user-friendly for PSP users. The device structure is illustrated by the following figure:



The UTSOI model is designed for transistors with a lightly doped silicon film. The silicon film thickness is typically lower than 10nm.

This model is compatible with the use of thin buried oxide (typically 10nm). However, this model is not designed for double gate transistor where the back Si-SiO₂ interface can be in inversion.

This section covers the following topics:

- [LETI-UTSOI MOSFET Model Updates](#)
- [UTSOI MOSFET Model — Global Model Flags and Parameters](#)
- [UTSOI MOSFET Model — Local Level Parameters \(SWSCALE=0\)](#)
- [UTSOI MOSFET Model — Global Level Parameters \(SWSCALE=1\)](#)

LETI-UTSOI MOSFET Model Updates

This section covers the following topics:

- [LETI-UTSOI MOSFET Model 2.0.0 Updates](#)
- [LETI-UTSOI MOSFET Model 1.1.4 Updates](#)
- [LETI-UTSOI MOSFET Model 1.1.3 Updates](#)
- [LETI-UTSOI MOSFET Model 1.1.2 Updates](#)
- [LETI-UTSOI MOSFET Model 1.1.1 Updates](#)

LETI-UTSOI MOSFET Model 2.0.0 Updates

The following summarizes the bug fixes and changes from UTSOI Model 1.1.4 to UTSOI Model 2.0.0 per the CEA-LETI UTSOI release note:

- FUTSOI2 has been developed with the aim of being able to describe device operations with a strongly inverted back interface. Thus, an original analytical procedure has been developed to calculate the exact values of the surface potentials at front and back interfaces in all operating conditions.
- Besides this surface potential calculation, new drain current and intrinsic charge models have also been developed. It should be noticed that this new model core is valid not only for FDSOI technologies, but more generally for all Independent Double Gate device architectures.
- The effect of backplane depletion is introduced in UTSOI2 and computed through a bulk MOSFET like surface potential calculation. This effect can be turned-on or turned-off using the SWSUBDEP flag. If the flag is set to 0, the backplane is assumed metallic, as in UTSOI1.
- UTSOI2 offers the possibility to define two different junctions at source and drain sides, as done in PSP. Junction related parameters are thus duplicated, the drain related parameters having the same name as their source side counterparts plus a final "D". This possible junction asymmetry can be turned-on or turned-off using the SWJUNASYM flag. When it is turned-off, drain related parameters are ignored.
- It should be noticed that the UTSOI1 possibility to switch from external to internal series resistance through the SWRSMOD flag is no longer included in UTSOI2.

Chapter 2: MOSFET Models

LEVEL 76: LETI-UTSOI MOSFET Model

LETI-UTSOI MOSFET Model 1.1.4 Updates

The following summarizes the bug fixes and changes from UTSOI Model 1.1.3 to UTSOI Model 1.1.4 per the CEA-LETI UTSOI release note:

- Drain-bulk and source-bulk perimeter capacitances.
- New parameter for high-K gate oxide (EPSROX).
- New parameters to describe the channel material (EPSRSI, EG, STEG1, STEG2, NI, STNI).
- Geometrical dependence of XCOR and CS parameters.
- New implementation of the HF noise model.
- Several bug fixes:
 - A new expression of `Mutmp` variable has been implemented to avoid unexpected transition in the calculation.
 - A new expression of `BET_ith` variable has been implemented.
 - New variables have been added in the HF noise model implementation.

LETI-UTSOI MOSFET Model 1.1.3 Updates

The following summarizes the bug fixes and changes from UTSOI Model 1.1.2 to UTSOI Model 1.1.3 per the CEA-LETI UTSOI release note:

- A switch to turn-off the induced gate noise model.
- Operation point output variables.
- Several bug fixes:
 - A new expression of `SP_S_delta0` variable has been implemented in the surface potential calculation.
 - Calculation errors of drain and source has been fixed.
 - New min/max for GC3CH, GC3OV, GC3CHO, GC3OVO parameters have been implemented.
 - A new expression for `Vbx`, `Gmob`, `Dd`, `qim`, `qim1`, `temp`, and `t1` variables has been implemented.

LETI-UTSOI MOSFET Model 1.1.2 Updates

The following summarizes the bug fixes and changes from UTSOI Model 1.1.1 to UTSOI Model 1.1.2 per the CEA-LETI UTSOI release note:

- Improvement of accurate during the calculation of the surface potential in the overlaps.
- The overlap capacitance and the fringing capacitance contributions are separated (COV parameter is added).
- Maximum NOV and NOVO values are now 10^{21} cm^{-3} .
- Several bug fixes.

LETI-UTSOI MOSFET Model 1.1.1 Updates

This version is the first reference model version as per the CEA-LETI UTSOI release note.

UTSOI MOSFET Model — Global Model Flags and Parameters

| Name | Unit | Default | Min. | Max. | Description |
|---------|------|---------|--------|------|---|
| TYPE | - | 1 | -1 | 1 | Channel type parameter, +1=NMOS, -1=PMOS. |
| TR | °C | 21.0 | -273.0 | - | Reference temperature. |
| SWSCALE | - | 0 | 0 | 1 | Flag for scaling rules, 0=local parameter set, 1=global parameter set. |
| VERSION | - | 2.0 | - | - | Flag for model version. |
| SWIGATE | - | 0 | 0 | 1 | Flag for gate current, 0=turn off. |
| SWGIDL | - | 0 | 0 | 1 | Flag for GIDL current, 0=turn off. |
| SWSHE | - | 0 | 0 | 1 | Flag for self heating effect, 0=turn off. |
| SWRSMOD | - | 0 | 0 | 1 | Flag for access resistance calculation, 0=includes in mobility model, 1=using internal nodes. |
| SWIGN | - | 1 | 0 | 1 | Flag for induced gate noise, 0=turn off. |

UTSOI MOSFET Model — Local Level Parameters (SWSCALE=0)

This section covers the following topics:

- UTSOI Model — Local Level Instance Parameters
- UTSOI Model — Local Level Process Parameters
- UTSOI Model — Local Level Quantum Effect Parameter
- UTSOI Model — Local Level Interface Coupling Parameter
- UTSOI Model — Local Level Short Channel Effect Parameter
- UTSOI Model — Local Level DIBL Parameters
- UTSOI Model — Local Level Mobility Parameters
- UTSOI Model — Local Level Series Resistance Parameters
- UTSOI Model — Local Level Velocity Saturation Parameters
- UTSOI Model — Local Level Saturation Voltage Parameters
- UTSOI Model — Local Level Channel Length Modulation Parameters
- UTSOI Model — Local Level Gate Current Parameters
- UTSOI Model — Local Level Gate Induced Drain/Source Leakage Current Parameters
- UTSOI Model — Local Level Charge Model Parameters
- UTSOI Model — Local Level Self Heating Parameters
- UTSOI Model — Local Level Noise Model Parameters

UTSOI Model — Local Level Instance Parameters

| Name | Unit | Default | Min. | Max. | Description |
|---------|----------------|-------------------|------|------|-------------------------------|
| ASOURCE | m ² | 10 ⁻¹² | 0 | - | Source region area. |
| ADRAIN | m ² | 10 ⁻¹² | 0 | - | Drain region area. |
| PSOURCE | m | 10 ⁻⁶ | 0 | - | Source region perimeter. |
| PDRAIN | m | 10 ⁻⁶ | 0 | - | Drain region perimeter. |
| MULT | - | 1 | 1 | - | Number of device in parallel. |

UTSOI Model — Local Level Process Parameters

| Name | Unit | Default | Min. | Max. | Description |
|--------|------------------------------|-----------------|------------|-----------|---|
| VFB | V | 0.0 | - | - | Flat-band voltage at TR. |
| STVFB | V/K | 5.10^{-4} | - | - | Temperature dependence of VFB. |
| TOX | m | 2.10^{-9} | 10^{-10} | - | Gate oxide thickness. |
| EPSROX | - | 3.9 | 1.0 | - | Relative permittivity of gate dielectric. |
| TSI | m | 10^{-8} | 10^{-9} | 10^{-7} | Silicon film thickness. |
| EPSRSI | - | 11.8 | 11.8 | 16.5 | Relative permittivity of silicon film. |
| EG | V | 1.179 | 0.6 | 1.2 | Band-gap of silicon film at 300K. |
| STEG1 | V/ $^{\circ}$ C | $9.025.10^{-5}$ | - | - | First temperature coefficient of EG. |
| STEG2 | V/ $^{\circ}$ C ² | $3.05.10^{-7}$ | - | - | Second temperature coefficient of EG. |
| NI | cm ⁻³ | $1.45.10^{10}$ | 10^{10} | 10^{14} | Intrinsic doping of silicon film at 300K. |
| STNI | - | 1.5 | 0.5 | 3.0 | Temperature dependence factor of NI. |
| TBOX | m | 10^{-7} | 10^{-8} | 10^{-6} | Buried oxide thickness. |
| NSI | cm ⁻³ | 0.0 | - | 10^{18} | Lightly silicon film doping, 0=undoped. |
| NSUB | cm ⁻³ | 3.10^{18} | 10^{16} | 10^{21} | Substrate doping, negative value=N-type, positive value=P-type. |
| DVFBB | V | 0.0 | - | - | Offset of back-gate flat-band voltage. |
| CT | - | 0.0 | 0.0 | - | Interface states factor. |
| TOXOV | m | 2.10^{-9} | 10^{-10} | - | Overlap oxide thickness. |
| NOV | cm ⁻³ | 0.0 | 10^{17} | 10^{21} | Effective doping of overlap region, 0=no doping effect. |

Chapter 2: MOSFET Models

LEVEL 76: LETI-UTSOI MOSFET Model

UTSOI Model — Local Level Quantum Effect Parameter

| Name | Unit | Default | Min. | Max. | Description |
|------|------|---------|------|------|----------------------------|
| QMC | - | 1 | 0 | - | Quantum correction factor. |

UTSOI Model — Local Level Interface Coupling Parameter

| Name | Unit | Default | Min. | Max. | Description |
|------|------|---------|------|------|---|
| CIC | - | 1.0 | 0.1 | 10.0 | Substrate bias dependence factor of interface coupling. |

UTSOI Model — Local Level Short Channel Effect Parameter

| Name | Unit | Default | Min. | Max. | Description |
|------|------|---------|------|------|--------------------------------|
| PSCE | - | 0.0 | 0.0 | - | SCE-parameter above threshold. |

UTSOI Model — Local Level DIBL Parameters

| Name | Unit | Default | Min. | Max. | Description |
|------|-----------------|---------|------|------|----------------------------------|
| CF | V ⁻¹ | 0.0 | 0.0 | - | DIBL-parameter. |
| CFB | V ⁻¹ | 0.0 | 0.0 | - | Substrate bias dependence of CF. |
| STCF | - | 0.0 | - | - | Temperature dependence of CF. |

UTSOI Model — Local Level Mobility Parameters

| Name | Unit | Default | Min. | Max. | Description |
|-------|---------------------|--------------------|-------------------|------|--|
| BETN | m ² /V/s | 5.10 ⁻² | 10 ⁻¹⁰ | - | Channel aspect ratio times zero-field mobility |
| STBET | - | 1.0 | - | - | Temperature dependence of BETN |
| MUE | m/V | 0.5 | 0.0 | - | Mobility reduction coefficient at TR |
| STMUE | - | 0.0 | - | - | Temperature dependence of MUE |
| THEMU | - | 1.5 | 0.0 | - | Mobility reduction exponent at TR. |

| Name | Unit | Default | Min. | Max. | Description |
|---------|-----------------|---------|------|------|--|
| STTHEMU | - | 1.5 | - | - | Temperature dependence of THEMU. |
| CS | - | 0.0 | 0.0 | - | Remote Coulomb scattering parameter at TR. |
| CSB | - | 0.0 | - | - | Substrate bias dependence of CS |
| THECS | - | 1.5 | 0.0 | - | Remote Coulomb scattering exponent at TR. |
| STTHECS | - | 1.5 | - | - | Temperature dependence of THECS. |
| STCS | - | 0.0 | - | - | Temperature dependence of CS. |
| XCOR | V ⁻¹ | 0.0 | 0.0 | - | Non-universality factor. |
| STXCOR | - | 0.0 | - | - | Temperature dependence of XCOR. |
| FETA | - | 1.0 | 0.0 | - | Effective field parameter. |

UTSOI Model — Local Level Series Resistance Parameters

| Name | Unit | Default | Min. | Max. | Description |
|--------|----------|---------|------|------|---------------------------------------|
| RS | Ω | 30.0 | 0.0 | - | Source/Drain series resistance at TR. |
| RSG | - | 0.0 | -0.5 | - | Gate bias dependence of RS. |
| THERSG | - | 2.0 | 0.0 | - | Gate bias dependence exponent of RS. |
| STRS | - | 1.0 | - | - | Temperature dependence of RS. |

UTSOI Model — Local Level Velocity Saturation Parameters

| Name | Unit | Default | Min. | Max. | Description |
|----------|-----------------|---------|------|------|---|
| THESAT | V ⁻¹ | 0.0 | 0.0 | - | Velocity saturation parameter at TR. |
| STTHESAT | - | 1.0 | - | - | Temperature dependence of THESAT. |
| THESATB | - | 0.0 | -0.5 | - | Substrate bias dependence of velocity saturation. |
| THESATG | V ⁻¹ | 0.0 | 0.0 | - | Gate bias dependence of velocity saturation. |

Chapter 2: MOSFET Models

LEVEL 76: LETI-UTSOI MOSFET Model

UTSOI Model — Local Level Saturation Voltage Parameters

| Name | Unit | Default | Min. | Max. | Description |
|------|------|---------|------|------|--------------------------------------|
| AX | - | 10.0 | 1.0 | 10.0 | Linear/saturation transition factor. |

UTSOI Model — Local Level Channel Length Modulation Parameters

| Name | Unit | Default | Min. | Max. | Description |
|------|------|---------|------------|------|---|
| ALP | ? | 0 | 0 | - | CLM pre-factor. |
| ALP1 | V | 0 | 0 | - | CLM enhancement factor above threshold. |
| VP | V | 0.05 | 10^{-10} | - | CLM logarithm dependence factor. |

UTSOI Model — Local Level Gate Current Parameters

| Name | Unit | Default | Min. | Max. | Description |
|---------|------|---------|------|------|--|
| GCO | - | 0.0 | -10 | 10.0 | Gate tunneling energy adjustment. |
| IGINV | A | 0.0 | 0.0 | - | Gate to channel current pre-factor in inversion. |
| IGOINV | A | 0.0 | 0.0 | - | Gate to overlap current pre-factor in inversion. |
| IGOVACC | A | 0.0 | 0.0 | - | Gate to overlap current pre-factor in accumulation. |
| GC2CH | - | 0.375 | 0.0 | 10.0 | Gate current slope factor for gate to channel current. |
| GC3CH | - | 0.063 | -2.0 | 2.0 | Gate current curvature factor for gate to channel current. |
| GC2OV | - | 0.375 | 0.0 | 10.0 | Gate current slope factor for overlap currents. |
| GC3OV | - | 0.063 | -2.0 | 2.0 | Gate current curvature factor for overlap currents. |
| STIG | - | 2.0 | - | - | Temperature dependence of all gate currents. |
| CHIB | V | 3.1 | 1.0 | - | Tunneling barrier height. |

UTSOI Model — Local Level Gate Induced Drain/Source Leakage Current Parameters

| Name | Unit | Default | Min. | Max. | Description |
|---------|------------------|---------|------|------|------------------------------------|
| AGIDL | A/V ³ | 0.0 | 0.0 | - | GIDL pre-factor. |
| BGIDL | V | 41.0 | 0.0 | - | GIDL probability factor at TR. |
| STBGIDL | V/K | 0.0 | - | - | Temperature dependence of BGIDL. |
| CGIDL | - | 0.0 | - | - | Substrate bias dependence of GIDL. |

UTSOI Model — Local Level Charge Model Parameters

| Name | Unit | Default | Min. | Max. | Description |
|-------|------------------|--------------------|------|------|--|
| COX | F | 10 ⁻¹⁴ | 0.0 | - | Oxide capacitance for intrinsic channel. |
| CBOX | F/m ² | 5.10 ⁻⁴ | 0.0 | - | Unit area buried oxide capacitance of drain/source region. |
| CGBOV | F | 0.0 | 0.0 | - | Oxide capacitance for gate-substrate overlap. |
| COV | F | 0.0 | 0.0 | - | Overlap capacitance. |
| CFR | F | 0.0 | 0.0 | - | Outer fringe capacitance. |
| CSDO | F | 0.0 | 0.0 | - | Outer drain-source capacitance. |
| CSDBP | F/m | 0.0 | 0.0 | - | Drain/source to substrate perimeter capacitance. |

UTSOI Model — Local Level Self Heating Parameters

| Name | Unit | Default | Min. | Max. | Description |
|-------|---------|---------------------|------|------|-------------------------------|
| RTH | °C/W | 1500.0 | 0.0 | - | Substrate thermal resistance |
| STRTH | - | 0.0 | 0.0 | - | Temperature dependence of RTH |
| CTH | W.s /°C | 5.10 ⁻¹⁰ | 0.0 | - | Substrate thermal capacitance |

Chapter 2: MOSFET Models

LEVEL 76: LETI-UTSOI MOSFET Model

UTSOI Model — Local Level Noise Model Parameters

| Name | Unit | Default | Min. | Max. | Description |
|------|---------------------------------|--------------------|------|------|---|
| FNT | - | 1.0 | 0.0 | - | Thermal noise coefficient. |
| NFA | V ⁻¹ /m ⁴ | 8.10 ²² | 0.0 | - | First coefficient of flicker noise. |
| NFB | V ⁻¹ /m ² | 3.10 ⁷ | 0.0 | - | Second coefficient of flicker noise. |
| NFC | V ⁻¹ | 0.0 | 0.0 | - | Third coefficient of flicker noise. |
| EF | - | 1.0 | 0.1 | - | Frequency coefficient of flicker noise. |

UTSOI MOSFET Model — Global Level Parameters (SWSCALE=1)

This section covers the following topics:

- [UTSOI Model — Global Level Instance Parameters](#)
- [UTSOI Model — Global Level Geometry Scaling Parameters](#)
- [UTSOI Model — Global Level Mechanical Stress Model Parameters](#)
- [UTSOI Model — Global Level Process Parameters](#)
- [UTSOI Model — Global Level Quantum Effect Parameter](#)
- [UTSOI Model — Global Level Interface Coupling Parameter](#)
- [UTSOI Model — Global Level Short Channel Effect Parameters](#)
- [UTSOI Model — Global Level DIBL Parameters](#)
- [UTSOI Model — Global Level Mobility Parameters](#)
- [UTSOI Model — Global Level Series Resistance Parameters](#)
- [UTSOI Model — Global Level Velocity Saturation Parameters](#)
- [UTSOI Model — Global Level Saturation Voltage Parameter](#)
- [UTSOI Model — Global Level Channel Length Modulation Parameters](#)
- [UTSOI Model — Global Level Gate Current Parameters](#)
- [UTSOI Model — Global Level Gate Induced Drain/Source Leakage Current Parameters](#)

- [UTSOI Model — Global Level Charge Model Parameters](#)
- [UTSOI Model — Global Level Self Heating Parameters](#)
- [UTSOI Model — Global Level Noise Model Parameters](#)

UTSOI Model — Global Level Instance Parameters

| Name | Unit | Default | Min. | Max. | Description |
|---------|-------|------------|-----------|------|---|
| L | m | 10^{-6} | 10^{-9} | - | Drawn channel length. |
| W | m | 10^{-6} | 10^{-9} | - | Drawn channel width. |
| SA | m | 0.0 | - | - | Distance between OD-edge and gate at source side. |
| SB | m | 0.0 | - | - | Distance between OD-edge and gate at drain side. |
| SD | m | 0.0 | - | - | Distance between neighboring fingers. |
| ASOURCE | m^2 | 10^{-12} | 0.0 | - | Source region area. |
| ADRAIN | m^2 | 10^{-12} | 0.0 | - | Drain region area. |
| PSOURCE | m | 10^{-6} | 0.0 | - | Source region perimeter. |
| PDRAIN | m | 10^{-6} | 0.0 | - | Drain region perimeter. |
| NF | - | 1.0 | 1.0 | - | Number of fingers. |
| MULT | - | 1.0 | 1.0 | - | Number of device in parallel. |

UTSOI Model — Global Level Geometry Scaling Parameters

| Name | Unit | Default | Min. | Max. | Description |
|-------|------|---------|------|------|--|
| LVAR0 | m | 0.0 | - | - | Geometry-independent difference between physical and drawn gate lengths. |
| LVARL | - | 0.0 | - | - | Length dependence of LPS. |
| LVARW | - | 0.0 | - | - | Width dependence of LPS. |
| LAP | m | 0.0 | - | - | Effective channel length reduction per side. |

Chapter 2: MOSFET Models

LEVEL 76: LETI-UTSOI MOSFET Model

| Name | Unit | Default | Min. | Max. | Description |
|-------|------|---------|------|------|---|
| WVARO | m | 0.0 | - | - | Geometry-independent difference between physical and drawn field-oxide opening. |
| WVARL | - | 0.0 | - | - | Length dependence of WOD. |
| WVARW | - | 0.0 | - | - | Width dependence of WOD. |
| WOT | m | 0.0 | - | - | Effective reduction of channel width per side. |
| DLQ | m | 0.0 | - | - | Effective channel length offset for CV. |
| DWQ | m | 0.0 | - | - | Effective channel width offset for CV. |

UTSOI Model — Global Level Mechanical Stress Model Parameters

| Name | Unit | Default | Min. | Max. | Description |
|---------|------|-----------|-----------|------|---|
| SAREF | m | 10^{-6} | 10^{-9} | - | Reference distance between OD edge to poly from one side. |
| SBREF | m | 10^{-6} | 10^{-9} | - | Reference distance between OD edge to poly from other side. |
| WL0D | m | 0.0 | - | - | Width parameter. |
| KU0 | m | 0.0 | - | - | Mobility degradation/enhancement coefficient. |
| KVSAT | m | 0.0 | -1.0 | 1.0 | Saturation velocity degradation/enhancement parameter. |
| TKU0 | - | 0.0 | - | - | Temperature coefficient of KU0. |
| LKU0 | - | 0.0 | - | - | Length dependence of KU0. |
| WKU0 | - | 0.0 | - | - | Width dependence of KU0. |
| PKU0 | - | 0.0 | - | - | Cross-term dependence of KU0. |
| LLODKU0 | - | 0.0 | 0.0 | - | Length parameter for mobility stress effect. |
| WL0DKU0 | - | 0.0 | 0.0 | - | Width parameter for mobility stress effect. |
| KVTH0 | V.m | 0.0 | - | - | Threshold shift parameter. |
| LKVTH0 | - | 0.0 | - | - | Length dependence of KVTH0. |

| Name | Unit | Default | Min. | Max. | Description |
|---------|------|---------|------|------|--|
| WKVTHO | - | 0.0 | - | - | Width dependence of KVTHO. |
| PKVTHO | - | 0.0 | - | - | Cross-term dependence of KVTHO. |
| LLODVTH | - | 0.0 | 0.0 | - | Length parameter for threshold voltage stress effect. |
| WLODVTH | - | 0.0 | 0.0 | - | Width parameter for threshold voltage stress effect. |
| STETAO | m | 0.0 | - | - | ETAO shift factor related to threshold voltage change. |
| LODETAO | - | 1.0 | | - | ETAO shift modification factor. |

UTSOI Model — Global Level Process Parameters

| Name | Unit | Default | Min. | Max. | Description |
|----------|------|-------------|------------|-----------|---|
| VFB0 | V | 0.0 | - | - | Geometry-independent flat-band voltage at TR. |
| VFBL | - | 0.0 | - | - | Length dependence of VFB. |
| VFBLEXP | - | 1.0 | - | - | Exponent describing length dependence of VFB. |
| VFBW | - | 0.0 | - | - | Width dependence of VFB. |
| VFB LW | - | 0.0 | - | - | Area dependence of VFB. |
| STVFBO | V/K | 5.10^{-4} | - | - | Geometry-independent temperature dependence of VFB. |
| STVFBL | - | 0.0 | - | - | Length dependence of STVFB. |
| STVFBW | - | 0.0 | - | - | Width dependence of STVFB. |
| STVFB LW | - | 0.0 | - | - | Area dependence of STVFB. |
| TOXO | m | 2.10^{-9} | 10^{-10} | - | Gate oxide thickness.. |
| EPSROXO | - | 3.9 | 1.0 | - | Relative permittivity of gate dielectric. |
| TSIO | m | 10^{-8} | 10^{-9} | 10^{-7} | Silicon film thickness. |
| EPSRSIO | - | 11.8 | 11.8 | 16.5 | Relative permittivity of silicon film. |

Chapter 2: MOSFET Models

LEVEL 76: LETI-UTSOI MOSFET Model

| Name | Unit | Default | Min. | Max. | Description |
|--------|------------------------------|-----------------------|------------------|------------------|---|
| EGO | V | 1.179 | 0.6 | 1.2 | Band-gap of silicon film at 300K. |
| STEG1O | V/ $^{\circ}$ C | $9,025 \cdot 10^{-5}$ | - | - | First temperature coefficient of EG. |
| STEG2O | V/ $^{\circ}$ C ² | $3,05 \cdot 10^{-7}$ | - | - | Second temperature coefficient of EG. |
| NIO | cm ⁻³ | $1,45 \cdot 10^{10}$ | 10^{10} | 10^{14} | Intrinsic doping of silicon film at 300K. |
| STNIO | - | 1.5 | 0.5 | 3.0 | Temperature dependence factor of NI. |
| TBOXO | m | 10 ⁻⁷ | 10 ⁻⁸ | 10 ⁻⁶ | Buried oxide thickness. |
| NSIO | cm ⁻³ | 0.0 | - | - | Lightly silicon film doping, 0=intrinsic doping. |
| NSUBO | cm ⁻³ | $-3 \cdot 10^{18}$ | 10^{16} | 10^{21} | Substrate doping, negative value=N-type, positive value=P-type. |
| DVFBB0 | V | 0.0 | - | - | Offset of back-gate flat-band voltage. |
| CTO | - | 0.0 | 0.0 | - | Interface states factor. |
| TOXOVO | m | $2 \cdot 10^{-9}$ | 10^{-10} | - | Overlap oxide thickness. |
| LOV | m | 0.0 | 0.0 | - | Length of gate/drain and date/source overlaps. |
| NOVO | cm ⁻³ | 0.0 | 10^{17} | 10^{21} | Effective doping of overlap region, 0=No doping effect. |

UTSOI Model — Global Level Quantum Effect Parameter

| Name | Unit | Default | Min. | Max. | Description |
|------|------|---------|------|------|----------------------------|
| QMC | - | 1 | 0 | - | Quantum correction factor. |

UTSOI Model — Global Level Interface Coupling Parameter

| Name | Unit | Default | Min. | Max. | Description |
|------|------|---------|------|------|--|
| CICO | - | 1.0 | 0.1 | 10.0 | Geometry-independent part of substrate bias dependence factor of interface coupling. |
| CICL | - | 0.0 | - | - | Length dependence of CIC. |

| Name | Unit | Default | Min. | Max. | Description |
|---------|------|---------|------|------|---|
| CICLEXP | - | 1.0 | - | - | Exponent describing length dependence of CIC. |
| CICW | - | 0.0 | - | - | Width dependence of CIC. |
| CICLW | - | 0.0 | - | - | Area dependence of CIC. |

UTSOI Model — Global Level Short Channel Effect Parameters

| Name | Unit | Default | Min. | Max. | Description |
|----------|------|---------|------|------|--|
| PSCEL | - | 0.0 | 0.0 | - | Length dependence of short channel effect above threshold. |
| PSCELEXP | - | 1.0 | - | - | Exponent describing length dependence of PSCE. |
| PSCEW | - | 0.0 | 0.0 | - | Width dependence of PSCE. |

UTSOI Model — Global Level DIBL Parameters

| Name | Unit | Default | Min. | Max. | Description |
|--------|-----------------|---------|------|------|---------------------------------------|
| CFL | V ⁻¹ | 0.0 | 0.0 | - | Length dependence of DIBL parameter. |
| CFLEXP | - | 2.0 | - | - | Exponent for length dependence of CF. |
| CFW | - | 0.0 | - | - | Width dependence of CF. |
| CFBO | - | 0.0 | 0.0 | - | Substrate bias dependence of CF. |
| STCFO | - | 0.0 | - | - | Temperature dependence of CF. |

UTSOI Model — Global Level Mobility Parameters

| Name | Unit | Default | Min. | Max. | Description |
|----------|---------------------|--------------------|------|------|--|
| UO | m ² /V/s | 5.10 ⁻² | - | - | Zero-field mobility at TR. |
| BETNL | - | 0.0 | - | - | Second order length dependence of BETN. |
| BETNLEXP | - | 1.0 | - | - | Exponent for second order length dependence of BETN. |

Chapter 2: MOSFET Models

LEVEL 76: LETI-UTSOI MOSFET Model

| Name | Unit | Default | Min. | Max. | Description |
|-----------|-----------------|---------|------|------|---|
| BETNW | - | 0.0 | - | - | Second order width dependence of BETN. |
| STBETO | - | 1.0 | - | - | Geometry-independent part of temperature dependence of BETN. |
| STBETL | - | 0.0 | - | - | Length dependence of STBET. |
| STBETW | - | 0.0 | - | - | Width dependence of STBET. |
| STBETLW | - | 0.0 | - | - | Area dependence of STBET. |
| MUEO | m/V | 0.5 | 0.0 | - | Mobility reduction coefficient at TR. |
| STMUEO | - | 0.0 | - | - | Temperature dependence of MUE. |
| THEMUEO | - | 1.5 | 0.0 | - | Mobility reduction exponent at TR. |
| STTHEMUEO | - | 1.5 | - | - | Temperature dependence of THEMU. |
| CSO | - | 0.0 | - | - | Geometry-independent part of remote coulomb scattering parameter at TR. |
| CSL | - | 0.0 | - | - | Length dependence of CS. |
| CSLEXP | - | 1.0 | - | - | Exponent describing length dependence of CS. |
| CSW | - | 0.0 | - | - | Width dependence of CS. |
| CSLW | - | 0.0 | - | - | Area dependence of CS. |
| CSBO | - | 0.0 | 0.0 | - | Back bias dependence of CS. |
| THECSO | - | 1.5 | 0.0 | - | Remote coulomb scattering exponent at TR3. |
| STCSO | - | 0.0 | - | - | Temperature dependence of CS. |
| STTHECSO | - | 1.5 | - | - | Temperature dependence of THECS. |
| XCORO | V ⁻¹ | 0.0 | - | - | Geometry-independent part non-universality factor. |
| XCORL | - | 0.0 | - | - | Length dependence of XCOR. |
| XCORLEXP | - | 1.0 | - | - | Exponent describing length dependence of XCOR. |

| Name | Unit | Default | Min. | Max. | Description |
|---------|------|---------|------|------|---------------------------------|
| XCORW | - | 0.0 | - | - | Width dependence of XCOR. |
| XCORLW | - | 0.0 | - | - | Area dependence of XCOR. |
| STXCORO | - | 0.0 | - | - | Temperature dependence of XCOR. |
| FETAO | - | 1.0 | 0.0 | - | Effective field parameter. |

UTSOI Model — Global Level Series Resistance Parameters

| Name | Unit | Default | Min. | Max. | Description |
|---------|----------|---------|------|------|---|
| RSW1 | Ω | 30.0 | - | - | Source/Drain series resistance for channel width WEN at TR. |
| RSW2 | - | 0.0 | - | - | Higher-order width scaling of source/drain series resistance. |
| RSGO | - | 0.0 | -0.5 | - | Gate-bias dependence of RS. |
| THERSGO | - | 2.0 | - | - | Gate-bias dependence exponent of RS. |
| STRSO | - | 1.0 | - | - | Temperature dependence of RS. |

UTSOI Model — Global Level Velocity Saturation Parameters

| Name | Unit | Default | Min. | Max. | Description |
|------------|----------|---------|------|------|---|
| THESATO | V^{-1} | 0.0 | 0.0 | - | Geometry-independent Velocity saturation parameter at TR. |
| THESATL | - | 0.0 | - | - | Length dependence of THESAT. |
| THESATLEXP | - | 1.0 | - | - | Exponent for length dependence of THESAT. |
| THESATW | - | 0.0 | - | - | Width dependence of THESAT. |
| THESATLW | - | 0.0 | - | - | Area dependence of THESAT. |
| THESATGO | V^{-1} | 0.0 | 0.0 | - | Geometry-independent gate bias dependence of velocity saturation parameter at TR. |

Chapter 2: MOSFET Models

LEVEL 76: LETI-UTSOI MOSFET Model

| Name | Unit | Default | Min. | Max. | Description |
|------------|-----------------|---------|------|------|---|
| STTHESATO | - | 1.0 | - | - | Geometry-independent of temperature dependence of THESAT. |
| STTHESATL | - | 0.0 | - | - | Length dependence of STTHESAT. |
| STTHESATW | - | 0.0 | - | - | Width dependence of STTHESAT. |
| STTHESATLW | - | 0.0 | - | - | Area dependence of STTHESAT. |
| THESATBO | V ⁻¹ | 0.0 | -0.5 | 1.0 | Substrate bias dependence of velocity saturation. |

UTSOI Model — Global Level Saturation Voltage Parameter

| Name | Unit | Default | Min. | Max. | Description |
|--------|------|---------|------|------|--|
| AXO | - | 10.0 | - | - | Geometry-independent of linear/saturation transition factor. |
| AXL | - | 0.0 | 0.0 | - | Length dependence of AX. |
| AXLEXP | - | 1.0 | 0.0 | - | Exponent for length dependence of AX. |

UTSOI Model — Global Level Channel Length Modulation Parameters

| Name | Unit | Default | Min. | Max. | Description |
|----------|------|---------|------|------|--|
| ALPL1 | - | 0.0 | 0.0 | - | Length dependence of CLM pre-factor ALP. |
| ALPLEXP | - | 1.0 | - | - | Exponent for length dependence of ALP. |
| ALPL2 | - | 0.0 | - | - | Second order length dependence of ALP. |
| ALPW | - | 0.0 | - | - | Width dependence of ALP. |
| ALP1L1 | V | 0.0 | 0.0 | - | Length dependence of CLM enhancement factor. |
| ALP1LEXP | - | 1.0 | - | - | Exponent for length dependence of ALP1. |
| ALP1L2 | - | 0.0 | - | - | Second order length dependence of ALP1. |

| Name | Unit | Default | Min. | Max. | Description |
|-------|------|---------|------------|------|----------------------------------|
| ALP1W | - | 0.0 | - | - | Width dependence of ALP1. |
| VPO | V | 0.05 | 10^{-10} | - | CLM logarithm dependence factor. |

UTSOI Model — Global Level Gate Current Parameters

| Name | Unit | Default | Min. | Max. | Description |
|----------|------|---------|-------|------|---|
| GCOO | - | 0.0 | -10.0 | 10.0 | Gate tunneling energy adjustment |
| IGINVWL | A | 0.0 | 0.0 | - | Gate channel current pre-factor for a channel area of WEN.LEN |
| IGOINVW | A | 0.0 | 0.0 | - | Gate to overlap current pre-factor in inversion for an overlap of WEN.LOV |
| IGOVACCW | A | 0.0 | 0.0 | - | Gate to overlap current pre-factor in accumulation overlap of WEN.LOV |
| GC2CHO | - | 0.375 | 0.0 | 10.0 | Gate current slope factor for gate to channel current |
| GC3CHO | - | 0.063 | -2.0 | 2.0 | Gate current curvature factor for gate to channel current |
| GC2OVO | - | 0.375 | 0.0 | 10.0 | Gate current slope factor for overlap currents |
| GC3OVO | - | 0.063 | -2.0 | 2.0 | Gate current curvature factor for overlap currents |
| STIGO | - | 2.0 | - | - | Temperature dependence of all gate currents |
| CHIBO | V | 3.1 | 1.0 | - | Tunneling barrier height |

UTSOI Model — Global Level Gate Induced Drain/Source Leakage Current Parameters

| Name | Unit | Default | Min. | Max. | Description |
|--------|------------------|---------|------|------|--------------------------------------|
| AGIDLW | A/V ³ | 0.0 | 0.0 | - | Width dependence of GIDL pre-factor. |
| BGIDLO | V | 41.0 | 0.0 | - | GIDL probability factor at TR. |

Chapter 2: MOSFET Models

LEVEL 76: LETI-UTSOI MOSFET Model

| Name | Unit | Default | Min. | Max. | Description |
|----------|------|---------|------|------|------------------------------------|
| STBGIDLO | V/K | 0.0 | - | - | Temperature dependence of BGIDL. |
| CGIDLO | - | 0.0 | - | - | Substrate bias dependence of GIDL. |

UTSOI Model — Global Level Charge Model Parameters

| Name | Unit | Default | Min. | Max. | Description |
|--------|------|---------|------|------|--|
| CGBOVL | F | 0.0 | 0.0 | - | Oxide capacitance for gate-substrate overlap. |
| CFRW | F | 0.0 | 0.0 | - | Outer fringe capacitance. |
| CSDBPO | F/m | 0.0 | 0.0 | - | Drain/source to substrate perimeter capacitance. |

UTSOI Model — Global Level Self Heating Parameters

| Name | Unit | Default | Min. | Max. | Description |
|--------|--------|--------------|------|------|---|
| RTHO | °C/W | 1500.0 | 0.0 | - | Geometry-independent part of substrate thermal resistance. |
| RTHL | - | 0.0 | - | - | Length dependence of RTH. |
| RTHW | - | 0.0 | - | - | Width dependence of RTH. |
| RTHLW | - | 0.0 | - | - | Area dependence of RTH. |
| CTHO | W.s/°C | 5.10^{-10} | 0.0 | - | Geometry-independent part of substrate thermal capacitance. |
| STRTHO | - | 0.0 | - | - | Temperature dependence of substrate thermal resistance. |

UTSOI Model — Global Level Noise Model Parameters

| Name | Unit | Default | Min. | Max. | Description |
|--------|---------------------------------|-------------|------|------|--------------------------------------|
| FNTO | - | 1.0 | 0.0 | - | Thermal noise coefficient. |
| NFALW | V ⁻¹ /m ⁴ | 8.10^{22} | 0.0 | - | First coefficient of flicker noise. |
| NFB LW | V ⁻¹ /m ² | 3.10^7 | 0.0 | - | Second coefficient of flicker noise. |

Chapter 2: MOSFET Models
LEVEL 76: LETI-UTSOI MOSFET Model

| Name | Unit | Default | Min. | Max. | Description |
|-------|-----------------|---------|------|------|---|
| NFCLW | V ⁻¹ | 0.0 | 0.0 | - | Third coefficient of flicker noise. |
| EFO | - | 1.0 | 0.1 | - | Frequency coefficient of flicker noise. |

LEVEL 77: BSIM6 MOSFET Model

The BSIM6 model is a compact model to describe the behavior of bulk planar MOSFET devices.

This model captures all important transistor behaviors. BSIM6, as a charge based physical compact model, is believed to be more accurate for current and charge modeling than the V_{th}-based compact models when devices operation is from the sub-V_{th} to strong inversion region. And so, it is more suitable for low-power, low V_{dd} or RF and analog applications.

BSIM6 is a result of a collaboration and co-development between UC Berkeley and a team at EPFL (École Polytechnique Fédérale de Lausanne) that developed the EKV model in the past. As a result, BSIM6 incorporates a few features from the EKV model, most notably:

- The normalized pinch-off potential.
- The saturation voltage.

Included in the model are other important effects, such as: mobility degradation, velocity saturation, velocity overshoot, series resistance, channel length modulation, quantum mechanical effects, poly depletion, gate tunneling current, gate-induced-drain-leakage, and parasitic capacitance models.

This section covers the following topics:

- [BSIM6 MOSFET Model — General Syntax](#)
- [BSIM6 MOSFET Model Parameters](#)

BSIM6 MOSFET Model — General Syntax

Syntax:

```
Mxxx nd ng ns nb mname [L=val] [W=val] [M=val]
+ [AD=val] [AS=val] [PD=val] [PS=val]
+ [RGATEMOD=val] [RBODYMOD=val]
+ [GEOMOD=val] [RGEOMOD=val]
+ [NRS=val] [NRD=val] [RBPB=val] [RBPD=val]
+ [RBPS=val] [RBDB=val] [RBSB=val] [NF=val]
+ [MINZ=val] [VFBSDOFF=val] [XGW=val] [NGCON=val]
+ [SA=val] [SB=val] [SC=val] [SD=val]
+ [SCA=val] [SCB=val] [SCC=val]
+ [OFF] [IC=Vds, Vgs, Vbs]
```

BSIM6 MOSFET Model Parameters

The following sections define these parameters:

- [BSIM6 Model — Instance Parameters](#)
- [BSIM6 Model — Control and Process Parameters](#)
- [BSIM6 Model — Basic Parameters](#)
- [BSIM6 Model — High-Speed/RF Parameters](#)
- [BSIM6 Model — Flicker and Thermal Noise Parameters](#)
- [BSIM6 Model — Layout-Dependent Parasitic Parameters](#)
- [BSIM6 Model — Asymmetric Source/Drain Junction Diode Parameters](#)
- [BSIM6 Model — Temperature-Dependent Parameters](#)
- [BSIM6 Model — Stress Effect Parameters](#)
- [BSIM6 Model — Well-Proximity Effect Parameters](#)

Note: Binnable parameters are marked as ^(b).

BSIM6 Model — Instance Parameters

| Parameter | Unit | Default | Min | Max | Description |
|-----------|----------------|---------|-----|-----|--|
| AD | m ² | 0 | 0 | - | Drain to Substrate Junction Area |
| AS | m ² | 0 | 0 | - | Source to Substrate Junction Area |
| GEOMOD | - | 0 | 0 | 10 | Same as BSIM4 |
| L | m | 10u | 1n | - | Designed Gate Length |
| MINZ | - | 0 | 0 | 1 | Minimize either number of drain or source ends |
| NF | - | 1 | 1 | - | Number of fingers |
| NGCON | - | 1 | 1 | 2 | Number of gate contacts |
| NRD | - | 0 | 0 | - | Number of drain diffusion squares |
| NRS | - | 0 | 0 | - | Number of source diffusion squares |
| PD | M | 0 | 0 | - | Drain to Substrate Junction Perimeter |

Chapter 2: MOSFET Models

LEVEL 77: BSIM6 MOSFET Model

| Parameter | Unit | Default | Min | Max | Description |
|-----------|------|---------|-----|-----|---|
| PS | M | 0 | 0 | - | Source to Substrate Junction Perimeter |
| RBDB | Ohm | 50 | 1mV | - | Resistance between dbNode and bNode |
| RBODYMOD | - | 0 | 0 | 2 | Substrate resistance network model selector |
| RBPB | Ohm | 50 | 1mV | - | Resistance between bNodePrime and bNode |
| RBPD | Ohm | 50 | 1mV | - | Resistance between bNodePrime and dbNode |
| RBPS | Ohm | 50 | 1mV | - | Resistance between bNodePrime and sbNode |
| RBSB | Ohm | 50 | 1mV | - | Resistance between sbNode and bNode |
| RGATEMOD | - | 0 | 0 | 2 | Gate resistance model selector |
| RGEOMOD | - | 0 | 0 | 8 | Bias independent parasitic resistance model selector (same as BSIM4) |
| SA | - | 0 | 0 | - | Distance between OD edge from Poly from one side |
| SB | - | 0 | 0 | - | Distance between OD edge from Poly from other side |
| SC | - | 0 | 0 | - | Distance to a single well edge |
| SCA | - | 0 | 0 | - | Integral of the first distribution function for scattered well dopant |
| SCB | - | 0 | 0 | - | Integral of the second distribution function for scattered well dopant |
| SCC | - | 0 | 0 | - | Integral of third distribution function for scattered well dopant |
| SD | - | 0 | 0 | - | Distance between neighboring fingers |
| VFBSDOFF | - | 0 | - | - | Source-Drain flat band offset |
| W | m | 10u | - | - | Designed Gate Width (per finger) |
| XGW | m | 0 | 0 | - | Distance from gate contact center to dev edge |

BSIM6 Model — Control and Process Parameters

| Parameter | Unit | Default | Min | Max | Description |
|----------------------|-----------------|---------|------|------|--|
| COVMOD | - | 0 | 0 | 1 | Bias-independent overlap capacitance:0, Bias-dependent overlap capacitance:1 |
| DLC ^(b) | m | 0 | - | - | Length reduction parameter for CV (dopant diffusion effect) |
| DMCG | - | 0 | 0 | - | Distance of mid-contact to gate edge |
| DMCGT | - | 0 | 0 | - | Distance of mid-contact to gate edge in test |
| DMCI | - | DCMG | 0 | - | Distance of mid-contact to isolation |
| DMDG | - | 0 | 0 | - | Distance of mid-diffusion to gate edge |
| DWC ^(b) | m | 0 | - | - | Width reduction parameter for CV (dopant diffusion effect) |
| EPSROX | - | 3.9 | 1 | - | Relative dielectric constant of the gate insulator |
| EPSRSUB | - | 11.9 | 1 | - | Relative dielectric constant of the channel material |
| GEOMOD | - | 0 | 0 | 10 | Model selector (same as BSIM4) |
| GIDLMOD | - | 0 | 0 | 1 | Turn-off GIDL model:0, Turn-on GIDL model:1 |
| LINT ^(b) | m | 0 | 0 | - | Length reduction parameter (dopant diffusion effect) |
| NDEP ^(b) | m ⁻³ | 1e24 | - | - | channel (body) doping concentration. Global Scaling Parameters - NDEPL1, NDEPLEXP1, NDEPL2, NDEPLEXP2, NDEPW, NDEPWEXP, NDEPWL, NDEPWLEXP |
| NGATE ^(b) | m ⁻³ | 5e25 | - | - | Parameter for Poly Gate doping. Set NGAT E = 0 for metal gates |
| NI0SUB | m ⁻³ | 1.1e16 | - | - | Intrinsic carrier concentration of channel at 300.15K |
| NSD ^(b) | m ⁻³ | 1e26 | 2e25 | 1e27 | S/D doping concentration |
| PERMOD | - | 1 | 0 | 1 | Whether PS/PD (when given) includes the gate-edge perimeter: <ul style="list-style-type: none"> ■ 1: (including the gate-edge perimeter) ■ 0: (not including the gate-edge perimeter) |
| RBODYMOD | - | 0 | 0 | 2 | Substrate resistance network model selector |

Chapter 2: MOSFET Models

LEVEL 77: BSIM6 MOSFET Model

| Parameter | Unit | Default | Min | Max | Description |
|---------------------|------|---------|-----|-----|--|
| RDSMOD | - | 0 | 0 | 1 | Internal RDS:0, External RDS:1 |
| RGATEMOD | - | 0 | 0 | 2 | Gate resistance model selector |
| RGEOMOD | - | 0 | 0 | 8 | Bias independent parasitic resistance model selector (same as BSIM4) |
| TOX | m | 3.0n | | | SiO_2 equivalent gate dielectric thickness |
| TYPE | - | 1 | -1 | 1 | NMOS=1, PMOS=-1 |
| VFB ^(b) | V | -0.5 | - | - | Flat band voltage |
| WINT ^(b) | m | 0 | - | - | Width reduction parameter (dopant diffusion effect) |
| XJ ^(b) | m | 1.5e-7 | - | - | S/D junction depth |
| XL | m | 0 | - | - | L offset for channel length due to mask/etch effect |
| XW | m | 0 | - | - | W offset for channel length due to mask/etch effect |

BSIM6 Model — Basic Parameters

| Name | Unit | Default | Min | Max | Description |
|----------------------|---------------------------------|----------------------------------|-----|-----|--|
| ADOS | - | 0.0 | 0.0 | - | Quantum mechanical effect pre-factor cum switch in inversion |
| AGIDL ^(b) | - | 0.0 | - | - | Pre-exponential coefficient for GIDL. Global Scaling Parameters -AGIDLL, AGIDLW |
| AGISL ^(b) | - | 0.0 | - | - | Pre-exponential coefficient for GISL (AGISL< 0 means GISL parameters will same as GIDL parameters). Global Scaling Parameters -AGISLL, AG-ISLW |
| AIGC ^(b) | $(\text{F s}^2/\text{g})^{0.5}$ | 1.36e-2 (NMOS) and 9.8e-3 (PMOS) | - | - | Parameter for I_{gcs} and I_{gcd} . Global Scaling Parameters -AIGCL, AIGCW |
| AIGD ^(b) | $(\text{F s}^2/\text{g})^{0.5}$ | 1.36e-2 (NMOS) and 9.8e-3 (PMOS) | - | - | Parameter for I_{gd} . Global Scaling Parameters -AIGDL, AIGDW |

| Name | Unit | Default | Min | Max | Description |
|-------------------------|--------------------------------------|-----------------------------------|-----|-----|--|
| AIGS ^(b) | (F s ² /g) ^{0.5} | 1.36e-2 (NMOS) and 9.8e-3 (PMOS) | - | - | Parameter for I _{gs} . Global Scaling Parameters -AIGSL, AIGSW |
| ALPHA0 ^(b) | - | 0.0 | - | - | First parameter of impact ionization current. Global Scaling Parameters -ALPHA0L, ALPHA0LEXP |
| BDOS | - | 1.0 | 0.0 | - | Charge centroid parameter -slope of CV curve under QME in inversion |
| BETA0 ^(b) | - | 0.0 | - | - | First Vds dependent parameter of impact ionization current |
| BGIDL ^(b) | - | 2.3e-9 | - | - | Exponential coefficient for GIDL |
| BGISL ^(b) | - | 2.3e-9 | - | - | Exponential coefficient for GISL |
| BIGC ^(b) | (F s ² /g) ^{0.5} | 1.71e-3 (NMOS) and 7.59e-4 (PMOS) | - | - | Parameter for I _{gcs} and I _{gcd} |
| BIGD ^(b) | (F s ² /g) ^{0.5} | 1.71e-3 (NMOS) and 7.59e-4 (PMOS) | - | - | Parameter for I _{gd} |
| BIGS ^(b) | (F s ² /g) ^{0.5} | 1.71e-3 (NMOS) and 7.59e-4 (PMOS) | - | - | Parameter for I _{gs} |
| CDSCB ^(b) | F/m ² | 7e-03 | 0.0 | - | Body-bias sensitivity of Subthreshold Swing. Global Scaling Parameters -CDSCBL, CDSCBLEXP |
| CDSCD ^(b) | F/m ² | 7e-03 | 0.0 | - | Drain-bias sensitivity of Subthreshold Swing. Global Scaling Parameters -CDSCDL, CDSCDLEXP |
| CF ^(b) | F/m | 0.0 | 0.0 | - | Outer fringe cap |
| CFRCOEFF ^(b) | F/m | 1.0 | 1.0 | - | Outer fringe cap coefficient |
| CGBO | F/m | 0.0 | 0.0 | - | Gate-substrate overlap capacitance per unit channel length |
| CGDL ^(b) | F/m | 0.0 | 0.0 | - | Overlap capacitance between gate and lightly-doped drain region |

Chapter 2: MOSFET Models

LEVEL 77: BSIM6 MOSFET Model

| Name | Unit | Default | Min | Max | Description |
|------------------------|--------------------------------------|------------------------------|-------|-----|---|
| CGDO | F/m | Calculated | 0.0 | - | Non LDD region drain-gate overlap capacitance per unit channel width |
| CGIDL ^(b) | - | 0.5 | - | - | exponential coefficient for GIDL |
| CGISL ^(b) | - | 0.5 | - | - | Exponential coefficient for GISL |
| CGSL ^(b) | F/m | 0.0 | 0.0 | - | Overlap capacitance between gate and lightly-doped source region |
| CGSO | F/m | Calculated | 0.0 | - | Non LDD region source-gate overlap capacitance per unit channel width |
| CIGC ^(b) | (F s ² /g) ^{0.5} | 0.075 (NMOS) and 0.03 (PMOS) | - | - | Parameter for I_{gcs} and I_{gcd} |
| CIGD(b) | (F s ² /g) ^{0.5} | 0.075 (NMOS) and 0.03 (PMOS) | - | - | Parameter for I_{gd} |
| CIGS ^(b) | (F s ² /g) ^{0.5} | 0.075 (NMOS) and 0.03 (PMOS) | - | - | Parameter for I_{gs} |
| CIT ^(b) | F/m ² | 1e-08 | 0.0 | - | Interface trap capacitance |
| CKAPPAD ^(b) | V | 0.6 | 0.02 | - | Coefficient of bias-dependent overlap capacitance for the drain side |
| CKAPPAS ^(b) | V | 0.6 | 0.02 | - | Coefficient of bias-dependent overlap capacitance for the source side |
| DELTA ^(b) | - | 0.125 | > 0 | 0.5 | Smoothing factor for Vds to Vdsat. Global Scaling Parameters -DELTAL, DELTALEXP |
| DLCIG ^(b) | m | LINT | - | - | Source/Drain overlap length for I_{gs} |
| DLCIGD ^(b) | m | DLCIG | - | - | Source/Drain overlap length for I_{gd} |
| DSUB ^(b) | - | 0.375 | > 0.0 | - | DIBL exponent coefficient |
| DVTP0 ^(b) | - | 1e-10 | - | - | Coefficient of drain-induced Vth shift for long channel devices with pocket implant |
| DVTP1 ^(b) | - | 0.0 | - | - | Coefficient of drain-induced Vth shift for long channel devices with pocket implant |

| Name | Unit | Default | Min | Max | Description |
|-----------------------|-------|---------|-------|-----|---|
| DVTP2 ^(b) | - | 0.0 | - | - | Coefficient of drain-induced Vth shift for long channel devices with pocket implant |
| DVTP3 ^(b) | - | 0.0 | - | - | Coefficient of drain-induced Vth shift for long channel devices with pocket implant |
| DVTP4 ^(b) | - | 0.0 | - | - | Coefficient of drain-induced Vth shift for long channel devices with pocket implant |
| DVTP5 ^(b) | - | 0.0 | - | - | Coefficient of drain-induced Vth shift for long channel devices with pocket implant |
| EGIDL ^(b) | - | 0.8 | - | - | band bending parameter for GIDL |
| EGISL ^(b) | - | 0.8 | - | - | band bending parameter for GISL |
| ETA0 ^(b) | - | 0.08 | - | - | DIBL coefficient |
| ETAB ^(b) | - | -0.07 | - | - | Body bias sensitivity to DIBL effect. Global Scaling Parameters ETABLEXP |
| ETAMOB | - | 1.0 | - | - | Effective field parameter |
| ETAQM | - | 0.54 | 0.0 | - | Bulk charge coefficient for charge centroid in inversion |
| EU ^(b) | cm/MV | 1.5 | > 0.0 | - | Phonon / surface roughness scattering. Global Scaling Parameters -EUL, EU-LEXP, EUW, EUWEXP, EUWL |
| FPROUT ^(b) | - | 0.0 | 0.0 | - | gds degradation factor due to pocket implant. Global Scaling Parameters -FPROUTL, FPROUTLEXP |
| K2 ^(b) | V | 0.0 | - | 0.0 | Vth shift due to nonuniform vertical doping. Global Scaling Parameters -K2L, K2LEXP, K2W, K2WEXP |
| LLONG | m | 10μm | - | - | Length of extracted long channel device |

Chapter 2: MOSFET Models
LEVEL 77: BSIM6 MOSFET Model

| Name | Unit | Default | Min | Max | Description |
|------------------------|-----------------|---------|-------|-----|--|
| NDEPCV ^(b) | m ⁻³ | NDEP | - | - | Channel (body) doping concentration for CV. Global Scaling Parameters - NDEPCVL1, NDEPCVLEXP1, NDEPCVL2, NDEPCVLEXP2, NDEPCVW, NDEPCVWEXP, NDEPCVWL, NDEPCVWLEXP |
| NFACTOR ^(b) | | 0.0 | 0.0 | - | Subthreshold Swing factor. Global Scaling Parameters -NFACTORL, NFACTORLEXP, NFACTORW, NFACTORWEXP, NFACTORWL |
| NTOX ^(b) | - | 1.0 | - | - | Exponent for the gate oxide ratio |
| PCLM ^(b) | - | 0.013 | > 0.0 | - | Channel Length Modulation (CLM) parameter. Global Scaling Parameters -PCLML, PCLMLEXP |
| PCLMCV ^(b) | - | PCLM | > 0.0 | - | Channel Length Modulation (CLM) parameter for CV. Global Scaling Parameters -PCLMCVL, PCLMCVLEXP |
| PCLMG | - | 0.0 | - | - | Gate bias dependent parameter for channel Length Modulation (CLM) |
| PDIBLC ^(b) | - | 2e-4 | 0.0 | - | DIBL effect on Rout. Global Scaling Parameters -PDIBLCL, PDI-BLCLEXP |
| PDIBLBC ^(b) | - | 0.0 | 0.0 | - | Body-bias sensitivity on DIBL |
| PDITS ^(b) | - | 0.0 | - | - | Drain-induced Vth shift |
| PDITSD ^(b) | - | 0.0 | ? | - | VDS dependence of Drain-induced Vth shift |
| PDITSL | - | 0.0 | ? | - | L dependence of Drain-induced Vth shift |
| PHIN ^(b) | V | 0.045 | - | - | Vertical nonuniform doping effect on surface potential |
| PIGCD ^(b) | - | 1.0 | - | - | Vds dependence of I_{gcs} and I_{gcd} . Global Scaling Parameters - PIGCDL, PIGCDLEXP |
| POXEDGE ^(b) | - | 1.0 | - | - | Factor for the gate oxide thickness in source/drain overlap regions |

| Name | Unit | Default | Min | Max | Description |
|------------------------|---------------------------|---------|-------|-----|--|
| PRWB ^(b) | V ⁻¹ | 0.0 | 0.0 | - | body bias dependence of S/D extension resistance. Global Scaling Parameters -PRWBL, PRWBLEXP |
| PRWG ^(b) | V ⁻¹ | 1.0 | 0.0 | - | gate bias dependence of S/D extension resistance |
| PSAT | - | 1.0 | 0.25 | 1.0 | Velocity saturation exponent. Global Scaling Parameters -PSATL, PSATLEXP |
| PSATB | - | 0.0 | - | - | Velocity saturation exponent for nonzero Vbs |
| PSATX | - | 1.0 | 0.25 | 4.0 | Fine tuning of PTWG effect |
| PSCBE1 ^(b) | - | 4.24e08 | - | - | Substrate current body-effect coefficient |
| PSCBE2 ^(b) | - | 1.0e08 | - | - | Substrate current body-effect coefficient |
| PTWG ^(b) | V ⁻² | 0.0 | - | - | Correction factor for velocity saturation. Global Scaling Parameters -PTWGL, PTWGLEXP |
| PVAG ^(b) | - | 1.0 | - | - | Vgs dependence on early voltage |
| QM0 | - | 1e-3 | > 0.0 | - | Charge centroid parameter -starting point for QME in inversion |
| RDSW ^(b) | $\Omega \cdot \mu_m^{WR}$ | 10.0 | 0.0 | - | Zero bias LDD resistance per unit width for RDSMOD=0. Global Scaling Parameters -RDSWL, RDSWLEXP |
| RDSWMIN ^(b) | $\Omega \cdot \mu_m^{WR}$ | 0.0 | 0.0 | - | LDD resistance per unit width at high Vgs for RDSMOD = 0 |
| RDW ^(b) | $\Omega \cdot \mu_m^{WR}$ | 10.0 | 0.0 | - | Zero bias drain extension resistance per unit width. Global Scaling Parameters -RDWL, RDWLEXP |
| RDWMIN ^(b) | $\Omega \cdot \mu_m^{WR}$ | 0.0 | 0.0 | - | Drain extension resistance per unit width at high Vgs |
| RSH | Ω | 0.0 | 0.0 | - | Sheet resistance |

Chapter 2: MOSFET Models

LEVEL 77: BSIM6 MOSFET Model

| Name | Unit | Default | Min | Max | Description |
|-------------------------|---------------------------|---------|-------|-----|---|
| RSW ^(b) | $\Omega \cdot \mu_m^{WR}$ | 10.0 | 0.0 | - | Zero bias source extension resistance per unit width. Global Scaling Parameters -RSWL, RSWLEXP |
| RSWMIN ^(b) | $\Omega \cdot \mu_m^{WR}$ | 0.0 | 0.0 | - | Source extension resistance per unit width at high Vgs |
| TOXREF | m | 3.0e-9 | - | - | Nominal gate oxide thickness for gate dielectric tunneling current model only |
| U0 ^(b) | $m^2/V \cdot s$ | 67e-02 | - | - | Low field mobility. Global Scaling Parameters -U0L, U0LEXP |
| UA ^(b) | $(cm/MV)^{EU}$ | 0.001 | > 0.0 | - | Phonon / surface roughness scattering. Global Scaling Parameters -UAL, UALEXP, UAW, UAWEXP, UAWL |
| UC ^(b) | - | 0.001 | > 0.0 | - | Body-bias sensitivity on mobility. Global Scaling Parameters -UCL, UCLEXP |
| UCS ^(b) | - | 2.0 | 1.0 | 2.0 | Coulombic scattering. |
| UD ^(b) | cm/MV | 0.001 | > 0.0 | - | Coulombic scattering. Global Scaling Parameters -UDL, UDLEXP |
| VFBCV ^(b) | m^{-3} | VFB | - | - | channel (body) doping concentration for CV. Global Scaling Parameters -VFBCVL, VFBCVLEXP, VF-BCVW, VFBCVWEXP, VFBCVWL, VFBCVWLEXP |
| VFBSDOFF ^(b) | V | 0.0 | - | - | Flatband Voltage offset parameter |
| VSAT ^(b) | m/s | 1e6 | - | - | Saturation velocity. Global Scaling Parameters -VSATL, VSATEXP, VSATW, VSATWEXP |
| VSATCV ^(b) | m/s | VSAT | - | - | Saturation velocity for CV. Global Scaling Parameters -VSATCVL, VSACVL-EXP, VSATCVW, VSATCVWEXP |
| WR ^(b) | - | 1.0 | - | - | W dependence parameter of S/D extension resistance |

| Name | Unit | Default | Min | Max | Description |
|-------|------|---------|-----|-----|--|
| WWIDE | m | 10μm | - | - | Width of extracted long channel device |

BSIM6 Model — High-Speed/RF Parameters

| Name | Unit | Default | Min | Max | Description |
|---------|------|-------------|-----|-----|--|
| GBMIN | Ω | 1.0e-12 mho | - | - | Conductance in parallel with each of the five substrate resistances to avoid potential numerical instability due to unreasonably too large a substrate resistance (Warning message is issued if less than 1.0e-20 mho) |
| RBDB | Ω | 50.0 Ω | - | - | Resistance connected between dbNode and bNode (Also an instance parameter). |
| RBDBX0 | Ω | 100.0 Ω | - | - | Scaling pre-factor for RBDBX |
| RBDBY0 | Ω | 100.0 Ω | - | - | Scaling pre-factor for RBDBY |
| RBPB | Ω | 50.0 Ω | - | - | Resistance connected between bNodePrime and bNode (Also an instance parameter). |
| RBPBX0 | Ω | 100.0 Ω | - | - | Scaling pre-factor for RBPBX |
| RBPBXL | - | 0.0 | - | - | Length scaling parameter for RBPBX |
| RBPBXNF | - | 0.0 | - | - | Number of fingers scaling parameter for RBPBX |
| RBPBXW | - | 0.0 | - | - | Width scaling parameter for RBPBX |
| RBPBY0 | Ω | 100.0 Ω | - | - | Scaling pre-factor for RBPBY |
| RBPBYL | - | 0.0 | - | - | Length scaling parameter for RBPBY |
| RBPBYNF | - | 0.0 | - | - | Number of fingers scaling parameter for RBPBY |
| RBPBYW | - | 0.0 | - | - | Width scaling parameter for RBPBY |
| RBPD | Ω | 50.0 Ω | - | - | Resistance connected between bNodePrime and dbNode (If less than 1.0e-3ohm, reset to 1.0e-3ohm) (Also an instance parameter). |
| RBPD0 | Ω | 50.0 Ω | - | - | Scaling pre-factor for RBPD |
| RBPDL | - | 0.0 | - | - | Length scaling parameter for RBPD |

Chapter 2: MOSFET Models

LEVEL 77: BSIM6 MOSFET Model

| Name | Unit | Default | Min | Max | Description |
|-----------------------|----------|----------------|-----|-----|---|
| RBPDNF | - | 0.0 | - | - | Number of fingers scaling parameter for RBPD |
| RBPDW | - | 0.0 | - | - | Width scaling parameter for RBPD |
| RBPS | Ω | 50.0 Ω | - | - | Resistance connected between bNodePrime and sbNode (If less than 1.0e-3ohm, reset to 1.0e-3ohm) (Also an instance parameter). |
| RBPS0 | Ω | 50.0 Ω | - | - | Scaling pre-factor for RBPS |
| RBPSL | - | 0.0 | - | - | Length Scaling parameter for RBPS |
| RBPSNF | - | 0.0 | - | - | Number of fingers scaling parameter for RBPS |
| RBPSW | - | 0.0 | - | - | Width Scaling parameter for RBPS |
| RBSB | Ω | 50.0 Ω | - | - | Resistance connected between sbNode and bNode (Also an instance parameter). |
| RBSBX0 | Ω | 100.0 Ω | - | - | Scaling pre-factor for RBSBX |
| RBSBY0 | Ω | 100.0 Ω | - | - | Scaling pre-factor for RBSBY |
| RBSDBXL | - | 0.0 | - | - | Length scaling parameter for RBSBX and RBDBX |
| RBSDBXNF | - | 0.0 | - | - | Number of finders scaling parameter for RBSBX and RBDBX |
| RBSDBXW | - | 0.0 | - | - | Width scaling parameter for RBSBX and RBDBX |
| RBSDBYL | - | 0.0 | - | - | Length scaling parameter for RBSBY and RBDBY |
| RBSDBYNF | - | 0.0 | - | - | Number of fingers scaling parameter for RBSBY and RBDBY |
| RBSDBYW | - | 0.0 | - | - | Width scaling parameter for RBSBY and RBDBY |
| XRCRG1 ^(b) | - | 12.0 | - | - | Parameter for distributed channel-resistance effect for both intrinsic-input resistance and charge-deficit NQS models (Warning message is issued if binned XRCRG1 <= 0:0) distributed channel-resistance effect for both intrinsic-input resistance and charge-deficit NQS models (Warning message is issued if binned XRCRG1 <= 0:0) |

| Name | Unit | Default | Min | Max | Description |
|-----------------------|------|---------|-----|-----|--|
| XRCRG2 ^(b) | - | 1.0 | - | - | Parameter to account for the excess channel diffusion resistance for both intrinsic input resistance and charge-deficit NQS models |

BSIM6 Model — Flicker and Thermal Noise Parameters

| Name | Unit | Default | Min | Max | Description |
|---------|------|---|-----|-----|--|
| AF | - | 1.0 | - | - | Flicker noise exponent |
| EF | - | 1.0 | - | - | Flicker noise frequency exponent |
| EM | - | 4.1e7V/m | - | - | Saturation field |
| KF | - | 0:0 ^{A2-EF} s ^{1-EF} | - | - | Flicker noise coefficient |
| LINTNOI | - | 0.0 m | - | - | Length Reduction Parameter Oset |
| NOIA | - | NMOS: 6:25e41(eV) ⁻¹ s ^{1-EF} EF _m ⁻³ | - | - | Flicker noise parameter A |
| | | PMOS: 3.125e26(eV) ⁻¹ s ^{1-EF} EF _m ⁻³ | | | |
| NOIB | - | NMOS: 3:125e26(eV) ⁻¹ s ^{1-EF} EF _m ⁻¹ | - | - | Flicker noise parameter B |
| | | PMOS: 1:5e25(eV) ⁻¹ s ^{1-EF} EF _m ⁻¹ | | | |
| NOIC | - | 8:75(eV) ⁻¹ s ^{1-EF} _m | - | - | Flicker noise parameter C |
| NTNOI | - | 1.0 | - | - | Noise factor for short-channel devices for TNOIMOD=0 only |
| RNOIA | - | 0.577 | - | - | Thermal Noise coefficient |
| RNOIB | - | 0.5164 | - | - | Thermal Noise coefficient |
| RNOIC | - | 0.395 | - | - | Correlation coefficient parameter |
| TNOIA | - | 1.5 | - | - | Coefficient of channel-length dependence of total channel thermal noise |
| TNOIB | - | 3.5 | - | - | Channel-length dependence parameter for channel thermal noise partitioning |

Chapter 2: MOSFET Models

LEVEL 77: BSIM6 MOSFET Model

| Name | Unit | Default | Min | Max | Description |
|-------|------|---------|-----|-----|--|
| TNOIC | - | 0 | - | - | Length dependent parameter for correlation coefficient |

BSIM6 Model — Layout-Dependent Parasitic Parameters

| Name | Unit | Default | Min | Max | Description |
|-------|------|--|-----|-----|--|
| DMCG | - | 0.0m | - | - | Distance from S/D contact center to the gate edge |
| DMCGT | - | 0.0m | - | - | DMCG of test structures |
| DMCI | - | DMCG | - | - | Distance from S/D contact center to the isolation edge in the channel-length direction |
| DMDG | - | 0.0m | - | - | Same as DMCG but for merged device only |
| DWJ | - | DWC (in CVmodel) | - | - | Offset of the S/D junction width |
| MINZ | - | 0 (minimize the drain diffusion fusion number) | - | - | Whether to minimize the number of drain or source diffusions for even-number fingered device (instance parameter only). |
| NF | - | 1 | - | - | Number of device fingers (Fatal error if less than one) (instance parameter only). |
| NGCON | - | 1 | - | - | Number of gate contacts (Fatal error if less than one; if not equal to 1 or 2, a warning message is issued and reset to 1) (Also an instance parameter). |
| XGL | - | 0.0m | - | - | Offset of the gate length due to variations in patterning |
| XGW | - | 0.0m | - | - | Distance from the gate contact to the channel edge (Also an instance parameter). |
| XL | - | 0.0m | - | - | Channel length offset due to mask/ etch effect |
| XW | - | 0.0m | - | - | Channel width offset due to mask/etch effect |

BSIM6 Model — Asymmetric Source/Drain Junction Diode Parameters

| Name | Unit | Default | Min | Max | Description |
|------|------|---------|-----|-----|---|
| BVD | - | BVS | - | - | Breakdown voltage (If not positive, reset to 10.0V) |

| Name | Unit | Default | Min | Max | Description |
|----------|------|-------------------------|-----|-----|--|
| BVS | - | 10.0 V | - | - | Breakdown voltage (If not positive, reset to 10.0V) |
| CJD | - | CJS | - | - | Bottom junction capacitance per unit area at zero bias |
| CJS | - | 5.0e-4 F/m ² | - | - | Bottom junction capacitance per unit area at zero bias |
| CJSWD | - | CJSWS | - | - | Isolation-edge sidewall junction capacitance per unit area |
| CJSWGD | - | CJSWS | - | - | Gate-edge sidewall junction capacitance per unit length |
| CJSWGS | - | CJSWS | - | - | Gate-edge sidewall junction capacitance per unit length |
| CJSWS | - | 5.0e-10 F/m | - | - | Isolation-edge sidewall junction capacitance per unit area |
| IJTHDFWD | - | IJTHSFWD | - | - | Limiting current in forward bias region (If not positive, reset to 0.1A) |
| IJTHDREV | - | IJTHSREV | - | - | Limiting current in reverse bias region (If not positive, reset to 0.1A) |
| IJTHSFWD | - | 0.1A | - | - | Limiting current in forward bias region (If not positive, reset to 0.1A) |
| IJTHSREV | - | 0.1A | - | - | Limiting current in reverse bias region (If not positive, reset to 0.1A) |
| JSD | - | JSS | - | - | Bottom junction reverse saturation current density |
| JSS | - | 1.0e-4A/m ² | - | - | Bottom junction reverse saturation current density |
| JSWD | - | JSWS | - | - | Isolation-edge sidewall reverse saturation current density |
| JSWGD | - | JSWGS | - | - | Gate-edge sidewall reverse saturation current density |
| JSWGS | - | 0.0A/m | - | - | Gate-edge sidewall reverse saturation current density |

Chapter 2: MOSFET Models

LEVEL 77: BSIM6 MOSFET Model

| Name | Unit | Default | Min | Max | Description |
|---------|------|---------------------|-----|-----|--|
| JSWS | - | 0.0A/m | - | - | Isolation-edge sidewall reverse saturation current density |
| JTSD | - | JTSS | - | - | Bottom trap-assisted saturation current density |
| JTSS | - | 0.0A/m | - | - | Bottom trap-assisted saturation current density |
| JTSSWD | - | JTSSWS | - | - | STI sidewall trap-assisted saturation current density |
| JTSSWGD | - | JTSSWGS | - | - | Gate-edge sidewall trap-assisted saturation current density |
| JTSSWGS | - | 0.0A/m | - | - | Gate-edge sidewall trap-assisted saturation current density |
| JTSSWS | - | 0.0A/m ² | - | - | STI sidewall trap-assisted saturation current density |
| JTWEFF | - | 0.0 | - | - | Trap-assistant tunneling current density width dependence |
| MJD | - | MJS | - | - | Bottom junction capacitance grating coefficient |
| MJS | - | 0.5 | - | - | Bottom junction capacitance grating coefficient |
| MJSWD | - | MJSWS | - | - | Isolation-edge sidewall junction capacitance grading coefficient |
| MJSWGD | - | MJSWS | - | - | Gate-edge sidewall junction capacitance grading coefficient |
| MJSWGS | - | MJSWS | - | - | Gate-edge sidewall junction capacitance grading coefficient |
| MJSWS | - | 0.33 | - | - | Isolation-edge sidewall junction capacitance grading coefficient |
| NJTS | - | 20.0 | - | - | Non-ideality factor for JTSS and JTSD |
| NJTSD | - | NJTS | - | - | Non-ideality factor for JTSS and JTSD |
| NJTSSW | - | 20.0 | - | - | Non-ideality factor for JTSSWS and JTSSWD |
| NJTSSWD | - | NJTSSW | - | - | Non-ideality factor for JTSSWS and JTSSWD |

| Name | Unit | Default | Min | Max | Description |
|-----------|------|----------|-----|-----|--|
| NJTSSWG | - | 20.0 | - | - | Non-ideality factor for JTSSWGS and JTSSWGD |
| NJTSSWGD | - | NJTSSWG | - | - | Non-ideality factor for JTSSWGS and JTSSWGD |
| PBD | - | PBS | - | - | Bottom junction built-in potential |
| PBS | - | 1.0V | - | - | Bottom junction built-in potential |
| PBSWD | - | PBSWS | - | - | Isolation-edge sidewall junction built-in potential |
| PBSWGD | - | PBSWGS | - | - | Gate-edge sidewall junction built-in potential |
| PBSWGS | - | 1.0V | - | - | Gate-edge sidewall junction built-in potential |
| PBSWS | - | 1.0V | - | - | Isolation-edge sidewall junction built-in potential |
| TNJTS | - | 0.0 | - | - | Temperature coefficient for NJTS and NJTSD |
| TNJTSD | - | TNJTS | - | - | Temperature coefficient for NJTS and NJTSD |
| TNJTSSW | - | 0.0 | - | - | Temperature coefficient for NJTSSW and NJTSSWD |
| TNJTSSWD | - | TNJTSSW | - | - | Temperature coefficient for NJTSSW and NJTSSWD |
| TNJTSSWG | - | 0.0 | - | - | Temperature coefficient for NJTSSWG and NJTSSWG |
| TNJTSSWGD | - | TNJTSSWG | - | - | Temperature coefficient for NJTSSWG and NJTSSWG |
| VTSD | - | VTSS | - | - | Bottom trap-assisted voltage dependent parameter |
| VTSS | - | 10.0 V | - | - | Bottom trap-assisted voltage dependent parameter |
| VTSSWD | - | VTSSWS | - | - | STI sidewall trap-assisted voltage dependent parameter |
| VTSSWGD | - | VTSSWS | - | - | Gate-edge sidewall trap-assisted voltage dependent parameter |

Chapter 2: MOSFET Models

LEVEL 77: BSIM6 MOSFET Model

| Name | Unit | Default | Min | Max | Description |
|---------|------|---------|-----|-----|--|
| VTSSWGS | - | 10.0 V | - | - | Gate-edge sidewall trap-assisted voltage dependent parameter |
| VTSSWS | - | 10.0 V | - | - | STI sidewall trap-assisted voltage dependent parameter |
| XJBVD | - | XJBVS | - | - | Fitting parameter for diode breakdown |
| XJBVS | - | 1.0 | - | - | Fitting parameter for diode breakdown |
| XTSD | - | 0.02 | - | - | Power dependence of JTSS, JTSD on temperature |
| XTSS | - | 0.02 | - | - | Power dependence of JTSS, JTSD on temperature |
| XTSSWD | - | 0.02 | - | - | Power dependence of JTSSWS, JTSSWD on temperature |
| XTSSWGD | - | 0.02 | - | - | Power dependence of JTSSWGS, JTSSWGD on temperature |
| XTSSWGS | - | 0.02 | - | - | Power dependence of JTSSWGS, JTSSWGD on temperature |
| XTSSWS | - | 0.02 | - | - | Power dependence of JTSSWS, JTSSWD on temperature |

BSIM6 Model — Temperature-Dependent Parameters

| Name | Unit | Default | Min | Max | Description |
|---------------------|------|-----------|-----|-----|--|
| AT ^(b) | m/s | 3.3e4 m/s | - | - | Temperature coefficient for saturation velocity |
| DTEMP | - | 0 | - | - | Variability handle for temperature |
| KT1 | V | -0.11V | - | - | Temperature coefficient for threshold voltage |
| KT1EXP | - | 1.0 | - | - | Temperature exponent for threshold voltage |
| KT1L ^(b) | Vm | 0.0Vm | - | - | Channel length dependence of the temperature coefficient for threshold voltage |

| Name | Unit | Default | Min | Max | Description |
|-------------------------|-------------------|---|-----|-----|--|
| KT2 ^(b) | - | 0.022 | - | - | Body-bias coefficient of V_{th} temperature effect |
| NJD | - | NJS | - | - | Emission coefficients of junction for source and drain junctions, respectively |
| NJS | - | 1.0 | - | - | Emission coefficients of junction for source and drain junctions, respectively |
| PRT ^(b) | - | 0.0 ohm-m | - | - | Temperature coefficient for R_{dsW} |
| PTWGT ^(b) | - | 0.0 | - | - | Temperature coefficient for PTWG |
| TCJ | 1/ ^o K | 0.0 | - | - | Temperature coefficient of CJ |
| TCJSW | 1/ ^o K | 0.0 | - | - | Temperature coefficient of CJSW |
| TCJSWG ^(b) | 1/ ^o K | 0.0 | - | - | Temperature coefficient of CJSWG |
| TETA0 ^(b) | - | 0.0 | - | - | Temperature coefficient of ETA0 |
| TNFACTOR ^(b) | - | 0.0 | - | - | Temperature coefficient of NFACTOR |
| TNOM | °C | 27°C | - | - | Temperature at which the model is extracted |
| TPB | V/K | 0.0 | - | - | Temperature coefficient of PB |
| TPBSW | V/K | 0.0 | - | - | Temperature coefficient of PBSW |
| TPBSWG | V/K | 0.0 | - | - | Temperature coefficient of PBSWG |
| TVFBSDOFF | 1/ ^o K | 0.0 | - | - | Temperature coefficient of VFBSDOFF |
| UA1 ^(b) | - | 1.0e-9m/V | - | - | Temperature coefficient for UA |
| UC1 ^(b) | - | 0.056V-1 for MOBMOD=1; 0.056e-9m/V ² for MOBMOD=0 and 2 | - | - | Temperature coefficient for UC |
| UCSTE ^(b) | - | -4.775e-3 | - | - | Temperature coefficient of coulombic mobility |

Chapter 2: MOSFET Models

LEVEL 77: BSIM6 MOSFET Model

| Name | Unit | Default | Min | Max | Description |
|--------------------|------|------------------------|-----|-----|---|
| UD1 ^(b) | - | 0:0 (1/m) ² | - | - | Temperature coefficient for UD |
| UTE ^(b) | - | -1.5 | - | - | Mobility temperature exponent |
| XTID | - | XTIS | - | - | Junction current temperature exponents for source and drain junctions, respectively |
| XTIS | - | 3.0 | - | - | Junction current temperature exponents for source and drain junctions, respectively |

BSIM6 Model — Stress Effect Parameters

| Name | Unit | Default | Min | Max | Description |
|---------|------|---------|-----|-----|--|
| KU0 | - | 0.0m | - | - | Mobility degradation/enhancement coefficient for stress effect |
| KVSAT | - | 0.0m | - | - | Saturation velocity degradation/ enhancement parameter for stress effect (1 <= kvsat <= 1) |
| KVTH0 | - | 0.0 Vm | - | - | Threshold shift parameter for stress effect |
| LKU0 | - | 1e-6m | - | - | Length dependence of ku0 |
| LKVTH0 | - | 0.0 | - | - | Length dependence of kvth0 |
| LLODKU0 | - | 0.0 | - | - | Length parameter for u0 stress effect (>0) |
| LLODVTH | - | 0.0 | - | - | Length parameter for Vth stress effect (>0) |
| LODETA0 | - | 1.0 | - | - | eta0 shift modification factor for stress effect (>0) |
| LODK2 | - | 0.0 | - | - | K2 shift modification factor for stress effect (>0) |
| PKU0 | - | 0.0 | - | - | Cross-term dependence of ku0 |
| PKVTH0 | - | 0.0 | - | - | Cross-term dependence of kvth0 |
| SA | - | 0.0 | - | - | Distance between OD edge to Poly from one side (If not given or (<= 0), stress effect will be turned-off) (An instance parameter). |
| SAreff | - | 1e-6m | - | - | Reference distance between OD and edge to poly of one side (>0.0) |

| Name | Unit | Default | Min | Max | Description |
|---------|------|---------|-----|-----|---|
| SB | - | 0.0 | - | - | Distance between OD edge to Poly from other side (If not given or (≤ 0), stress effect will be turned-off) (An instance parameter). |
| SBref | - | 1e-6m | - | - | Reference distance between OD and edge to poly of the other side (>0.0) |
| SD | - | 0.0 | - | - | Distance between neighboring fingers (For $NF > 1$: If not given or (≤ 0), stress effect will be turned-off) (An instance parameter). |
| STETA0 | - | 0.0m | - | - | η_{t0} shift factor related to V_{th0} change |
| STK2 | - | 0.0m | - | - | K_2 shift factor related to V_{th0} change |
| TKU0 | - | 0.0 | - | - | Temperature coefficient of K_{U0} |
| WKU0 | - | 0.0 | - | - | Width dependence of k_{U0} |
| WKVTH0 | - | 0.0 | - | - | Width dependence of k_{Vth0} |
| WLOD | - | 0.0m | - | - | Width parameter for stress effect |
| WLODKU0 | - | 0.0 | - | - | Width parameter for U_0 stress effect (>0) |
| WLODVTH | - | 0.0 | - | - | Width parameter for V_{th} stress effect (>0) |

BSIM6 Model — Well-Proximity Effect Parameters

| Name | Unit | Default | Min | Max | Description |
|--------------------|------|---------|-----|-----|---|
| $K_{2WE}^{(b)}$ | - | 0.0 | - | - | K_2 shift factor for well proximity effect |
| $K_{U0WE}^{(b)}$ | - | 0.0 | - | - | Mobility degradation factor for well proximity effect |
| $K_{VTH0WE}^{(b)}$ | - | 0.0 | - | - | Threshold shift factor for well proximity effect |
| SC | - | 0.0m | - | - | Distance to a single well edge (If not given or ≤ 0 : turn-off WPE) (An instance parameter). |
| SCA | - | 0.0 | - | - | Integral of the first distribution function for scattered well dopant (If not given, calculated) (An instance parameter). |

Chapter 2: MOSFET Models

LEVEL 77: BSIM6 MOSFET Model

| Name | Unit | Default | Min | Max | Description |
|-------|------|---------|-----|-----|--|
| SCB | - | 0.0 | - | - | Integral of the second distribution function for scattered well dopant (If not given, calculated) (An instance parameter). |
| SCREF | - | 1e-6m | - | - | Reference distance to calculate SCA, SCB and SCC (<0) |
| SCC | - | 0.0 | - | - | Integral of the third distribution function for scattered well dopant (If not given, calculated) (An instance parameter). |
| WEB | - | 0.0 | - | - | Coefficient for SCB (>0.0) |
| WEC | - | 0.0 | - | - | Coefficient for SCC (>0.0) |

BSIMx and BSIMx SOI — Supported Instance Parameters

The following lists the instance parameters that are currently supported by HSPICE in these four model types:

| Instance Parameter | BSIM3 | BSIM4 | BSIM3 SOI | BSIMSOI4 |
|--------------------|-------|-------|-----------|----------|
| ACNQSMOD | yes | yes | no | no |
| AD | yes | yes | yes | yes |
| AS | yes | yes | yes | yes |
| CTH0 | yes | no | yes | yes |
| DELDVT0 | no | yes | no | no |
| DELK1 | yes | yes | no | yes |
| DELK2 | no | yes | yes | no |
| DELNFCFT | yes | yes | no | yes |
| DELLPE0 | no | yes | no | no |
| DELRSRH | no | yes | no | no |
| DELRSHG | no | yes | no | no |
| DELTOX | yes | yes | yes | yes |
| DELVTO | yes | yes | yes | yes |
| DELXJ | no | yes | no | no |
| DTEMP | yes | yes | yes | yes |
| GEO | yes | yes | no | no |
| GEOMOD | no | yes | no | no |
| IC | yes | yes | yes | yes |
| L | yes | yes | yes | yes |

Chapter 2: MOSFET Models

BSIMx and BSIMx SOI — Supported Instance Parameters

| Instance Parameter | BSIM3 | BSIM4 | BSIM3 SOI | BSIMSOI4 |
|--------------------|-------|-------|-----------|----------|
| MIN | no | yes | no | no |
| MULID0 | no | yes | yes | yes |
| MULNGATE | no | yes | no | no |
| MULU0 | yes | yes | yes | yes |
| MULVSAT | no | yes | no | yes |
| NF | no | yes | yes | yes |
| NGCON | no | yes | no | no |
| NRD | yes | yes | yes | yes |
| NRS | yes | yes | yes | yes |
| OFF | yes | yes | yes | yes |
| PD | yes | yes | yes | yes |
| PS | yes | yes | yes | yes |
| RBDB | no | yes | no | yes |
| RBODYMOD | no | yes | no | yes |
| RBPB | no | yes | no | yes |
| RBPD | no | yes | no | no |
| RBPS | no | yes | no | no |
| RBSB | no | yes | no | yes |
| RDC | no | yes | no | no |
| RGATEMOD | no | yes | yes | yes |
| RGEOMOD | no | yes | no | no |
| RSC | no | yes | no | no |
| RTH0 | yes | no | no | no |
| SA | yes | yes | no | yes |

Chapter 2: MOSFET Models
BSIMx and BSIMx SOI — Supported Instance Parameters

| Instance Parameter | BSIM3 | BSIM4 | BSIM3 SOI | BSIMSOI4 |
|--------------------|---------------|-------|-----------|----------|
| SA1 | yes | yes | no | no |
| SA10 | yes | yes | no | no |
| SA2 | yes | yes | no | no |
| SA3 | yes | yes | no | no |
| SA4 | yes | yes | no | no |
| SA5 | yes | yes | no | no |
| SA6 | yes | yes | no | no |
| SA7 | yes | yes | no | no |
| SA8 | yes | yes | no | no |
| SA9 | yes | yes | no | no |
| SB | yes | yes | no | yes |
| SB1 | yes | yes | no | no |
| SB10 | yes | yes | no | no |
| SB2 | yes | yes | no | no |
| SB3 | yes | yes | no | no |
| SB4 | yes | yes | no | no |
| SB5 | yes | yes | no | no |
| SB6 | yes | yes | no | no |
| SB7 | yes | yes | no | no |
| SB8 | yes | yes | no | no |
| SB9 | yes | yes | no | no |
| SC | 3.22 or later | yes | no | no |
| SCA | 3.22 or later | yes | no | no |
| SCB | 3.22 or later | yes | no | no |

Chapter 2: MOSFET Models

BSIMx and BSIMx SOI — Supported Instance Parameters

| Instance Parameter | BSIM3 | BSIM4 | BSIM3 SOI | BSIMSOI4 |
|--------------------|---------------|-------|-----------|----------|
| SCC | 3.22 or later | yes | no | no |
| SD | yes | yes | no | yes |
| SOIQ0 | no | no | yes | yes |
| STIMOD | yes | yes | no | no |
| SW1 | yes | yes | no | no |
| SW10 | yes | yes | no | no |
| SW2 | yes | yes | no | no |
| SW3 | yes | yes | no | no |
| SW4 | yes | yes | no | no |
| SW5 | yes | yes | no | no |
| SW6 | yes | yes | no | no |
| SW7 | yes | yes | no | no |
| SW8 | yes | yes | no | no |
| SW9 | yes | yes | no | no |
| TNODEOUT | yes | no | yes | yes |
| TRNQSMOD | no | yes | no | no |
| W | yes | yes | yes | yes |
| XGW | no | yes | no | no |

References

- [1] Vladimirescu, Andrei and Liu, Sally. "Simulation of MOS Integrated Circuits Using SPICE2." University of California at Berkeley: Memorandum No. UCB/ERL M80/7, February 1980.
- [2] Huang, J.S., and Taylor, G.W. "Modeling of an Ion-Implanted Silicon Gate Depletion-Mode IGFET." *IEEE Trans. Elec. Dev.*, Vol. ED-22, pp. 995-1000, Nov. 1975.
- [3] Frohman-Bentchkowski, D. and Grove, A. S. "On the Effect of Mobility Variation on MOS Device Characteristics," *Proc. IEEE*, 56, 1968.
- [4] Fargher, H. E. and Mole, P. J. The Implementation Of A 3 Terminal SOSFET Model In SPICE For Circuit Simulation. GEC VLSI Research Laboratory, MOS1 Division.
- [5] Marciniak, W. et. al., "Comments on the Huang and Taylor Model of Ion-Implanted Silicon-gate Depletion-Mode IGFET," *Solid State Electron.*, Vol. 28, No.3, pp. 313-315, 1985.
- [6] Ballay, N. et. al., "Analytic Modeling of Depletion-Mode MOSFET with Short- and Narrow-Channel Effects," *IEEE PROC*, Vol. 128, Pt.I, No.6 (1981).
- [7] Tsividis, Y. Operations and Modeling of the MOS Transistor, McGraw-Hill, New York, 1987 p. 145; p. 241f. BFRC's counterpart in BSIM is x2u0.
- [8] Jeng, M. C. *Design and Modeling of Deep Submicrometer MOSFETs*, Ph.D. Dissertation, University of California, Berkeley, 1989.
- [9] Duster, J.S., Jeng,M.C., Ko, P. K. and Hu, C. *User's Guide for the BSIM2 Parameter Extraction Program and the SPICE3 with BSIM Implementation*. Industrial Liaison Program, Software Distribution Office, University of California, Berkeley, May 1990.
- [10] Duster, J.S., Jeng, M.C., Ko, P. K., and Hu, C. *User's Guide for the BSIM2 Parameter Extraction Program and the SPICE3 with BSIM Implementation*. Industrial Liaison Program, Software Distribution Office, University of California, Berkeley, May 1990.
- [11] *Surface potential based model of ultra-thin fully depleted SOI MOSFET for IC simulations*, O. Rozeau, M.-A. Jaud, T. Poiroux and M. Benosman, 2011 IEEE International SOI conference, Tempe Arizona, USA, October 2011.

Chapter 2: MOSFET Models

References

- [12] *PSP: An Advanced Surface-Potential-Based MOSFET Model for Circuit Simulation*, G. Gildenblat, X. Li, W. Wu, H. Wang, A. Jha, R. van Langevelde, G. D. J. Smit, A. J. Scholten and D. B. M. Klaassen, IEEE Trans. on Electron Devices, Vol. 53, No. 9, Sept. 2006.

MOSFET Capacitance Models

This chapter discusses use of available capacitance models.

HSPICE ships hundreds of examples for your use; see [Listing of Demonstration Input Files](#) for paths to demo files.

This section covers the following topics:

- [MOS Gate Capacitance Models](#)
- [Selecting Capacitor Models](#)
- [Transcapacitance](#)
- [Operating Point Capacitance Printout](#)
- [Element Template Printout](#)
- [Calculating Gate Capacitance](#)
- [MOSFET Gate Capacitance — Model Parameters](#)
- [Specifying XQC and XPART for CAPOP=4, 9, 11, 12, 13](#)
- [Overlap Capacitance Equations](#)
- [CAPOP=0 — SPICE Meyer Gate Capacitances](#)
- [CAPOP=1 — Modified Meyer Gate Capacitances](#)
- [CAPOP=2—Parameterized Modified Meyer Capacitance](#)
- [CAPOP=3 — Gate Capacitances \(Simpson Integration\)](#)
- [CAPOP=4 — Charge Conservation Capacitance Model](#)
- [CAPOP=5 — No Gate Capacitance](#)
- [CAPOP=6 — AMI Gate Capacitance Model](#)
- [CAPOP=13 — BSIM1-based Charge-Conserving Gate Capacitance Model](#)

Chapter 3: MOSFET Capacitance Models

MOS Gate Capacitance Models

- [CAPOP=39 — BSIM2 Charge-Conserving Gate Capacitance Model](#)
 - [Calculating Effective Length and Width for AC Gate Capacitance](#)
-

MOS Gate Capacitance Models

You can use capacitance model parameters with all MOSFET model statements.

Three fixed-capacitance parameters (`CGDO`, `CGSO`, and `CGBO`) represent gate-to-drain, gate-to-source, and gate-to-bulk overlap capacitances to model charge storage, use fixed and nonlinear gate capacitances and junction capacitances. The algorithm used for calculating nonlinear, voltage-dependent MOS gate capacitance depends on the value of the `CAPOP` model parameter.

To model MOS gate capacitances as a nonlinear function of terminal voltages, use Meyer's piecewise linear model for all MOS levels. The charge conservation model is also available for MOSFET model Levels 2 through 7, 13, and 27. For LEVEL 1, you must specify the `TOX` model parameter to invoke the Meyer model. The next three sections describe the Meyer, Modified Meyer, and Charge Conservation MOS Gate Capacitance models.

Some of the charge conserving models (Ward-Dutton or BSIM) can cause “timestep too small” errors if you do not specify other nodal capacitances.

Selecting Capacitor Models

When you select a gate capacitance model, you can choose various combinations of capacitor models and DC models. You can incrementally update older DC models with new capacitance equations, without having to move to a new DC model. You can use the `CAPOP` model parameter to select the gate capacitance and validate the effects of different capacitance models.

The `CAPOP` capacitance model selection parameter selects the capacitor models to use for modeling the MOS gate capacitance:

- gate-to-drain capacitance
- gate-to- source capacitance
- gate-to-bulk capacitance.

You can use CAPOP to select several versions of the Meyer and charge conservation model.

Some capacitor models are tied to specific DC models (DC model level in parentheses below). Other models are designated as general; any DC model can use them.

| Parameter | Description |
|-----------|--|
| CAPOP=0 | SPICE original Meyer gate-capacitance model (general) |
| CAPOP=1 | Modified Meyer gate-capacitance model (general) |
| CAPOP=2 | Parameterized Modified Meyer gate-capacitance model (general default) |
| CAPOP=3 | Parameterized Modified Meyer gate-capacitance model with Simpson integration (general) |
| CAPOP=4 | Charge conservation capacitance model (analytic), Levels 2, 3, 6, 7, 13, 28, and 39 only |
| CAPOP=5 | No capacitor model |
| CAPOP=6 | AMI capacitor model (LEVEL 5) |
| cAPOP=9 | Charge conservation model (LEVEL 3) |
| CAPOP=11 | Ward-Dutton model (specialized, LEVEL 2) |
| CAPOP=12 | Ward-Dutton model (specialized, LEVEL 3) |
| CAPOP=13 | Generic BSIM Charge-Conserving Gate Capacitance model (default for Levels 13, 28, 39) |
| CAPOP=39 | BSIM2 Charge-Conserving Gate Capacitance model (LEVEL 39) |

CAPOP=4 selects the recommended charge-conserving model from among CAPOP=11, 12, or 13 for the specified DC model.

| MOS Level | Default CAPOP | CAPOP=4 selects |
|------------|---------------|-----------------|
| 2 | 2 | 11 |
| 3 | 2 | 12 |
| 13, 28, 39 | 13 | 13 |

Chapter 3: MOSFET Capacitance Models

Transcapacitance

| MOS Level | Default CAPOP | CAPOP=4 selects |
|--------------|---------------|-----------------|
| Other levels | 2 | 11 |

The proprietary models (Levels 5, 17, 21, 22, 25, 31, 33), the SOS model (LEVEL 27), and models higher than 49 have their own built-in capacitance routines.

Transcapacitance

If a capacitor has two terminals (1 and 2) with charges named Q1 and Q2 on the two terminals that sum to zero (for example, Q1=-Q2), then the charge is a function of the voltage difference between the terminals ($V_{12}=V_1-V_2$). One quantity ($C=dQ_1/dV_{12}$) completely describes the small-signal characteristics of the device.

If a capacitor has four terminals, the sum of the charges on the four terminals must equal zero ($Q_1+Q_2+Q_3+Q_4=0$). They can depend only on voltage differences, but they are otherwise arbitrary functions. Because three independent charges (Q_1 , Q_2 , Q_3) are functions of three independent voltages (V_{14} , V_{24} , V_{34}), you must specify nine derivatives to describe the small-signal characteristics.

You can consider the four charges separately as functions of the four terminal voltages, $Q_1(V_1, V_2, V_3, V_4)$, ... $Q_4(V_1, V_2, V_3, V_4)$. The derivatives form a four-by-four matrix, dQ_i/dV_j , $i=1..4$, $j=1..4$. Simulation directly interprets this matrix as AC measurements.

If you apply an AC voltage signal to the j terminal and you ground the other terminals to AC, and if you measure AC current into the i terminal, then the current is the imaginary constant times $2\pi i \text{frequency} \times dQ_i/dV_j$.

- Because the charges add up to zero, each column of this matrix must add up to zero.
- Because the charges can depend only on voltage differences, each row must add up to zero.

In general, the matrix is not symmetrical:

dQ_i/dV_j need not equal dQ_j/dV_i

This is not an expected event because it does not occur for the two-terminal case. For two terminals, because the rows and columns must add up to zero, dQ_1/dV_2 must equal dQ_2/dV_1 .

$$\frac{dQ_1}{dV_1} + \frac{dQ_2}{dV_1} = 0, \frac{dQ_1}{dV_1} + \frac{dQ_1}{dV_2} = 0$$

For three or more terminals, this relation does not generally hold.

The terminal input capacitances are the diagonal matrix entries:

$$C_{ii} = dQ_i/dV_i \quad i=1, .4$$

The transcapacitances are the negative of off-diagonal entries:

$$C_{ij} = -dQ_i/dV_j \quad i \text{ not equal to } j$$

All of the C values are normally positive.

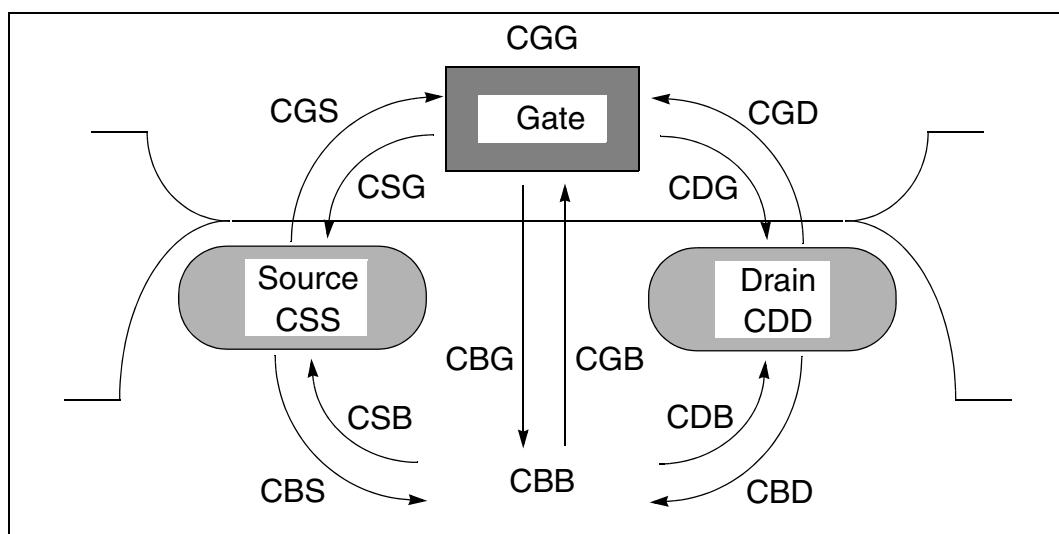


Figure 18 MOS Capacitances

In Figure 18, C_{ij} determines the current transferred out of the i node from a voltage change on the j node. The arrows, representing direction of influence, point from node j to node i .

A MOS device with terminals named D, G, S, and B provides:

$$CGG = \frac{dQ_g}{dVG}, CGD = -\frac{dQ_g}{dVD}, CDG = -\frac{dQ_D}{dVG}$$

Chapter 3: MOSFET Capacitance Models

Operating Point Capacitance Printout

- CGG represents input capacitance: a change in gate voltage requires a current equal to $CGG \cdot dV_G/dt$ into the gate terminal.
- CGD represents Miller feedback: a change in drain voltage creates a current equal to $CGG \cdot dV_D/dt$ out of the gate terminal.
- CDG represents Miller feedthrough, capacitive current out of the drain due to a change in gate voltage.

To show how CGD might not equal CDG, the following example is a simplified model with no bulk charge with a gate charge as a function of VGS only, and with the 50/50 channel charge partitioned into QS and QD:

$$QG = Q(vgs), QS = -0.5 \cdot Q(vgs), QD = -0.5 \cdot Q(vgs), QB = 0$$

Consequently:

$$CGD = -\frac{dQG}{dVD} = 0, CDG = -\frac{dQD}{dVG} = 0.5 \cdot \frac{dQ}{dvgs}$$

Therefore, this model has Miller feed through, but no feedback.

Operating Point Capacitance Printout

The operating point printout reports six capacitances:

| Capacitance | Value |
|-------------|------------|
| cdtot | dQD/dVD |
| cgtot | dQG/dVG |
| cstot | dQS/dVS |
| cbtot | dQB/dVB |
| cgs | $-dQG/dVS$ |
| cgd | $-dQG/dVD$ |

These capacitances include gate-drain, gate-source, and gate-bulk overlap capacitance, and drain-bulk and source-bulk diode capacitance. Drain and source refer to node 1 and 3 of the MOS element (physical instead of electrical).

The following table shows the printout quantities for the Meyer models, where charges such as QD are not well defined.

| Capacitance | Value |
|-------------|-------------|
| cdtot | cgd+cdb |
| cgtot | cgs+cgd+cgb |
| cstot | cgs+csb |
| cbtot | cgb+csb+cdb |
| cgs | cgs |
| cgd | cgd |

Element Template Printout

The MOS element template printouts for gate capacitance are LX18 to LX23 and LX32 to LX34. From these nine capacitances, you can construct the complete four-by-four matrix of transcapacitances. The nine LX printouts are:

$$\begin{aligned}
 LX18 \text{ (m)} &= dQG/dVGB = CGGBO \\
 LX19 \text{ (m)} &= dQG/dVDB = CGDBO \\
 LX20 \text{ (m)} &= dQG/dVSB = CGSBO \\
 LX21 \text{ (m)} &= dQB/dVGB = CBGBO \\
 LX22 \text{ (m)} &= dQB/dVDB = CBDBO \\
 LX23 \text{ (m)} &= dQB/dVSB = CBSBO \\
 LX32 \text{ (m)} &= dQD/dVG = CDGBO \\
 LX33 \text{ (m)} &= dQD/dVD = CDDBO \\
 LX34 \text{ (m)} &= dQD/dVS = CDSBO
 \end{aligned}$$

These capacitances include gate-drain, gate-source, and gate-bulk overlap capacitance, and drain-bulk and source-bulk diode capacitance. Drain and source refer to node 1 and 3 of the MOS element (physical instead of electrical).

For an NMOS device with source and bulk grounded:

- LX18 is the input capacitance.
- LX33 is the output capacitance.

Chapter 3: MOSFET Capacitance Models

Calculating Gate Capacitance

- LX19 is the Miller feedback capacitance (gate current induced by voltage signal on the drain).
- LX32 is the Miller feedthrough capacitance (drain current induced by the voltage signal on the gate).

A device operating with node 3 as electrical drain —for example an NMOS device with node 3 at higher voltage than node 1— is in *reverse mode*.

The LX values are physical, but you can translate them into electrical definitions by interchanging D and S:

$$\begin{aligned} \text{CGG (reverse)} &= \text{CGG} = \text{LX18} \\ \text{CDD (reverse)} &= \text{CSS} = dQ_S/dV_S = d(-Q_G-Q_B-Q_D)/dV_S = \\ &\quad -\text{LX20}-\text{LX23}-\text{LX34} \\ \text{CGD (reverse)} &= \text{CGS} = -\text{LX20} \\ \text{CDG (reverse)} &= \text{CSG} = -dQ_S/dV_G = d(Q_G+Q_B+Q_D)/dV_G = \\ &\quad \text{LX18}+\text{LX21}+\text{LX32} \end{aligned}$$

For Meyer models, QD and other charges are not well defined. The formulas (such as LX18= CGG, LX19= -CGD) are still true, but the transcapacitances are symmetrical; for example, CGD=CDG. In terms of the six independent Meyer capacitances (cgd, cgs, cgb, cdb, csb, and cds), the LX printouts are:

$$\begin{aligned} \text{LX18 (m)} &= \text{CGS}+\text{CGD}+\text{CGB} \\ \text{LX19 (m)} &= \text{LX32 (m)} = -\text{CGD} \\ \text{LX20 (m)} &= -\text{CGS} \\ \text{LX21 (m)} &= -\text{CGB} \quad \text{LX22 (m)} = -\text{CDB} \\ \text{LX23 (m)} &= -\text{CSB} \\ \text{LX33 (m)} &= \text{CGD}+\text{CDB}+\text{CDS} \\ \text{LX34 (m)} &= -\text{CDS} \end{aligned}$$

Calculating Gate Capacitance

The following input file example shows a gate capacitance calculation in detail for a BSIM model. TOX is chosen so that: $\frac{e_{ox}}{tox} = 1e-3 F/m^2$

In this example, Vfb0, phi, and k1 are chosen so that vth=1v. The AC sweep is chosen so that the last point is: $2 \cdot \pi \cdot freq = 1e6 s^{-1}$

This section covers the following topics:

- [Gate Capacitance — Input File](#)
- [Gate Capacitance — Calculations](#)

- Gate Capacitance — Results
 - Gate Capacitance — Plotting Gate Capacitances
 - Gate Capacitance — Control Options
 - Gate Capacitance — Scaling
-

Gate Capacitance — Input File

This example is based on demonstration netlist `calcap.sp`, which is available in directory `$installdir/demo/hspice/mos`:

```
$  
m d g 0 b nch l=0.8u w=100u ad=200e-12 as=200e-12  
vd d 0 5  
vg g 0 5 ac 1  
vb b 0 0  
.ac dec 1 1.59155e4 1.59155e5  
.print CGG=lx18(m) CDD=lx33(m) CGD=par('-lx19(m)')  
+ CDG=par('-lx32(m)')  
.print ig_imag=ii2(m) id_imag=ii1(m)  
.model nch nmos level=13 update=2  
+ xqc=0.6 toxm=345.315 vfb0=-1 phi0=1 k1=1.0 muz=600  
+ mus=650 acm=2  
+ xl=0 ld=0.1u meto=0.1u cj=0.5e-4 mj=0 cjsw=0  
.alter  
vd d 0 5 ac 1  
vg g 0 5  
.end
```

Gate Capacitance — Calculations

$$L_{eff} = 0.6u$$

$$\frac{eox}{tox} = 1e - 3F/m^2$$

$$Cap = \frac{L_{eff} \cdot W_{eff} \cdot eox}{tox} = 60e - 15F$$

BSIM equations for internal capacitance in saturation with $xqc=0.4$:

$$body = 1 + 0.5 \cdot \left(1 - \frac{1}{(1.744 + 0.8364 \cdot (PHI0 + vsb)))} \right) \cdot \frac{K1}{\sqrt{(PHI0 + vsb)}}$$

Chapter 3: MOSFET Capacitance Models

Calculating Gate Capacitance

$$1 + 0.5 \cdot \left(1 - \frac{1}{(1.744 + 0.8364)}\right) = 1.3062$$

$$cgg = Cap \cdot \left(1 - \frac{1}{(3 \cdot body)}\right) = Cap \cdot 0.7448 = 44.69F$$

$$cgd = 0$$

$$cdg = \left(\frac{4}{15}\right) \cdot Cap = 16F$$

$$cdd = 0$$

$$\text{Gate-drain overlap} = (ld + meto) \cdot Weff \cdot \frac{eox}{tox} = 20e - 15F$$

Adding the overlaps:

$$cgg = 44.69F + 2 \cdot 20F = 84.69F$$

$$cgd = 20F$$

$$cdg = 36F$$

$$cdd = 20F$$

$$\text{Drain-bulk diode cap} = cj \cdot ad = (0.5e - 4) \cdot (200e - 12) = 10F$$

Adding the diodes:

$$cgg = 84.69F$$

$$cgd = 20F$$

$$cdg = 36F$$

$$cdd = 30F$$

Gate Capacitance — Results

```
subckt
element 0:m
model 0:nch
cdtot 30.0000f
cgtot 84.6886f
cstot 65.9999f
cbtot 43.4213f
cgs 61.2673f
cgd 20.0000f
```

The calculation and simulation results match.

Gate Capacitance — Plotting Gate Capacitances

The following input file shows how to plot gate capacitances as a function of bias. Set .OPTION DCCAP to turn on capacitance calculations for a DC sweep. The model used is the same as for the previous gate capacitance calculations.

The following example is based on demonstration netlist *gatecap.sp*, which is available in directory *\$installdir/demo/hspice/mos*:

```
$ gate capacitance plots
.option dccap=1 post
m d g 0 b nch l=0.8u w=100u ad=200e-12 as=200e-12
vd d 0 0
vg g 0 5
vb b 0 0
.dc vd 0 5 .1
.print vds=v(d) CGG=lx18(m)
+ CGD=par('-lx19(m)') CDG=par('-lx32(m)')
+ CGS=par('-lx20(m)') CSG=par('lx18(m)+lx21(m)+lx32(m)')
+ CGB=par('lx18(m)+lx19(m)+lx20(m)') CBG=par('-lx21(m)')
.model nch nmos
+ level=13 update=2 xqc=0.6 toxm=345.315
+ vfb0=-1 phi0=1 k1=1.0 muz=600 mus=650
+ acm=2 xl=0 ld=0.1u meto=0.1u
+
.end
```

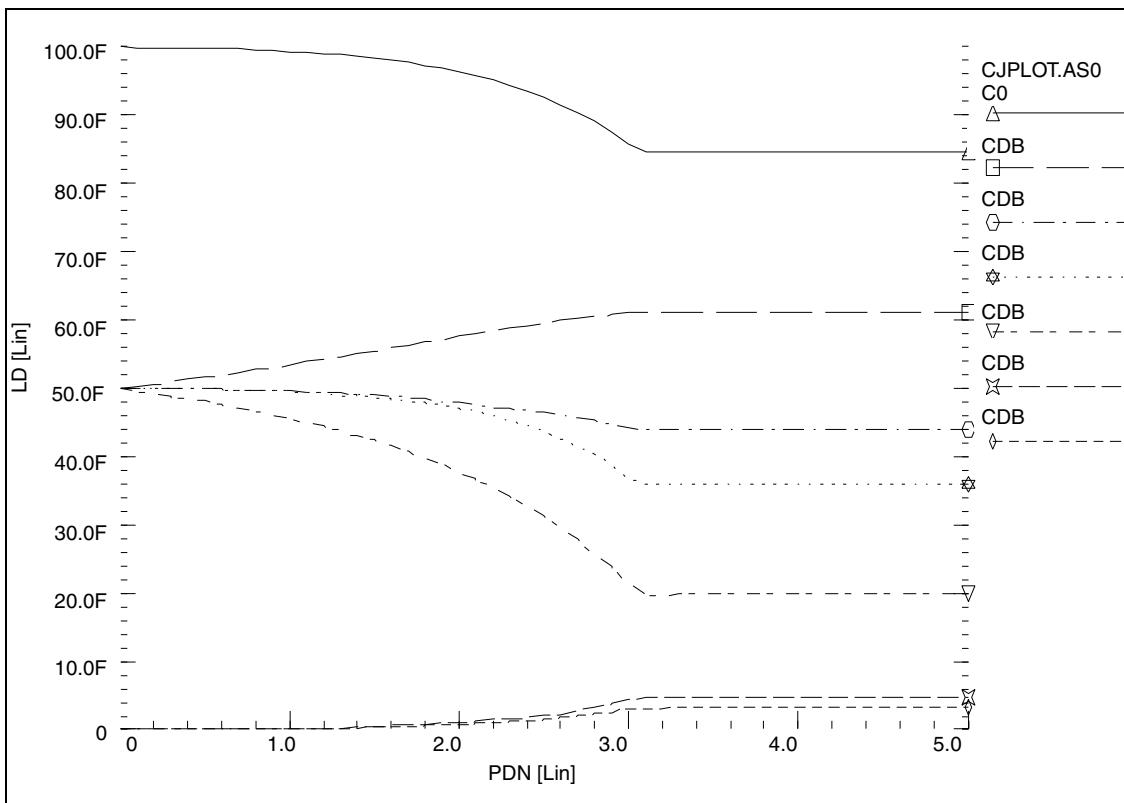


Figure 19 Gate Capacitance

Gate Capacitance — Control Options

The SCALM, CVTOL, DCSTEP, and DCCAP control options affect the CAPOP models.

- SCALM scales the model parameters (ignored in Levels 49 and higher).
- CVTOL controls the error tolerance for convergence for the CAPOP=3 model (see [CAPOP=3 — Gate Capacitances \(Simpson Integration\)](#)).
- DCSTEP models capacitances with a conductance during DC analysis.
- DCCAP calculates capacitances in DC analysis.

Gate Capacitance — Scaling

.OPTION SCALM scales the CGBO, CGDO, CGSO, COX, LD, and WD parameters according to fixed rules, which are a function of the parameter's units. If the model parameter's units are in meters, simulation multiplies the parameter by SCALM. For example:

- The LD parameter uses units in meters; to obtain its scaled value, simulation multiplies the value of LD by SCALM.
- If the units are in meters squared, simulation multiplies the parameter by SCALM².
- If the units are in reciprocal meters, the parameter's value is divided by SCALM. For example, because CGBO is in farads/meter, the value of CGBO is divided by SCALM.
- If the units are in reciprocal meters squared, then the parameter is divided by SCALM².

For the scaling equations specific to each CAPOP level, see the individual CAPOP subsections.

MOSFET Gate Capacitance — Model Parameters

This section covers the following topics:

- [Gate Capacitance — Basic Parameters](#)
- [Gate Capacitance — Gate Overlap Capacitance Parameters](#)
- [Gate Capacitance — Meyer Capacitance Parameters CAPOP=0, 1, 2](#)
- [Gate Capacitance — Charge Conservation Parameters \(CAPOP=4\)](#)

Gate Capacitance — Basic Parameters

| Name (Alias) | Units | Default | Description |
|--------------|------------------|----------|--|
| CAPOP | - | 2.0 | Capacitance model selector. |
| COX (CO) | F/m ² | 3.453e-4 | Oxide capacitance. If you do not specify COX, simulation calculates it from TOX. The default corresponds to the TOX default of 1e-7: $COX_{scaled} = COX/SCALM^2$ |

Chapter 3: MOSFET Capacitance Models

MOSFET Gate Capacitance — Model Parameters

| Name (Alias) | Units | Default | Description |
|--------------|-------|---------|--|
| TOX | m | 1e-7 | Oxide thickness, calculated from COX (if you specify COX). The program uses the default if you do not specify COX. For TOX>1, simulation assumes that the unit is Angstroms. A level-dependent default can override it. See specific MOSFET levels in this manual. |

Gate Capacitance — Gate Overlap Capacitance Parameters

| Name (Alias) | Units | Default | Description |
|-----------------|-------|---------|---|
| CGBO (CGB) | F/m | 0.0 | Gate-bulk overlap capacitance per meter channel length. If you set WD and TOX, but you do not set CGBO, then simulation calculates CGBO. CGBOscaled = CGBO/SCALM |
| CGDO (CGD, C2) | F/m | 0.0 | Gate-drain overlap capacitance per meter channel width. If you set LD or METO and TOX, but you do not set CGDO, then simulation calculates CGDO. CGDOscaled = CGDO/SCALM |
| CGSO (CGS, C1) | F/m | 0.0 | Gate-source overlap capacitance per meter channel width. If you set LD or METO and TOX, but you do not set CGSO, then simulation calculates CGSO. CGSOscaled = CGSO/SCALM |
| LD (LATD, DLAT) | m | | Lateral diffusion into channel from source and drain diffusion. <ul style="list-style-type: none"> ■ If you do not specify either LD or XJ, then the LD default=0.0. ■ If you specify XJ but you do not specify LD, then simulation calculates LD from XJ. ■ LD default=0.75 · XJ for all levels except LEVEL 4 for which LD default=0.75. LDscaled = LD · SCALM LEVEL 4: LDscaled = LD · XJ · SCALM |
| METO | m | 0.0 | Fringing field factor for gate-to-source and gate-to-drain overlap capacitance calculation. METOscaled = METO · SCALM |
| WD | m | 0.0 | Lateral diffusion into channel from bulk along width. WDScaled = WD · SCALM |

Gate Capacitance — Meyer Capacitance Parameters CAPOP=0, 1, 2

| Name (Alias) | Units | Default | Description |
|--------------|-------|---------|---|
| CF1 | V | 0.0 | Modified MEYER control for transition of cgs from depletion to weak inversion for CGSO (for CAPOP=2 only) |

| Name (Alias) | Units | Default | Description |
|--------------|-------|---------|---|
| CF2 | V | 0.1 | Modified MEYER control for transition of cgs from weak to strong inversion region (for CAPOP=2 only) |
| CF3 | | 1.0 | Modified MEYER control for the cgs and cgd transition from the saturation region to the linear region as a function of vds (for CAPOP=2 only) |
| CF4 | | 50.0 | Modified MEYER control for the contour of the cgb and cgs smoothing factors |
| CF5 | | 0.667 | Modified MEYER control for the capacitance multiplier for cgs in the saturation region |
| CF6 | | 500.0 | Modified MEYER control for contour of cgd smoothing factor |
| CGBEX | | 0.5 | cgb exponent (for CAPOP=1 only) |

Gate Capacitance — Charge Conservation Parameters (CAPOP=4)

| Name (Alias) | Units | Default | Description |
|--------------|-------|---------|---|
| XQC | | 0.5 | Coefficient of channel charge share attributed to drain; its range is 0.0 to 0.5. This parameter applies only to CAPOP=4 and some of its level-dependent aliases. |

Specifying XQC and XPART for CAPOP=4, 9, 11, 12, 13

Parameter rules for the gate capacitance charge sharing coefficient (XQC & XPART) in the saturation region:

- If you do not specify either XPART or XQC, then simulation uses the 0/100 model.
- If you specify both XPART and XQC, then XPART overrides XQC.
- If you specify XPART, but you do not specify XQC, then:
 - XPART=0 → 40/60
 - XPART=0 . 4 → 40/60
 - XPART=0 . 5 → 50/50
 - XPART=1 → 0/100

Chapter 3: MOSFET Capacitance Models

Overlap Capacitance Equations

- $\text{XPART} = \text{any other value less than } 1 \rightarrow 40/60$
- $\text{XPART} > 1 \rightarrow 0/100$ If XQC is specified:
 - If you specify XQC but you do not specify XPART , then:
 - $\text{XQC}=0 \rightarrow 0/100$
 - $\text{XQC}=0.4 \rightarrow 40/60$
 - $\text{XQC}=0.5 \rightarrow 50/50$
 - $\text{XQC}=1 \rightarrow 0/100$
 - $\text{XQC} = \text{any other value less than } 1 \rightarrow 40/60$
 - $\text{XQC}>1 \rightarrow 0/100$

The only difference is the treatment of the 0 parameter value.

After you specify XPART/XQC , the gate capacitance ramps from 50/50 at $V_{ds}=0$ volt (linear region) to the value (with V_{ds} sweep) in the saturation region in XPART/XQC . Ramping the charge-sharing coefficient ensures smooth gate capacitance characteristics.

Overlap Capacitance Equations

The overlap capacitors are common to all models. You can input them explicitly or the program can calculate them. Either way, these overlap capacitors must be added into the respective voltage-variable capacitors before integration, and before the DC operating point reports the combined parallel capacitance.

Gate-to-Bulk Overlap Capacitance

If you specify CGBO , then: $\text{CGBO}_{eff} = M \cdot L_{eff} \cdot \text{CGBO}_{scaled}$

Otherwise: $\text{CGBO}_{eff} = 2 \cdot W_{scaled} \cdot L_{eff} \cdot COX_{scaled} \cdot M$

Gate-to-Source Overlap Capacitance

If you specify CGSO , then: $\text{CGSO}_{eff} = W_{eff} \cdot \text{CGSO}_{scaled}$

Otherwise: $\text{CGSO}_{eff} = W_{eff} \cdot (L_{scaled} + METO_{scaled}) \cdot COX_{scaled}$

Gate-to-Drain Overlap Capacitance

If you specify CGDO , then: $\text{CGDO}_{eff} = W_{eff} \cdot \text{CGDO}_{scaled}$

Otherwise: $\text{CGDO}_{eff} = W_{eff} \cdot (L_{scaled} + METO_{scaled}) \cdot COX_{scaled}$

Simulation calculates the L_{eff} value for each model differently, and saves this value in the corresponding model section. The W_{eff} calculation is not the same as the W_{eff} value in the LEVEL 1, 2, 3, 6, 7 and 13 models.

$$Weff = M \cdot (Wscaled \cdot WMLT + XWscaled)$$

The $2 \cdot WD_{scaled}$ factor is not subtracted.

CAPOP=0 — SPICE Meyer Gate Capacitances

Definition: $cap = COXscaled \cdot Weff \cdot Leff$

This section covers the following topics:

- Gate-Bulk Capacitance (cgb)
- Gate-Source Capacitance (cgs)
- Gate-Drain Capacitance (cgd)

Gate-Bulk Capacitance (cgb)

Accumulation, $vgs \leq vth-PH1$: $cgb = cap$

Depletion, $vgs < vth$: $cgb = cap \cdot \frac{vth - vgs}{PH1}$

Strong Inversion, $vgs \geq vth$: $cgb = 0$

Gate-Source Capacitance (cgs)

Accumulation: $vgs \leq vth - \frac{PHI}{2}$

$$cgs = 0$$

Depletion, $vgs \leq vth$: $cgs = CF5 \cdot cap + \frac{cap \cdot (vgs - cth)}{0.75 \cdot PHI}$

Strong Inversion Saturation Region: $vgs > vth$ and $vds \geq vdsat$

$$cgs = CF5 \cdot cap$$

Strong Inversion Linear Region: $vgs > vth$ and $vds < vdsat$

$$cgs = CF5 \cdot cap \cdot \left\{ 1 - \left[\frac{vdsat - vds}{2 \cdot (vdsat + vsb) - vds - vsb} \right]^2 \right\}$$

Gate-Drain Capacitance (cgd)

The gate-drain capacitance has value only in the linear region.

Strong Inversion Linear Region: $vgs > vth$ and $vds < vdsat$

$$cgd = CF5 \cdot cap \cdot \left\{ 1 - \left[\frac{vdsat + vsb}{2 \cdot (vdsat + vsb) - vds - vsb} \right]^2 \right\}$$

The following example is based on demonstration netlist capop0.sp, which is available in directory `$installdir/demo/hspice/mos`:

```
*file capop0.sp--capop=0 capacitances
*
*this file is used to create spice meyer gate c-v plots
**
*(capop=0) for low vds and high vds
*
.options acct=2 post=2 dccap=1 nomod
.dc vgl -1 4 .01
.print dc cgb_vdsp05=par('-lx21(m1)') cgd_vdsp05=par('-lx19(m1)')
+ cgs_vdsp05=par('-lx20(m1)')
.print dc cgb_vdsp8=par('-lx21(m2)') cgd_vdsp8=par('-lx19(m2)')
+ cgs_vdsp8=par('-lx20(m2)')
*****
m1 d1 g1 0 0 mn l=5e-6 w=20e-6 $ create capacitances for vds=0.05
m2 d2 g1 0 0 mn l=5e-6 w=20e-6 $ create capacitances for vds=0.80
*****
vd1 d1 0 dc 0.05
vd2 d2 0 dc 0.80
vg1 g1 0 dc 0.0
*
*****
.model mn nmos ( level = 2
+ vto = 1.0 gamma = 1.40 nsub = 7.20e15
+ uo = 817 ucrit = 3.04e4 phi=.6
+ uexp = 0.102 neff = 1.74 vmax = 4.59e5
+ tox = 9.77e-8 cj = 0 cjsw = 0 js = 0
+ capop=0 )
.end
```

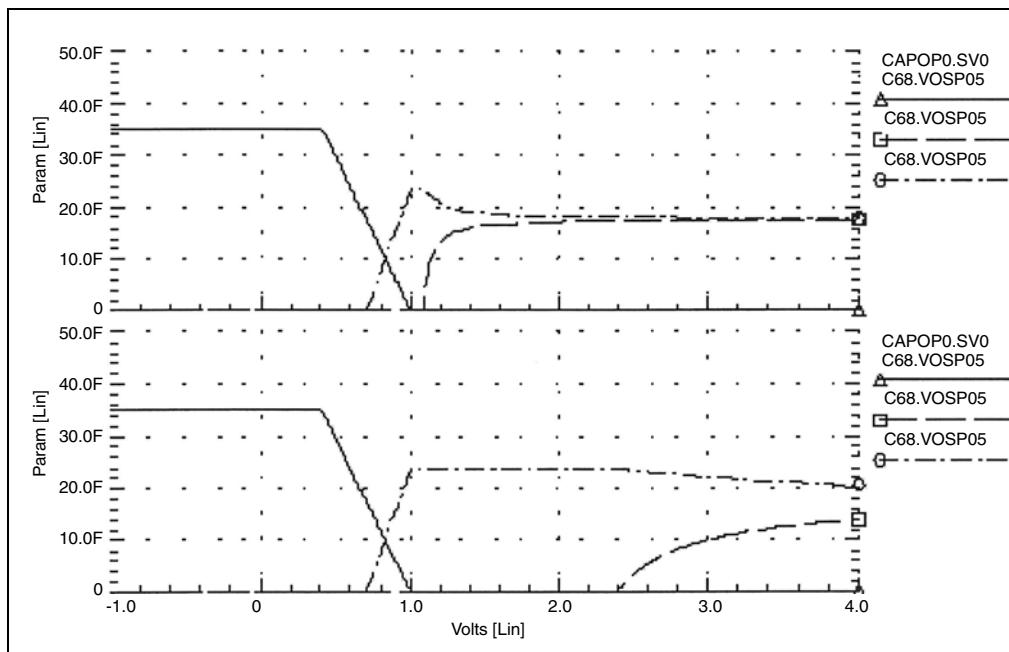


Figure 20 CAPOP=0 Capacitances

CAPOP=1 — Modified Meyer Gate Capacitances

Define: $cap = COXscaled \cdot Weff \cdot Leff$

In the following equations, G^- , G^+ , D^- , and D^+ are smooth factors. You cannot change the values of these parameters.

This section covers the following topics:

- Gate-to-Bulk Overlap Capacitance
- Gate-to-Source Overlap Capacitance
- Gate-to-Drain Overlap Capacitance

Gate-Bulk Capacitance (cgb)

Accumulation, $vgs \leq vfb - vsb$

$$cgb = cap$$

Depletion, $vgs \leq vth$

$$cgb = \frac{cap}{\left[1 + 4 \cdot \frac{vgs + vsb - vfb}{GAMMA^2} \right]^{CGBEX}}$$

Strong Inversion, $vgs > vth$

$$cgb = \frac{G^+ \cdot cap}{\left[1 + 4 \cdot \frac{GAMMA \cdot (vsb + PHI)^2 + vsb + PHI}{GAMMA^2} \right]^{CGBEX}}$$

These equations replace GAMMA with effective γ for model levels higher than 4.

Gate-Source Capacitance (cgs)

Low vds ($vds < 0.1$)

Accumulation, $vgs \leq vth$ $cgs = CF5 \cdot cap \cdot G^- \cdot D^-$

Weak Inversion, $vgs < vth + 0.1$

$$cgs = CF5 \cdot cap \cdot \left\{ \frac{vgs - vth}{0.1} \cdot \left[1 - \left(\frac{0.1 - vds}{0.2 - vds} \right)^2 - D^- \right] + D^- \right\}$$

Strong Inversion, $vgs \geq vth + 0.1$

$$cgs = CF5 \cdot cap \cdot \left\{ 1 - \left[\frac{vgs - vth - vds}{2 \cdot (vgs - vth) - vds} \right]^2 \right\}$$

High vds ($vds \geq 0.1$)

Accumulation, $vgs \leq vth$ $cgs = CF5 \cdot cap \cdot G^-$

Saturation Region, $vgs < vth + vds$ $cgs = CF5 \cdot cap$

Linear Region, $vgs \geq vth + vds$

$$cgs = CF5 \cdot cap \cdot \left\{ 1 - \left[\frac{vgs - vth - vds}{2 \cdot (vgs - vth) - vds} \right]^2 \right\}$$

Gate-Drain Capacitance (cgd)

Low vds ($vds < 0.1$)

Accumulation, $vgs \leq vth$ $cgd = CF5 \cdot cap \cdot G^- \cdot D^+$

Weak Inversion, $vgs < vth + 0.1$

$$cgd = CF5 \cdot cap \cdot \left\{ D^+ + \frac{vgs - vgh}{0.1} \cdot \max \left[0, 1 - \left(\frac{0.1}{0.2 - vds} \right)^2 - D^+ \right] \right\}$$

Strong Inversion, $vgs \geq vth + 0.1$

$$cgd = CF5 \cdot cap \cdot \max \left\{ D^+, 1 - \left[\frac{vgs - vth}{2 \cdot (vgs - vth) - vds} \right]^2 \right\}$$

High vds (vds < 0.1)

Accumulation, $vgs \leq vth$: $cgd = CF5 \cdot cap \cdot G^- \cdot D^+$

Saturation Region, $vgs < vth + vds$: $cgd = CF5 \cdot cap \cdot D^+$

Strong Inversion, $vgs \geq vth + vds$:

$$cgd = CF5 \cdot cap \cdot \max \left\{ D^+, 1 - \left[\frac{vgs - vth}{2 \cdot (vgs - vth) - vds} \right]^2 \right\}$$

The following example is based on demonstration netlist `capop1.sp`, which is available in directory `$installdir/demo/hspice/mos`:

```
*file capop1.sp---capop1 capacitances
*
*this file creates the modified meyer gate c-v plots
*(capop=1) for low vds and high vds.
*
.options acct=2 post=2 dccap=1 nomod
.dc vg1 -1 4 .01
.print dc cgb_vdsp05=par('-lx21(m1)') cgd_vdsp05=par('-
lx19(m1)')
+cgs_vdsp05=par('-lx20(m1)')
.print dc cgb_vdsp8=par('-lx21(m2)') cgd_vdsp8=par('-lx19(m2)')
+cgs_vdsp8=par('-lx20(m2)')
*****
m1 d1 g1 0 0 mn l=5e-6 w=20e-6 $creates capacitances for vds=0.05
m2 d2 g1 0 0 mn l=5e-6 w=20e-6 $creates capacitances for vds=0.80
*****
vd1 d1 0 dc 0.05
vd2 d2 0 dc 0.80
vg1 g1 0 dc 0.0
*
*****
.model mn nmos ( level = 2
+ vto = 1.0 gamma = 1.40 nsub = 7.20e15
```

Chapter 3: MOSFET Capacitance Models

CAPOP=2—Parameterized Modified Meyer Capacitance

```
+ tox = 9.77e-8 uo = 817 ucrit = 3.04e4
+ uexp = 0.102 neff = 1.74 vmax = 4.59e5
+ phi = 0.6 cj = 0 cjsw = 0 js = 0
+ capop=1 )
.end
```

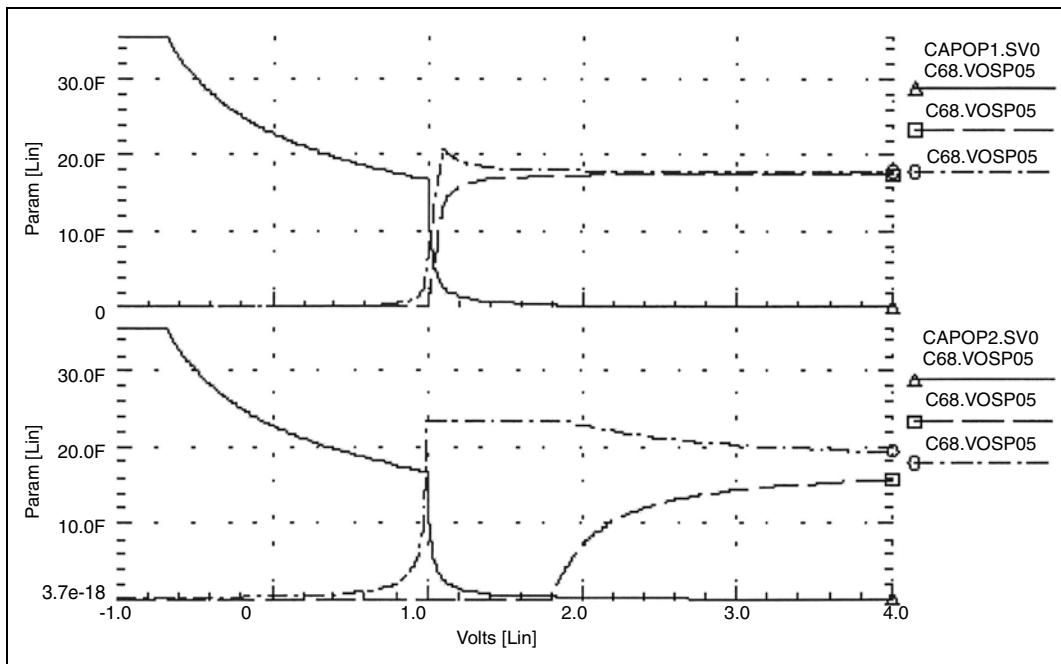


Figure 21 CAPOP=1 Capacitances

CAPOP=2—Parameterized Modified Meyer Capacitance

The CAPOP=2 Meyer capacitance model is the more general form of Meyer capacitance. The CAPOP=1 Meyer capacitance model is the special case of CAPOP=2 if CF1=0, CF2=0.1, and CF3=1.

In the following equations, G^- , G^+ , D^- , and D^+ are smooth factors. You cannot change the values of these parameters.

Definition: $cap = COXscaled \cdot Weff \cdot Leff$

This section covers the following topics:

- Gate-Bulk Capacitance (cgb)
- Gate-Source Capacitance (cgs)
- Gate-Drain Capacitance (cgd)

Gate-Bulk Capacitance (cgb)

Accumulation, $vgs \leq vfb - vsb$: $cgb = cap$

$$\text{Depletion, } vgs \leq vth: cgb = \frac{cap}{\left(1 + 4 \cdot \frac{vgs + vsb - vfb}{GAMMA^2}\right)^{1/2}}$$

Inversion, $vgs > vth$:

$$cgb = \frac{G^+ \cdot cap}{\left[1 + 4 \cdot \frac{GAMMA \cdot (PHI + vsb)^{1/2} + PHI + vsb}{GAMMA^2}\right]^{1/2}}$$

These equations replace GAMMA with effective γ for model levels higher than 4.

Gate-Source Capacitance (cgs)

Low vds ($vds < 0.1$)

Accumulation, $vgs < vth - CF1$: $cgs = CF5 \cdot cap \cdot G^- \cdot D^-$

Depletion, $vgs \leq vth + CF2 - CF1$:

$$cgs = CF5 \cdot cap \cdot \left\{ \frac{vgs - vth + CF1}{CF2} \cdot \left[1 - \left(CF2 - \frac{vds}{2 \cdot (CF2 - vds)} \right)^2 - D^- \right] + D^- \right\}$$

Strong Inversion, $vgs > vth + \max(CF2 - CF1, CF3 \cdot vds)$, UPDATE=0

Strong Inversion, $vgs > vth + CF2 - CF1$, UPDATE=1:

$$cgs = CF5 \cdot cap \cdot \left\{ 1 - \left[\frac{vgs - vth + CF1 - vds}{2 \cdot (vgs - vth + CF1) - vds} \right]^2 \right\}$$

High vds

$$(vds \geq 0.1)$$

Accumulation, $vgs < vth - CF1$: $cgs = CF5 \cdot cap \cdot G^- \cdot D^+$, $CF1 \neq 0$

$$cgs = CF5 \cdot cap \cdot G^-, CF1 = 0$$

Chapter 3: MOSFET Capacitance Models

CAPOP=2—Parameterized Modified Meyer Capacitance

Weak Inversion, $vgs < vth + CF2 - CF1$, $CF1 \neq 0$:

$$cgs = CF5 \cdot cap \cdot \max\left(\frac{vgs - vth + CF1}{CF2}, D^+\right)$$

Saturation Region, $vgs < vth + CF3 \cdot vds$: $cgs = CF5 \cdot cap$

Linear Region, $vgs > vth + CF3 \cdot vds$:

$$cgs = CF5 \cdot cap \cdot \left\{ 1 - \left[\frac{vgs - vth - vds}{2 \cdot (vgs - vth) - vds} \right]^2 \right\}, \text{ UPDATE}=0, CF1=0$$

$$cgs = CG5 \cdot cap \cdot \left\{ 1 - \left[\frac{vgs - vth - CF3 \Rightarrow vds}{2 \cdot (vgs - vth) - CF3 \Rightarrow vds} \right]^2 \right\}, \text{ UPDATE}=1$$

Gate-Drain Capacitance (cgd)

Low vds, ($vds < 0.1$)

Accumulation, $vgs \leq vth - CF1$: $cgd = CF5 \cdot cap \cdot G^- \cdot D^-$

Weak Inversion, $vgs < vth + CF2 - CF1$:

$$cgd = CF5 \cdot cap \cdot \left\{ D^- + \frac{vgs - vth + CF1}{CF2} \cdot \max\left[0, 1 - \left(\frac{CF2}{2 \cdot CF2 - vds} \right)^2 - D^- \right] \right\}$$

Strong Inversion, $vgs \geq vth + CF2 - CF1$:

$$cgd = CF5 \cdot cap \cdot \max\left\{ D^-, 1 - \left[\frac{vgs - vth + CF1}{2 \cdot (vgs - vth + CF1) - vds} \right]^2 \right\}$$

High vds ($vds > 0.1$)

Accumulation, $vgs \leq vth - CF1$: $cgd = CF5 \cdot cap \cdot G^- \cdot DD^+$

Saturation Region, $vgs \leq vth + CF3 \cdot vds$: $cgd = CF5 \cdot cap \cdot DD^+$

DD^+ is a function of $CF3$, if $\text{UPDATE}=1$.

Linear Region, $vgs > vth + CF3 \cdot vds$:

$$cgd = CF5 \cdot cap \cdot \max\left\{ DD^+, 1 - \left[\frac{vgs - vth}{2 \cdot (vgs - vth) - CF3 \Rightarrow vds} \right]^2 \right\}$$

The following example is based on demonstration netlist capop2.sp, which is available in directory `$installdir/demo/hspice/mos`:

```
*file capop2.sp capop=2 capacitances
*
*this file creates parameterized modified gate capacitances
*(capop=2) for low and high vds.
*
.options acct=2 post=2 dccap=1 nomod
.dc vg1 -1 4 .01
.print dc cgb_vdsp05=par('-lx21(m1)') cgd_vdsp05=par('-
lx19(m1)')
+ cgs_vdsp05=par('-lx20(m1)')
.print dc cgb_vdsp8=par('-lx21(m2)') cgd_vdsp8=par('-
lx19(m2)')
+ cgs_vdsp8=par('-lx20(m2)')
*****
m1 d1 g1 0 0 mn l=5e-6 w=20e-6 $creates capacitances for vds=0.05
m2 d2 g2 0 0 mn l=5e-6 w=20e-6 $creates capacitances for vds=0.80
*****
vd1 d1 0 dc 0.05
vd2 d2 0 dc 0.80
vg1 g1 0 dc 0.0
*
*****
.model mn nmos ( level = 2
+ vto = 1.0 gamma = 1.40 nsub = 7.20e15
+ tox = 9.77e-8 uo = 817 ucrit = 3.04e4
+ uexp = 0.102 neff = 1.74 phi = 0.6
+ vmax = 4.59e5 cj = 0 cjsw = 0 js = 0
+ capop=2 cf1=0.15 cf2=.2 cf3=.8 cf5=.666)
.end
```

Chapter 3: MOSFET Capacitance Models

CAPOP=3 — Gate Capacitances (Simpson Integration)

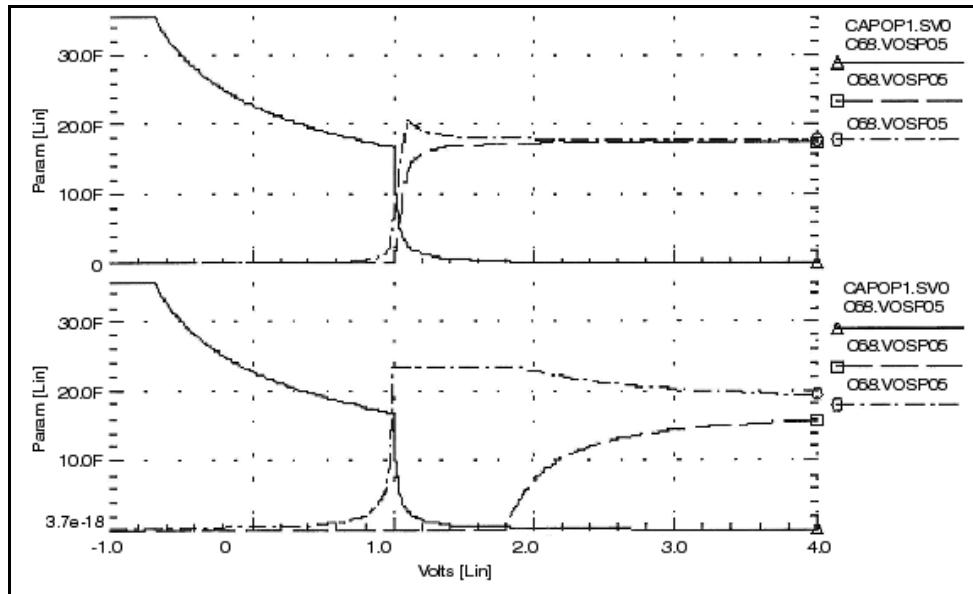


Figure 22 CAPOP=2 Capacitances

CAPOP=3 — Gate Capacitances (Simpson Integration)

The CAPOP=3 model uses the same set of equations and parameters as the CAPOP=2 model. Simulation obtains the charges using Simpson numeric integration instead of the box integration found in the CAPOP=1, 2, and 6 models.

Gate capacitances are not constant values with respect to voltages. The incremental capacitance best describes the capacitance values:

$$C(v) = \frac{dq(v)}{dv}$$

In the preceding equation, $q(v)$ is the charge on the capacitor, and v is the voltage across the capacitor.

The formula for calculating the differential is difficult to derive. Furthermore, the voltage is required as the accumulated capacitance over time. The timewise formula is:

$$i(t) = \frac{dq(v)}{dt} = C(v) \cdot \frac{dv(t)}{dt}$$

The charge is: $q(v) = \int_0^v C(v)dv$

To calculate the current: $i(t) = \frac{dq(v)}{dt} = \left(\frac{d}{dt}\right) \int_0^v C(v)dv$

For small intervals: $I(n+1) = \frac{dq(v)}{dt} = \frac{1}{t(n+1) - t(n)} \int_{V(n)}^{V(n+1)} C(v)dv$

In SPICE, the following equation approximates the integral:

$$I(n+1) = \left(\frac{V(n+1) - V(n)}{t(n+1) - t(n)} \right) \cdot \left(\frac{C[V(n+1)] + C[V(n)]}{2} \right)$$

This last formula is the trapezoidal rule for integration over two points. The charge is approximated as the average capacitance times the change in voltage. If the capacitance is nonlinear, this approximation can be in error. To accurately estimate the charge, use Simpson's numerical integration rule. This method provides charge conservation control.

To use this model parameter:

- Set the CAPOP model parameter to 3 and use the existing CAPOP=2 model parameters.
- Modify the .OPTION RELV (relative voltage tolerance), .OPTION RELMOS (relative current tolerance for MOSFETs), and .OPTION CVTOL (capacitor voltage tolerance) settings.

The default of 0.5 is a good nominal value for CVTOL. The CVTOL option uses the following equation to set the number of integration steps:

$$n = \frac{|V(n+1) - V(n)|}{CVTOL}$$

Use a large value for CVTOL to decrease the number of integration steps for the n to n+1 time interval; this yields slightly less accurate integration results. Using a small CVTOL value increases the computational load, sometimes severely.

CAPOP=4 — Charge Conservation Capacitance Model

The charge conservation method (See “A Charge-Oriented Model for MOS Transistor,” Ward, Donald E. and Robert W. Dutton) is not implemented correctly into the SPICE2G.6 program. There are errors in the derivative of charges, especially in LEVEL 3 models. Also, the channel charge partition is not continuous from the linear region to the saturation region.

In the Synopsys MOSFET device models, these problems are corrected. If you specify the CAPOP=4 model parameter, then simulation uses the level-dependent recommended charge conservation model. The XQC model parameter selects ratio of channel charge partitioning between drain/source.

For example, if you set XQC=.4, then in the saturation region, 40% of the channel charge is associated with the drain and the remaining 60% is associated with the source. In the linear region, the ratio is 50/50. Simulation uses an empirical equation to make a smooth transition from 50/50 (linear region) to 40/60 (saturation region).

The capacitance coefficients are the derivative of gate, bulk, drain, and source charges, and are continuous. LEVEL 2, 3, 4, 6, 7, and 13 models include a charge-conservation capacitance model. To invoke this model, set CAPOP=4.

The following example compares only the CAPOP=4 charge conservation capacitance and the CAPOP=9 improved charge conservation capacitance for the LEVEL 3 model. The CGS and CGD capacitances for CAPOP=4 model (SPICE2G.6) show discontinuity at the boundary between the saturation and linear regions. The CAPOP=9 model does not have discontinuity. The modified Meyer capacitances (CAPOP=2) are also provided for comparison. The shape of CGS and CGD capacitances resulting from CAPOP=9 are much closer to those of CAPOP=2.

Example 1:

This example is based on demonstration netlist mcap3.sp, which is available in directory \$installdir/demo/hspice/mos:

Chapter 3: MOSFET Capacitance Models
CAPOP=4 — Charge Conservation Capacitance Model

```
FILE MCAP3.SP CHARGE CONSERVATION MOSFET CAPS., CAPOP=4,9 LEVEL=3
* CGGB = LX18(M) DERIVATIVE OF QG WITH RESPECT TO VGB.
* CGDB = LX19(M) DERIVATIVE OF QG WITH RESPECT TO VDB.
* CGSB = LX20(M) DERIVATIVE OF QG WITH RESPECT TO VSB.
* CBGB = LX21(M) DERIVATIVE OF QB WITH RESPECT TO VGB.
* CBDB = LX22(M) DERIVATIVE OF QB WITH RESPECT TO VDB.
* CBSB = LX23(M) DERIVATIVE OF QB WITH RESPECT TO VSB.
* CDGB = LX32(M) DERIVATIVE OF QD WITH RESPECT TO VGB.
* CDDB = LX33(M) DERIVATIVE OF QD WITH RESPECT TO VDB.
* CDSB = LX34(M) DERIVATIVE OF QD WITH RESPECT TO VSB.
* SIX NONRECIPROCAL CAPACITANCES (CGB,CBG,CGS,CSG,CGD,AND CDG)
* ARE DERIVED FROM THE ABOVE CAPACITANCE FACTORS.
.OPTION DCCAP=1 POST NOMOD
.PARAM XQC=0.4 CAPOP=4
.DC VGG -2 5 .02
.print CGB=PAR('LX18(M)+LX19(M)+LX20(M)')
+ CBG=PAR('-LX21(M)')
+ CGS=PAR('-LX20(M)')
+ CSG=PAR('LX18(M)+LX21(M)+LX32(M)')
+ CGD=PAR('-LX19(M)')
+ CDG=PAR('-LX32(M)')
.print
+ CG =par('LX14(M)')
VDD D 0 2.5
VGG G 0 0
VBB B 0 -1
M D G 0 B MOS W=10U L=5U
.MODEL MOS NMOS LEVEL=3 COX=1E-4 VTO=.3 CAPOP=CAPOP
+ UO=1000 GAMMA=.5 PHI=.5 XQC=XQC
+ THETA=0.06 VMAX=1.9E5 ETA=0.3 DELTA=0.05 KAPPA=0.5 XJ=.3U
+ CGSO=0 CGDO=0 CGBO=0 CJ=0 JS=0 IS=0
*
.ALTER
.PARAM CAPOP=9
.END
```

Chapter 3: MOSFET Capacitance Models

CAPOP=4 — Charge Conservation Capacitance Model

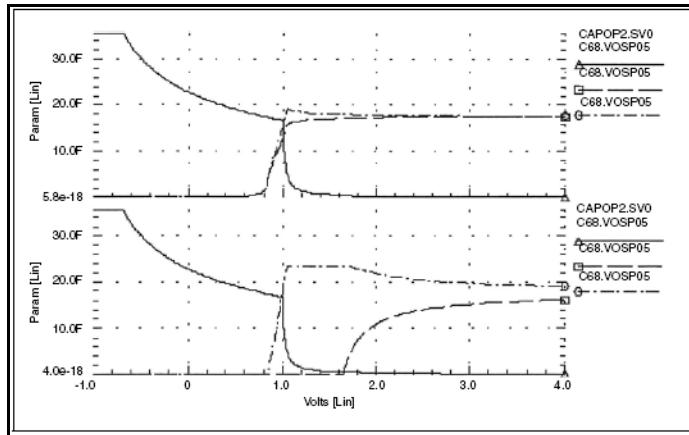


Figure 23 CAPOP=4, 9 Capacitances for LEVEL 3 Model

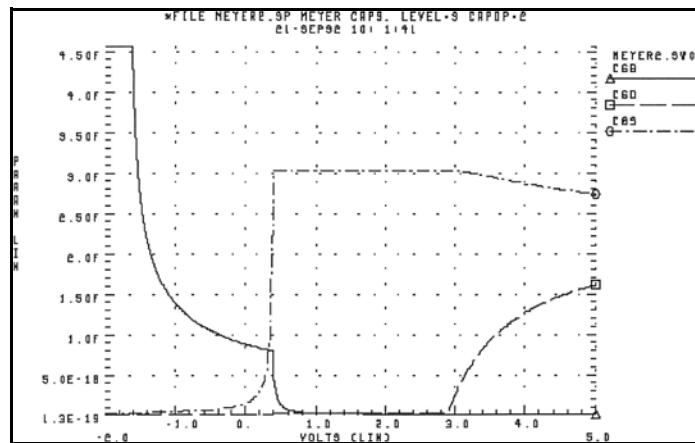


Figure 24 CAPOP=2 Capacitances for LEVEL 3 Model

The example below tests the charge conservation capacitance model (Yang, P., B.D. Epler, and P.K. Chaterjee ‘An Investigation of the Charge Conservation Problem’) and compares the Meyer and charge conservation models. As the graph in [Figure 26](#) shows, the charge conservation model returns more accurate results.

Example 2:

This example is based on demonstration netlist chrgpump.sp, which is available in directory `$installdir/demo/hspice/mos`:

```

chrgpump.sp: charge conservation test for charge pump circuit
*test circuit of a mosfet capacitor and a linear capacitor
.options post acct list nomod $ method=gear
+ reltol=1e-3 abstol=1e-6 chgtol=1e-14 $ delmax=0.1ns
.param capop=2
.op
.tran 2ns 470ns sweep capop poi 2 2,9
.ic v(s)=1
*
vin g 0 pulse 0 5 15ns 5ns 5ns 50ns 100ns
vbb 0 b pulse 0 5 0ns 5ns 5ns 50ns 100ns
vdd d d- pulse 0 5 25ns 5ns 5ns 50ns 100ns
*
rc d- s 10k
c2 s 0 10p
m1 d g s b mm w=3.5u l=5.5u
+ad=100p as=100p pd=50u ps=50u nrd=1 nrs=1
*
.model mm nmos level=3 vto=0.7 kp=50e-6 gamma=0.96
+phi=0.5763 tox=50e-9 nsub=1.0e16 ld=0.5e-6
+vmax=268139 theta=0.05 eta=1 kappa=0.5 cj=1e-4
+cjsw=0.05e-9 rsh=20 js=1e-8 pb=0.7
+cgd=0 cgs=0 is=0 js=0
+capop=capop
*
.probe tran vout=v(s)
.probe tran vd=v(d) vg=v(g) vb=v(b)
.print tran v(s) v(d) v(g) v(b)
.end

```

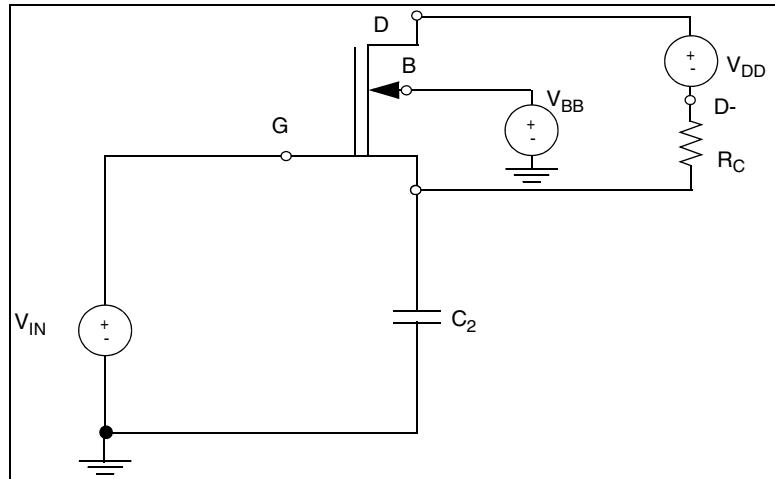


Figure 25 Charge Pump Circuit

Chapter 3: MOSFET Capacitance Models

CAPOP=4 — Charge Conservation Capacitance Model

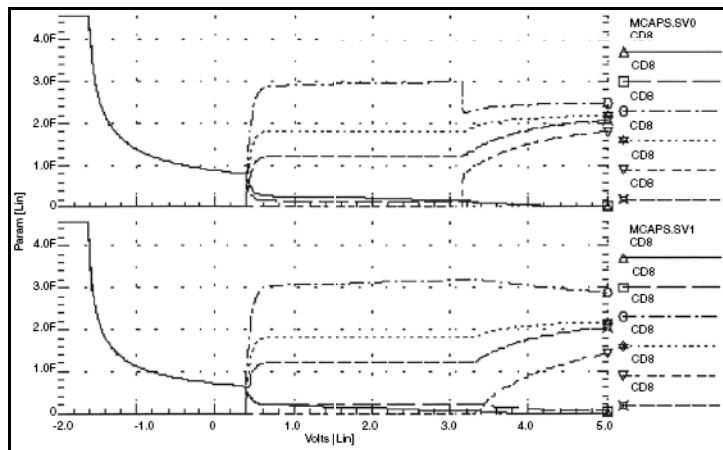


Figure 26 Charge Conservation Test: CAPOP=2 or 9

The following example applies a pulse through a constant capacitance to the gate of a MOS transistor. Ideally, if the model conserves charge, then the voltage at node 20 should become zero when the input pulse becomes zero. Consequently, the model that provides voltage closer to zero for node 20 conserves the charge better. The results of the CAPOP=4 model are better than the CAPOP=2 model.

This example compares charge conservation models in SPICE2G.6 and Synopsys device models. The results indicate that the Synopsys device models are more accurate.

Example 3:

This example is based on demonstration netlist mcap2_a.sp, which is available in directory `$installdir/demo/hspice/mos`:

```

FILE MCAP2_A.SP
.OPTION SPICE NOMOD DELMAX=.25N POST=2
.PARAM CAPOP=4
.TRAN 1NS 40NS SWEEP CAPOP POI 2 4 2
.PRINT TRAN V(1) V(20)
VIN 1 0 PULSE (0V, 5V, 0NS, 5NS, 5NS, 5NS, 20NS)
CIN 1 20 1PF
RLEAK 20 0 1E+12
VDD 10 0 1.3
VBB 30 0 -1
M 10 20 0 30 MOS W=10U L=5U
.MODEL MOS NMOS LEVEL=2 TOX=250E-10 VTO=.3
+ UO=1000 LAMBDA=1E-3 GAMMA=.5 PHI=.5 XQC=.5
+ THETA=0.067 VMAX=1.956E5 XJ=.3U
+ CGSO=0 CGDO=0 CGBO=0
+ CJ=0 JS=0 IS=0
+ CAPOP=CAPOP
.END

```

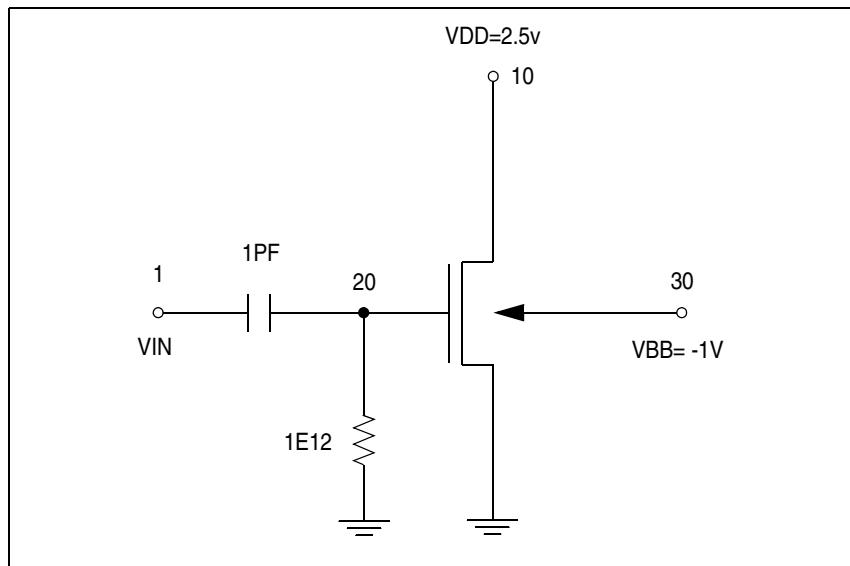


Figure 27 Charge Conservation Test Circuit

CAPOP=5 — No Gate Capacitance

If CAPOP=5 for no capacitors, then simulation does not calculate gate capacitance.

CAPOP=6 — AMI Gate Capacitance Model

Define: $vgst = vgs - \frac{(vth + vfb)}{2}$, $cox = \frac{\epsilon_{ox}}{TOX \cdot 1e-10} \cdot Weff \cdot Leff$

The following equations calculate the cgs gate capacitance in the different regions.

0.5 · (vth + vfb) > vgs

$$cgs = 0$$

0.5 · (vth + vfb) < vgs < vth

$$\text{For } vgst < vds: cgs = \frac{4}{3} \cdot \frac{cox \cdot vgst}{vth - vfb}$$

$$\text{For } vgst > vds: cgs = arg \cdot \frac{4}{3} \cdot \frac{cox \cdot vgst}{vth - vfb}$$

vgs > vth

$$\text{For } vgst < vds: cgs = \frac{2}{3} \cdot cox$$

$$\text{For } vgst > vds: cgs = arg \cdot \frac{2}{3} \cdot cox, arg = vgst \cdot \frac{(3 \cdot vgst - 2 \Rightarrow vds)}{(2 \cdot vgst - vds)^2}$$

The following equations calculate the cgd gate capacitance in the different regions.

vgs < vth

$$cgd = 0$$

vgs > vth and vgst < vds

$$cgd = 0$$

vgs > vth and vgst > vds

$$cgd = arg \cdot \frac{2}{3} \cdot cox, arg = (3 \cdot vgst - vds) \cdot \frac{(vgst - vds)}{(2 \cdot vgst - vds)^2}$$

The following equation combines the cgb gate capacitance with the calculation of both oxide capacitance and depletion capacitance:

$$cgb = \frac{cgbx \cdot cd}{cgbx + cd}$$

Simulation calculates the oxide capacitance (cgbx) as:

$$cgbx = cox - cgs - cgd$$

Depletion capacitance (cd) is voltage-dependent:

$$cd = \frac{\epsilon si}{wd} \cdot Weff \cdot Leff, wd = \left(\frac{2 \cdot \epsilon si \cdot vc}{q \cdot NSUB} \right)^{1/2}$$

vc = The effective voltage from channel to substrate (bulk)

The following equations show vc under various conditions:

vgs + vsb < vfb

$$vc = 0$$

vgs + vsb > vfb

$$vc = vgs + vsb - vfb$$

vgst > 0, vgs < vth, vgst < vds

$$vc = \frac{1}{2} \cdot (vth - vfb) + \frac{3}{2} \cdot vgst + vsb$$

vgst > 0, vgs < vth, vgst > vds

$$vc = \frac{1}{2} \cdot (vth - vfb) + vgst + \frac{1}{2} \cdot vds + vsb$$

vgs > vth, vgst < vds

$$vc = vth - vfb + \frac{1}{2} \cdot vgst + vsb$$

vgs > vth, vgst > vds

$$vc = vth - vfb + \frac{1}{2} \cdot vds + vsb$$

CAPOP=13 — BSIM1-based Charge-Conserving Gate Capacitance Model

See [LEVEL 13: BSIM Model](#).

CAPOP=39 — BSIM2 Charge-Conserving Gate Capacitance Model

See [LEVEL 13: BSIM Model](#).

Calculating Effective Length and Width for AC Gate Capacitance

For some MOS processes and parameter extraction method, AC analysis might need different L_{eff} and W_{eff} values than for DC analysis. For AC gate capacitance calculations, substitute the LDAC and WDAC model parameters for LD and WD in the L_{eff} and W_{eff} calculations. You can use LD and WD in L_{eff} and W_{eff} calculations for DC current.

To use LDAC and WDAC, enter XL, LD, LDAC, XW, WD, and WDAC in the .MODEL statement. The model uses the following equations for DC current calculations.

$$Leff = L + XL - 2 \cdot LD$$

$$Weff = W + XW - 2 \cdot WD$$

The model parameters also use the following equations to calculate the AC gate capacitance:

$$Leff = L + XL - 2 \cdot LDAC$$

$$Weff = W + XW - 2 \cdot WDAC$$

The noise calculations use the DC W_{eff} and L_{eff} values.

Use LDAC and WDAC with the standard XL, LD, XW, and WD parameters. Do not use LDAC and WDAC with other parameters, such as DL0 and DW0.

MOSFET Diode Models

This chapter discusses use of available MOSFET diode models.

HSPICE ships hundreds of examples for your use; see [Listing of Demonstration Input Files](#) for paths to demo files.

This section covers the following topics:

- [Selecting MOSFET Diode Models](#)
- [Enhancing Convergence](#)
- [MOSFET Diode Model Parameters](#)
- [Using an ACM=0 MOS Diode](#)
- [Using an ACM=1 MOS Diode](#)
- [Using an ACM=2 MOS Diode](#)
- [Using an ACM=3 MOS Diode](#)
- [MOS Diode Equations](#)

Selecting MOSFET Diode Models

You can use the Area Calculation Method (ACM) parameter to precisely control bulk-to-source and bulk-to-drain diodes within MOSFET models. Use the ACM model parameter to select one of three different modeling schemes for the MOSFET bulk diodes. This section discusses the model parameters and model equations used for the different MOSFET diode models.

To select a MOSFET diode model, set the ACM parameter within the MOSFET model statements.

Chapter 4: MOSFET Diode Models

Enhancing Convergence

- If `ACM=0`, the pn bulk junctions of the MOSFET are modeled in the SPICE style.
- The `ACM=1` diode model is the original ASPEC model.
- The `ACM=2` model parameter specifies the improved diode model, which is based on a model similar to the ASPEC MOSFET diode model.
- The `ACM=3` diode model is a further improvement that deals with capacitances of shared sources and drains, and gate edge source/drain-to-bulk periphery capacitance.
- If you do not set the `ACM` model parameter, the diode model defaults to the `ACM=0` model.
- If `ACM=0` and `ACM=1` models, you cannot specify `HDIF`. In the `ACM=0` model, you cannot specify `LDIF`. The `ACM=1` model does not use the `AD`, `AS`, `PD`, and `PS` geometric element parameters.

Enhancing Convergence

- The `GMIN` option creates a parallel conductance across the bulk diodes and drain-source for transient analysis.
- The `GMINDC` option creates a parallel conductance across the bulk diodes and drain-source for DC analysis.

These options enhance the convergence properties of the diode model, especially when the model has a high off resistance. Use the `RSH`, `RS`, and `RD` parameters to prevent over-driving the diode in either a DC or transient forward bias condition. These parameters also enhance the convergence properties of the diode model.

MOSFET Diode Model Parameters

This section covers the following topics:

- [MOSFET Diode Model — DC Parameters](#)
- [MOSFET Diode Model — Capacitance Parameters](#)
- [MOSFET Diode Model — Drain and Source Resistance Parameters](#)
- [MOSFET Diode Model — MOS Geometry Parameters](#)

MOSFET Diode Model — DC Parameters

| Name (Alias) | Units | Default | Description |
|--------------|--------------------|---------|--|
| ACM | | 0 | Area calculation method |
| JS | amp/m ² | | Bulk junction saturation current: JSscaled=JS/SCALM2 – for ACM=1 unit is amp/m and JSscaled=JS/SCALM. |
| JSW | amp/m | 0 | Sidewall bulk junction saturation current: JSWscaled=JSW/SCALM. |
| IS | amp | 1e-14 | Bulk junction saturation current. For the ASPEC=1 option, default=0. |
| N | | 1 | Emission coefficient. |
| NDS | | 1 | Reverse bias slope coefficient. |
| VNDS | V | -1 | Reverse diode current transition point. |

MOSFET Diode Model — Capacitance Parameters

| Name (Alias) | Units | Default | Description |
|--------------------|------------------|------------------------------|---|
| CBD | F | 0 | Zero bias bulk-drain junction capacitance. Used only when CJ and CJSW are 0. |
| CBS | F | 0 | Zero bias bulk-source junction capacitance. Use only when CJ and CJSW are 0. |
| CJ (CDB, CSB, CJA) | F/m ² | 579.11 µF/ m ² | Zero-bias bulk junction capacitance: <ul style="list-style-type: none"> ■ CJscaled = CJ/SCALM2 —for ACM=1 the unit is F/m. ■ CJscaled = CJ/SCALM. Default for the ASPEC=0 option is: $CJ = \left(\frac{\epsilon si \cdot q \cdot NSUB}{2 \cdot PB} \right)^{1/2}$ |
| CJGATE | F/m | CSJW | Zero-bias gate-edge sidewall bulk junction capacitance (ACM=3 only). CJGATEScaled=CJGATE/SCALM <ul style="list-style-type: none"> ■ Default = CJSW for Hspice releases later than H9007D. ■ Default = 0 for HSPICE releases H9007D and earlier, or if you do not specify CJSW. |
| CJSW (CJP) | F/m | 0 | Zero-bias sidewall bulk junction capacitance. CJSWscaled = CJSW/SCALM. Default = 0. |

Chapter 4: MOSFET Diode Models

MOSFET Diode Model Parameters

| Name (Alias) | Units | Default | Description |
|-------------------------|-------------------|---------|--|
| FC | | 0.5 | Forward-bias depletion capacitance coefficient (not used). |
| MJ (EXA, EXJ, EXS, EXD) | | 0.5 | Bulk junction grading coefficient. |
| MJSW (EXP) | | 0.33 | Bulk sidewall junction grading coefficient. |
| NSUB (DNB, NB) | 1/cm ³ | 1.0e15 | Substrate doping. |
| PB (PHA, PHS, PHD) | V | 0.8 | Bulk junction contact potential. |
| PHP | V | PB | Bulk sidewall junction contact potential. |
| TT | s | 0 | Transit time |

MOSFET Diode Model — Drain and Source Resistance Parameters

| Name (Alias) | Units | Default | Description |
|--------------|--------------------|---------|--|
| LRD | ohm/m | 0 | Drain resistance length sensitivity. Use this parameter with automatic model selection, WRD, and PRD to factor a model for the device size. |
| LRS | ohm/m | 0 | Source resistance length sensitivity. Use this parameter with automatic model selection, WRS, and PRS to factor a model for the device size. |
| PRD | ohm/m ² | 0 | Drain resistance product (area) sensitivity (used with LRD). |
| PRS | ohm/m ² | 0 | Source resistance product (area) sensitivity (used with LRS). |
| RD | ohm/sq | 0.0 | Drain ohmic resistance. This parameter is usually the sheet resistance of a lightly-doped region for $ACM \geq 1$. |
| RDC | ohm | 0.0 | Additional drain resistance due to contact resistance. |
| RS | ohm/sq | 0.0 | Source ohmic resistance. This parameter is usually the sheet resistance of a lightly-doped region for $ACM \geq 1$. |
| RSC | ohm | 0.0 | Source resistance due to contact resistance. |
| RSH (RL) | ohm/sq | 0.0 | Drain and source diffusion sheet resistance. |
| WRD | ohm/m | 0 | Drain resistance width sensitivity (used with LRD). |

| Name (Alias) | Units | Default | Description |
|--------------|-------|---------|--|
| WRS | ohm/m | 0 | Source resistance width sensitivity (used with LRS). |

MOSFET Diode Model — MOS Geometry Parameters

| Name (Alias) | Units | Default | Description |
|----------------|-------|---------|---|
| HDIF | m | 0 | Length of heavily-doped diffusion, from contact to lightly-doped region (ACM=2, 3 only): $HDIF_{scaled} = HDIF \cdot SCALM$ |
| LD (DLAT,LATD) | m | | Lateral diffusion into the channel from the source and drain diffusion. <ul style="list-style-type: none"> ■ If you do not specify LD and XJ, LD default=0.0. ■ If you specify LD, but you do not specify XJ, then simulation calculates LD from XJ. Default=0.75 · XJ. ■ For LEVEL 4 only, lateral diffusion is derived from LD · XJ. $LD_{scaled} = LD \cdot SCALM$ |
| LDIF | m | 0 | Length of lightly-doped diffusion adjacent to the gate (ACM=1, 2): $LDIF_{scaled} = LDIF \cdot SCALM$ |
| WMLT | | 1 | Width diffusion layer shrink reduction factor. |
| XJ | m | 0 | Metallurgical junction depth: $XJ_{scaled} = XJ \cdot SCALM$ |
| XW (WDEL, DW) | m | 0 | Accounts for masking and etching effects: $XW_{scaled} = XW \cdot SCALM$ |

Using an ACM=0 MOS Diode

Figure 28 shows the parameter value settings for a MOSFET diode, designed with a MOSFET that has a channel length of 3 μm and a channel width of 10 μm .

Chapter 4: MOSFET Diode Models

Using an ACM=0 MOS Diode

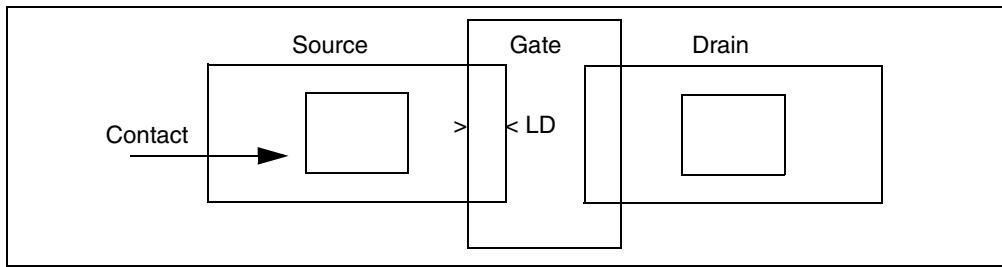


Figure 28 ACM=0 MOS Diode

For example, a transistor might include:

$$LD = .5 \text{ mm} \quad W = 1.0 \text{ mm} \quad L = 3 \text{ mm}$$

| Parameter | Description |
|-----------|--|
| AD | area of drain (about 80 pm^2) |
| AS | area of source (about 80 pm^2) |
| CJ | $4e-4 \text{ F/m}^2$ |
| CJSW | $1e-10 \text{ F/m}$ |
| JS | $1e-8 \text{ A/m}^2$ |
| JSW | $1e-13 \text{ A/m}$ |
| NRD | number of squares for drain resistance |
| NRS | number of squares for source resistance |
| PD | sidewall of drain (about $36 \mu\text{m}$) |
| PS | sidewall of source (about $36 \mu\text{m}$) |

This section covers the following topics:

- [Calculating Effective Areas and Peripheries](#)
- [Calculating Effective Saturation Current](#)
- [Calculating Effective Drain and Source Resistances](#)

Calculating Effective Areas and Peripheries

For ACM=0, simulation calculates the effective areas and peripheries as follows:

$$AD_{eff} = M \cdot AD \cdot WMLT^2 \cdot SCALE^2$$

$$AS_{eff} = M \cdot AS \cdot WMLT^2 \cdot SCALE^2$$

$$PD_{eff} = M \cdot PD \cdot WMLT \cdot SCALE$$

$$PS_{eff} = M \cdot PS \cdot WMLT \cdot SCALE$$

Calculating Effective Saturation Current

For ACM=0, simulation calculates the MOS diode effective saturation currents as follows:

Source Diode Saturation Current

Define: $val = JSscaled \cdot AS_{eff} + JSWscaled \cdot PS_{eff}$

If $val > 0$, then $isbs = val$

Otherwise, $isbd = M \cdot IS$

Drain Diode Saturation Current

Define: $val = JSscaled \cdot AD_{eff} + JSWscaled \cdot PD_{eff}$

If $val > 0$, then $isbd = val$

Otherwise, $isbd = M \cdot IS$

Calculating Effective Drain and Source Resistances

For ACM=0, simulation calculates the effective drain and source resistances as follows:

Source Resistance

Define: $val = NRS \cdot RSH$

If $val > 0$, then $RS_{eff} = \frac{val + RSC}{M}$

Chapter 4: MOSFET Diode Models

Using an ACM=1 MOS Diode

$$\text{Otherwise, } RSeff = \frac{RS + RSC}{M}$$

Drain Resistance

Define: $val = NRD \cdot RSH$

$$\text{If } val > 0, \text{ then } RDeff = \frac{val + RDC}{M}$$

$$\text{Otherwise, } RDeff = \frac{RD + RDC}{M}$$

Using an ACM=1 MOS Diode

If you specify the ACM=1 model parameter, simulation uses ASPEC-style diodes, and does not use the AD, PD, AS, and PS parameters. The JS and CJ units differ from SPICE-style diodes (ACM=0).

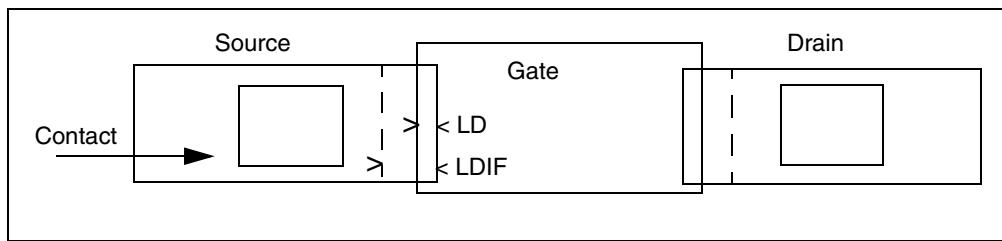


Figure 29 ACM=1 MOS Diode

Example:

The following table lists parameter value settings for a transistor with the following parameter values:

- LD=0.5 μm
- W=10 μm

- L=3 μm
- LDIF=0.5 μm

| Parameter | Description |
|-----------|---|
| CJ | 1e-10 F/m of gate width Note the change from F/m ² (in ACM=0) to F/m. |
| CJSW | 2e-10 F/m of gate width |
| JS | 1e-14 A/m of gate width Note the change from A/m ² (in ACM=0) to A/m |
| JSW | 1e-13 A/m of gate width |
| NRD | number of squares for drain resistance |
| NRS | number of squares for source resistance |

This section covers the following topics:

- [Calculating Effective Areas and Peripheries](#)
- [Calculating Effective Saturation Current](#)
- [Calculating Effective Drain and Source Resistances](#)

Calculating Effective Areas and Peripheries

For ACM=1, simulation calculates the effective areas and peripheries as follows:

$$A_{Deff} = W_{eff} \cdot WMLT$$

$$A_{Seff} = W_{eff} \cdot WMLT$$

$$P_{Dff} = W_{eff}$$

$$P_{Sff} = W_{eff}$$

The following equation calculates the W_{eff} value used in the preceding equations:

$$W_{eff} = M \cdot (W_{scaled} \cdot WMLT + XW_{scaled})$$

Chapter 4: MOSFET Diode Models

Using an ACM=1 MOS Diode

Note: The W_{eff} value is not the same as the w_{eff} value in the LEVEL 1, 2, 3, 6, and 13 models. The $2 \cdot WD_{scaled}$ term is not subtracted.

Calculating Effective Saturation Current

For ACM=1, the MOS diode effective saturation currents are calculated as follows:

Source Diode Saturation Current

Define: $val = JS_{scaled} \cdot A_{Seff} + JSW_{scaled} \cdot P_{Seff}$

If $val > 0$, then $isbs = val$

Otherwise, $isbs = M \cdot IS$

Drain Diode Saturation Current

Define: $val = JS_{scaled} \cdot A_{Deff} + JSW_{scaled} \cdot P_{Deff}$

If $val > 0$, then $isbd = val$

Otherwise, $isbd = M \cdot IS$

Calculating Effective Drain and Source Resistances

For ACM=1, simulation calculates the effective drain and source resistances as follows.

Source Resistance

For UPDATE=0:

$$RS_{eff} = \frac{LD_{scaled} + LDIF_{scaled}}{Weff} \cdot RS + \frac{NRS \cdot RSH + RSC}{M}$$

If UPDATE ≥ 1 , LDIF=0, and you specify the ASPEC option, then:

$$RS_{eff} = \frac{1}{M} \cdot (RS + NRS \cdot RSH + RSC)$$

Drain Resistance

For UPDATE=0:

$$RDeff = \frac{LDscaled + LDIFscaled}{Weff} \cdot RD + \frac{NRD \cdot RSH + RDC}{M}$$

If UPDATE ≥ 1 , LDIF=0, and you specify the ASPEC option, then:

$$RDeff = \frac{1}{M} \cdot (RD + NRD \cdot RSH + RDC)$$

See [LEVEL 6: Lattin-Jenkins-Grove \(ASPEC\) Model on page 100](#) and [LEVEL 7: Lattin-Jenkins-Grove \(SPICE\) Model on page 128](#) for more possibilities.

Using an ACM=2 MOS Diode

If you set the ACM=2 model parameter, simulation uses HSPICE-style MOS diodes. You can use a fold-back calculation scheme similar to the ASPEC method, retaining full model-parameter compatibility with the SPICE procedure. This method also supports both lightly-doped and heavily-doped diffusions (the LD, LDIF, and HDIF parameters set the diffusion type). This model preserves the JS, JSW, CJ, and CJSW units (used in SPICE) for full compatibility.

ACM=2 automatically generates more-reasonable diode parameter values than those for ACM=1. You can generate the ACM=2 geometry in either of two ways:

- AD, AS, PD, and PS element parameters in the element statement generate parasitics. These parameters do not have default option values.
- To suppress the diode, set IS=0, AD=0, and AS=0.

If you set AS=0 in the element and IS=0 in the model, simulation suppresses the source diode. Use this setting for shared contacts.

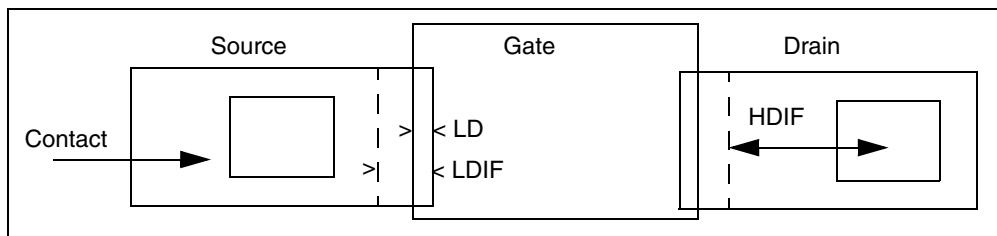


Figure 30 ACM=2 MOS Diode

Chapter 4: MOSFET Diode Models

Using an ACM=2 MOS Diode

Example

For a transistor with $LD=0.07\mu m$, $W=10\mu m$, $L=2\mu m$, $LDIF=1\mu m$, and $HDIF=4\mu m$. [Table 8](#) shows typical MOSFET diode parameter values.

Table 8 ACM=2 MOS Diode Parameters

| Parameter | Description |
|-----------|--|
| AD | Area of drain. Default option value for AD is not applicable. |
| AS | Area of source. Default option value for AS is not applicable. |
| CJ | $1e-4 F/m^2$ |
| CJSW | $1e-10 F/m$ |
| JS | $1e-4 A/m^2$ |
| JSW | $1e-10 A/m$ |
| HDIF | Length of heavily-doped diffusion contact-to-gate (about $2\mu m$). $HDIF_{eff}=HDIF \cdot WMLT \cdot SCALM$ |
| LDIF+LD | Length of lightly-doped diffusion (about $0.4\mu m$). |
| NRD | Number of squares drain resistance. Default value for NRD does not apply. |
| NRS | Number of squares source resistance. Default for NRS does not apply. |
| PD | Periphery of drain, including gate width for ACM=2. No default. |
| PS | Periphery of source, including gate width for ACM=2. No default. |
| RD | Resistance (ohm/square) of lightly-doped drain diffusion (about 2000). |
| RS | Resistance (ohm/square) of lightly-doped source diffusion (about 2000). |
| RSH | Diffusion sheet resistance (about 35). |

Calculating Effective Areas and Peripheries

For ACM=2, simulation calculates the effective areas and peripheries as follows:

- If you do not specify `AD`, then $A_{Deff} = 2 \cdot HDIF_{eff} \cdot W_{eff}$
Otherwise, $A_{Deff} = M \cdot AD \cdot WMLT^2 \cdot SCALE^2$
- If you do not specify `AS`, then $A_{Seff} = 2 \cdot HDIF_{scaled} \cdot W_{eff}$
Otherwise, $A_{Seff} = M \cdot AS \cdot WMLT^2 \cdot SCALE^2$
- If you do not specify `PD`, then $P_{Deff} = M \cdot (4 \cdot HDIF_{eff} + 2 \cdot W_{eff})$
Otherwise, $P_{Deff} = M \cdot PD \cdot WMLT \cdot SCALE$
- If you do not specify `PS`, then $P_{Seff} = M \cdot (4 \cdot HDIF_{eff} + 2 \cdot W_{eff})$
Otherwise, $P_{Seff} = M \cdot PS \cdot WMLT \cdot SCALE$

The following equations calculate values used in the preceding equation:

$$W_{eff} = W_{scaled} \cdot WMLT + XW_{scaled}$$

$$HDIF_{eff} = HDIF_{scaled}$$

$$HDIF_{scaled} = HDIF \cdot SCALM \cdot WMLT$$

The W_{eff} value is not the same as the W_{eff} value in the LEVEL 1, 2, 3, and 6 models. The $2 \cdot WD_{scaled}$ term is not subtracted.

Calculating Effective Saturation Currents

For ACM=2, simulation calculates the MOS diode effective saturation currents as follows.

Source Diode Saturation Current

Define: $val = JS_{scaled} \cdot A_{Seff} + JSW_{scaled} \cdot P_{Seff}$

If $val > 0$, then $isbs = val$

Otherwise, $isbs = M \cdot IS$

Drain Diode Saturation Current

Define: $val = JS_{scaled} \cdot A_{Deff} + JSW_{scaled} \cdot P_{Deff}$

If $val > 0$, then $isbd = val$

Otherwise, $isbd = M \cdot IS$

Calculating Effective Drain and Source Resistances

For ACM=2, simulation calculates the effective drain and source resistances as follows.

Source Resistance

If you specify NRS, then:

$$RSeff = \frac{LDscaled + LDIFscaled}{Weff} \cdot RS + \left(\frac{NRS \cdot RSH + RSC}{M} \right)$$

Otherwise:

$$RSeff = \frac{RSC}{M} + \frac{HDIFeff \cdot RSH + (LDscaled + LDIFscaled) \cdot RS}{Weff}$$

Drain Resistance

If you specify NRD, then:

$$RDeff = \frac{LDscaled + LDIFscaled}{Weff} \cdot RD + \left(\frac{NRD \cdot RSH + RDC}{M} \right)$$

Otherwise:

$$RDeff = \frac{RDC}{M} + \frac{HDIFeff \cdot RSH + (LDscaled + LDIFscaled) \cdot RD}{Weff}$$

Using an ACM=3 MOS Diode

Use ACM=3 to properly model MOS diodes of stacked devices. You can also use the CJGATE parameter to model the drain and source periphery capacitances separately, along the gate edge. Therefore, the PD and PS calculations do not include the gate periphery length. CJGATE defaults to the CJSW value, which in turn defaults to 0.

The AD, AS, PD, and PS calculations depend on the device layout as determined by the value of the GEO element parameter. You can specify the following GEO values in the MOS element description:

- GEO=0: other devices do not share the drain and source of the device (default).
- GEO=1: another device shares the drain.

- GEO=2: another device shares the source.
- GEO=3: another device shares the drain and source.

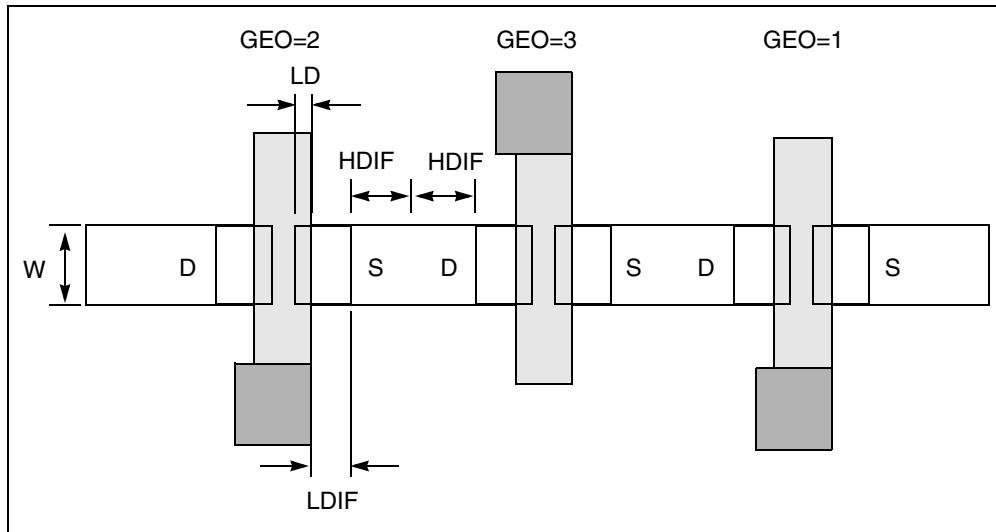


Figure 31 Stacked Devices and Corresponding GEO Values

Calculating Effective Areas and Peripheries

ACM=3 calculates the effective areas and peripheries based on the GEO value.

- If you do not specify AD, then:
 - For GEO=0 or 2, $AD_{eff} = 2 \cdot HDIF_{eff} \cdot Weff$
 - For GEO=1 or 3, $AD_{eff} = HDIF_{eff} \cdot Weff$
 - Otherwise, $AD_{eff} = M \cdot AD \cdot WMLT^2 \cdot SCALE^2$
- If you do not specify AS, then:
 - For GEO=0 or 1, $AS_{eff} = 2 \cdot HDIF_{eff} \cdot Weff$
 - For GEO=2 or 3, $AS_{eff} = HDIF_{eff} \cdot Weff$
 - Otherwise, $AS_{eff} = M \cdot AS \cdot WMLT^2 \cdot SCALE^2$
- If you do not specify PD, then:
 - For GEO=0 or 2, $PD_{eff} = 4 \cdot HDIF_{eff} + Weff$

Chapter 4: MOSFET Diode Models

MOS Diode Equations

- For $GEO=1$ or 3 , $PDeff = 2 \cdot HDIFeff$
- Otherwise, $PDeff = M \cdot PD \cdot WMLT \cdot SCALE$
- If you do not specify PS , then:
 - For $GEO=0$ or 1 , $PSeff = 4 \cdot HDIFeff + Weff$
 - For $GEO=2$ or 3 , $PSeff = 4 \cdot HDIFeff$
 - Otherwise, $PSeff = M \cdot PS \cdot WMLT \cdot SCALE$

Simulation calculates $Weff$ and $HDIF_{eff}$ as follows:

$$Weff = M \cdot (W_{scaled} \cdot WMLT + XW_{scaled})$$

$$HDIF_{eff} = HDIF_{scaled} \cdot WMLT$$

Note: The $Weff$ value is not the same as the $Weff$ value in the LEVEL 1, 2, 3, and 6 models. The $2 \cdot WD_{scaled}$ term is not subtracted.

Effective Saturation Current Calculations

The $ACM=3$ model calculates the MOS diode effective saturation currents the same as $ACM=2$.

Effective Drain and Source Resistances

The $ACM=3$ model calculates the effective drain and source resistances the same as $ACM=2$.

MOS Diode Equations

This section describes MOS diode equations.

DC Current

- Simulation parallels the drain and source MOS diodes with GMINDC conductance in the DC analysis.
- Simulation parallels the drain and source MOS diodes with GMIN conductance in the transient analysis.

The total DC current is the sum of the diode current and the conductance current. The diode current is calculated as follows.

Drain and Source Diodes Forward Biased

- $v_{bs} > 0$: $i_{bs} = i_{sbs} \cdot (e^{v_{bs}/(N \cdot v_t)} - 1)$
- $v_{bd} > 0$: $i_{bd} = i_{sbd} \cdot (e^{v_{bd}/(N \cdot v_t)} - 1)$

Drain and Source Diodes Reverse Biased

- For $0 > v_{bs} > VNDS$: $i_{bs} = g_{sbs} \cdot v_{bs}$
- For $v_{bs} < VNDS$: $i_{bs} = g_{sbs} \cdot VNDS + \left(\frac{g_{sbs}}{NDS}\right) \cdot (v_{bs} - VNDS)$
- For $0 > v_{bd} > VNDS$: $i_{bd} = g_{sbd} \cdot v_{bd}$
- For $v_{bd} < VNDS$: $i_{bd} = g_{sbd} \cdot VNDS + \left(\frac{g_{sbd}}{NDS}\right) \cdot (v_{bd} - VNDS)$

The following equations calculate values used in the preceding equations:

$$|g_{sbs}| = |i_{sbs}| \text{ and } |g_{sbd}| = |i_{sbd}|$$

Using MOS Diode Capacitance Equations

Each MOS diode capacitance is the sum of diffusion and depletion capacitance. Simulation evaluates the diffusion capacitance in terms of the small signal conductance of the diode and a TT model parameter, representing the transit time of the diode. The depletion capacitance depends on which ACM you choose.

To calculate bias-dependent depletion capacitance, define C0BS, C0BD, C0BS_SW, and C0BD_SW intermediate quantities. These depend on geometric parameters, such as AS_{eff} and PS_{eff}, calculated under various ACM specifications.

Chapter 4: MOSFET Diode Models

MOS Diode Equations

For $ACM=3$, the $C0BS_SW$ and $C0BD_SW$ intermediate quantities include an extra term to account for $CJGATE$.

$ACM=2$ includes the $CJGATE$ parameter for backward compatibility. Therefore, the default behavior of $CJGATE$ makes the $C0BS_SW$ and $C0BD_SW$ intermediate quantities the same as for previous versions. The default patterns are:

- If you do not specify $CJSW$ or $CJGATE$, both default to zero.
- If you do not specify $CJGATE$, it defaults to $CJSW$, which defaults to zero.
- If you specify $CJGATE$, but you do not specify $CJSW$, then $CJSW$ defaults to zero.

Simulation calculates the $C0BS$, $C0BS_SW$, $C0BD$, and $C0BD_SW$ intermediate quantities as follows.

$$\begin{aligned}C0BS &= CJscaled * ASeff \\C0BD &= CJscaled * ADeff\end{aligned}$$

- If ($ACM=0$ or 1), then:

$$\begin{aligned}C0BS_SW &= CJSWscaled * PSeff \\C0BD_SW &= CJSWscaled * PDeff\end{aligned}$$

- If ($ACM=2$) and ($PSeff < W_{eff}$), then:

$$C0BS_SW = CJGATEscaled * PSeff$$

- If ($ACM=2$) and ($PSeff > W_{eff}$), then:

$$C0BS_SW = CJSWscaled * (PSeff - W_{eff}) + CJGATEscaled * W_{eff}$$

- If ($ACM=2$) and ($PDeff < W_{eff}$), then:

$$C0BD_SW = CJGATEscaled * PDeff$$

- If ($ACM=2$) and ($PDeff > W_{eff}$), then:

$$C0BD_SW = CJSWscaled * (PDeff - W_{eff}) + CJGATEscaled * W_{eff}$$

- If ($ACM=3$), then:

$$\begin{aligned}C0BS_SW &= CJSWscaled * PSeff + CJGATEscaled * W_{eff} \\C0BD_SW &= CJSWscaled * PDeff + CJGATEscaled * W_{eff}\end{aligned}$$

Source Diode Capacitance

- If $(C0BS + C0BS_SW) > 0$ and $vbs < 0$, then:

$$capbs = TT \cdot \frac{\partial ibs}{\partial vbs} + C0BS \cdot \left(1 - \frac{vbs}{PB}\right)^{-MJ}$$

$$+ C0BS_SW \cdot \left(1 - \frac{vbs}{PHP}\right)^{-MJSW}$$

If $(C0BS + C0BS_SW) > 0$ and $vbs > 0$, then:

$$capbs = TT \cdot \frac{\partial ibs}{\partial vbs} + C0BS \cdot \left(1 + MJ \cdot \frac{vbs}{PB}\right)$$

$$+ C0BS_SW \cdot \left(1 + MJSW \cdot \frac{vbs}{PHP}\right)$$

Otherwise, if $(C0BS + C0BS_SW) \leq 0$, then:

For $vbs < 0$: $capbs = TT \cdot \frac{\partial ibs}{\partial vbs} + M \cdot CBS \cdot \left(1 - \frac{vbs}{PB}\right)^{-MJ}$

For $vbs > 0$: $capbs = TT \cdot \frac{\partial ibs}{\partial vbs} + M \cdot CBS \cdot \left(1 + MJ \cdot \frac{vbs}{PB}\right)$

Drain Diode Capacitance

- If $(C0BD + C0BD_SW) > 0$, then:

$$capbd = TT \cdot \frac{\partial ibd}{\partial vbd} + C0BD \cdot \left(1 - \frac{vbd}{PB}\right)^{-MJ}$$

$$+ PDeff \cdot C0BD_SW \cdot \left(1 - \frac{vbd}{PHP}\right)^{-MJSW}$$

For $vbd < 0$:

$$capbd = TT \cdot \frac{\partial ibd}{\partial vbd} + C0BD \cdot \left(1 + MJ \cdot \frac{vbd}{PB}\right)$$

$$+ C0BD_SW \cdot \left(1 + MJSW \cdot \frac{vbd}{PHP}\right)$$

For $vbd > 0$:

Otherwise, if $(AD_{eff} \cdot CJ_{scaled} + PD_{eff} \cdot CJSW_{scaled}) \leq 0$, then:

Chapter 4: MOSFET Diode Models

MOS Diode Equations

$$\text{For } vbd < 0: capbd = TT \cdot \frac{\partial ibd}{\partial vbd} + M \cdot CBD \cdot \left(1 - \frac{vbd}{PB}\right)^{-MJ}$$

$$\text{For } vbd > 0: capbd = TT \cdot \frac{\partial ibd}{\partial vbd} + M \cdot CBD \cdot \left(1 + MJ \cdot \frac{vbd}{PB}\right)$$

CMC MOS Varactor Model

This chapter discusses use of CMC MOSFET resistor varactor models.

This section covers the following topics:

- [LEVEL 7: CMC Varactor Model](#)
- [CMC Varactor Model Parameters](#)

LEVEL 7: CMC Varactor Model

The MOS varactor compact model is based in part on the PSP MOSFET model and is intended for analog and RF design. It includes dynamic inversion, finite poly doping, quantum mechanics, tunneling currents, and parasitics to model advanced MOS technologies.

The CMC MOS varactor model is Level 7 in the Synopsys models. To use this model, specify:

```
cXXX g [bi] b cmname w=1u l=1u  
.MODEL cmname c LEVEL=7
```

General Syntax for CMC MOS varactor Model, Version 1.1, Version 1.0, Revision 0.8

The general syntax for a CMC MOS varactor Model element in a netlist is:

```
cXXX g [bi] b cname [L=val] [W=val]  
+ [M=val] [M_SEG=val] [NGCON=val> [DTA=val]
```

Chapter 5: CMC MOS Varactor Model

CMC Varactor Model Parameters

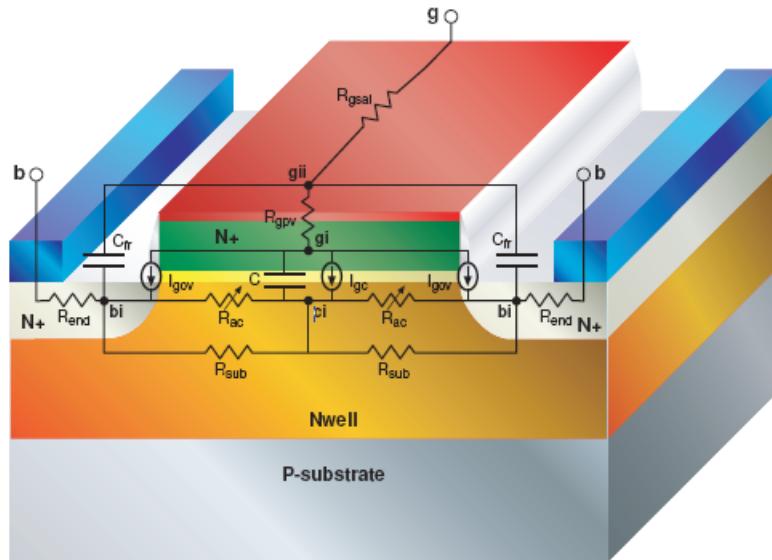


Figure 32 Cross-section of MOS varactor with equivalent circuit model overlapped

In Figure 32, **g**, **bi** and **b** are the external terminals while **gii**, **gi** and **ci** are the internal nodes

The following section describes the PSP-based varactor model parameter set.

CMC Varactor Model Parameters

This section covers the following topics:

- [CMC Varactor Model — Instance Parameters](#)
- [CMC Varactor Model — Special Parameters](#)
- [CMC Varactor Model — Basic Parameters](#)

CMC Varactor Model — Instance Parameters

| Name | Units | Default | Min. | Max. | Description |
|------|-------|-----------|------|------|-----------------------------|
| L | m | 10^{-6} | 0 | - | Design length of a varactor |
| W | m | 10^{-6} | 0 | - | Design width of a varactor |

| Name | Units | Default | Min. | Max. | Description |
|-------|-------|---------|------|------|--|
| m | | 1 | 0 | - | Multiplicity factor |
| M_SEG | | 1 | 1 | - | Number of gate segments |
| NGCON | | 1 | 1 | 2 | Number of gate contacts |
| DTA | ° C | 0 | - | - | Local temperature offset with respect to ambient circuit temperature |

CMC Varactor Model — Special Parameters

| Name | Units | Default | Min. | Max. | Description |
|---------|-------|---------|------|------|-----------------------------|
| version | | 1 | N/A | N/A | Model version |
| TMIN | ° C | -100 | -250 | 27 | Minimum ambient temperature |
| TMAX | ° C | 500 | 27 | 1000 | Maximum ambient temperature |

CMC Varactor Model — Basic Parameters

| Name | Units | Default | Min. | Max. | Description |
|--------|-------|---------------------|------|------|---|
| CFRL | F/m | 0 | 0 | - | Fringing capacitance in length direction |
| CFRW | F/m | 0 | 0- | - | Fringing capacitance in width direction |
| DLQ | m | 0 | - | - | Length delta for capacitor size |
| DNSUBO | | 0 | 0 | 100 | Doping profile slope parameter |
| DWQ | m | 0 | - | - | Width delta for capacitor size |
| DWR | m | 0 | - | - | Width delta for substrate resistance calculation |
| FETA | | 1.0 | 0 | - | Effective field parameter |
| LMAX | m | $9.9 \cdot 10^{-8}$ | 0 | - | Maximum allowed drawn length |
| LMIN | m | 10^{-8} | 0 | - | Minimum allowed drawn length |
| MNSUBO | | 1 | 1 | 10 | Maximum change in absolute doping, limited to 1 order of magnitude up |

Chapter 5: CMC MOS Varactor Model

CMC Varactor Model Parameters

| Name | Units | Default | Min. | Max. | Description |
|--------|--------------------|---------------------|--------------------|-------------------|---|
| NSLPO | | 0.1 | 0.1 | 1 | Doping profile smoothing parameter |
| NSUBO | m^{-3} | $3 \cdot 10^{23}$ | 10^{22} | 10^{25} | Substrate doping level |
| REND | $\Omega \cdot m$ | 10^{-4} | 0 | - | End resistance (extrinsic well resistance plus vertical contact resistance to well) per width |
| RPV | $\Omega \cdot m^2$ | 0 | 0 | - | Vertical resistance down through gate |
| RSHG | Ω / sq | 1 | 0 | - | Gate sheet resistance |
| RSHS | Ω / sq | 1000 | 0 | - | Substrate sheet resistance |
| STREND | | 0 | - | - | Temperature dependence of R_{end} |
| STRPV | | 0 | - | - | Temperature dependence of R_{pv} |
| STRSHG | | 0 | - | - | Temperature dependence of R_{shg} |
| STRSHS | | 0 | - | - | Temperature dependence of R_{shs} |
| STUAC | | 0 | - | - | Temperature dependence of U_{ac} |
| STVFB | V/K | 0 | - | - | Temperature dependence of V_{fb} |
| TOXO | m | $2 \cdot 10^{-9}$ | $5 \cdot 10^{-10}$ | $2 \cdot 10^{-8}$ | Oxide thickness |
| TR | $^{\circ} C$ | 21 | -250 | 1000 | Nominal (reference) temperature |
| UAC | $m^2 / V \cdot s$ | $5 \cdot 10^{-2}$ | 0 | - | Accumulation layer zero-bias mobility |
| UACRED | V^{-1} | 0 | 0 | - | Accumulation layer mobility degradation factor |
| VFBO | V | -1 | - | - | Flat-band voltage ¹ |
| VNSUBO | | 0 | -5 | 5 | Doping profile corner voltage parameter |
| WMAX | m | $9.9 \cdot 10^{-8}$ | 0 | - | Maximum allowed drawn width |
| WMIN | m | 10^{-8} | 0 | - | Minimum allowed drawn width |

Chapter 5: CMC MOS Varactor Model
CMC Varactor Model Parameters

| Name | Units | Default | Min. | Max. | Description |
|--|-----------------|------------------|------------------|------------------|---|
| Switch or switch-like parameters | | | | | |
| SWRES | | 1 | 0 | 1 | Switch to control series resistance: 0: exclude 1: include |
| NPO | m ⁻³ | 10 ²⁷ | 10 ²⁴ | 10 ²⁷ | Polysilicon doping level |
| QMC | | 1 | 0 | - | Quantum mechanical correction factor |
| SWIGATE | | 0 | 0 | 1 | Flag for gate current: 0: turn off 1: turn on |
| TAU | s | 0.1 | 0 | 10 | Time constant for inversion charge recombination/generation |
| TYPE | | -1 | -1 | 1 | Substrate doping type: -1: n-type +1:p-type |
| TYPEP | | -1 | -1 | 1 | Polysilicon doping type: -1: ntype +1! p-type |
| Additional model parameters for modeling gate tunneling currents | | | | | |
| CHIBO | V | 3.1 | 1.0 | - | Tunneling barrier height for electrons |
| CHIBPO | V | 4.5 | 1.0 | - | Tunneling barrier height for holes |
| GC2EVO | | 0.375 | 0 | 0 | EVB gate current slope factor |
| GC2HVO | | 0.375 | 0 | 0 | HVB gate current slope factor |
| GC2O | | 0.375 | 0 | 0 | ECB gate current slope factor |
| GC3EVO | | 0.063 | -10 | 10 | EVB gate current curvature factor |
| GC3HVO | | 0.063 | -10 | 10 | HVB gate current curvature factor |
| GC3O | | 0.063 | -10 | 10 | ECB gate current curvature factor |
| GCOEVO | | 0 | -10 | 10 | EVB gate tunneling energy adjustment |
| GCOHVO | | 0 | -10 | 10 | HVB gate tunneling energy adjustment |
| GCOO | | 0 | -10 | 10 | ECB gate tunneling energy adjustment |
| IGCEVLW | A | 0 | 0 | - | EVB gate channel current prefactor for $1\mu m^2$ channel area |

Chapter 5: CMC MOS Varactor Model

CMC Varactor Model Parameters

| Name | Units | Default | Min. | Max. | Description |
|---------|----------|-------------------|-----------|-----------|---|
| IGCHVLW | A | 0 | 0 | - | HVB gate channel current prefactor for $1\mu m^2$ channel area |
| IGINVLW | A | 0 | 0 | - | ECB gate channel current prefactor for $1\mu m^2$ channel area |
| IGMAX | A | 10^{-5} | 0 | - | Maximum gate current |
| IGOVEVW | A | 0 | 0 | - | EVB gate overlap current pre-factor for $1\mu m$ wide gate overlap region |
| IGOVHVW | A | 0 | 0 | - | HVB gate overlap current prefactor for $1\mu m$ wide gate overlap region |
| IGOVW | A | 0 | 0 | - | ECB gate overlap current pre-factor for $1\mu m$ wide gate overlap region |
| LOV | m | 0 | 0 | - | Overlap length |
| NOVO | m^{-3} | $5 \cdot 10^{25}$ | 10^{22} | 10^{26} | Effective doping level of overlap regions |

1. In PSP, VFBO corresponds to NMOS and is negative of the actual value for PMOS. For varactor, you specify the actual value.

6

MOSFET Noise Models

This chapter discusses use of available MOSFET noise model parameters.

HSPICE ships hundreds of examples for your use; see [Listing of Demonstration Input Files](#) for paths to demo files.

These topics are presented in the following sections:

This section covers the following topics:

- [MOSFET Model — Noise Parameters](#)
- [MOSFET Model — Noise Equations](#)

MOSFET Model — Noise Parameters

This section describes noise model parameters.

| Name (Alias) | Units | Default | Description |
|--------------|--------------------|---------|---|
| AF | | 1.0 | Flicker noise exponent. |
| KF | | 0.0 | Flicker noise coefficient. Reasonable values for KF are in the range 1e-19 to 1e-25 V ² F. |
| NLEV | | 2.0 | Noise equation selector. Values are 1, 2, or 3. |
| RD | V ² /Hz | | Output thermal noise due to drain resistor. |
| RS | V ² /Hz | | Output thermal noise due to source resistor. |

Chapter 6: MOSFET Noise Models

MOSFET Model — Noise Equations

| Name (Alias) | Units | Default | Description |
|--------------|------------------------|---------|---|
| RX | | | Transfers the function of thermal noise to the output. This is not noise, but is a transfer coefficient, which reflects the contribution of thermal noise to the output. For example: $V(\text{output}) = I(\text{local}) * rx(\text{from local to output})$ Where $V(\text{output})$ is the noise voltage at the output port, $I(\text{local})$ is the local noise current in the specific noise element. It is clear that rx should have an unit of impedance, therefore we call it transimpedance. By summarizing all the contributions (power) from each independent noisy element, we can get the total noise contribution(power) at the output port. |
| ID | V^2/Hz | | Output channel thermal noise: $ID = RX^2 P$ (channel thermal noise) 2 . |
| FN | V^2/Hz | | Output flicker noise: $FN = RX^2 P$ (flicker noise) 2 . |
| IFEX | | | Noise due to floating body |
| LGS | | | Shot noise due to I_{gs} |
| LGD | | | Shot noise due to I_{gd} |
| LGF | | | Shot noise due to I_{gf} |
| TOT | V^2/Hz | | Total output noise: $TOT = RD + RS + ID + FN + IFEX + RG + IGS + IGD + IGF$. |

For different MOS models, the total noise equation maybe different; it always equals the sum of the noise types listed. RD, RS, ID, FN are the basic noise types (all MOSFET models contain these).

MOSFET Model — Noise Equations

The MOSFET model noise equations have a selector parameter, NLEV, that selects either the original SPICE flicker noise or an equation proposed by Gray and Meyer.

You can model thermal noise generation in the drain and source resistors as two sources, inrd and inrs (units amp/(Hz) $^{1/2}$) as shown in [Example 33](#).

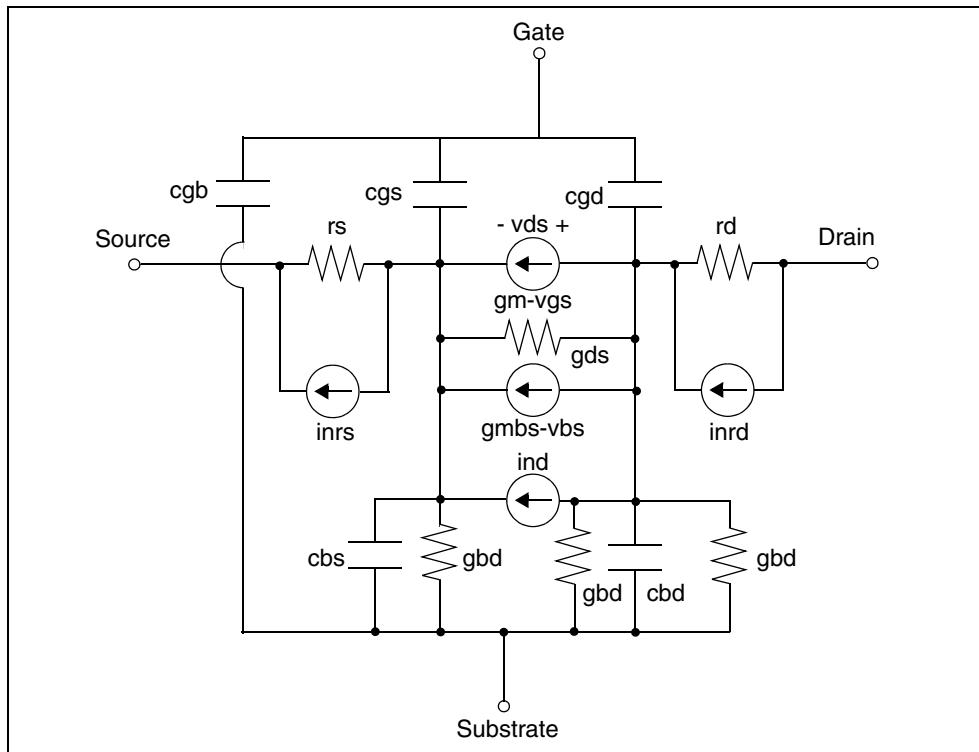


Figure 33 Equivalent Circuit, MOSFET AC Noise Analysis

The following equations calculate the values of these sources:

$$inrs = \left(\frac{4kt}{rs} \right)^{1/2}, \quad inrd = \left(\frac{4kt}{rd} \right)^{1/2}$$

You can model the channel thermal noise and the flicker noise as the ind current source, which the following equation defines:

$$ind^2 = (\text{channel thermal noise})^2 + (\text{flicker noise})^2$$

If the NLEV model parameter is less than 3, then:

$$\text{channel thermal noise} = \left(\frac{8kT \cdot gm}{3} \right)^{1/2}$$

The preceding formula, used in both saturation and linear regions, can lead to wrong results in the linear region. For example, at VDS=0, channel thermal noise becomes zero because gm=0. This calculation is physically impossible. If you set the NLEV model parameter to 3, simulation uses a different equation,

Chapter 6: MOSFET Noise Models

MOSFET Model — Noise Equations

which is valid in both linear and saturation regions. (See *Operation and Modeling of the MOS Transistor* by Yanis P. Tsivids, published by McGraw-Hill, 1987, p. 340.)

For NLEV=3

$$\text{channel thermal noise} = \left(\frac{8kt}{3} \cdot \beta \cdot (vgs - vth) \cdot \frac{1+a+a^2}{1+a} \cdot GDSNOI \right)^{1/2}$$

The following equations calculate the a value used in the preceding equation:

$$a = 1 - \frac{vds}{vdsat} \quad \text{Linear region}$$

$$a = 0 \quad \text{Saturation region}$$

Use the AF and KF parameters in the small-signal AC noise analysis to determine the equivalent flicker noise current generator, which connects the drain to the source.

NLEV=0 (SPICE):

$$\text{flicker noise} = \left(\frac{KF \cdot Ids^{AF}}{COX \cdot L_{eff}^2 \cdot f} \right)^{1/2}$$

For NLEV=1

L_{eff}^2 in the above equation is replaced by $W_{eff} \cdot L_{eff}$.

For NLEV=2, 3

$$\text{flicker noise} = \left(\frac{KF \cdot gm^2}{COX \cdot W_{eff} \cdot L_{eff} \cdot f^{AF}} \right)^{1/2}$$

A

Technology Summary for HSPICE MOSFET Models

Describes the technology used in all HSPICE MOSFET models.

This section covers the following topics:

- [MOSFET Equivalent Circuits](#)
- [MOSFET DC Operating Point Output](#)
- [Common Threshold Voltage Equations](#)
- [MOSFET Impact Ionization](#)
- [Temperature Parameters and Equations](#)

MOSFET Equivalent Circuits

This section covers the following topics:

- [Equation Variables](#)
- [Using MOSFET Current Convention](#)
- [Using MOSFET Equivalent Circuits](#)

Equation Variables

This section lists the equation variables and constants.

Variable/Quantity Definition

| | |
|---------|---|
| cbd:cbd | Bulk-to-drain transcapacitance |
| cbs:cbs | Bulk-to-source transcapacitance |
| cbg:cbg | Gate-to-bulk transcapacitance |
| cgd:cgd | Gate-to-drain transcapacitance |
| cgs:cgs | Gate-to-source transcapacitance |
| cds:csd | Drain-to-source transcapacitance |
| f | Frequency |
| gbd | Bulk-to-drain dynamic conductance |
| gbs | Bulk-to-source dynamic conductance |
| gds | Drain-to-source dynamic conductance (controlled by vds) |
| gdb | Drain-to-bulk impact ionization conductance |
| gm | Drain-to-source dynamic transconductance (controlled by vgs) |
| gmbs | Drain-to-source dynamic bulk transconductance (controlled by vsb) |
| ibd | Bulk-to-drain DC current |
| ibs | Bulk-to-source DC current |
| ids | Drain-to-source DC current |
| idb | Drain-to-bulk impact ionization current |
| ind | Drain-to-source equivalent noise circuit |
| inrd | Drain resistor equivalent noise circuit |
| inrs | Source resistor equivalent noise circuit |
| rd | Drain resistance |

Variable/Quantity Definition

| | |
|----------------------|--|
| rs | Source resistance |
| v _{sb} | Source-to-bulk voltage |
| v _{ds} | Drain-to-source voltage |
| v _{gs} | Gate-to-source voltage |
| Δt | t-t _{nom} |
| ɛ _{si} | 1.0359e-10F/m dielectric constant of silicon |
| k | 1.38062e-23 (Boltzmann's constant) |
| q | 1.60212e-19 (electron charge) |
| t | New temperature of model or element in °K |
| t _{nom} | t _{nom} = TNOM + 273.15. This variable represents the nominal temperature of parameter measurements in °K (user input in °C). |
| v _t | k · t/q |
| v _{t(tnom)} | k · t _{nom} /q |

Using MOSFET Current Convention

[Figure 34](#) shows the assumed direction of current flow through a MOS transistor. To print the drain current, use either I(M1) or I1(M1) syntax.

- I2 produces the gate current.
- I3 produces the source current.
- I4 produces the substrate current.

References to bulk are the same as references to the substrate.

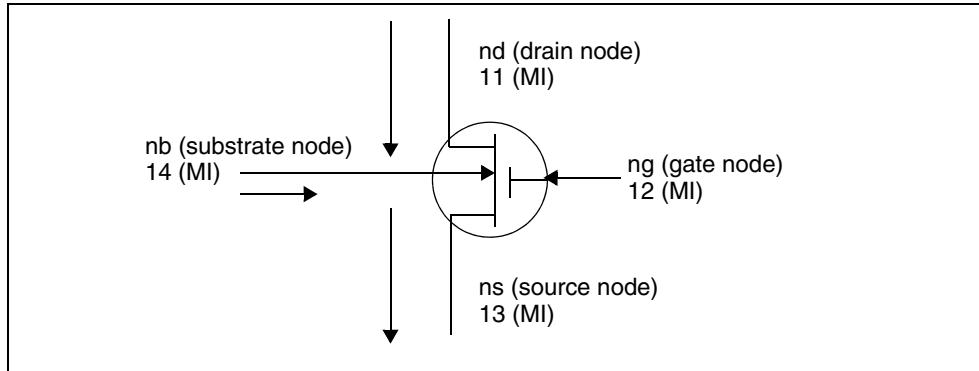


Figure 34 MOSFET Current Convention, N-channel

Using MOSFET Equivalent Circuits

Simulators use three equivalent circuits to analyze MOSFETs:

- DC
- Transient
- AC and noise-equivalent circuits

The components of these circuits form the basis for all element and model equations. The equivalent circuit for DC sweep is the same as the one used for transient analysis, but excludes capacitances. [Figure 35](#) through [Figure 37](#) display the MOSFET equivalent circuits.

The fundamental component in the equivalent circuit is the DC drain-to-source current (i_{ds}). Noise and AC analyses do not use the actual i_{ds} current. Instead, the model uses the partial derivatives of i_{ds} with respect to the v_{gs} , v_{ds} , and v_{bs} terminal voltages.

The names for these partial derivatives are as follows.

$$\text{Transconductance: } g_m = \frac{\partial(i_{ds})}{\partial(v_{gs})}$$

$$\text{Conductance: } g_{ds} = \frac{\partial(i_{ds})}{\partial(v_{ds})}$$

$$\text{Bulk Transconductance: } g_{mbs} = \frac{\partial(i_{ds})}{\partial(v_{bs})}$$

Appendix A: Technology Summary for HSPICE MOSFET Models
MOSFET Equivalent Circuits

The i_{ds} equation describes the basic DC effects of the MOSFET. Simulation considers the effects of gate capacitance, and of source and drain diodes, separately from the DC i_{ds} equations. Simulation also evaluates the impact ionization equations separately from the DC i_{ds} equation, even though the ionization effects are added to i_{ds} .

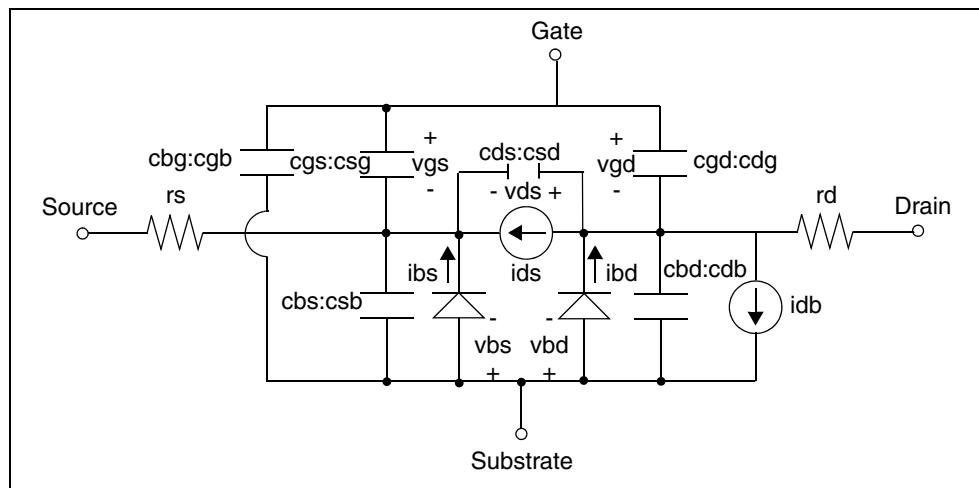


Figure 35 Equivalent Circuit, MOSFET Transient Analysis

Appendix A: Technology Summary for HSPICE MOSFET Models

MOSFET Equivalent Circuits

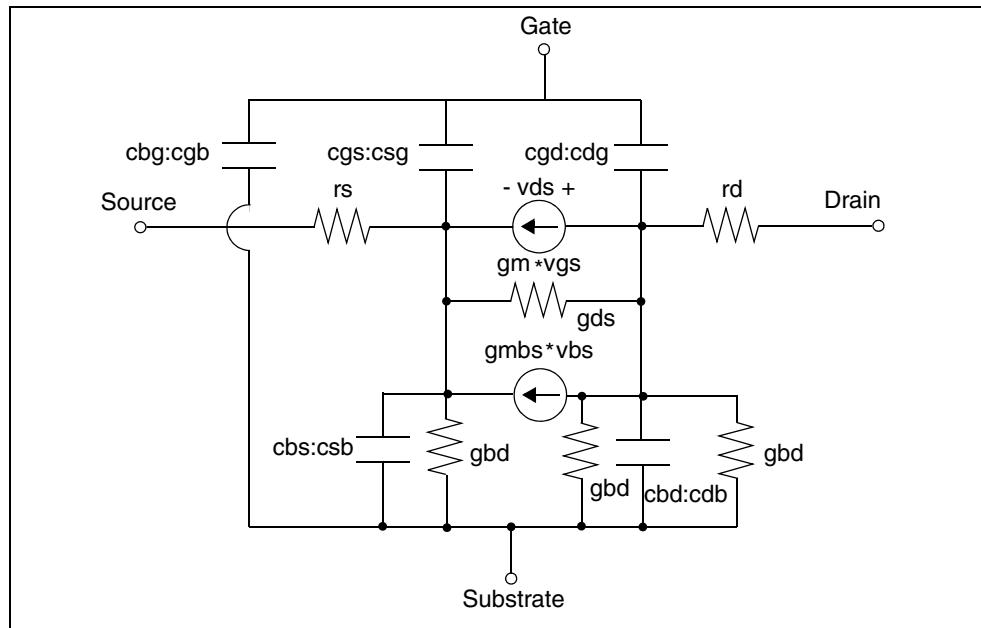


Figure 36 Equivalent Circuit, MOSFET AC Analysis

Appendix A: Technology Summary for HSPICE MOSFET Models
MOSFET Equivalent Circuits

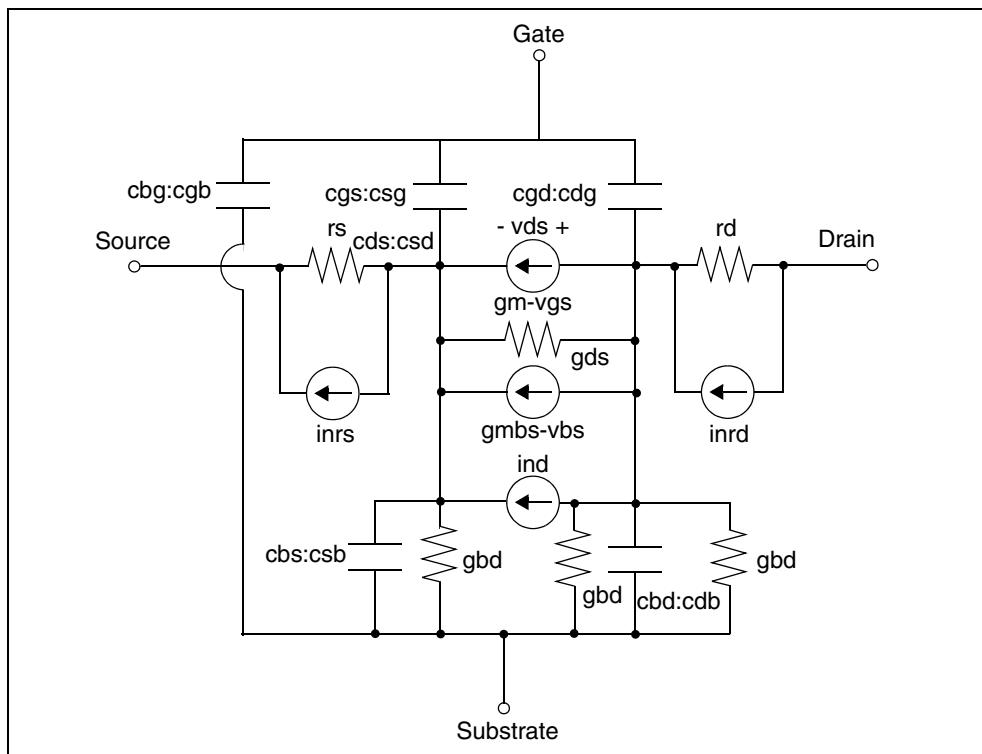


Figure 37 *Equivalent Circuit, MOSFET AC Noise Analysis*

MOSFET DC Operating Point Output

Table 9 General MOSFET DC Operating Point Output

| Quantities | Definitions |
|------------|---|
| id | drain current |
| ibs | B-S bulk-to-source current |
| ibd | B-D bulk-to-drain current |
| vgs | G-S gate-source voltage |
| vds | D-S drain-source voltage |
| vbs | B-S bulk-source voltage |
| vth | threshold voltage |
| vdsat | saturation voltage |
| beta | beta value |
| gam eff | gamma effective |
| gm | DC gate transconductance |
| gds | D-S drain-source conductance |
| gmb | B-S bulk-source conductance |
| cdtot | total drain capacitance |
| cgtot | total gate capacitance |
| cstot | total source capacitance |
| cbtot | total bulk capacitance (total floating body capacitance for SOI MOSFET) |
| cgs | total gate- to-source capacitance |
| cgd | total gate- to-drain capacitance |

Hspice also supports extended DC operating point output with .OPTION
EXT_OP=1

Appendix A: Technology Summary for HSPICE MOSFET Models
MOSFET DC Operating Point Output

The extended DC OP output supports MOSFET model Level=49 (BSIM3), Level 54 (BSIM4), Level 69 (PSP), and Level 76 (UTSOI):

| Name | Unit | Formulation | Description |
|--------------------------|------|-------------------------------------|--|
| Total currents | | | |
| Ide | A | - | Total DC drain current |
| Ige | A | - | Total DC gate current |
| Ise | A | - | Total DC source current |
| Ibe | A | - | Total DC bulk current |
| Internal currents | | | |
| Ids | A | - | DC Drain current, excluding avalanche, tunnel, GISL, GIDL, and junction currents |
| idb | A | - | DC drain-bulk current |
| isb | A | - | DC source-bulk current |
| Applied voltages | | | |
| V _{ds} | V | - | Drain-Source DC voltage |
| V _{sb} | V | - | Source-Bulk DC voltage |
| V _{gs} | V | - | Gate-Source DC voltage |
| Transconductances | | | |
| Gm | A/V | $\delta(\text{ide})/\delta(V_{gs})$ | DC transconductance |
| Gmb | A/V | $\delta(\text{ide})/\delta(V_{sb})$ | DC bulk transconductance |
| Gds | A/V | $\delta(\text{ide})/\delta(V_{ds})$ | DC output conductance |
| Transcapacitors | | | |
| C _{gs} | F | See Transcapacitance | AC Gate-Source capacitance, including overlap capacitances |
| C _{gd} | F | See Transcapacitance | AC Gate-Drain capacitance, including overlap capacitances |

Appendix A: Technology Summary for HSPICE MOSFET Models

MOSFET DC Operating Point Output

| Name | Unit | Formulation | Description |
|---------------------------|----------|-----------------------|---|
| Csb | F | See Transcapacitance | AC Source-Bulk capacitance |
| Cgb | F | See Transcapacitance | AC Gate-Bulk capacitance |
| Cdb | F | See Transcapacitance | AC Drain-Bulk capacitance |
| Cds | F | See Transcapacitance | AC Drain-Source capacitances |
| Cdg | F | See Transcapacitance | AC Drain-Gate capacitance |
| Csg | F | See Transcapacitance | AC Source-Gate capacitance |
| Csd | F | See Transcapacitance | AC Source-Drain capacitance |
| Cbd | F | See Transcapacitance | AC Bulk-Drain capacitance |
| Cbg | F | See Transcapacitance | AC Bulk-Gate capacitance |
| Cbs | F | See Transcapacitance | AC Bulk-Source capacitance |
| Capacitors | | | |
| Cgg | F | See Capacitance | AC Gate capacitance. Including overlap capacitances |
| Cdd | F | See Capacitance | AC Drain capacitance |
| Css | F | See Capacitance | AC Source capacitance |
| Cbb | F | See Capacitance | AC Bulk capacitance |
| Derived parameters | | | |
| Vth | V | - | Threshold voltage including back bias and drain bias effects |
| Vgt | V | Vgs - Vth | Effective gate drive voltage including back bias and drain bias effects |
| Vdss | V | - | Drain saturation voltage at actual bias |
| Vsat_marg | V | Vds – Vdss | Vds margin |
| Self_gain | - | Gm/Gds | Transistor self gain |
| Rout | Ω | 1/gds | AC output resistor |
| Beff | A/(V*V) | 2*abs(jide)/(vgt*vgt) | Gain factor |

Appendix A: Technology Summary for HSPICE MOSFET Models

Common Threshold Voltage Equations

| Name | Unit | Formulation | Description |
|----------|----------|-----------------------|-------------------------------------|
| Fug | Hz | $Gm/[2 * \pi * cg_g]$ | Unity gain frequency at actual bias |
| Rgate | Ω | See Rgate | MOS gate resistance |
| Gmoverid | 1/V | Gm/Id_s | Gm over Id |
| Vearly | V | $abs(id_e)/g_{ds}$ | Equivalent early voltage |

Common Threshold Voltage Equations

The parameters described in this section works for MOSFET model Level 1, 2, 3, 13, 28, 47, and 50.

This section covers the following topics:

- [Common Threshold Voltage Parameters](#)
- [Calculating PHI, GAMMA, and VTO](#)

Common Threshold Voltage Parameters

The parameters described in this section works for MOSFET model Level 1, 2, 3, 13, 28, 47, and 50.

| Name (Alias) | Units | Default | Description |
|----------------|-----------|----------|---|
| DELVTO | V | 0.0 | Zero-bias threshold voltage shift. |
| GAMMA | $V^{1/2}$ | 0.527625 | Body effect factor. If you do not set GAMMA, simulation calculates it from NSUB. |
| NGATE | $1/cm^3$ | - | Polysilicon gate doping, used for analytical models only. Undoped polysilicon is represented by a small value. If NGATE ≤ 0.0 , it is set to $1e+18$. |
| NSS | $1/cm^2$ | 1.0 | Surface state density. |
| NSUB (DNB, NB) | $1/cm^3$ | $1e15$ | Substrate doping. |
| PHI | V | 0.576036 | Surface potential. NSUB default= $1e15$. |

Appendix A: Technology Summary for HSPICE MOSFET Models

Common Threshold Voltage Equations

| Name (Alias) | Units | Default | Description |
|--------------|-------|---------|---|
| TPG (TPS) | - | 1.0 | Type of gate material for analytical models. LEVEL 4 TPG default=0. The TPG value can be: <ul style="list-style-type: none"> ■ TPG = 0 al-gate. ■ TPG = 1 same as source-drain diffusion. ■ TPG = -1 gate type opposite to source-drain diffusion. |
| VTO (VT) | V | - | Zero-bias threshold voltage. |

Calculating PHI, GAMMA, and VTO

Use the PHI, GAMMA, and VTO model parameters to calculate threshold voltages. If you do not specify these parameters, simulation calculates them as follows, except for the LEVEL 5 model.

If you do not specify PHI, then: $\text{PHI} = 2 \cdot vt \cdot \ln\left(\frac{NSUB}{ni}\right)$

If you do not specify GAMMA, then: $\text{GAMMA} = \frac{(2 \cdot q \cdot \varepsilon si \cdot NSUB)^{1/2}}{COX}$

The following equations determines the energy gap (eg) and intrinsic carrier concentration used in the above equations:

$$eg = 1.16 - 7.02e-4 \cdot \frac{tnom^2}{tnom + 1108}$$

$$ni = 1.45e+10 \cdot \left(\frac{tnom}{300}\right)^{3/2} \cdot e^{\left[\frac{q \cdot eg}{2 \cdot k} \cdot \left(\frac{1}{300} - \frac{1}{tnom}\right)\right]} (1/\text{cm}^3)$$

In the preceding equation, $tnom = TNOM + 273.15$.

If you do not specify VTO, then for Al-Gate ($\text{TPG}=0$), the following equation determines the Φ_{ms} ms work function: $\Phi_{ms} = -\frac{eg}{2} - \text{type} \cdot \frac{\text{PHI}}{2} - 0.05$

In the preceding equation, type is +1 for n-channel or -1 for p-channel.

For Poly-Gate ($\text{TPG}=\pm 1$), the following equations determine the work function.

If you do not specify the NGATE model parameter, then:

$$\Phi_{ms} = type \cdot \left(-TPG \cdot \frac{eg}{2} - \frac{PHI}{2} \right)$$

If you specify NGATE, then: $\Phi_{ms} = type \cdot \left[-TPG \cdot vt \cdot \ln\left(\frac{NGATE}{ni}\right) - \frac{PHI}{2} \right]$

If you do not specify the VTO model parameter, then the following equation determines the VTO voltage: $VTO = vfb + type \cdot (GAMMA \cdot PHI^{1/2} + PHI)$

In the preceding equation, $vfb = \Phi_{ms} - \frac{q \cdot NSS}{COX} + DELVTO$.

If you specify VTO, then: $VTO = VTO + DELVTO$.

MOSFET Impact Ionization

The parameters described in this section works for MOSFET model Level 1, 2, 3, 13, 28, 47, and 50.

Impact ionization current is available for all MOSFET levels. ALPHA, VCR, and IIRAT are the controlling parameters. IIRAT sets the fraction of the impact ionization current sent to the source.

$$I_{ds} = I_{ds_normal} + IIRAT \cdot I_{impact}$$

$$I_{db} = I_{db_diode} + (1-IIRAT) \cdot I_{impact}$$

IIRAT defaults to zero, which sends all impact ionization current to bulk. Leave IIRAT at its default value unless data is available for both drain and bulk current.

| Name (Alias) | Units | Default | Description |
|--------------|--------|---------|---------------------------------------|
| ALPHA | 1/V | 0.0 | Impact ionization current coefficient |
| LALPHA | μm/V | 0.0 | ALPHA length sensitivity |
| WALPHA | μm/V | 0.0 | ALPHA width sensitivity |
| VCR | V | 0.0 | Critical voltage |
| LVCR | μm · V | 0.0 | VCR length sensitivity |

Appendix A: Technology Summary for HSPICE MOSFET Models

MOSFET Impact Ionization

| Name (Alias) | Units | Default | Description |
|--------------|------------------------------|---------|---|
| WVCR | $\mu\text{m} \cdot \text{V}$ | 0.0 | VCR width sensitivity |
| IIRAT | | 0.0 | Portion of impact ionization current sent to the source |

This section covers the following topics:

- [Calculating the Impact Ionization Equations](#)
- [Calculating Effective Output Conductance](#)
- [Cascoding Example](#)
- [Cascode Circuit](#)

Calculating the Impact Ionization Equations

The following equations calculates the I_{impact} current due to the impact

$$\text{ionization effect: } I_{\text{impact}} = I_{ds} \cdot \text{ALPHA}_{eff} \cdot (v_{ds} - v_{dsat}) \cdot e^{\frac{-VCReff}{v_{ds} - v_{dsat}}}$$

The following equations calculate values used in the preceding equation:

$$\text{ALPHA}_{eff} = \text{ALPHA} + L\text{ALPHA} \cdot 1e-6 \cdot \left(\frac{1}{L_{eff}} - \frac{1}{LREF_{eff}} \right)$$

$$W\text{ALPHA} \cdot 1e-6 \cdot \left(\frac{1}{W_{eff}} - \frac{1}{WREF_{eff}} \right)$$

$$VCReff = VCR + LVCR \cdot 1e-6 \cdot \left(\frac{1}{L_{eff}} - \frac{1}{LREF_{eff}} \right)$$

$$WVCR \cdot 1e-6 \cdot \left(\frac{1}{W_{eff}} - \frac{1}{WREF_{eff}} \right)$$

The following equations calculate the $LREF_{eff}$ and $WREF_{eff}$ values used in the preceding equations:

$$LREF_{eff} = LREF + XLREF - 2 \cdot LD$$

$$WREF_{eff} = WREF + XWREF - 2 \cdot WD$$

Calculating Effective Output Conductance

You can use the element template to directly output gds. For example:

```
.PRINT I(M1) gds=LX8(M1)
```

If you use impact ionization current, gds is the derivative of I_{ds} only, rather than the total drain current, which is $I_{ds}+I_{db}$.

The complete drain output conductance is:

$$g_{dd} = \frac{\partial I_d}{\partial V_d} = \frac{\partial I_{ds}}{\partial V_{ds}} + \frac{\partial I_{db}}{\partial V_{db}} = \frac{\partial I_{ds}}{\partial V_{ds}} + \frac{\partial I_{bd}}{\partial V_{bd}} = g_{ds} + g_{bd}$$

$$G_{dd} = LX8 + LX10$$

For example, to print the drain output resistance of the M1 device:

```
.PRINT rout=PAR('1.0/(LX8(M1)+LX10(M1))')
```

Appendix A: Technology Summary for HSPICE MOSFET Models

MOSFET Impact Ionization

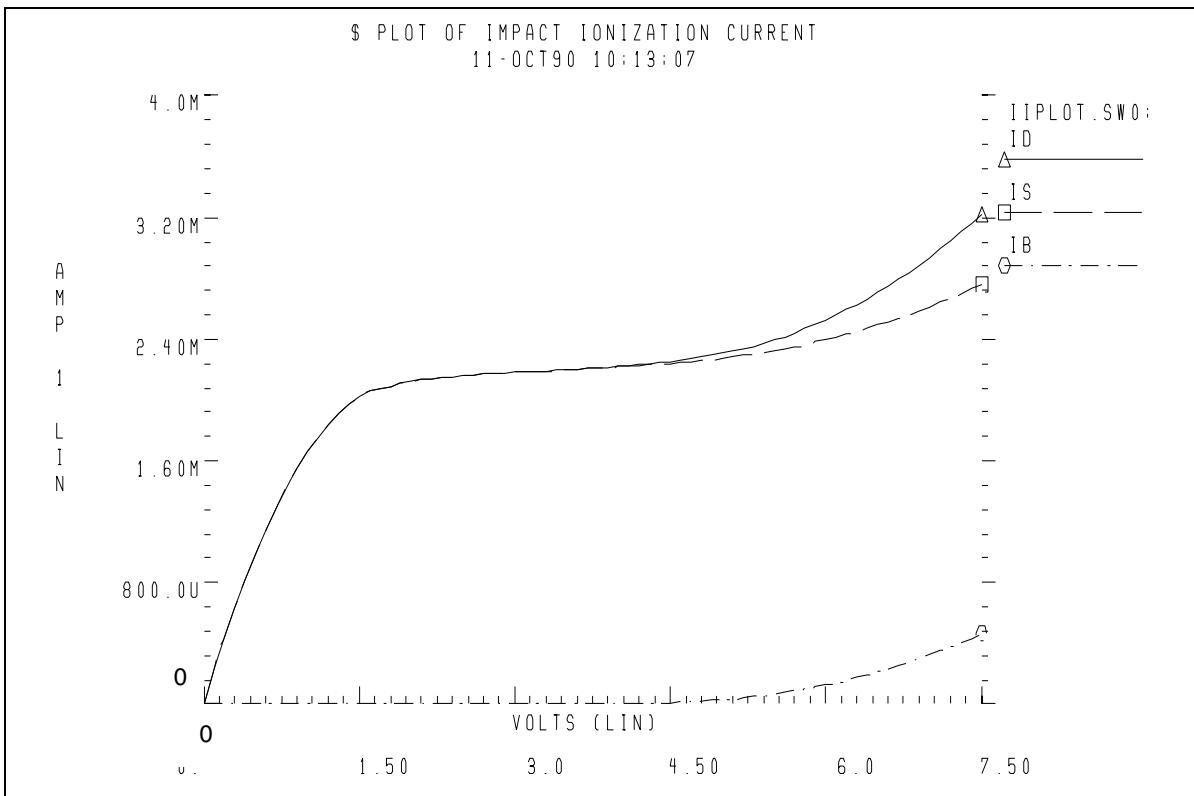


Figure 38 Drain, Source, and Bulk Currents for $v_{gs}=3$ with $IIRAT=0.5$

Cascoding Example

Drain-to-bulk impact ionization current limits the use of cascoding to increase output impedance. The following cascode example shows the effect of changing **IIRAT**. If **IIRAT** is less than 1.0, the drain-to-bulk current lowers the output impedance of the cascode stage.

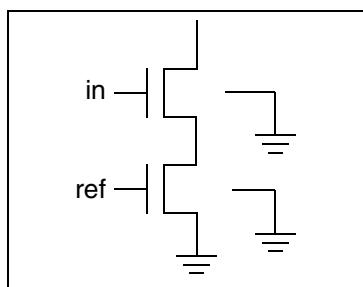


Figure 39 Low-frequency AC Analysis Measuring Output Impedance

Cascode Circuit

Example

| iirat | gout_ac | rout |
|-------|---------|----------|
| 0.0 | 8.86E-6 | 113 K |
| 0.5 | 4.30E-6 | 233 K |
| 1.0 | 5.31E-8 | 18.8 Meg |

This example is based on demonstration netlist cascode.sp, which is available in directory \$<installdir>/demo/hspice/mos:

```
$ cascode test
.option post
.param pvds=5.0 poref=1.4 pvin=3.0
vdd dd 0 pvds ac 1
$ current monitor vd
vd dd d 0
vin in 0 pvin
vref ref 0 poref
x1 d in ref cascode
.macro cascode out in ref
m1 out in 1 0 n L=1u W=10u
mref 1 ref 0 0 n L=1u W=10u
.eom
.param xiirat=0
.ac dec 2 100k 1x sweep xiirat poi 3 0, 0.5, 1.0
.print ir(vd)
.measure gout_ac avg ir(vd)
.model n nmos level=3
+ tox=200 vto=0.8 gamma=0.7 uo=600 kappa=0.05
+ alpha=1 vcr=15 iirat=xiirat
.end
```

Temperature Parameters and Equations

This section covers the following topics:

- [Temperature Parameters](#)
- [Temperature Equations](#)

Appendix A: Technology Summary for HSPICE MOSFET Models

Temperature Parameters and Equations

Temperature Parameters

The following temperature parameters apply to all MOSFET model levels and the associated bulk-to-drain and bulk-to-source MOSFET diode within the MOSFET model. The TLEV and TLEVC parameters select the temperature equations used to calculate the temperature effects on the model parameters.

| Name (Alias) | Units | Default | Description |
|--------------|------------------|---------|--|
| BEX | | -1.5 | Low field mobility, UO, temperature exponent. |
| CTA | 1/ $^{\circ}$ K | 0.0 | Junction capacitance (CJ) temperature coefficient. If TLEVC=1, CTA overrides the default temperature compensation. |
| CTP | 1/ $^{\circ}$ K | 0.0 | Junction sidewall capacitance (CJSW) temperature coefficient. If TLEVC=1, CTP overrides the default temperature compensation. |
| EG | eV | | Energy gap for pn junction diode for TLEV=0 or 1, default=1.11; for TLEV=2, default=1.16 1.17 – silicon 0.69 – Schottky barrier diode 0.67 – germanium 1.52 – gallium arsenide |
| F1EX | | 0 | Bulk junction bottom grading coefficient |
| GAP1 | eV/ $^{\circ}$ K | 7.02e-4 | First bandgap correction factor (from Sze, alpha term). 7.02e-4 – silicon 4.73e-4 – silicon 4.56e-4 – germanium 5.41e-4 – gallium arsenide |
| GAP2 | $^{\circ}$ K | 1108 | Second bandgap correction factor (from Sze, beta term). 1108 – silicon 636 – silicon 210 – germanium 204 – gallium arsenide |
| LAMEX | 1/ $^{\circ}$ K | 0 | LAMBDA temperature coefficient. |
| N | | 1.0 | Emission coefficient. |
| MJ | | 0.5 | Bulk junction bottom grading coefficient. |
| MJSW | | 0.33 | Bulk junction sidewall grading coefficient. |

Appendix A: Technology Summary for HSPICE MOSFET Models

Temperature Parameters and Equations

| Name (Alias) | Units | Default | Description |
|--------------|-----------------|---------|---|
| PTA | V/ $^{\circ}$ K | 0.0 | Junction potential (PB) temperature coefficient. If you set TLEVC to 1 or 2, PTA overrides the default temperature compensation. |
| PTC | V/ $^{\circ}$ K | 0.0 | Fermi potential (PHI) temperature coefficient. If you set TLEVC to 1 or 2, PTC overrides the default temperature compensation. |
| PTP | V/ $^{\circ}$ K | 0.0 | Junction potential (PHP) temperature coefficient. If TLEVC=1 or 2, PTP overrides the default temperature compensation. |
| TCV | V/ $^{\circ}$ K | 0.0 | Threshold voltage temperature coefficient. Typical values are +1mV for n-channel and -1mV for p-channel. |
| TLEV | | 0.0 | Temperature equation level selector. Set TLEV=1 for ASPEC style. Default is SPICE style. If you invoke the ASPEC option, the program sets TLEV for ASPEC. |
| TLEVC | | 0.0 | Temperature equation level selector for junction capacitances and potentials. Interacts with TLEV. Set TLEVC=1 for ASPEC style. Default is SPICE style. If you invoke the ASPEC option, the program sets TLEVC for ASPEC. |
| TRD | 1/ $^{\circ}$ K | 0.0 | Temperature coefficient for drain resistor. |
| TRS | 1/ $^{\circ}$ K | 0.0 | Temperature coefficient for source resistor. |
| XTI | | 0.0 | Saturation current temperature exponent. Use XTI=3 for silicon diffused junction. Set XTI=2 for Schottky barrier diode. |

MOS Temperature Coefficient Sensitivity Parameters

Model levels 13 (BSIM1), 39 (BSIM2), and 28 (METAMOS) include length and width sensitivity parameters as shown in [Table 10](#). Use these parameters with the Automatic Model Selector to enable more accurate modeling for various device sizes. The default value of each sensitivity parameter is zero to ensure backward compatibility.

Table 10 MOS Temperature Coefficient Sensitivity Parameters

| Parameter | Description | Sensitivity Parameters | | |
|-----------|--|------------------------|-------|---------|
| | | Length | Width | Product |
| BEX | Low field mobility, UO, temperature exponent | LBEX | WBEX | PBEX |

Appendix A: Technology Summary for HSPICE MOSFET Models

Temperature Parameters and Equations

Table 10 MOS Temperature Coefficient Sensitivity Parameters

| Parameter | Description | Sensitivity Parameters | | |
|-----------|---|------------------------|-------|---------|
| | | Length | Width | Product |
| FEX | Velocity saturation temperature exponent | LFEX | WFEX | PFEX |
| TCV | Threshold voltage temperature coefficient | LTCV | WTCV | PTCV |
| TRS | Temperature coefficient for source resistor | LTRS | WTRS | PTRS |
| TRD | Temperature coefficient for drain resistor | LTRD | WTRD | PTRD |

Temperature Equations

This section covers the following topics:

- [Energy Gap Temperature Equations](#)
- [Saturation Current Temperature Equations](#)
- [MOS Diode Capacitance Temperature Equations](#)
- [Surface Potential Temperature Equations](#)
- [Threshold Voltage Temperature Equations](#)
- [Mobility Temperature Equations](#)
- [Channel Length Modulation Temperature Equation](#)
- [Calculating Diode Resistance Temperature Equations](#)

Energy Gap Temperature Equations

These equations set the energy gap for temperature compensation:

For TLEV = 0 or 1:

$$egnom = 1.16 - 7.02e-4 \cdot \frac{tnom^2}{tnom + 1108.0}$$

$$eg(t) = 1.16 - 7.02e-4 \cdot \frac{t^2}{t + 1108.0}$$

For TLEV = 2:

$$egnom = EG - GAP1 \cdot \frac{tnom^2}{tnom + GAP2}$$

$$eg(t) = EG - GAP1 \cdot \frac{t^2}{t + GAP2}$$

Saturation Current Temperature Equations

$$isbd(t) = isbd(tnom) \cdot e^{facln/N}, \quad isbs(t) = isbs(tnom) \cdot e^{facln/N}$$

The following equation calculates the `facln` value used in the preceding equations:

$$facln = \frac{egnom}{vt(tnom)} - \frac{eg(t)}{vt(t)} + XTI \cdot \ln\left(\frac{t}{tnom}\right)$$

MOSFET Diode Models defines the `isbd` and `isbs` values.

MOS Diode Capacitance Temperature Equations

TLEVVC selects the temperature equation level for MOS diode capacitance.

For TLEVVC=0:

$$PB(t) = PB \cdot \left(\frac{t}{tnom} \right) - vt(t) \Rightarrow \left[3 \cdot \ln\left(\frac{t}{tnom}\right) + \frac{egnom}{vt(tnom)} - \frac{eg(t)}{vt(t)} \right]$$

$$PHP(t) = PHP \cdot \left(\frac{t}{tnom} \right) - vt(t) \Rightarrow \left[3 \cdot \ln\left(\frac{t}{tnom}\right) + \frac{egnom}{vt(tnom)} - \frac{eg(t)}{vt(t)} \right]$$

$$CBD(t) = CBD \cdot \left[1 + MJ \cdot \left(400u \cdot \Delta t - \frac{PB(t)}{PB} + 1 \right) \right]$$

$$CBS(t) = CBS \cdot \left[1 + MJ \cdot \left(400u \cdot \Delta t - \frac{PB(t)}{PB} + 1 \right) \right]$$

$$CJ(t) = CJ \cdot \left[1 + MJ \cdot \left(400u \cdot \Delta t - \frac{PB(t)}{PB} + 1 \right) \right]$$

$$CJSW(t) = CJSW \cdot \left[1 + MJSW \cdot \left(400u \cdot \Delta t - \frac{PHP(t)}{PHP} + 1 \right) \right]$$

For TLEVVC=1:

$$PB(t) = PB - PTA \Rightarrow \Delta t, \quad PHP(t) = PHP - PTP \Rightarrow \Delta t$$

$$CBD(t) = CBD \cdot (1 + CTA \cdot \Delta t), \quad CBS(t) = CBS \cdot (1 + CTA \cdot \Delta t)$$

$$CJ = CJ \cdot (1 + CTA \cdot \Delta t), \quad CJSW = CJSW \cdot (1 + CTP \cdot \Delta t)$$

Appendix A: Technology Summary for HSPICE MOSFET Models

Temperature Parameters and Equations

For TLEV=2:

$$PB(t) = PB - PTA \Rightarrow \Delta t, PHP(t) = PHP - PTP \Rightarrow \Delta t$$

$$CBD(t) = CBD \cdot \left(\frac{PB}{PB(t)} \right)^{MJ}, CBS(t) = CBS \cdot \left(\frac{PB}{PB(t)} \right)^{MJ}$$

$$CJ(t) = CJ \cdot \left(\frac{PB}{PB(t)} \right)^{MJ}, CJSW(t) = CJSW \cdot \left(\frac{PHP}{PHP(t)} \right)^{MJSW}$$

For TLEV=3:

$$PB(t) = PB + dpbdt \cdot \Delta t, PHP(t) = PHP + dphpd़t \cdot \Delta t$$

$$CBD(t) = CBD \cdot \left(1 - 0.5 \Rightarrow dpbdt \Rightarrow \frac{\Delta t}{PB} \right)$$

$$CBS(t) = CBS \cdot \left(1 - 0.5 \Rightarrow dpbdt \Rightarrow \frac{\Delta t}{PB} \right)$$

$$CJ(t) = CJ \cdot \left(1 - 0.5 \Rightarrow dpbdt \Rightarrow \frac{\Delta t}{PB} \right)$$

$$CJSW(t) = CJSW \cdot \left(1 - 0.5 \Rightarrow dphpd़t \Rightarrow \frac{\Delta t}{PHP} \right)$$

If TLEV=3 and TLEV=0 or 1, then:

$$dpbdt = -\frac{\left[egnom + 3 \cdot vt(tnom) + (1.16 - egnom) \cdot \left(2 - \frac{tnom}{tnom + 1108} \right) - PB \right]}{tnom}$$

$$dphpd़t = -\frac{\left[egnom + 3 \cdot vt(tnom) + (1.16 - egnom) \cdot \left(2 - \frac{tnom}{tnom + 1108} \right) - PHP \right]}{tnom}$$

For TLEV=2:

$$dpbdt = -\frac{\left[egnom + 3 \cdot vt(tnom) + (EG - egnom) \cdot \left(2 - \frac{tnom}{tnom + GAP2} \right) - PB \right]}{tnom}$$

$$dphpd़t = -\frac{\left[egnom + 3 \cdot vt(tnom) + (EG - egnom) \cdot \left(2 - \frac{tnom}{tnom + GAP2} \right) - PHP \right]}{tnom}$$

Surface Potential Temperature Equations

For TLEV=0:

$$PHI(t) = PHI \cdot \left(\frac{t}{tnom} \right) - vt(t) \Rightarrow \left[3 \cdot \ln \left(\frac{t}{tnom} \right) + \frac{egnom}{vt(tnom)} - \frac{eg(t)}{vt(t)} \right]$$

For TLEV=1:

$$PHI(t) = PHI - PTC \Rightarrow \Delta t$$

If you do not specify the PHI parameter, simulation calculates it as:

$$PHI(t) = 2 \cdot vt(t) \cdot \ln \left(\frac{NSUB}{ni} \right)$$

The intrinsic carrier concentration, ni, must be temperature updated, and it is calculated from the silicon bandgap at room temperature.

$$ni = 145e16 \cdot \left(\frac{t}{tnom} \right)^{3/2} \cdot \exp \left[EG \cdot \left(\frac{t}{tnom} - 1 \right) \cdot \left(\frac{1}{2 \cdot vt(t)} \right) \right]$$

For TLEV=2:

$$PHI(t) = PHI - PTC \Rightarrow \Delta t$$

For TLEV=3:

$$PHI(t) = PHI + dphidt \cdot \Delta t$$

If TLEV=3 and TLEV=0 or 1, then:

$$dphidt = -\frac{\left[egnom + 3 \cdot vt(tnom) + (1.16 - egnom) \cdot \left(2 - \frac{tnom}{tnom + 1108} \right) - PHI \right]}{tnom}$$

For TLEV=2:

$$dphidt = -\frac{\left[egnom + 3 \cdot vt(tnom) + (EG - egnom) \cdot \left(2 - \frac{tnom}{tnom + GAP2} \right) - PHI \right]}{tnom}$$

Threshold Voltage Temperature Equations

The threshold temperature equations are:

Appendix A: Technology Summary for HSPICE MOSFET Models

Temperature Parameters and Equations

For TLEV=0:

$$vbi(t) = vbi(tnom) + \frac{PHI(t) - PHI}{2} + \frac{egnom - eg(t)}{2}$$

$$VTO(t) = vbi(t) + GAMMA \cdot (PHI(t))^{1/2}$$

For TLEV=1:

$$VTO(t) = VTO - TCV \cdot \Delta t$$

$$vbi(t) = VTO(t) - GAMMA \cdot (PHI(t))^{1/2}$$

For TLEV=2:

$$VTO(t) = VTO + \left(1 + \frac{GAMMA}{2 \cdot PHI^{1/2}}\right) \cdot dphi/dt \cdot \Delta t$$

$$vbi(t) = VTO(t) - GAMMA \cdot (PHI(t))^{1/2}$$

Mobility Temperature Equations

The MOS mobility temperature equations are:

$$UO(t) = UO \cdot \left(\frac{t}{tnom}\right)^{BEX}$$

$$KP(t) = KP \cdot \left(\frac{t}{tnom}\right)^{BEX}$$

$$F1(t) = F1 \cdot \left(\frac{t}{tnom}\right)^{F1EX}$$

Channel Length Modulation Temperature Equation

If you specify the LAMEX model parameter, then the temperature modifies the LAMBDA value.

$$LAMBDA(t) = LAMBDA \cdot (1 + LAMEX \cdot \Delta t)$$

Calculating Diode Resistance Temperature Equations

The following equations are examples of the effective drain and source resistance:

$$RD(t) = RS \cdot (1 + TRD \cdot \Delta t), RS(t) = RS \cdot (1 + TRS \cdot \Delta t)$$

Index

A

AC analysis, MOSFETs 812
ACM
 model parameter 779
 MOS diode 781, 784, 787, 790
 parameter 13, 777, 778
alternate saturation model parameters 100
analysis
 MOSFETs
 AC 805, 812, 813
 transient 811
ASPEC
 compatibility 126, 787
 option 13
automatic model selection
 failure 7
 multisweep or .TEMP effect 7
 See also model selection

B

basic model parameters
 LEVEL 2 58
 LEVEL 39 192
 LEVEL 49, 53 261
 LEVEL 5 59
 LEVEL 57 360
 LEVEL 58 389
 LEVELs 6, 7 59
Berkeley
 junction model 249
 NonQuasi-Static (NQS) model 249
BJT models 814
BSIM model
 VERSION parameter effects 143
BSIM2 model
 VERSION parameter effects 202
BSIM3 model
 equations 227
 Leff/Weff 227
 SOI FD 399
BSIM3 SOI FD
 template output 407

BSIM3 Version 2 MOS model 223
BSIM3v3
 Ig model 259
 WPE model 258
BSIM3v3 model
 HSPICE 244
 MOS 238
BSIM4 Juncap2 model 298
BSIM4 model
 STI/LOD 301
BSIM4.5.0 327
BSIM4.6.0 327
BSIM-CMG model
 LEVEL 72, BSIM-CMG model 605
BSIMMG model (see BSIM-CMG) 605
bulk
 transconductance, MOSFETs 810
BYPASS option 13, 15

C

capacitance
 CAPOP model selector 11
 control options 752
 equations 793
 model
 parameters 753
 selection 743
 MOSFETs
 AC gate 776
 BSIM model 147
 diodes 793
 gate capacitance 751
 gate capacitance example 748
 gate capacitance length/width 776
 gate capacitance models 742
 Meyer model 742
 models 743
 overlap 756
 plotting 751
 capacitor models
 gate 742
 list 12

Index

D

capacitor, transcapacitance 744
CAPOP model parameter 11, 743, 753
 XPART 755
cascoding example 822
CBD model parameter 779
CBS model parameter 779
CDB model parameter 779
channel length modulation
 equations
 LEVEL 2 74
 LEVEL 3 80
 LEVEL 38 189
 LEVEL 5 95
 LEVEL 6 122
 LEVEL 8 133
 parameters
 LEVEL 8 129
charge conservation 768, 770
CJ model parameter 779
CJA model parameter 779
CJGATE model parameter 779
CJP model parameter 779
CJSW model parameter 779
CMC MOS Varactor 797
CMC MOS Varactor Model
 Level 7 797
commands
 .LIB 4
conductance
 MOSFETs 810, 821
 preventing negative output 151, 202
control options
 ASPEC 13
 BYPASS 13
 capacitance 752
convergence, MOSFET diodes 778
CSB model parameter 779
current convention 809

D

DC
 current 793
DEFAD option 13
DEFAS option 13
DEFL option 13
DEFNRD option 13
DEFNRS option 13

DEFPD option 13
DEFW option 14
diodes
 capacitance equations 793
 MOSFETs
 capacitance equations 793
 equations 792
 model selector 13
 models 777
 resistance temperature 830
DLAT model parameter 781
DNB model parameter 780
drain current equation 232
DW model parameter 781

E

Early voltage 69
effective channel length
 equations
 LEVEL 1 70
 LEVEL 13 144
 LEVEL 28 178
 LEVEL 49 272
 LEVEL 5 89
 LEVEL 6 103
 LEVEL 8 130
 parameters
 LEVEL 3 78
effective channel width
 equations
 LEVEL 1 70
 LEVEL 13 144
 LEVEL 2 72
 LEVEL 28 178
 LEVEL 5 89
 LEVEL 6 103
 parameters
 LEVEL 8 130
effective channel width, MOSFETs
 equations
 LEVEL 2 72
 LEVEL 3 78
effective mobility
 equations
 LEVEL 28 179
 LEVEL 3 80
 LEVEL 8 132
 parameters 118
EFPS option 13

element
 statements 4
 templates 747
element parameters
 MOSFETs 790
 scaling 15
Empirical model
 equations 77
 example 83
.ENDL command 4
energy gap temperature 826
equations
 capacitance
 MOSFETs 793
 diodes 792, 793
 impact ionization 820
MOSFETs
 diode 792, 830
 impact ionization 820
 LEVEL 62 437
 model parameters 818
 models, BSIM3 223, 227
 models, Empirical 77
 models, HP a-Si TFT 217
 noise 804
 temperature 826
 voltage 817
MOSFETs, models, modified - BSIM LEVEL 28
 177
MOSFETs, models, Schichman-Hodges 69, 71
noise 351, 804
temperature
 energy gap 826
 MOSFETs 826
equivalent circuit 807, 810
AC analysis 812
AC noise analysis 805, 813
transient analysis 811
EXA model parameter 780
example
 cascoding 822
 MOSFETs
 IDS LEVEL 7 108, 111
EXD model parameter 780
EXJ model parameter 780
EXP model parameter 780
EXS model parameter 780

F
FC model parameter 780
flicker noise 804
G
gate capacitance 773
 AMI 774
 charge sharing coefficient 755
 length/width 776
 LEVEL 39 201, 206
 model (CAPOP=39) 203
 parameters 742
 plotting 751
gate direct tunneling currents 259
geometry
 scaling 15
global scaling 15
GMIN option 14
GMINDC option 14, 778

H
HDIF model parameter 781
HiSIM2 model 517
HiSIM241 489
HiSim-HV model 679
HP a-Si TFT model
 equations 217
HSPICE
 VERSION parameter 143

I
IDS
 equations
 LEVEL 1 69
 LEVEL 13 144
 LEVEL 2 71
 LEVEL 3 77
 LEVEL 38 185
 LEVEL 5 88
 LEVEL 6 103
 LEVEL 8 130
 LEVEL 6
 example 108, 111
 LEVEL 8
 equations 130
lg model, BSIM3v3 259

Index

J

impact ionization
 BSIM2 206
 MOSFETs 820
 equations 811, 820
 LEVEL 39 206
inactive devices
 See latent devices
intrinsic model parameters 353
IS model parameter 779
ISPICE LEVEL 6 model 115

J

JS model parameter 779
JSW model parameter 779
juncap2 junction model 298

L

lambda equations 104, 105
LATD model parameter 781
latency option 15
latent devices 15
LD model parameter 781
LDAC parameter 776
LDIF model parameter 781
Level 68 HiSIM Model 489
Level 68, HiSIM2.3.1 517
.LIB command 4
 nesting 4
libraries 6
 building 4
linear region equations 231
LRD model parameter 780
LRS model parameter 780

M

MBYPASS option 13, 16
Meyer capacitance
 gate 759
 model 742
 modified 762
MJ model parameter 780
MJSW model parameter 780
mobility
 parameters
 curve fitting 65

 LEVEL 2 65–67
 LEVEL 5 67
reduction equations
 LEVEL 2 73
 LEVEL 38 188
 LEVEL 5 95
model name identification 10
model names, periods in 7
model parameters
 ACM 13
 intrinsic limits 353
 MOSFETs 123, 124
 scaling 15
model selection
 failure to find a model 7
 program 7, 16
 See also automatic model selection
.MODEL statement 3, 4
 BSIM models 143
 MOSFETs 9
 VERSION parameter 143
models
 automatic selection 16
 capacitance 11
 equations
 LEVEL 61 422
 LEVEL 62 431, 437
MOSFETs
 BSIM3-SOI FD 407
 Empirical 77
 HP a-Si TFT 217
 Hspice junction 249
 LEVEL 55, updates 355
 modified BSIM LEVEL 28 177
 RPI a-Si TFT 419
 Schichman-Hodges 69, 71
 UFSOI 388
MOSFETs, BSIM3, equations 227
MOSFETs, BSIM3-SOI 357
MOSFETs, BSIM3v3, NQS 249
MOSFETs, IDS - LEVEL 6 and LEVEL 7 100
MOSFETs, IDS, LEVEL 5, equations 92
MOSFETs, IDS, LEVEL 6, example 108, 111
MOSFETs, junction 249
 scaling 15
 simulator access 4
 specifying 8
modified BSIM LEVEL 28
 equations 177

- MOSFET output templates 19
MOSFETs
 7-node limit 10
 BEX factor 157
 bulk transconductance 810
 capacitance
 effective length and width 776
 Meyer model 742
 models 743
 scaling parameters 753
 channel length modulation 830
 charge
 storage modeling 742
 conductance 810
 current convention 809
 diodes
 DC current equations 793
 DC model parameters 778
 effective areas 783
 effective drain and source resistance 783, 786,
 790, 792
 effective saturation current 783, 792
 equation 792
 equations 793
 GEO element parameter 790
 model parameters 778
 model select 777
 resistance, temperature equations 830
 suppressing 787
 temperature equations 827
 effective
 length and width 776
 output conductance 821
 energy gap temperature equations 826
 equivalent circuits 810
 AC analysis 812
 AC noise analysis 805, 813
 transient analysis 811
 gate
 capacitance example 748
 capacitance model parameters 742
 impact ionization equations 811, 820
 level parameter 9
 LEVELs 6, 7 UPDATE selector 101
 mobility temperature equations 830
 model parameters
 A0 401
 A1 401
 A2 401
AGIDL 402
AGS 402
ALPHA0 402
ASD 405
AT 406
B0 402
B1 402
BGIDL 402
BSIM3-SOI FD 400
CAPMOD 401
CDSC 402
CDSCB 402
CDSCD 402
CF 405
CGDL 405
CGDO 405
CGSL 405
CGSO 405
change conservation 755
CIT 402
CJSWG 405
CKAPPA 405
CLC 406
CLE 406
CSDESW 406
CSDMIN 406
CTH0 406
DELTA 402
DLC 406
DROUT 402
DSUB 402
DVT0 403
DVT0W 403
DVT1 403
DVT1W 403
DVT2 403
DVT2W 403
DWB 403
DWC 406
DWG 403
ETA0 403
ETAB 403
gate capacitance, basic 753
gate capacitance, Meyer 754
gate capacitance, overlap 754
impact ionization 819
ISBJT 403
ISDIF 403

Index

M

- ISREC 403
ISTUN 403
K1 403
K2 403
K3 403
K3B 403
KB1 403
KETA 404
KT1 406
KT2 406
KTIL 406
LEVEL 401
Level 60 410
Level 70 563
LINT 404
MJSWG 406
MOBMOD 401
NCH 401
NDIO 404
NFACTOR 404
NGATE 401
NGIDL 404
NLX 404
NOIMOD 401
noise 803
NSS 405
NSUB 401
NTUN 404
PBSWG 406
PCLM 404
PDIBLC1 404
PDIBLC2 404
PRT 406
PRWB 404
PRWG 404
PVAG 404
RBODY 404
RBSH 404
RDSW 404
RSH 404
RTH0 407
SHMOD 401
SII0 402
SII1 402
SII2 402
SIID 402
TBOX 401
temperature 824
threshold voltage 817
TNOM 407
TOX 401
TSI 401
TT 406
U0 404
UA 405
UA1 407
UB 405
UB1 407
UC 405
UC1 407
UTE 407
VBSA 405
VERSION 240
VOFF 405
VSAT 405
VSDFB 406
VSDTH 406
VTH0 405
WINT 405
WR 405
XBJT 407
XDIF 407
XPART 406
XREC 407
XTUN 407
models
 Berkeley, BSIM3-SOI DD 408
 Berkeley, junction 249
 BSIM 136
 BSIM, equations 143
 BSIM, LEVEL 13 example 151
 BSIM2 192, 196
 BSIM3, equations 227
 BSIM3v3, NQS 249
 Cypress 182, 184
 Empirical 77
 EPFL-EKV 330, 337
 HP a-Si TFT 215, 217
 IDS - LEVEL 5 87
 IDS - LEVEL 6 equations 103, 114
 IDS - LEVEL 6 example 108, 111
 IDS - LEVEL 7 128
 IDS - LEVEL 8 129
 LEVELs 49 and 53 equations 275
 modified BSIM LEVEL 28 171, 177
 MOS 86

Philips MOS9 280
quasi-static, equations 348
RPI Poli-Si TFT 425
Schichman-Hodges 69, 71
SOSFETs 160
statement 8
University of Florida SOI 388
n-channel specification 9
noise 804
model equations 804
model parameters 803, 804
p-channel specification 9
RPI a-Si TFT model 419
saturation current 827
sensitivity factors 176
surface potential 829
temperature
 coefficient model parameters 825
 effects parameters 824
 parameters 824
template input 407
threshold voltage
 model parameters 817
 temperature equations 829
 transconductance 810
Multi-Level Gamma model, example 108, 111

N

N model parameter 779
narrow width effect 72
NB model parameter 780
NDS model parameter 779
nested library calls 4
noise
 MOSFETs 803
 equivalent circuits 805, 813
NonQuasi-Static (NQS) model 249
NSUB model parameter 780

O

operating point
 capacitance printout 746
Early voltage 352
model internal variables 352
Overdrive voltage 352
saturation voltage 352
SPICE-like threshold voltage 352

transconductance efficiency factor 352
.OPTION MBYPASS 16
output conductance 821
overlap capacitors 756

P

parameter range limit
 Level 54 293
 Level 57 370
 Level 70 583
 Levels 49/53 272
parameters
 simulator access 4
 voltage 817
parasitic
 diode, MOSFETs LEVEL 39 206
 generation 787
 MOSFETs LEVEL 13 156
PB model parameter 780
PHA model parameter 780
PHD model parameter 780
PHP model parameter 780
PHS model parameter 780
PRD model parameter 780
PRS model parameter 780

R

RD model parameter 780
RDC model parameter 780
resistance
 MOSFETs model parameters 780
RL model parameter 780
RPI
 a-Si TFT model 419
RS model parameter 780
RSC model parameter 780
RSH model parameter 780

S

saturation
 voltage equations, MOSFETs
 LEVEL 1 70
 LEVEL 13 146
 LEVEL 2 73
 LEVEL 28 179
 LEVEL 3 79

Index

T

- LEVEL 38 188
- LEVEL 5 95
- LEVEL 6 113
- LEVEL 8 131
- SCALE option 14, 15
- scaling 15
 - global SCALM override 15
 - global vs model 15
- MOSFETs capacitance parameters 753
- SCALM 14
 - parameter
 - global scaling 15
 - overriding in a model 15
 - scaling by model 15
- Schichman-Hodges model 71
- sensitivity factors 176
- short-channel effect 72
- Simpson Integration 766
- simulation 69
- SOI model 163
- SPICE
 - compatibility
 - BSIM model 153
 - diodes 787
 - MOSFETs
 - LEVEL 39 200
 - MOSFETs, LEVEL 13 153
 - UTRA model parameter 65
 - Meyer gate capacitances 757
- stacked devices 790
- statements
 - .ENDL 4
 - .LIB 4
 - nesting 4
- subthreshold current equations
 - LEVEL 13 146
 - LEVEL 2 75
 - LEVEL 3 81
 - LEVEL 38 189
 - LEVEL 5 96
 - LEVEL 6 116
 - LEVEL 8 134
- T**
- temperature compensation
 - BSIM LEVEL 13 156
- effect
 - BSIM LEVEL 13 147
 - LEVEL 39 205
- equations 826
- MOSFETs
 - diode 827
 - equations 826
 - parameters 824
 - parameters 824
- temperature compensation 234
- threshold voltage
 - equations 817
 - LEVEL 1 70
 - LEVEL 13 146
 - LEVEL 2 72
 - LEVEL 28 178
 - LEVEL 3 79
 - LEVEL 38 186
 - LEVEL 47 228
 - LEVEL 5 93
 - LEVEL 6 104
 - LEVEL 8 131
 - parameters 817
 - LEVEL 2 65
 - LEVEL 5 61
- transcapacitance 744
- transconductance 810
- transient analysis 811
- transistors
 - process parameters
 - LEVEL 13 137–141
 - LEVEL 28 171
- TT model parameter 780
- U**
- University of California SOI model 357
- University of Florida SOI model 388
- UPDATE parameter 158
 - LEVEL 13 158
 - LEVEL 6, 7 101
- V**
- varactor model, Level 7 797
- VERSION parameter 143
- VNDS model parameter 779
- voltage 817

W

- WDAC parameter 776
- WDEL model parameter 781
- well-proximity effects 258
- WL option 14
- WMLT model parameter 781
- WPE model, BSIM3v3 258
- WRD model parameter 780

WRS model parameter 781

X

- XJ model parameter 781
- XPART CAPOP model parameter 755
- XQC CAPOP model parameter 755
- XW model parameter 781

Index
X