

An 8T-SRAM for Variability Tolerance and Low-Voltage Operation in High-Performance Caches

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Abstract—An eight-transistor (8T) cell is proposed to improve variability tolerance and low-voltage operation in high-speed SRAM caches. While the cell itself can be designed for exceptional stability and write margins, array-level implications must also be considered to achieve a viable memory solution. These constraints can be addressed by modifying traditional 6T-SRAM techniques and conceding some design complexity and area penalties. Altogether, 8T-SRAM can be designed without significant area penalty over 6T-SRAM while providing substantially improved variability tolerance and low-voltage operation with no need for secondary or dynamic power supplies. The proposed 8T solution is demonstrated in a high-performance 32 kb subarray designed in 65 nm PD-SOI CMOS that operates at 5.3 GHz at 1.2 V and 295 MHz at 0.41 V.

Index Terms—Multiport memories, SRAM, stability, static noise margin, variation, write margin.

I. INTRODUCTION

AS VARIABILITY concerns mount in future CMOS technologies, SRAM cell stability, which depends on delicately balanced transistor characteristics, becomes a significant concern [1]. With small device dimensions, aggressive ground rules, and an ever-increasing demand for on-chip cache capacity, SRAM is particularly sensitive to device variation. Unlike general logic paths, where random variation can be averaged out to an extent by placing multiple logic stages in series, each memory cell must function within specifications. While tradeoffs between power and performance exist just as in logic design, variability brings new tradeoffs to SRAM design.

In traditional 6T-SRAM (Fig. 1(a)), cells must be both stable during a read event and writeable during a write event. Ignoring redundancy, such functionality must be preserved for each cell under worst-case variation. Concessions must generally be made in power, performance, or area to achieve sufficient yield. At the cell level, transistor strength ratios must be chosen such that cell static noise margin and write margin are both maintained, which presents conflicting constraints on

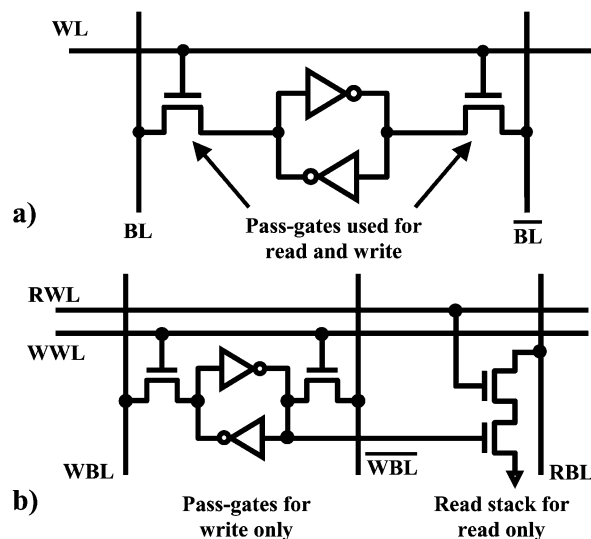


Fig. 1. Circuit diagrams for a) standard 6T-SRAM cell and b) 8T-SRAM cell.

the cell transistor strengths. For cell stability during a read, it is desirable to strengthen the storage inverters and weaken the pass-gates. The opposite is desired for cell writeability: a weak storage inverter and strong pass-gates. This delicate balance of transistor strength ratios can be severely impacted by device variation, which dramatically degrades stability and write margins, especially in scaled technologies. Low supply voltages further exacerbate the problem as threshold voltage variation consumes a larger fraction of these voltage margins. Variability can thus limit the minimum operating voltage of SRAM.

To circumvent variability problems, many design techniques have been proposed to enable low-voltage operation of 6T cells. The addition of a second higher supply voltage dedicated to the SRAM array [2] is an effective method to ensure sufficient margins with scaling of the logic supply voltage. In such a case, the SRAM voltage does not scale with technology and could even be increased as variability intensifies. Instead of being tied to a fixed higher supply, SRAM arrays could also use dynamically modulated supplies [3], [4] that are pulsed to different levels when a read or write event occurs. To an extent, this decouples read and write events from the standby condition such that the optimum bias conditions can be used in each case. Such techniques invariably add complexity to the design, but can be used to improve cell stability and writeability [3] or standby leakage [4]. While tradeoffs between cell optimization for read and write can be reduced by these methods, they cannot be eliminated.

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In a 6T cell, variability tolerance is compromised by the conflicting needs of cell read stability and writeability. Because the same pass-gate devices are used to both read and write the cell, it is inevitable that the two conditions cannot be simultaneously optimized. Just as dynamically modulated power supplies decouple requirements for read and write, such an effect can also be achieved by modifying the cell itself. In an 8T cell [5], [6], two transistors are added to create a disturb-free read mechanism. Since read and write are controlled by separate devices within the cell, the two are entirely decoupled—a level that 6T cells can never reach even with dual or dynamic voltage techniques. This widens the cell optimization space to achieve sufficient stability and writeability margins without the need for secondary or dynamic voltage supplies. In addition, like register files, separation of read and write ports in the cell itself enables 1R1W dual-port operation, which provides significant systems performance advantages. While other cell options have been proposed in the literature for variability tolerance, they generally carry considerable tradeoffs in floorplanning [7] or cell size [8]; in contrast, the 8T cell enables reuse of traditional SRAM and register file design techniques.

6T cell stability problems also arise during a write operation to an unselected column when the word line is activated while both bit lines are held high—a situation that produces equivalent bias conditions to a read operation. While the 8T cell itself removes read stability concerns, the only true method to eliminate cell disturbs during such a partial write operation requires that column select functionality within the array be disallowed. Predictably, this requires modifications in the array organization. Just as important as the cell itself, such array-level changes are necessary to achieve the full stability benefit of an 8T implementation.

In this work, 8T-SRAM cell and array design techniques to achieve high-speed, variation-tolerant caches are presented. Improved cell stability enables writeability enhancement, which, in turn, can lead to higher speed, lower voltage cache operation and potentially allow for continued technology scaling. Practical array implementation techniques to achieve a design that is competitive in area with 6T-SRAM are discussed—culminating in the demonstration of a high-performance 32 kb subarray fabricated in 65 nm PD-SOI CMOS [6].

II. 8T-SRAM CELL DESIGN

The 8T cell used in this work is shown in Fig. 1(b), in which a two-transistor read stack is added to a conventional 6T cell. The original 6T word line is used exclusively for write operations while a second read word line is tied to the read stack. With this configuration, cell disturbs during a read access are effectively eliminated.

Depending on the impact of variability, the additional two transistors in an 8T cell could lead to an increase in cell area over conventional 6T cells. The cell schematic, however, enables a compact layout (Fig. 2(b)) that can be placed into an array in a similar manner to 6T cells. Like the word line in a 6T cell, the read and write word lines (RWL and WWL) in an 8T cell can run horizontally across the cell width. The additional word line increases metal density, which could increase wire delay or

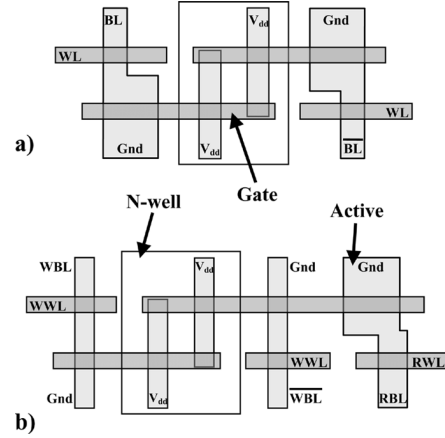


Fig. 2. Cell layouts for a) 6T-SRAM and b) 8T-SRAM.

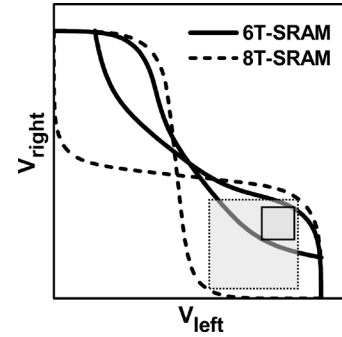


Fig. 3. Worst-case static noise margin for 8T-SRAM is simply that for two cross-coupled inverters, which is significantly better than that of 6T-SRAM.

enhance capacitive coupling between adjacent word lines; however, both can be controlled with proper design. The cell aspect ratio maintains a short read bit line length in the vertical direction. In a 65 nm node technology at constant read current, the penalty over a dense 6T cell (as might be used for higher level caches) is approximately 30% while a comparison with a high performance 6T cell (as might be used for lower level caches) yields a penalty closer to 20%. A key reason for this difference is that 6T cells require that both halves of the cell be enlarged to improve cell read performance while 8T cells only need a size increase in a single read stack. This cell size penalty over 6T can be expected to reduce or disappear completely with technology and voltage scaling. For the high-performance applications targeted in this work, the fabricated 8T cell size in 65 nm hardware is $0.9 \mu\text{m}^2$. No additional process steps (implant masks, gate oxides, etc.) on top of a standard flow were used to build this cell.

In an 8T cell, a read operation does not affect the contents of the cell. The worst-case static noise margin [9] is simply that for two cross-coupled inverters (Fig. 3). For a 6T cell, however, the worst-case static noise margin occurs in the read condition. In this case, the pass-gate disturbs the “0” storage node by pulling it up above ground, which significantly degrades the static noise margin (Fig. 3). Even if the cell β ratio for a 6T cell is increased [5] (thus trading off cell area to match that of the 8T), the 8T still provides a considerably improved static noise margin (Fig. 4), which significantly improves cell yield. Usage of the 8T cell is

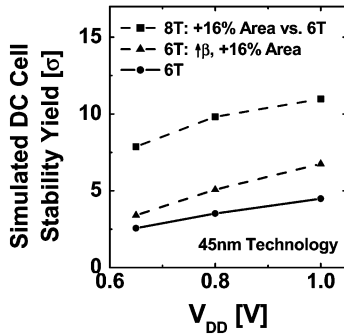


Fig. 4. Stability margins of an 8T cell can be dramatically improved over that of a high-performance 6T cell even when the 6T cell size is grown to increase the cell beta ratio.

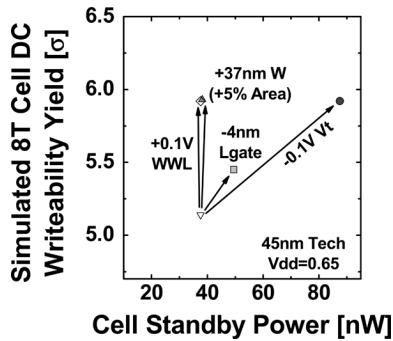


Fig. 5. Since 8T cell stability is not an issue, write margins can be improved by strengthening the pass-gate nFETs at the cost of write bit line leakage and/or cell area. Simulations assume minimum-strength storage inverters (e.g., min W , max L_{gate} , high V_T).

thus a more effective way to improve cell stability than simply growing a conventional 6T cell.

Without read disturb concerns, there is no limit to the minimum β ratio in an 8T cell. To improve cell write margins and reduce cell area, it is desirable to minimize the width of the pull-down nFET. While this increases variation, a write margin improvement will generally be observed. Further write margin enhancement can be achieved by strengthening the pass-gate devices—either by lowering V_T , reducing gate length, increasing device width, or expanding WWL voltage swing. Since these techniques do not affect stability, 8T cells can simultaneously improve both stability and writeability yields. These techniques may, however, come at the cost of cell leakage (Fig. 5).

Depending on the balance between gate and subthreshold leakage current levels, migration from a 6T cell to an 8T cell at the same supply voltage may increase cell leakage somewhat as pass-gate leakage and the two additional read stack transistors offset the minimum-width, high- V_T pull-down nFETs and pull-up pFETs. On the other hand, this may be an issue since voltage scaling is enabled by 8T-SRAM, which reduces leakage currents. It should also be noted that due to asymmetry in the cell read stack, cell leakage is data-dependent.

Read performance in an 8T cell is determined by the strength of the two-transistor read stack. Due to layout restrictions, the top read transistor is generally of smaller width, and thus likely limits read current. Cell write performance will largely be determined by the pass-gate device strength, but may also be affected somewhat by asymmetric loading of the storage nodes

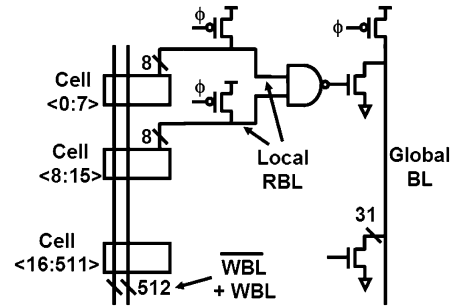


Fig. 6. The dual-port nature of the 8T cell enables separate optimization of the read (e.g., 8 bits per read bit line) and write paths (512 bits per write bit line) and simple local evaluation circuitry.

due to the read transistor; however, any slowdown will be mitigated by minimization of the pull-down nFET size. Without stability or write margin concerns, 8T cell performance—like regular logic—is limited only by normal power, performance, and area tradeoffs.

III. ARRAY DESIGN IMPLICATIONS

In contrast with conventional 6T-SRAM, 8T-SRAM arrays must consider both the dual-port nature of the cell as well as the elimination of column select functionality in the array. While separation of the read and write ports can create performance and array efficiency benefits, the lack of column select results in tradeoffs for some specific array applications.

A. Read and Write Port Separation

With separate read and write ports, control circuitry in the periphery of the array must be altered and can, in fact, be reduced over conventional 6T designs. First, port separation requires a second set of WL drivers, which adds to the area of the array. Whereas the write WL driver is largely similar to standard WL drivers used in 6T arrays due to similar capacitive loading, the read WL driver can be significantly reduced in size due to the single-ended cell read stack.

At the same time, however, with separate read and write word line signals, a read/write multiplexer is no longer needed at the local bit line level, which greatly simplifies local evaluation circuitry. Pass transistors normally used in 6T-SRAM to switch the local bit lines between write data drivers and the cell read stack can be eliminated. As a result, local write bit line control logic is not needed and only local read sense amplifier logic is required. Especially for high performance arrays that utilize short local bit line lengths, reduction of the local evaluation circuit area can have a sizeable impact on overall array area.

Since the local evaluation circuitry no longer needs to manage the cell write bit lines, global write drivers can instead be used to control the write data. In effect, read and write paths can be independently optimized by sharing the read and write bit lines across different numbers of bits. In this work (Fig. 6), the write bit line is shared across 512 bits to improve array efficiency by globally amortizing the write data driver area. The read bit line, however, is shared across only 8 bits, which, combined with a hierarchical sensing scheme, helps to ensure a high-speed read

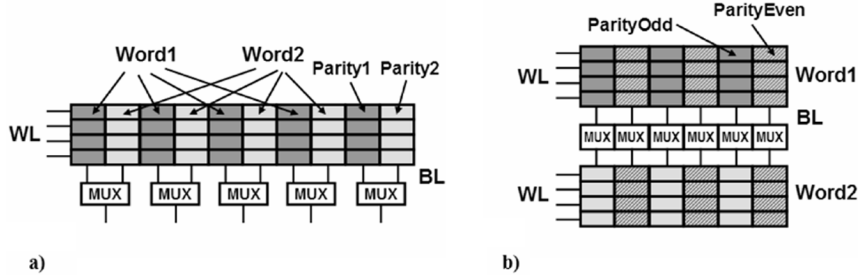


Fig. 7. (a) Traditional 6T floorplans, in which column select enables physical interleaving of bits from different words. (b) 8T floorplan, in which all bits of each word are spatially adjacent. Additional parity (as shown) or ECC bits are needed to prevent multi-bit soft errors.

path. Thus, 8T-SRAM enables simultaneous optimization of the read and write paths for performance and area.

B. Elimination of Column Select

While the 8T cell removes read stability concerns, cell disturbs can also occur in unselected columns during a write event. In this case, the write word line may be turned on while the write bit lines (held high) are relied upon to ensure cell stability—a situation identical to a read disturb in a 6T cell. While it is possible to optimize an 8T cell to withstand such write disturbs, any cell stability advantage would be lost. Instead, this issue must be addressed by the array organization by entirely prohibiting the column select condition in an 8T array.

Traditionally, column select functionality can be used to improve array efficiency by multiplexing adjacent columns into shared sense amplifiers. The cost includes active power, since multiple columns are read in a single event, and some performance, since the multiplexer has a finite delay. Column select also enables protection from multi-bit soft error events as bits from different words can be physically interleaved to ensure that a multi-bit error can affect at most one bit per word with high probability—an error that can be easily detected or corrected with simple parity checking or error correcting codes (ECC). Partial word writes, in which it may be desirable to update only a small portion of the bits sharing a single word line, may also be facilitated by the ability to perform column select. Each of these conditions must be addressed by alternative means in the design and organization of 8T-SRAM.

To avoid column select, an 8T array should be floorplanned so that all bits in a word are spatially adjacent (Fig. 7(b)). The number of cells sharing a write word line is thus generally limited by the word length desired by the array architecture. It should be noted that this limitation applies only to the write word line whereas the read word line could be shared across multiple words. Such a floorplan may increase the wiring overhead to properly multiplex the array output, but array efficiency can likely be maintained as column decode circuitry can be eliminated. Essentially, this column circuitry is simply moved to control the write word line. Active power in the 8T array can thus be reduced because only those columns that need to be accessed will switch. There is no unnecessary reading of unselected columns as would occur in a 6T array with column select since these columns reside on a separate write word line.

TABLE I
WITHOUT PHYSICAL BIT INTERLEAVING, PARITY OR ERROR CORRECTION CODES CAN INSTEAD BE INTERLEAVED (WHICH INCREASES BIT OVERHEAD) TO ACHIEVE RESILIENCY TO MULTI-BIT SOFT ERROR EVENTS

	# ECC bits	# Parity bits
Multi-bit SEU protection with column select (e.g. 6T-SRAM)	$2 + \log_2 N$	1
2-bit SEU protection without column select (e.g. 8T-SRAM)	$2 \times (1 + \log_2 N)$ interleaved	2 interleaved

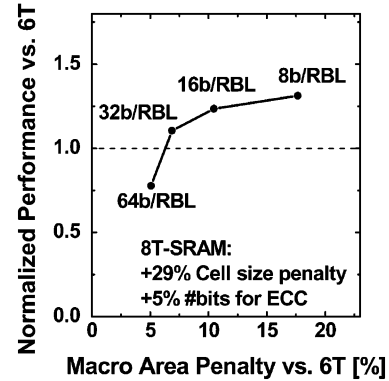


Fig. 8. Despite a larger cell and the lack of column select, 8T array area can be within $\sim 7\%$ of 6T at equal simulated performance due to improved array efficiency.

Since the storage element in an 8T cell is still comprised of CMOS inverters, there is no fundamental difference in soft error rate from a 6T cell. However, cell transistor sizing plays a role as smaller inverter devices and the additional asymmetric read stack alters the single-bit soft error rate. Since bits from different words in 8T-SRAM cannot be physically interleaved, protection from multi-bit soft error events must instead be achieved by interleaving the parity or ECC code as shown in Fig. 7. Table I shows an example for protection from soft errors affecting two adjacent bits. Separate codes can be used for the odd and even bits of the word to afford comparable resilience to multi-bit errors as the physical interleaving of bits. An area penalty must be incurred over 6T arrays, however, as the number of bits needed to store the parity or ECC code increases. However, depending on the data word length, the extra bit penalty can be small for ECC ($< 5\%$ versus 6T arrays for a 128 bits word) and nearly negligible for parity. Such interleaving of the ECC or parity codes

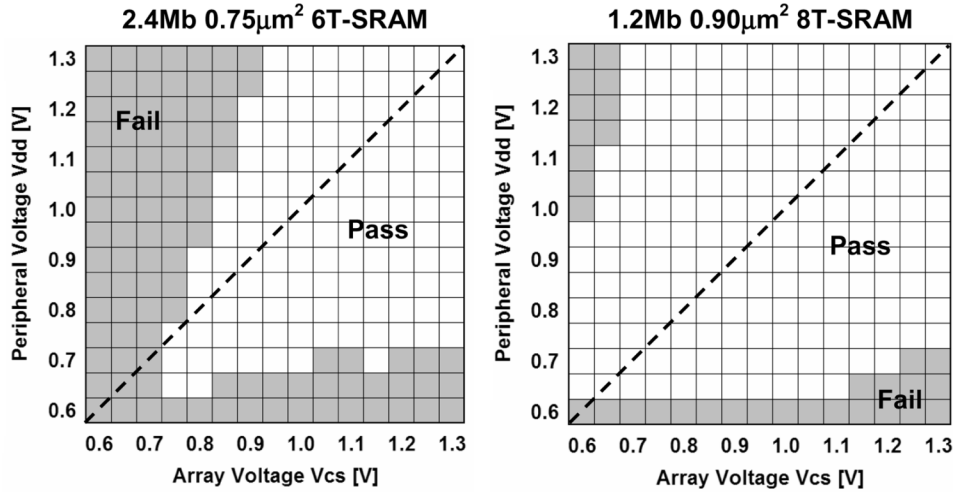


Fig. 9. In slow-speed testing, a 65 nm 8T-SRAM yield monitor shows improved low-voltage functionality as compared with 6T-SRAM down to the V_{dd} limit of the peripheral logic (~ 0.6 V).

can be extended to handle soft error events of greater than two bits. For arrays that only use parity checking, the bit penalty incurred can remain quite small, but if ECC is required, then the penalty incurred is larger.

For specific applications, systems requirements may dictate the need for partial-word writes. While this likely does not affect a large number of arrays and could be potentially be eliminated by systems architecture changes, 8T-SRAM can be modified for such functionality even without column select techniques. One method to achieve this would be to segment the word line to the partial-word length. Alternatively, a read-modify-write scheme [10], in which a read always precedes a write to combine the new and old data bits, can mimic partial-word write operations with minimal area penalty.

With all the aforementioned changes to array design needed to implement 8T-SRAM, the overall effect is that improved array efficiency mitigates area penalties associated with a larger cell, an extra WL driver, and added ECC bits. As a result, 8T array area can be competitive (+7% at equal performance) with that for 6T (Fig. 8). Higher speed arrays with larger 6T cells can show even smaller area penalties as the array efficiency for such arrays is usually low to begin with, thus minimizing the impact of the larger cell.

IV. YIELD AND PERFORMANCE ENHANCEMENT

Due to “ideal” read stability and improved writeability of the 8T cell, yield at low operating voltages can be enhanced. This improved variability tolerance can also be translated into improved performance and power. Furthermore, 8T-SRAM provides the capability of 1R1W dual-port operation, which can improve systems-level performance.

Measured hardware in a 65 nm SOI technology demonstrates the improved variability tolerance and minimum operating voltage of 8T-SRAM as compared with 6T-SRAM (Fig. 9). The yield of large (> 1 Mb) arrays under slow speed testing is plotted as a function of both the array supply voltage, V_{cs} , and the supply voltage of the peripheral circuits, V_{dd} , for a

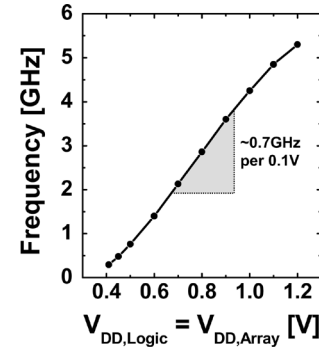


Fig. 10. A high-performance 32 kb 8T-SRAM subarray operates at 5.3 GHz at a single 1.2 V supply and 295 MHz at a single 0.41 V supply.

0.75 μm^2 6T cell and a 0.9 μm^2 8T cell designed with the same ground rules for similar performance. The 6T array shows a strong dependence on $V_{cs} > V_{dd}$, has a steep yield roll-off for V_{cs} less than 0.95 V, and, in general, has very low yield for V_{cs} less than 0.75 V. The 8T array, on the other hand, has no need for $V_{cs} > V_{dd}$ and yields well to below $V_{cs} = 0.6$ V—likely limited by array peripherals. While the specific arrays evaluated were of different sizes (2.4 Mb for 6T, 1.2 Mb for 8T), the Schmo plots demonstrate the fundamental benefit of the 8T cell: it removes the need for a second supply voltage to achieve sufficient yield.

The same 0.9 μm^2 8T cell was placed into a high-performance array design [6], which adheres to all of the design constraints as described in the previous section. Array performance was optimized as discussed with the additional introduction of peripheral circuits designed in limited switch dynamic logic (LSDL) [11] and a gated diode sense amplifier [12]. Fig. 10 shows that while the array can perform at 5.3 GHz at 1.2 V, it is also able to function down to very low voltages without the need for secondary or dynamic power supplies. High frequency operation of 295 MHz at $V_{dd} = V_{cs} = 0.41$ V is enabled by the incorporation of an 8T cell. Cell optimization techniques as previously described were used to dramatically improve array performance at these low voltages. Reducing both the gate length

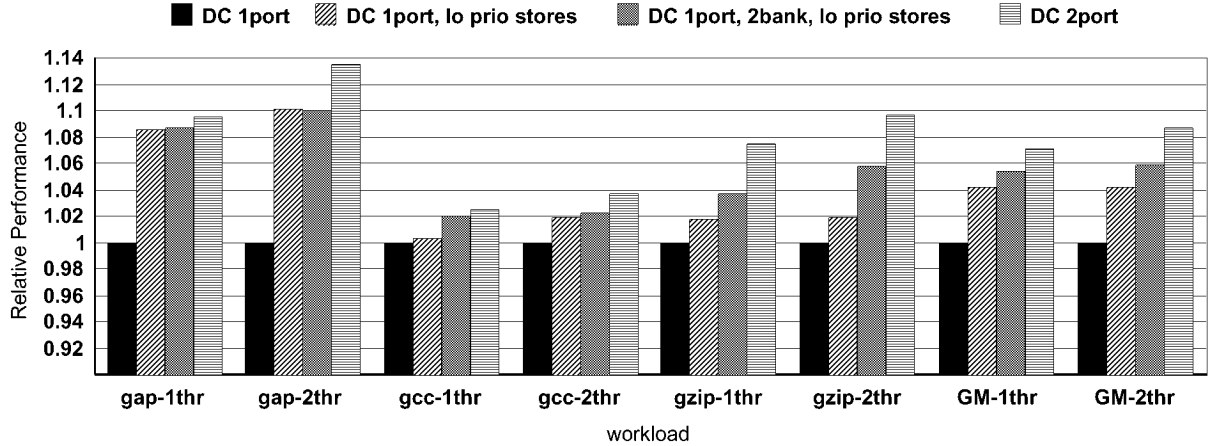


Fig. 11. Predicted data cache performance for three representative workloads as well as the geometric mean (GM) of 12 SPECint2000 workloads.

and threshold voltage of write pass-gate and read stack transistors improves cell writeability and read performance, which enhances low-voltage operation. Scaling the supply voltage from 1.2 V to 0.41 V results in a dramatic leakage current reduction of over 60x.

In addition to providing potential for improved array latency, the 8T cell also enables 1R1W dual-port operation, which can offer systems-level performance benefits. Fig. 11 shows the predicted performance of a data cache for a Power 5-like processor [13]. A single-port cache results in conflicts between processor loads, stores, and linefills (when data is returned from the L2 cache). Performance can be improved by reducing the priority of store operations—thus changing the priority order for cache operations from linefills-stores-loads to linefills-loads-stores. Further improvements can be achieved by implementing the cache with two banks, in which each can perform an independent operation. Address conflicts must be resolved, however, which could create significant additional logic complexity. A two-port design as enabled by the 8T cell is the simplest way to minimize conflicts between cache operations. Fig. 11 shows that such a design provides the optimum performance across all workloads with an average improvement in systems performance over the single-port base case of approximately ~7%. When multiple threads are assumed to run on the processor, a higher throughput and cache miss rate increases the bandwidth needed to supply data to the cache. In such a case, the benefit of a dual-port cache is enhanced.

V. TECHNOLOGY SCALING TRENDS

8T-SRAM is more scalable than traditional 6T-SRAM due to improved variability tolerance. To limit variability, scaling of device dimensions begins to saturate in 6T cells; however, devices in 8T cells can continue to scale. Thus, the cell size penalty incurred by 8T cells at the 65nm node (20% versus high performance 6T cells) can be expected to decrease with technology and/or voltage scaling. Scaling beyond the 32nm node, which will place severe scaling limitations on 6T cells, could see a crossover point in which 8T cells could, in fact, be smaller than 6T counterparts despite the addition of two transistors.

The precise scaling benefit provided by the 8T cell depends on read current requirements and the degree of variability in a technology. In a 6T cell, transistor sizes may need to remain large as technology scales due to variability concerns. While this could be detrimental to cell size, read current will be high. 8T cell size comparison at such constant read current would thus require large read stack transistors, which reduces the perceived scaling advantage. If product specifications allow for scaling of the cell read current with the technology node, then the 8T scaling benefit can be enhanced. Additionally, low power technologies that require scaled operating voltages will be more susceptible to variability, which further augments the 8T benefit.

VI. CONCLUSION

The 8T cell as proposed in this work is especially attractive for high-performance arrays (e.g., first-level cache in a microprocessor) as performance tradeoffs needed to enable the use of 6T cells in such applications can be severe. In addition, the small bit count and lower array efficiency of such arrays minimizes the impact of the larger 8T cell footprint. Furthermore, the benefits of dual-port operation are maximized in those arrays closest to the microprocessor core.

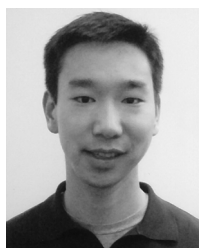
In summary, 8T-SRAM can provide exceptional variability tolerance as compared with traditional 6T-SRAM cell designs. This eliminates the need for secondary or dynamic power supplies and enable low-voltage operation. While some new design techniques may be needed for array-level implementation, in the end, the 8T cell provides a simple solution for SRAM stability and writeability that can be achieved without significant area penalty.

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REFERENCES

- [1] A. J. Bhavnagarwala *et al.*, "The impact of intrinsic device fluctuations on CMOS SRAM cell stability," *IEEE J. Solid-State Circuits*, vol. 36, no. 4, pp. 658–665, Apr. 2001.
- [2] J. Davis *et al.*, "A 5.6 GHz 64 kB dual-read data cache for the POWER6™ processor," in *IEEE Int. Solid-State Circuits Conf. (ISSCC) Dig. Tech. Papers*, 2006, pp. 622–623.
- [3] A. J. Bhavnagarwala *et al.*, "A transregional CMOS SRAM with single, logic V_{DD} and dynamic power rails," in *Symp. VLSI Circuits Dig.*, 2004, pp. 292–293.
- [4] K. Zhang *et al.*, "A 3-GHz 70 Mb SRAM in 65nm CMOS technology with integrated column-based dynamic power supply," in *IEEE Int. Solid-State Circuits Conf. (ISSCC) Dig. Tech. Papers*, 2005, pp. 474–475.
- [5] L. Chang *et al.*, "Stable SRAM cell design for the 32nm node and beyond," in *Symp. VLSI Technology Dig.*, 2005, pp. 128–129.
- [6] L. Chang *et al.*, "A 5.3GHz 8T-SRAM with operation down to 0.41 V in 65 nm CMOS," in *Symp. VLSI Circuits Dig.*, 2007, pp. 252–253.
- [7] K. Takeda *et al.*, "A read-static-noise-margin-free SRAM cell for low-VDD and high-speed applications," *IEEE J. Solid-State Circuits*, vol. 41, no. 1, pp. 113–121, Jan. 2006.
- [8] B. Calhoun and A. Chandrakasan, "A 256 kb sub-threshold SRAM in 65 nm CMOS," in *IEEE Int. Solid-State Circuits Conf. (ISSCC) Dig. Tech. Papers*, 2006, pp. 628–629.
- [9] E. Seevinck *et al.*, "Static-noise margin analysis of MOS SRAM cells," *IEEE J. Solid-State Circuits*, vol. 22, no. 5, pp. 748–754, Oct. 1987.
- [10] C. A. Adams and A. G. Aipperspach, "Methods and apparatus for accessing memory," U.S. Patent 7,239,559, Jul. 3, 2007.
- [11] R. Montoye *et al.*, "A double precision floating point multiply," in *IEEE Int. Solid-State Circuits Conf. (ISSCC) Dig. Tech. Papers*, 2002, pp. 336–337.
- [12] W. K. Luk and R. H. Dennard, "Gated diode amplifiers," *IEEE Trans. Circuits and Systems II: Expr. Briefs*, vol. 52, no. 5, pp. 266–270, May 2005.
- [13] B. Sinharoy *et al.*, "POWER5 system microarchitecture," *IBM J. Res. Devel.*, vol. 49, no. 4/5, pp. 505–521, Jul./Sep. 2005.



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Robert K. Montoye (S'81-M'89) holds a B.S. degree in physics and M.S. and Ph.D. degrees in computer science, all from the University of Illinois.

Joining IBM in 1983, he designed and implemented the RS/6000 floating-point unit. After pursuing interests outside IBM from 1990 to 1995, he returned to IBM to focus on finding a lower supply circuit family with state-of-the-art performance and its impact on overall microarchitecture and architecture. He is a member of the IBM Academy of Technology. He has published 25 technical papers

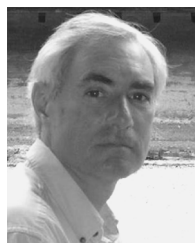
and holds more than 50 patents.



Yutaka Nakamura received the B.S. degree in mechanical control engineering from Waseda University, Tokyo, Japan.

He joined IBM Japan Ltd., at the Yasu plant, Shiga, Japan and worked on semiconductor device characterization and function testing. Then he moved to the Yasu Technology Application Laboratory and has worked on various kinds of memory circuit design, characterization, function testing and CAD setup for DRAMs in 4Mb to 64Mb generations, 4T/6T/8T SRAM, Pseudo-SRAM, NOR Flash,

Register File and also 4GHz Enhanced-DP CELL BE microprocessor circuit design. He is currently with IBM Japan's Global Engineering Solutions and responsible for Spin-Torque MRAM research and development.



Kevin A. Batson received the B.S. and M.S. degrees in electrical engineering in 1989, 1993, respectively, from Polytechnic University in New York City.

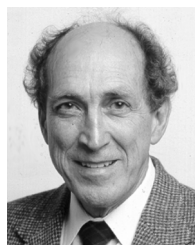
He joined IBM Microelectronics in 1993 as a SRAM Circuit Design Engineer. During his 14 years at IBM, he has designed ASIC SRAM arrays technology development test sites, Power PC microprocessor two port data caches, an 18 Mb CAM Chip and various stand-alone SRAM Chips. He holds 12 patents.



Richard J. Eickemeyer (M'87-SM'01) received the B.S. degree in electrical engineering from Purdue University, West Lafayette, IN, and the M.S. and Ph.D. degrees from the University of Illinois at Urbana-Champaign.

He is currently a Senior Technical Staff Member at IBM Corporation in Rochester, MN where he is the processor core performance team leader for IBM PowerPC servers and is working on a future processor design. Previously, he has worked on several different processor designs. His research interests are computer architecture and performance analysis. He has authored several papers and has been awarded 28 U.S. patents with others pending. He has been named an IBM Master Inventor.

Dr. Eickemeyer has received several IBM awards including two IBM Corporate Awards.



Robert H. Dennard (F'79) was born in Terrell, TX, in 1932. He received the B.S. and M.S. degrees in electrical engineering from Southern Methodist University, Dallas, TX, in 1954 and 1956 respectively, and the Ph.D. degree from Carnegie Institute of Technology, Pittsburgh, PA, in 1958.

He then joined IBM Research Division where his early experience included the study of new digital devices and circuits for logic and memory applications, and the development of advanced data communication techniques. Since 1963, he has been at the IBM

Thomas J. Watson Research Center, Yorktown Heights, NY, where he has been involved in microelectronics research and development from the early days onward. His primary work has been in MOS transistors and integrated digital circuits using them. In 1967, he invented the dynamic RAM memory cell used in most all computers today. With coworkers he developed the concept of MOS transistor scaling in 1972, which is often cited as a guiding principle for microelectronics. He was appointed an IBM Fellow in 1979. He has contributed numerous papers on advances in CMOS technology and on prospects and challenges of scaling that technology to very small dimensions.

Dr. Dennard is a Fellow of IEEE. He received the IEEE Cleo Brunetti Award in 1982 and the Edison Medal in 2001. He is a member of the National Academy of Engineering and the American Philosophical Society, and he has received many honors including the National Medal of Technology in 1988 and induction into the National Inventors Hall of Fame in 1997.



Wilfried Haensch received the Ph.D. in 1981 from the Technical University of Berlin, Germany in the field of theoretical solid state physics.

After a post doc position at Indiana University, where he worked on many particle modifications of the Boltzmann transport equation with Gerald Mahan, he joined the University of Hamburg in 1983 to continue his work on many body effects in electron transport. In 1984 he joined SIEMENS corporate research in Munich to investigate high field transport in MOSFET devices. He developed a simplified hydrodynamic transport model that was implemented into the device simulator MINIMOS. He developed a complete 2D hot e-module that allowed the self-consistent evaluation of hot e effects on MOSFET degradation including the transport of carriers in the gate oxide and. In 1988 he joined the DRAM development team at the SIEMENS research lab to investigate new cell concepts. In 1990 he joined the DRAM alliance between IBM and SIEMENS to develop quarter micron 64M DRAM. In this function he was involved with device characterization of shallow trench bounded devices and cell design questions. In 1996 he moved to a manufacturing facility to build various generations of DRAM. His main function was to transfer technologies

from development into manufacturing and to guarantee a successful yield ramp of the product. In 2001 he joined IBM T. J. Watson Research Center to lead a group for novel devices and applications. He is currently responsible for the 22 nm device design and other explorative technology options.



Damir Jamsek received the M.S. and Ph.D. degrees in electrical and computer engineering from Syracuse University in 1987 and 1990, respectively.

He joined the IBM Austin Research Laboratory in 1997 as a Research Staff Member and has managed a department engaged in VLSI research on high-speed arithmetic circuits and SRAM memory structures. His research has included design and verification of hardware, tools for analysis and simulation of VLSI circuits and most recently the use of massively parallel multithreaded compute resources to model and predict device and circuit behavior for 45nm and beyond technology nodes.