Scan design with shadow flip-flops for low performance overhead and concurrent delay fault detection

Sébastien Sarrazin[1], Samuel Evain[1], Lirida Alves de Barros Naviner[2], Yannick Bonhomme[1], Valentin Gherman[1]
[1] CEA, LIST,
PC 172, F-91191 Gif sur Yvette CEDEX, France
[2] Telecom ParisTech,
46 rue Barrault, 75634 Paris CEDEX13, France

***Abstract*—This paper presents new scan solutions with low latency overhead and on-line monitoring support. Shadow flip-flops with scan design are associated to system flip-flops in order to (a) provide concurrent delay fault detection and (b) avoid the scan chain insertion of system flip-flops. A mixed scan architecture is proposed which involves flip-flops with shadow scan design at the end of timing-critical paths and flip-flops with standard scan at non-critical locations. In order to preserve system controllability during test, system flip-flops with shadow scan can be *set* in scan mode and *selectively reset* before switching to capture mode. It is shown that shadow scan design with asynchronous *set* and *reset* may have a lower latency overhead than standard scan design. A shadow scan solution is proposed which, in addition to concurrent delay fault detection, provides simultaneous scan and capture capability.**

Keywords—shadow scan; dynamic variations; delay faults; monitoring; concurrent fault detection

I. INTRODUCTION

Energy efficiency, usually measured as performance per watt, is an important figure of merit for mobile devices. Power gating or dynamic voltage and frequency scaling (DVFS) are effective approaches to maximize energy efficiency. Power gating allows to switch-off idle modules whereas DVFS saves energy based on dynamic adjustments of the supply voltage and clock frequency. Such adjustments are limited by the necessity to introduce temporal safety margins to absorb dynamic latency variations that may be induced by wear-out or voltage and temperature variations [4]. Latency variations can be sensed with the help of on-die sensors [13][24], but these are expensive in terms of calibration time and inefficient in handling within-die variations [3][5].

On-line monitoring based on concurrent delay fault detection is a natural approach to reduce safety margins for aggressive DVFS scaling [2][3][5][7][16][19]. Here, we consider a concurrent fault detection scheme in which a shadow flip-flop (FF) is associated to each system FF placed at the end of timing-critical paths [5][16]. In order to enable error prediction and prevent data-path metastability, the shadow FFs must have a higher probability to be affected by delay faults than the corresponding system FFs [5][16]. One way to achieve this is to select shadow FFs with a larger setup time than system FFs. Care should be taken since the additional setup time may affect circuit latency.

On the other hand, product quality requires the execution of high quality manufacturing test and diagnosis. Standard scan is a widely employed technique to effectively address these issues [25]. Unfortunately, standard scan design is also a source of latency overhead since the system FFs need to be replaced with slower scan FFs.

Here, shadow scan solutions are proposed to reduce the latency overhead of scan and concurrent delay fault detection. This solution is applied to system FFs located at the end timing-critical paths in order to avoid their scan chain insertion. A mixed scan architecture may be obtained if standard scan design is applied to the remaining FFs.

During test, shadow scan design does not affect observability since test responses can still be captured and scanned out. 0-controllability of the system FFs with shadow scan is achieved with the help of a *selective reset* operation performed before the system switches to capture mode. A system FF is reset only if the last value scanned in the associated shadow FF is logic 0. Full controllability can be ensured if, in addition to the *selective reset* operation, the system FFs with shadow scan are *set* in scan mode. The *set* operation can be controlled by the *scan enable* signal. It is shown that shadow scan design with asynchronous *set* and *reset* may have a lower latency overhead than standard scan design.

A special shadow scan design is presented which, besides concurrent delay fault detection, allows to perform simultaneous scan and capture operations. This feature allows to take real-time snapshots at consecutive clock cycles without halting the system. This is not possible with existing solutions based on enhanced or isolated serial scan architectures [1][11][14]. The proposed shadow scan solution can be used to enhance circuit observability during software-based self-testing (SBST) [18][12]. The impact of using concurrent delay fault detection during SBST has already been shown to increase the coverage of transition delay faults [8], but the method introduced here also provides a better observability of the stuck-at faults.

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On-line reuse of design-for-testability resources was proposed in [15] in order to provide concurrent soft error detection. This solution requires the existence of an enhanced scan infrastructure and does not ameliorate latency overhead. In [23], shadow FFs are used to transfer the scan multiplexer latency from the input to the output of the scan FFs placed at the end of timing-critical paths. Latency savings can only be obtained if there is no scan FF which is both source and sink of timing-critical paths. The shadow FFs are used only in test mode and do not contribute to on-line monitoring.

In Section II and Section III, two shadow scan solutions are presented which enable concurrent delay fault detection for on-line monitoring and different degrees of controllability of the system FFs during test. Latency overhead reductions are analyzed in Section IV. A shadow scan design with simultaneous scan and capture capability is discussed in Section V. Concluding remarks are grouped in Section VI.

II. Shadow Scan Design with Concurrent Delay Fault Detection and Partial Test Controlability

This section presents a first shadow scan solution which enables concurrent delay fault detection during system mission together with system observability and 0-controllability during test.

Figure 1 illustrates a system FF with a shadow FF (FF*) that can be inserted into a scan chain with the help of a multiplexer controlled by a *scan enable* signal. In capture mode, the *scan enable* signal is set to logic 0 and the shadow and system FFs capture the same logic values. The path which arrives to the shadow FF has a larger latency. The latency difference between the paths arriving at the shadow and system FFs is equal to the multiplexer latency plus the difference between the setup times of the two FFs. During system mission, if the *D* signal is affected by a delay fault with increasing amplitude, the shadow FF is expected to be the first that captures a wrong value. The *xor*-gate allows to detect any mismatch between the two FFs. In this way, a warning is generated and action can be taken before errors are generated. Moreover, the shadow FF will be affected by metastabillity before the system FF which reduces the necessity of metastability detectors [5].

All delay faults able to propagate to the shadow FF but with insufficient amplitude to reach the system FF can be detected [16]. The size of the detectable delay faults can be increased by choosing a shadow FF with a larger setup time or a multiplexer with increased latency. This may privilege the selection of shadow FFs with smaller hardware and power overhead.

During test, the shadow FF allows to observe the circuit under test (CUT) since (a) it receives the same functional input as the system FF and (b) its content can be scanned out. The *xor*-gate allows to check whether the test stimuli shifted into the shadow FF are really applied to the CUT by the associated system FF.

In scan mode, the *scan enable* signal is set to logic 1 and

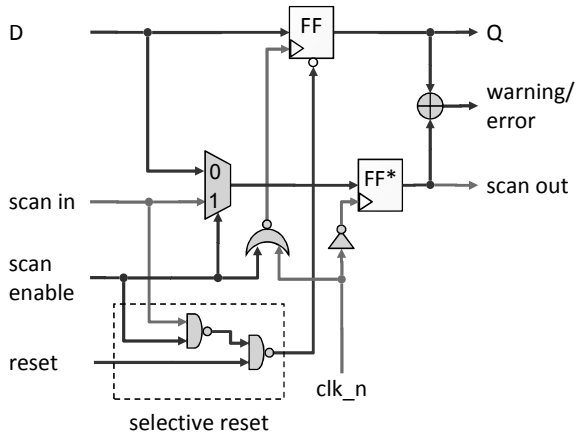

Figure 1. Partially controllable system FF with shadow scan FF (FF*) that enables concurrent delay fault detection.

the clock of the system FF is blocked with the help of a *nor*-gate under the assumption that the system FF is positive edge-triggered. The system FF can be controlled to 0 with the help of a *selective reset* operation performed during the last clock cycle in scan mode. This operation is controlled by the last value scanned in the shadow FF before the capture mode and it is implemented with the help of two *nand*-gates driven by the *scan in*, *scan enable* and *reset* signals, under the assumption that the *reset* signal is active high. In capture mode, the *reset* signal can reach the system FF since the *scan enable* signal is set to logic 0, while, in scan mode, the system FF can be reset only if the *scan in* signal is set to logic 0.

Glitches on the *scan enable* signal are usually electrically filtered by the high load capacitance of the signal distribution wires. They may also be logically and electrically filtered by the *nor*-gate. Glitches on the *scan in* and *scan enable* signals cannot reach the *reset*-input of the system FF as long as the *reset* signal is inactive.

During test, 1-controlability of the system FF can be ensured only with the help of sequential automated test pattern generation since this FF is not directly inserted into a scan chain.

In order to evaluate the impact on testability of the proposed shadow scan solution, we considered *ITC'99* benchmark circuits [26] with a mixed scan architecture, as shown in Figure 2. Shadow scan design was applied only to a fraction of all system FFs starting with those located at the end of timing-critical paths. Sequential test patterns were generated with Synopsys TetraMAX for test-equivalent versions of these circuits where each shadow FF was replaced by three virtual test points [10], as indicated in Figure 3. Two observation points are connected to virtual primary outputs (POs) and one control point is driven by a virtual primary input (PI). The observation points are used to model the observability gain enabled by the shadow FF and the *xor*-gate in Figure 1. The control point is implemented with the help of a 2-input *and*-gate and provides 0-controllability equivalent to that obtained with the selective reset operation. In reality, each value used to drive the virtual PI in capture mode

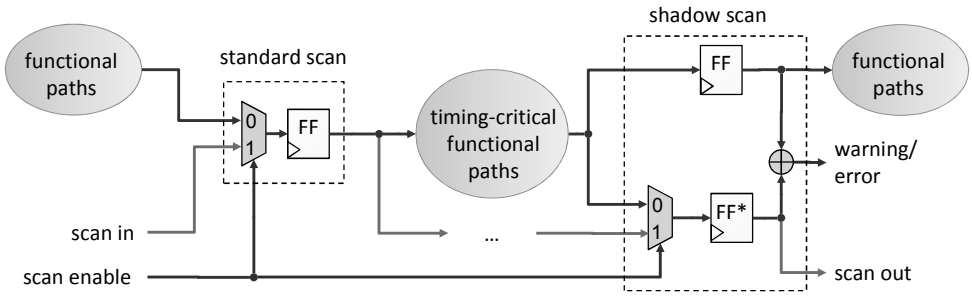

Figure 2. Mixed scan architecture with standard and shadow scan design.

should be scanned in the shadow FF. For this reason, the state of a system FF with shadow scan should be blocked in scan mode.

For each benchmark, we considered (a) the original version, (b) a standard scan version and (c) a mixed scan version with 10% shadow scan and 90% standard scan. Table I reports the obtained stuck-at fault coverage (FC) and the total number of test patterns which also includes the initialization patterns. Compared to the standard scan versions, the mixed scan versions provided the same FC only for *b06*. For six circuits, the FC was reduced by up to 3% and, for the remaining seven circuits, the FC reduction was between 6% and 9%. The average FC reduction was 4.5%. For mixed scan architectures with 20% shadow scan, an average FC reduction of 10.5% was obtained.

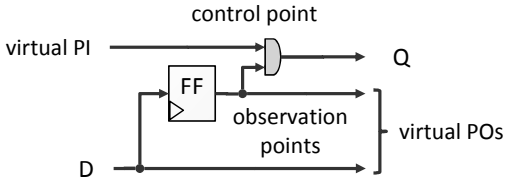

Figure 3. Test equivalent version of the FF with shadow scan in Figure 1.

TABLE I. IMPACT ON TESTABILITY OF THE SHADOW SCAN DESIGN IN FIGURE 1

ITC'99 benchmark circuits	original version (no scan design)		10% shadow scan + 90% standard scan		full standard scan	
	# test patterns	fault coverage	# test patterns	fault coverage	# test patterns	fault coverage
b01	151	85%	40	97% (-3%)	16	100%
b02	58	94%	31	97% (-3%)	12	100%
b03	69	52%	52	93% (-7%)	33	100%
b04	366	83%	86	97% (-1%)	62	98%
b05	15	9%	138	94% (-3%)	97	97%
b06	76	92%	39	99% (0%)	15	99%
b07	7	3%	126	98% (-2%)	79	100%
b08	18	3%	103	94% (-6%)	60	100%
b09	9	4%	74	94% (-6%)	45	100%
b10	118	80%	149	93% (-7%)	52	100%
b11	108	60%	284	94% (-6%)	103	100%
b12	20	12%	235	92% (-8%)	198	100%
b13	59	21%	134	91% (-9%)	60	100%
b14	1631	55%	1290	97% (-2%)	833	99%

Due to the limited controllability, the FC and the test sequence length may be seriously affected by the increasing ratio of FFs with shadow scan. A shadow scan solution that provides better controllability is presented in the following section.

III. SHADOW SCAN DESIGN WITH CONCURRENT DELAY FAULT DETECTION AND FULL TEST CONTROLABILITY

Figure 4 shows a shadow scan design that enables full controllability of the system FF at the cost of latency as compared to the solution in Figure 1. The system FF is set in scan mode to logic 1 with the help of the *scan enable* signal and can be reset if a logic 0 value needs to be applied to the CUT. This can be done with the help of a pulse applied to the *reset*-input during the transition phase from scan mode to capture mode, as illustrated in Figure 5. Usually, this transition phase is sufficiently long in order to provide enough time to the *scan enable* signal to propagate along low speed wires. Due to the *nand*-gate which masks the *reset* signal, the system FF can be reset only if the state of the shadow FF is logic 0. This *selective reset* operation transfers the last value scanned in the shadow FF to the system FF.

In Figure 4, glitches on the *scan out* signal cannot reach the *reset*-input of the system FF as long as the *reset* signal is inactive. As before, glitches on the *scan enable* signal are expected to be electrically filtered by the high load capacitance of the signal distribution wires.

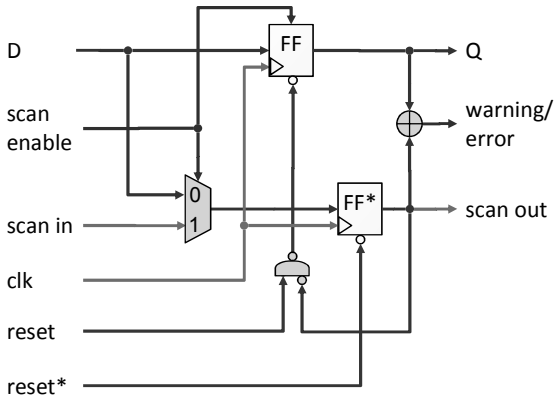

Figure 4. Fully controllable system FF with shadow scan FF (FF*) that enables concurrent delay fault detection.

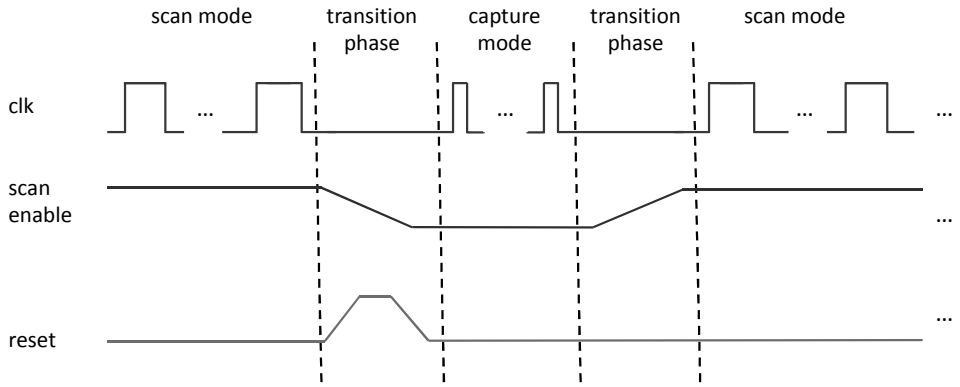

Figure 5. Test application sequence with a reset pulse during the transition phase from scan mode to capture mode.

Apart from the necessity to activate the reset signal during the transition phase from scan mode to capture mode, test sequences can be scanned in, applied and scanned out as in the case of full standard scan design. During test, the observability of the logic cone that drives the *D* signal in Figure 4 is ensured by the shadow FF. All stuck-at faults that affect the output and the inputs of the system FF, except for the *D*-input, are (a) implicitly controlled with the help of the set and selective reset operations and (b) implicitly observed via the *warning* signal. Test patterns with at least two capture clock cycles are necessary to test stuck-at faults on the *D*-input.

In Figure 4, a stuck-at 0 fault on the *set*-input of the system FF or a stuck-at 0 fault on the wire that connects the *nand*-gate to the shadow FF can affect only the application of test patterns that need to be scanned in. Stuck-at faults on the wire that connects the *nand*-gate to the shadow FF can be observed via the *warning* signal only at the end of the first capture clock cycle of a test pattern and only if the *reset* signal is activated as shown in Figure 5.

Warning signals from several FFs with shadow scan can be collected with the help of an or-tree as shown in Figure 6. Once the *global warning* signal becomes equal to logic 1, it is stuck until it is reset with the help of the *refresh* signal.

Each time the *reset* signal is activated as indicated in Figure 5, all warning signals should become equal to logic 0. Consequently, all stuck-at 1 faults on the paths connecting the *warning* signals to the output of the or-tree in Figure 6 are tested implicitly. In order to test the stuck-at 0 faults on these paths, no pulse on the *reset* signal should be applied and appropriate test patterns with a logic 1 value in all except one shadow FF are required. Since the *reset* signal is not activated, such a pattern implicitly tests the stuck-at 1 fault on the *reset*-input of the *nand*-gate in Figure 4 if a 0 logic value is scanned in the shadow FF.

In Figure 6, the scan FF may be clocked with the same clock signal used for system flip-flops with standard or shadow scan. If the or-tree is pipelined and the pipeline registers have standard scan design, the number of additional patterns required to test the circuitry in Figure 6 has an upper bound equal to the fan-in of the largest logic cone in the first pipeline stage. Certain stuck-at 0 and slow-to-rise faults affecting the or-tree may be tolerated if their only effect is to make inaccessible a user defined ratio of *warning* signals. During manufacturing test, slow-to-rise faults on the paths along which *warning* signals are propagated cannot be tested based on a *broadside* scheme [21] since the output of the *xor*-gate in Figures 1 and 4 becomes low in capture mode. Slow-to-fall faults inside the or-tree can only affect system reactivity and can be tolerated if their amplitude does not exceed a user defined limit.

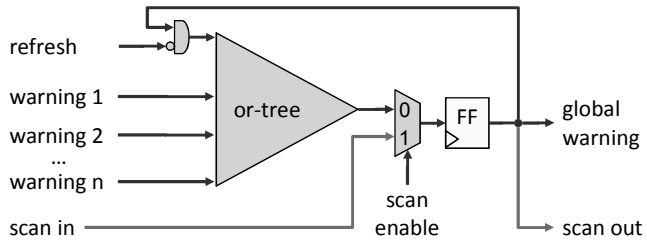

Figure 6. Gathering of *warning* signals [19][20].

Glitches on the *warning* signals can be filtered by the or-tree via logical or electrical masking and by the output FF or by the eventual pipeline registers in the or-tree via latching-window masking [22]. Latching-window masking is especially effective if the or-tree does not contain timing-critical paths.

The *reset** signal in Figure 4 is used to reset the shadow FF each time the system FF needs to be reset during system mission. This ensures that the *reset* signal is not masked and reaches the system FF and, implicitly, a coherent system state can be achieved after a global reset operation. The *reset** signal can also be used to reset the FFs with standard scan design.

The *reset** signal can be inferred from the *reset* signal with the help of an additional scan FF, as illustrated in Figure 7. After one clock cycle in capture mode, the state of the scan FF becomes logic 1 and the *reset** signal can be driven by the *reset* signal. During the transition phase from scan mode to capture mode, the *reset** is kept inactive if the state of scan FF is logic 0. A logic 1 value allows to test the wires

used to distribute the *reset** signal. Glitches on the *scan out* signal cannot propagate to the *reset** signal as long as the *reset* signal is inactive.

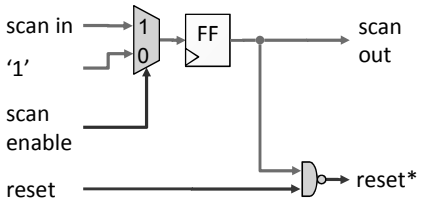

Figure 7. Generation of the *reset** signal from the *reset* signal under the assumption that *reset* is active high and *reset** is active low.

Observation 1

The shadow FFs illustrated in Figure 1 and Figure 4 allow concurrent detection of soft errors induced by transient faults which affect the system FF, the shadow FF or the upstream combinational logic [5][16]. To that end, the *xor*-gate output should be interpreted as an error and not as a warning signal.

Observation 2

The system FFs in Figure 1 and Figure 4 can be replaced with system latches without affecting system testability since these FFs are not inserted into scan chains. The resulting configuration remembers one solution proposed in [5] and enables latch-based design and system latency reduction. In a mixed scan architecture as sketched in Figure 2, the system FFs with shadow scan can be replaced with latches if min-delay constraints are fulfilled. The resulting architecture is different from the one presented in [17], as latches are only used to replace the system FFs with timing-critical incoming paths and no halving of the maximal working frequency is required. On the other hand, the approach proposed in [17] enables better soft-error detection.

IV. Latency Overhead Reductions

The shadow scan designs presented above are characterized by a lower latency overhead than standard scan design. As an example, Table II reports the best timing characteristics of some relevant types of positive edge-triggered FFs from TSMC N40LP library [27]. The latency overhead of the shadow scan solutions sketched in Figure 1 and Figure 4 can be inferred from the timing characteristics of the FFs with asynchronous set and/or reset reported in Table II. As long as concurrent fault detection is required, the comparison between shadow and standard scan solutions can be made without taking into account the latency and hardware overhead introduced by the presence of shadow FFs.

The FFs with asynchronous set and reset have a setup time between 3 and 4 times smaller than the standard scan FFs independently of the presence of a *reset* signal. Even if the clock-to-Q latency is increased, the sum between the maximal setup time and the maximal clock-to-Q time is sensibly lower in the case of the FFs with asynchronous set and reset. The higher latency of FFs with standard scan is due to the synchronous implementation of the scan operations, e.g. with the help of a multiplexer placed in front of the FFs.

The different distributions of the setup and clock-to-Q times in Table II provide more opportunities for timing optimization, which can be exploited during system synthesis. Thus, FFs with shadow scan can be used at locations with incoming timing-critical paths, while FFs with standard scan can be placed at the end of less critical paths especially if these are followed by timing-critical paths [23].

TABLE II. Timing Characteristics of Different Positive Edge-Triggered FFs from TSMC N40LP Library

positive edge triggered D flip-flops with:	cell width [μm]	rise time [ps]		fall time [ps]		maximal setup+ maximal clock-to-Q
		setup	clock-to-Q	setup	clock-to-Q	
asynchronous reset (DFCND1BWPLVT)	3.64	13	86	-3	95	108
asynchronous set and reset (DFCSND1BWPLVT)	4.06	11	82	7	100	111
standard scan 1 (SDFD4BWPLVT)	5.18	40	72	40	74	114
standard scan 2 (SDFD1BWPLVT)	4.06	36	72	28	86	122
standard scan and asynchronous reset (SDFCND2BWPLVT)	5.18	37	84	29	91	128

V. Shadow Scan Design for SBST and Concurrent Delay Fault Detection

Figure 8 illustrates a shadow scan design which, besides concurrent delay fault detection, provides simultaneous scan and capture capability. Here, the scan chain insertion of the shadow FF is ensured by a *xor*-gate instead of a multiplexer. In capture mode, the *scan enable* and *scan dump* signals are set to logic 0 in order to provide concurrent delay fault detection as in the previous shadow scan solutions.

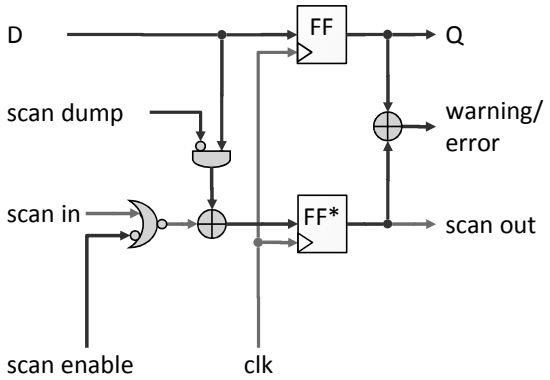

Figure 8. System FF with shadow scan FF (FF*) that enables concurrent delay fault detection and simultaneous scan and capture operations.

A scan and capture mode can be enabled if the *scan enable* signal is set to logic 1 and the *scan dump* signal is set to logic 0. In this mode, the shadow FF is connected to both *D* and *scan in* signals via the *xor*-gate. In this way, the shadow FF is able to sense system behaviour and simultaneously scan out the captured data at consecutive clock cycles

without halting the system. This is impossible with existing shadow scan solutions like enhanced or isolated serial scan architectures [1][11][14]. In this mode, the *warning* signal should be neglected since the logic states of the system and shadow FFs may be different.

A scan dump mode may be introduced if the *scan enable* and *scan dump* signals are set to logic 1. In this mode, the shadow FF is only connected to the *scan in* signal. This allows not only to unload, but also to load the shadow scan chains which, combined with one of the selective reset techniques presented in Sections II and III, can be employed to enable the control of the system FF during test.

Besides concurrent delay fault detection, this solution has the potential to ameliorate system observability during software-based self-test (SBST). Efficient SBSTs for control components in processor cores can be generated from formal verification routines [12]. Such routines mainly provide component controllability since they only need to be simulated. The challenge of transforming them into SBST routines is to make the internal processor state observable. It has been shown that the utilization of concurrent delay fault detectors during SBSTs can improve the observability of transition delay faults such that their test coverage can be ameliorated by up to 20% [8]. Unfortunately, concurrent delay fault detectors cannot be used to improve stuck-at fault observability.

This issue can be addressed with the help of the shadow scan design in Figure 8 since, in scan and capture mode, it allows to (a) continuously sense the functional data sampled by the system FFs with shadow scan and (b) scan out this data. A way to use the shadow scan chains during SBST is to connect their outputs to a multiple input signature register [6] [9] whose logic state may be compared with precalculated signatures once or several times during a test procedure.

VI. CONCLUSIONS

New shadow scan solutions have been presented to reduce the latency overhead of scan design and enable concurrent delay fault detection for on-line monitoring. During test, these solutions have negligible impact on system observability and ensure full controllability or 0-controllability of the system FFs with shadow scan with the help of set and selective reset operations. A shadow scan solution has been presented which, in addition to concurrent delay fault detection, allows to perform simultaneously scan and capture operations. This solution can be used to improve circuit observability during SBST.

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REFERENCES

[1] M. Abramovici, M.A. Breuer, A.D. Friedman "Digital Systems Testing and Testable Design," Revised printing, IEEE Press, 1990.

[2] M. Agarwal et al. "Circuit Failure Prediction and its Application to Transistor Aging," IEEE VLSI Test Symposium, 2007, pp. 277–286.

[3] D. Blaauw et al. "Razor II: In Situ Error Detection and Correction for PVT and SER Tolerance," ISSCC, 2008, pp. 400–622.

[4] S. Borkar "Designing Reliable Systems from Unreliable Components: the Challenges of Transistor Variability and Degradation," Micro 25, No. 6, 2005, pp. 10–16.

[5] K.A. Bowman et al. "Energy-Efficient and Metastability-Immune Resilient Circuits for Dynamic Variation Tolerance," J. Solid-State Circuits, January, 2009, pp. 49–63.

[6] R. David "Signature Analysis of Multi-Output Circuits," International Symposium on Fault-Tolerant Computing, 1984, pp. 366–371.

[7] P. Franco, E. J. McCluskey "On-Line Delay Testing of Digital Circuits," VLSI Test Symposium, 1994, pp. 167–173.

[8] V. Gherman et al. "Error Prediction based on Concurrent Self-test and Reduced Slack Time," DATE, 2011, pp. 1626–1631.

[9] S.Z. Hassan et al. "Parallel Signature Analysers–Detection Capability and Extensions," Computer Society International Conf., 1983, pp. 440–445.

[10] J.P. Hayes, A.D. Friedman "Test Point Placement to Simplify Fault Detection," Transactions on Computers, Vol. C-33, 1974, pp. 727–735.

[11] H.F. Ko, N. Nicolici "Combining Scan and Trace Buffers for Enhancing Real-time Observability in Post-Silicon Debugging," European Test Symposium, 2010, pp. 62-67.

[12] N. Kranitis et al. "Hybrid-SBST Methodology for Efficient Testing of Processor Cores," Design & Test of Computers, 25(1), 2008, pp. 64–75.

[13] T. Kim et al. "Silicon Odometer: An On-chip Reliability Monitor for Measuring Frequency Degradation of Digital Circuits," J. Solid-State Circuits, April, 2008, pp. 874–880.

[14] R. Kuppuswamy et al. "Full Hold-Scan Systems in Microprocessors: Cost/Benefit Analysis," Intel Technology Journal, vol.8, no.1, February, 2004, pp. 63–72.

[15] S. Mitra et al. "Robust system design with built-in soft-error resilience," Computer, Special Issue, 38(2), 2005, pp. 43–52.

[16] M. Nicolaidis "Time redundancy Based Soft-Error Tolerance to Rescue Nanometer Technologies," VLSI Test Symposium, 1999, pp. 86–94.

[17] M. Nicolaidis "GRAAL: a new fault tolerant design paradigm for mitigating the flaws of deep nanometric technologies," ITC, 2007, pp. 1–10.

[18] A.M. Paschalis, D. Gizopoulos "Effective Software-Based Self-Test Strategies for On-Line Periodic Testing of Embedded Processors," Trans. on CAD of Integrated Circ. and Syst., 24(1), January, 2005, pp. 88–99.

[19] B. Rebaud et al. "Timing slack monitoring under process and environmental variations: Application to a DSP performance optimization," Microelectronics Journal , Vol. 42, Issue 5 , 2011, pp. 718-732.

[20] D. Rossi, M. Omana, C. Metra "Transient fault and soft error on-die monitoring scheme," International Symposium on Defect and Fault Tolerance in VLSI Systems, 2010, pp. 391–398.

[21] J. Savir, S. Patil "Broad-Side Delay Test," Tran. on CAD of Integrated Circuits and Systems, Vol. 13, No. 8, 1994, pp. 1057–1064.

[22] P. Shivakumar at al. "Modeling the effect of technology trends on the soft error rate of combinational logic," International Conference on Dependable Systems and Networks, 2002, pp. 389–398.

[23] O. Sinanoglu "Eliminating Performance Penalty of Scan," International Conference on VLSI Design, 2012, pp. 346–351.

[24] A.K. Uht "Uniprocessor Performance Enhancement through Adaptive Clock Frequency Control," Trans. on Comp., Vol. 54, No. 2, February, 2005, pp. 132–140.

[25] M.J.Y. Williams, J.B. Angell "Enhancing Testability of Large Scale Integrated Circuits Via Test points and Additional Logic," Trans. on Computers, Vol. C-22, January, 1973, pp. 46–60.

[26] http://www.cad.polito.it/downloads/tools/itc99.html

[27] http://www.synopsys.com/dw/ipsearch.php?p=TCBN40LPBWPLVT