TECHNOLOGICAL INSTITUTE OF THE PHILIPPINES - MANILA
LOGIC CIRCUITS AND DESIGN
CPE 203 - CPE22S1

2 Bit Adder with LED and 7 Segment Display

SUBMITTED ON:
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Truth Table

A1	A0	B1	B0	C1 (Carry)	S1	S0	Binary Sum	Decimal
0	0	0	0	0	0	0	000	0
0	0	0	1	0	0	1	001	1
0	0	1	0	0	1	0	010	2
0	0	1	1	0	1	1	011	3
0	1	0	0	0	0	1	001	1
0	1	0	1	0	1	0	010	2
0	1	1	0	0	1	1	011	3
0	1	1	1	1	0	0	100	4
1	0	0	0	0	1	0	010	2
1	0	0	1	0	1	1	011	3
1	0	1	0	1	0	0	100	4
1	0	1	1	1	0	1	101	5
1	1	0	0	0	1	1	011	3
1	1	0	1	1	0	0	100	4
1	1	1	0	1	0	1	101	5
1	1	1	1	1	1	0	110	6

Figure 1. Truth Table for Logic Circuit

The table represents the truth table of a 2-bit full adder, which performs binary addition of two 2-bit numbers labeled as A1A0 and B1B0. Each input number is composed of a most significant bit (MSB) and a least significant bit (LSB). The addition process is done in two stages: first, the LSBs (A0 and B0) are added to produce a sum bit S0 and possibly a carry into the next stage. Then, the MSBs (A1 and B1) are added along with the carry from the first stage to produce the second sum bit S1 and a final carry-out C1. The result of the addition is shown as a 3-bit binary number (C1S1S0) under the "Binary Sum" column, and its decimal equivalent is listed in the "Decimal" column. This full adder can represent sums ranging from 0 (when both inputs are 00) up to 6 (when both inputs are 11). The table helps visualize how binary addition works, including carry propagation between bit positions.

Logic Diagram

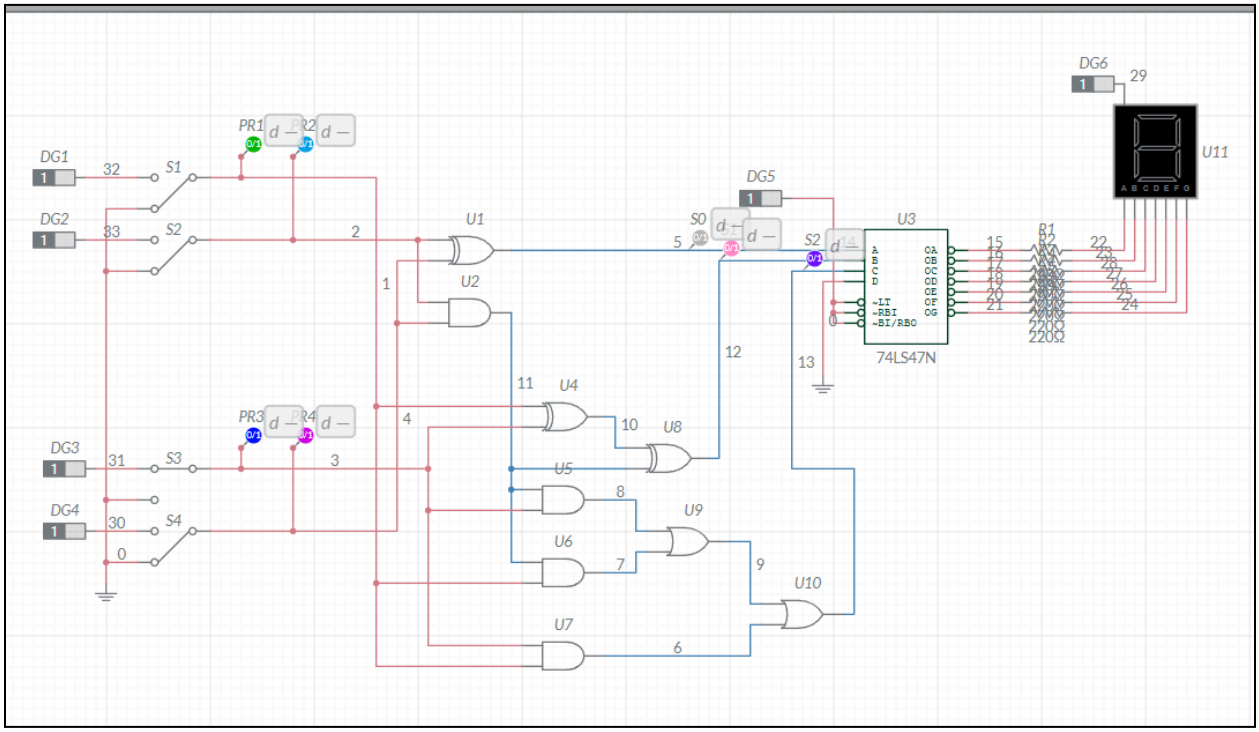
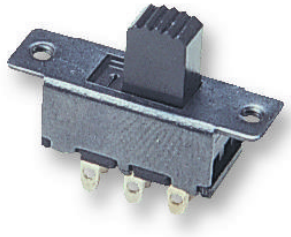
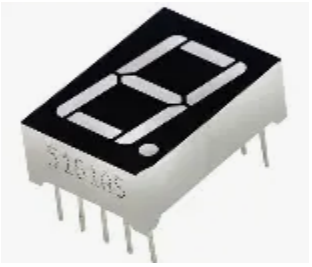
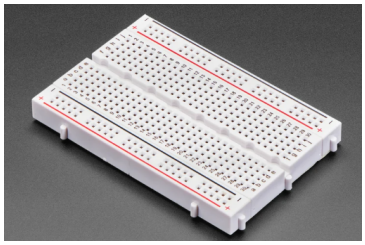
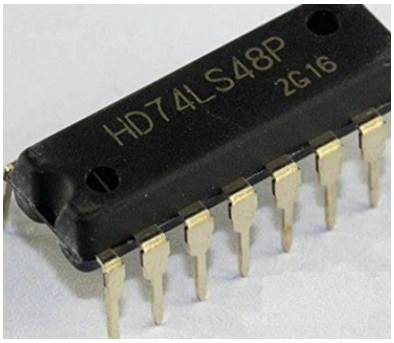


Figure 2. Logic Diagram for Logic Circuit

As seen at figure 2, the logic diagram represents a 4-bit binary to decimal display system using four input switches (S1 to S4) connected to a network of AND, OR, and NOT gates that process binary combinations. The resulting signals are fed into a 74LS47N decoder, which converts the binary-coded decimal (BCD) input into signals for a 7-segment display. This display visually represents the decimal equivalent of the binary input, dynamically updating as the switches are toggled, demonstrating binary-to-decimal conversion using combinational logic.

Materials Used:

Materials	Quantity	Picture
Slide Switches	4	
IC 7486 (XOR)	1	
IC 7408 (AND)	1	
IC 7432 (OR)	1	
7-Segment Display (Common Cathode)	1	

220Ω Resistors	7	
Breadboard	2	
7448 BCD to 7-Segment Decoder	1	
Wires	100