

Development of Digital Architectures for Pixelated Readout of Time Projection Chambers: Q-Pix

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ABSTRACT

The Standard Model (SM) of physics has proven successful over the past decades, despite several measurements that indicate its incomplete description of nature. The search for New Physics (NP) continues at higher energies ($\gg 1$ GeV) with larger detectors (≈ 10 kT). One such future detector is the Deep Underground Neutrino Experiment (DUNE). DUNE is a combination of two detectors, a near detector (ND) and a far detector (FD), which will be used together to search for Charge-Parity Violations (CPV) in the lepton sector. The DUNE FD will be a combination of four large (≈ 10 kT) Liquid Argon Time Projection Chambers (LArTPC). Each 10-kT FD requires high precision in both time ($lg \mu s$) and spatial resolution (≈ 1 mm) for vertex reconstruction and particle identification (PID) of neutrino events.

This dissertation discusses the progress and characterization of a novel implementation of a new pixelated LArTPC readout technology that can be used in an FD. This novel readout is based on a pixel-level charge-integrate-reset circuit: Q-Pix. We present the basic pixel-level readout circuit and the implications of such an implementation when used in kiloton LArTPCs. We also show results from the first prototype implementation based on the Q-Pix readout, which was designed using only off-the-shelf electronics.

One problem with any pixelated readout is the ability to handle a large number of unique data channels, which in the case of the DUNE-FD is $\approx 10^8$. To address the scaling problem, we have developed and tested a modular digital back-end prototype as a proof of concept. This prototype is based on the first Q-Pix digital ASIC design also presented in this thesis. We discuss the back-end system requirements for a Q-Pix based readout technology to provide neutrino oscillation measurements up to 10 GeV, and present the first demonstration of local oscillator calibrations (~ 0.1 ppm). Simulations were performed based on radiogenic backgrounds and high-energy neutrino beamline events, providing first constraints on digital back-end requirements in both the quiescent and active states. Finally, based on these results from the simulations and prototypes presented here, we discuss the digital back-end readout of a fully realized Q-Pix implementation within a 10 kT DUNE-FD module.

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Chapter 1

INTRODUCTION

The aim of this thesis is to demonstrate the viability of the digital back-end novel of a novel pixelated readout to be used in Time Projection Chambers (TPCs). We begin this chapter with an introduction to the Standard Model (SM) in Section 1.1. We pay special attention to the experimental work that has been done to lay the foundation of the knowledge of physics that we have today.

In Section 1.2 we briefly discuss the history and development TPCs. The novel readout presented in this thesis is in Chapter 2 is designed specifically for use in TPC detectors. Chapter 3 provides the first measurements Q-Pix front-end readout in gas-based TPCs.

We continue in Section 1.3 to describe the future Deep Underground Neutrino Experiment (DUNE). The studies of Chapters 4 and 5 demonstrate how this novel charge readout could be scaled to a DUNE Far Detector (DUNE-FD).

In Section 1.4 we provide a brief history on the discovery of the neutrino and discuss its relevance for searching for physics beyond the Standard Model. We also give a short review of the theory behind neutrino oscillations. Oscillation measurements, and by extension, the search for Charge-Parity violation in the lepton sector, are a primary scientific goal of the DUNE experiment. These measurements involve interactions that occur at GeV energy scales. We provide the first demonstration of the required capabilities at these energy scales for the Q-Pix back-end readout in Chapter 5.

1.1 The State of Things: The Standard Model

What is the universe made of? What are the fundamental building blocks of matter? Throughout history thinkers have questioned the nature of the universe and wondered what the basic building blocks of nature are. Answering these fundamental questions is the motivation for particle physics.

In the history of science, it is easy to argue that the most successful of all models is the Standard Model of Physics. The Standard Model (SM) [1–3] was originally developed in the mid to late 1970’s and is the model responsible for unifying the weak, strong, and electromagnetic forces

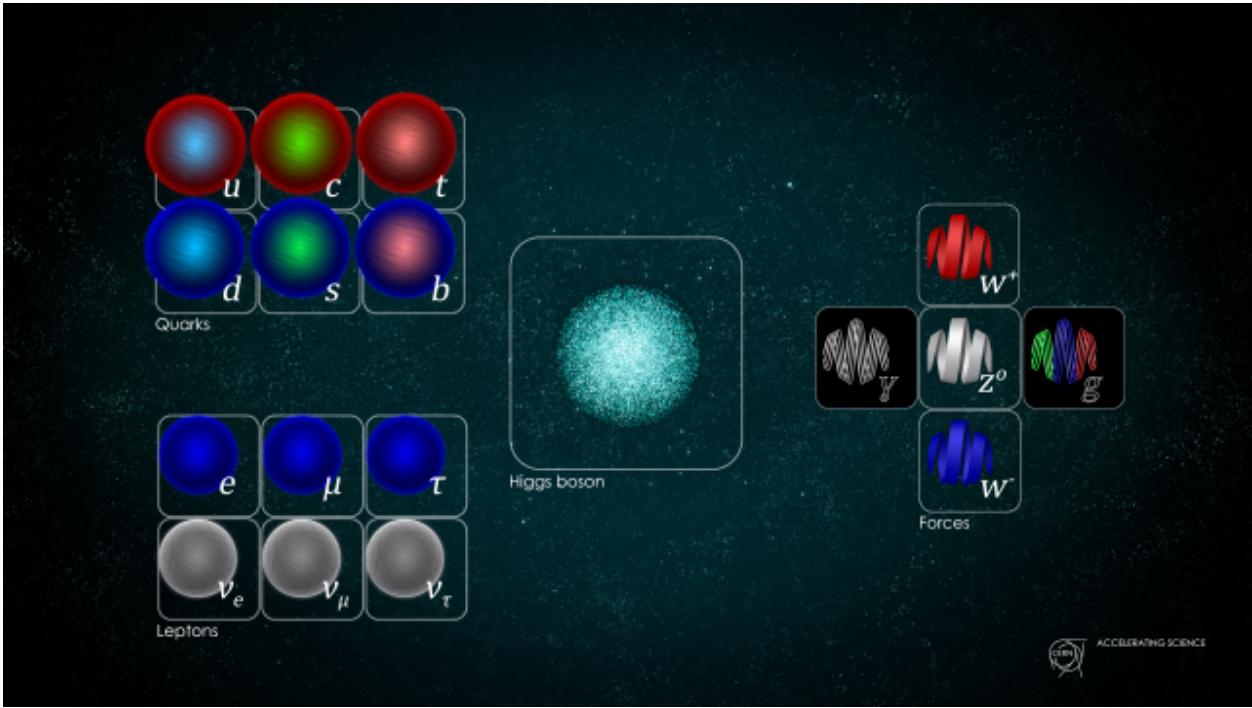


Figure 1.1: Image of fundamental particles in the Standard Model, taken from [5]. All known matter and particle interactions involves combinations of the particles shown here.

together. It has made remarkable predictions about the existence of elusive neutrinos, quarks and vector bosons before they were discovered, and more.

A comprehensive and extensive list of known particles, as well as various cross-sections, lifetimes, and other known information can be found from the bi-annually published Particle Data Group (PDG) [4]. The SM has been tested experimentally more exhaustively than any other theory. The SM has stood the test of time, despite the many mysteries it cannot explain.

The Basics of the Standard Model

The SM itself dictates the fundamental constituents of matter and energy. Its purpose is to explain the origin of observed matter and to provide a description of all observable interactions. The interactions described by the SM involve three of the four known fundamental forces observed in nature: the electromagnetic, weak, and strong forces. The missing fourth force is one of the major shortcomings of the SM: its inability to incorporate a quantum description of gravity.

All currently known fundamental particles are represented in Fig. 1.1. These particles represent the today's knowledge of the building blocks of all observed matter in the universe.

Quark	Charge	Mass (MeV)	Year Discovered	Ref.
up	$\frac{2}{3}$	2.16	1968	SLAC [8, 9]
down	$-\frac{1}{3}$	4.67	1968	SLAC [8, 9]
strange	$-\frac{1}{3}$	93.4	1968	SLAC [8, 9]
charm	$\frac{2}{3}$	1270	1974	SLAC [10] and BNL [11]
bottom	$-\frac{1}{3}$	4180	1977	Fermilab [12]
top	$\frac{2}{3}$	173000	1995	Fermilab [13]

Table 1.1: Description of the discovery of quarks. The presented data are rounded to three significant figures based on [4].

Particle	Charge	Mass (MeV)	Year Discovered	Ref.
e^-	-1	0.511	1896	[14]
μ	-1	105.7	1936	[15]
τ	-1	1,776.9	1975	[16]
ν_e	0	unknown	1956	[17]
ν_μ	0	unknown	1977	[18]
ν_τ	0	unknown	1995	[19]

Table 1.2: Description of the discovery of the leptons.

The quarks represent particles in the upper left of Figure 1.1. In 1961 Murray Gell-Mann proposed his “eight-fold way” [6], which provided a method of grouping the hadrons. Shortly thereafter, the quark model was then proposed by Gell-Mann in 1964 [7]. A unique feature of quarks compared to leptons is that no “free” quark has ever been observed. This means that all current direct observations of quarks are in bound states.

The leptons represent particles in the lower left of Figure 1.1. Like the quarks, the leptons come in three families (e , μ , τ). Also like the quarks, the leptons have charge, mass, and flavor which means they can decay. Unlike the quarks, the leptonic particles do not have a color quantum number and therefore do not combine together to form composite particles.

All forces within the SM (electromagnetism, weak, and strong) are governed via a “carrier” particle, known as a gauge boson. These bosons are represented on the center-right of Figure 1.1. Table 1.3 provides a relative strength chart of the forces, and provides references for the first discovery of the carrier particle.

The strong-nuclear force is governed by the exchange of the gluon (g), and is described by Quantum-

Force	Scale	Theory	Carrier	Ref.
Strong	10	Chromodynamics	gluon	TASSO [20, 21]
Electromagnetic	10^{-2}	Electrodynamics	photon	Recognized Quanta in Ref. [22]
Weak	10^{-13}	Flavordynamics	W^\pm, Z	CERN [23],[24]
Gravity	10^{-42}	General Relativity	graviton	not observed

Table 1.3: Relative strength chart of the four fundamental forces of nature. Although gravity is not included within the SM it is included, as well as its theoretical force carrier the graviton.

Chromodynamics (QCD). This force is responsible for the color quantum numbers of matter and describes why nuclei are held together. The electromagnetic force is governed by particle exchanges of a photon, and is described by Quantum-Electrodynamics (QED). The neutrinos are the only particles within the quarks and leptons which do not interact at all with the electromagnetic force. The weak-nuclear force is governed by particles exchanges of one of the three particles in the center: W^\pm and Z , and is described by Quantum-Flavordynamics (QFD). This force involves a change in flavor of a particle, and affects both quarks and leptons. It is also responsible for all nuclear decay processes.

The last particle to be discovered in Figure 1.1 in the SM was the Higgs particle. The Higgs particle was originally predicted in 1964 by Peter Higgs [25]. This particle is important to describe how mass is given to the elementary particles described by the SM. The Higgs was discovered in 2012 at the Large Hadron Collider (LHC) [26].

Physics Beyond the Standard Model

Despite the SM's many successes there is still much about the universe remains unexplained. SM does not incorporate gravity, it does not account for the matter-antimatter asymmetry of the universe, nor does it account for sources of dark energy and dark matter. SM also doesn't explain some of its fundamental properties, such as: why are there only three generations of leptonic particles (e , μ , and τ)?

The search for answers to these questions motivates the search for physics beyond the SM. The success of the SM is also a sign of the difficulty of discovering new physics. Likely, in order to push beyond the Standard Model (BSM) physicists will have to develop not only larger, but more clever detectors (Sect. 1.3). In Section 1.4 we discuss another missed initial prediction of the SM: neutrino oscillations.

1.2 Time Projection Chambers

The Time Projection Chamber (TPC) was first developed by David Nygren [27] in 1974. The first TPC design used high pressure gas and was able to measure thousands of particle tracks per second and provide full 3-D event reconstruction. This detector was originally used in the Positron-Electron Project (PEP-4) experiment, which measured electron-positron collisions from the 29 GeV electron beam produced at the Stanford Linear Accelerator (SLAC).

The basic operating principle of a TPC is that a charged, moving particle ionizes other particles in the detector and produces scintillation light. The ionized electrons are then drifted by an external electric field down towards a collection plane (the anode) and are then readout by the electronics. The electric field also prevents recombination of the ionized electrons in the medium. A diagram of this process is shown in Figure 1.2. The detected scintillation photons (not shown in Figure 1.2) can be used to determine the time of the interaction. The track of the ionizing particle can then be reconstructed using the 2-D information from the wires, the timing collected from the photons, and the drift time of the electrons.

The development of the TPC closely followed the development of fast (> 1 MHz) digitizing electronics. Using fast digitizers and closely spaced wires Georges Charpak (1924-2010) created the first multi-wire proportional chamber (MWPC) in 1968 [29]. Current and future TPCs (see Section 1.3) use MWPC as a basis for their readout electronics.

TPCs have proven to be extremely capable in high energy physics experiments. They are used in many applications such as dark matter experiments [30] and neutrino experiments [31]. TPCs are so useful because they provide high resolution in both temporal and spatial dimensions, as well as offer 3-D track reconstruction.

Liquid Argon Time Projection Chambers

Alternatives to gaseous TPCs are liquid TPCs, which (as the name implies) uses a liquid detection medium. A specific type of liquid based TPC is a Liquid Argon Time Projection Chamber (LArTPC) [32]. Liquid was originally proposed as an alternative to the gaseous TPCs to provide a denser active volume. Experiments such as neutrino or dark matter measurements have low interaction cross sections, and thus greatly benefit from a dense active detector medium. Recently, much progress has been made in the implementation of LArTPCs for neutrino experiments ([31,

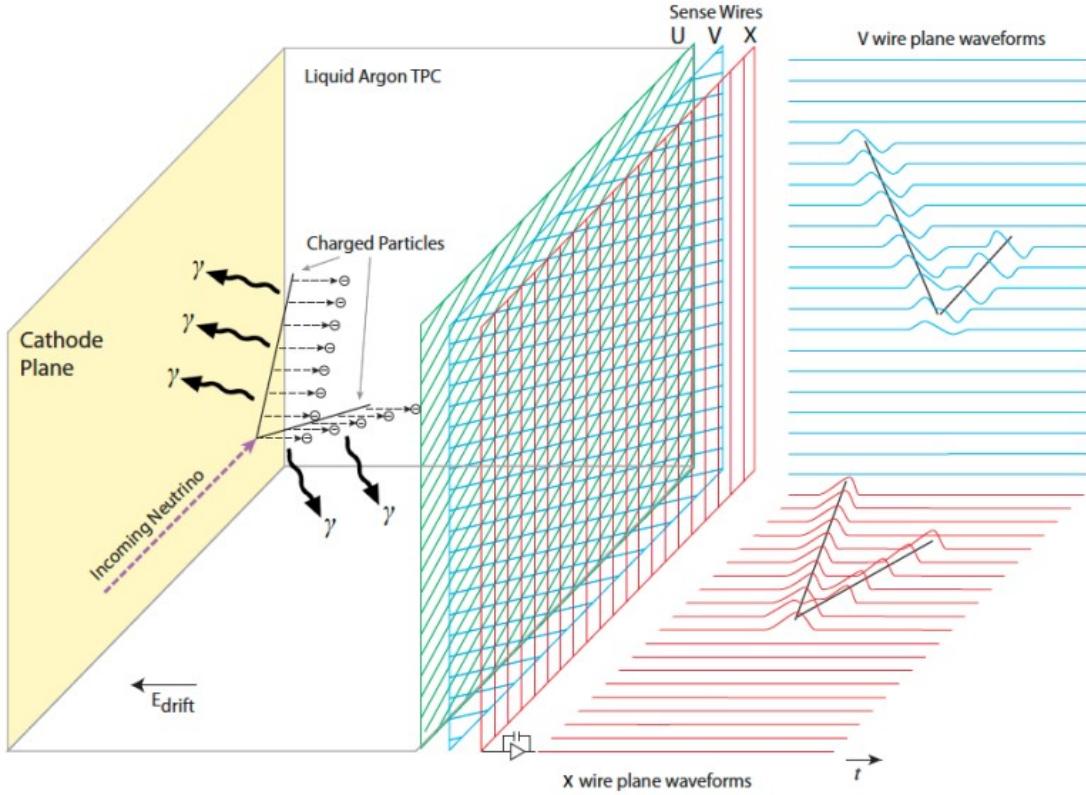


Figure 1.2: Image of a Time Projection Chamber (TPC). Charge is accumulated within the volume as ions are removed from the fiducial volume from another charged ion as it passes through the material. An uniform electric field drifts the freed electrons towards the anode plane. The collection and readout of charge on this anode plane is what is recorded within the detector. Shown in the image are the three wire collection planes used in the DUNE experiment. Image is taken from [28].

33, 34]).

LArTPCs provide a stable noble element (argon) with a high nucleon density. Argon offers several key advantages for its selection as a detector medium. Some key advantages of argon are its ability to produce large ($\sim 10\text{kT}$) detectors, its high breakdown voltage, and its high ionization and scintillation yields. The relevant properties of a LArTPC are shown in Table 1.4.

1.3 The Deep Underground Neutrino Experiment

The Deep Underground Neutrino Experiment (DUNE) is a long-baseline neutrino beam experiment [28, 36–38]. DUNE, when constructed, will consist of two detectors, a near detector (ND) and a far detector (FD) which are separated by a distance of 1300 km. The neutrino beam measured

Property	Symbol	Value	Unit
Density	ρ	1.3973	$g cm^{-3}$
Dielectric Constant	ϵ	1.505	-
electron drift velocity	v_e	0.1601	$cm/\mu s$
Ionization Energy of single e^-	W_i	23.6	eV/e^-
Minimum Specific energy loss	$(dE/dX)_{MIP}$	2.12	MeV/cm
Longitudinal Diffusion Coefficients	D_L	6.6270	cm^2/s
Transverse Diffusion Coefficients	D_T	13.2327	cm^2/s

Table 1.4: Relevant Liquid Argon parameter information. Values are taken from [35], with temperature $T_s = 87K$ and electric field $E_f = 0.5kVcm^{-1}$.

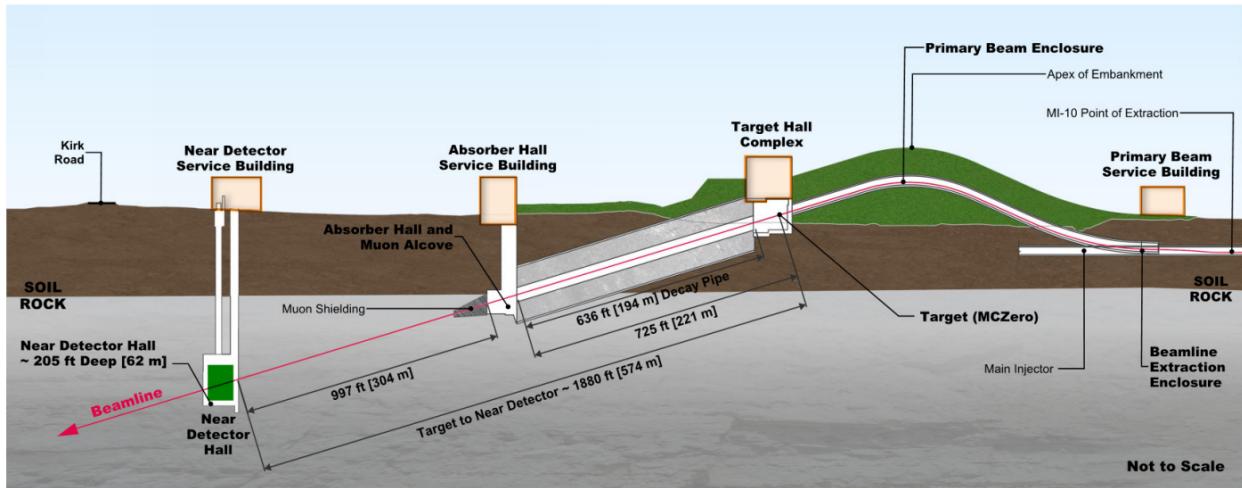


Figure 1.3: Image of the near detector hall located relative to the neutrino beam at Fermilab in Illinois. The ND is ≈ 525 m from the neutrino target. Image is taken directly from [28].

at the ND and FD will be generated at the Long Baseline Neutrino Facility (LBNF) [39] beamline at Fermilab. An image of the beam and the ND are shown in Figure 1.3.

The ND is located at Fermilab and its purpose is to characterize the unoscillated neutrino beam. The ND serves as a control for DUNE's. Results from the interaction rates at the ND provide evidence for the null hypothesis within the standard three neutrino oscillation paradigm. It will measure the unoscillated spectra for ν_e , ν_μ , and their anti-particle pairs as a function of their energy, upon which the oscillation probability depends. The FD will use these unoscillated neutrino spectrum measurements to predict which neutrino interaction spectra it should measure.

The ND is a suite of three detectors all exposed to a LBNF beam. One component of the ND is a LArTPc (ND-LAr) which is a pixelated detector to be built using ArgonCube technology.

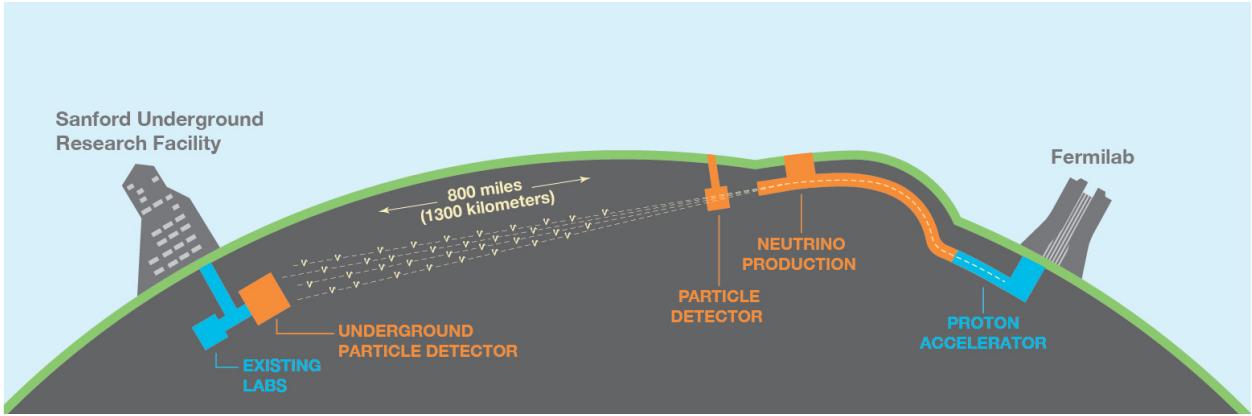


Figure 1.4: Representation of the Near and Far Detectors for the DUNE experiment. The ND is located within the image labeled as the Particle Detector. One of the key purposes for the ND is to tag outgoing particles from the proton beam. The FD is located at SURF on the left of the image, and will contain four 10 kT LArTPCs, which are the target of the neutrino beam. The beam’s energy and distance between the ND and FD are chosen to optimize sensitivity to neutrino oscillation measurements (See Section 1.4). Image was taken from [39].

Another component of the ND is a high pressure (10 atm) argon gas based TPC (ND-GAr). The ND-Gar has superior identification capabilities of charged pions than the LArTPC, and prevents misidentification of these pions as protons. The final component of the ND is the System for on-Axis Neutrino Detection (SAND), which is a magnetized beam monitor. SAND is used to measure the beam flux sent to the FD.

The FD will be located underground at Sanford Underground Research Facility (SURF) and be approximately 1300 km away from the ND. The FD will consist of four separate 10 kiloton LArTPC modules (DUNE-FD SP), an example of a single module is shown in Figure 1.5. This detector represents an enormous engineering challenge to place such a large, cold, and complicated detector.

At least two of these four modules at least will use a known wire-based readout technology. The remaining two modules are considered modules of opportunity and their readout technology is yet unknown. A purpose of this dissertation is demonstrate the viability of a novel readout technology targeted at a large 10 kT LArTPC Single-Phase (SP) module, which is discussed in Chapter 2.

DUNE has three main science goals, all of which are geared towards pushing beyond the SM:

- Hadron Decay (Section 1.3)
- Core-collapse Supernovae (Section 1.3)

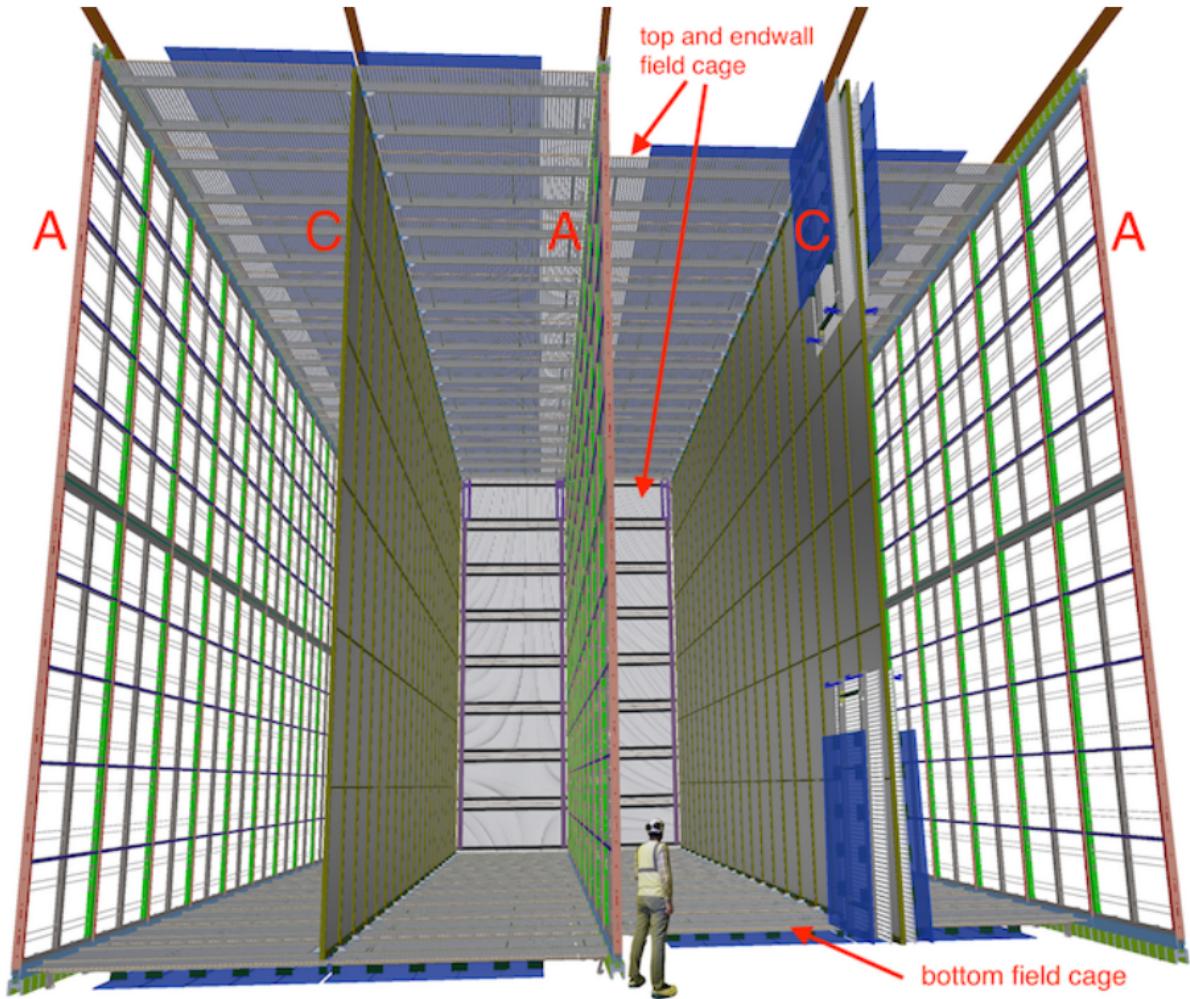


Figure 1.5: Image of a single 10 kT DUNE Far-detector Single-Phase (DUNE-FD SP) module. The dimensions of the module are 58.2 m into the page, 12.0 m high, and each drift distance is 3.5 m between the anode (A) and cathode (C) planes. The ionization charges drift horizontally in the SP scheme, where electrons are drifted toward the anode (A) planes. Image is taken directly from [28].

- Neutrino Oscillation (Section 1.4)

DUNE plans to offer an incredibly rich search in the areas listed above 1.3. We will discuss the relevance of each of the first two items in the next two sections. We provide a more complete discussion of neutrino oscillations in section 1.4 because of its relevance to the results presented in chapter 5.

Hadron Decay

Does a proton decay? This is the fundamental question for physicists studying hadron decay. The SM predicts that the proton itself is stable, so it should never decay. Thus, the search for proton decay offers a path for physics beyond the SM. Attempts to unify all the fundamental forces of nature into a single theory are called Grand Unified Theories (GUTs), and according to many GUTs, the proton does indeed decay.

Current measurements on the proton lifetime indicate that its lifetime is on the order of magnitude (or above) 10^{34} years. Even at its most frequent, this is an exceedingly rare event considering that the lifetime of the universe is $\approx \mathcal{O}(10^{10}$ yrs). Since these events are so rare, extremely large detectors with large numbers of protons inside of them are required to constantly observe many protons. LArTPCs (as in DUNE) are excellent candidates for observing these rate events due to their active detector volume. An example of a second generation proton decay study is the Imaging Cosmic and Rare Underground Signals (ICARUS) experiment [40].

There are at least two prominent decay chains that are expected to be dominant, depending on the Grand-Unification-Theory (GUT) that hopes to go beyond the SM. The first one is:

$$p^+ \rightarrow e^+ + \pi^0 + 2\gamma \quad (1.1)$$

This interaction is easily detectable in cherenkov based detectors due to the emission of both the gammas as well as the high energy of the emitted positron. In fact, the worlds best estimate for proton lifetime comes from this decay-chain [41].

Other Supersymmetric GUT models predict instead [42]:

$$p^+ \rightarrow K^+ + \nu \quad (1.2)$$

In this case, the kaon generally moves too slowly to be measured by Cherenkov detectors. However, TPC-based detectors are still sensitive to the charge deposited by it. This is interesting because the

Super-Kamiokande experiment, itself a Cherenkov-based detector in water, currently provides the world's best limits.

These searches are interesting, though difficult, in part because of the rarity of such an event. If any detector could unambiguously measure even a single proton decay, it would provide direct evidence for physics beyond the SM. Future detectors that will continue to search for nucleon decay are DUNE, Hyper-Kamiokande, and JUNO [28, 43, 44]. These searches are interesting, if albeit difficult, both due to the rareness of such an event JUNO [28, 43, 44].

Supernova Studies

A supernova occurs when a massive star runs out of the elemental fuel needed to fuel nuclear fusion at its core. When this happens, the inward gravitational pull of the star's mass overcomes the reduced outward pressure from nuclear fusion.

It has been nearly 30 years since the last neutrinos were observed from a galactic core-collapse supernova, SN 1987A [45]. The rarity of these events encourages large, precise, long-lived detectors to ensure a capture of neutrinos from the next event. Sensitivity to supernova neutrinos is crucial for understanding the mechanisms that govern particles at these extreme densities and pressures. Interestingly, because neutrinos are so weakly interacting, it is possible to observe their signature and arrival before the arrival of photons from a Type II supernova.

The principal interaction chain observable in a TPC is:

$$\nu_e + {}^{40} \text{Ar} \rightarrow e^- + {}^{40} \text{Kr}^+ \quad (1.3)$$

It has been almost 30 years since the last neutrinos were observed from a galactic core collapse supernova, SN 1987A [45]. The rarity of these events encourages large, precise, long-lived detectors to ensure the capture of neutrinos from the next event. Sensitivity to supernova neutrinos is crucial for understanding the mechanisms that govern particles at these extreme densities and pressures. Interestingly, because neutrinos interact so weakly, it is possible to observe their signature and arrival before the arrival of photons from a Type II supernova.

1.4 Neutrinos and Oscillations

Evidence for the existence of neutrinos began in the early 20th century. More than 100 years ago, Chadwick showed that the energy spectrum of a decaying electron was continuous [46]. This

unknown cause of the spectrum even led some physicists to believe that the conservation of energy might be violated. Wolfgang Pauli instead predicted that a particle he originally called the neutron would also be a decay product, but not easily observable. This third particle in the decay would explain the energy spectrum of the electron. The discovery of the neutron([47]) and the continuous spectrum of beta decay forced Pauli to come up with a new theory that attempted to describe beta decay [48]. Finally, some 26 years later, in 1956, the first observation of ν_e [17] was made.

Originally, the mass of the neutrino predicted by the SM was massless. That was until the solar neutrino anomaly measured significantly fewer neutrinos than predicted [49]. The solution was oscillation. Since then, many large experiments have been devoted to measuring the three generations of neutrinos. [50–58]

Neutrino oscillation describes the behavior that a neutrino can undergo a flavor transition as it moves through space. The flavor transition relevant to DUNE is the transition of $\nu_\mu \rightarrow \nu_e$ and its associated antiparticles. The flavor transition occurs because the mass and flavor eigenstates are not the same. Here we give a general description of a model to describe neutrino oscillation. We elucidate the measurable parameters that govern this oscillation and describe how these values are currently measured in experiments. The standard notation refers to the mass eigenstates (ν_i) and the flavor eigenstates (ν_α):

$$\nu_i = U_{i\alpha} \nu_\alpha \quad (1.4)$$

This can be expanded into matrix notation as:

$$\begin{pmatrix} \nu_e \\ \nu_\mu \\ \nu_\tau \end{pmatrix} = \begin{pmatrix} U_{e1}, U_{e2}, U_{e3} \\ U_{u1}, U_{u2}, U_{u3} \\ U_{\tau1}, U_{\tau2}, U_{\tau3} \end{pmatrix} \begin{pmatrix} \nu_1 \\ \nu_2 \\ \nu_3 \end{pmatrix} \quad (1.5)$$

The matrix elements within U_{li} represent the mixing coefficients and are used to calculate the probability that a certain neutrino will oscillate from one family to another. We identify U_{ij} as the commonly known U_{PMNS} matrix, where PMNS stands for: Pontecorvo–Maki–Nakagawa–Sakata, or the four theorists who helped developed this convention. Luckily, there are not a total of nine free parameters within the SM that determine this. The U_{PMNS} matrix can be additionally rewritten following [59, 60] as:

$$U_{PMNS} = U_{sol} \times U_{rea} \times U_{atm} \times U_{maj} \quad (1.6)$$

After expanding the matrix representations, Equation 1.6 becomes:

$$U_{PMNS} = \begin{pmatrix} 1 & 0 & 0 \\ 0 & C_{23} & S_{23} \\ 0 & -S_{23} & C_{23} \end{pmatrix} \times \begin{pmatrix} C_{13} & 0 & S_{13}e^{-i\delta_{CP}} \\ 0 & 1 & 0 \\ -S_{13}e^{-i\delta_{CP}} & 0 & C_{13} \end{pmatrix} \times \begin{pmatrix} C_{12} & S_{12} & 0 \\ -S_{12} & C_{12} & 0 \\ 0 & 0 & 1 \end{pmatrix} \times \begin{pmatrix} 0 & 0 & 1 \\ e^{i\alpha_1} & 0 & 0 \\ 0 & e^{i\alpha_2} & 0 \end{pmatrix} \quad (1.7)$$

We identify above the additional matrix components where historically these values are measured. Therefore, instead of nine unknown parameters for the SM, there are only six. The components C_{ij} and S_{ij} in the matrices are defined to be $\cos(\theta_{ij})$ and $\sin(\theta_{ij})$, respectively.

Then, the six parameters of the U_{PMNS} are identified as:

- θ_{13} - Reactor measurements.
- θ_{12} - Atmospheric measurements.
- θ_{23} - Solar measurements.
- δ_{CP} - Charge-conjugation parity violation.
- α_1/α_2 , The two Majorana Phase parameters, not observable in beam experiments.

The Majorana phases (α_i) are sensitive in experiments that can detect the Majorana nature of neutrinos such as neutrinoless double beta decay. In neutrino oscillation measurements, these phases cancel out and are not measurable. Therefore, we can safely ignore these two phases for the work presented here.

Next we demonstrate the calculation of the probability of oscillation from one mass eigenstate to another. We calculate the probability $P(\mu \rightarrow e)$, which is the probability of interest for the DUNE beam experiment. First we identify that Equation 1.4 can be rewritten to isolate the flavor-eigenstate terms (v_α) by multiplying by the adjoint of the PMNS matrix (U_{PMNS}^*). Then the relationship between the time dependent mass and flavor eigenstates become:

$$|v_\alpha(t)\rangle = U_{PMNS}^* |v_i(t)\rangle \quad (1.8)$$

The value of interest is $P(\mu \rightarrow e)$, which occurs if the ν_μ travels after some time, t , and interacts via a charged-current (CC) interaction. The probability to end up in state ν_e beginning from ν_μ is:

$$P(\mu \rightarrow e) = |\langle v_e | v_\mu(t) \rangle|^2 \quad (1.9)$$

We then use Equation 1.8 to represent the matrix elements of U_{PMNS} from v_e and v_μ to obtain [61]:

$$P(\mu \rightarrow e) = \left| \sum_i U_{ei} U_{\mu i}^* e^{-iE_i t} \right|^2 = |2U_{\mu 3}^* U_{e3} \sin \Delta_{31} e^{-i\Delta_{32}} 2U_{\mu 2}^* U_{e2} \sin \Delta_{21}|^2 \quad (1.10)$$

Where we identify that the cross terms of the exponential introduce a phase difference shown as Δ_{ij} in the second term in Equation 1.10. We also substituted $E_i t = m_i^2 L / 2E$, to express the oscillation parameter in terms of distance traveled, L. Then, the Equation 1.10 represents the probability of a v_μ to interact via a produce a flavor-changing CC interaction after traveling some distance L.

Finally, the last parameters which govern the neutrino oscillations are identified as the mass differences between the three mass states (Δ_{ij}). These two mass-squared differences are represented in Figure 1.6. We note that though there are three combinations of Δ_{ij} there are only two independent parameters, which are conventionally known as Δ_{12} and Δ_{23} . Δ_{12} is the term which governs the oscillation from the neutrinos in the sun, which are mostly originally v_e and flavor change to v_μ . By the similar reasoning, Δ_{13} , is referred to as atmospheric, since it describes the neutrino oscillations normally observed from atmospheric neutrinos, which flavor change into a v_τ . Unfortunately, since the value of the squared mass-difference is measured (Δ_{12}^2 and Δ_{13}^2), it is not known which mass eigenstate of the neutrinos is the heaviest.

The sign uncertainty leads to two possible orderings of the masses, known as normal (NO) and inverted (IO) order. NO indicates that the masses of the neutrinos follow the ordering of their charged partners. That is, NO implies a mass ordering of: $v_e < v_\mu < v_\tau$. Whereas, IO has a mass ordering: $v_\tau < v_e < v_\mu$.

Neutrino oscillations in matter exhibit slight deviations compared to those in a vacuum [63]. The Mikheyev-Smirnov-Wolfenstein (MSW) effect [64] further contributes to the differentiation of neutrino oscillations as they traverse through regions of varying matter density, introducing additional complexity to the calculations. The MSW effect plays a crucial role in the DUNE experiment as it affects neutrinos and anti-neutrinos differently, providing valuable insights for the measurement of δ_{cp} . In beam-line experiments, this resonance effect primarily influences electron neutrinos (v_e) in the case of normal mass ordering (NO), resulting in enhanced neutrino flavor conversion. Conversely, in the case of inverted mass ordering (IO), the antineutrino counterpart (\bar{v}_e) experiences resonance, making flavor transformation more probable for (v_e).

Neutrino Mass Hierarchy

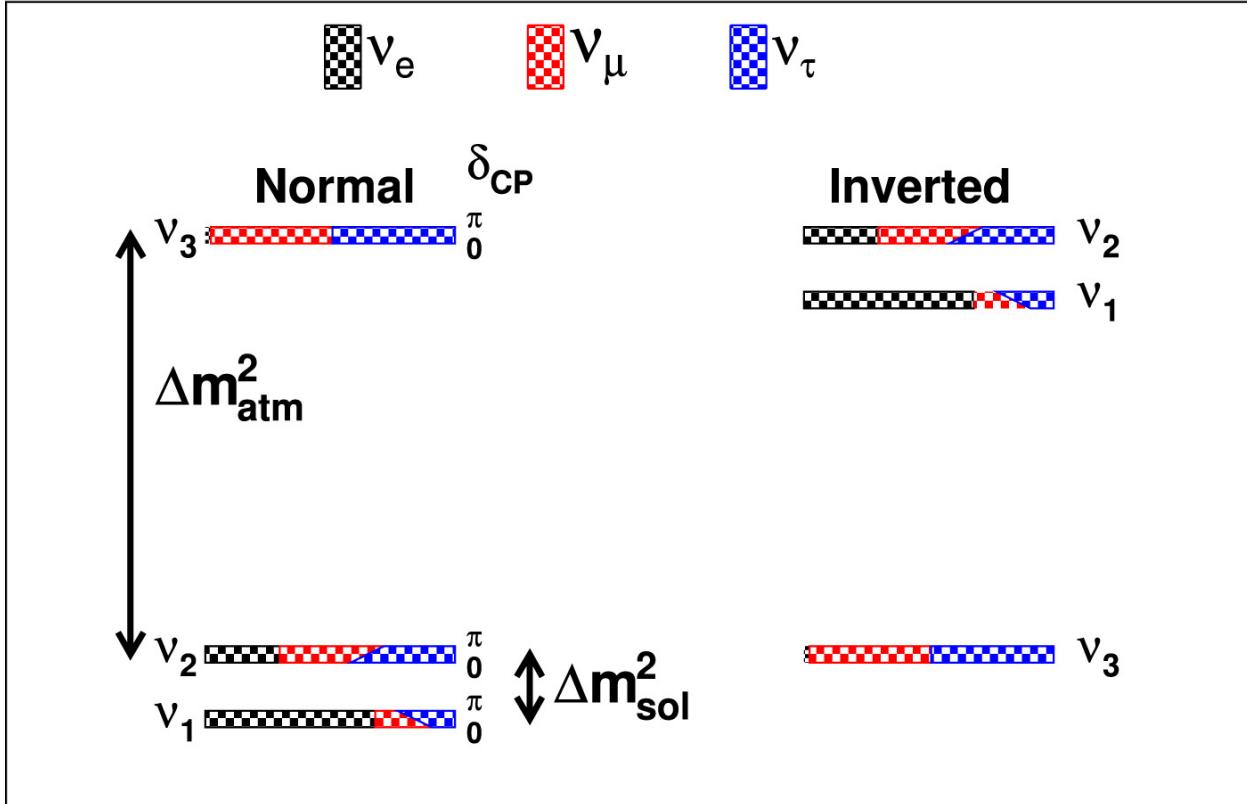


Figure 1.6: Representation of the mass hierarchy scales. This is a representation of the two possible orderings of neutrino masses, due to the uncertain sign of m_{13} . It is also interesting to observe that the absolute mass scale is not measured since oscillation measurements only give difference mass squares. Image was taken from [62].

Parameter	Best Fit	Unit	Best Source
θ_{13}	$8.57^{+0.12}_{-0.12}$	na	Reactor
θ_{12}	$33.44^{+0.77}_{-0.74}$	na	Atmospheric
θ_{23}	$49.2^{+0.9}_{-1.2}$	na	Solar
δ_{cp}	197^{+27}_{-24}	na	Atmospheric+Accelerator
Δm_{21}^2	$7.42^{+0.21}_{-0.20}$	$10^{-5} eV^2$	Solar
Δm_{31}^2	$2.517^{+0.026}_{-0.028}$	$10^{-3} eV^2$	Atmospheric

Table 1.5: Known Oscillation Parameters of Interest. Values are taken from the global fit [65]. The values shown assume normal mass ordering for neutrinos and include atmospheric Super-Kamikonde Data.

Chapter 2

A NOVEL READOUT TECHNIQUE FOR TPCS: Q-PIX

We begin this chapter in Section 2.1 by introducing a novel pixel-based readout concept for TPCs. Pixel-based readouts offer several advantages over the traditional wire readouts [66]. A key improvement offered by pixelization is true 3-D image reconstruction. This allows for sharper vertex reconstruction, which improves the overall resolution of a LArTPC and can reduce the time required for a NP measurement. Other benefits include a reduction in the amount of data storage required and easier data analysis.

Next, in Section 2.2 we discuss how this readout technology can be extended to a DUNE-FD 10 kT module. We compare the design specifications for the current wire-based readout of a DUNE-FD and discuss how the Q-Pix readout can meet similar design goals. We note the advantages of pixelization come at the cost of increased design complexity. The traditional wire-based readout of a DUNE-FD module will have hundreds to thousands of channels, while a pixel-based readout will have tens of millions of channels. This number of channels is required to provide a stable readout over the expected lifetime of DUNE (≈ 20 years), where the electronics are operated continuously at liquid argon temperatures ($\simeq 87$ K). This dissertation addresses the channel size problem in Chapter 5.

Two prototype ASICs have been developed to test each side of the readout shown in Figure 2.2. We refer to the ASIC designed to test the front-end as the "analog ASIC". Likewise, we refer to the ASIC developed to test the back-end as the "digital ASIC". The contributions to the design of the digital ASIC are a major part of this thesis. In Section 2.3 we discuss the design challenges of a large pixelated detector, with a special emphasis on the requirements of the digital back-end. Finally, in Sections 2.4 and 2.5 we briefly describe other work towards validating the Q-Pix design in a LArTPC.

2.1 Q-Pix: The Circuit Level Design

The fundamental Q-Pix circuit (2.1) was first introduced by Nygren and Mei [67]. The principle of the front-end circuit operates on producing a signal output from Schmitt trigger connected to a

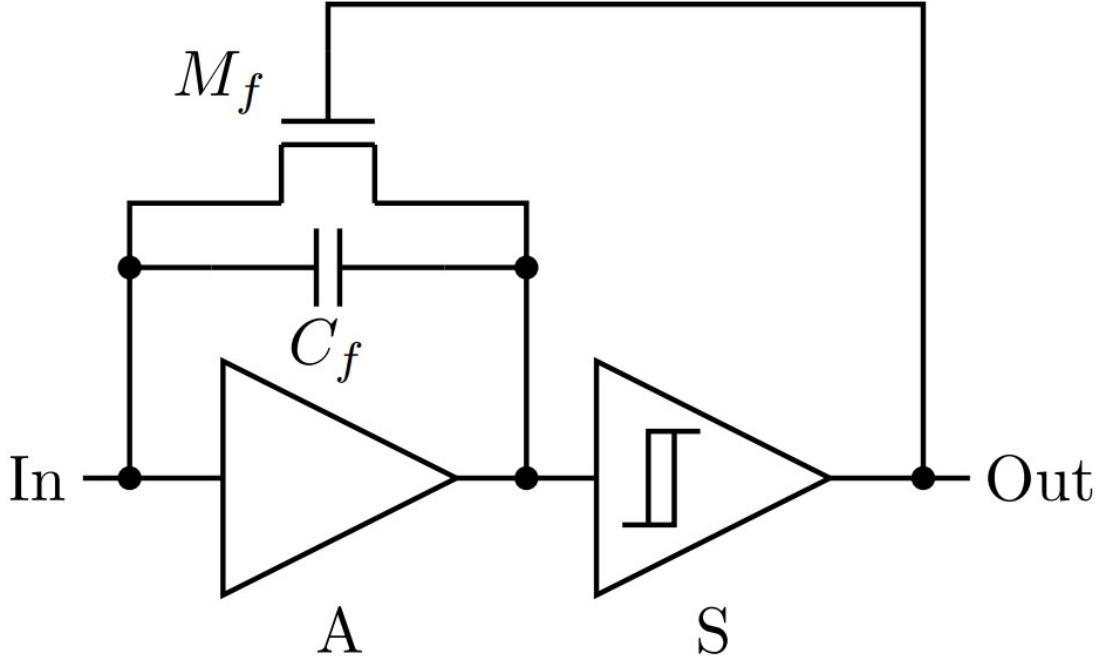


Figure 2.1: A simplified schematic of front-end Q-Pix Readout circuit. The front-end is a charge sensitive amplifier (CSA) whose output is connected to a Schmitt trigger. The trigger (output) occurs when enough charge as accumulated on the capacitor C_f (currently 1 fC). One of the design parameters for the Q-Pix front-end is the choice of C_f . This front-end circuit is designed within a single analog ASIC which has contains 16 of these circuits. The schematic for this ASIC is shown in Appendix B. Image is taken from [67].

charge sensitive amplifier (CSA) circuit. The input of the CSA is connected to the anode of a TPC, where drifted electron charge accumulates. Voltage is then built up across the capacitor from the accumulated charge according to the equation:

$$Q_i = C_i V_i \quad (2.1)$$

After the capacitor voltage exceeds a set threshold (V_i) the schmitt trigger activates. The Schmitt trigger output is sent as a signal input to the digital logic to be recorded. This signal is shown as the output in Figure 2.1. The Schmitt trigger input to the digital back-end is recorded against a free running local oscillator ($f_o = 30$ MHz).

The Q-Pix readout records 32-bit latch values as a response to the Schmitt trigger output; it does not measure voltage, charge, or time. We refer to this 32-bit measurement as a "timestamp". These

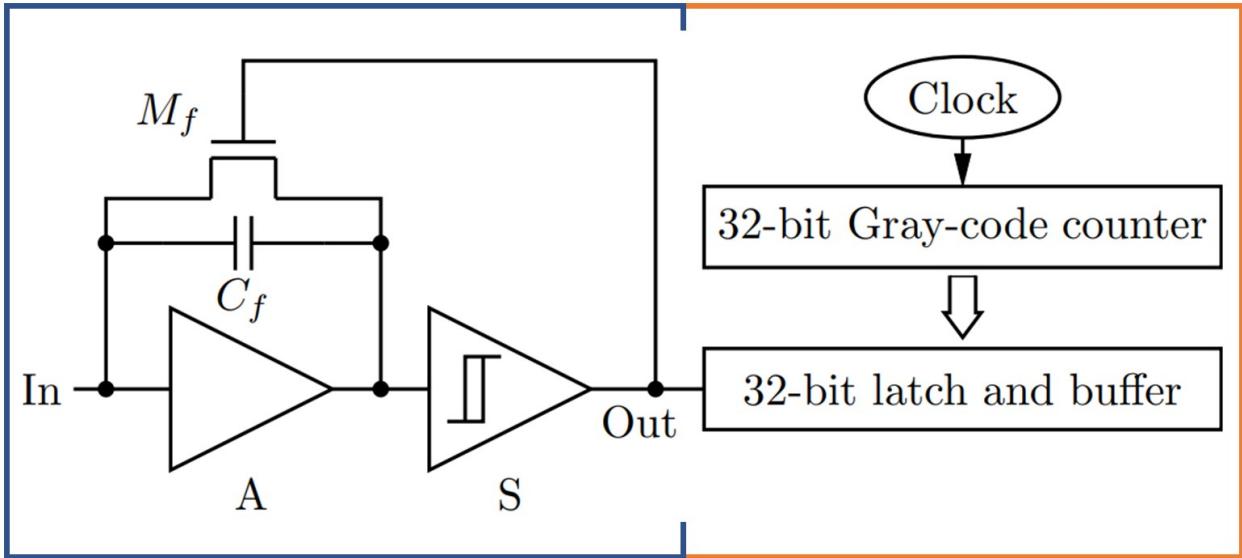


Figure 2.2: A modified image from [67] is shown. The blue box is the Q-Pix circuit (Figure 2.1), which we refer to as the Q-Pix "analog front-end". The right side of the image, encompassed in orange box, we refer to as the "digital back-end". The back-end is responsible for providing the local oscillator as well as accurately recording a reference counter to correspond to the time when the Schmitt trigger signal is received.

timestamps are generated in response to the reset pulse sent from the Schmitt Trigger. Since these resets only occur in response to accumulated charge, the Q-Pix readout does not require an external trigger to acquire data.

There are two components of the Q-Pix readout: analog and digital. The analog portion of the readout begins with the CSA and ends at the Schmitt trigger output. The digital portion of the readout begins at the timestamp record. These two parts are shown in Figure 2.2.

Current Reconstruction

Here we describe the basic principle of reconstructing the input current from a collection of timestamp measurements.

A timestamp measurement indicates that a certain amount of charge was accumulated at the CSA. Since total charge is conserved we can say that the total accumulated charge ($Q_{in}(t)$) is equal total amount of charge discharged from each reset ($Q_{out}(t)$) plus any residual charge still on the pixel ($Q_c(t)$). Therefore, we can relate the total accumulated charge to the total charge discharged with the following equation:

$$Q_{in}(t) = Q_{out}(t) + Q_c(t) \quad (2.2)$$

One of the features of the analog front-end ASIC is a replenishment circuit. This circuit is a constant current source which removes a constant number of electrons from the CSA. This provides a major simplification to the current reconstruction. Assuming that each reset removes the same amount of charge (Q_o), we can rewrite the total charge out (Q_{out}) in terms of the integer number of resets at time t, ($N(t)$):

$$Q_{out}(t) = Q_o N(t) \quad (2.3)$$

Equation 2.3 then gives us the measured current by definition ($I_{out} = \frac{dQ_{out}}{dt}$):

$$I_{out} = \frac{d}{dt}(Q_o N(t)) = Q_o \frac{dN}{dt} \quad (2.4)$$

We identify $\frac{dN}{dt}$ at the number of resets per unit time. We can calculate the average current between two resets, or $\frac{dN}{dt} = \frac{1}{dT}$. Then, dT is the time difference between two resets and is measured at the local oscillator: $dT = \frac{f_o}{N_{rtd}}$, where N_{rtd} is the difference between the two timestamps. Equation 2.4 becomes:

$$I_{out} = \frac{Q_o f_o}{N_{rtd}} \quad (2.5)$$

Equation 2.5 shows the fundamental equation for the Q-Pix readout reconstruction. There are three important parameters: the charge per reset (Q_o), the frequency of each local oscillator (f_o), and N_{rtd} which is the difference between two timestamp measurements. Figures which demonstrate the transistor level effects of this reconstruction are shown in Figures 2.3 and 2.4. Figures 2.3 and 2.4 show the charge reconstructions with a Q_o value of 1 fC and 0.3 fC, respectively.

Of the three parameters in Equation 2.5, two of them need to be calibrated. Validation of the charge calibration is beyond the scope of this work, but is briefly described in Chapter 5 Section 5.4. The local oscillator frequency is a digital ASIC level calibration and its results are a product of this thesis. Its procedure and first results are described in Chapter 4. The remaining reconstruction parameter is the timestamp, which is recorded by the digital back-end.

Track Reconstruction

One of the important features of a TPC is the ability to precisely reconstruct full tracks of ionizing particles. An intended benefit of a pixelated readout on any TPC is to show that there are

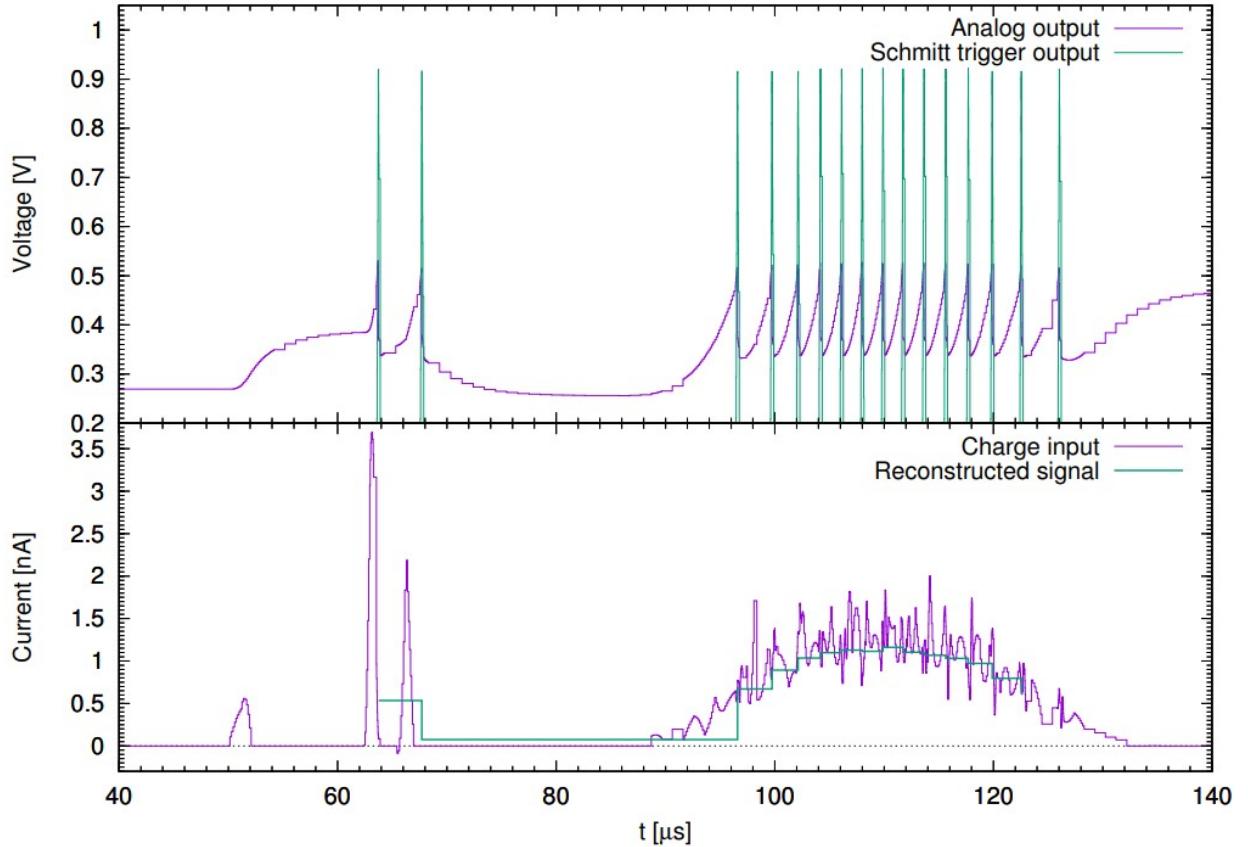


Figure 2.3: Example reconstruction of the reset time difference (RTD) based on the Q-Pix readout design. Shown is transistor-level charge integration simulation results for minimum ionizing tracks in LAr. The purple curve of the top panel represents charge accumulating on the CSA, where the green curve is the reset output from the Schmitt trigger. The bottom panel shows input charge (purple curve) overlaid on top of the reconstructed current signal. The Q_o value taken here is equal to 1 fC. Image is taken from [67].

improvements to reconstruction of these 3-D images. Event reconstruction requires 3-spatial coordinates (x, y, z) of a track's charge as well as time, t . The Q-Pix readout gives two (x, y) coordinates for "free". Time is intrinsic to the Q-Pix datum, and may also be provided by an external photonics system (see Section 2.4). The first measured timestamp could also be used as The starting time of any reconstructed track.

The final coordinate, z , is obtained with the LAr drift velocity (Table 1.4) and the drift time (t_{drift}) by the equation:

$$z_{drift} = v_e * t_{drift} \quad (2.6)$$

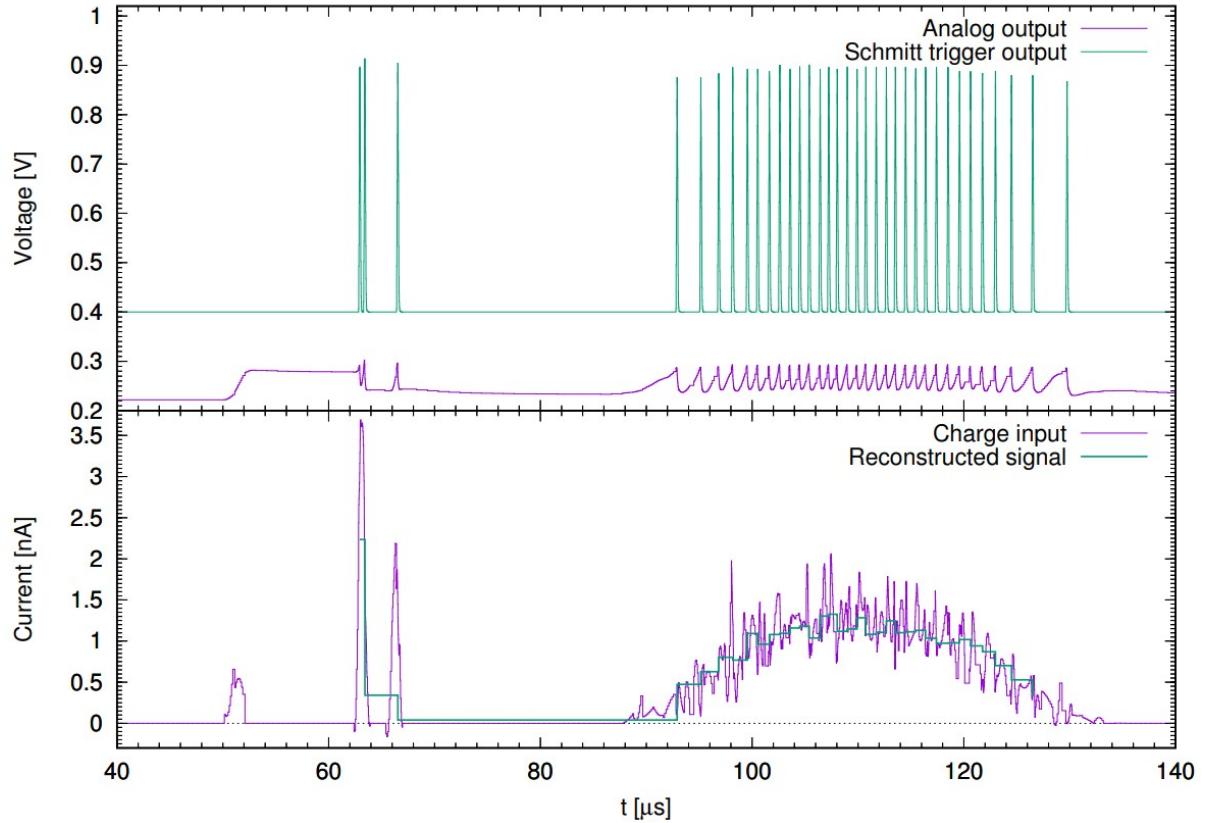


Figure 2.4: Example reconstruction of the reset time difference (RTD) based on the Q-Pix readout design. Shown is transistor-level charge integration simulation results for minimum ionizing tracks in LAr. Q_o was chosen to be 0.3 fC . The bottom panel in this image shows a better match of the reconstructed signal with a smaller Q_o . However, more ($\approx 1.0 \text{ fC} / 0.3 \text{ fC}$) resets are produced as a result. Image is taken from [67].

The current input onto a pixel calculated from Equation 2.5. If a pixel requires a calibrated Q_o to perform a reset, we can relate the charge and current with:

$$Q_{i,drift}(t) = \frac{Q_o f_o}{N_{i,rtd}} t \quad (2.7)$$

The reconstructed charge as a function of time is a piece-wise function of time based on the difference between successive $N_{rtd}(i)$. The slopes of the i-th interval are given by $\frac{Q_o f_o}{N_{i,rtd}}$ Equation 2.7. Finally, the charge as a function of position (z position of the charge), is calculated by identifying $t = t_{drift}$ between Equations 2.6 and 2.7.

Comments on Uncertainties

The verification of the Q-Pix readout, in part, relies on tests to show that these timestamp data can be safely recorded and sent without loss to disc. Here we briefly discuss potential uncertainties within the Q-Pix readout.

Near Maximum Reset Rate

Equation 2.5 relates the maximum current (I_{max}) in a Q-Pix readout at the limiting case of $N_{rtd} = 1$. For $Q_o = 1 \text{ fC}$ and $f_o = 30 \text{ MHz}$, $I_{max} = 30 \text{ nA}$. However, since N_{rtd} is a difference between two 32-bit timestamps, it can only take positive integer values. This means that each current measurement can only take the form, for N integer:

$$I_{max} \sim \frac{30 \text{ nA}}{N}$$

Therefore, there can be large uncertainty in the measured currents for RTDs near the frequency of the oscillator. However, if there is sufficient total charge these discrete uncertainties can be accounted for after digital processing. An example of a periodic artificial input current of with $I \approx I_{max}/10$ is shown below in Figure 2.5. The reconstructed charge over time is shown in Figure 2.6.

Comments on Reconstruction Requirements

The uncertainty for the two transverse coordinates (\hat{x} and \hat{y}) comes from the pixel size. If we assume that the electric field is uniform, on average, over all $O(10^7)$ pixels in an APA, then the charge drift will be uniformly distributed over the pixel size. Then, the pixel size determines the resolution: $\frac{3mm}{\sqrt{12}} \approx 0.87mm$.

To achieve the required uncertainty for the z-position measurement ($\sigma_z \approx 1 \text{ mm}$), the uncertainty from f_o must be small ($\sim 1 \text{ ppm}$). Other measurement uncertainties come from the Equation 2.5. The precision of the local oscillator frequency and the constant charge per reset determine the current reconstruction precision. Variable replenishment circuits can greatly impact Q_o from reset to reset, which will also affect σ_z .

2.2 How Q-Pix fits into a 10 kt LArTPC

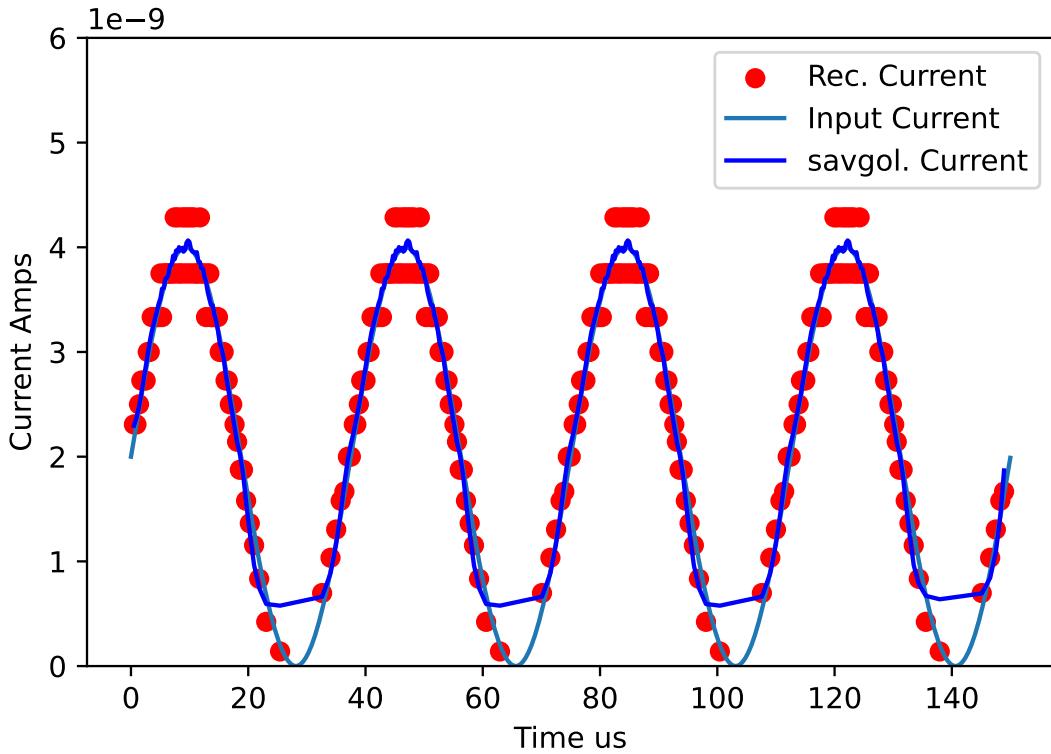
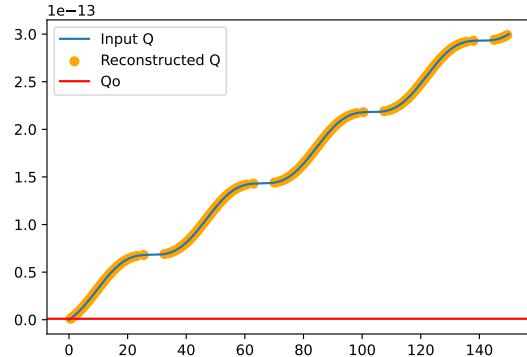
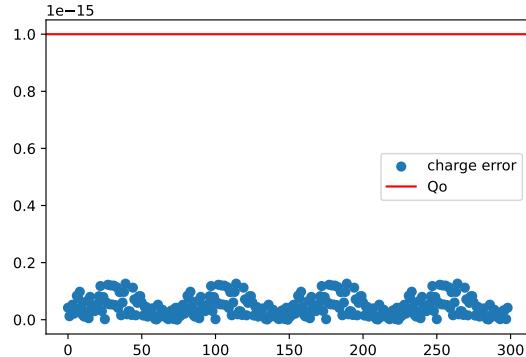


Figure 2.5: Arbitrary sine wave based current input. The maximum amplitude is chosen to be close to I_{max} . Reset Charge is chosen to be 1 fC and digital clock frequency of 30 MHz. The input current amplitude is close to the maximum, so that the reconstructed current can be far from the actual. This occurs since N_{rtd} can only take integer values, the reconstructed current can only take values of $\frac{30}{N}$. The red points indicate possible reconstructed current values, where the two highest points correspond to $\frac{30}{7}$ and $\frac{30}{8}$, respectively. However, an example of a savgol filter (dark blue) is performed on the resets after the fact with near agreement of the large input. A use case of this kind of digital filtering would be applied to large current values only (peaks of the curves), and not for low current inputs where the pure timestamp difference provides better results.



((a)) CDF



((b)) Difference

Figure 2.6: Reconstruction of Sub figures cumulative distribution function (CDF) of charge as a function of time (a) and the error (b). The input current for these data are shown in in Figure 2.5. The pause in resets are when the error is small, since the current input is near zero. The red line indicates the minimum charge required for a single reset. The right plot indicates the difference between the true and reconstructed charge distributions compared to a single reset.

A future target detector for the Q-Pix readout is a DUNE-FD 10 kt module. To explore how Q-Pix could be used in this detector we provide a brief over-view of the DUNE-FD electronics and compare with those requirements for Q-Pix based readout. The simulation results presented in Chapter 5 are based on the detector volume of a single APA within a DUNE-FD module.

The DUNE Far Detector Electronics

The DUNE-FD is a modular assembly of Anode Plane Assemblies (APA) as shown in Figure 2.8. Each Single-Phase (SP) 10 kT module will consist of 100-200 APAs (depending on the drift distance). The APA's full description can be found at [38]. Each APA stores its own the front-end electronics which are in the LAr and are shown in Figure 2.7.

Figure 2.7 shows that each APA uses 20 FEMBs to digitize 128 of the 2560 channels. Of the 128 channels 40 are each taken from the U and V (induction) layers, and 48 wires are taken from the X (conduction) layer. Each FEMB also houses a total of 18 ASICs which smooth, digitize, and aggregate data before being sent to the Warm Interface CRATE (WIC). The total number of ASICs per APA is $18 \times 20 = 360$. Since each 10 kt module uses 150 APAs the total number of ASICs would be multiplied by 150.

On each FEMB are three ASICs are responsible for collecting the charge as it passes between the wires and sending it out of the cryostat. The first ASIC is a waveform-shaping and amplification

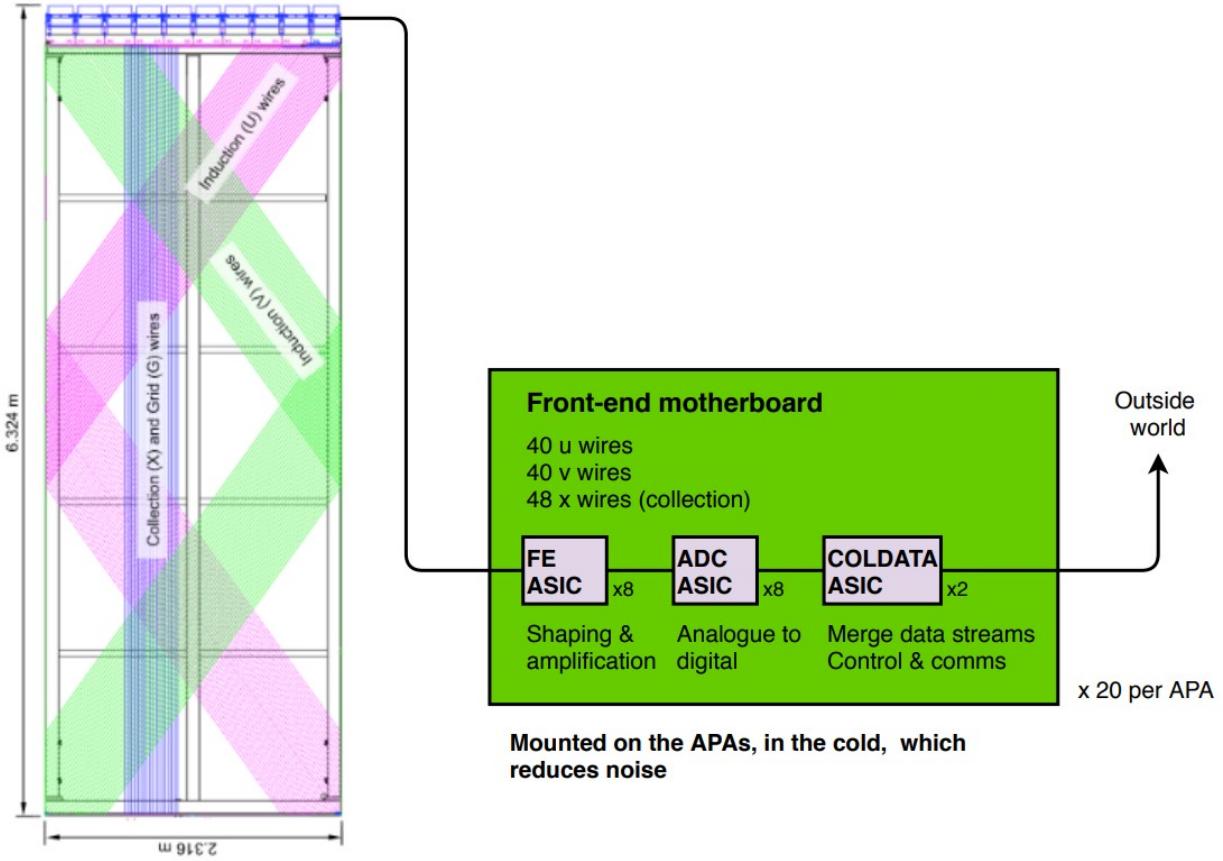


Figure 2.7: Image taken from [38], Fig 1.12 of section 1.8. Image shows an overlay the the relevant charge collection wires within a DUNE-FD SP LArTPC.

ASIC. The second ASIC is the ADC ASIC and is responsible for the converting the analog signal to digital. The final ASIC, called the COLDATA ASIC, merges the data streams from the previous ASICs and is responsible for communication between the motherboard and the outside world.

Table 2.1 summarizes the electronic requirements expected for the DUNE-FD SP module. The maximum expected data collection is expected to not exceed more than 30 PB/year, which corresponds roughly to $\approx 1Gb/s$ of continuous collection. The expected wire electron noise level is design to be $\approx 1000 e^-$. Sampling frequency of 12 bit ADCs is 12 MHz. Large signals require a linear response of $500 ke^-$, and ensures that fewer than 10% of beam events experience saturation. Dune expects to draw less than 50 mW per channel, and incur less than 1% dead channels.

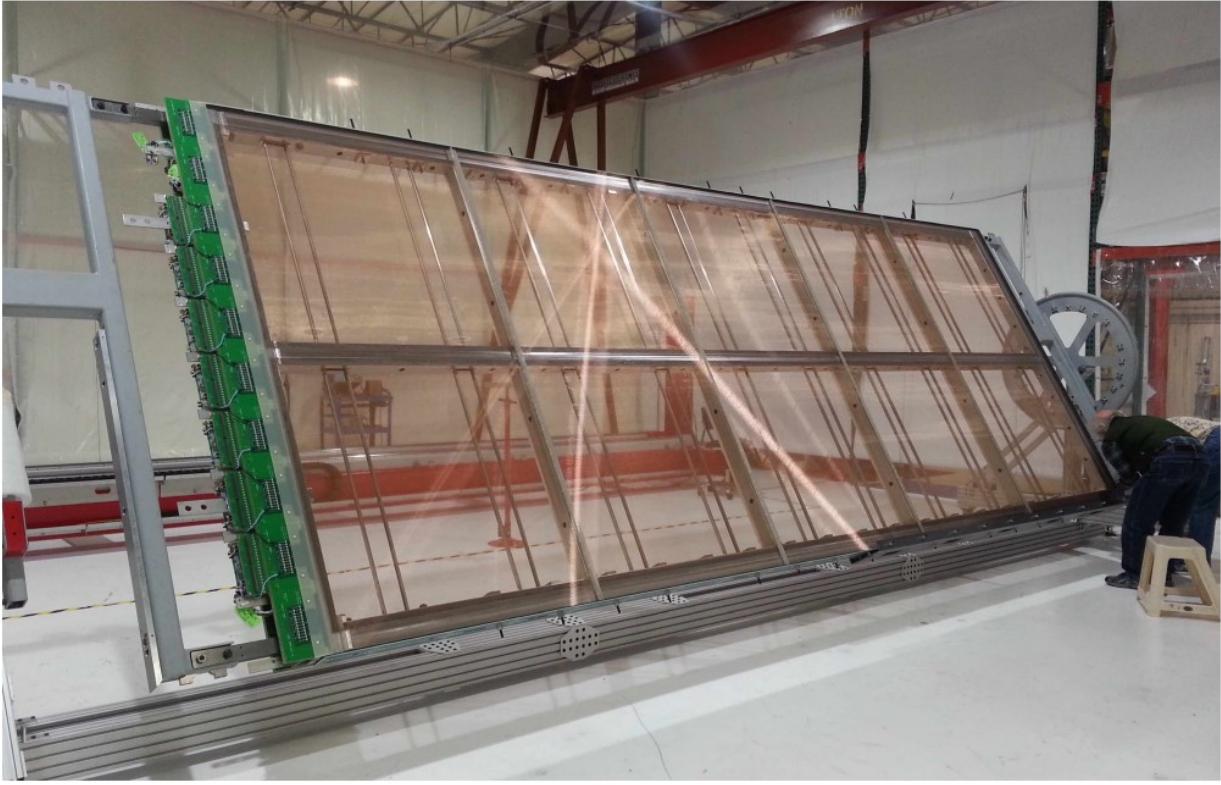


Figure 2.8: Cross sectional picture of a single DUNE-FD APA bracket [38]

Q-Pix Comparison to DUNE-FD Electronics

Each APA is $6.324 \text{ m} \times 2.316 \text{ m}$, for a total area of 14.646 m^2 . From these dimensions the expected channel count of the QPix readout on the DUNE-FD APA is

$$N_{pix} = 14.646 \text{ m}^2 * \frac{1 \text{ pixel}}{4 \text{ mm}^2} * \frac{1000^2 \text{ mm}^2}{m^2} = 915399 \quad (2.8)$$

The total number of free running oscillators (N_{osc}) per DUNE-APA for a given pixel pixel of 4 mm^2 is:

$$N_{osc} = \frac{915399}{16} \approx 57213 \quad (2.9)$$

N_{osc} represents the total number of front-end ASICs whose data must be aggregated and sent outside of the cold electronics to a warm interface. Therefore we expect the order of the number of free running oscillators per DUNE-APA $O(10^5)$. This also gives an order of magnitude estimate of the increase of number of ASICs compared to the MWPC readout of Single-Phase (SP) DUNE-FD.

To have a comparable power consumption to DUNE-FD, which has 2560 channels, then QPix would need less than $\approx 140 \mu\text{W}$ of power consumption per channel. Too much power dissipated in

Description	Specification	Rationale
System Noise	$< 1000 e^-$	Provides $>5:1$ S/N on induction planes for pattern recognition and two-track separation.
Signal Saturation	$500,000 e^-$	Maintain calorimetric performance for multi-proton final state.
Cold Electronics Power Consumption	$< 50 \text{ mW per channel}$	No bubbles in LAr to reduce HV discharge risk
Number of Channels per front-end motherboard	128	The total number of wires on one side of an APA, 1,280, must be an integer multiple of the number of channels on the FEMBs.
Dead Channels	$< 1\%$	Minimize the degradation in physics performance over the > 20 -year detector operation.
Maximum diameter of conduit enclosing the cold cables while they are routed through the APA frame.	6.35 cm (2.5")	Avoid the need for further changes to the APA frame and for routing the cables along the cryostat walls

Table 2.1: Selected Requirements of DUNE-FD TPC electronics and Expected QPix Design goals of first generation ASIC development for comparison. The table information is taken from the inner three columns of Table 4.1 in [38]. Due to the different charge sensitive geometries between a wire and pixel-based readout, the required noise and number of channels are not easily comparable.

the LAr creates bubbles, which is a high voltage (HV) discharge risk. The total number of channels for a 10 kT module is based on 150 DUNE-APAs or $2560 \times 150 = 384000$. Thus, the number of additional analog channels that QPix must measure compared to a typical wire readout increases by a factor of $915399/2560 \approx 357$.

Q-Pix will instead offer conversion from analog (charge) to digital (32 bit time) signals on a single ASIC. These front-end ASICs would be arrayed in modular tiles within a single APA. Where the tiles themselves would be connected and spread out to cover the entire area of an APA.

To connect the entire APA the Q-Pix readout will design modular tiles which will hold a subset of nodes ($\sim 16 \times 16$ ASICs). Each tile will interface with a single FPGA (or other ASIC) chip which would concentrate the digital data for each tile; we refer to this FPGA as the DAQ-Node (DN). Then, each DN can interface could optionally connect a single concentrator FPGA for the entire APA. This final concentrator would send the data to the Warm-Interface-Cards (WIC) out of the

Description	Specification	Rationale
System Noise	$\approx 300e^-$	Provides $\approx 17:1$ S/N ratio, a component of front-end integrator.
Signal Saturation	30 nA per pixel	Upper limit from local oscillator frequency and integrator reset.
Cold Electronics Power Consumption	$< 100\mu\text{W}$ per channel	Equivalent power consumption for heating found in DUNE-FD.
Number of Channels per Tile	4096	Design parameter to be calculated.

Table 2.2: Q-Pix based Requirements which are compared to the equivalent DUNE-FD SP module found in table 2.1. Results here are necessarily speculative, but provide an insight to the design goal. The system noise is a contribution of leakage current per reset, uneven electric fields in the TPC, or uncertainties in the replenishment circuit per reset. Signal saturation is defined as the maximum measurable current based $Q_o = 1 \text{ fC}$ and $f_o = 30 \text{ MHz}$. The Q-Pix readout can also be saturated by too many resets if the FIFO buffers overflow (see Chapter 5 for further discussion). The power consumption per channel is a direct division compared to Table 2.1. The number of channels per tile depends on the tile size as well as the number of pixels per ASIC (see Chapter 4 for further discussion).

cold electronics (CE). The final concentrator FPGA we refer to as the Super-DAQ-node (SDN).

The exact description and characterization of the WIC for a Q-Pix depends on the final implementation of the SDN.

2.3 The Digital Back-end

We define the digital back-end as the part of the larger Q-Pix readout system that is responsible for handling the timestamp data once it is recorded. This sub-system must be able to record and store data, be robust against SPF, define error states, and more.

In this section we introduce considerations which guided the design of the first two Q-Pix ASIC prototypes. These design choices for the digital prototype are enumerated in table 2.3.

Digital ASIC Prototype Design Choices

The Table 2.3 highlights some design choices of the first digital Q-Pix ASIC prototype. Four neighbor connections were chosen as the design choice two allow for communication in either

Parameter Name	Value	Description
Local Oscillator Frequency	30 MHz	Determines maximum current reconstruction (Equation 2.5). Stability of local oscillator also determines z-position reconstruction uncertainty (Sect. 2.1).
Connections	4×2 (Tx and Rx)	Eight differential pair connections are made to support four transmitter (Tx) and receiver (Rx) lines.
Communication Protocol	Endeavor	Protocol determines packet stability based on oscillator frequency as well as packet transaction time. Results of these tests are done in Chapter 4.
Timestamp Bits	32	Determines the total number of unique counts each timestamp value can take. Also determines the "wrap-around" time based on the local oscillator.
Local FIFO Depth	64	Total number of timestamps the ASIC can store before running out of memory. ASIC will not record additional resets until emptied.
Remote FIFO Depth	128	Total number of remote packets ASIC can store before running out of memory. ASIC will not write additional packets from neighbors.

Table 2.3: Summary of design parameters for the first Q-Pix digital ASIC. The local oscillator is a ring oscillator with a targeted mean of 30 MHz. Each ASIC will be able to communicate with up to four neighbor nodes via a custom "Endeavor" protocol. The testing and verification of the endeavor protocol is found in Chapter 4. The values of the local and remote FIFO depth were selected due to fabrication requirements, whose future values are discussion of Chapter 5.

direction along the x and y axes. The local and remote FIFO depths determine how many resets and communication packets the ASIC may store at any one time.

Single Point Failures

Q-Pix digital design should provide “robust resilience” against single point failure (SPF). The readout technology presented here relies on huge numbers of readout channels (10^8) compared to current MWPC designs (10^5). As such, extra care must be made in designing new technology to improve over established, seemingly simpler means.

This principal guides design choices such as the use of independent local oscillators at the pixel-level instead of a provided distributed clock. This design choice, in particular, is discussed at length in Chapter 4, and the findings presented there are one of the major contributions presented in this thesis.

The design which avoids SPF and handles the digital requirements presented here, namely: the continual time calibration of each local oscillator ($N_{osc} \approx 10^5$) is a product of this thesis. However, the amount of data produced depends on the charge collected in each event, therefore the amount of data collected can not be known before recording.

2.4 Q-Pix and Light Detection

The results of this thesis analyze the response of the Q-Pix digital readout without any analysis paid towards photon collection. However, recent progress regarding amorphous selenium (aSe) [68] has been made towards inclusion of an optical system.

The current pixel dimensions of Q-Pix are $4\text{ mm} \times 4\text{ mm}$ which have a total active area of 16mm^2 . Most of this active area is unused for the charge collection pad, which could be as small as drill-hole via (6 mil $<< 16\text{mm}^2$). Most of the remaining area, then, could be plated with a photo-sensitive material (such as aSe).

aSe could capture incoming scintillation photons and provide an additional voltage measurement at each pixel. Depending on the sensitivity, such a measurement could be used to reconstruct tracks by providing a $\frac{dE}{dX}$ measurement, or even be used as a time-tag or a trigger.

The use of a reference trigger could be useful to establish event-time within the same system, and allow adjacent pixels which would receive photons, but not charge, to contribute to time reconstruction. Any reconstructed event requires some T_o time to indicate the start of the event. Typically this is done via scintillation photons from a secondary system, where the photons arrive nearly instantly at the collection planes compared to the slow drift speed of the electrons.

The natural pixelization of Q-Pix required the charge collection can also be used to be sensitive to scintillation photons. These photons could not only provide the required event timing but also provide an additional means of calorimetry and track reconstruction. Additional work is currently underway to demonstrate the viability.

Currently there are two competing geometries to incorporate light collection within Q-Pix. Figure 2.9 shows the vertical and horizontal drift geometries. The vertical drift geometry is an easier design geometry, however the top electrode must not only be able to collect charge it must also be transparent. On the other hand, the horizontal drift geometry solves the transparency problem but involves a more complicated hardware design.

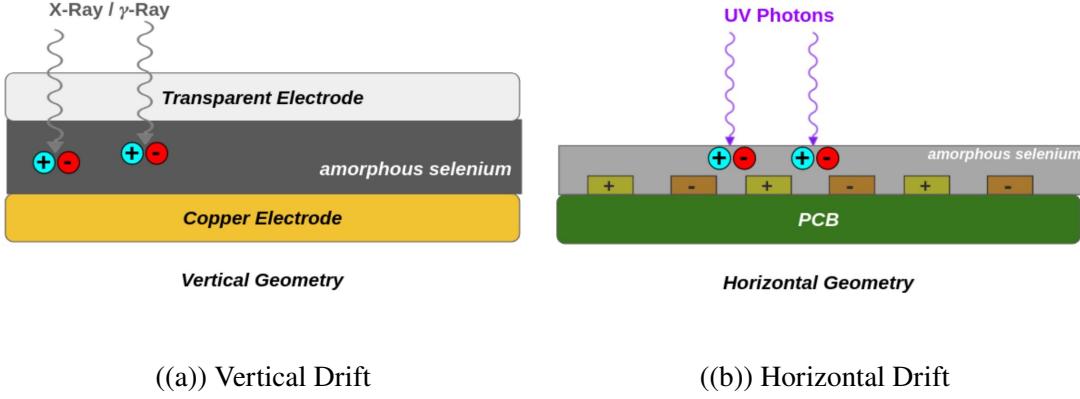


Figure 2.9: Images taken from [68]. The vertical drift geometry (left) shows an electrode on the top layer, whereas the horizontal (right) geometry integrates the electrodes within the aSe. The vertical geometry is an easier design, but most electrodes are not transparent to VUV scintillation light. The horizontal geometry solves this problem, at the cost of a more complicated design.

2.5 Q-Pix at Low Energy: Supernova Studies

Work has been done to characterize a Q-Pix readout ability measure core collapse supernovae [69] events within a DUNE-FD module. These studies involved particle Geant4-based([70]) simulations for low energy ($\simeq 10$ MeV) neutrino events. The results indicate several advantages Q-Pix readout will have over a traditional wire-based readout.

One advantage is the lower overall data rates ($1.03 \times 10^{-6} < 2$ pB per year) compared to the traditional single-phase readout. This reduction in data rates could allow for a 10 kT Q-Pix module to collect timestamp data continually. Such a continuous readout, with no trigger, could be particularly useful in collecting supernova burst events. Figure 2.10 compares the trigger sensitivity supernova trigger burst efficiencies between the Q-Pix readout against traditional wire-readout.

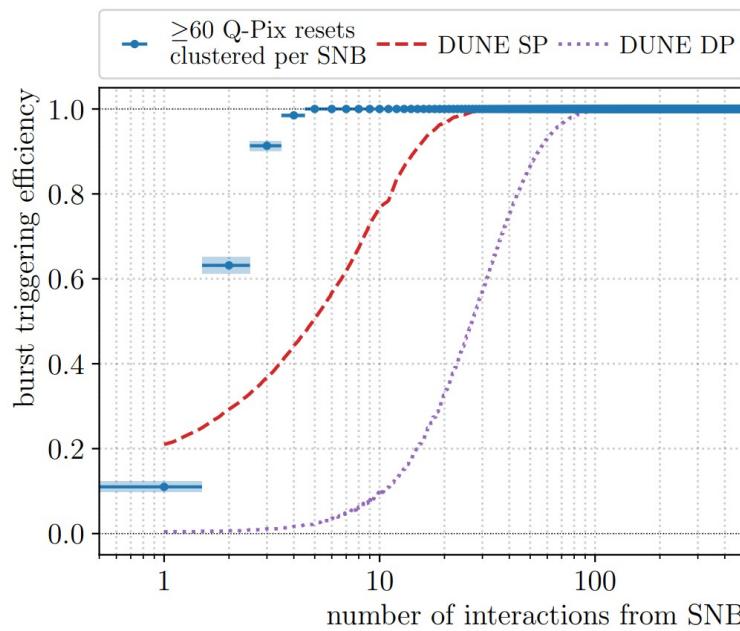


Figure 2.10: Image is taken directly from [69]. Plotted is the supernova burst triggering efficiency as a function of ν_e interactions in a 10 kT DUNE-FD module. The points in blue indicate that a series of 60 resets are "clustered" to use as an identification of a supernova event. The other curves are taken from Ref. [71].

THE FIRST ANALOG PROTOTYPE

In this chapter we present the first implementation of the Q-Pix front-end design using off-the-shelf electronics.

This section describes the first prototype based on the Q-Pix readout: The Simplified Analog Q-Pix (SAQ). First we discuss the design goals of the prototype and highlight the basic building blocks of any Q-Pix based prototype. We present these results as a demonstration Q-Pix timestamp procedure to perform measurements. Next, We describe the prototype status as well as lessons learned in characterizing noise and performing calibrations.

In the final part of this section we briefly describe the future goals of this prototype, including the calibration of the detector response with Gas Electron Multipliers (GEMs) [72]. We emphasize that at the time of the writing of this thesis the acquisition and analysis of data from this experiment are incomplete. Nevertheless, the lessons learned so far, particularly in calibration, are useful to explore the abilities of the Q-Pix readout. The final results of SAQ are just beyond the scope of this work, but we provide SAQ's details here as a means of introducing the front-end of Q-Pix as well as highlighting my personal contributions to Q-Pix's overall development.

The entire data acquisition (DAQ) chain used for both SAQ experimental setups are my sole independent work. My contributions include the the development and deployment firmware on the Zybo-Z7 FPGA, as well as the embedded software code on the integrated SoC processing system. I developed the the Python3 software which handles packet communication as well as the GUI for data collection. I also developed the data storage trees, which are the original containers for all data used in the analysis. Additionally, I wrote analysis scripts used for the work done at the SAQ site at the University of Texas at Arlington.

3.1 Simplified Analog Q-Pix: System Design

The Simplified Analog Q-Pix (SAQ) experiment aims to demonstrate the first physics measurement using the analog front-end of a Q-Pix based readout. The desired measurement is the transverse diffusion of electron in Argon gas (Equation 3.1). In the simplest case, the diffusion of electrons

within a TPC is described by:

$$\sigma_T^2 = 2D_{trans}L \quad (3.1)$$

Where L is the drift length of the electrons, D_{trans} is the (field dependent) diffusion coefficient, and σ_T is the transverse diffusion standard deviation. A Q-Pix readout could perform a measurement of D_{trans} in Equation 3.1 by collecting charge at different radii from the center.

Measurements of Transverse and Longitudinal diffusion of electrons within electric fields of strength 500 $\frac{V}{cm}$ have been performed before [73]. A diffusion measurement is a natural starting point to verify a charge accumulation readout such as Q-Pix. One difference between SAQ and a "normal" Q-Pix readout is that instead of an array of pixels, SAQ uses a series of 16 concentric rings to collect charge. Although a 2-D array of pixels may be used, since transverse diffusion is radially symmetric about the collection plane rings of different radii will collect different amounts of charge according to Equation 3.1. Also, the use of circular 'pixels' reduces the amount digitization channels in the prototype.

SAQ has built two different TPCs: one at the University of Texas at Arlington (UTA) and the other at Wellesley College (WC). The experimental setup at UTA is shown in Figure 3.1, and the setup at Wellesley is shown in Figure 3.2. Both TPCs shown are circular TPCs with a drift length of ≈ 10 cm.

The experimental setups at both UTA and Wellesley are nearly identical except for the placement of the readout electronics. The SAQ readout board for UTA is placed on the outside of the TPC, whereas at WC it is placed within a P10 argon gas, but not within the field cage of the TPC. The drift medium used within the TPC at UTA is an ultra pure (99.99%) argon gas.

Electrons are produced in the TPC from gold foil and a Hamamatsu L13651 [74] Xenon Gas Lamp via the photo-electric effect [22]. As the electrons are removed from the gold, they enter the electric field and are drifted down to a collection plane. A simplified image of the working TPC, rings, and GEM placement are shown in Figure 3.3. The design of the GEM PCB as well as its operating voltages is based on work presented in [75]. The GEM is used to provide a necessary charge amplification ($\gg 10^3$) per channel to induce resets in rings far from the center.

The Integrator Circuit

A schematic of the integrator circuit used in the SAQ experiment is shown in Figure 3.4. The Integrated Circuit (IC) used is the IVC-102 [76], where the selected capacitor is 10 pF. We selected

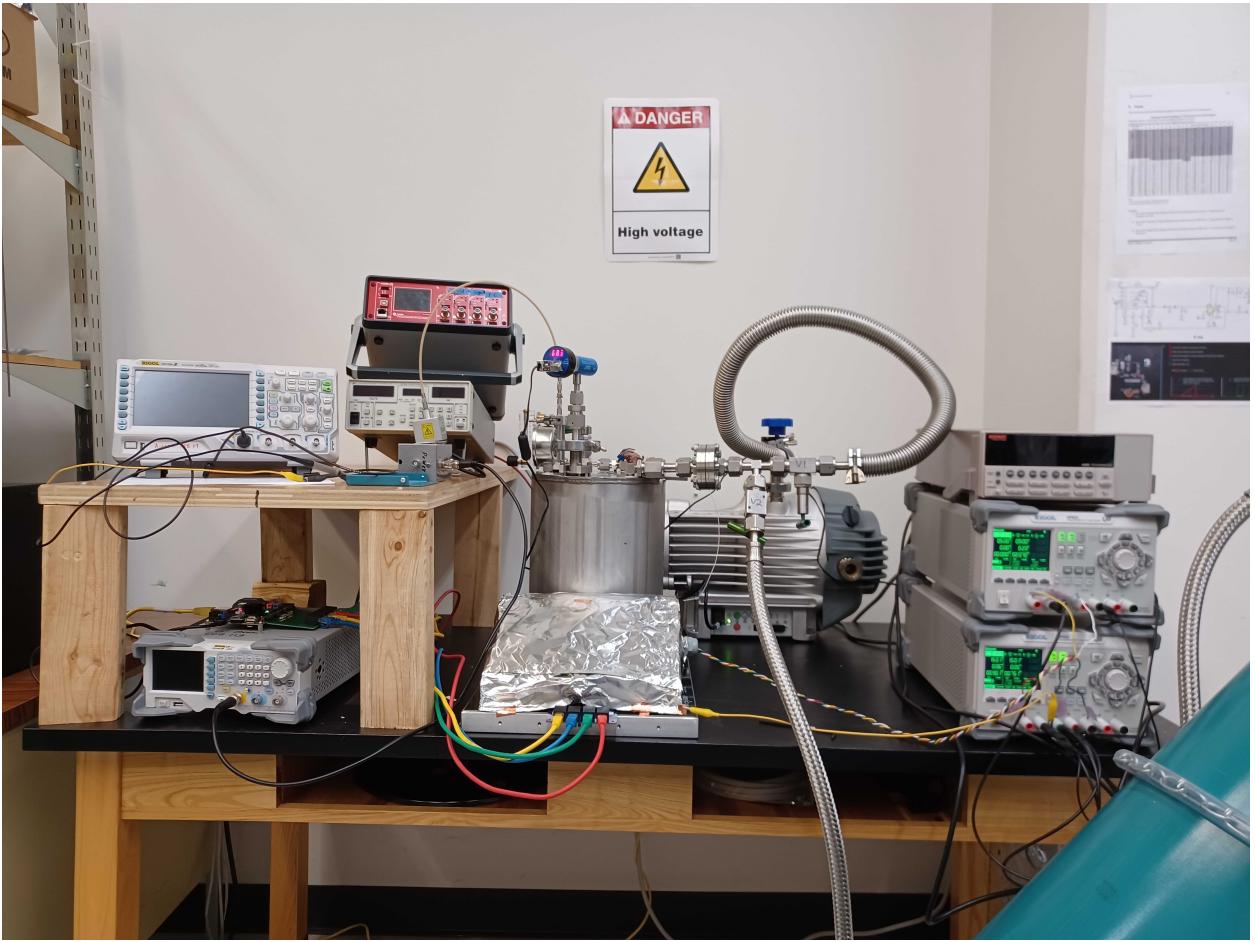


Figure 3.1: The SAQ setup at UTA. In the center is the TPC, SAQ board (Figure 3.5), and pump as shown in Figure 3.3.

the lowest available capacitance of the IVC chip in order to ensure that resets are produced with the lowest amount of possible charge (Equation 2.1). Further configuration of the charge required per reset uses a configurable voltage (VDD in Figure 3.4) with a variable resistor. Charge is accumulated from the TPC as an input into the IVC chip. The comparator (AD8561 [77]) sends an output pulse with a width of $\approx 10 \mu\text{s}$ once the voltage on the IVC exceeds four times the voltage across VDD, due to the voltage divider.

A simplified diagram of how charge-integrate-reset behavior of SAQ is shown in Figure 3.6. The voltage across the integrator increases as charge is accumulated. Once a specific charge (Q_o) as accumulated on the integrator, the comparator sends an output pulse that causes a reset and is recorded by digital back-end. The specific value of charge per channel must be calibrated (Section 3.3). Once the reset stops, charge accumulates until the next reset pulse.

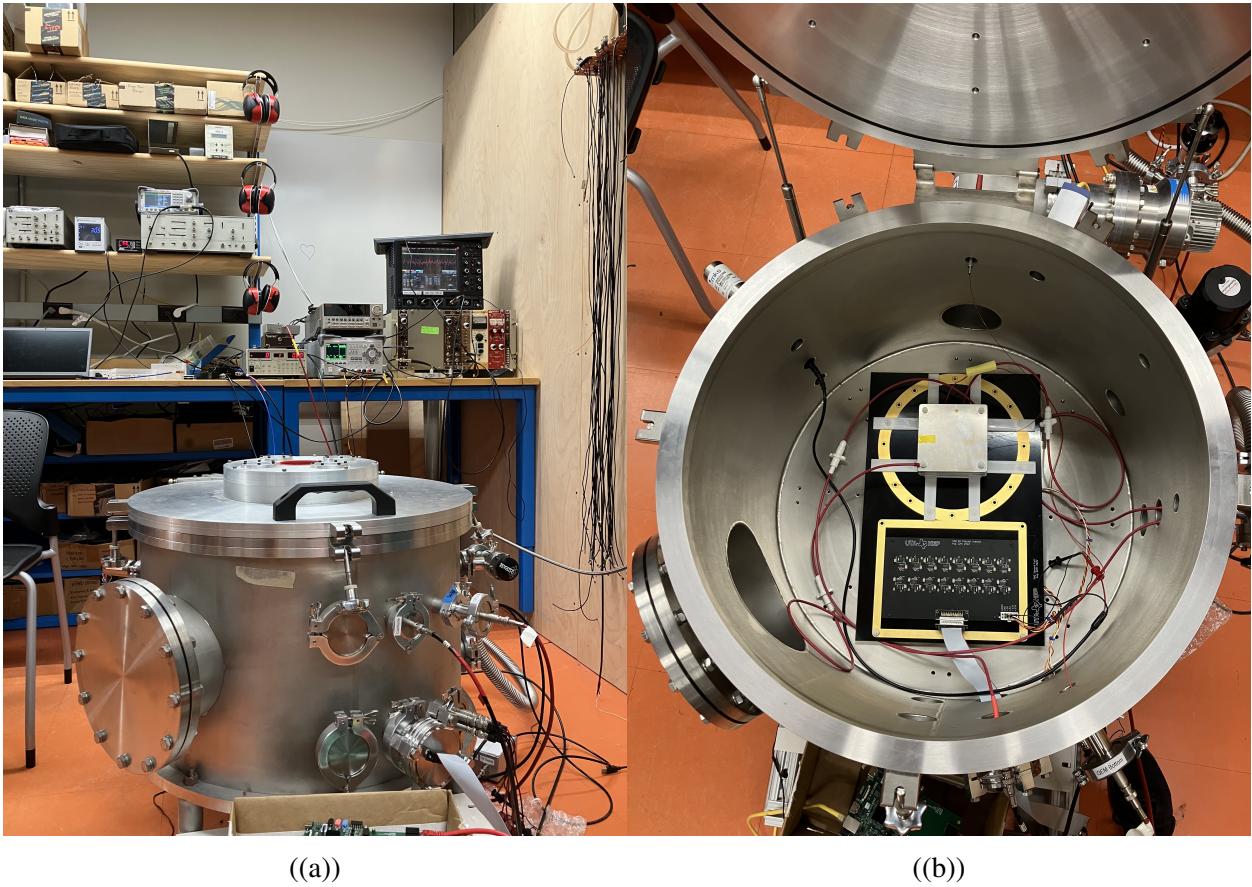


Figure 3.2: Picture of the TPC and DAQ setups at Wellesley University. Image of the TPC cage (left) is used to store P-10 Argon gas. P-10 Argon gas uses a 10% mixture of methane, and prevents sparking from the high-voltage of the TPC. Inside of the TPC (right) shows the SAQ readout board. The SAQ readout board is used at both UTA and Wellesley.

An example of resets produced from the integrator circuit is shown in Figure 3.7. Each reset corresponds to a charge accumulation of $\approx 10 \text{ pC}$. The time difference between each reset shown is equivalent to the amount current accumulated at the IVC (Equation 2.4). The initial reset occurs $\approx 30 \mu\text{s}$ after the flash lamp is triggered, which corresponds to the drift speed of electrons in gas, plus the flash lamp response measurement. The additional resets which occur much latter ($\approx 100 \mu\text{s}$) are from currently unknown sources, and are likely either discharges from the GEM or electronic cross-talk.

3.2 Data Acquisition

All resets are recorded via a Zybo-Z7-20 Digilent FPGA prototype board, which uses an Zynq-7000 System on Chip (SoC). The clock (30.3 MHz) is provided by the Processing System (PS), a ARM

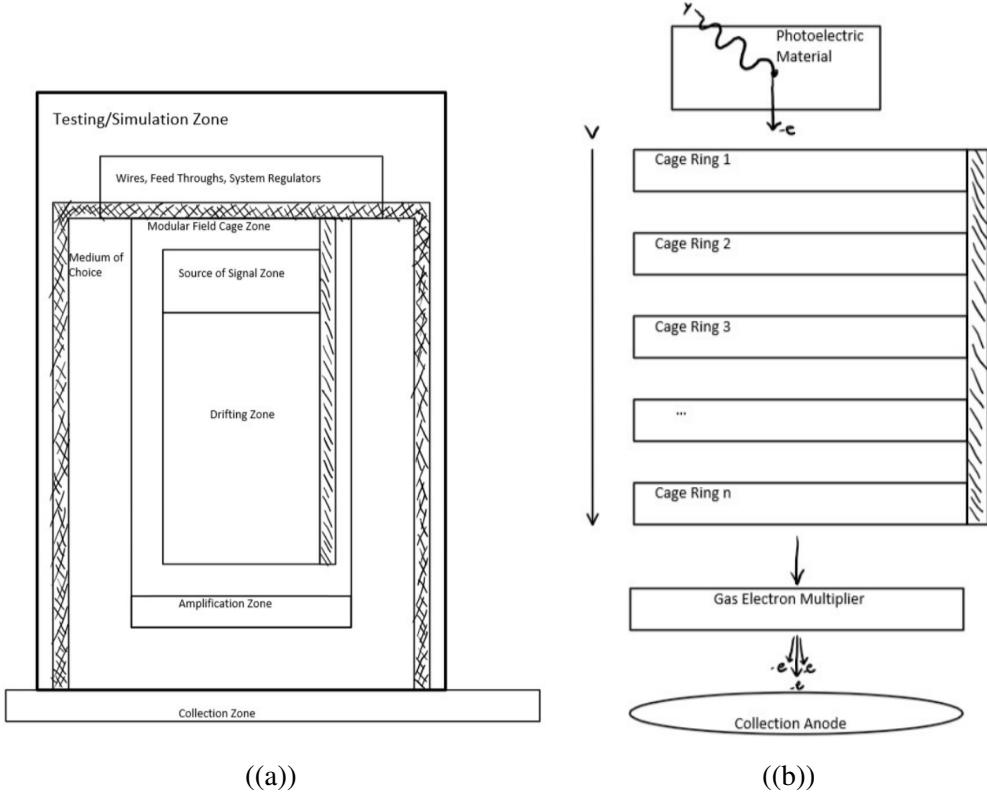


Figure 3.3: The SAQ model shown explicitly Figure 3.1. The TPC (left) shows that the gold foil target for the flash lamp target is at the top of the detector. Electrons are removed and drifted through the rings (right) of the TPC. The rings are separated by ≈ 0.84 cm, where they encounter an average drift field of $500 \frac{V}{cm}$.

Cortex-A9, to the Programmable Logic (PL) in the FPGA. The PL records a 32-bit counter (the timestamp) on the next clock cycle after the reset, connected as a latch to a single pin input, is driven high. The reference manual for the Zybo Z7 board used in SAQ can be found at [78].

The timestamp data and the channel mask are accumulated in a First-In-First-Out (FIFO) buffer. If any one (or more) of the 16 input channels transitions from low to high and the FIFO register is enabled, data are written to the FIFO. The input from all 16 channels are recorded at the time of the trigger, regardless of which channel caused the trigger. Multiple triggers from the same reset pulse are prevented by detecting the edge of the reset pulse. Therefore, in order for a new reset to be recorded on the same channel the reset pulse must first be driven low for at least one clock cycle ($> \approx 33$ ns) to reset the latch at the input channel. This timestamp trigger procedure is identical to the implementation of the Q-Pix digital ASIC presented in Chapter 4.

A flow chart of control system for the Zybo is shown in Figure 3.8. The PS connects to both a

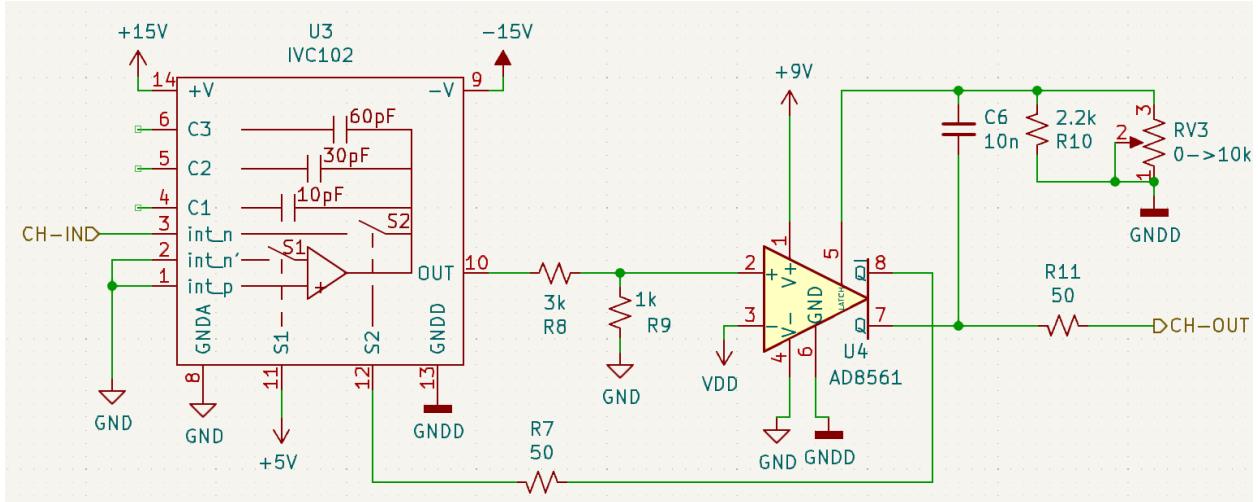


Figure 3.4: A schematic of the front-end CSA and trigger components. The IVC [76] chip chosen as the off-the-shelf integrator for this experiment. This part was selected is due to its low input bias current $\ll 750 \text{ fA}$ and variable capacitance. A voltage divider between resistors R8 and R9 reduces the voltage reference to the comparator by a factor of four. VDD is a configurable voltage which can be tuned per channel.

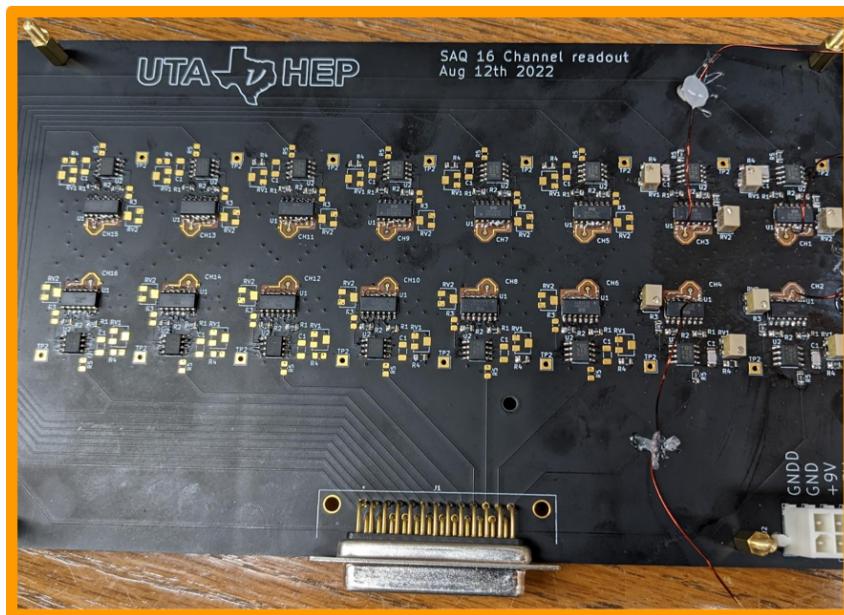


Figure 3.5: The SAQ front-end board of 16 input IVC channels. Each of the 16 channels are based on Figure 3.4.

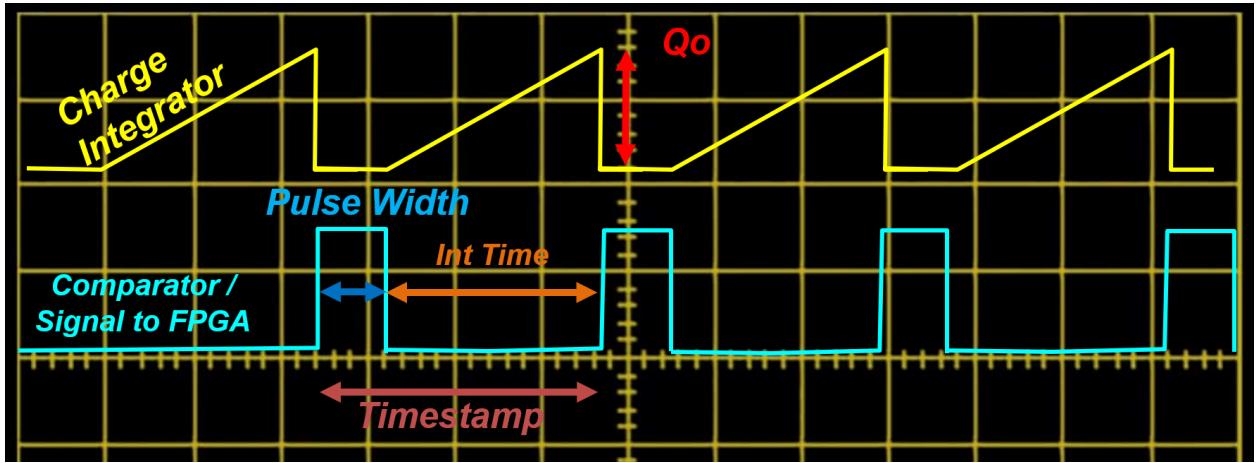


Figure 3.6: Sample voltage waveforms of the integrator (top) and output (trigger) are shown. Charge accumulates on the integrator until a value, $Q_{o,o}$, is reached causing a reset and output pulse sent from the comparator. During the reset, no charge is accumulated on the integrator so the voltage does not change. After the reset completes, charge builds back up on the integrator until another reset. A Reset-Time-Difference (RTD) is the difference between two timestamp measurements, and includes the time of the pulse-width as well as the true integration time.

User-Datagram-Protocol (UDP) and Transmission Control Protocol (TCP) socket on a controlling computer. The UDP socket on the computer is only a listening socket and receives the timestamp data from the Zybo. The TCP socket is used to read and write to the control registers on the PL. Relevant control registers include channel masking, timestamp division, and a write enable to the FIFO.

A summary of the connection ports to the Zybo are shown in Figure 3.9. The Zybo is connected to the PC via a 1 GBs Ethernet link. The SAQ timestamp connections use two right-angle connectors. Also included the Figure is the connection to the Q-Pix Digital Board (QDB) presented in Chapter 4. Reference 10 μ s pulses at varied frequencies (2-256 Hz) are generated in the last marked connector.

A division register is used to configure the relative count rate of the timestamp compared to the local oscillator on the Zybo (\approx 30 MHz). The charge integration period for some channels, especially in tests without the GEM, can take several minutes to produce a single reset. Each timestamp a 32-bits value read from a register counter and wraps-around due to the 30 MHz oscillator every \approx 143 seconds. A division register is used to change the count frequency to correspond to the number of clock cycles that cause the timestamp to increment by one; for example, a division of two will wrap-around every \approx 286 seconds. The maximum division register is also a 32-bit number, and provides a maximum of a 64-bit timestamp, which has a wrap-around of \approx $20 \cdot 10^3$ years at 30 MHz.

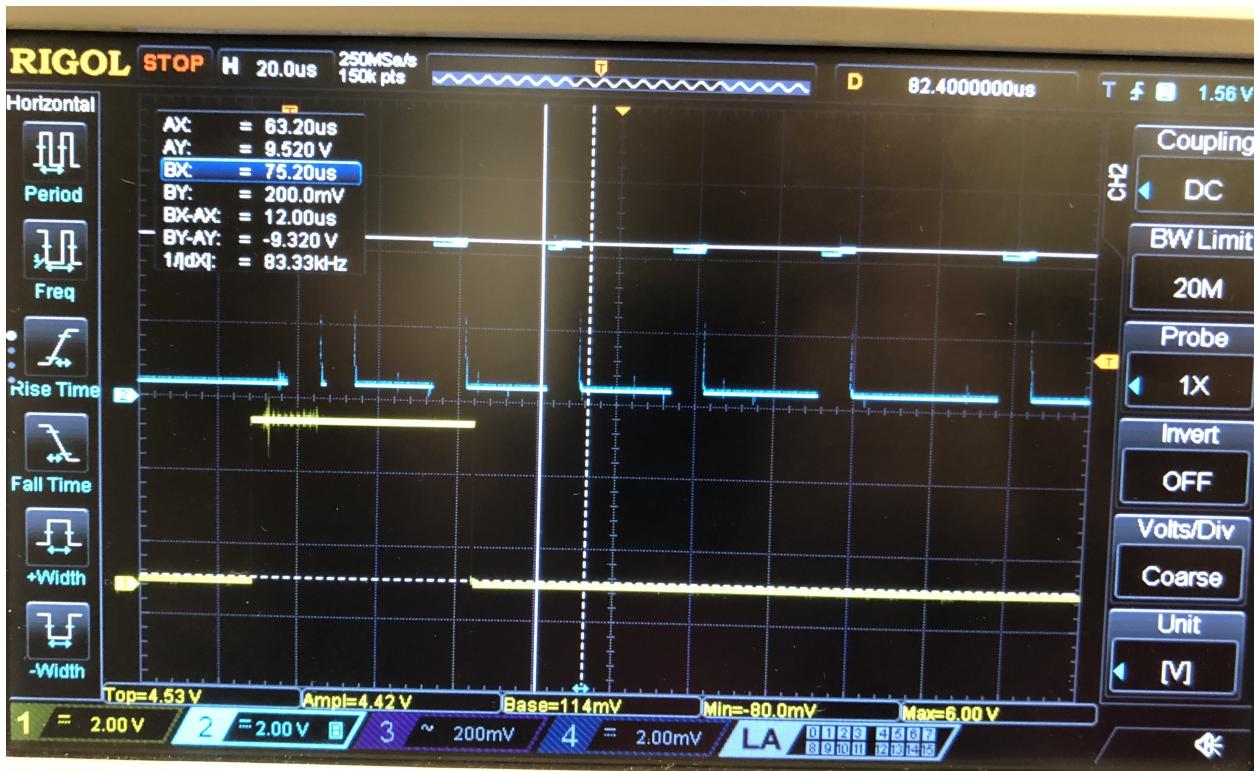


Figure 3.7: Waveform measurements of the trigger sent to the Xenon Flash lamp (yellow, bottom), and the reset pulse responses sent by the comparator. Each reset corresponds to a build up of ≈ 10 pC of charge stored up on the IVC capacitor. Seen in the waveform is a decaying amount of charge buildup on the capacitor, which is reflected in the increasing time separation between successive resets.

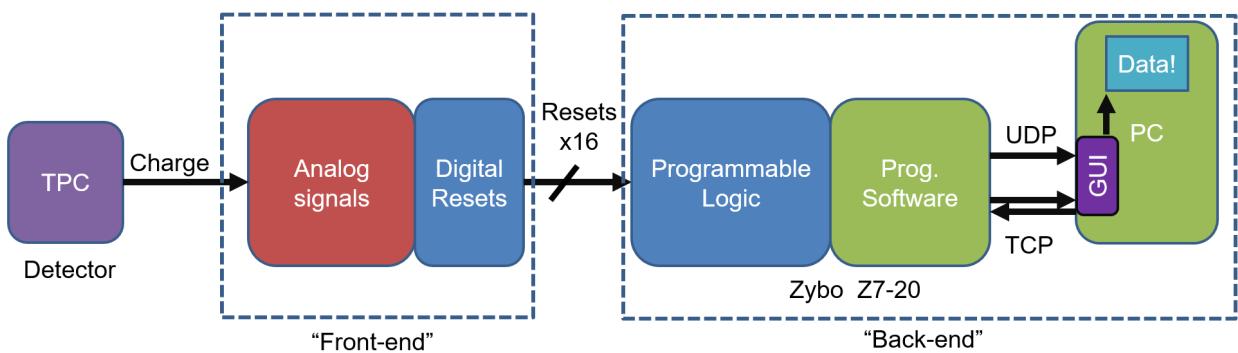


Figure 3.8: SAQ system over view connecting the front-end and back-end parts of a Q-Pix readout. Gaseous Argon is used for the drift medium of the TPCs at both UTA and Wellesley. Accumulated charge is read by the front-end which consists of 16 integrating amplifiers each connected to a comparator used as a trigger 3.4. The back-end board is a Digilent Zybo-Z7-20 (Figure 3.9).

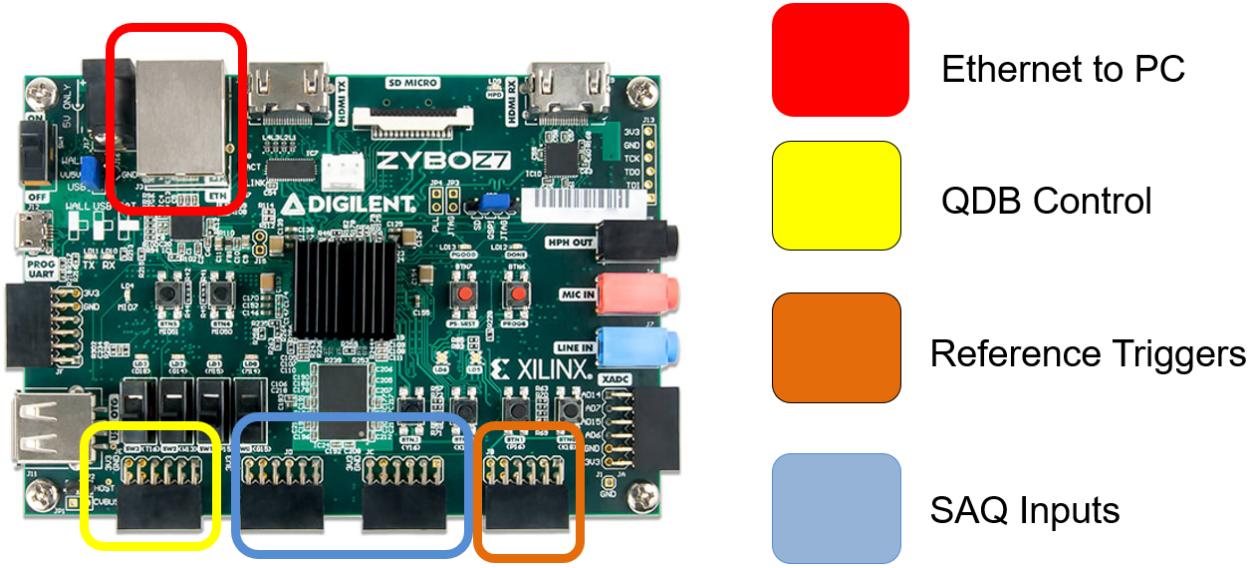


Figure 3.9: An image of the data acquisition board from Digilent, Zybo Z7-20. This board was chosen for its multiple configurable input channels, as well as the Zynq-based architecture of the onboard FPGA. Additionally, the use of the ethernet provides 1 GB transfer speeds, which is more than sufficient for the application. Packet data transfer rates have been verified with this readout at stable rates of 10 kHz. This board is also used to control the Q-Pix Digital Boards (QDB), discussed in Chapter 4.

A summary of the firmware and embedded software is shown in Figure 3.10. The control of the SAQ Data-Acquisition (DAQ) is handled via a Graphical-User-Interface (GUI) which also handles the UDP and TCP sockets. The data collected by the DAQ are originally written as binary packets to the PC, but are eventually parsed into output ROOT files for analysis.

The data are sent from the PL to the PS and finally to the PC once a (register controlled) number of timestamps are written to the FIFO. The AXI-Sream FIFO packages the timestamp and channel data in to a singular packet that is then written to the DDR3 memory in the PS. The PS receives an interrupt signal from the DMA to notify that it received a new packet of data. The PS then sends all timestamp and channel mask data as a single packet via UDP. One additional byte is appended to the packet and include the number of timestamps included in the packet as well as a packet identification number. The controlling software uses the identification number to flag for any missed packets to notify the user of possible missing data.

3.3 Status and Calibration Procedures

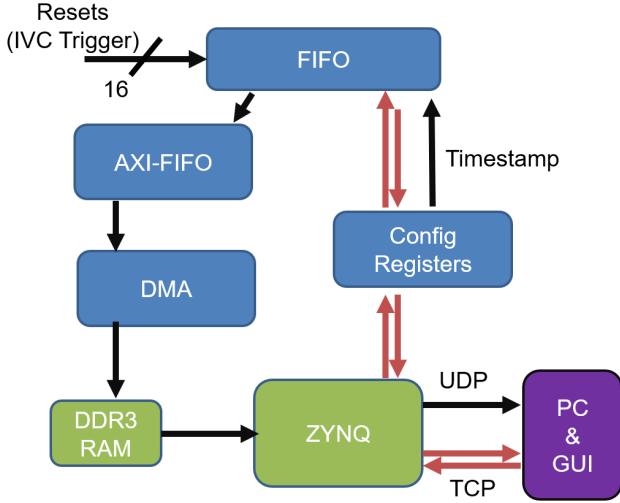


Figure 3.10: A flowchart of the firmware (top, blue), and the embedded software (bottom, green), within the Z-7000 SoC. A FIFO is used to collect the timestamp and channel mask output from the SAQ Board 3.5. The AXI-FIFO and Direct-Memory-Access (DMA) send data from the FIFO once a (register controlled) number of timestamps have been written to the FIFO. These data are collected by the PS and sent via UDP to the PC. The control registers are configured via TCP within the same GUI (Figure 3.11) application that collects and provides real-time plotting of the timestamp data.

The Q-Pix readout is dependent on two factors (Equation 2.5): the charge and frequency calibrations. The frequency calibration depends on the stability of the local oscillator and its reliability to accurately record the time of reset. A drifting local oscillator on the digital board, the Zybo for SAQ, will cause poor reconstructions of current.

A clock calibration is performed by using a reference clock to provide input to the test clock. The test for the stability of the Zybo is performed with a fixed trigger (10 kHz) into the Zybo. The pulse frequency of 10 kHz is chosen so that the pulse width is identical to that produced by the IVC chip (Section 3.1). The reconstructed timestamp difference gives the period of the input trigger. Figure 4.25 shows the Zybo measurements in response to a 10 kHz function generator with 1 ppm.

The effective charge calibration per pixel uses a constant current source as an input to each channel. A current source is used to deposit a known quantity of charge, which is related to the number of resets by:

$$\Delta Q = I_o t = N_{reset} Q_o \quad (3.2)$$

Where Q_o is average charge per reset, I_o is the input current from the source current, and N_{reset} is

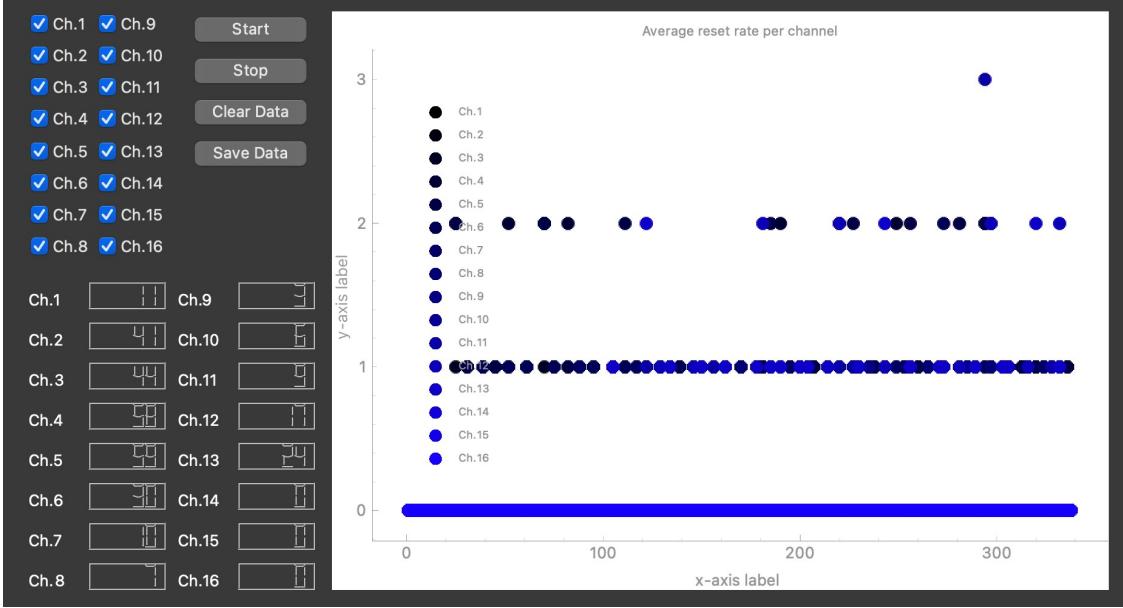


Figure 3.11: The SAQ GUI with real time plotting of incoming resets to the Zybo board. Every second the GUI updates the number of resets acquired by each of the channels in the previous second. The GUI allows channel masking features of individual channels shown by the checked boxes in the top left.

the number of resets observed in time t . Then, the charge calibration is:

$$Q_o = \frac{I_o t}{N_{reset}} \quad (3.3)$$

Equation 3.3 is accurate in the limit that the time difference between successive resets is large compared to the pulse-width. Charge is not accumulated for $10 \mu\text{s}$ after every reset, so if the distance between resets during calibration is $\approx 1 \text{ s}$, the amount of charge lost during the reset is $\frac{\delta Q_o}{Q_o} \simeq 10^{-5}$.

The Leakage current is measured using a Keithley-6485 [79] pico-ammeter and a nominal estimation of the leakage in the presence of only field and gas measured to be $\approx 0.9 \text{ pA}$ per channel. Leakage current arises due to non-ideal behavior of the integrator operational amplifier, where the voltage across the two input terminals is nonzero. The voltage difference causes a continual build-up

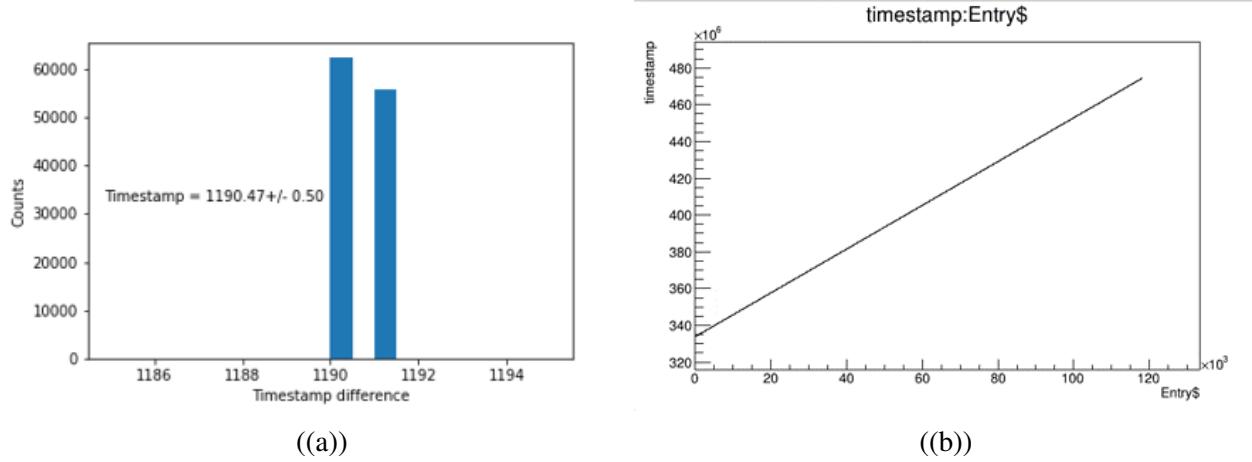


Figure 3.12: Image of calculated RTDs (left) between successive triggers to the Zybo and the running plot of the timestamp value measured (right). The clock period on the Zybo was reconstructed to within a single clock cycle, as shown on the left image. The period of a 10 kHz signal is $100 \mu\text{s}$ and does not result in an even distribution of clocks, which is why two peaks are shown. The expected RTD will come no faster than 90 Hz, which is more than two orders of magnitude slower than tested here.

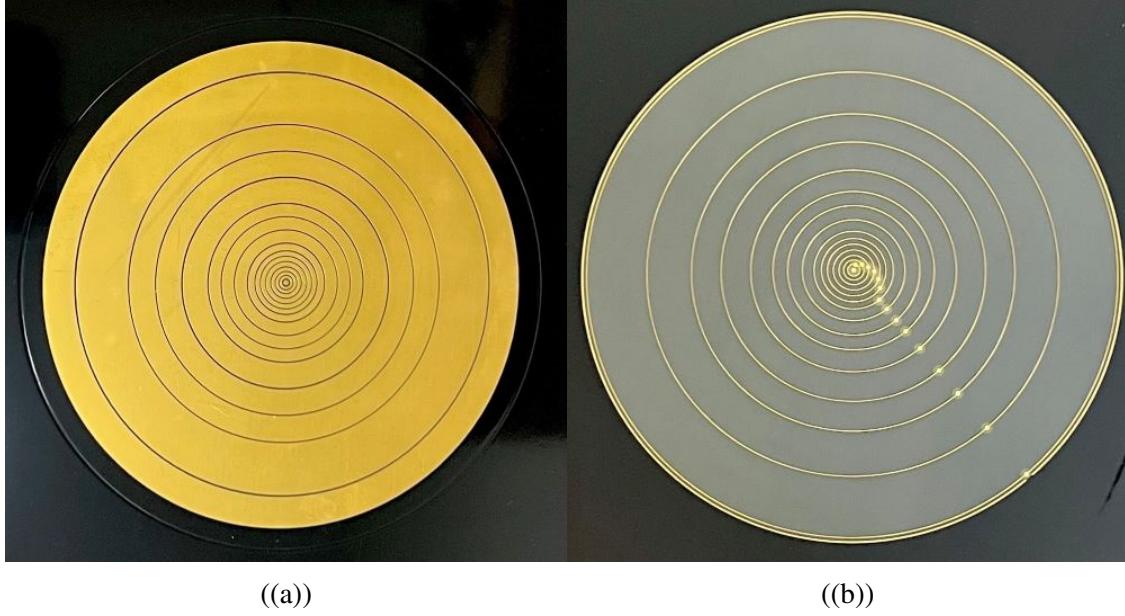
(or removal of) electronics from the capacitor in the integrating circuit. Since each reset requires $\approx 10 \text{ pC}$ of charge, the leakage removes roughly one reset from a pixel every 11 seconds. Therefore, any charge introduced by drift in the TPC to trigger a reset should deposit charge more quickly than 11 seconds to ensure minimal charge loss from leakage.

Current Results

Two different collection plane geometries are tested. The two different geometries change the amount of exposed copper and are shown in Figure 3.13. The "thin" trace (right image) board exposes 6 mm wide copper rings around the center of the TPC. The "thick" trace board inverts the silt-screen and exposed copper and instead separates the collection rings by 6 mm wide silt-screen traces.

Examples of data taken with the two collection boards at UTA are shown in Figure 3.14. These data represent multiple five minute charge collection runs using the thick and thin trace boards. One of the current uncertainties is the large difference for the outer channel.

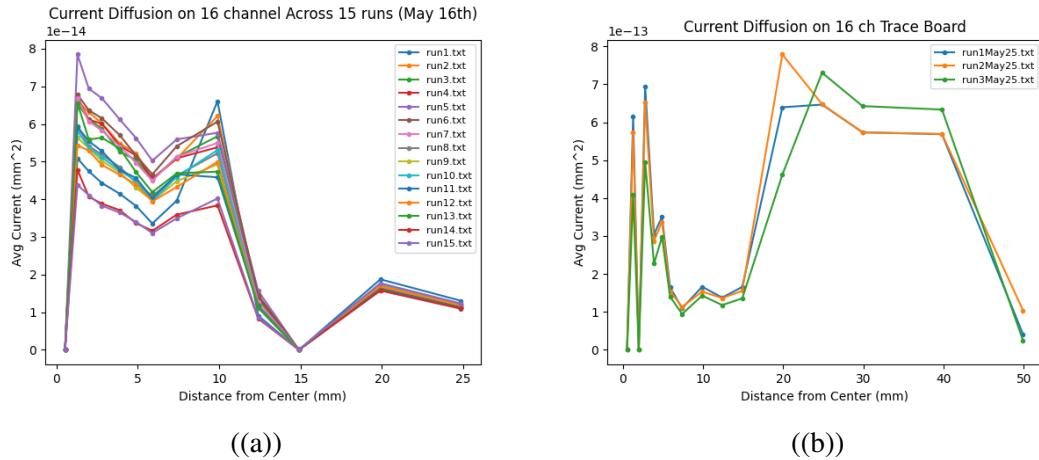
A plot of initial results from the WC group are shown in Figure 3.15. These data represent an averaged number of resets divided by the area of the ring on the collection board. These data indicate that center channels acquire more charge (produce more resets) than outer channels.



((a))

((b))

Figure 3.13: Different Trace Boards used in the SAQ Experiment. The thick trace board (left) differs from the thin trace board (right) in that most of surface area is exposed copper target for the drift electrons. The thin (right) trace board replaces the collection rings with silt-screen, and the silt-screen with collection rings. Because the traces are so small, vias are used to connect the thin collection rings to the input of the integrator channels.



((a))

((b))

Figure 3.14: Different Trace Boards used in the SAQ Experiment. The thick trace board (left) differs from the thin trace board (right) in that most of the surface area in the field cage can collect electrons. The thin (right) trace board replaces the collection rings with silt-screen, and the silt-screen with collection rings. Because the traces are so small, vias are used to connect the thing collection rings to the input of the integrator.

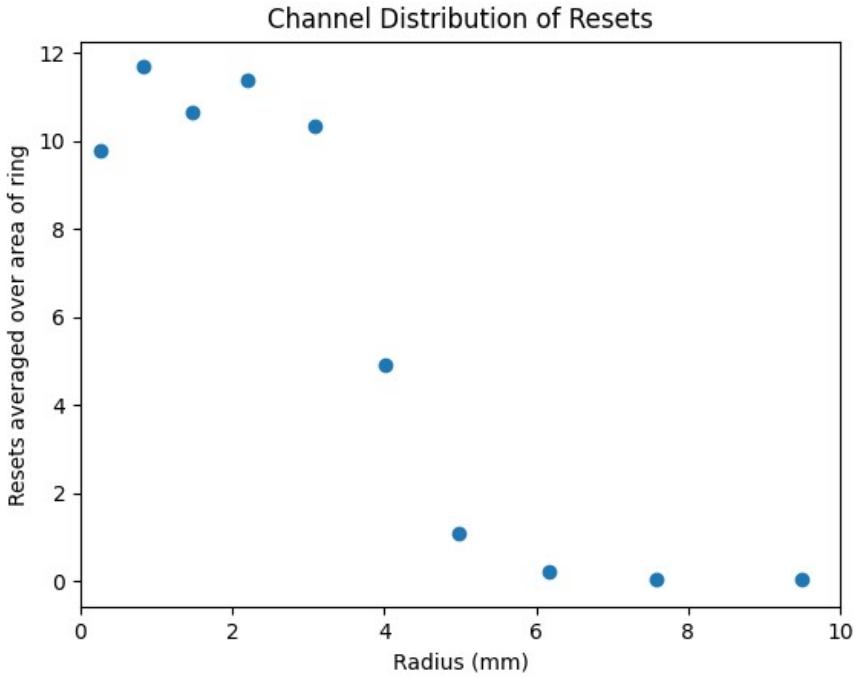


Figure 3.15: First diffusion measurement in P-10 gas performed at Wellesley University. The "double peak" feature is thought to be due to an offset center electron source. Analysis is currently underway to characterize how charge collection would vary from an offset electron center.

3.4 Summary and Future Tests

Although the diffusion measurements of SAQ are not complete at the time of the writing of this thesis, the work contributed by the author has been demonstrated. Timestamp data for various gas based TPCs have been collected and been shown to result from accumulated charge on an integrating circuit. These first tests demonstrate the Q-Pix front-end capability with off-the-shelf components. The work that remains for SAQ is a characterization of the TPC, GEM, and electric fields, not the front-end readout technology, which is the aim of this thesis.

Work still remains to understand charge accumulation data presented at UTA (Figure 3.14) and WC (Figure 3.15). Simulations are being performed to understand the differences between the electric fields with the two different charge collection boards. Additional tests are underway to understand the behavior of the GEM, and to deduce the charge source causing the delayed resets in some channels, as seen in Figure 3.7.

THE Q-PIX DIGITAL BACK-END

In Chapter 2 we introduced the Q-Pix readout concept, where in Section 2.3 we introduced the concept of the digital back-end. This chapter is dedicated to fully exploring the requirements of a Q-Pix digital back-end, where we discuss the design of the first digital prototypes to test this readout.

In Section 4.1 we describe the operating behavior of the first Q-Pix digital ASIC. We describe the relevant communication procedures, configuration registers, and other design choices. We complete the discussion of the prototype behavior in Section 4.2 where we describe the Finite-State Machine (FSM) and control logic of the ASIC. Next, in sections 4.3 and 4.4 we introduce and discuss the design challenges required of the digital back-end.

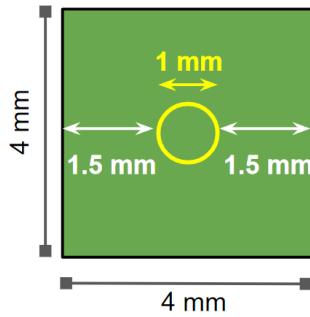
Section 4.5 introduces a new calibration procedure for the digital readout. We test this procedure on the first digital prototype boards presented in Section 4.7. The Lattice Semiconductor FPGAs [80] were selected because of the small form factor, pin out, availability, as well as low power consumption. This calibration procedure is an essential capability to be able use free running oscillators in the Q-Pix readout to meet the timing requirements [67].

Finally, we conclude this chapter with a discussion on the the next steps to extend this readout into a DUNE-FD LArTPC.

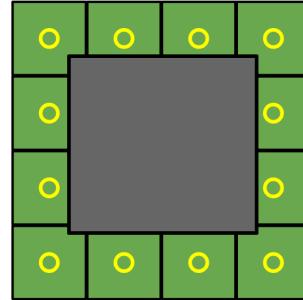
The results presented in this chapter that are my individual work include the development of the prototype test boards, the soft-trigger and routing behavior of the digital ASIC, the development and verification of the calibration procedure, as well as the formalism to describe the collection of digital nodes.

4.1 The Digital Back-end and The First Digital Prototype

The digital system of the Q-Pix readout begins when the first digital data are recorded. This occurs during the collection of a recorded timestamp in response to the logic reset pulse sent from the Schmitt Trigger from analog front-end. These triggers are sent as the response from a build up of



((a)) Single Charge Collection Pixel



((b)) Q-Pix ASIC connected to 4×4 pixels

Figure 4.1: Each Q-Pix ASIC (B) is expected to connect to up 16 pixels (A) within the LAr. The dimensions of each pixel are $4 \times 4 \text{ mm}^2$, where the collection ring has a diameter of 1 mm. Each ASIC supports up to a maximum of 16 channels, or pixels.

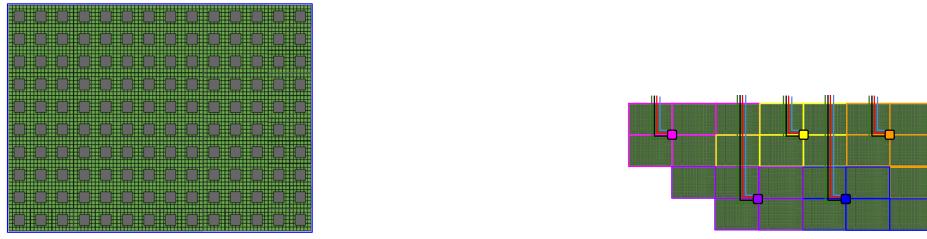
charge on a pixel in a LArTPC (Section 1.2). An example of a pixel ring with a connected ASIC are shown in Figure 4.1.

This record happens in response any one, or more, of the pixels, which for the first ASIC prototype is up to 16. The timestamp is the value of a local 32-bit counter at the time the ASIC receives the reset pulse. When a trigger is sent from any pixel the data recorded are local counter as well as the input level of all pixels ('1' indicates high, '0' indicates low).

The full Q-Pix digital back-end is a collection of interconnected ASICs that form tiles. Tiles are then connected to controlling nodes as shown in Figure 4.2, indicated by the colored boxes. In order for the system to work each ASIC must be able to send and receive data, which are routed to and from its tile via the controlling nodes. The sheer number of pixels required for an DUNE-FD 10 kT module require an extremely reliable means of charge and time calibration, stable buffer depths, and protection against single-point failure (SPF).

The logical components of each ASIC are represented in Figure 4.3. These components are responsible for controlling the basic features of the ASIC including communications, configuration, and data collection. Data communication between ASICs is of primary consideration, since all recorded data must be transmitted between ASICs, through aggregators, and eventually to a storage disc.

The QPixComm module describes the communication layer of the ASIC, and determines how to communicate with the ASIC, described in Section 4.1. To allow flexible communications, each transaction is capable of being encoded to serve different functions within the ASIC. Each ASIC is able to determine its appropriate response to a packet based on its contents; this procedure is



((a)) A single tile of 10×14 Q-Pix ASICs

((b)) An array of inter-connected tiles.

Figure 4.2: A modular tile (A) of Q-pix ASICs can be inter-connected (B) to create a larger charge collection plane. The highlighted nodes in (B) indicate possible locations aggregator nodes to interconnect multiple tiles from a single controlling node. These aggregators can connect power, clock, ground, and data out of the full detector which are represented by the four colored traces leaving the tile array.

described in Section 4.1.

Dynamic programming of remote routing is a key feature of the Q-Pix back-end design. Although each ASIC currently supports the ability to route itself, the results of Chapter 5 indicate that routing updates of a tile are better suited to the aggregator. The controlling node can update a register within any ASIC to purposefully direct its routing. Each ASIC is also capable of determining its location within a tile, as well as controlling its routing via register information, described by the QpixRegFile block. We provide further detail the various control registers in Section 4.1.

Finally, the data collection module, QPixDataProc, controls how the ASIC records triggers sent from the analog front-end. We describe the ASIC's response to pixel triggers in Section 4.1

Inter-ASIC communication via endeavor protocol

The data must be transmitted between ASICs. Since one design feature of the Q-Pix readout require that the ASICs have independent oscillators, the communication between neighbors is necessarily asynchronous. Each ASIC permits up to four neighbor connections as shown in Figure 4.4.

The asynchronous communication protocol used is called an "Endeavor" protocol, which was originally developed for the Asynchronous Multi-ASIC Communication version 2 (AMACv2) ASIC. The endeavor protocol was specifically designed for high-speed asynchronous data communication between neighbor ASICs. An example of a transmission of data using this protocol is shown in Figure 4.5.

Data are sent one bit at a time following the procedure shown in Figure 4.5. The procedure follows

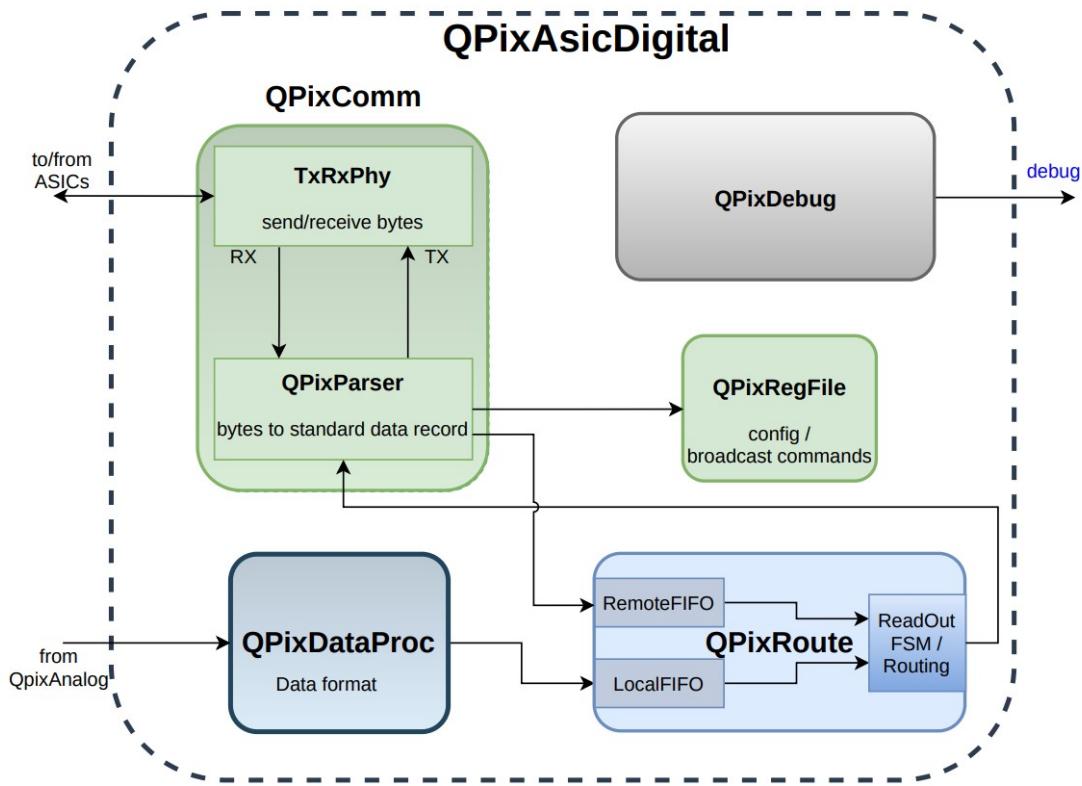


Figure 4.3: Diagram of the different components of the digital node. Shown are the different sections of the control logic for the ASIC: QpixComm, QpixDataProc, QpixRoute, and QpixRegFile. The QpixComm layer is responsible for routing packets between the physical layer and handles the parsing of incoming data packets. The QpixDataProc layer is responsible for recording timestamp data during a reset from the analog front-end. The QpixRegFile contains configuration information, such as routing, ASIC location, and the timestamp counter. QpixRoute determines the controlling state machine that, based on register configurations, determines what packets are sent to which neighboring nodes. The Remote and Local FIFOs determine the packet memory of the ASIC. The QpixDebug layer connects internal signals (such as the local oscillator) to external pins for planned futures tests of the ASIC prototype.

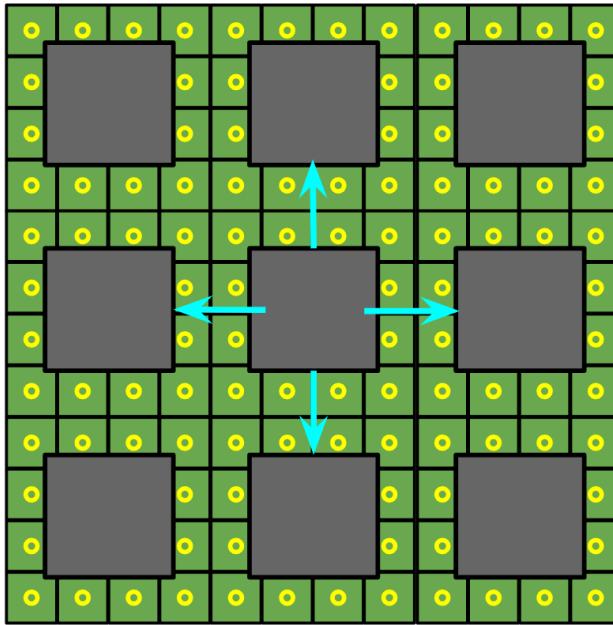


Figure 4.4: Every ASIC permits connections to its neighbors in the cardinal directions. Each connection is two pairs of differential connections which permit asynchronous data transfer. Four connections of two pairs of differential connections require a total of 16 PCB traces to fully connect an ASIC to four neighbors.

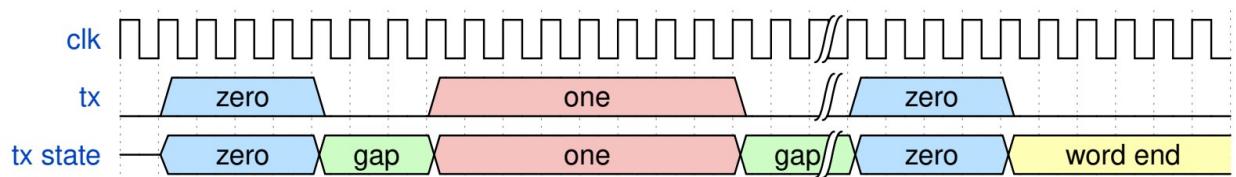


Figure 4.5: Diagram of the endeavor transmission (Tx) protocol. The primary components of the endeavor protocol involve how long the transmitter (Tx) drives the signal high. The receiver (Rx) counts how long each signal is driven high, then based on the count it determines whether the transmitter intended to send a '1' or a '0' bit. The convention used in the prototype ASIC sends a '1' bit for twice the number of clock cycles it will send a '0' bit. After a bit is sent, there is a gap period where the Tx preps the Rx for another bit. The conclusion of the transmission occurs after 64 bits have been sent, where the Tx holds the signal low for longer than a normal gap word indicating the packet is complete.

that a Tx drives the transmission line high for a variable time to send either a One ('1') or a Zero ('0') bit. After each bit is sent, the Tx drives the line low for a period known as the 'Gap'. A transaction is complete when 64 bits have been sent, and the Tx drives the line low for a longer period known as 'Finish'. The range of clocks for acceptable states are described in Table 4.1.

We refer to a completed transaction of data between neighbor ASICs as a "packet". For simplicity, each ASIC expects that every data transaction will send (and therefore receive) exactly 64 bits. A packet is constructed where the first bits that are sent are the "lowest bits" of the packet.

The ASIC reads the packet by first inspecting the "type" of the packet, which are controlled by "packet header". The packet header bits are the four bits sent as the 57th through 60th bits in the packet. We refer to "bit location" as the order of the bit sent in the Endeavor transaction, where the packet sends the 1st bit, and concludes with the 64th bit. There are four bit locations shared by all packets:

- Y Location of sending ASIC: 33–36
- X Location of sending ASIC: 37–40
- Packet Header: 57–60
- Unused Bits, but required for valid packet: 61–64

When an ASIC receives a valid packet, the ASIC enables a valid signal. The packet is handled based on the bits within the header of this packet. How the packet is handled is determined by the packet header 4.1.

If the packet originated from the aggregator node then this packet is treated as a broadcast. Broadcast commands record unique numbers associated with this request and are also sent to all connected neighbors except from the direction that the broadcast is received. A unique broadcast number is used to avoid registering the same request.

If the packet was not from an aggregator node then this packet is treated as "remote packet" from a neighbor node. All data transfers of any kind are treated so that all communication happens between individual nodes and an aggregator node. Therefore, any packet that originates on a node that isn't the aggregator node will be sent to the aggregator node. The direction of that this packet is sent is determined by the configuration register.

Bit	Allowed Minimum	Allowed Maximum	Sent by Tx	Purpose
Zero	4	12	8	Number of Clock cycles Tx drives signal high to send a '0' bit.
One	16	32	24	Number of Clock cycles Tx drives signal high to send a '1' bit.
Gap	8	32	16	Determines range of clock cycles Tx should drive low to pause between next bit.
Finish	40	None	40	Determines minimum number of clock cycles Tx should drive signal to indicate packet is complete.

Table 4.1: The parameters of the Endeavor protocol used by the Q-Pix digital prototype discussed in this thesis. The column 'Sent by Tx' indicates how many clock the Tx will sent during each step. The Zero and One bits indicate the number of clock cycles that the Tx line should drive the signal high to send a '1' or a '0' bit, respectively. The Gap and Finish are used to prep the Rx to receive the next data bit or to indicate the packet has finished. The ASIC will only accept packets that contain exactly 64 bits. An example of this protocol in use is shown in Figure 4.5.

One important note about the Endeavor protocol is that the transaction time of the packet is not constant. The number of clocks required to send a '1' bit differs from the number of clocks for a '0' bit. However, it is straight forward to show that the number of clocks the Tx will use to send a packet is give by:

$$N_{clocks} = N_{One}N_1 + N_{Zero}N_0 + 64N_{gap} + N_{finish} \quad (4.1)$$

Where N_1 and N_0 refer to the number of bits within the 64 bit sequence will be '1' and '0' respectively. The values N_{one} , N_{Zero} , N_{gap} and N_{finish} can be taken from Table 4.1. However since each packet must contain four zero unused bits, and $60 = N_1 + N_0$, Equation 4.1 can be rewritten as:

$$N_{clocks} = 24(60 - N_0) + 8N_0 + 64 * 16 + 40 \quad (4.2)$$

If we assume the average packet has equal high bits and low bits, $N_0 = 30 + 4$, the average clocks in a transaction is:

$$N_{avg} = 24 * 28 + 8 * 34 + 64 * 16 + 40 \sim 2000 \quad (4.3)$$

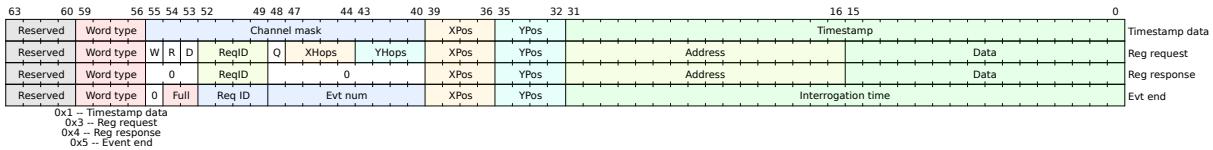


Figure 4.6: Example of Datum words and their allocation as currently implemented in the simulation and first prototypes. The two types of data packets (Table 4.4) are timestamp data and event end data which are used to record reset times and interrogation times respectively. The interrogation time is described in Section 4.1. The Register Request packet is special because it can only be created by an aggregator node, described in Table 4.3. The Register response is created and sent back to the aggregator node in response to a request,.

Types of Packets

How each digital node responds to a successful packet transaction depends on the packet header. One primary development goal for the Q-Pix digital ASIC is to make the simplest design possible that achieves its goals. To this end, there are only four different types of packets words used, as shown in Figure 4.6.

The timestamp and event end packets are created by each ASIC and represent true data for analysis. The Register Request and Register Response packets indicate communication between an ASIC and an aggregator.

The Register Request is a special packet that can only be created by an aggregator node; The Q-Pix digital ASIC can not create a Register Request packet. This packet contains a special bit (48) that indicates if this packet came from the aggregator node, and is only valid on the first ASIC which sees this packet. If this packet is configured as a broadcast (See Section 4.1), or to another node, the ASIC will send this packet identically except with bit 48 ("Q" in Figure 4.6) held low.

The Register Response packet is created by an ASIC to send to an aggregator node upon a register read request from an aggregator. When an ASIC receives a packet that isn't a register request, it knows that this packet did not originate from the aggregator node, and therefore handles these packets identically, described in Section 4.2.

Configuration Registers

The configuration of the digital node is handled through local registers. These registers can only be updated when an ASIC receives a Register Request from an aggregator node.

Address	Name	Function
0x01	Command	four bits are used to select hard and soft interrogations, full ASIC reset, or transfer reset, respectively.
0x03	Routing	one bit toggle and four bit selection of direction to send data, otherwise dynamic.
0x04	Channel Mask	16 bit mask selection of triggers from input pixels.
0x05	Position	8 Bit selection of data to determine ASIC position within tile.
0x06	Disable	Four bit selection of which neighbor node inputs are ignored.
0x07	Local Disable	Single bit selection to stop collecting data when sending.

Table 4.2: The address values are not sequential because some registers have become deprecated through development. The command register controls for resets and triggers (interrogations) for data. The Routing controls either dynamic or manual routing.

These registers are described within QpixRegFile module, shown in Figure 4.3. These registers include the ability to control routing of data packets, reset, enable, and channel masking. The Table 4.2 describes the implemented register addresses and their functions:

The composition of any register word is shown in Table 4.3. Each of the registers in Table 4.2 are accessed by setting the correct address value in the register request packet.

The two essential registers for connecting to and reading from the ASIC are the Routing (0x03) and Command (0x01) registers. The routing register allows the ASIC to be configured in either a manual or a dynamic routing. The dynamic routing state allows an ASIC to send its data in the direction it receives a broadcast (Section 4.1) from, whereas a manual routing allows the aggregator to predetermine the path of the data words. The Command register controls both ASIC system resets as well as broadcast types.

Local Data Collection

The digital node is responsible for collecting and storing local timestamps in response to pixel resets as well as being able to communicate these data with neighbor nodes. The node must be able to buffer data so as to prevent packet loss during transactions. The separation of the remote and local packets are contained within two different FIFOs, as shown in Figure 4.3.

Bit Location	Name	Function
0–15	Data	Excess bits
16–31	Address	Excess bits
40–43	Y Position Transfers	Next Y position in tile.
44–47	X Position Transfers	Next X position in tile.
48	Source Flag	Single Bit flag to indicate whether or not packet originated from aggregator.
49–52	Request ID	Identifier bits to specify broadcast.
53	Destination Flag	Identifier bit to specify if broadcast is meant for a specific node.
54	Read Flag	Identifier flag to specify if register request is a read.
55	Write Flag	Identifier flag to specify if register request is a write.

Table 4.3: Description of the bit values within the register request word.

Bit Location	Name	Function
0–31	Timestamp	Basic Datum which records the local counter at the time of the reset pulse.
32–35	Y Position	Assigned Y position in tile.
36–39	X Position	Assigned X position in tile.
40–55	Pixel Mask	Pixels which were issuing a reset at this time.
56–59	Word Header	Header value, which is common to all packets.
60–63	Reserved	Unused bits for all packets.

Table 4.4: The 64 bits (starting from zero) which make a Data word.

There are two conditions which must be met in order for a timestamp to be recorded. First, an incoming reset pulse must be supplied from one of the pixels. Second, at the time of this incoming reset the corresponding pixel mask must not be set in the channel mask register (See Table 4.2). When both conditions the value of the local reset is recorded into a 32 bit wide FIFO shown in QpixRoute in Figure 4.3.

The composition of the data word is shown in Table 4.3.

The Local Data Packet and Broadcasts

The transmission of the reset data from the local FIFO to adjacent neighbor nodes begins when an incoming register request from the aggregator is received. This request is supplied as register request to the command register (Table 4.2). This request may be considered either a “hard” or a “soft” interrogation command.

The difference between the two types of an interrogation command is whether or not the event end packet is created. In the case of a “hard”–interrogation, the event end packet is always created, regardless of the local FIFO. A Hard Interrogation happens if the first bit of the data written to the command register is high. In the case of a “soft”–interrogation, the event end packet is created only if the local FIFO is not empty. A soft interrogation happens if the second, and not the first, bit of the data written to the command register is high.

The use of two different types of interrogations allows the aggregator control flexibility in how many packets are created during an interrogation. Interrogations may happen on timescales much more quickly than expected resent pulses ($O(10^1$ s), Chapter 2). The ability to request data only if available prevents an over abundance of packets which prevents needless data transfers, reduces remote FIFO buildup, and conserves power.

The Event End Packet

The event end words perform multiple functions. First, they may used as checksums to indicate at the aggregator node, or on disk, that this node has successfully transmitted all of its data. Secondly, the event end word, since it is necessarily 64 bits long, also transmits its own timestamp with the excess bits. The timestamp that the event end word carries is the time that the node received the broadcast. This timestamp is used in the frequency calibration of the node; the method for calibration is described in greater detail in Section 4.5.

4.2 The Digital Finite State Machine

The Finite State Machine (FSM) of the digital ASIC controls the ASIC’s response to packets. Possible inputs that the ASIC can respond to are timestamps from pixels or communication packets from neighbor ASICs. Figure 4.7 shows a representation of the different states as well as the conditions to enter or leave each state. The two conditions to leave the default (IDLE) state of the ASIC happen when either its remote FIFO is not empty, or it receives a system interrogation (register request packet).

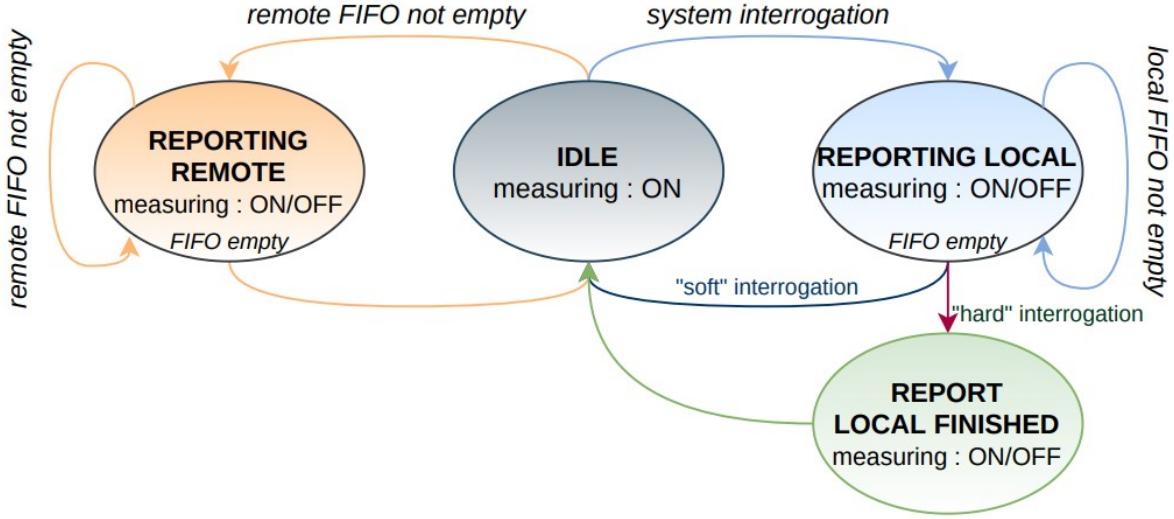


Figure 4.7: Diagram of the Digital node’s FSM which determines how to respond to incoming packets. This FSM is defined within the QpixRoute section in Figure 4.3. The Route FSM determines how and when packets are sent from the ASIC.

- Idle - Normal ASIC operation.
- Transmit Local - Requires soft or Hard Integration from aggregator.
- Transmit Finish - Requires Hard Integration or soft integration with available timestamp data.
- Transmit Remote - Entered whenever packet received from neighbor that isn’t a broadcast.

One of the contributions of this work is to demonstrate how an ASIC that sends data only on the states described in Figure 4.7 can be used in a large scale LArTPC. The scale of a DUNE-FD LArTPC requires millions of pixels to run for nearly a decade and requires precision measurements. To meet these goals, the Q-Pix readout is designed to avoid all potential places of SPF. One, always unforeseeable, place of failure is correct, but not intended behavior of an ASIC. To avoid this, we limit, as much as possible, the possible behaviors of the ASIC.

In the next section we discuss the design challenges this ASIC must overcome.

4.3 The Digital Back-end problem

The main objectives of the digital back-end are to correctly measure the data presented to it by the analog front-end and ensure lossless transport of that data to disk. More simply, the goals of the digital portion of the Q-Pix readout are to record and send data. We note that the successful completion of these two objectives to be goal of these simulation studies.

Previous sections (sections 4.1 and 4.2) described the design of the current Q-Pix digital ASIC. This section presents and defends the motivation for this design.

The Basic Datum

We begin with a discussion of the basic datum and mention initial design choices at the physical connection interface. The structure of this datum determines the buffer widths and depths required to store the data at the local ASIC level as well as the protocol used to transfer this data between ASICs and eventually out of the detector.

The minimum data which the timestamp, the relative location of the ASIC, plus the status of all channels during the timestamp. Each these factors require bits which must be recorded.

We choose the number of bits for the timestamp (N_T) to be 32, which prevents frequency wrap-around based on a fast clock frequency. We choose as the number of bits to assign a location (N_{loc}) to be 8, which provides a maximum possible number of unique positions before aggregation to be 256. Next, since the number of pixels (required by analog front-end design) is 16 we choose this number as the number of bits to represent a “mask” ($N_{bits} = 16$). We need to record all of the channels during each reset since it is technically possible (even if less likely) for multiple analog channels to provide a reset within the same clock window.

We calculate the minimum number of bits per datum to be:

$$N_{bits} = N_T + N_{pix} + N_{loc} = 32 + 16 + 8 = 56 \quad (4.4)$$

Since buffer memory addresses and widths are normally characterized by powers of two, we can construct the basic datum size above the minimum number of bits provided by 4.4 to get $N_{datum} = 64$. The remaining bits are useful for constructing different types of packets to be used by the digital ASICs for additional uses such as register configuration or to provide packet identification.

Communication of the Datum

There exist several asynchronous protocols of communication of digital information. Most of the differences between protocols exist based on the number of connections between devices and

whether or not one pin is allocated to share a clock, etc. The design of the Q-Pix ASIC limits the number of connections to only two.

Our design considerations for this readout include reduction of SPF risk, low power, and minimal electrical routing. Partly for these reasons, the design choice for communication relies on only two connections between ASICs. One connection is defined as a data receiver (Rx) and the other as a data transmitter (Tx). This choice of interface dramatically limits a choice of possible protocols.

The importance of choosing a valid protocol is to ensure lossless data transmission. Since there are free running clocks, an asynchronous communication protocol is required. One way to ensure that data can be moved between clocks of different speeds is to stretch the signal or to repeat bits (Figure 4.5). The more the word is stretched in time, the larger the allowable difference in frequency between the two devices. However, this lengthening can't proceed forever, obviously, otherwise data transmission time could exceed data capture rates.

It is another important design consideration to ensure that transactions proceed as quickly as possibly without data loss. Additional concerns of long data transactions include the use of more clock cycles which use more power and increase the risk noise to leak to the analog front-end. However, these risks can be mitigated if transmission and data acquisition occur at different times. Our choice of the endeavor protocol is tested in Section 4.6.

Although Endeavor is slower than a traditional Universal Asynchronous Receive Transmitter (UART) protocol, it is stable for approximately double the frequency range: $\approx 20\%$. In Chapter 5 we show that the overall average packet transaction time is much less ($\sim 0.1\%$) of the wait time between interactions for neutrino events.

Buffer Depth Requirements

One feature of a Q-Pix readout is that the amount of memory associated with an event depends on the amount of charge deposited. The more charge that is deposited, the more resets that are produced. Each reset corresponds to a new packet to be recorded by the ASIC. Therefore, the amount of memory than an ASIC has provides a limit to how much charge (energy) it can record within a single event. The memory for each ASIC is stored in the local and remote FIFOs within the QPixRoute module shown in Figure 4.3.

The major contribution from Chapter 5 is to test the required buffer depths for high energy (~ 10 GeV) events in a DUNE-FD LArTPC. The ice40 FPGAs tested in Section 4.6 have a total of

30 Embedded Block Ram models (EBRs). This allows for a local and remote FIFO depth each of 1024 packets.

4.4 Constraining the Digital Back-end Design

Section 2.2 describes how a Q-Pix based hardware readout architecture could fit within a single DUNE-APA. Here we extend this discussion and use those constraints as the starting point for a search to a solution to the digital back-end architecture. The first problem to solve is how to aggregate the all timestamp data supplied by the large number of channels within a DUNE-FD APA.

A Q-Pix architecture will likely use either a high-performance FPGA or a custom ASIC to aggregate the large number of ($O(10^7)$) channels. The number of aggregated digital channels determines the required capabilities of the aggregator node and the selection of an FPGA or ASIC. Since each additional aggregator node represents an additional SPF risk, our design goal suggests that the optimal configuration is one that produces the least number of aggregator nodes. Therefore, the goal is to design a routing architecture which is responsible for as many digital channels as possible for each data aggregator node while still accounting for accurate timing calibration and lossless data acquisition.

In a fully realized design an aggregator might in fact be responsible for multiple tiles, which need not necessarily be the same size. The requirements of an aggregator node require that it be capable of sending packets faster than it can receive it. If an aggregator node connects to one ASIC per tile, the average incoming data rate is the number of tiles times the average packet transaction in Equation 4.3.

The Q-Pix ASIC data rates (8 bytes per $\sim 60 \mu\text{s} = \sim 117 \text{ kB}$) are incredibly slow compared to the ethernet protocol of the aggregator presented in Section 4.6. If a Q-Pix ASIC sent data at a rate of 117 kB/s, and the aggregator sent data via 5 GBs ethernet, a single aggregator could connect to over 40000 tiles without data loss. For comparison, the dimensions of the DUNE-FD APA in Chapter 5 use 862,500 pixels, which would take only 3370 16 \times 16 tiles.

However, as one increases the number of digital channels per aggregator node one also increases the amount of local oscillators per aggregator, each of which must be calibrated (Section 4.5). Additionally, since each digital channel requires extra communication time (as discussed in Section 4.3) the introduction of more channels negatively affects the precision of timing calibrations

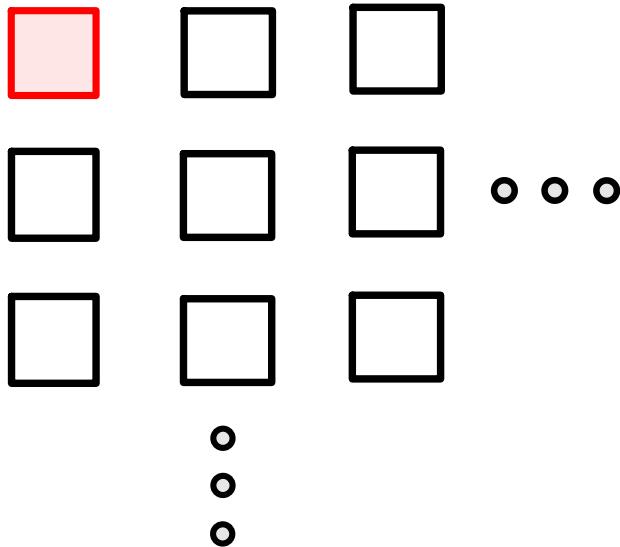


Figure 4.8: Example of an Corner Base-Node configuration. The base-node is colored and highlighted in red. The base-node (ASIC) is the special node which is the only ASIC that connects to the aggregator. All data paths, regardless of routing must pass through this node.

and potentially increases SPF risk of digital channels. We consider then that an optimal number of digital channels per aggregator node is one that maximizes the number of digital channels but still maintains the required timing calibration and transmits lossless data.

Tile Routing Considerations

A tile is a rectangular array of digital ASICs which must provide a path for data from all ASICs to the aggregator. There is one special node within the tile that connects to the aggregator. This special node we refer to as the “base-node” as all data and instruction commands, regardless of routing, must pass through this node. The symmetry of the rectangular tile allows any corner node to be the base node, and we choose the upper-left to define a convention. An example of a tile with a corner base-node is shown in Figure 4.8.

The most robust protection a tile can have is to be fully connected, which allows the maximum number of unique paths from the base node to any other node. Each path (Tx or Rx connection) is as an edge between nodes.

Here we introduce a particular representation for a tile which is useful for simplifying simulations

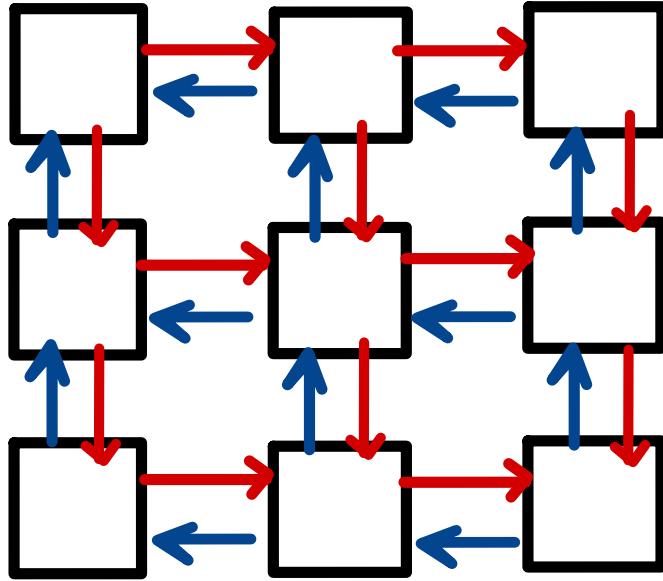


Figure 4.9: Example of the fully connected routing configuration for a tile (FCT). Each Node represents a digital ASIC which must be aggregated, and the red and blue connections distinguish directions of communication. The red connection lines indicate pathways away from the base node, whereas the blue lines represent connection paths towards the base-node in the upper-left. The FCT can be viewed as a directional, weighted graph where the edges are the Tx and Rx connections between ASICs (nodes).

and for analyzing particular routing configurations. The most general tile configuration occurs when we assume that all adjacent nodes within the tile are connected; this creates what we refer to as a “fully connected tile” (FCT). An example of a FCT is shown in Figure 4.9. Any particular choice of an effective routing must then be a subset of this fully connected version.

To elaborate on the adjacency matrix of the FCT we consider an 2×3 tile. A 2×3 tile has six total nodes, where we consider the upper-left most node to be the base node. Then, the unweighted

adjacency matrix has dimensions 6×6 of the form:

$$M = \begin{pmatrix} 0 & 1 & 0 & 1 & 0 & 0 \\ 1 & 0 & 1 & 0 & 1 & 0 \\ 0 & 1 & 0 & 0 & 0 & 1 \\ 1 & 0 & 0 & 0 & 1 & 0 \\ 0 & 1 & 0 & 1 & 0 & 1 \\ 0 & 0 & 1 & 0 & 1 & 0 \end{pmatrix} \quad (4.5)$$

Where each non-zero value of M_{ij} represents a connection between nodes i and j . As an unweighted, undirected graph this is a symmetric matrix.

In practice each digital channel within a tile is actually controlled by a unique, free-running oscillator. Therefore, we can define the length of each edge between nodes as the length of time to send of a packet of data between two nodes ($T_{i \rightarrow j}$). With this we can extend the model the adjacency matrix to a weighted and directed graph if we recognize that the non-zero elements of M_{ij} become $T_{i \rightarrow j}$, or the length of time it takes for the i^{th} local oscillator to transmit a packet to node j .

We can generalize this matrix in terms of an arbitrary number of rows (r) and columns (c). We define a convention of numbering nodes within the tile in terms of increasing column number followed by increasing row number. With this convention we obtain the general adjacency matrix with values defined by:

$$M_{ij} = T_{i \rightarrow j}(\delta_{i,j=i \pm 1} + \delta_{i,j=i \pm r}) \quad (4.6)$$

An adjacency list can similarly be constructed from Equation 4.6 where the non-zero connections are given by the Kronecker deltas factors.

The length between the nodes represents the time it takes for a packet to transact from one node to the next. This is determined by both the number of clocks to be sent in the communication protocol (N_{bits}) and the period of the transmitting and receiving oscillators, T_i and T_j , respectively. Unlike the transmitter, the receiver only affects the transaction time with a single clock cycle, as the protocols we test here, (UART and Endeavor), each conclude a packet transaction when the receiver records the last bit transaction from the transmitter.

The full length between two nodes, i and j , connected by an edge is represented by:

$$T_{i \rightarrow j} = N_{bits}T_i + T_j(t) \quad (4.7)$$

where $T_j(t)$ represents the time dependent fractional part of one nominal clock period of the receiving node. The expectation value of $T_j(t)$ is half of the nominal window so that mean Equation 4.7 is:

$$\bar{T}_{i \rightarrow j} \simeq N_{bits} T_i + \frac{T_j}{2} \quad (4.8)$$

Since the transaction time of a packet is much larger than a single clock cycle ($N_{bits} \simeq O(10^2) \gg \frac{1}{2}$), we can approximate Equation 4.8:

$$\bar{T}_{i \rightarrow j} \approx N_{bits} T_i \quad (4.9)$$

This representation is also useful to model certain SPF where a node becomes inactive. Dead or inactive nodes are ones in which all of their connections are effectively disconnected. This is equivalent to setting their transaction lengths to zero: $T_{SPF} = 0$.

We comment that although it is possible to construct tiles where more than one node connects to the aggregator, we observe that this configuration simply produces two (or more) effective tiles. These distinct tiles then are the data paths which are unique to each base-node. In this graphical representation a packet of data can follow one, and only one path from the origin node to the base-node unless there was duplication of packets. We emphatically avoid designs which might depend on data duplication for redundancy; situations with multiple base nodes produce multiple unconnected graphs.

The SPF Cost

We define the average SPF cost as the amount of nodes that will be lost during a transaction as the number of digital channels at a height below the failed digital channel. For example, the number of nodes which are lost if a leaf-node fails is one since no other channels are between it and the data node. Likewise, the number of nodes which are lost in the event of a base-node failure is the total tile, N .

We can then calculate a mean cost SPF, C_{SPF} , :

$$C_{SPF} = \frac{1}{N} \sum_{node} \frac{n_i}{N} = \frac{1}{N^2} \sum_{node} n_i \quad (4.10)$$

Minimize Occupancy

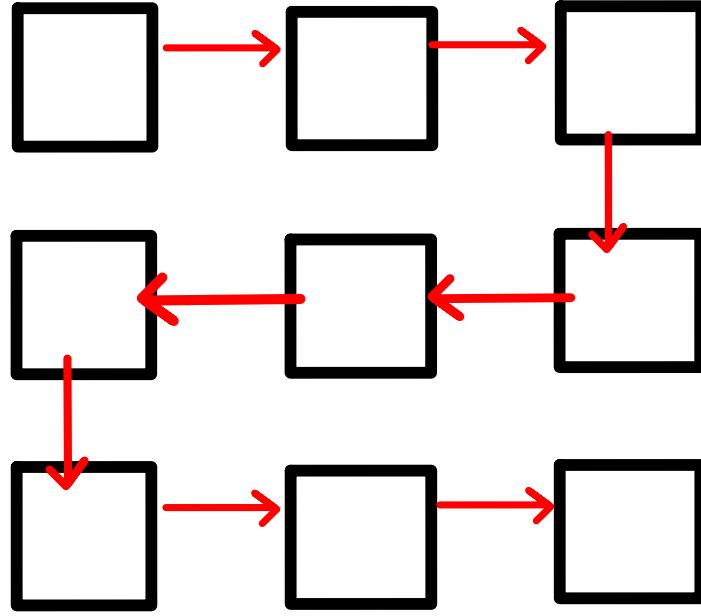


Figure 4.10: Minimal Occupancy Path of a FCT, or "Snake" routing. This routing path ensures that the number of input connections equal the number of output paths for the node.

One of the goals of a successful digital design is to ensure lossless data transfer. One point of failure on the digital side is an overabundance of data arriving at a single layer within the tree. This data loss occurs when data are sent to a node faster than the data leaves the node, and persists for long enough such that the buffers of the node overflow. This creates a horrible loss of data which can't be recovered.

A routing scheme which minimizes the overall occupancy in the tree depths is shown in Figure 4.10. We refer to the style of routing as “Snake”-routing, because this is also the longest possible routing scheme for a square tile.

We inspect the SPF risk from this routing scheme with Equation 4.10, where we notice that the n_i of each node is simply a running sum from the leaf to N at the base node.

$$C_{SPF} = \frac{1}{N^2} \frac{N(N+1)}{2} = \frac{1}{n} \frac{N+1}{2} = \frac{1}{2} + \frac{1}{2N} \quad (4.11)$$

Equation 4.11 tells us that the SPF risk of this routing configuration converges to half as the size

of the tile grows. Intuitively, this makes sense, since it is equally likely to select a node close to the base-node as it is far away, which implies that the sum should converge to half the tile size for large N .

Although this routing scheme provides the most lax constraint on the required buffers at each digital channel, it provides the longest average path between the base node. The longer the transaction delay between the base-node and other nodes increases the reconstruction time uncertainty. Therefore, a natural alternative routing scheme is one that minimizes the communication scheme.

Minimize Delay

For any given node in an edge FCT with location (R_i, C_i) , the shortest path to the base-node is simply the sum of its coordinates: $R_i + C_i$. An example of such a routing configuration for a tile is shown in Figure 4.11.

We can calculate C_{SPF} for this routing configuration if we identify that there are a C number of rows which sum from one to $R - 1$. Likewise, the far-left column in Figure 4.11 shows that the number of rows, R , sum from one to C . We can rewrite the sum over all nodes in Equation 4.10 as:

$$\sum_{node} n_i = C \sum_{i=0}^{i=R-1} i + R \sum_{i=0}^{i=C} i \quad (4.12)$$

We simplify the running sum of each term in Equation 4.12:

$$\sum_{node} n_i = C \frac{R(R - 1)}{2} + R \frac{C(C + 1)}{2} = RC(\frac{R + C}{2}) \quad (4.13)$$

Using this result we obtain C_{SPF} by identifying $N = RC$:

$$C_{SPF} = \frac{1}{N^2} \sum_{node} n_i = \boxed{\frac{R + C}{2RC}} \quad (4.14)$$

This result informs that relative cost of losing a node tends to zero as the size of the tile grows. Again, this result can be obtained intuitively, since as the number of columns (or rows) grow in size, the probability of a single failure occurring on the aggregator column is increasingly less likely.

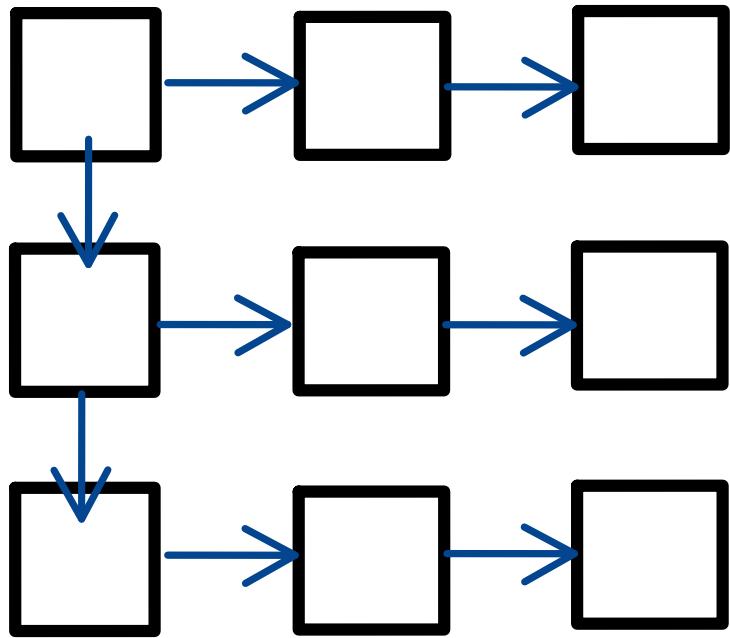


Figure 4.11: Minimal Delay Path of a FCT, or "Left" routing. This routing path ensures that the minimum number of transactions occur from every node in the FCT to reach the base-node. For any node along any column this is equivalent to the sum of the row and column of that node.

Broadcasts to avoid SPF

In order to protect against SPF we only consider designs which implement the FCT. A FCT allows searches to probe all possible paths to any node via a “broadcast” produced from packets sent by the aggregator to the base-node. Therefore the broadcast algorithm can be represented by a complete circuit which begins at the base-node and proceeds to a target node with no repeated nodes until the target node is reached. The backward path is then completed in reverse by following the edges (Tx and Rx connections) between each node until arriving finally again at the base-node.

In practice, broadcasts are encoded as a register request (Table 4.2) created at the aggregator node where Bit 53 (4.6) is set to '1'. To differentiate between broadcasts an identification number is also included in the packet. Then, any node when receives a broadcast packet will record the identification number of the most recent broadcast, and send this packet to its connected neighbors in the direction it did not receive the broadcast. The node uses the identification number to discard

repeated broadcast packets.

In the event that a particular node becomes inactive it will “block” data coming from the nodes along its path. In this case, there must be some sort of “broadcast” originating from the base-node that would allow information transverse regardless of the effective routing path.

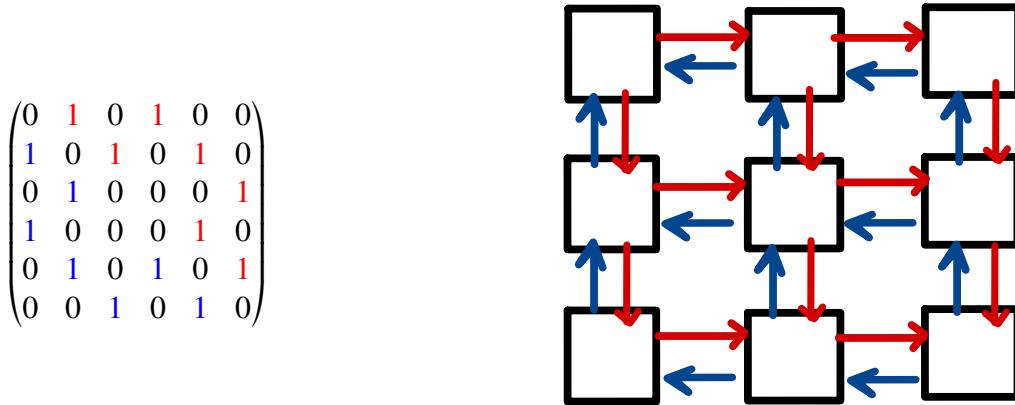


Figure 4.12: Minimal Routing Path of a FCT. This routing path ensures that the number of input connections equal the number of output paths for the node. The matrix image highlights the appropriate indices which correspond to the 2×3 subset of the tile (right). The matrix represents transactions that proceed towards (red) and away from (blue) the base node.

Comments on the Edge Base-node and Other Routings

We discuss here the case of a FCT with an edge base node. An edge base node (EBN) is a node which connects to the aggregator and to three other digital channels within a tile. An example of an EBN is shown in Figure 4.13. Like before, this base-node must provide a unique path during data transmission to all digital channels within the tile. In this configuration the adjacency matrix is still the same as given in Equation 4.6.

4.5 Frequency Calibration of Local Oscillators

The Q-Pix calibration requirements are described in detail in Section 2.1. The important parameters which must be calibrated for each pixel are the charge per reset and the frequency of the local oscillator. An aim of this work is to demonstrate an additional frequency calibration method using the minimal required connections between each digital node.

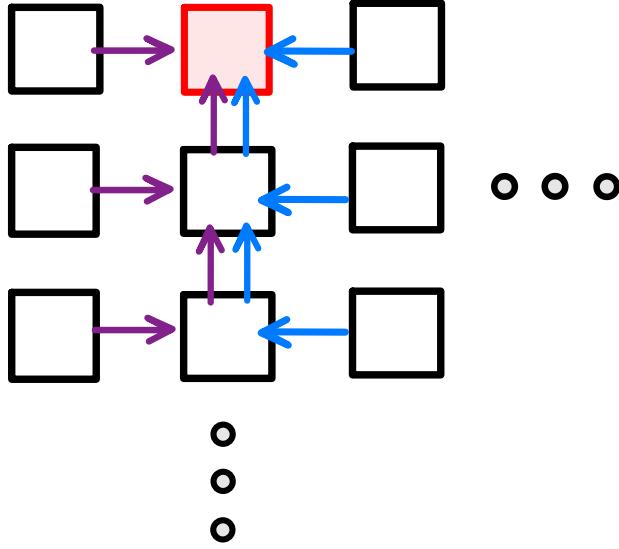


Figure 4.13: Example of an Edge base-node configuration. The base-node is colored and highlighted in red. Image shows how the EBN can be thought of as a super-position of two corner base-nodes, represented by the purple (left "tile") and blue (right "tile") connections. Instead of a 3×3 tile, there are two 2×3 "tiles".

Any method of a frequency calibration must synchronize time measurements between all digital nodes within a tile and the aggregator. There are several possible methods to achieve this, but ultimately the data that are recorded must be some time at the aggregator, T_a , and the time at any specific node, T_j .

A direct method is one where the aggregator distributes its own clock to all nodes in the tile. This scenario removes the need for a calculation of the frequency of each node altogether since the clock of each node is already known from the aggregator. This is the simplest case for timing calibration: remove all free running oscillators.

A distributed clock network indeed removes ambiguity of the remote oscillator frequencies, but at the cost of hardware complexity. Whether or not this design choice is preferred is entirely detector dependent, but likely increases in difficulty with the scale of the TPC.

We comment, however, that we ignore this scenario because it may altogether be unnecessary depending on future ASIC performance. In the event that frequency calibrations of sufficient precision ($\bar{f} \approx 1\text{ ppm}$) are possible occur on free-running local oscillators future detectors would need only to acquire these ASICs and place them with minimal cost in terms of both time and

money.

Another simple scenario is one where the aggregator itself connects directly to all nodes within a tile via a single connection which can be used as a reference trigger. This means that some trigger from the aggregator would issue directly into each node at the same time: $T_a = T_n$. To calculate the frequency in this manner, the controller would issue two triggers from the aggregator with a known time separation, $T_o = T_{a2} - T_{a1}$. The remote nodes would each record and send their timestamps back to the aggregator, where the time difference would be calculated as:

$$T_o = T_{a2} - T_{a1} = T_{n2} - T_{n1} \quad (4.15)$$

this is rewritten in terms of frequency as follows:

$$f_n = \frac{T_{n2} - T_{n1}}{T_o} \quad (4.16)$$

This calibration method, though extremely simple, introduces an additional connection to each ASIC between itself and the aggregator. For a large scale system such as Q-Pix a single connection per ASIC introduces $\approx 60 \times 10^3$ hardware points of failure per APA.

Both of these scenarios are valid implementations of a Q-Pix readout system. In both of these scenarios, however, there is added complexity into the hardware design of the system in the form of additional routing where each route which represents a possible point of failure.

In a world of perfect hardware and costless routing in terms of both time and money these routing schemes would clearly be sufficient. However, no hardware is perfect. Therefore we introduce and discuss a calibration technique which relies on no additional routing and could be optionally implemented even in the above schemes in the event of a failure. Therefore, even if not the primary implemented calibration technique, since this calibration introduces no superfluous routing it could still be used regardless of the actual future hardware implementation.

A Minimal Connection Calibration Procedure

As stated previously, any frequency calibration records a reference time at the aggregator (T_a) and an event time (T_n) at a ASIC within a tile. The time calibration procedure presented here requires only the minimal routing required in any Q-Pix readout system, where we assume time-dependent free-running local oscillators at each ASIC within the tile.

The calibration procedure begins at a time (T_0) where the aggregator sends a calibration packet. Next, the packet propagates through the tile to some remote ASIC, N_j . This ASIC receives the packet later at some time T_{n1} :

$$T_{n1} = T_o + T_{f1} \quad (4.17)$$

Where T_{f1} is the propagation time of the packet from the aggregator to the N_j ASIC. This remote ASIC then sends the packet with its time (T_{n1}) back to the aggregator. The aggregator will wait some calibration time (T_{cal}) before issuing another calibration packet. This wait period ($\mathcal{O}(10^{0-2})$) can be long compared to the full transaction time to the N_j ASIC ($\mathcal{O}(j * 10^{-5})$).

After the wait period, the aggregator will issue a second calibration packet to be sent to a remote ASIC at time:

$$T_1 = T_{cal} + T_0 \quad (4.18)$$

Similarly to the first packet this packet will propagate to N_j with some new time T_{f2} where N_j will record time T_{n2} :

$$T_{n2} = T_1 + T_{f2} \quad (4.19)$$

Now, we define ΔT_j as the difference in the two time measurements from the two packets sent from the aggregator. The time difference is related to the number of clocks that occurred between the two different measured values of the clock, T_{n1} and T_{n2} .

$$\Delta T_j = T_{n2} - T_{n1} \quad (4.20)$$

We use the known relationships for T_{n2} and T_{n1} to obtain:

$$\Delta T_j = (T_1 + T_{f2}) - (T_o + T_{f1}) = (T_1 - T_0) + (T_{f2} - T_{f1}) = T_{cal} + \Delta T_f \quad (4.21)$$

Where we defined ΔT_f as the difference in forward propagation times from the packets sent from the aggregator at T_1 and T_0 .

We arrive at the result which compares the measured time at the aggregator T_{cal} and the time measured at each ASIC, ΔT_j :

$$\Delta T_j = T_{cal} + \Delta T_f \quad (4.22)$$

A perfect reconstruction of the nodal frequency would follow if $\Delta T_f = 0$. But it is sufficient to note that the wait period happens on the order of seconds, whereas ΔT_f is on the order of μs or at least a six order of magnitude difference. We then use $\Delta T_f \ll T_{cal}$ to obtain:

$$\Delta T_j \approx T_{cal} \quad (4.23)$$

We convert time into frequency with the difference of the timestamps measured and a known aggregator frequency (f_a):

$$\frac{\Delta N_j}{f_j} = \frac{\Delta N_a}{f_a} \quad (4.24)$$

or,

$$f_j \simeq \frac{\Delta N_j}{\Delta N_a} f_a \quad (4.25)$$

Where ΔN_j and ΔN_a are the differences in the timestamps of the 32-bit clocks at the remote node and aggregator, respectively.

Packet Transaction Time

We next examine the approximation that $\Delta T_f \ll T_{cal}$ and consider its contribution to the error in the reconstruction of T_j in Equation 4.25. This analysis also provides a constraint on the duration of T_{cal} (Equation 4.18) to ensure an accurate measurement of each T_j in a tile. We begin by discussing how long it takes for a packet to traverse a tile.

The time it takes for each packet to be received by the next node is given in Equation 4.9. The value, N_{bit} , is the number of clock cycles used for the packet and is protocol-dependent. Since the protocol is deterministic (Section 4.1) for each packet, N_{bits} is the same for each transaction on the path from the base-node to the remote node. As an example, the time it takes for a packet to go from the base-node, N_1 , to a remote node, N_3 , via the path $1 \rightarrow 2 \rightarrow 3$ is determined by:

$$T_{1 \rightarrow 3} = T_{1 \rightarrow 2} + T_{2 \rightarrow 3} \approx \frac{N_{bits}}{f_1} + \frac{N_{bits}}{f_2} = N_{bits} \left(\frac{1}{f_1} + \frac{1}{f_2} \right) \quad (4.26)$$

Where, f_i , is the frequency of the clock at sending node. The approximation is within a single clock cycle of the receiving digital node (≈ 33 ns). Therefore the time it takes for a packet to go from the base-node to any remote node is proportional to N_{bits} multiplied by the sum of the edges in the full adjacency matrix given by Equation 4.6.

We generalize Equation 4.26 to represent the time it takes a packet to go from the aggregator ($i = 0$) to any remote node, N_j :

$$T_f = T_{0 \rightarrow j} = N_{bits} \sum_{i=0}^{i=j-1} \frac{1}{f_i} \quad (4.27)$$

We require that every calibration packet on the protocol uses the same number of clocks (N_{bits} is the same for each identical Register Request, Section 4.1). ΔT_f becomes:

$$\Delta T_f = N_{bits} \sum_{i=0}^{i=j-1} \frac{1}{\Delta f_i} = N_{bits} \sum_{i=0}^{i=j-1} \Delta T_i \quad (4.28)$$

We recognize ΔT_i as the nominal time-dependent clock drift of the each local oscillator in the path between the base-node to the remote-node. We can provide an order of magnitude estimate for ΔT_f if we assume a (poor) $\approx 5\%$ drift in each of the remote clocks within the tile during a period of $T_{cal} \approx 1$ s. In this approximation we also assume that the mean of the periods of the nodes are the designed value (≈ 33 ns) for which a 5% error gives $\sigma_{T_f} \approx 15$ ps. If we further assume that all of the clocks drift have error which drifts in the same direction (the mean drift doesn't cancel) then for 31 (16×16 tile broadcast) transactions with 2000 clocks per transaction (Equation 4.3), we obtain for ΔT_f :

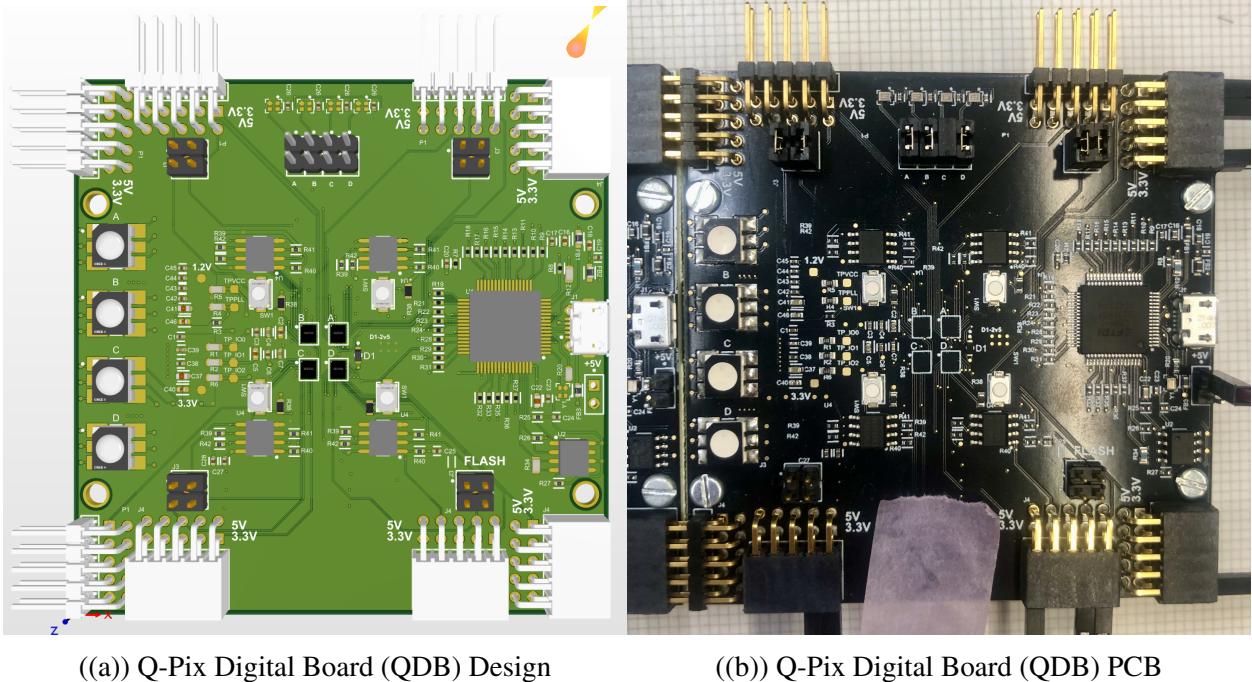
$$\Delta T_f \approx 2000 * 31 * 15 \times 10^{-12} \approx 0.92 \mu\text{s} \quad (4.29)$$

Equation 4.29 provides an estimation of the timing uncertainty introduced by the calibration scheme in a worst case 16×16 tile scenario. In the next section we introduce a prototype modular prototype board which was designed to test the stability of the communication protocol and the frequency calibration procedure presented here.

4.6 The Q-Pix Digital Board

We describe the design of a modular digital back-end prototype board and discuss first results of the Q-Pix digital logic in an Field Programmable Gate Array (FPGA). The results presented here constructed a tile 4×4 array of Lattice iCE40UP5K-UWG30ITR FPGAs. These FPGAs were chosen because of their small form factor, availability and pin out. Each FPGA is programmed with the logic described in the previous sections based on the Q-Pix digital ASIC prototype.

The FPGAs are used to test the control logic, communication stability, buffer requirements, and calibration procedure which will be tested in the future Q-Pix digital prototype ASIC. The most



((a)) Q-Pix Digital Board (QDB) Design

((b)) Q-Pix Digital Board (QDB) PCB

Figure 4.14

important quantity to be calibrated for the digital nodes is the frequency of the local oscillator. The Q-Pix reconstruction for both time and z position are dependent on this parameter (see Chapter 2).

An example block diagram of the prototype board (QDB) is shown in Figure 4.14. Each PCB connects 4 FPGAs in a 2×2 array. In the diagram shown, FPGA-A can connect to FPGA-B and FPGA-D, but not FPGA-C. The external right angle bracket connectors are used to interconnect multiple tiles for a modular design.

Future implementations of the digital back-end for Q-Pix may, of course, use different oscillators. However, these results are still beneficial as a proof of concept for the frequency calibration, as well as tests to the packet loss susceptibility. Packet loss is a function of relative frequency drift between neighbor nodes.

Each iCE40 FPGA is uses an 12 MHz external oscillator [81], which is then connected to a phase-locked loop (PLL). The PLL uses a multiply by five and divide by three circuit to achieve the desired 30 MHz average frequency. The PLL is a special IP for the ice40UP5k FPGA's [82].

FPGA's are labeled A through D on each QDB, beginning in the "top-right" of the board and proceeding counter-clock wise, as shown in Figure 4.14. Each FPGA has access to two right-angle connectors, which allow the QDBs to be inter-connected into a larger tile as shown in Figure 4.15.

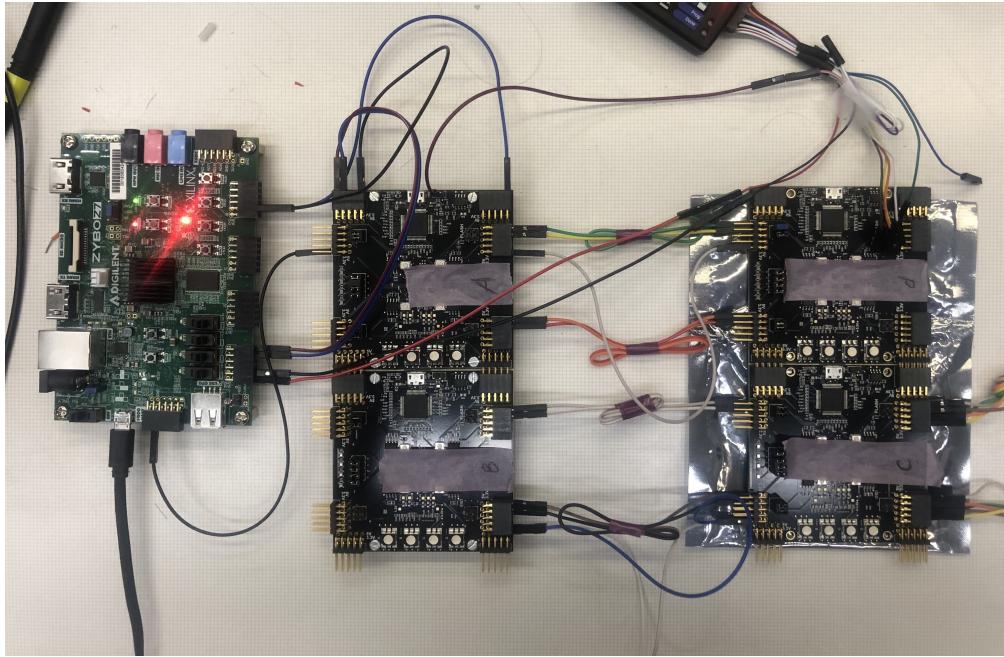


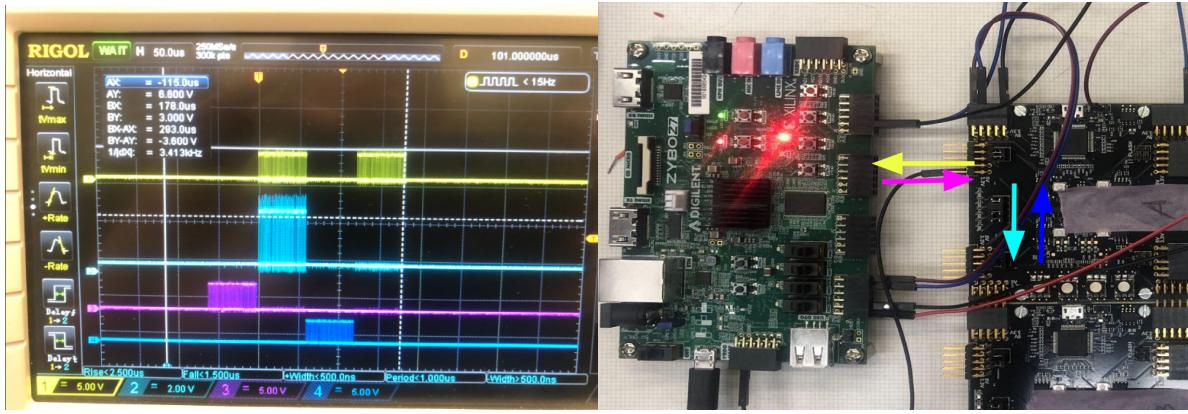
Figure 4.15: Layout of a Zybo-Z7 aggregator node connected to a single FPGA in an interconnected 2×2 QDB Tile. The total amount of interconnected FPGAs for the tile size is 4×4 . The FPGA that connects to the Zybo is FPGA-A as shown in Figure 4.14 on Board-A. Not shown is the ethernet connection from the Zybo back to the controlling PC. Some QDB boards are connected via jumper wires to allow easier programming of the FPGAs and for probing pins.

The numerical location (x,y) of each FPGA corresponds to number of transactions "left" or "right" (x), and "up" or "down" (y) from the aggregator as viewing in Figure 4.14.

We use the Zybo-Z7 prototype board from digilent as the aggregator node. Communication to and from the board uses a custom software interface that allows data communication between the Zybo and a PC. This DAQ is nearly identical to the procedure used in the SAQ experiment in Chapter 3.

One of the main objectives of the prototype boards is to verify the communication protocol (Section 4.3). An example of a broadcast transaction between the Zybo and two FPGAs on a single QDB is shown in Figure 4.16. The transaction depicted is a broadcast register write, written to the command register (Table 4.2). From left to right in image A, the packets follow this pattern: The Zybo constructs a packet based on the protocol read from the

1. Zybo Sends Broadcast Register Write (Hard Interrogation)
2. FPGA-A Forwards and responds to broadcast and responds



((a)) Example of a Hard interrogation.

((b)) Communication Route on Prototype

Figure 4.16: Timescale is $50 \mu\text{s}$. An example of a Hard Interrogation with two connected FPGAs is shown. The first incoming packet is the broadcast (Register Write to command register) from the Zybo board. The FPGA (0,0) responds and sends the broadcast. The bottom waveform is FPGA (1,0) responding to the request sent from (0,0). The right image shows the direction of the packets as viewed on the QDB tile.

3. FPGA-B Responds to broadcast
4. FPGA-A routes the remote packet to the Zybo

4.7 Prototype Frequency Calibration Results

We describe here the methods of measuring a stable oscillator frequency for the prototype PCB based on the frequency calibration scheme developed in Section 4.5.

The interrogation procedure involves using a Hard Interrogation on the FPGA to ensure that each FPGA responds with an Event End packet (packets defined in Section 4.1). The Zybo records the time that it sends the interrogation time and collects 16 response packets from each FPGA. We test the effects of the calibration rate (T_{cal} in Equation 4.18) by performing two sets of interrogation rates at 0.1 Hz and 4 Hz, which we refer to as the "slow" and "fast" interrogation rates. The slow (0.1 Hz) frequency test is the expected lower limit of reset data to be acquired from radiogenic and noise contributions alone (Section 5.4). The fast (4 Hz) test allows only 250 ms for a tile readout and is much faster than any interrogation requirement for use in a DUNE-FD APA ($\simeq 1 \text{ unitHz}$ for beam spills).

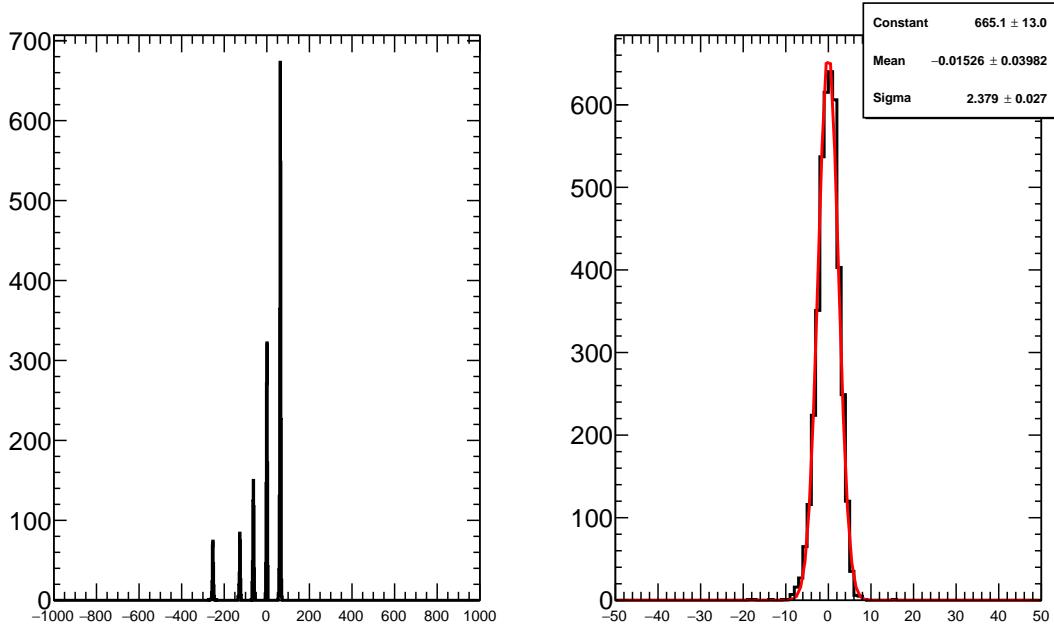


Figure 4.17: Example of frequency calibrations for the FPGA Adjacent to the Zybo, $T_{cal} = 250$ ms. Shown is the reconstructed frequency for the base node FPGA at (0,0) within the QDB tile. Figure 4.19 shows the corresponding reconstructed frequency pattern that represents the five individual peaks on the left. A mean subtraction is performed on all five histograms to produce the right image, where a Gaussian fit is performed to estimate a frequency uncertainty (σ).

Figures 4.17 and 4.18 show that there are five distinct frequency groupings for the reconstruction. These separate distribution of frequencies clearly correspond to the interrogation number of the Zybo as shown in Figure 4.19. The reason for the estimated drift is due to the difference of drift in the Zybo clock. The reconstruction formula (Equation 4.25) on the frequency of the aggregator (f_a). Therefore the uniform drift seen on all FPGAs can be attributed to the drift on the aggregator.

We remove this drift for each of the distributions by fitting a Gaussian to each of the distributions seen in Figure 4.18. Five Gaussian are fit to correspond to the five clusters, where the mean of the this fit are subtracted from the reconstructed points closed to this mean. These news points form average frequency as shown in the right of Figures 4.18 and 4.17. A final Gaussian is fit where we use the σ of the fit as the estimated uncertainty (δf_j) of each FPGA. These results are shown for both the slow and fast interrogation frequencies in Tables 4.5 and 4.6.

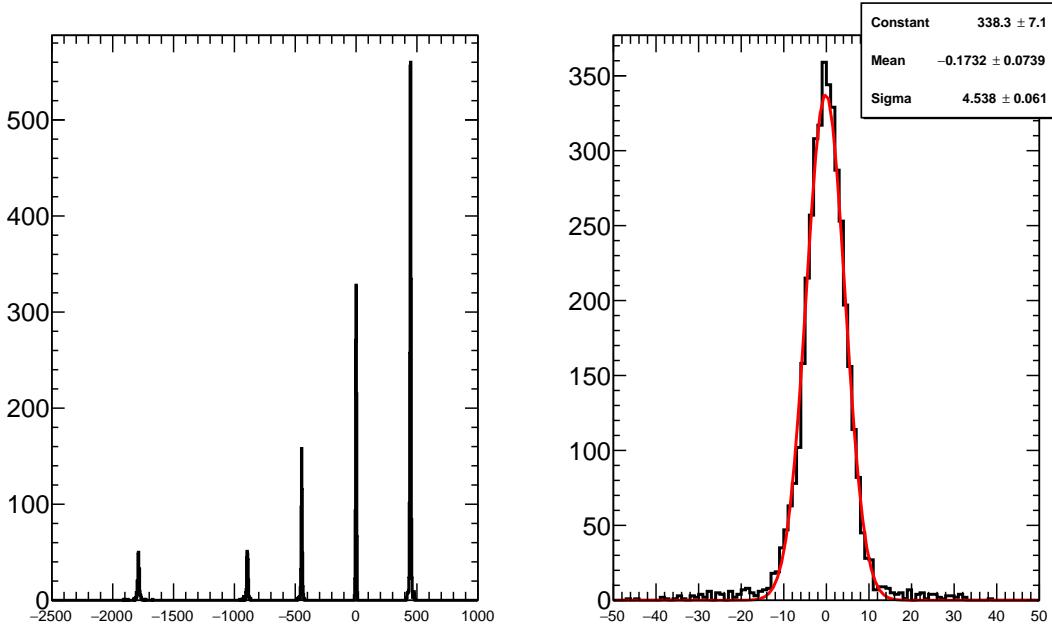


Figure 4.18: Reconstructed frequency of the FPGA at position (3,3) within the QDB tile. The relative drifts of the frequencies shown for the more distance FPGA are greater than the base node (0,0), which is only one transaction away from the aggregator.

Timing Stability and Communication Verification

To estimate the reliability of the packet communication we calculate the number of total successful transactions. During each Hard Interrogation each FPGA sends a broadcast register command plus the event end word as a response. Then, for every Hard Interrogation there are at least 32 successful packet transactions. However, the routing used during the frequency calibration was snake routing, so the average traversal of each response packet (the number of FPGAs used to send each packet), is half of the array, plus one: 9. Therefore, each interrogation required 16 correct broadcast packets plus $9 \cdot 16 = 144$ successful response packets, for a total of 160 packets. The total number of interrogations between both frequency tests was over 7000. This corresponds to at least 1,120,000 successful packet transactions.

Also, performed was a sequence of random register writes followed by read requests perform on each FPGA to the channel mask register (See Table 4.2). The channel mask register is a proxy scratch register, since it allows the reading and writing of any 16 bits. We performed a long run (\approx

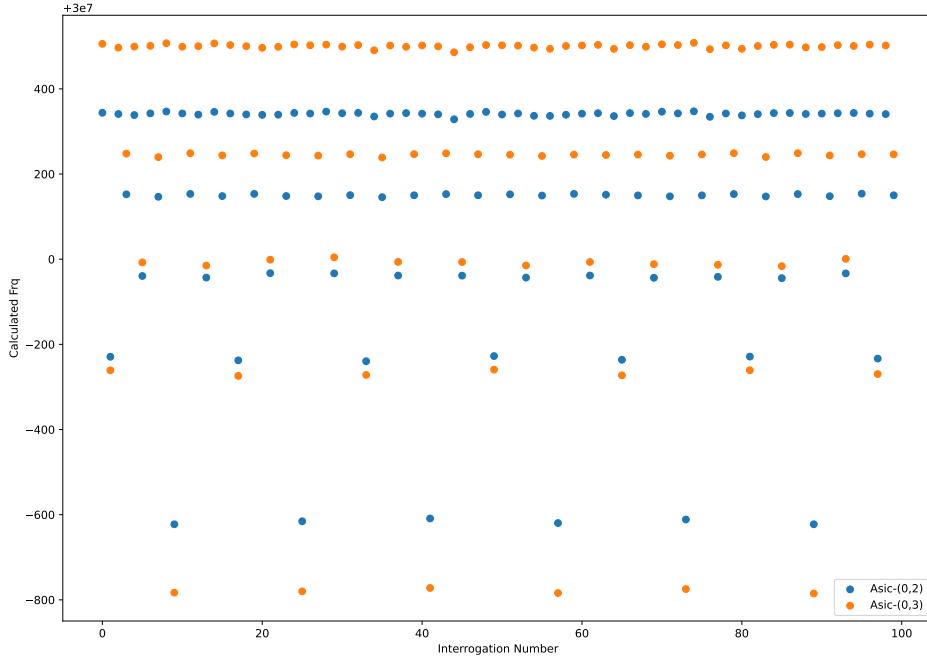


Figure 4.19: Fast calibration procedure results for two different FPGAs. Plotted are the reconstructed frequencies for increasing interrogation numbers. Each interrogation is separated by approximately 250 ms. There is a repeating pattern of five distinguishable reconstructed frequencies plotted for two different FPGAs. All 16 FPGAs follow this similar pattern, indicating that each of the reconstructed frequencies are varied by the aggregator's oscillator.

10 hours) where the Zynq would write to a random FPGA a random sequence of 16 bits, followed by a read. An error check was performed on any mismatch between the two bytes read and written. This read and write sequence occurred every 0.25 seconds, or 4 Hz, for a total of an expected 144,000 transactions. Each test, on average, writes an FPGA which is four transactions from the aggregator, and requires 8 transactions to respond. This requires 12 correct packets for each read and write, for a total of 24 correct packets per test. This readout successful tested another $\approx 24 \cdot 144,000 = 3,456,000$ packets. In total, an estimated 4,576,000 variable packets have been successfully sent without a single packet loss on the QDBs.

Figure 4.21 relates the calculated frequency stability of the QDB tile using the slow and fast calibration modes. The results show that the slow calibration mode produces a higher frequency ppm than the fast interrogation method. This indicates that the rate of the interrogation in the final

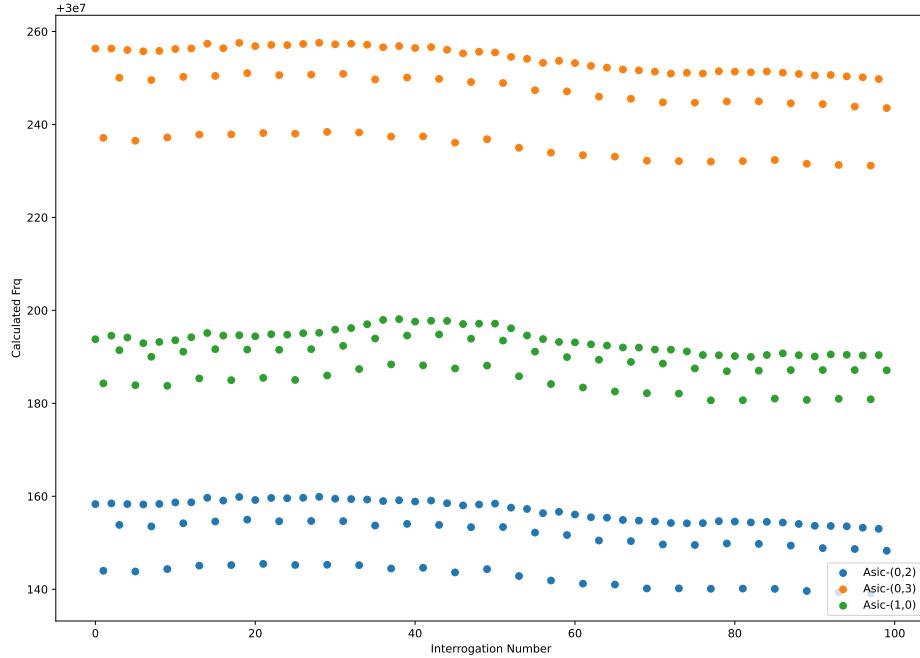


Figure 4.20: Slow calibration example ($T_{cal} = 10$ s). A similar periodic behavior is seen in the slow calibration results as compared to the fast. The drift of the three observable frequency drifts for the Zybo are clearly visible for the three FPGA frequency reconstructions shown.

system can be used to compensate for a less stable oscillator at ASICs further from the base-node. Also shown is that for both interrogation rates is that the result of the reconstruction depends on the FPGA (ASIC) location within a tile. These results (with the ASIC oscillator frequencies) indicate a limit to how large a tile can constructed. The distance from the base-node indicates the number of packet transactions that the interrogation must proceed through the tile before the Event End word is constructed. This means that fully connected tiles (FCT) will allow for largest tiles with local oscillators, since they provide the shortest path from the base-node to any remote node.

4.8 The Digital Back-End Summary

The Q-Pix digital back-end is expressed as a collection of inter-connected nodes as presented in Section 4.4. Each node represents an ASIC which connects to the front-end, which for Q-Pix is a collection of integrating CSA for each pixel in the TPC. The Q-Pix ASIC design is presented in Section 4.1, where we define its response to inputs by its FSM in Section 4.2

FPGA Position	Mean (30 MHz)	STD	$\frac{\delta f}{f_o} * 1e6$ (ppm)
(0,0)	245.543	2.379	0.079
(0,1)	190.646	2.979	0.099
(0,2)	153.908	3.334	0.111
(0,3)	248.831	3.843	0.128
(1,0)	192.729	2.860	0.095
(1,1)	210.905	3.405	0.114
(1,2)	116.212	3.984	0.133
(1,3)	159.824	4.158	0.139
(2,0)	351.431	3.685	0.123
(2,1)	193.845	4.285	0.143
(2,2)	200.278	4.071	0.136
(2,3)	152.633	4.263	0.142
(3,0)	183.359	3.954	0.132
(3,1)	209.788	4.561	0.152
(3,2)	192.277	4.169	0.139
(3,3)	171.302	4.538	0.151

Table 4.5: FPGA calibration results based on Hard Interrogations at a frequency of 4 Hz. The mean and standard deviation (STD) values are reconstructed for each ASIC within the tile as done in Figure 4.17 and 4.18. The listed STD value is the result of a Gaussian fit performed on the adjusted frequencies.

The full Q-Pix readout handles the large number of connections required in a DUNE-FD (\approx 58,000 per APA) by first collecting data via an aggregator node. The QDB prototype (described in Section 4.6) implements this first use of a Q-Pix tile and aggregator system. The use of a controllable aggregator removes the need for ASICs to dynamically self configure, and dramatically reduces the number of connections to collect all data. Each ASIC allows a configurable routing direction which is controlled by packets created at the aggregator.

The basic unit of the Q-Pix DAQ can be thought of as a tile and aggregator system, where one or more tiles are assigned to a single aggregator. Future implementations of Q-Pix can readily assign multiple tiles per aggregator. The number of tiles that an aggregator can be assigned to is dependent on its available pins as well as its maximum data output. Each aggregator will require at least two pairs of differential pins to connect to a base-node per tile, as well as provide at least 117 kB of data output either to disc or another controlling node per connected tile.

The results of the QDBs (Section 4.6) demonstrate the reliability of the communication protocol to more than 1 million packets. The calibration procedure is able to reconstruct remote FPGA

FPGA Position	Mean (30 MHz)	STD	$\frac{\delta f}{f_o} * 1e6$ (ppm)
(0,0)	243.223	3.895	0.130
(0,1)	187.225	4.631	0.154
(0,2)	151.020	6.255	0.208
(0,3)	246.553	8.229	0.274
(1,0)	188.851	4.521	0.151
(1,1)	207.837	6.468	0.216
(1,2)	111.344	7.882	0.263
(1,3)	156.660	9.985	0.333
(2,0)	348.263	6.748	0.225
(2,1)	190.976	8.622	0.287
(2,2)	196.369	9.919	0.331
(2,3)	148.284	11.844	0.395
(3,0)	179.718	8.375	0.279
(3,1)	207.859	10.655	0.355
(3,2)	188.123	11.836	0.395
(3,3)	165.011	13.725	0.457

Table 4.6: FPGA calibration results based on Hard Interrogations at a frequency of 0.1 Hz. These data are more tightly clustered together due to the longer wait time between each interrogation, and are not easily separable as done in Table 4.5. The listed mean is the simple geometric mean and standard deviation for a one hour run time.

frequencies in a Q-Pix 4×4 tile to better than 1 ppm ($\frac{\delta f_o}{f_o}$). We also find that the size of a tile is limited by the oscillator frequencies of the ASICs as well as the aggregator.

In Chapter 5 we explore simulations of the Q-Pix tile system and explore its ability to analyze radiogenic backgrounds and capture beam neutrino events.

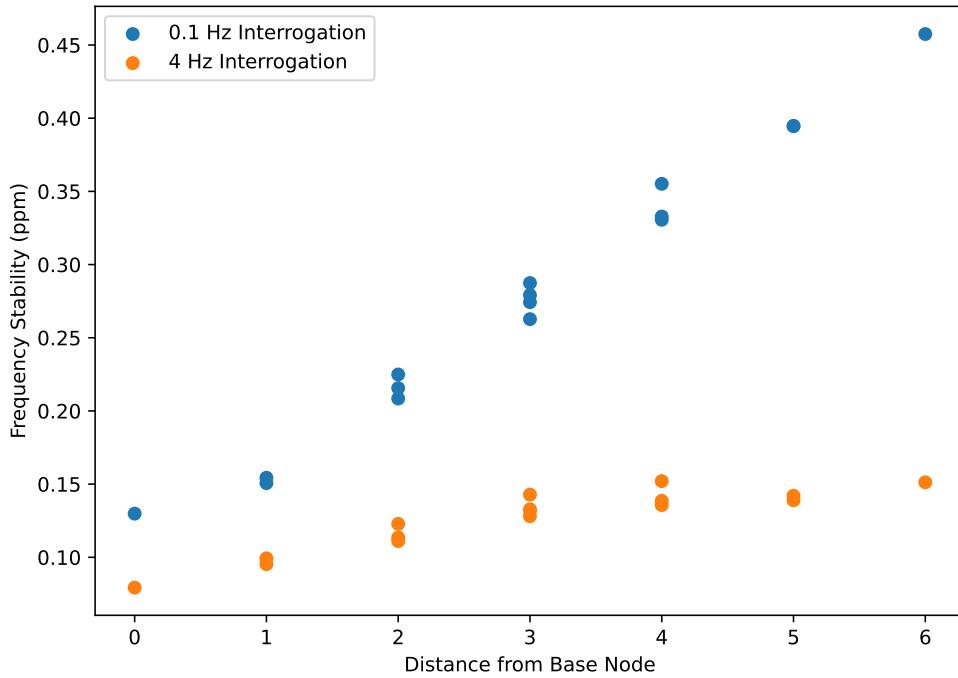


Figure 4.21: Shown are the relative values of the frequency part-per-million (ppm) values from the frequency calibration procedure in both the 4 Hz (orange) and 0.1 Hz tests. The x-axis represents the number of transactions required to reach the FPGA. These data are taken from Tables 4.5 and 4.6. Clearly indicated is the relationship between the interrogation rate: a faster interrogation leads to a sharper average time reconstruction. Also shown is that the further each FPGA is from the base-node, the worse the frequency reconstruction is. This happens since there are more average clock cycles to reach the remote ASIC (see Equation 4.29).

Chapter 5

THE Q-PIX BACK-END AND SIMULATION STUDIES FOR FUTURE Q-PIX PROTOTYPES

This chapter explores the requirements of a Q-Pix based digital back-end readout targeted at a DUNE-FD module.

The first part of this chapter describes the digital simulation used to evaluate the possible designs presented in the previous chapter. The Q-Pix readout (Chapter 2) relies on several key factors which promise possible improvements over a traditional MWPC readout: automatic calibration from quiescent radiogenic background, an overall reduction in volume of data collection, and simpler analysis chain and vertex reconstruction, to name a few. However, this novel readout technique not only changes the front-end analog structure but also dramatically increases the number of digitization channels. The increase of the number digital channels and required ASICs creates the need for a new digital back-end design.

The second part of this chapter presents results from a physical simulation framework based on radiogenic backgrounds in LArTPCs as well as high energy ($\approx 10\text{GeV}$) neutrino events. We use this physical simulation framework to address a number of design choices, since any sufficiently complicated design offers an intractable number of possible choices each of which can significantly alters the performance of a detector. A few examples of crucial design choices for the digital back-end are: the use of free-running local oscillators, the selection of an inter-ASIC communication protocol, the choice of inter-ASIC connections or routing profiles, and the buffer sizes of FIFOs to store charge-reset data. The goal of the simulation is to parameterize these design choices in order to provide an understanding of functional design targets and analysis of design tradeoffs.

The final part of this chapter synthesizes the results of the physical and digital simulations and provides a description of the effects of the most important parameters determined from these results. We use as inputs to the simulation the expected input charge from radiogenic background and beam-line neutrino interaction over a $2.3\text{m} \times 6.0\text{m}$ LArTPC. The characterization of the analog front-end, namely the charge characteristics per channel, is an on-going collaborative work whose results can be able to be applied here.

All results in this chapter are my own individual work.

5.1 The Tile Simulation Framework

The previous chapter introduced the digital back-end as well as discussed different design choices, namely tile size, routing configurations, and the effects of the aggregator position. Here we describe how we simulate events of interest for these different configurations.

A successful design is able to record and send loss less data for all events of interest. In a DUNE-FD LArTPC these sources range in intensity from sub-MeV-scale radiogenic backgrounds native to the LAr to 10's of GeV scale of beam neutrinos or atmospheric neutrinos. We consider the back-end design to be successful if and only if it provides the ability to fully capture and transmit of all collected resets from these sources.

We note that while it may be shown in the future that some resets may in fact not be needed for a reconstruction of particular events, we still assert that since Q-Pix is a novel readout, it is not yet possible to claim all scientific goals for which it may be used. For this reason we demand that no data be lost for any reason due to the digital back-end design.

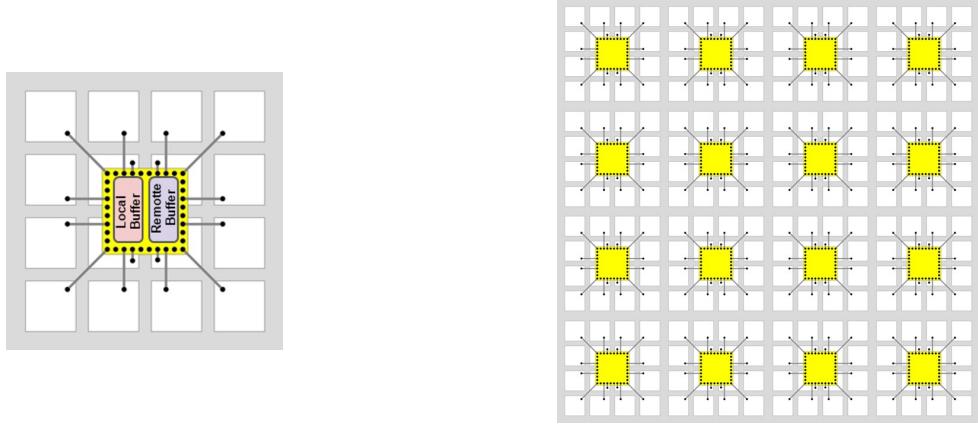
The Tile Representation

We model a tile (a group of digital nodes, or ASICs) based on the description given in Chapter 4. A tile is then represented in software (Python 3) as a linked list of nodes which store pointers to the adjacent nodes or neighbors.

We note a distinction between the nomenclature used here. The term "node" refers to the simulated back-end ASIC whereas our use of "ASIC" refers to the first digital prototype.

Every node in the tile holds two FIFO objects which store local and remote data. The local and remote FIFOs keep track of the total number of resets or packet transactions, respectively. If a node records a new reset the local FIFO is then written to, and the local FIFO transaction counter increases. Similarly, the remote FIFO's transaction count is increased when a write occurs on this FIFO, which happens every time a digital node receives a packet from a neighbor node, including the aggregator node.

In the current Q-Pix digital ASIC design (see Sect. 4.2) all packets sent between neighbor nodes, with the exception of broadcasts, are written on the remote FIFO. At the beginning of a simulation step each node first checks to see if its received an interrogation request. If the node has received a



((a)) Individual node with local and remote FIFOs.

((b)) Tile of node objects.

Figure 5.1: Composition of an example 4×4 tile. Each node in the tile represents a digital ASIC which contains two FIFOs. One FIFO is used to store timestamps from reset data, which we refer to as the local FIFO. The other FIFO we call the remote FIFO and is used to store all packet transactions from neighbor nodes. The local FIFO is 48 bits wide, where 32 bits come from the timestamp and 16 bits are from the pixels. The remote FIFO is 60 bits wide, since it must store all relevant bits for the 64 bit packet word, where there are 4 unused bits.

soft interrogation request (see Sect. 4.4), and has data in its local FIFO, it will first send its data in the local FIFO, followed by the event-end packet. If the node receives a Hard Interrogation request, the node will send local data, if any, and will send an event-end packet regardless of whether or not the local FIFO had any data. If the node's local FIFO is empty, and it has not received an interrogation, it will check the empty status of the remote FIFO. If the remote FIFO is not empty, this packet will be read and transmitted to its neighbors accordingly, otherwise the node remains in its idle state.

There are two types of remote data to send: broadcasts and responses. A broadcast is a register request sent to a digital node, which can only be created and sent from the aggregator node. The responses include all other kinds of packets sent from neighbor nodes which include: data packets, event-end packets, and register response packets.

The communication packet object is a custom struct object which uses an enumerated type to differentiate the kinds of packets that the digital node can read from its remote FIFO. Each simulated node's behavior to these incoming packets is mirrored to the digital FSM, shown in Fig. 4.7. When a node reads the packet from the remote FIFO it reads the enumerated type to determine how to communicate the packet to its neighbors, just as is done in the physical ASIC.

Also tested in these simulations are tiles which have a "push" architecture. This architecture changes the condition for a node to leave its idle state and send local data whenever the local FIFO is not empty. For this reason the push architecture is also more time consuming to simulate since each node can send a packet at any time, provided that it will inject a hit into its local FIFO following the procedure described in the next section. Nodes which require an interrogation in order to send local data we refer to as the "pull" architecture.

Injected Resets

In order to speed up the execution of the python simulation reset events are precalculated and loaded into separate list containers for each node. At the beginning of every simulation time step every node checks its injected resets list against the new simulation step time. If the new time step is larger than any of the timestamps in its resets list, the resets are then removed from this list and are written to the node's local FIFO.

Resets from simulated data whether radiogenic or neutrino data can occur at any pixel and at any time. The digital node (and the ASIC) is capable of recording multiple resets from multiple channels at the same time. This means that it is possible for multiple different pixel resets to only contribute to one local FIFO write. Therefore, extra care must be taken when adding injected resets with channel information.

In this simulation we consider the best case timestamp measurement for each reset, which is that each digital node can record a unique reset for each channel on every new clock cycle. Then, a procedure for combining resets from multiple channels calculates the clock cycle (timestamp) for which this node would record a timestamp for a particular channel. If a reset has already been recorded for this channel, the un-injected timestamp is incremented by one clock period for this node. The above procedure then repeats until all channels have had all of their resets recorded on unique timestamps for the digital node, where only different channels can be recorded on the same timestamp.

The Simulation Procedure

Upcoming sections will discuss values derived from simulating the readout of the tile. Here we briefly describe the simulation procedure and how the results are obtained. The procedure is also

Simulation Stepping Procedure

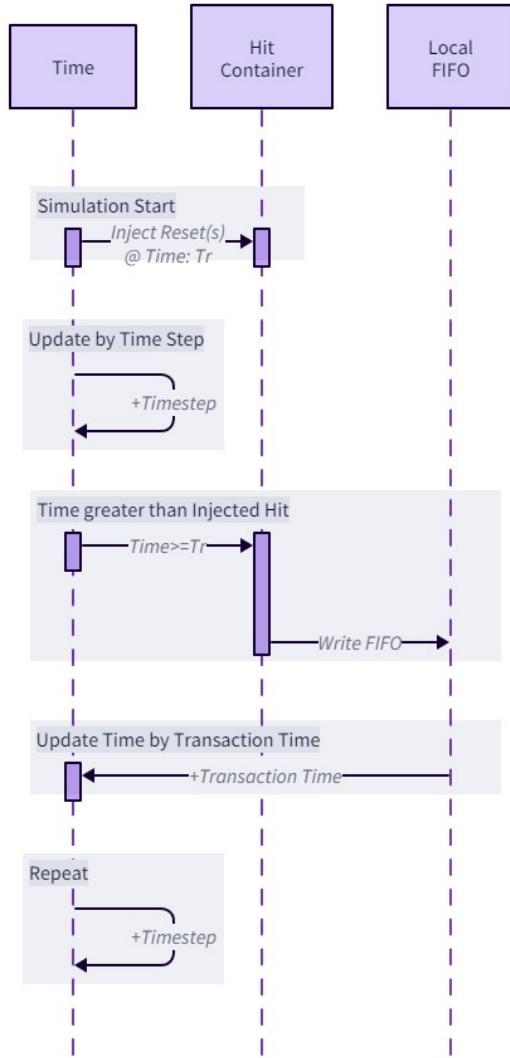


Figure 5.2: Example timeline for simulation time steps and injected hits. Before the simulation begins hits are added into a Hit Container for each node. When the simulation begins the time is incremented by a single time step ($\tau = 1\mu s$). The time increments until it is larger than the time of any of the injected hits. The values of the timestamps are then moved from the Hits container into the Local FIFO, where the timestamp that is recorded is the soonest clock cycle after the "true" time of the injected hit. When the data are ready to be transmitted from the Local FIFO, the time is then updated by transaction time. An example of this procedure is shown in Figure 5.3.

graphically demonstrated in Figure 5.1.

The simulation loop iteratively processes a single transaction from a queue of transactions and then processes all nodes in the tile at incremental timestamps. The timesteps used in the simulation results used here are steps $1 \mu\text{s}$. It is not necessary to perform smaller time steps than this, as packet transactions themselves are on the order of $\approx 50\mu\text{s}$, based on the endeavor protocol. If any processed node generates a new transaction(s), this transaction(s) is added to the transaction queue.

A transaction represents a 64-bit packet that is transferred between two nodes (Sect. 4.3). The sending node is responsible for calculating the true time when this transaction would complete. The receiving node records this byte onto its remote FIFO and performs the state check based on this packet according to Fig 4.7. Then the receiving node updates its time to its soonest clock cycle after this transaction completed. Next, each node in the entire tile is processed one forward timestep. If nodes are in the push state and receive a hit within this timestep window, they create a new outgoing packet, and add this packet to the transaction queue. We note that it is only possible for processed nodes which did not receive the transaction packet to create a new packet if they are in a push-based architecture.

The simulation is complete when all nodes have been processed up to the final requested time and no transactions are left in the queue. In the results presented here we process the tile for one second longer than any injected resets to ensure that the tile is fully read out.

5.2 The Tile Parameters

One goal of the simulations presented here is to parameterize different design choices in constructing both the digital nodes and the tiles. The different parameters which we test are described in Table 5.1.

There are a total of four parameters to test: frequency stability, tile size, routing, and architecture. Of the four parameters, we note that the frequency stability is the one parameter determined by the ASIC's physical design. Therefore, special care must be taken into account when designing the local oscillator for the ASIC. The other variables: routing, architecture, and tile size are either programmable registers or easily configurable in hardware layout.

It is intuitive (and the results indicate) that improved frequency stability leads to a more stable design. Nevertheless, we find it enlightening to demonstrate how remote buffer depths are affected in the case of a 5% (0.5%) clock deviation. When a tile is created with 5% (0.5%) frequency deviation each node within the tile is created by randomly sampling from a Gaussian distribution

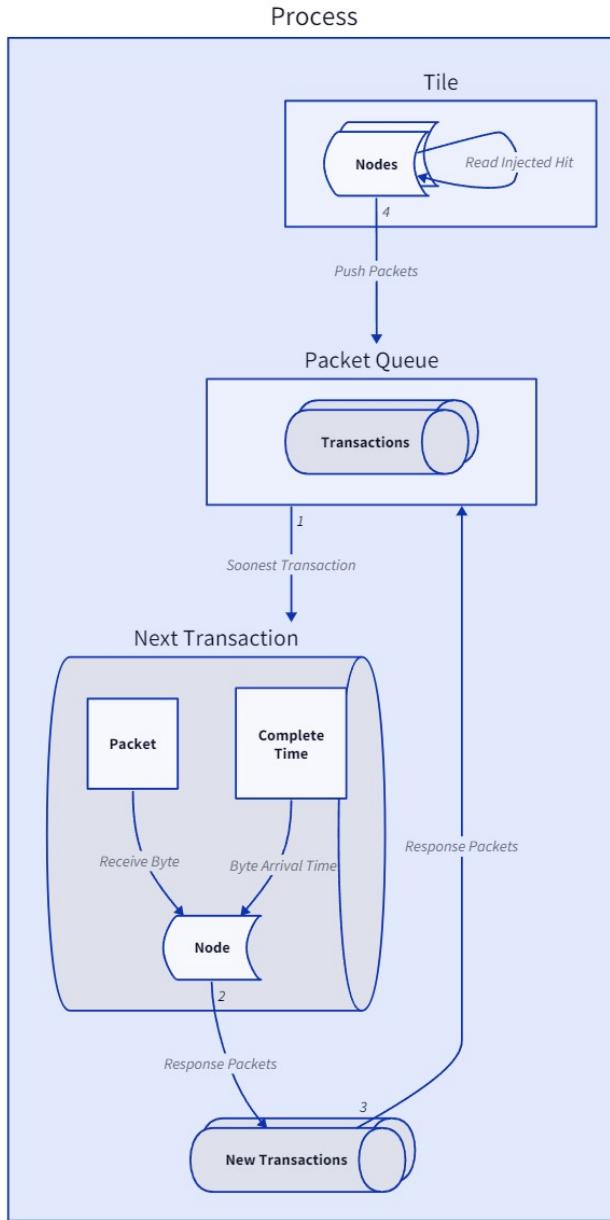


Figure 5.3: Flow chart of the simulation process method which occurs for every simulation time step. The simulation contains a queue of packet transactions. The queue is sorted by ascending time, so that the earliest transaction completed time is processed first. Each transaction contains a packet, a node, and the time the packet arrives. When the node receives the packet, it can optionally create more transactions, depending on the node's state and the packet. Any additional transactions are added to the simulation queue, and are time sorted. The simulation then increments the time for all other nodes within the tile. This procedure repeats until all nodes in the tile reach the designated time (11 seconds).

Parameter	Values Taken	Description
Oscillator Frequency	0.5%, 5%	High variance causes packet buildup or drift within the tile depending on whether packets are sent from slow to fast, or fast to slow clocks.
Tile Size	4×4, 8×8 10×14, 16×16	Affects total number of resets which must be routed to aggregator.
Routing	Snake, Left, and Trunk	Tiles with different routing are effectively different graphs which affect packet buildup (4.5). Different combinations of edges between nodes can cause packet buildup if nodes have more input edges than output edges.
Architecture	Push, Pull	Describes conditions for when node enters transmit-local state. 4.1. The push architecture allows individual nodes to transmit data when data are received, whereas pull architecture only send data upon receiving a special request packet from the aggregator.

Table 5.1: The different tile parameters that are used for the effective tile search. The frequency drift relates the relative distribution of the frequency of adjacent oscillators. The tile size determines how many digital nodes are within a single tile. The routing configurations are described in detail in the previous chapter, and refer to how local data words are sent to the aggregator. The two different architectures define how the node enters the transmit local state. The push architecture enters whenever a new reset is acquired, whereas the pull architecture enters only when a data request is received from the aggregator.

with a mean of 30MHz and a standard deviation of 5% (0.5%). Since many ($\approx 10^4$) events are performed per tile configuration each tile is created with a random seed to ensure that each node is created with the same frequency for each test.

The other design parameters are readily configurable in either hardware (tile size) or through register configurations of the digital node (routing and, possibly, architecture). Tile size is mostly an engineering and cost constraint. Larger tile sizes mean the full design would require less aggregator nodes and require less tiles to parameterize. We show results for small tile sizes to indicate possible connections portions of larger tiles could configure. The largest tile size we tested was 16×16 as the current limit in the Q-Pix digital prototype only allocates four bits for each x or y coordinate in a tile.

The routing and architecture parameters help guide the digital design efforts design of the digital ASIC. In practice it is all but certain that implemented routing for a digital tile will take on a

combination of the routing styles described here. The reason for this is simply that is likely that some digital nodes will fail (for whatever reason) in the life time of a DUNE-FD 10 kT module. Therefore, future tiles that contain hybrid routing we suggest to those users to individually analyze the sub tiles with appropriating routing and frequency distribution and determine if the buffer depths are appropriate.

Oscillator Frequency and Drift

Two different oscillator frequencies are tested, as shown in Table 5.1. These different frequency variances indicate mean differences in oscillator frequency between adjacent nodes. An example of the 5% oscillator variance is shown in Figure 5.2. The values plotted in this figure indicate relative factors above or below the expected 30MHz mean.

Local oscillator drift was not included as a testing parameter since transactions occur over small time scales compared to any likely meaningful oscillator drift. If these drifts occur on time scales much longer than the interrogation time than the oscillator, the frequency could be continually re-calculated with the method shown in the previous chapter. If these drifts are periodic about a mean frequency and on time scales much smaller than the interrogation time window then the drifts would average out. In the event that clock drift timescales are on the interrogation timescale ($\approx 1\text{s}$), then this is equivalent to a frequency uncertainty for the entire transaction cycle. This would mean that an oscillator has a $\approx 5\%$ uncertainty in its frequency on each interrogation. Such a node would not be able to reconstruct timestamps, and therefore not be able to reconstruct the z-position of charge with the required 1ppm estimated uncertainty for Q-Pix clocks [67].

5.3 Simulating The Tile Readout

The tile simulation is performed by injecting hits from two known sources: radiogenic backgrounds and beam neutrinos. All results presented in this chapter are based on 11 seconds of simulated run time. Radiogenic data are collected and used to occupy 10 seconds of background noise resets. The higher intensity neutrino events are offset so that interaction occurs at $t = 5.1\text{s}$. The simulation is run for a total of 11 seconds, instead of 10, to ensure that all of the packets are collected by the aggregator node. In practice, there would be additional resets from backgrounds which occur in that final second of data. However, the number of resets from the radiogenic events are much smaller (by about two orders of magnitude) than the neutrino events.

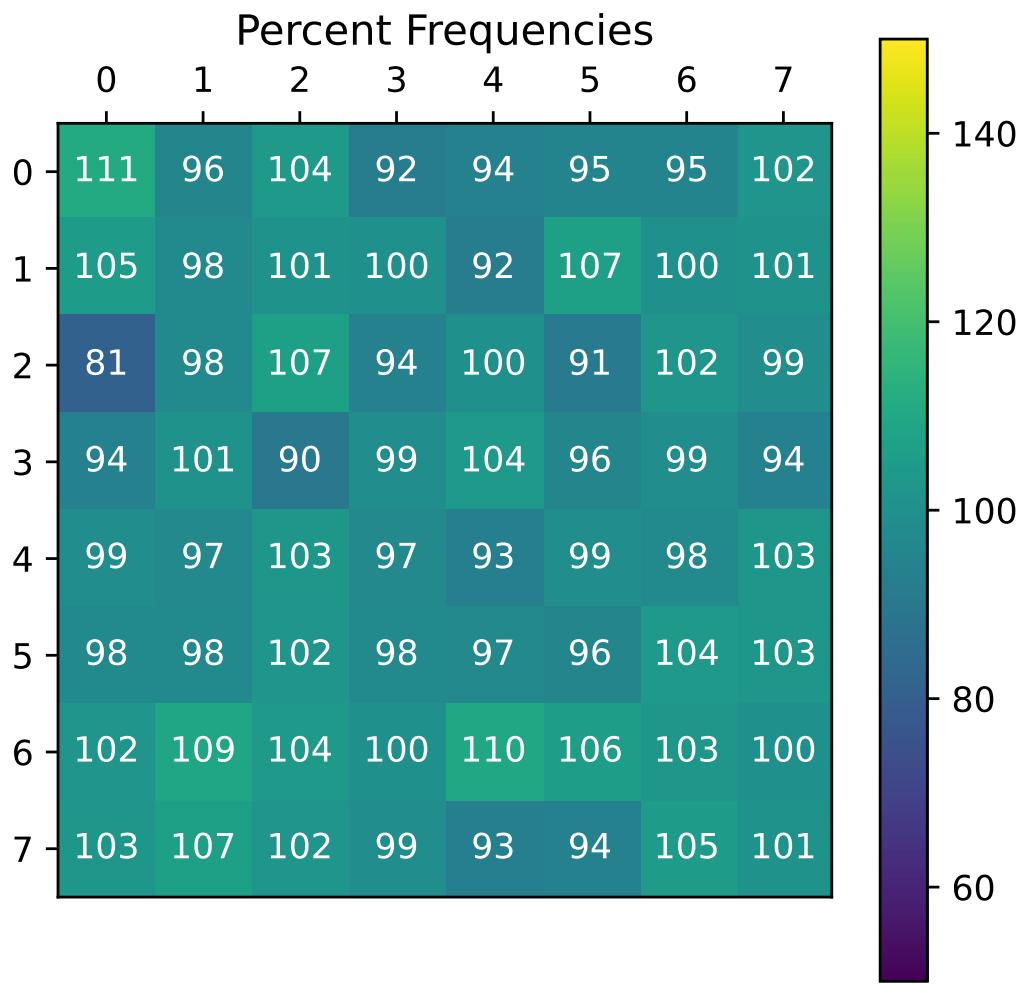


Figure 5.4: Distribution of ASIC frequencies used in the 8×8 tile, and in the example FIFO buffer depths for this chapter. The numbers plotted above each ASIC row and column indicate the relative frequency of this ASIC compared to the nominal 30MHz mean. For example, a number of 112 indicates an ASIC which is 12% faster than 30MHz, a frequency of $\approx 33.6MHz$.

The full readout of the tile occurs based on the number of packets times the average transaction length.

$$T_{readout} \approx 50\mu s \times N_{maxpackets}$$

If we set $T_{readout}$ to 1 second:

$$N_{maxpackets} \approx 20000$$

Since the simulation is run six seconds longer than the origin time of the neutrino events all reset events are accounted for if neutrino events cause less than ≈ 120000 resets. There are no simulated neutrino events which create these number of resets since this would require an energy of $\approx 15\text{GeV}$ deposited into the LAr.

The configuration of each node and the tile happens before the beginning of the simulation. The frequency and the routing directions are configured for each node during its creation.

Simulation Timing

The purpose of the simulation is to examine the communication behavior of digital nodes at different frequencies which communicate via packets of variable time width. For this reason special care is taken to ensure that the timing of packet transactions in the simulation are accurate. The behavior of each node is determined by its state machine properties, as described in Fig. 4.7. Therefore, an accurate measure of timing for each node is equivalent to ensuring that timing of ASIC state transitions are accurate.

Not shown are times when an ASIC receives or responds to a broadcast. Broadcast packets are uniquely handled by ASICs. An ASIC, instead of writing the request to the remote FIFO, immediately handles a broadcast by sending this packet to all neighbor ASICs, excluding the direction from which it received the broadcast. This means that an ASICs state does not change during a broadcast. This is handled by the simulation by tracking packet times on the ASIC connections. The broadcast packet is sent starting at the soonest available time on each connection. The full broadcast procedure is described in Section 4.4.

Snake Timing Example

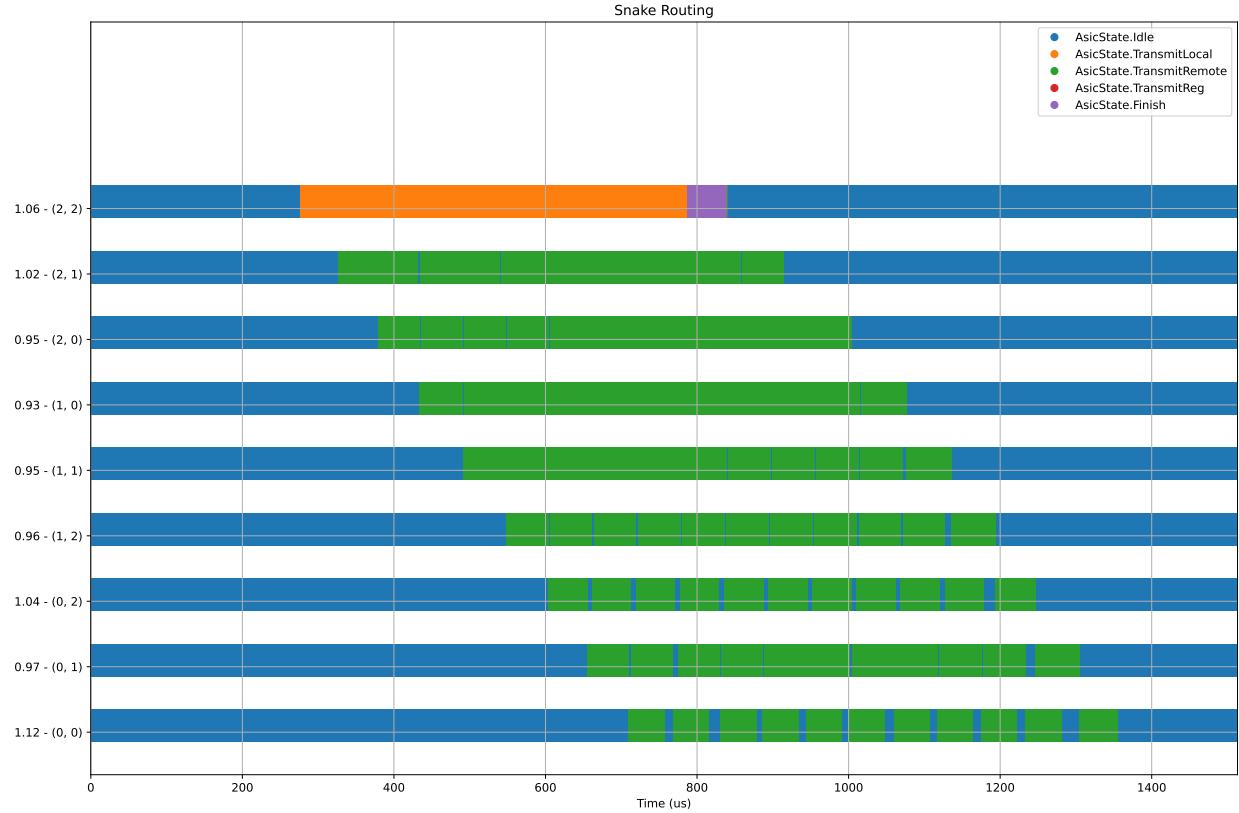
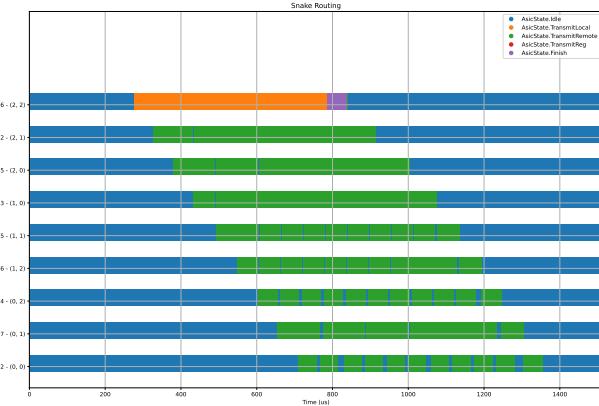
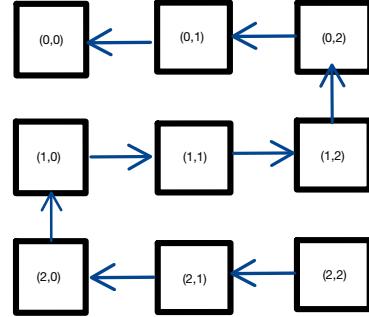


Figure 5.5: Example of timing ASIC state transitions in the simulation framework. The x-axis represents time in μs , and the different y-axis labels represent different ASICs within a 3×3 tile shown. The y-axis also indicates the relative frequencies of the ASICs in the tile, where the node at (0,0) has the fastest frequency, which is 12% faster than 30 MHz. The blue regions indicate that the ASIC is in the idle state. The first orange state indicates that this ASIC (2,2) received a register request from the aggregator node and is now sending its local data, concluding in the purple state, which is sending the event end word. The Packets drift apart in time as they are sent from slower to faster ASICs. Shown here is the possibility of packet drift due to asynchronous packet transfers that depends on the magnitude of the frequency drift between neighbor ASICs.



((a)) Snake Readout timing Diagram



((b)) Data Path in Snake Readout

Figure 5.6: A snake packet transaction example is shown. The broadcast is received by the further node $(2,2)$ and 10 data words are sent, followed by a event end word. Each packet traverses through all nodes in the tile where remote packets are sent immediately.

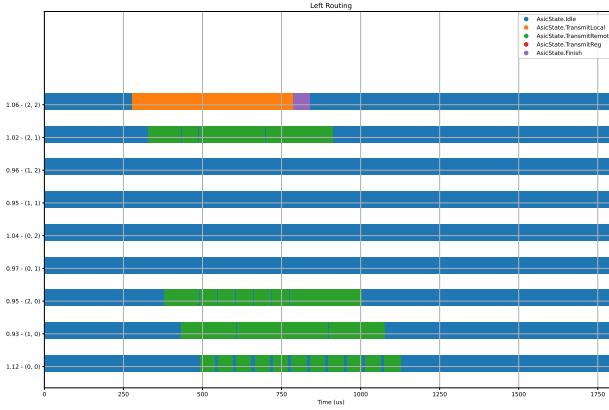
Here we refer to the "snake" routing as the maximal path routing. This routing is one that minimizes the number of input edges for all nodes within a tile. An example of a packet transfer which uses this routing is shown in Figure 5.3.

Since the snake routing minimizes the number of edges, it also maximizes the number of ASICs responsible for sending remote data in the tile. This increases the number of remote transactions in a tile readout. This demonstrated by the amount of time ASICs are in the transmit remote state shown in Figure 5.3.

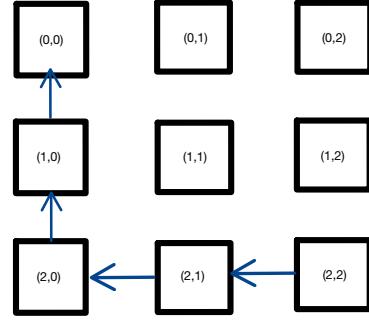
Left Timing Example

The naming convention for the "left" routing is arbitrary since the tile can be viewed from the opposite direction and the routing would appear "right". By "left" routing we mean a routing configuration in which the routed direction for all ASICs in all rows are in the same direction, except for the nodes which have no neighbor in that direction. These nodes then are routed "up" towards the aggregator. An example of a packet transfer with this routing configuration is shown in Figure 5.7.

This routing configuration minimizes the path length for all nodes in the tile when the base-node is at the corner.



((a)) Left Readout timing Diagram



((b)) Data Path in Left Readout

Figure 5.7: A left packet transaction example is shown. The packet transfers begin with the furthest node (2,2) receives a broadcast from the aggregator. The data are then sent to the "left" and then "up" towards the base node, and finally to the aggregator node.

Trunk Timing Example

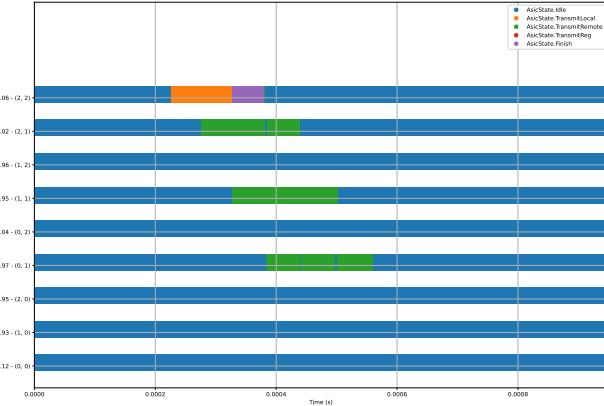
The final routing scheme we simulate we call the "trunk" routing. We name this routing the "trunk" because all data are sent to a central column within the tile and then up towards the edge base node. An example of a simple data transfer is shown in Figure 5.8.

For tiles of widths larger than three there are multiple choices for which column will be the trunk. In for example, a 4×4 tile can have either the second or third columns be the trunk. In all even width cases we test, we choose the smaller row value for simplicity. In the 4×4 case we choose the second column and in the 8×8 case, we choose the fourth (3,0) column instead of the fifth (4,0).

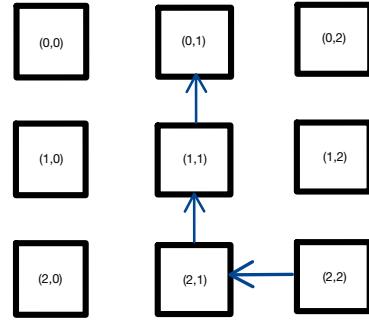
The Pull Architecture and FIFO Depths

The "pull" architecture describes a tile configuration where data are only sent by ASICs within the tile when they receive a broadcast packet. We describe an example simulation event in this section with the pull architecture and the three routing methods to demonstrate which variables are recorded. The example presented in Figure 5.3 stores resets accumulated over ten seconds from both radiogenic backgrounds and a 3GeV ν_e event. The data shown are the total local FIFO transactions (writes) that occurred in the ten second run.

The figures shown in figs. 5.10 to 5.12 demonstrate how the data are accumulated onto the remote FIFO depths for the snake, left, and trunk routings respectively.



((a)) Trunk Readout timing Diagram



((b)) Data Path in Trunk Readout

Figure 5.8: A trunk packet transaction example of two data words and a single event end word is shown. This routing method allows for the fastest possible transaction time since it minimizes the edge lengths between the base node and all other nodes within the tile. In this 3×3 example shown, the base node is at (1,0), or in the middle.

Routing	Local Max	Remote Maximum	Ratio of Remote:Local
Snake	153	208	1.36
Left	153	312	2.04
Trunk	153	306	2.00

Table 5.2: Example results obtained from the three simulation examples for the pull architectures shown in the previous figures. The value of interest in determining the required remote FIFO depths for each ASIC is the maximum depth that occurred on any node. A memory optimized routing configuration is one that would introduce the least strain on the remote buffer depths for a given local buffer depth input.

The following figures demonstrate why it is important to design all ASICs within a tile to meet the same specifications. Future Q-Pix ASICs within a tile will be exposed to events at or above these energy scales, and there is no guarantee (until the ASIC is in hand) what the frequency of its oscillator will be, or its location within a tile. In all three routing examples shown it was not the base node which experienced the most strain on its buffer depth, but the ASIC along the route path which had the lowest frequency.

The Push Architecture

The final simulated parameter to describe is the push architecture. Since the push architecture allows individual nodes to determine when packets can be sent all nodes must be inspected at each

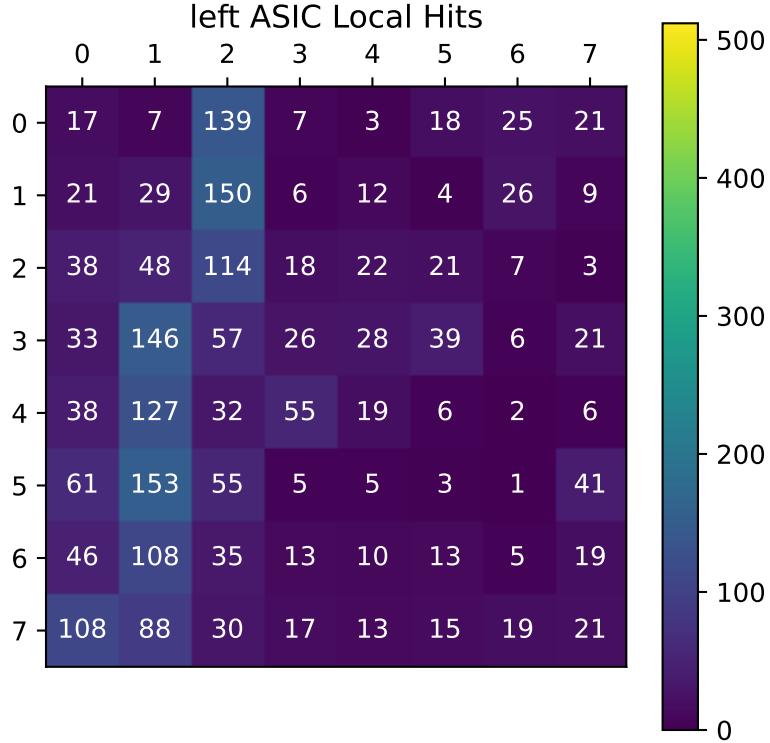
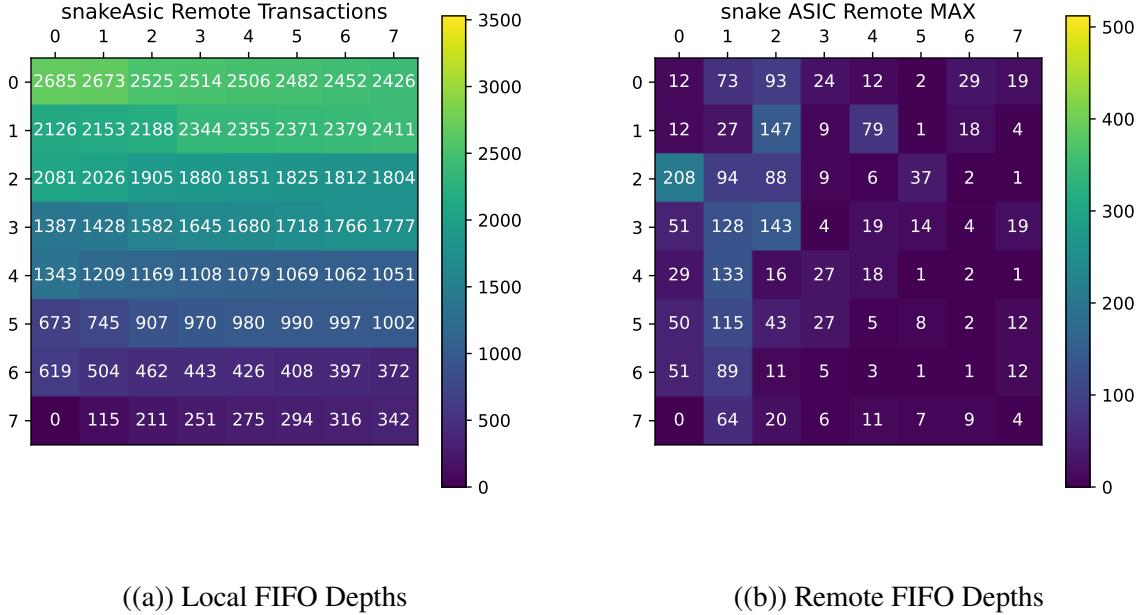


Figure 5.9: Example local FIFO distribution of a $\approx 3\text{GeV}$ ν_e event. The numbers over each tile represent the total number of writes which occurred to each local FIFO in the array. Even with the lowered resolution (each ASIC accounts for 16 pixels), different tracks are noticeable based on the FIFO depths. The maximum scale for the heatmap is chosen to be 512 resets.

time step to check if a reset occurs before this new time window. If a reset occurs at a time before the next simulation timestep, then the reset is removed from this node's hit list and is written to the node's local FIFO. The node will then see at this simulation timestep that the local FIFO is not empty, and leave its idle state to send this packet. An example of this process is shown in Figure 5.3.

Every simulated time step is shown and recorded along the x-axis. The distance in time between simulation steps increases during packet transfers since the nodes state is fully determined during this time. This simplification is performed to speed up simulation run time.



((a)) Local FIFO Depths

((b)) Remote FIFO Depths

Figure 5.10: Example of local (a) and Remote (b) fifo depths of the example neutrino event from 5.3 after processing. The color bar to highlight the maximum number of transactions is used to indicate remote transactions which were happening for 2% of the total readout time of 10 seconds. The node which has the largest remote buffer depth corresponds to the ASIC with the slowest frequency as shown in Figure 5.2. The reason for this excess of buffer depth is due to packet buildup on the slow ASIC.

5.4 Physical Simulation Studies

We now discuss the methodologies of the physical simulations used as input to the digital tile simulation described in the previous section.

Radiogenic Backgrounds as a Calibration Source

In this section we comment on the ability to the auto-calibration of the reset loss per charge. The full charge calibration procedure is beyond the scope of the work presented here, due to intricacies that depend on the final implementation of the reset circuit as well as the replenishment circuit of the final Q-Pix ASIC. This analog front-end ASIC currently exists and these features are currently being explored. Nevertheless, we describe the relevant portions to the problem here since the charge calibration along with the frequency calibration and timestamp measurements determine Q-Pix's z-position reconstruction.

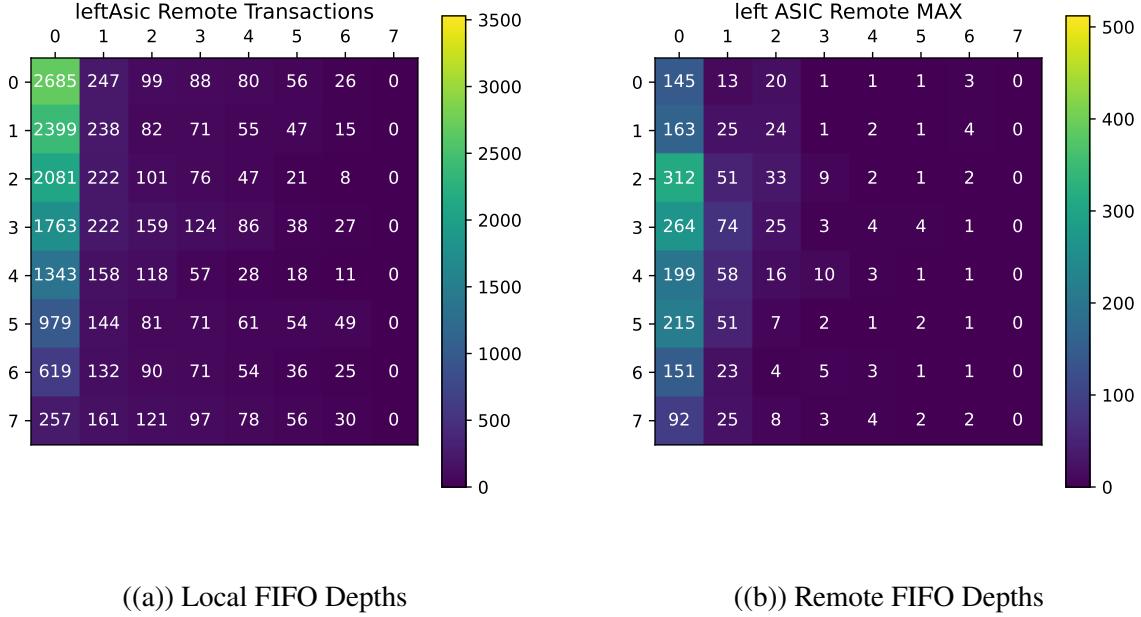


Figure 5.11: Example of local (a) and Remote (b) fifo depths of the example neutrino event from 5.3 after processing. The ASIC which has the largest remote buffer depth also corresponds to the ASIC with the lowest frequency as shown in Figure 5.2.

The main idea behind the auto-calibration of charge at the pixel level relies on using the known (and near constant) input current from the radiogenic backgrounds (mostly ^{39}Ar) in the detector. If a perfectly known and constant input current (I_o) source was input to a pixel it would produce resets separated by a constant time (τ_{rtd}). It would be a straight forward matter to calculate the charge per reset: $Q_o = I_o * \tau_{rtd}$.

Then, to analyze the ability for an auto-calibration procedure for Q-Pix it is important to analyze and understand the long-running charge accumulation (resets) from backgrounds present in the LAr. We use the following list of radiogenic sources of 10 distinct runs of 1000 seconds each. Further details on radiogenic backgrounds in LAr can be found at [38, 83, 84]

The well-known C++ based Geant4 [70] simulation toolkit is used to simulate particle decay and ionizing particle interactions within the LAr volume. We use the energy deposited along the track from each ionizing particle with the W-value for liquid argon (23.6 eV) to determine the number of electrons deposited in the LAr. The resulting number of electrons are then uniformly deposited over the individual track. Then we calculate the probability of recombination for each electron following the "modified box" model [85].

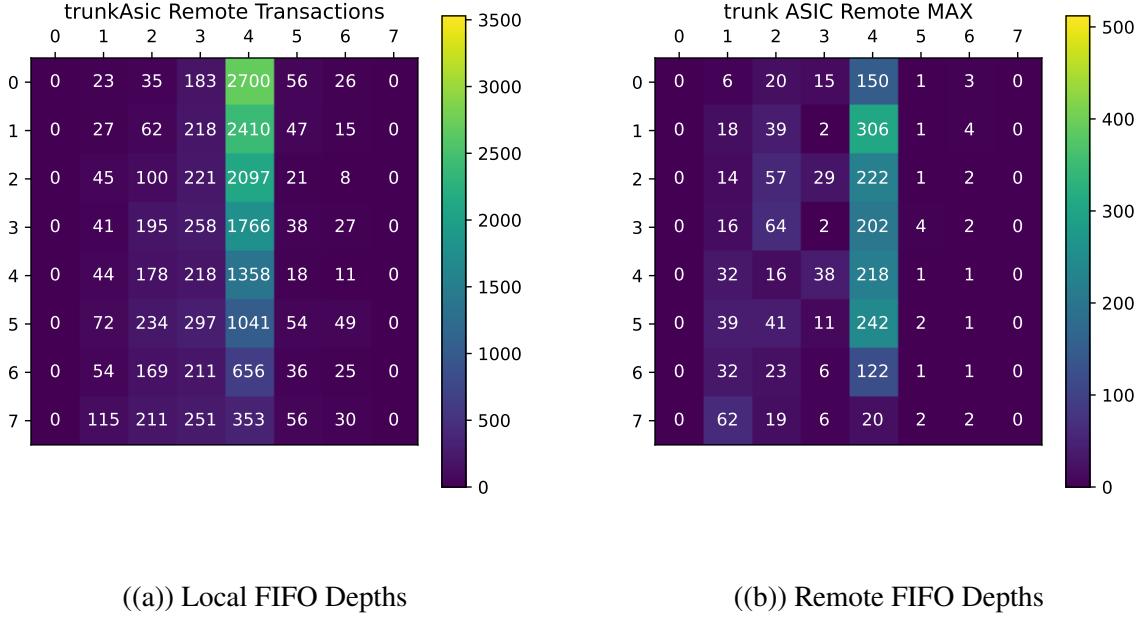


Figure 5.12: Example of local (a) and Remote (b) fifo depths of the example neutrino event from 5.3 after processing. The ASIC which has the largest packet buildup occurs at (4,1). This ASIC also corresponds to the ASIC which has the lowest frequency along the trunk column as shown in Figure 5.2.

The time and location of drift for each electron is calculated with an applied transverse and longitudinal diffusion with values taken from Table 1.4. The simulations for all particle interactions are run individually with a uniform random sampling of the initial decay time interval within the 1000 second window. All of the hits are then sorted by increasing time, so that the first hits read are the hits which occur the earliest. Sorting the hits by time before accumulating charge ensures that the resets are recorded at the correct time.

This simulation produces $\mathcal{O}(10^{11})$ hit interactions which produce $\mathcal{O}(10^{14})$ electrons, which in turn produces $\mathcal{O}(10^9)$ resets. To reduce the memory utilization of the simulation the electrons are accumulated on a hit-by-hit bases and are subdivided into a pre-determined 4×4 cross-sectional area of the detector. Each cross-sectional area defines a pixel. The dimension of the LArTPC volume is $2.3 \text{ m} \times 6.0 \text{ m}$ which divides into 575 pixels in the x-direction and 1500 pixels in the y-direction. There are then a total of 862,500 pixels, which store location and reset information.

As an example, the total resets from 1000 seconds of the simulation are shown in Figure 5.4. The most active pixel receives ≈ 220 resets during this simulation time. The bins for the histogram are

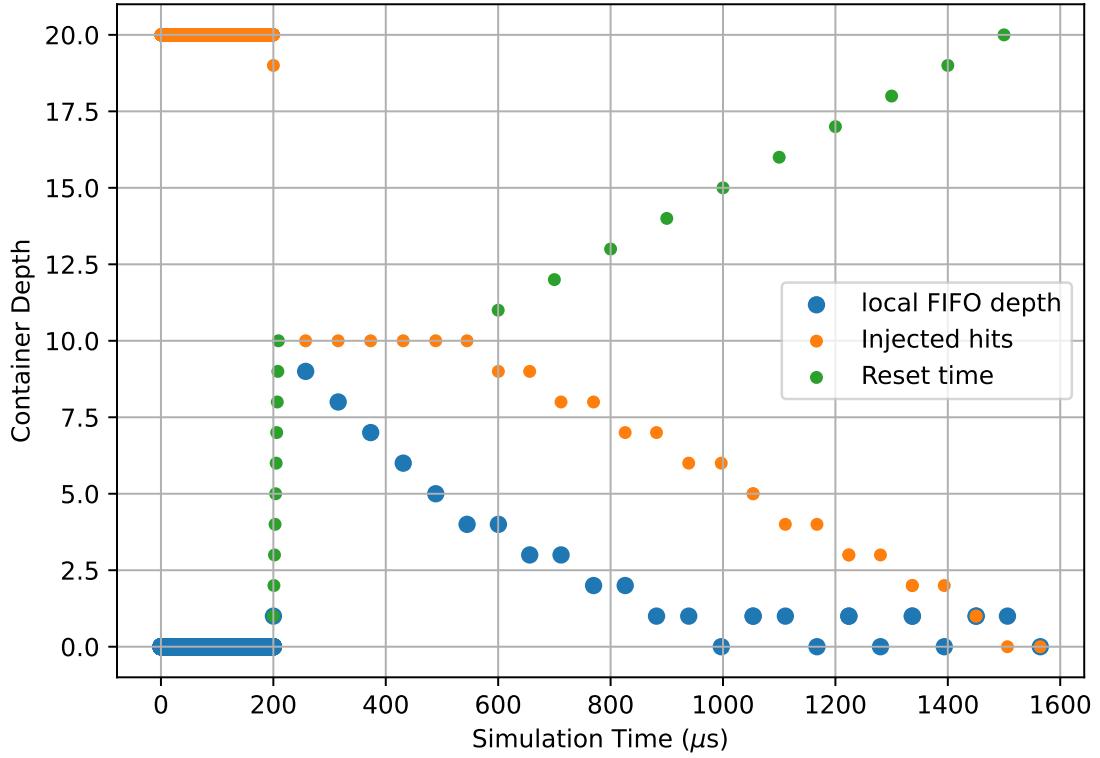


Figure 5.13: A simulated push architecture with 20 injected hits at different times. The time of the injected reset is indicated by the green points. Before the simulation is run a node has its hits injected into a storage (orange) list. Then, at each simulation time step ($\tau_{step} = 1\mu s$) the list is examined to see if a new hit will be written. When a hit is found the relative time of the node can move forward in time to when this packet will be completed in time, while all other writes can occur to the local FIFO. This is why the first local FIFO depth increases initially by one despite 10 nearly adjacent injected hits. On the next time step, the depth then moves to nine; the simulation has sent the first of the 10 packets, and records nine. This example correctly shows a maximum local FIFO depth of nine.

Isotope	Rate [Bq/kg]	Region	Region Mass [kg]	Rate [Bq]	Number of Decays (per 10 s window)
^{210}Po	0.2	PD [Bq/m ²]	2.46856	0.493712	5
^{60}Co	0.0455	CPA	90	4.095	41
^{40}K	0.49	APA	258	1,264.2	12,642
^{39}Ar	1.010	bulk LAr	70,000	70,700	707,000
^{42}Ar	0.000092	bulk LAr	70,000	6.44	64
^{42}K	0.000092	bulk LAr	70,000	6.44	64
^{222}Rn	0.04	bulk LAr	70,000	2800	28,000
^{214}Pb	0.01	bulk LAr	70,000	700	7,000
^{214}Bi	0.01	bulk LAr	70,000	700	7,000
^{85}Kr	0.115	bulk LAr	70,000	8050	80,500

Table 5.3: The radiogenic background distribution is the same as that found in previous work [69]. For each 1000 second analysis the pre-rounded values are scaled up by a factor of 100 to achieve the correct normalization of events for each isotope. A key difference between the backgrounds is the origin or source of each background. Of special note is ^{40}K whose source location is the APA beams, and whose resets can be distinctly seen in Figure 5.4 as the slightly more active (yellow) region of the APA. Due to this source alone, it is likely that precise auto-calibration for charges will likely have to account for the pixel location within the APA.

at the pixel level and represent the $4 \times 4 \text{ mm}^2$ of each pixel.

Additional information is tracked for each reset to identify the contribution of each radiogenic background for each reset. A reset occurs when 6250 e^- have accumulated on a pixel. The time recorded for the reset is the same as the time the simulation calculates the last of the required 6250 electrons to arrive at the designated pixel region. This optimization was added to the existing simulation framework to separate the unknown analog contribution to the timing uncertainty from the physical simulation.

In practice the analog front-end reset circuit obviously takes time to respond to added charge and to issue a replenishment and reset commands. There will always be some delay between the final electron's arrival, the time of the analog reset, the replenishment circuit, and the time recorded on the digital back-end. However, for the purposes of this analysis, we assume that this reset and replenishment circuit activity can happen more quickly than the average local oscillator of the digital back-end. Therefore this analysis assumes the best timing measurement based on the digital back-end. The time measurement is then limited only by the clock frequency of each local oscillator. Finally, we comment that this optimization of the timing of the analog front-end affects

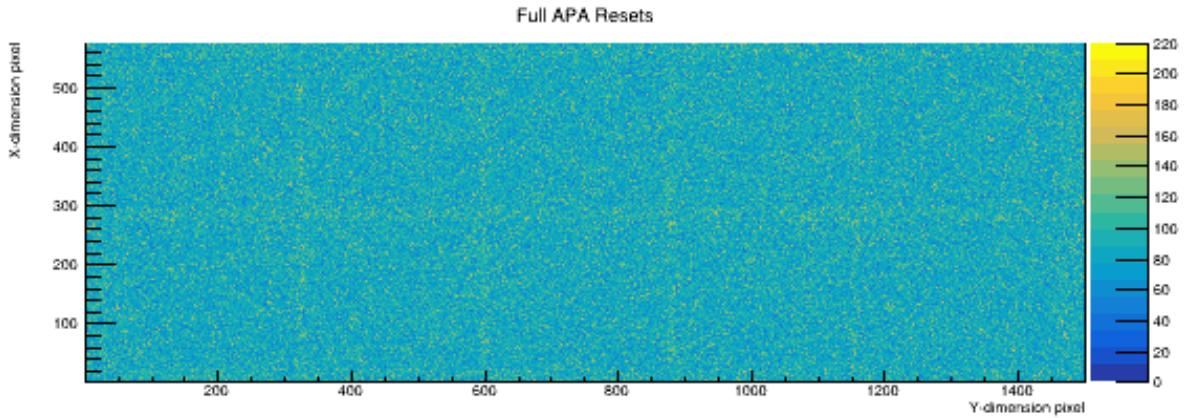


Figure 5.14: Full 1000 second of radiogenic background source simulation input into all pixels within the APA. A close examination of the resets can reveal the additional resets from the backgrounds which are location dependent. The majority of the uneven distribution of resets occur at the location of the APA bars due to the ^{40}K isotope.

only the time values, and by extension, the reconstruction of the particle tracks. It does not affect the total amount of charge, and therefore the total number of resets recorded by each pixel.

Any combination of the backgrounds can contribute some or all of the electrons required to produce a reset. The contribution of the total electrons for each of the radiogenic sources are shown in Figure 5.18. We refer to the contribution of the number of the electrons to the reset as the "weight" of the reset.

The ability to perform a charge auto-calibration using radiogenic events depends on the background to provide a reliable average input current source. We use only the data presented in Figure 5.4 and calculate the mean time between resets for all pixels. For this simple calculation, we simply take the total number of pixels (4096) and divide by the total number of recorded resets (411152) and obtain an average RTD of 9.96 seconds.

A very rough expectation of background current is $I_o \approx 100 \text{ aA}$. We can then use the following equation to calculate:

$$I_o = \frac{Q_o}{\tau_{rtd}}$$

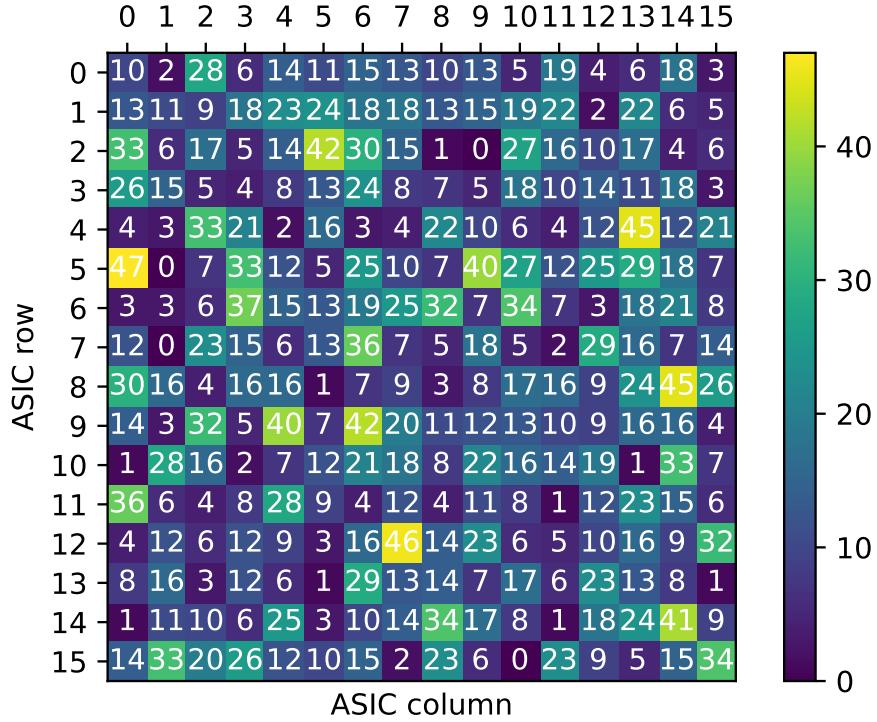


Figure 5.15: Baseline noise input for the digital simulation from all radiogenic sources and background leakage current. This figure shows the total resets in the 10 second window for the 16×16 tile. The other tile size configurations (4×4, 8×8, 10×14) also use these reset data for background noise. All tiles start with the top left node as their origin node.

solving for Q_o with $\tau_{rtd} = 9.96$ and $I_o \approx 100$ aA, we obtain:

$$Q_o \approx 100 * 10^{-18} * 9.96 / 1.6 * 10^{-19} \approx 6225$$

Calibration results from the first analog prototype and a more sophisticated analysis will be needed for pixel level charge calibration. The contrived derivation above assumes equal capacitance and charge replenishment on all pixels, which in practice is not necessarily true. Additional tests can likely be done for each pixel by comparing the peak of the distributions as shown in Figure 5.4.

Such an analysis is not appropriate yet since it is not yet known what the leakage current will be in the Q-Pix ASIC. As shown in both Figure 5.4 and Figure 5.18, the contribution from noise is not negligible. Therefore, any true analysis of the charge auto-calibration ability of Q-Pix awaits studies of both the leakage current and replenishment circuits of the analog front-end.

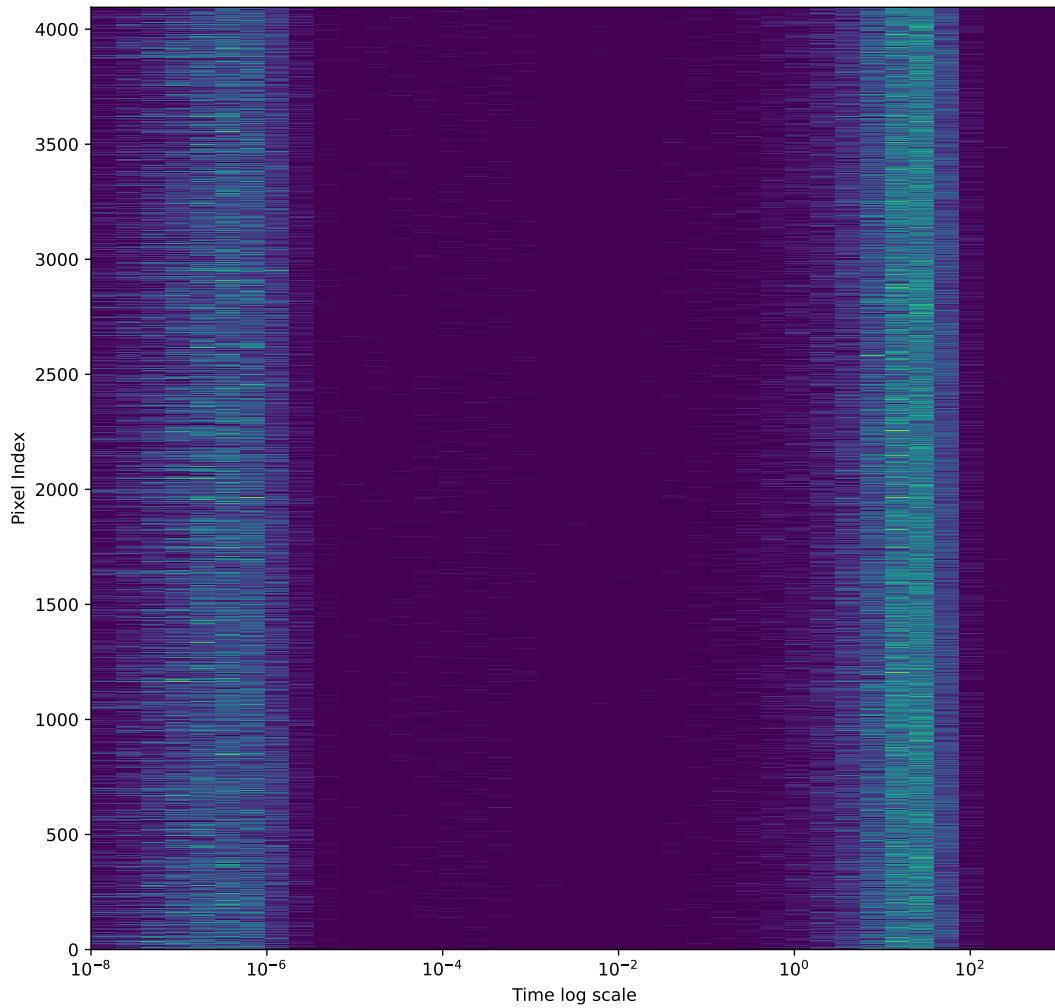


Figure 5.16: All 4096 pixels in the 16×16 tile for 1000 seconds of radiogenic data. The y-axis represents a different pixel, and the x-axis is a log-scale time axis with even bin widths. There are two clusters of resets for different time intervals. The first large cluster of resets occurs at $\approx 10^{-7}$ seconds and is due to a single radiogenic decay event causing additional resets. The second large cluster of resets occurs at ≈ 10 seconds. This second cluster of resets is caused from the first reset of a new radiogenic decay event. The ability to perform a charge calibration per pixel may depend on accurately resolving the mean for this "long period" RTD.

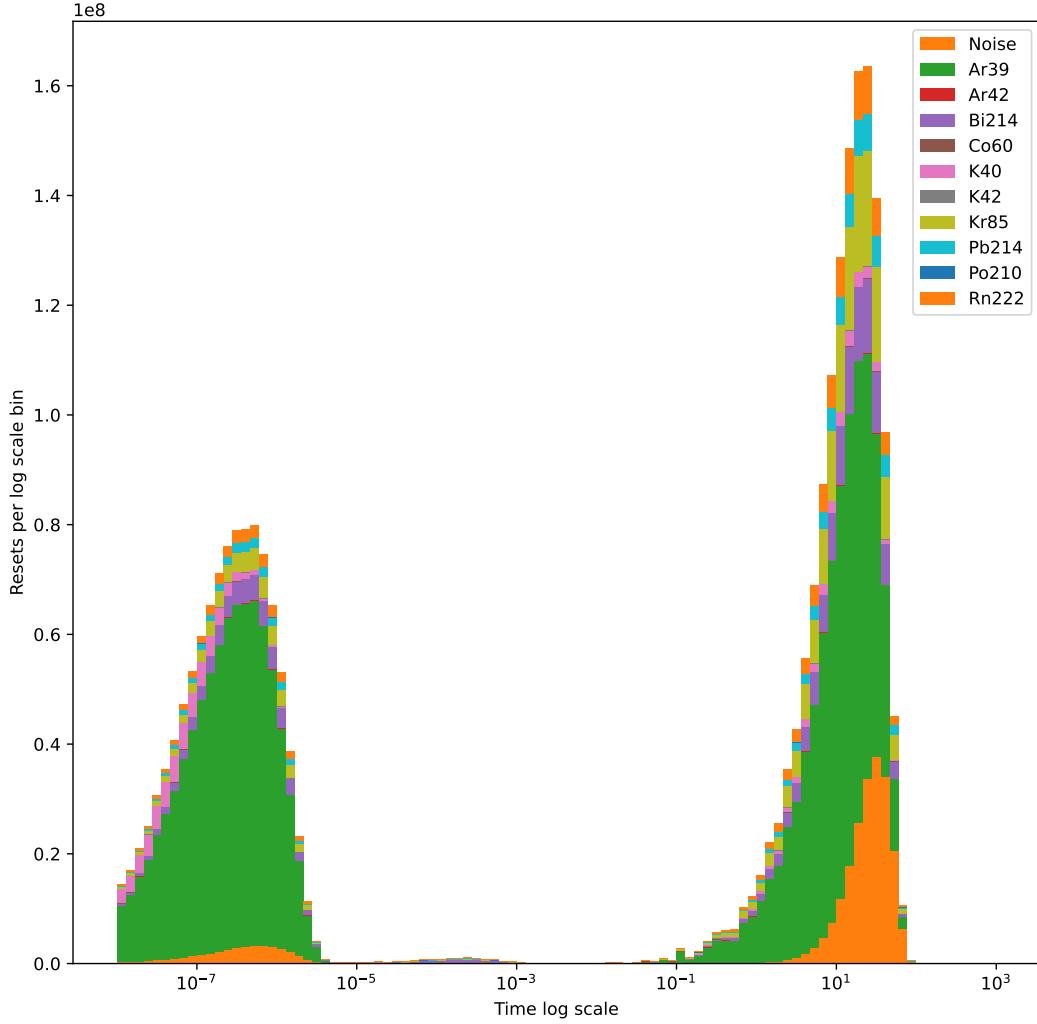
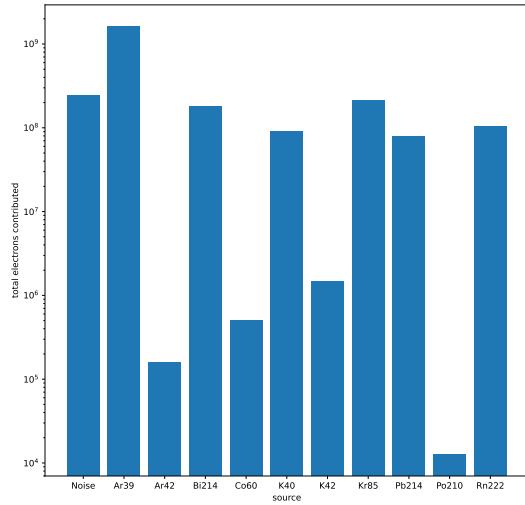
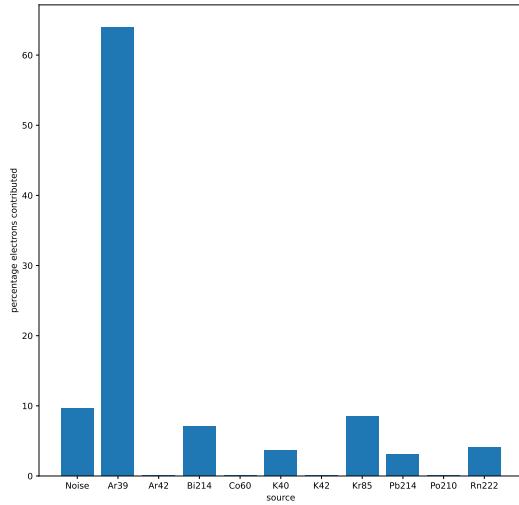


Figure 5.17: All 4096 pixels in the 16×16 array for 1000 seconds of radiogenic data. These data are the same as those shown in Figure 5.4, where all pixel RTDs are binned together. There are two clusters of resets on two different time scales. The first cluster of resets near at $\tau_{rtd} \approx \mathcal{O}(10^{-7})$ is due to events which produce more than one reset. The second cluster of resets near at $\tau_{rtd} \approx \mathcal{O}(10^1)$ are from a "waiting" period where there is no charge buildup from decays and only background noise. The dominant source of electrons on each pixel is from the ^{39}Ar , with a non-zero contribution from leakage. The leakage current value used in this simulation is 10 aA.



((a)) Contribution of total electrons.



((b)) Contribution of electrons by percentage.

Figure 5.18: Both figures indicate a comparison of the amount of electrons deposited on all pixels in the tile shown in Figure 5.4. Plot (A) represents the total number of electrons on a log scale. As expected, ^{39}Ar contributes the majority of background charge. The leakage current used is 10 aA, and represents about 10% of the total contribution of electrons. This implies that leakage currents from the front circuit which are ≈ 100 aA will contribute nearly as much electrons to the steady-state RTDs as the radiogenic backgrounds.

Reset Contribution of Radiogenic Sources and Leakage Current

Figure 5.18 compares the total (Plot-A) and percentage (Plot-B) electrons contributed from noise and radiogenic sources. These results highlight the importance of understanding and mitigating any leakage current for every pixel. A leakage current of 10 aA contributes $\approx 10\%$ to the total background current. What may prove difficult in the auto-calibration procedure of the Q-Pix readout is that while the contribution from radiogenic sources shown in Figure 5.18 may be the same, the leakage contributions may not be.

5.5 Neutrino Interaction Studies

Here we discuss the implementation of the digital framework within the high energy regime. For this we use as an input neutrino events from the Long-Baseline Neutrino Facility (LBNF) [39] and take the unoscillated flux of neutrinos which were used in [86]. These neutrino flux are simulated

using GENIE [87], v2.12.10. The interaction distributions for both the forward and reverse horn current directions are shown in Figure 5.5.

We do not perform any calculation involving the oscillation on the input neutrino flux. The reason for this is that the digital back-end should be able to fully record data from all possible ν_l events regardless of interaction type, not only the intended ν_e appearance spectra. It is equally important for a future readout to be able to correctly tag noise (ν_μ , or ν_e from the beam, etc.). For example, sensitivity to mass ordering and CP violation rely on the ability to measure ν_μ disappearance in addition to the ν_e appearance.

What will be shown in the upcoming sections is that capability of the digital back-end depends on the energy deposited in the volume of the LAr. By the virtue that oscillations change only the flavor (not the energy) of the ν , the constraints of the back-end do not depend on if more (or less) ν_e are measured compared to $\bar{\nu}_e$, provided the back-end is capable of fully measuring both events. Furthermore, by using the unoscillated flux of the neutrinos at the near detector, the neutrinos will be of necessarily higher energy than the expected flux at the far detector. The use of high energy helps in establishing what we will show as the upper-bound for the required local and remote FIFO depths for each ASIC.

Neutrino Event Parameters

Table 5.4 describes the parameters of each input for the simulation. The parameters used to vary the tiles for these neutrino input energies are shown on Table 5.1.

The Q-Pix readout presented here is designed for use in a LArTPC at the scale of DUNE-FD 10kT module 1.3. In order to test what kinds of requirements this readout will need we use high energy neutrino interactions as discussed in Section 5.5. The different selection parameters for each event are neutrino flavor, neutrino energy, horn current direction, Z-position vertex position, and source neutrino momentum direction (θ_z). We define the beam direction (the direction parallel to the surface of the APA) as $\theta_z = 0$. The X and Y positions are held constant for all interactions, at X = 120 cm and Y = 3200 cm.

The LBNF beam is not the only source of high energy particles DUNE will detect. Other high energy ($\simeq 10$ GeV) interactions may come from other sources. These other high energy events (such as nucleon decay, cosmic neutrinos) may also deposit energy on GeV scales per interaction.

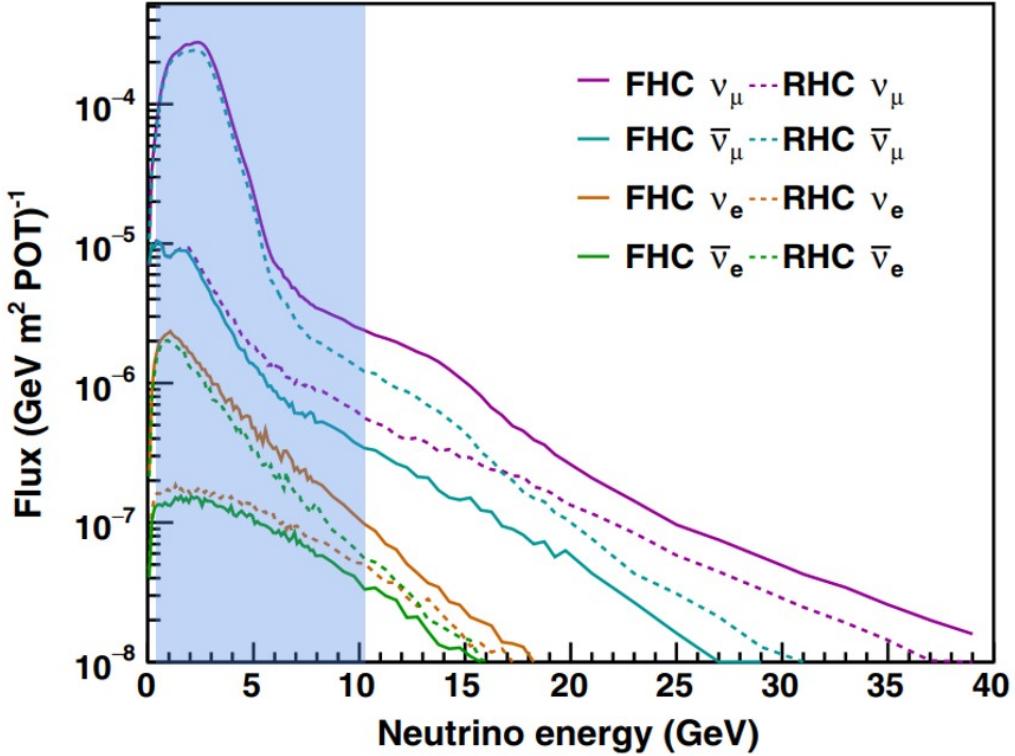


Figure 5.19: Flux spectrum of neutrinos from the neutrino beam used in this study. This figure is taken from [88]. Highlighted in blue is the reconstructed energy range of neutrinos that are used to seed the interaction with the APA LAr's volume.

These sources may interact with their net momentum vector pointing in any direction. For this reason we also test ν_e and ν_μ interactions at $\theta_z \pm 90^\circ$; this direction causes the secondary ionizing particles to carry momentum along the direction parallel to the pixel's surface normal. These two momentum directions, though nonphysical for beam interactions, still present possible interactions types within the scope of DUNE's proposed physics program [37].

Neutrino Event Results

Every simulated neutrino interaction generates some number of resets which are collected onto the pixel plane. The purpose of the study explored by the parameters described in Table 5.4 is

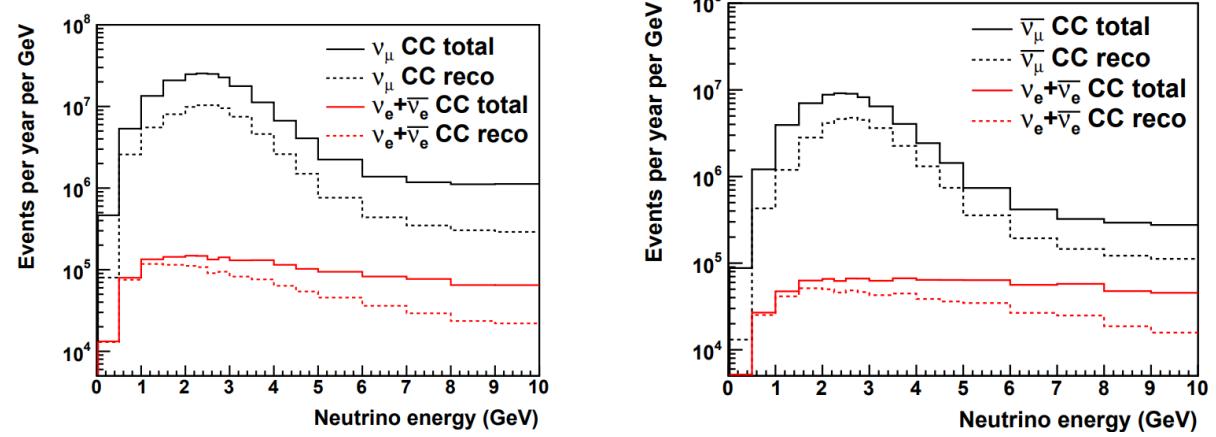


Figure 5.20: Rate of CC neutrino interactions based on flavor as a function of true neutrino energy. Figure is taken directly from [86]. Right is shown the neutrino interaction distribution for the forward horn current. The left image is for the reverse horn current. Both images assume an average exposure rate of 1.2 MW from LBNF beam.

to investigate the charge resets these interactions produce; we pay particularly close attention to ASICs where the number of resets (energy deposited) is the largest in a given event.

We bin the maximum number of resets in a 4×4 pixel array, or ASIC, for every neutrino event. The plot Figure 5.23-(A) shows a ν_e event and Figure 5.5 shows these resets binned into pixels. For every event we take the maximum ASIC value and use that as an entry into a histogram. Next, we take the integral of each histogram as shown in (B) of Figure 5.23 and (B) of Figure 5.24. The value of this integral gives the percentage of fully events a function of local FIFO depth.

Neutrino Energy Deposit

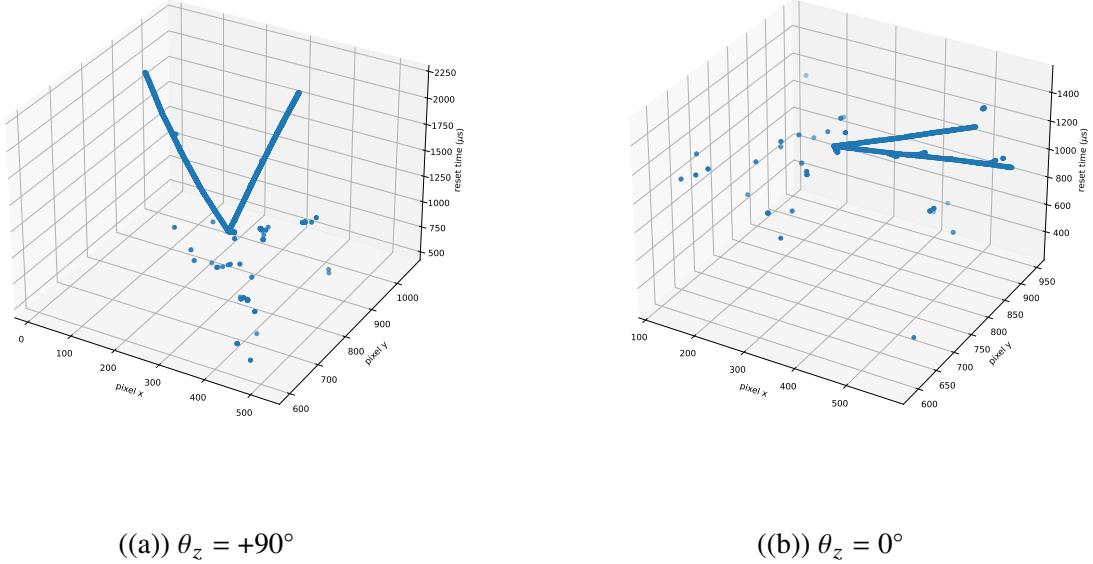
The true neutrino interaction energy is notoriously difficult to reconstruct. The neutrino itself carries no charge and its track is not directly reconstructed in the LAr. Other effects such as long

Name	Values	Relation
ν_l	$\nu_e, \bar{\nu}_e, \nu_\mu, \bar{\nu}_\mu$	Oscillation measurements require sensitivity to measurements for both ν_e appearance, and ν_μ disappearance.
ν_l Energy	0.25 GeV to 10 GeV, in steps of 0.25 GeV	neutrino energy determines output secondary energy, which causes more resets and directly affects buffer depths.
Horn Current	Forward and Reverse	Beam horn current direction affects neutrino flux, as shown in Figure 5.5. Additionally, mass hierarchy measurements (according to the MSW effect [64]) require difference in measurements of appearance probability for ν_e and $\bar{\nu}_e$.
Z-position	10 cm, 80 cm, 180 cm, 280 cm, 350 cm	Interaction z-position above the anode plane. Interactions which happen further from the collection plane have more time to diffuse or recombine.
θ_z	$0^\circ, \pm 2^\circ, \pm 90^\circ$	Different momentum angles are different Z-positions, in general, direct ionized particle tracks within the active volume.

Table 5.4: The different neutrino simulation parameters which are passed into Geant4 based simulation. The original interaction products are generated using GENIE [87] v2.12.10. The output products of the neutrino interaction produced from GENIE are then configured using the different parameters described above. We select ν_l events for different energies in bin-widths of 250 MeV; We follow the same bin width as is done in [36] for their neutrino oscillation analysis. A selection of 100 events for each ν_l is taken within each energy bin, for a total of 3900 ν_l events for each horn current direction, z-position, and θ_z selection. Since there are two current directions, four ν_l , five z-positions, and five θ_z positions, a total of 780,000 neutrino events are simulated.

neutron drift make perfect energy reconstruction of the neutrino interaction impossible by principle. For these reasons we show how the resets and ASIC FIFO depths vary both by the energy deposited into the LAr as well as the true neutrino energy. Figure 5.25 shows the relationship between the true ν_e energy and the max FIFO depth as well as the total APA resets. Figure 5.26 shows the same relationships instead as a function of the energy deposited.

One of the key differences of a Q-Pix readout compared to a traditional waveform readout is that the amount of data the Q-Pix readout collects depends on the energy deposited. Since Q-Pix is fundamentally a counting readout, the amount of counts (data) it collects depends on the amount of energy deposited. Therefore, one limit on its bandwidth is the total amount of resets it can measure, which is proportional to the energy deposited as shown in Figure 5.5.



((a)) $\theta_z = +90^\circ$

((b)) $\theta_z = 0^\circ$

Figure 5.21: Same ν_e interaction at Z-position = 180cm, which is in the middle of the drift length of the APA. Image (A) has the incident ν_e momentum rotated upwards ($\theta_z = +90^\circ$). Image (B) has the incident ν_e had momentum along the beam direction ($\theta_z = 0^\circ$). Since there are five different z-positions, and five different θ_z values, each of the 3900 ν_l interactions are repeated 25 times. These two plots show two of those 25 examples.

Local FIFO Depth Results

To predict the required local FIFO depth for the Q-pix ASIC, we perform the integral as shown in Figure 5.23 for each of the parameters described in Table 5.4. Since there are 200 different parameters, there are 200 different integral values.

Figure 5.30 and Figure 5.5 show the same integral results, but with different labeling. The results show two different distributions of buffer depths: those along the near-beam angle ($\theta_z \approx 0^\circ$) and near the azimuthal angle ($\theta_z \approx \pm 90^\circ$). The Table A.1 shows the complete list of values for the required local FIFO depth for each combination of the 200 parameters for the 95% and 99% capture intervals.

The two different distributions indicate that there are at least two different design specifications for

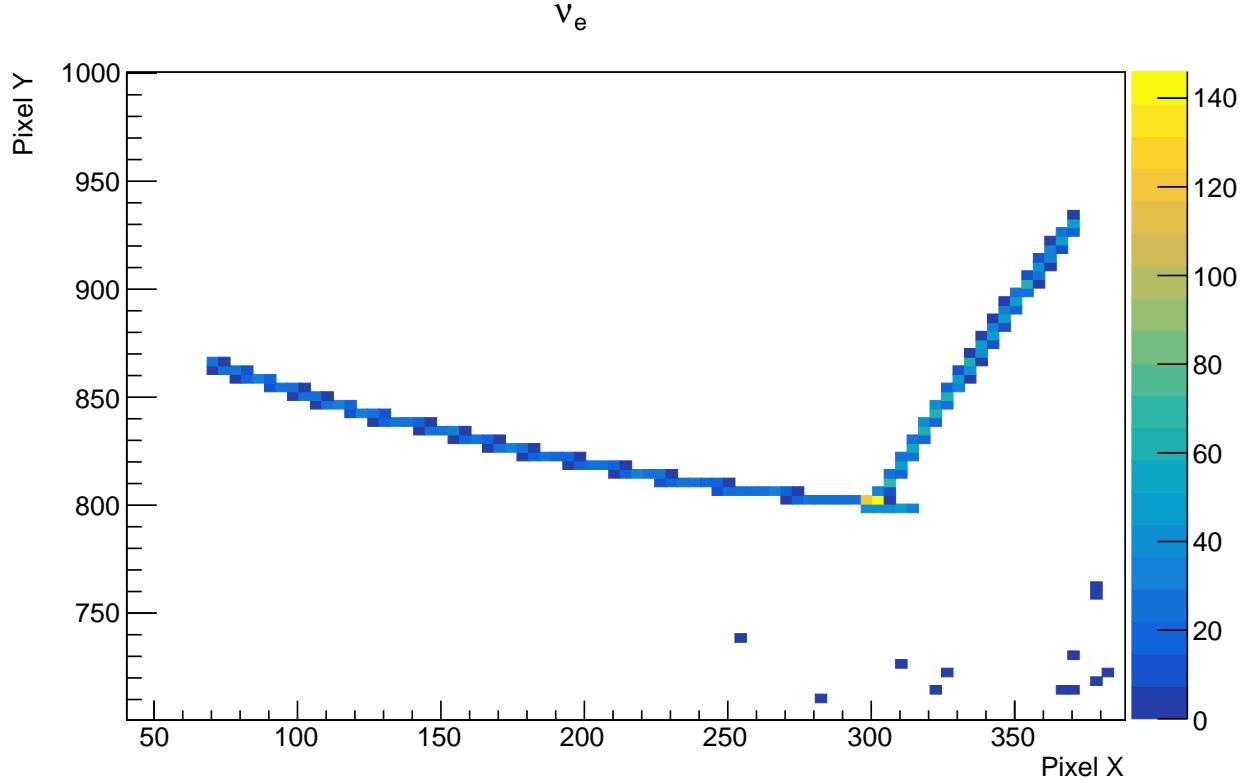
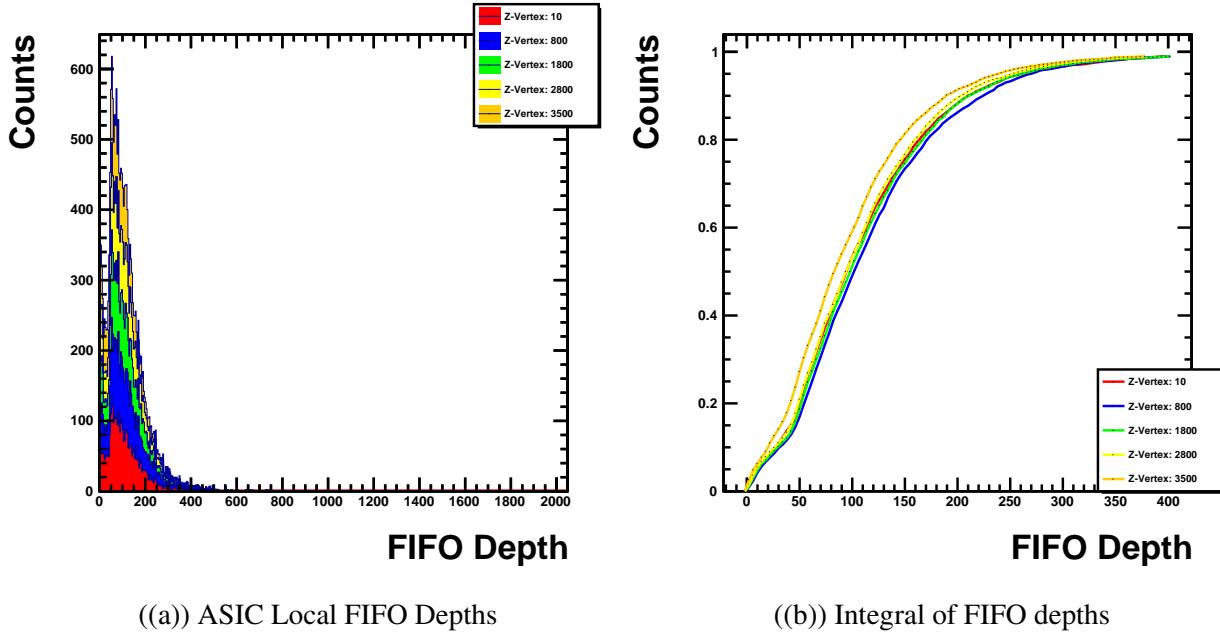


Figure 5.22: The same ν_e event as the one shown in Figure 5.21-(A). The plot is zoomed into to the region of interest where the bin widths represent the pixels dimensions in the collection plane. The energy of this ν_e was 546.1 MeV, and considering that each reset requires 0.1475 MeV, the maximum number of resets this event could produce is ≈ 4368 . The histogram records 3733 total resets. The most active pixel received 144 resets. When the pixels are binned into ASICs (4×4 pixels) the maximum number resets an ASIC received is 347.

future Q-Pix prototypes. The first capture distribution has a maximum value of 426. Therefore, a Q-Pix ASIC with a local FIFO depth of 426 would be able to fully capture resets for 99% of all neutrino interactions under 10 GeV and momentum within $\pm 2^\circ$ of the beam axis. In order for Q-Pix to record all resets of the same energy average energy but with momentum near the azimuthal ($\theta_z \approx \pm 90^\circ$) it would require a buffer depth of 1670.

5.6 Q-Pix for Neutrino Oscillation Measurements

The LBNF beam flux, neutrino oscillations, and neutrino cross-sections all affect the predicted neutrino event rate at the DUNE-FD. Instead of applying these factors the previous analysis tested neutrino interactions from a uniform distribution of true incident energy. We discuss Q-Pix's back-end requirements and extend our back-end analysis to the expected neutrino (dis)appearance



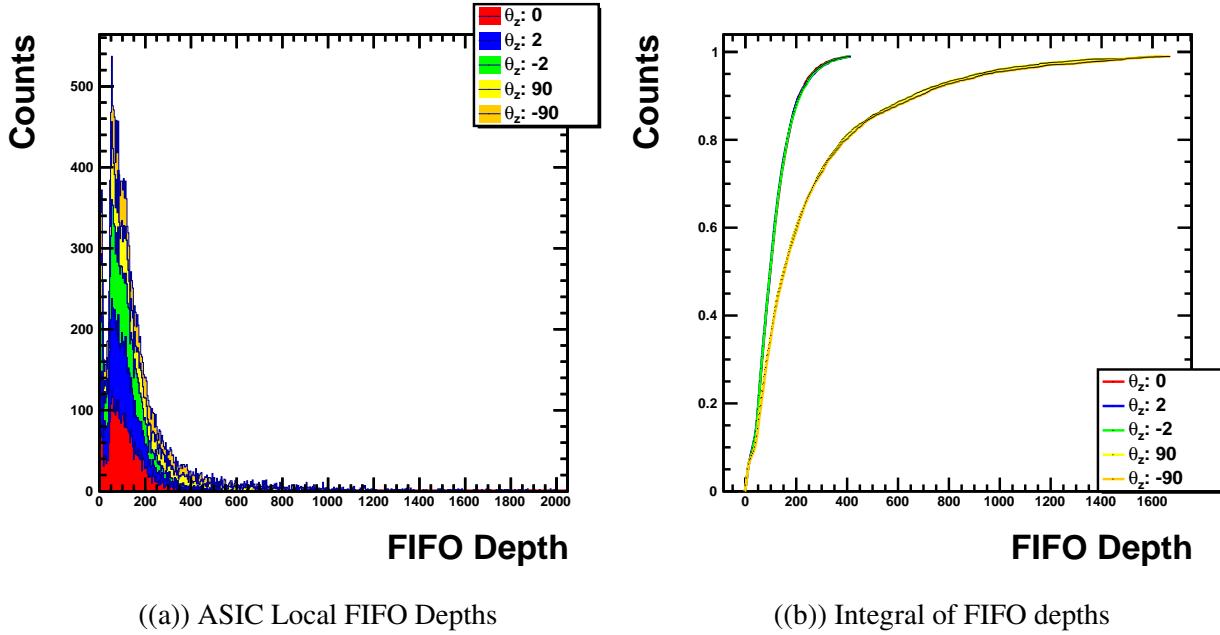
((a)) ASIC Local FIFO Depths

((b)) Integral of FIFO depths

Figure 5.23: Example ν_e events for different z-position of the vertex with $\theta_z = 0$ held constant. Plot (A) bins the maximum value of local FIFO depth for all 3900 events (ν_l energies between 250 MeV - 10 GeV) for variable z-position and $\theta_z = 0$. Plot (B) shows the running integral for each histogram shown in plot (A). The integral continues until 99% of all events are counted. This process is repeated for all 200 possible parameter choices as discussed in Table 5.4.

spectra as presented in [36]

To account for neutrino oscillation appearance probability as a function of energy, we weight each neutrino event based on the expected (dis)appearance spectra for each (anti)neutrino flavor as shown in Figures section 5.6. Since both flavors of (anti)neutrino have the peak of the distribution is below 5 GeV, and the previous use a uniform weighting for events up to 10 GeV the required buffer depths are an over estimate. Lower average energy interactions will produce less resets, which will require smaller buffer sizes. Figure 5.5 clearly shows the relationship between the energy deposited and the number of resets collected. The FIFO depth requirements for neutrino oscillation measurements at the DUNE-FD are shown in Figure 5.6.



((a)) ASIC Local FIFO Depths

((b)) Integral of FIFO depths

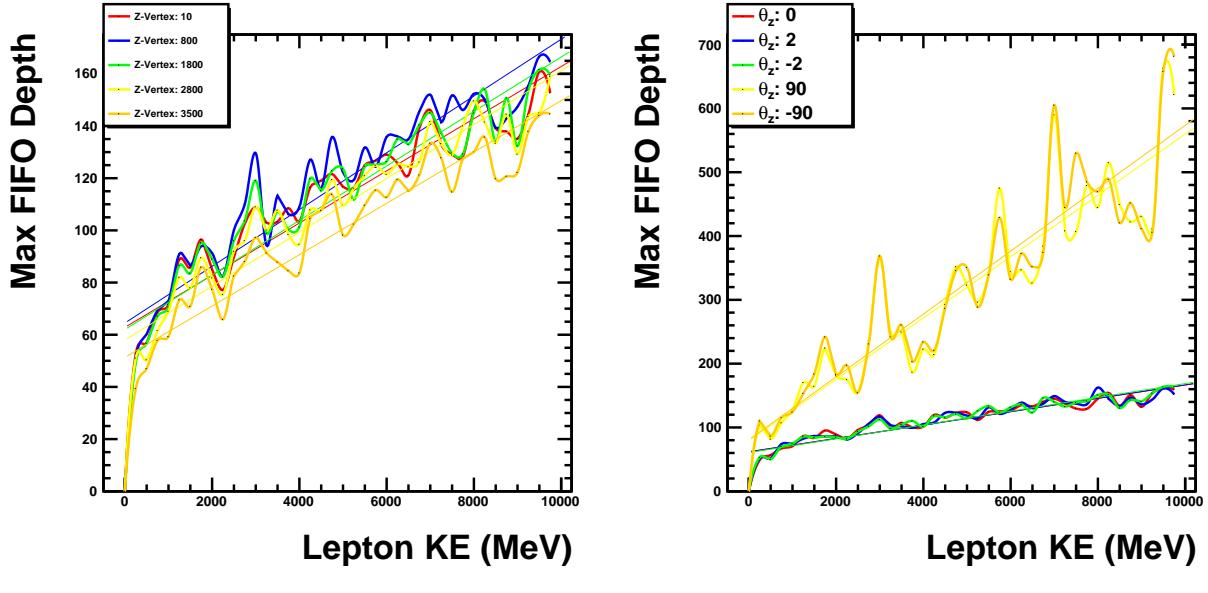
Figure 5.24: Example ν_e events for different θ_z with the vertex held constant with z-position = 180 cm. This is a similar plot to Figure 5.23 with the exception that θ_z is varied and the z-position is held constant at $z = 180$ cm. A notable difference to note here is the run away effect of the large values of θ_z . This effect is intuitive: the initial momentum direction affects the direction of where most charge will be deposited. As more charge is localized an ASICs area, it will collect more resets.

5.7 Neutrinos, Backgrounds, and Routing

A valid full reconstruction requires all packets to be collected regardless of neutrino type, energy within the valid range, interaction vertex, and should also be able to accept a range of incoming momentum angles. In this final section of the chapter we combine the results of the neutrino interactions as well as the radiogenic and leakage backgrounds into the simulation framework described in Section 5.1, which is based on the graph developed in Chapter 4. This back-end simulation framework is also my sole and independent work.

Combining the Digital and Physical Simulations

To synthesize the results of the neutrino events and the background sources we take a reference 10 second window slice from a 1000 second simulation of backgrounds as described in Section 5.3. We then select a single ν_e interaction from the forward horn current direction, where we accept any incoming θ_z , z-position, and energy. This event is offset to occur at time: $\tau_{int} = 5.1$ seconds. We do not perform this readout simulations for all parameters in Table 5.4 as Figure 5.31 indicates that



((a)) Constant $\theta_z = 0$ direction.

((b)) Constant Z-Position: $Z = 180$ cm.

Figure 5.25: Comparison of buffer depths as a function of energy for different parameters of θ_z and z-position. There is a large variance between the true ν_l incident energy and the actual energy deposited in the LAr. This is the reason why only the means are plotted for each energy bin. Plot-(A) shows that the average z-position has a minor affect on the overall local FIFO depth, where the furthest position has the lowest average reset count. Plot-(B) shows average FIFO depth for varied θ_z . The two curves represented by $\theta_z = \pm 90^\circ$ are similar because they use the same seeded events only pointed up or down, and should have the symmetrical effect since vertex is located in the center of the APA.

the local buffer requirement does not largely depend on neutrino flavor.

We choose $\tau_{int} = 5.1$ s so that the interaction occurs just after interrogation request from the aggregator node. This ensures that the entire ν_e interaction is buffered onto all local FIFOs in the tile before the request. We note that this time offset is the same for the push architecture, even though the neutrino reset packets will be sent when they are acquired.

Remote FIFO Depth Results

Figure 5.35 shows combined results for the remote transactions, remote FIFO depth, and 99% capture requirements. The remote transactions for both the left and trunk routings are much smaller on average than the snake routing for the reasons described in Section 5.3.

The Table 5.5 contains the results for the effect the different routings have on the average number of transactions.

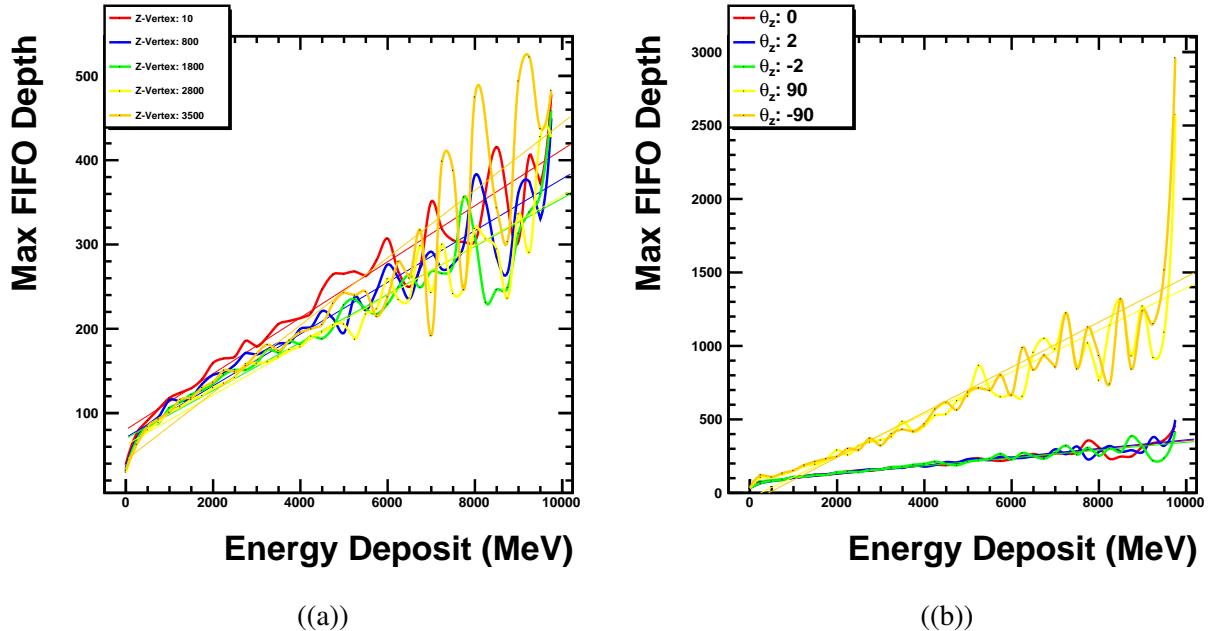


Figure 5.26: A comparison of ASIC resets vs the energy deposited into the LAr. Plot-(B) shows for Z-position=10 cm ends at ≈ 2 GeV since no ν_e events deposit this much energy into the LAr. Both plots indicate that the

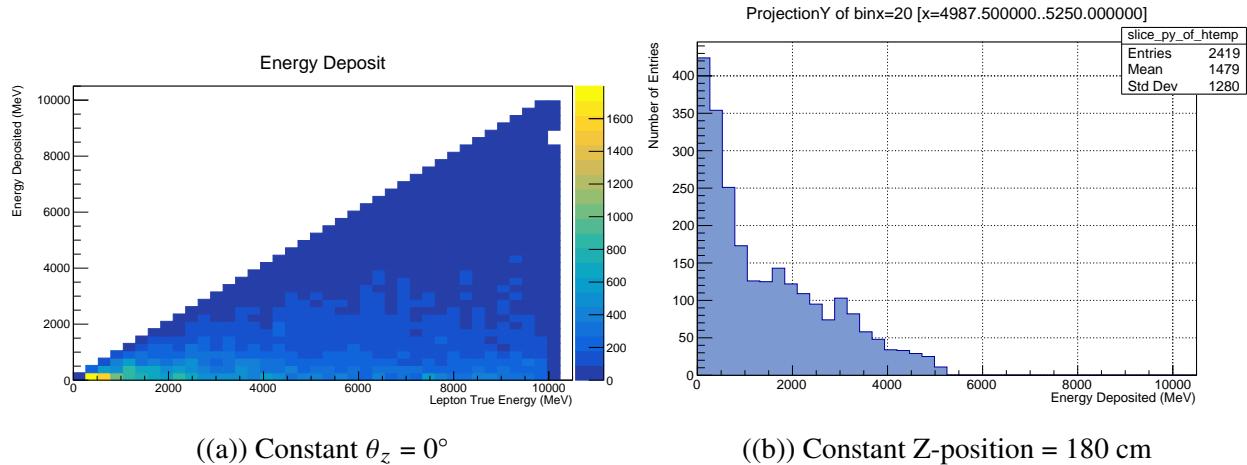


Figure 5.27: Plot-(A) shows a comparison of the energy deposited into the LAr as a function of the input neutrino (ν_e). Plot-(B) shows a projection against the y-axis for a single bin. The maximum allowed total energy deposited is limited to the total energy of the input neutrino. However, the lower bound for all energies is still, obviously, zero. Therefore, as the input neutrino energy increases the upper bound also increases. The mean value of Plot-(B) indicates that even for a maximum allowed total energy of 5 GeV the mean (average) energy deposited per event is 1479 MeV. Most interactions deposit less than 2 GeV into the LAr, as shown in Figure 5.27. Some pileup events are removed, see Figure 5.5.

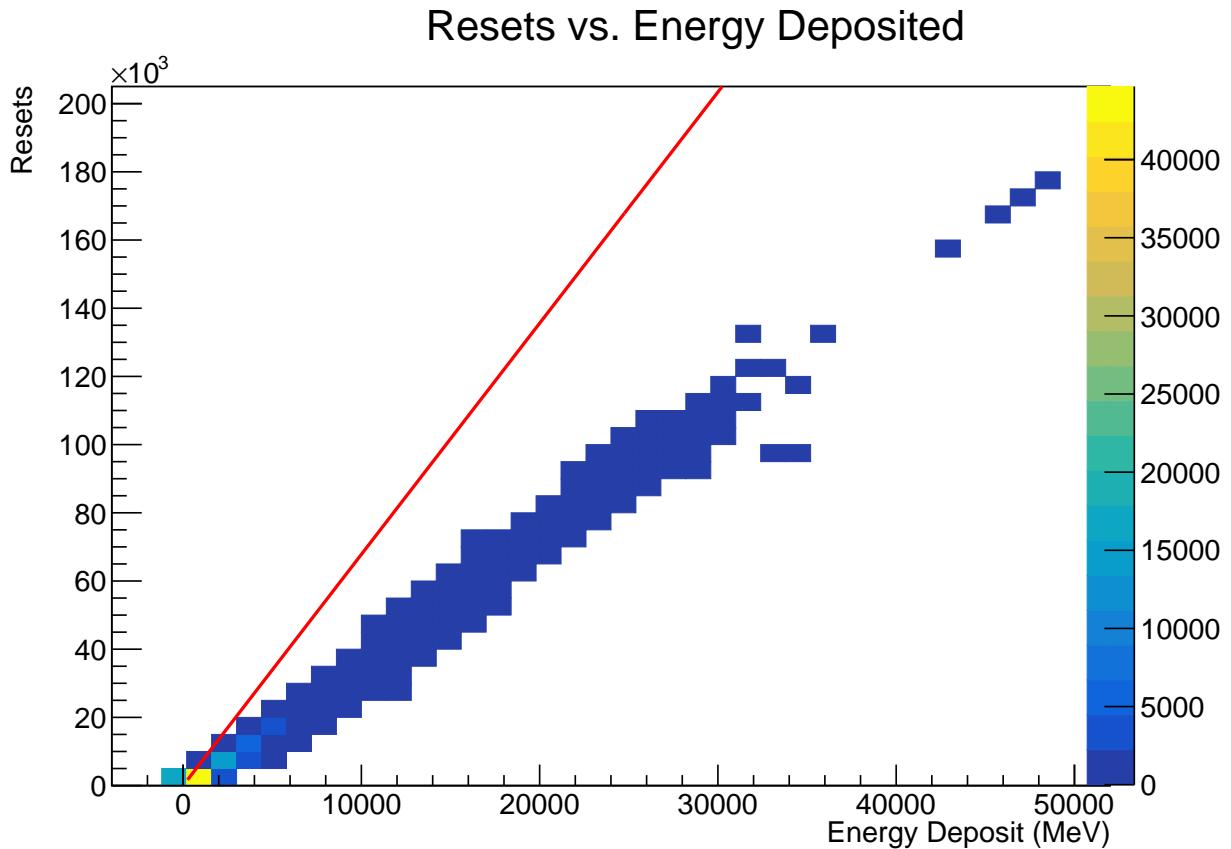


Figure 5.28: A relationship between the total number of resets detected in the APA and the energy deposited for ν_e interactions is shown. The solid red line indicates the maximum number of resets that could be measured for a given energy. The small distribution of energies below zero correspond to events that produced no resets. The energy deposited goes above the the threshold limit of 10 GeV. These events carry extra energy from additional leptons which are from pile-up at the DUNE-ND from the FNAL beam. These data are not included in the energy deposited analysis, or in the integrals as shown in Figure 5.21. These high energy deposit events are also not included in the FIFO depth analysis, since these events are beyond the energy range for oscillation measurements. These events are also removed from Figure 5.27.

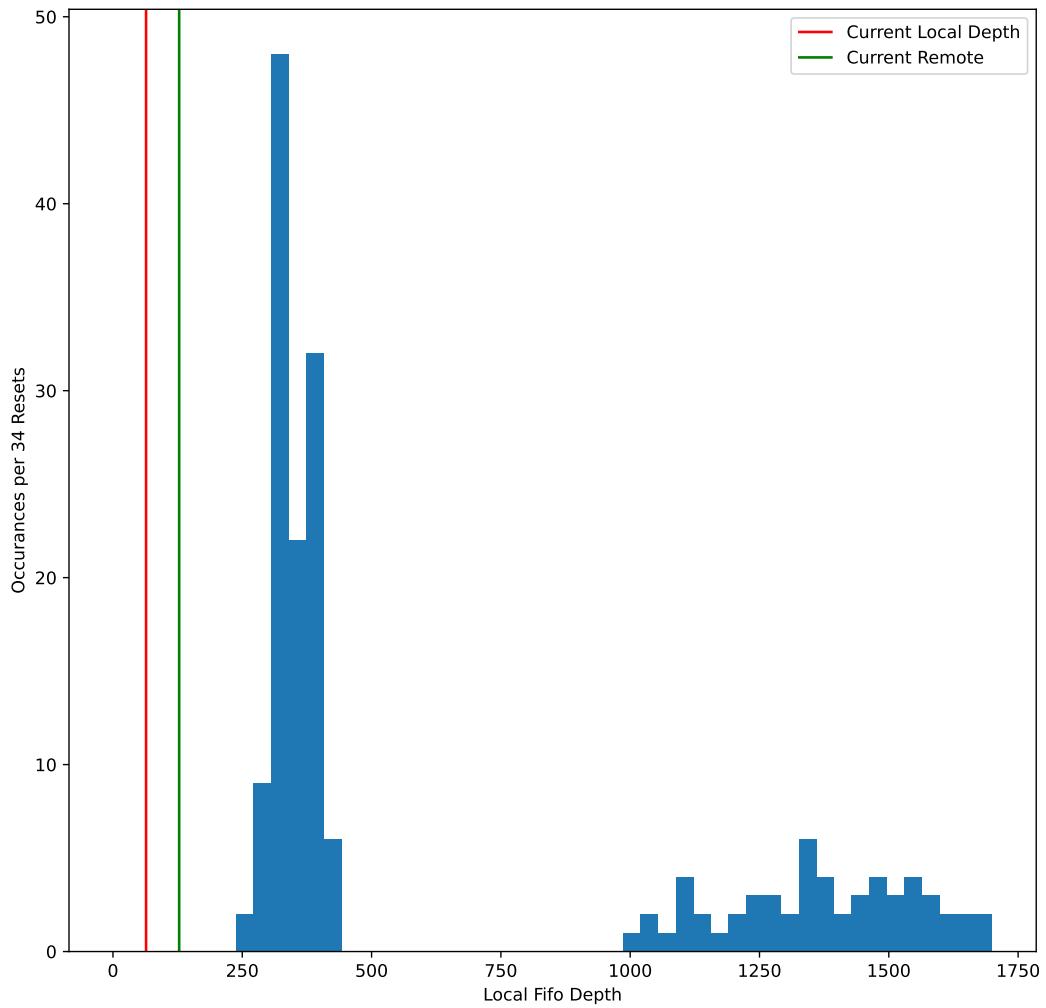
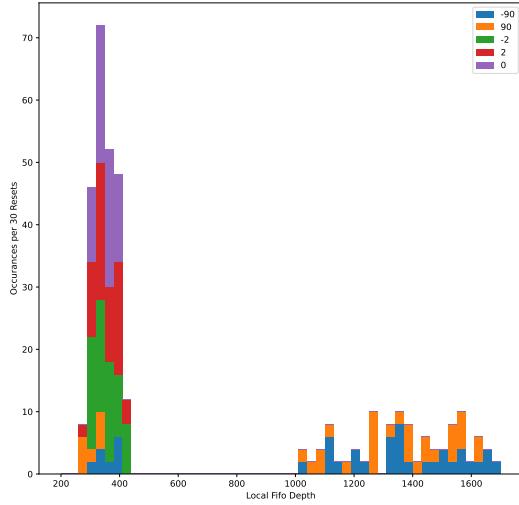
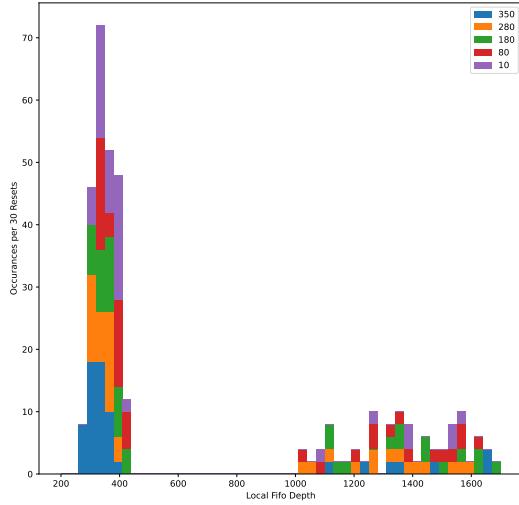


Figure 5.29: Total integral data for all neutrino event parameters described in Table 5.4. The values of the integrals binned in this figure can be found in Appendix A. These data clearly indicate two different distributions of FIFO requirements. The final Q-Pix design will choose some local FIFO depth. The current Q-Pix digital prototype local and remote FIFO depths are also shown by the red and green lines, respectively. The data in this plot required 6520 electrons to produce a single reset ($C_{pixel} = 1 \text{ fC}$ and $V_{pixel} = 1 \text{ V}$). Should the pixel's capacitance or voltage change, the x-axis of this plot would scale approximately by the same factor.



((a)) Colored by θ_z direction.



((b)) Colored by Z-position

Figure 5.30: Comparison of buffer depths integrated over energy colored by different parameters of θ_z and z-position. The most important result is shown in Plot-(A), which clearly indicates that only two different parameters account for the distribution of larger local FIFO depths. As expected, θ_z affects the localization of charge over individual ASICs which affect the local FIFO depth. Plot-(B) shows the distribution of resets indicated by different z-positions. Plot-(B) differs in that the second distribution of resets contains elements from each of the different z-positions.

The Table 5.6 summarizes the results of Plot-(B) in Figure 5.35 for the parameters described in Table 5.1.

The Table 5.7 summarizes the linear fit results of Plot-(D) in Figure 5.35 for the parameters described in Table 5.1. The final column of this table indicates the relative fit from the push-based architecture, for which only the snake routing was tested.

5.8 Summary and Further Studies

The results presented in this section provide first physical analysis of the Q-Pix digital readout. Included in the analysis are long exposure to radiogenic background sources, leakage current, neutrino beam events, and the response of the digital back-end ASICs. All events occur in a $2.3 \times 6.0 \text{ m}^2$ LAr container, with a maximum drift distance of 3.6 m. The parameters of the Geant4 simulation are identical to those in Table two from [69] with the exception that the sampling time

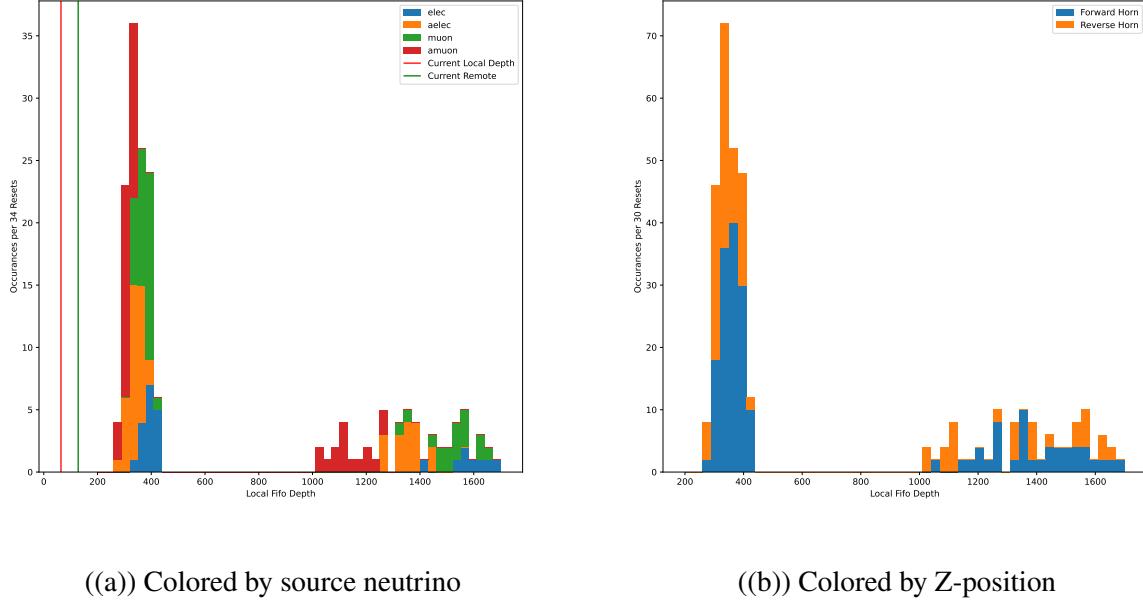


Figure 5.31: Comparison of buffer depths as in incoming prototype and horn current direction from neutrino beam. Plot-(A) indicates that there is not a large average difference between the different neutrino flavors and local FIFO depth. Plot-(B) indicates that the different flux from the two horn currents also do not measurably affect the two different distributions. Plot-(A) however does show a slight difference between ν_e and $\bar{\nu}_\mu$. ν_e has an average local FIFO depth of 394 in the small distribution, where $\bar{\nu}_\mu$ has an average of 313. Most ($\geq 65\%$) of this difference is accounted for the fact that the selected ν_e near-beam ($\theta_z = \pm 2^\circ, 0^\circ$) events deposited more energy, 1894 MeV than the $\bar{\nu}_\mu$ events 1219 MeV, causing more resets. After the energy correction the mean FIFO depths differ by less than one standard deviation.

Freq.	Tile Size	Avg. Local Hits	S. Tot	S. Per.	L. Tot.	L. Per.	T. Tot.	T. Per.
5%	16	772.001	423.293	42.329	166.403	16.640	138.380	13.838
0.5%	16	829.541	449.861	44.986	177.357	17.736	147.346	14.735
5%	64	2184.255	1332.440	133.244	286.929	28.693	227.595	22.759
0.5%	64	2321.148	1400.794	140.079	301.775	30.178	239.087	23.909
5%	140	3712.921	2298.912	229.891	355.037	35.504	262.448	26.245
0.5%	140	3944.215	2416.778	241.678	373.173	37.317	275.614	27.561
5%	256	6231.886	4020.649	402.065	465.629	46.563	354.405	35.440
0.5%	256	6592.433	4209.196	420.920	487.090	48.709	370.695	37.070

Table 5.5: Transaction Data

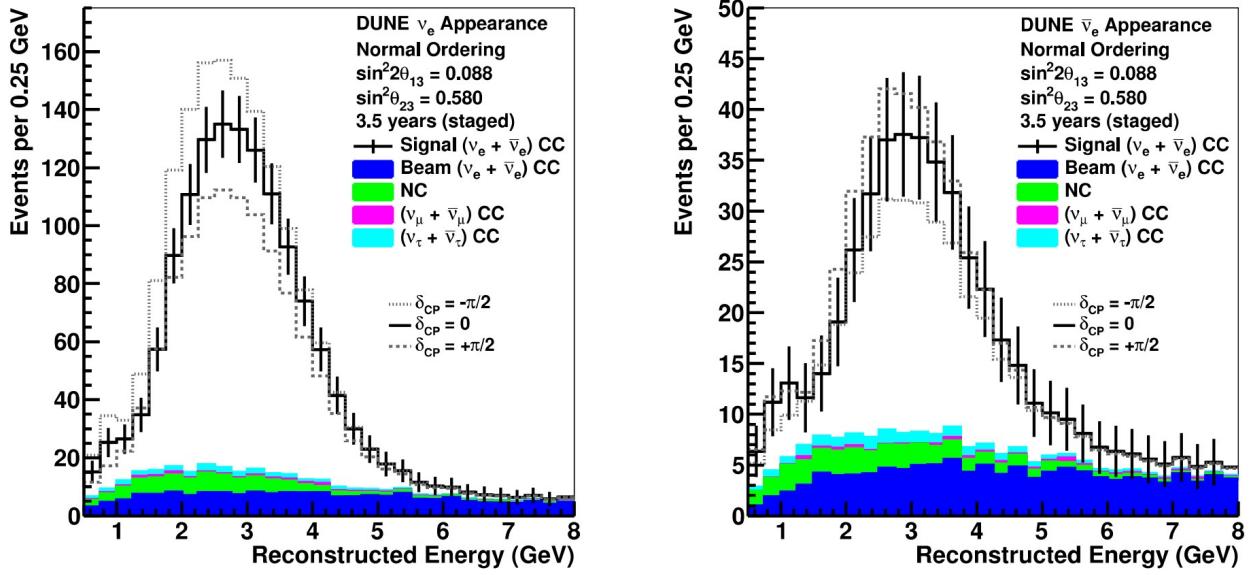


Figure 5.32: Figure is taken from from the DUNE-FD TDR [36]. Images show the ν_e and $\bar{\nu}_e$ appearance spectra respectively. The left image shows the reconstructed energy distribution for the beam running in the forward horn current direction for 3.5 years. The weight of appearance spectra decreases with increasing energy beyond ≈ 8 GeV and has a maximum between 1 and 2 GeV.

Freq.	Tile Size	Local Hits	95-S	99-S	95-L	99-L	95-T	99-T
5%	16	939	320	1014	535	1736	607	1971
0.5%	16	1014	322	975	603	1949	652	2125
5%	64	1200	598	2191	1098	4394	975	4295
0.5%	64	1307	403	1328	970	4298	974	4521
5%	140	1182	852	3486	1455	6558	1343	6309
0.5%	140	1393	440	1464	1327	6616	1382	6757
5%	256	1456	1039	3637	2026	7679	2008	8250
0.5%	256	1670	527	1668	1773	7460	1784	7368

Table 5.6: Buffer Data

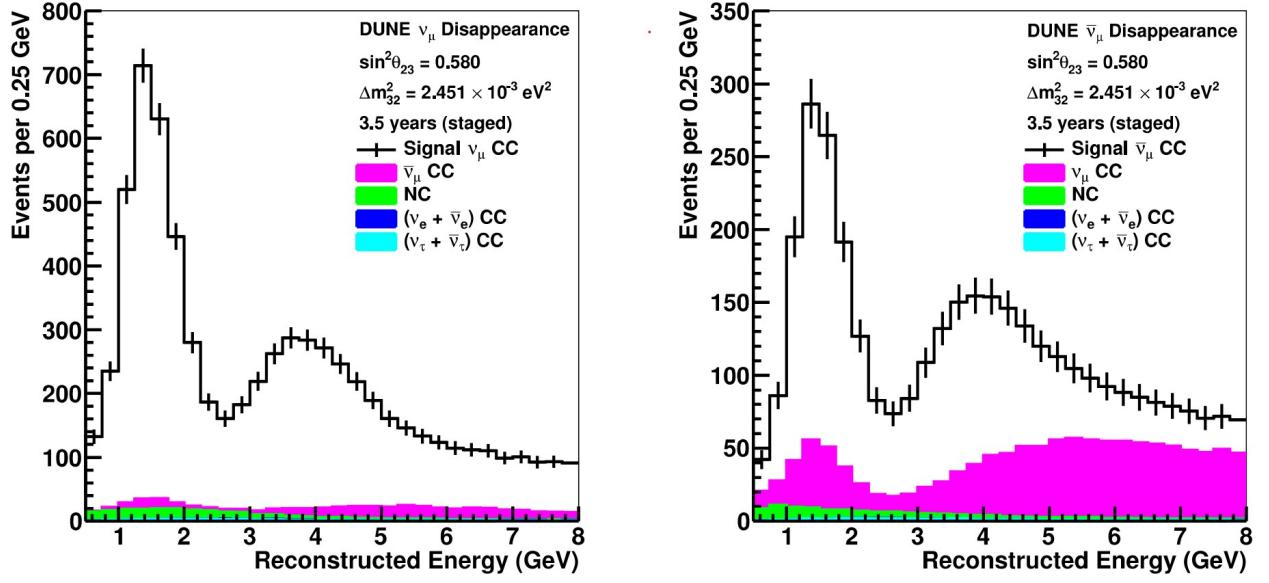


Figure 5.33: Figure is taken directly from the DUNE-FD TDR [36]. Images show the ν_μ and $\bar{\nu}_\mu$ disappearance spectra respectively. The plots assume normal mass ordering and are also staged for 3.5 years (staged) exposure for the beam running in the forward horn current and 7 years in the reverse horn current. The weight of disappearance spectra decreases with increasing energy beyond ≈ 8 GeV and has a maximum between 1 and 2 GeV.

Freq.	Tile Size	Snake Fit	Left Fit	Trunk Fit	Push Fit
5%	16	1.041	1.823	2.082	0
0.5%	16	0.948	1.879	2.039	0
5%	64	1.623	3.176	2.969	0
0.5%	64	1.006	2.514	2.727	0
5%	140	1.966	3.506	3.481	0
0.5%	140	1.021	3.033	3.131	0
5%	256	1.981	3.616	3.913	0
0.5%	256	1.027	3.243	3.336	0

Table 5.7: Transaction Fit Results

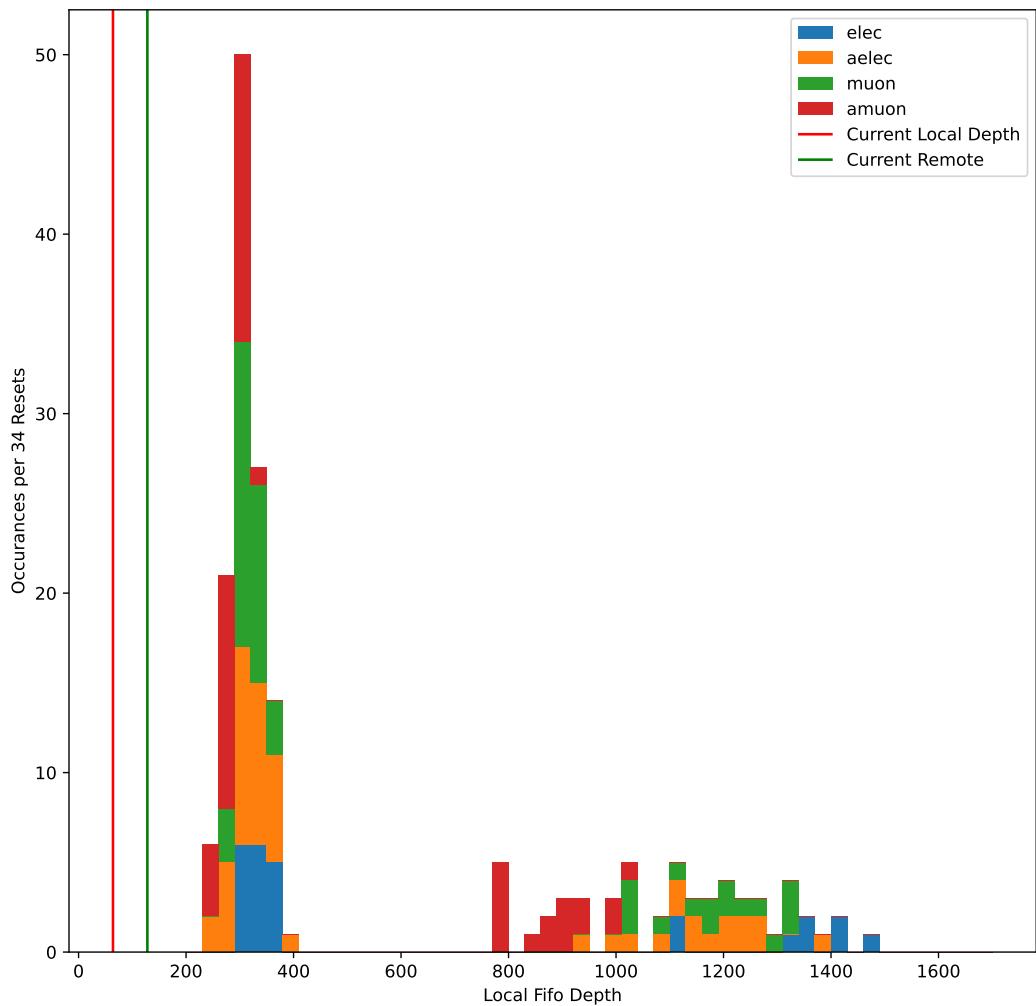


Figure 5.34: Weighted integrals for all neutrino event parameters, with weights drawn from the expected signal curves from Figure 5.6 and Figure 5.6. This plot is similar to Figure 5.5, with the exception that the interaction weights are drawn for the (dis)appearance spectra expected at the DUNE-FD module. The buffer for the oscillation measurements require 394 compared to the uniform interaction energy of 426.

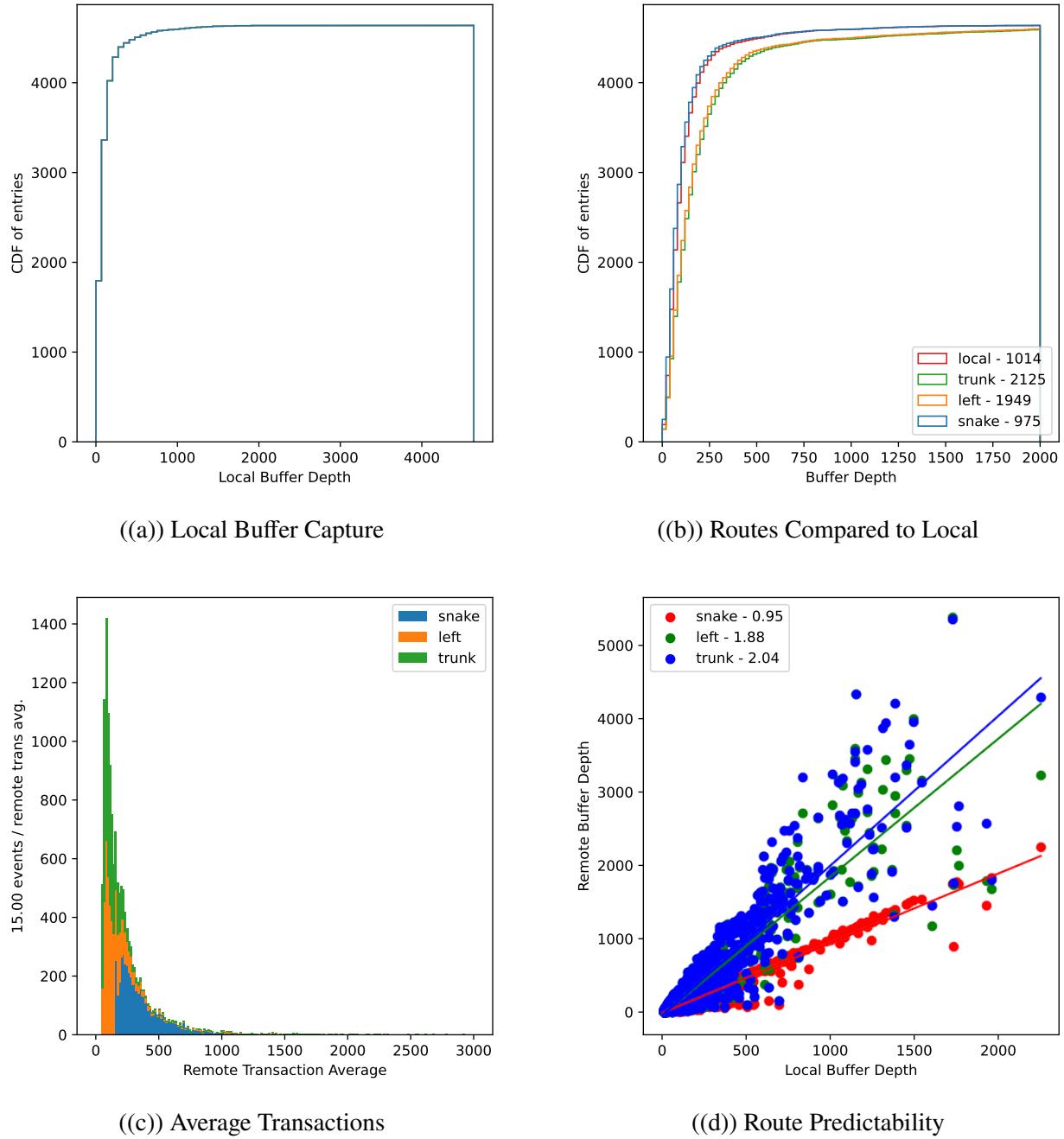


Figure 5.35: The results for a pull-based 4×4 tile with 0.5% frequency drift is shown. Plot-(A) shows the cumulative integral of the number of events that are fully captured as a function of the local buffer depth. Plot-(B) includes the three tested routings against the local buffer depth. The "Snake" routing is the only routing which limits the the remote FIFO depth near the local FIFO depth. Plot-(C) shows the relationship of the average number of transactions for all ASICs in each of the events. Plot-(D) is a scatter plot of the remote depth as a function of the local depth. The legend shows the slope values for linear best fits, which help guide the eye to show how the routes scale differently for large input events.

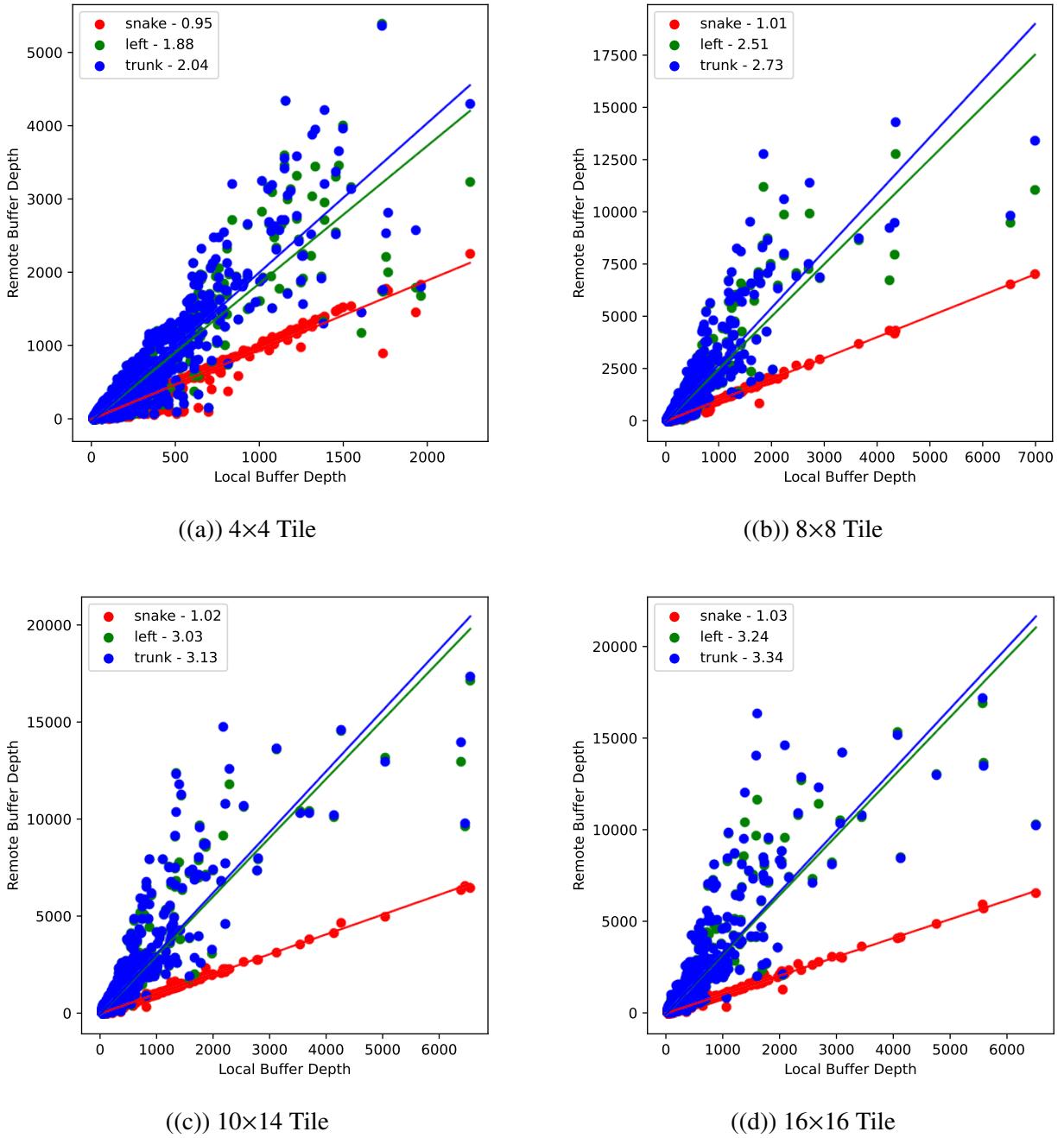


Figure 5.36: A comparison of the remote vs local FIFO depths for different tile sizes is shown. Each plot corresponds to a different tile size with a frequency distribution of 0.5%. Plot-(A) shows that even at small tile sizes (4×4) the remote buffer depths do not predictably scale with the local depths. Both the "Left" and "Trunk" routings slope's increase with the tile size to a maximum value over 3. Only the "Snake" routing maintains a predictable relationship between local and remote depths, as well as unit slope. These data indicate that any future routing for a Q-Pix tile, regardless of size, would need to dynamically route itself into a "Snake" routing in the event of SPF.

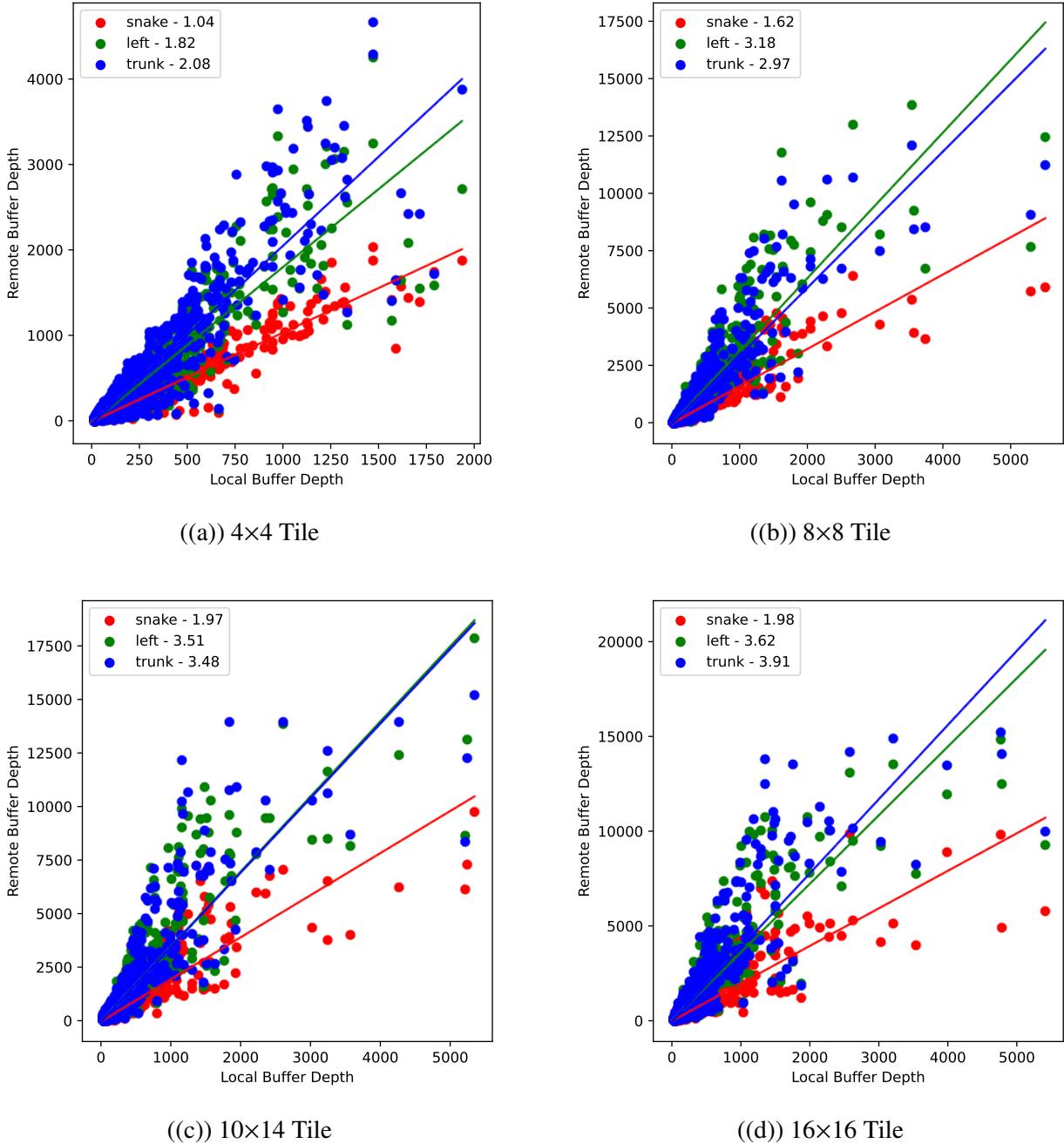


Figure 5.37: A comparison of the remote vs local FIFO depths for different tile sizes is shown. Each plot corresponds to a different tile size with a frequency distribution of 5%. This plot is identical to Figure 5.36, except that the frequency distribution is 5% instead of 0.5%. These results indicate that low frequency variance between neighbor nodes is essential in order to have a predictable remote FIFO depth response based on the snake routing. Not only is the fit poor in Plot-(D) for the 16×16 tile, but the slope has also doubled. This means that, on average, the requirement for the remote FIFO depth would be double that of the requirement on the local FIFO depth.

is configured to each digital node as described in Section 5.1. The flux of beam neutrino events are taken from [86] also using GENIE [87] v2.12.10.

We find that the digital back-end readout permits the ability to fully capture 99% events from beam neutrino events up to 10 GeV provided the local FIFO depth is at least 426. Each ASIC would be able to record all resets from these neutrino events regardless of incident neutrino momentum direction if the local FIFO depth is 1670. These results present an expected upper-bound of the required local and remote FIFO depths for the digital ASIC, since most electrons of reconstructed energy for neutrino oscillations (See Chapter 5 from [37]) expected to be less than 4 GeV, while the analysis presented here are for events up to 10 GeV.

The current Q-Pix digital prototype allows for dynamic and configurable routing. We find that the only stable relationship between the local FIFO depth and the remote FIFO depth occurs for the "Snake" based routing, where the required depths are approximately equal. Additionally, the relationship between these FIFO depths are independent of tile size, which imply that tiles of any size should reconfigure itself to always have an effective "Snake" routing in the event of SPF.

We also find no difference in the ability of a "push" architecture to better alleviate neutrino events than the current "pull" based architecture. The reason for this is due to the quick arrival time of neutrino resets compared to the average packet transaction time.

In order for a "push" architecture to be able to reduce both the remote and local FIFO depth requirements the average packet transaction time would have to be small compared to the average RTD on each node. The total decrease of the packet transaction time will likely have to be an order of magnitude, or more, according to Figure 5.8 The distribution of RTDs for the example scatter event clearly indicate that most of the resets come within 1 μ s of each other. Since the current packet transaction time is, on average $\approx 50 \mu$ s, for the push architecture to transfer packets more quickly than they arrive the packet transaction time would have to decrease by about a factor of 50.

A combination of changes could make this possible: a faster local oscillator, a different communication protocol, and zero-suppression on some packet data. Future designers will have to ask themselves if a redesign of the digital clock, the packet communication protocol, and/or the FSM of the digital ASIC is easier than increasing two FIFO depths. It is the humble opinion of the author of this work that it is not.

Finally, we remark how much the digital ASIC is capable of, despite it's seemingly simple design 4.2. In the spirit of the Q-Pix's principle of least action, we assert that the digital ASIC should be also

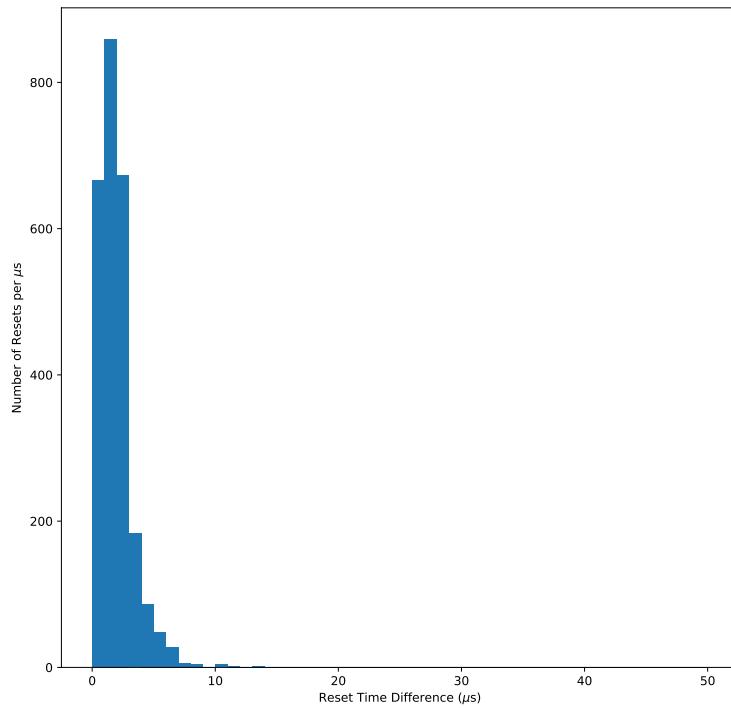


Figure 5.38: A calculation of all of the Reset Time Differences (RTDs) for the example scatter event shown in Figure 5.21. A packet transaction takes $\approx 50 \mu\text{s}$ to occur. The distribution of RTDs for a scatter event indicate that most of the resets occur separated by less than 1 μs .

be as simple as possible while relaying all data required for the application.

Chapter 6

SUMMARY AND OUTLOOK

6.1 Conclusions

The results presented in this work provide the first tests and verification of the digital back-end for novel pixel readout technology targeted at liquid Argon Time-Project-Chambers.

The first Q-Pix analog prototype using Off-The-Shelf analog components has been built and is currently taking measurements. This prototype promises to provide gaseous Argon diffusion measurements, which will likely be the first true physics measurement using a Q-Pix based readout.

We have built and verified the first digital prototype boards which have verified communication reliability to protect against potential data loss. We developed a frequency calibration method for remote nodes to demonstrate Q-Pix’s ability to have independent oscillators. We used this prototype and verified the ability to reconstruct remote oscillator frequencies with a precision more than an order of magnitude required ($0.1 \text{ ppm} < 1 \text{ ppm}$). These results are verified between two different interrogation frequencies.

We developed multiple simulations to model the detector’s response to long (1000 second) run time exposure of radiogenic backgrounds as well as tested the ability to readout beam neutrino events at LBNF. Our simulations show that the current ASIC’s local (64) and remote (128) FIFO depths of the digital ASIC prototype are too small to GeV scale neutrino events in a DUNE-FD. We estimate that the local FIFO depth should be at least be able to record 426 unique resets in order to fully capture 99% of neutrino events with energy up to 10 GeV. These results are modified to a required 394 when accounted for expected (dis)appearance spectra given in [36] This result provides the first limit on the memory required for a Q-Pix ASIC, should it be used in a DUNE-FD module to measure neutrino oscillations.

To test the remote FIFO depths and local oscillator frequency requirements we developed the first simulation to model the Q-Pix digital back-end response to physical events within a DUNE-FD APA. We find that the distribution of the ASIC frequency needs to be $\approx 0.5\%$ in order to maintain obtain reliable remote FIFO depths with the current readout protocol. These results also indicate that the only reliable routing methodology is the "Snake" routing (Section 5.3), which is shown

to be independent of both tile size and digital architecture (See Table 5.1). The routing ("Snake") provides a unitary relationship between the local and remote FIFO depth requirements.

The Future of Q-Pix

The Q-Pix design is a novel readout technology. However, "novelty does not confer automatically benefit", David Nygren. The full Q-Pix validation still awaits key results to demonstrate its capabilities in a DUNE-FD module. Namely, Q-Pix still needs to test both the analog and digital prototypes at cold liquid Argon temperatures.

The front-end requires a reliable replenishment circuit as well as low leakage current (≈ 100 aA or less to be below radiogenic backgrounds). Also, when known, the timing response of the replenishment circuit should be applied to the RTD results presented in this work. Knowledge of the timing response of the analog front-end can be combined with the neutrino simulation events shown here to allow for accurate event reconstruction. These reconstructed events will permit an analysis to estimate of Q-Pix's ability to perform neutrino oscillation measurements.

Q-Pix's First and Second Digital Prototypes

The work presented here can accurately be viewed both as a means to understand the Q-Pix's first digital ASIC and as a guide toward the second digital design. The key result of this work indicates that the local and remote FIFO depths of the second prototype should both be increased to at or above 394 to capture 99% of neutrino oscillation interactions. The reason the first prototype did not incorporate these larger buff sizes was due to fabrication limitations of the ASIC. If oscillator tests of the first prototype indicate that the mean drift between neighbor ASICs is reliably under 0.5%, then the local oscillator need not be changed either. All other underlying logic, with perhaps the exception of FWFT FIFOs, have been verified in the first digital prototype. These tests need only be repeated on the first prototype ASIC.

Eventually the Q-Pix front and back-end ASICs will likely be combined into a single chip. Still, the motivation provided by the results presented here for the second prototype (applied only to the digital portion) remain unchanged.

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Appendix A

NEUTRINO INTERACTION INTEGRAL DATA

lepton Pdg	Horn Current Direction	Z-Pos	Theta	95% Capture	99% Capture
12	forward	10	0	262	398
12	forward	80	0	270	402
12	forward	180	0	262	402
12	forward	280	0	254	378
12	forward	350	0	242	378
12	forward	10	2	266	390
12	forward	80	2	270	422
12	forward	180	2	270	414
12	forward	280	2	258	378
12	forward	350	2	238	398
12	forward	10	-2	266	426
12	forward	80	-2	266	426
12	forward	180	-2	266	410
12	forward	280	-2	258	398
12	forward	350	-2	246	366
12	forward	10	90	946	1526
12	forward	80	90	950	1554
12	forward	180	90	922	1638
12	forward	280	90	798	1426
12	forward	350	90	238	326
12	forward	10	-90	274	390
12	forward	80	-90	874	1570
12	forward	180	-90	954	1670
12	forward	280	-90	918	1586
12	forward	350	-90	906	1666

-12	forward	10	0	238	362
-12	forward	80	0	246	370
-12	forward	180	0	234	358
-12	forward	280	0	230	370
-12	forward	350	0	214	334
-12	forward	10	2	230	358
-12	forward	80	2	238	382
-12	forward	180	2	234	350
-12	forward	280	2	226	350
-12	forward	350	2	214	330
-12	forward	10	-2	234	382
-12	forward	80	-2	238	358
-12	forward	180	-2	238	358
-12	forward	280	-2	226	362
-12	forward	350	-2	214	334
-12	forward	10	90	710	1378
-12	forward	80	90	686	1274
-12	forward	180	90	666	1350
-12	forward	280	90	582	1250
-12	forward	350	90	206	306
-12	forward	10	-90	238	354
-12	forward	80	-90	634	1358
-12	forward	180	-90	670	1358
-12	forward	280	-90	702	1454
-12	forward	350	-90	666	1354
-12	reverse	10	0	222	342
-12	reverse	80	0	226	334
-12	reverse	180	0	226	326
-12	reverse	280	0	218	322
-12	reverse	350	0	202	306
-12	reverse	10	2	226	322
-12	reverse	80	2	222	330

-12	reverse	180	2	222	326
-12	reverse	280	2	214	318
-12	reverse	350	2	198	290
-12	reverse	10	-2	218	326
-12	reverse	80	-2	226	342
-12	reverse	180	-2	218	318
-12	reverse	280	-2	214	322
-12	reverse	350	-2	202	306
-12	reverse	10	90	710	1374
-12	reverse	80	90	674	1378
-12	reverse	180	90	642	1434
-12	reverse	280	90	578	1266
-12	reverse	350	90	194	286
-12	reverse	10	-90	230	330
-12	reverse	80	-90	590	1314
-12	reverse	180	-90	622	1334
-12	reverse	280	-90	674	1398
-12	reverse	350	-90	638	1310
14	forward	10	0	258	370
14	forward	80	0	258	386
14	forward	180	0	254	366
14	forward	280	0	246	358
14	forward	350	0	238	338
14	forward	10	2	258	382
14	forward	80	2	258	398
14	forward	180	2	258	394
14	forward	280	2	246	334
14	forward	350	2	226	338
14	forward	10	-2	254	378
14	forward	80	-2	262	386
14	forward	180	-2	254	354
14	forward	280	-2	238	346

14	forward	350	-2	230	326
14	forward	10	90	786	1534
14	forward	80	90	798	1470
14	forward	180	90	754	1454
14	forward	280	90	682	1338
14	forward	350	90	234	322
14	forward	10	-90	258	382
14	forward	80	-90	726	1494
14	forward	180	-90	778	1490
14	forward	280	-90	766	1366
14	forward	350	-90	786	1482
14	reverse	10	0	270	382
14	reverse	80	0	278	406
14	reverse	180	0	266	394
14	reverse	280	0	258	378
14	reverse	350	0	242	366
14	reverse	10	2	274	402
14	reverse	80	2	282	390
14	reverse	180	2	266	398
14	reverse	280	2	262	374
14	reverse	350	2	242	374
14	reverse	10	-2	262	406
14	reverse	80	-2	274	418
14	reverse	180	-2	262	378
14	reverse	280	-2	258	394
14	reverse	350	-2	238	354
14	reverse	10	90	942	1570
14	reverse	80	90	898	1618
14	reverse	180	90	842	1550
14	reverse	280	90	822	1522
14	reverse	350	90	234	334
14	reverse	10	-90	270	406

14	reverse	80	-90	838	1526
14	reverse	180	-90	898	1610
14	reverse	280	-90	914	1562
14	reverse	350	-90	894	1642
-14	forward	10	0	222	326
-14	forward	80	0	226	334
-14	forward	180	0	214	322
-14	forward	280	0	210	314
-14	forward	350	0	194	302
-14	forward	10	2	218	342
-14	forward	80	2	222	330
-14	forward	180	2	214	322
-14	forward	280	2	210	314
-14	forward	350	2	198	290
-14	forward	10	-2	218	322
-14	forward	80	-2	222	322
-14	forward	180	-2	214	310
-14	forward	280	-2	206	314
-14	forward	350	-2	202	298
-14	forward	10	90	578	1274
-14	forward	80	90	578	1254
-14	forward	180	90	522	1186
-14	forward	280	90	490	1046
-14	forward	350	90	182	270
-14	forward	10	-90	218	314
-14	forward	80	-90	546	1214
-14	forward	180	-90	570	1150
-14	forward	280	-90	538	1190
-14	forward	350	-90	550	1238
-14	reverse	10	0	218	338
-14	reverse	80	0	218	326
-14	reverse	180	0	210	318

-14	reverse	280	0	206	306
-14	reverse	350	0	194	294
-14	reverse	10	2	210	318
-14	reverse	80	2	210	338
-14	reverse	180	2	218	326
-14	reverse	280	2	206	302
-14	reverse	350	2	194	278
-14	reverse	10	-2	218	310
-14	reverse	80	-2	218	334
-14	reverse	180	-2	214	314
-14	reverse	280	-2	206	306
-14	reverse	350	-2	194	290
-14	reverse	10	90	514	1098
-14	reverse	80	90	486	1082
-14	reverse	180	90	498	1102
-14	reverse	280	90	446	1030
-14	reverse	350	90	174	266
-14	reverse	10	-90	218	326
-14	reverse	80	-90	486	1014
-14	reverse	180	-90	494	1110
-14	reverse	280	-90	494	1122
-14	reverse	350	-90	506	1118
12	reverse	10	0	286	426
12	reverse	80	0	290	426
12	reverse	180	0	286	422
12	reverse	280	0	278	426
12	reverse	350	0	262	410
12	reverse	10	2	282	422
12	reverse	80	2	286	430
12	reverse	180	2	286	454
12	reverse	280	2	278	426
12	reverse	350	2	250	422

12	reverse	10	-2	270	434
12	reverse	80	-2	294	446
12	reverse	180	-2	286	446
12	reverse	280	-2	274	426
12	reverse	350	-2	258	382
12	reverse	10	90	1126	1774
12	reverse	80	90	1098	1630
12	reverse	180	90	1014	1694
12	reverse	280	90	910	1498
12	reverse	350	90	246	362
12	reverse	10	-90	286	406
12	reverse	80	-90	970	1658
12	reverse	180	-90	1114	1686
12	reverse	280	-90	1022	1770
12	reverse	350	-90	1014	1622

Table A.1: APA Integral Data. Integrals are performed on histograms of bin widths of two.

Appendix B

Q-PIX ANALOG ASIC FIRST PROTOTYPE

QPIX Layout: Integrator + Amplifier + Comparator

Size: 350um x 90 um

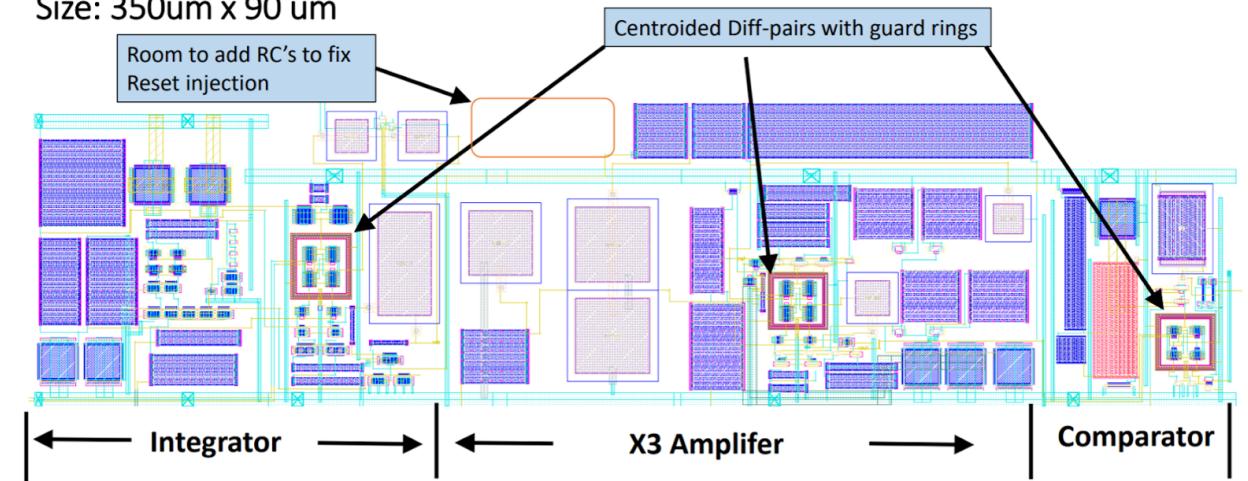


Figure B.1: Full Schematic of the upcoming Q-Pix analog front-end ASIC.