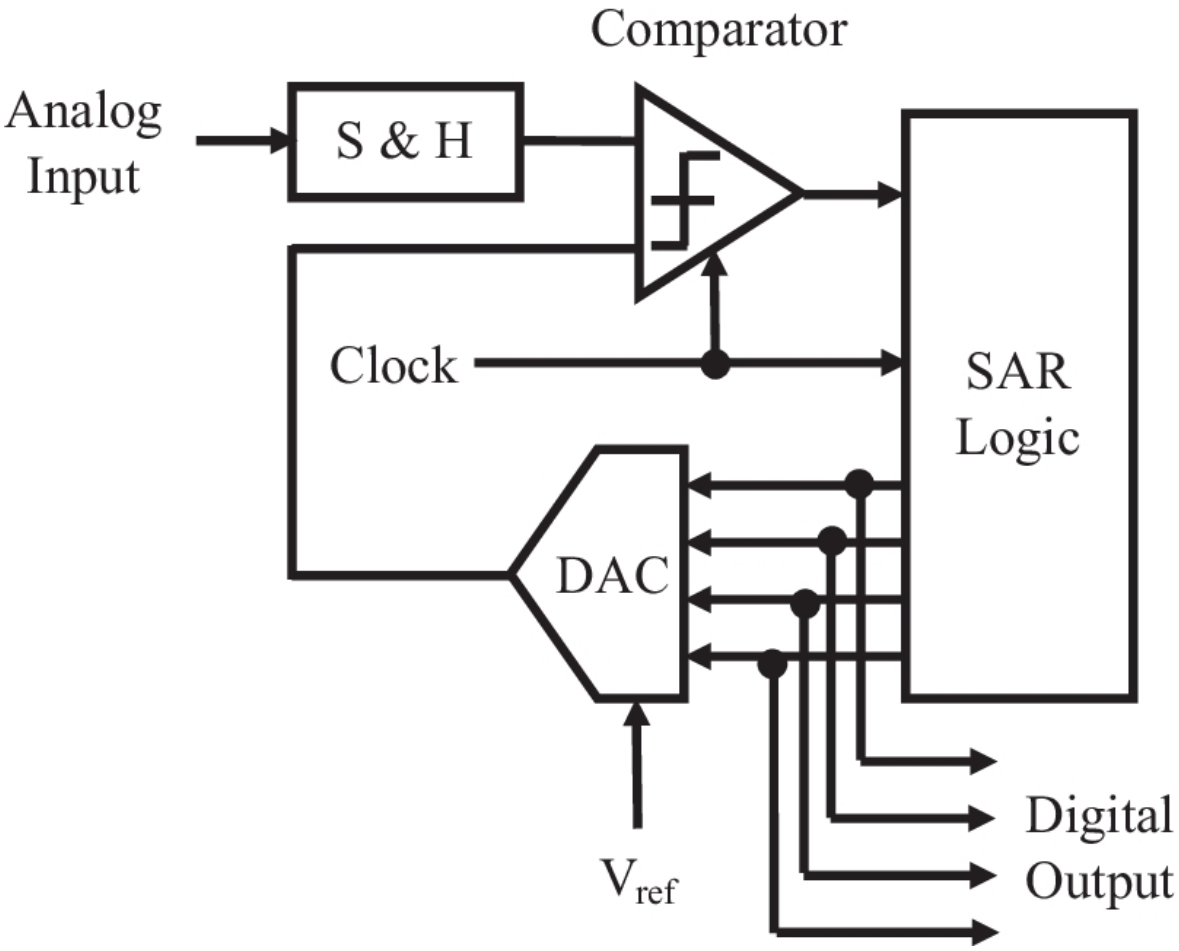
SAR ADC

DESIGN & VERIFICATION



BY: Khaled Ahmed Hamed

ADC Winter 2025 Training

Under supervision of **Dr. Hesham Omran**

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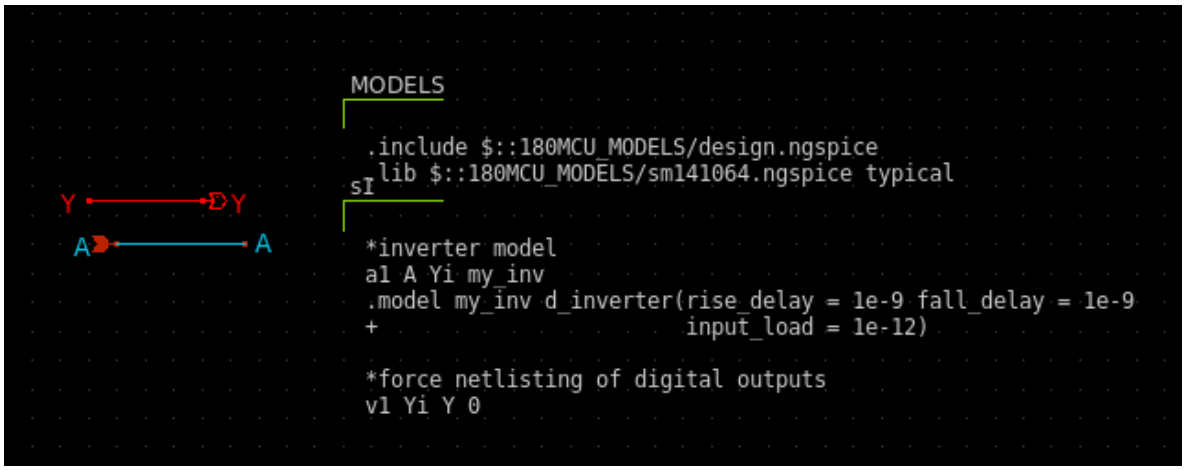

Figure 1: Inverter Circuit

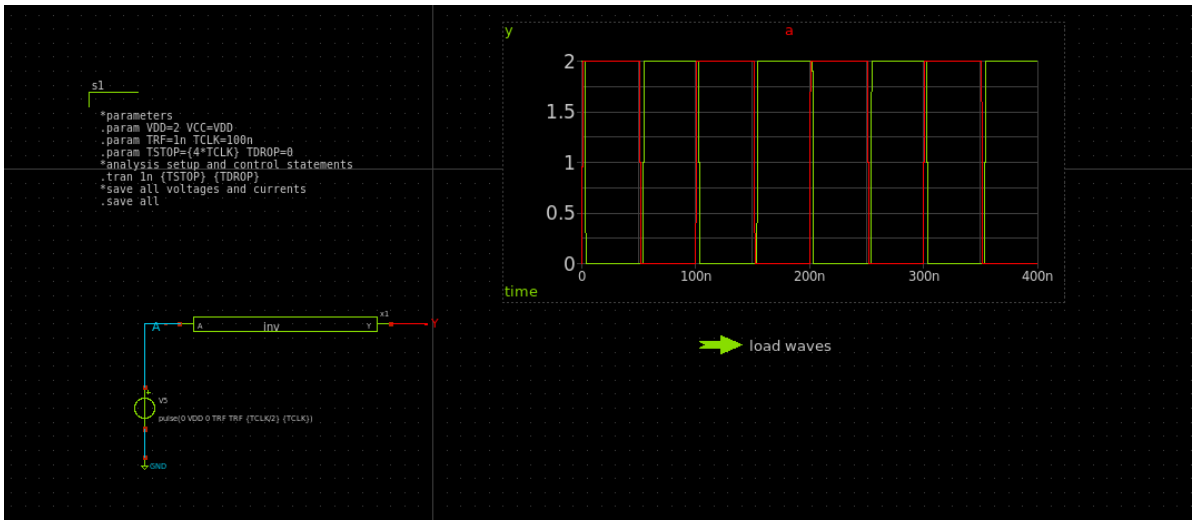

Figure 2: Inverter Testbench

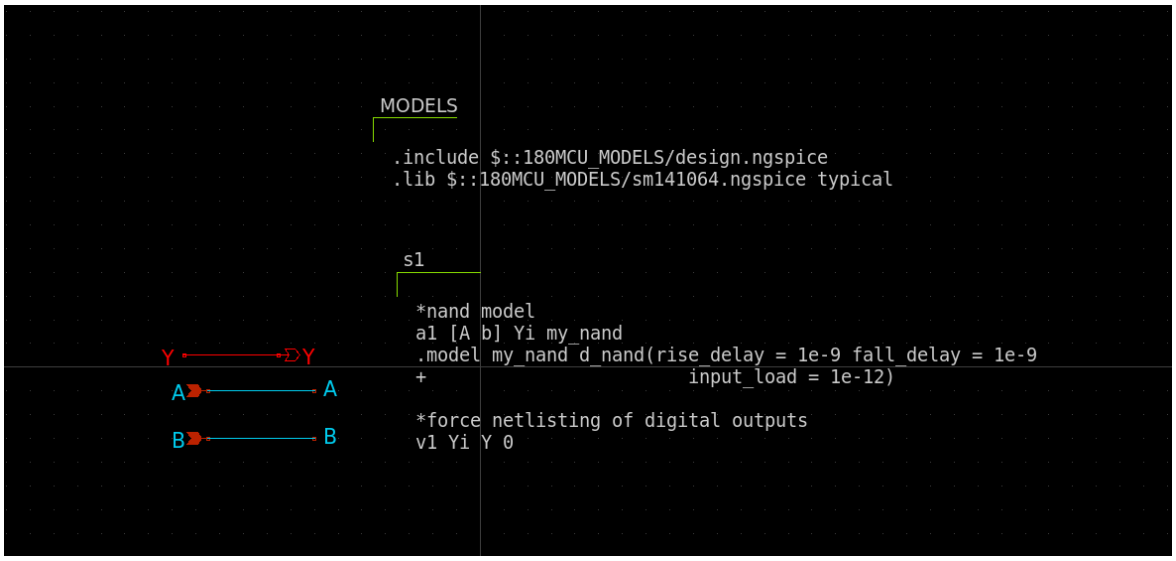

Figure 3: NAND Circuit

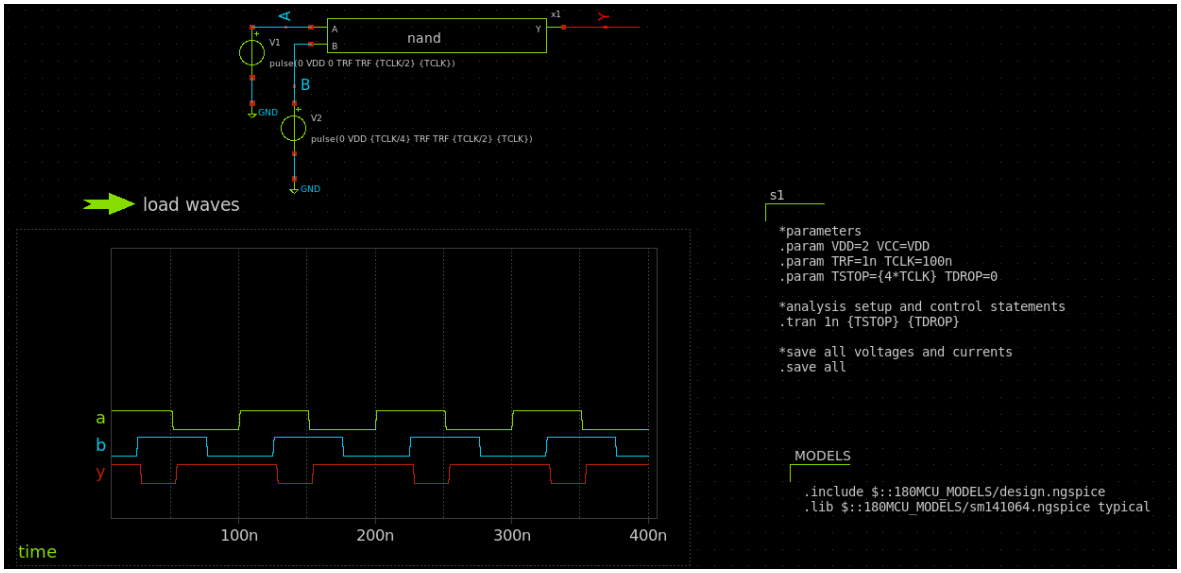

Figure 4: NAND Testbench

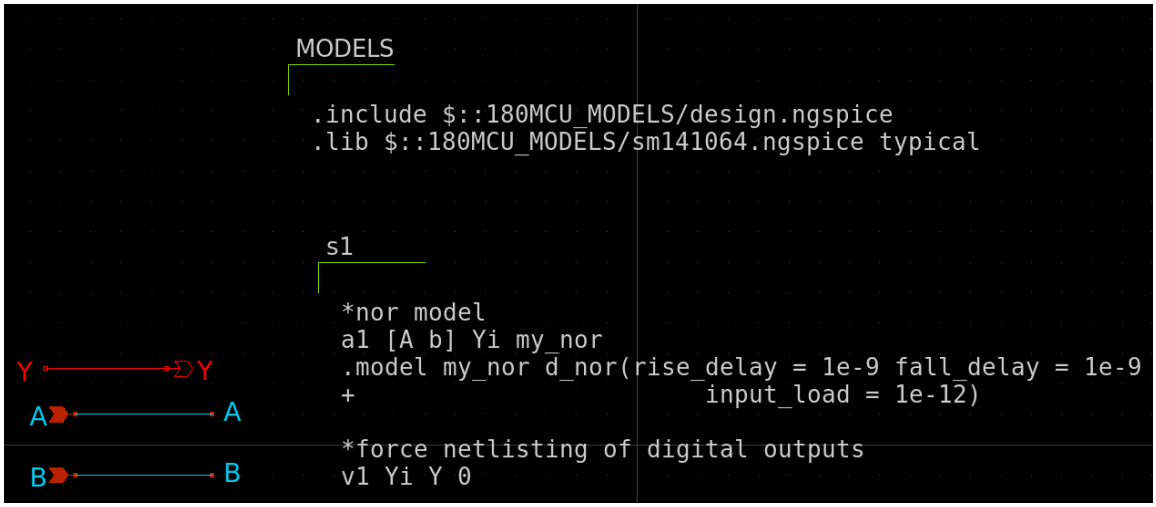

Figure 5: NOR Circuit

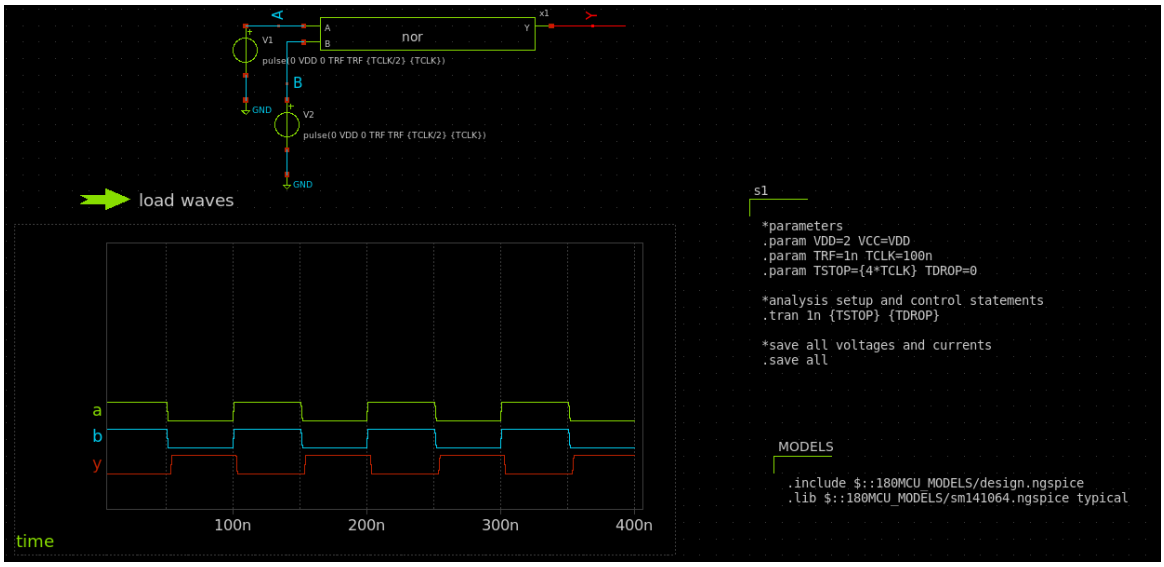

Figure 6: NOR Testbench

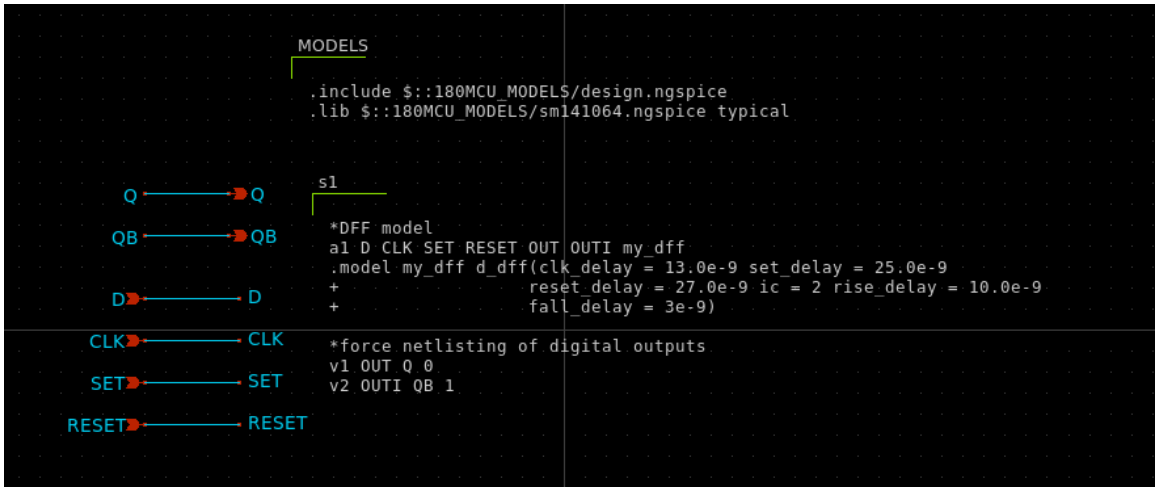

Figure 7: D Flip Flop Circuit

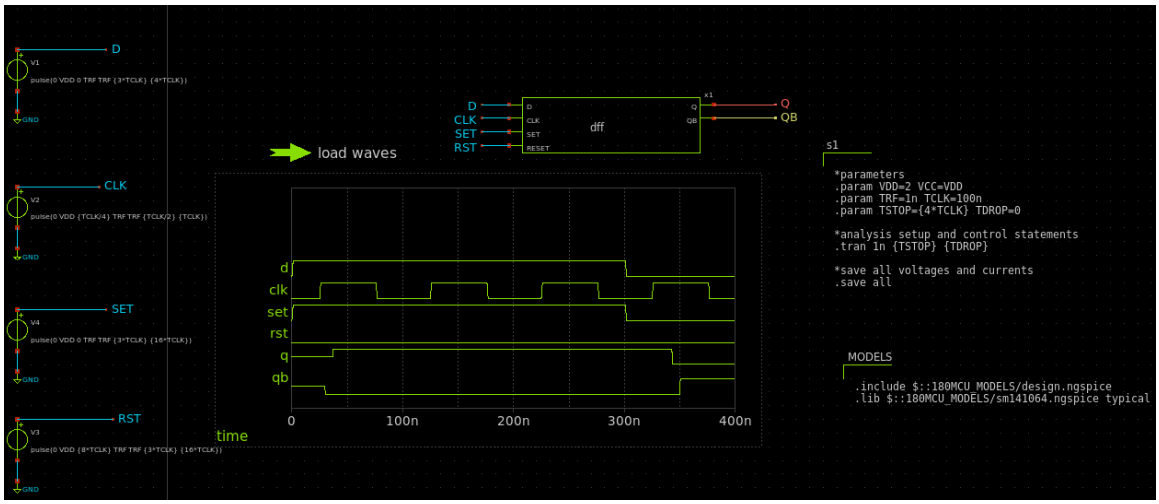

Figure 8: D Flip Flop Testbench

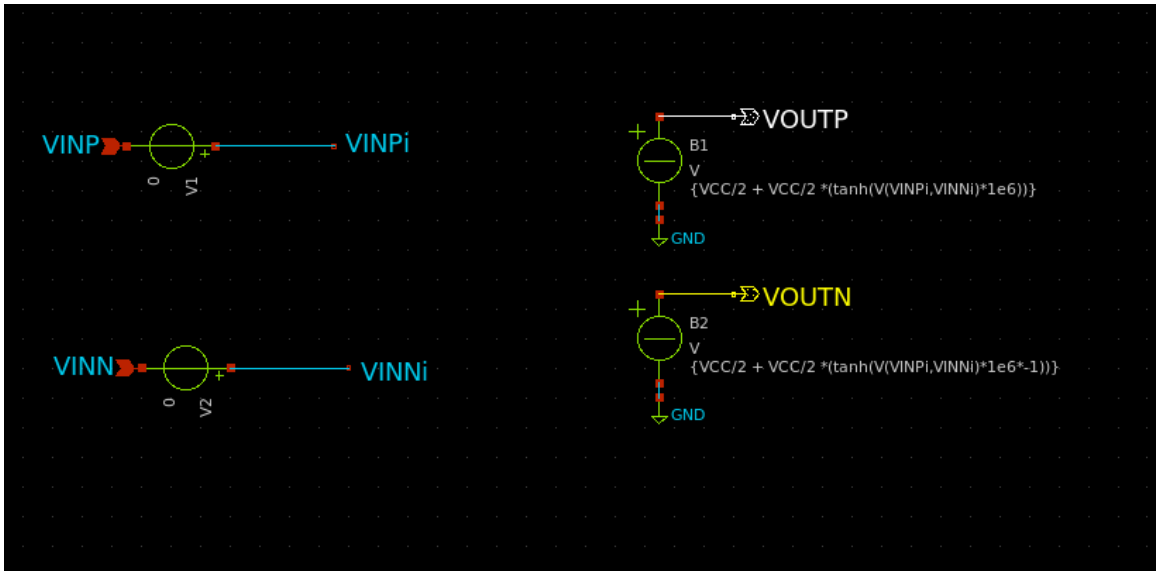

Figure 9: Comparator Circuit

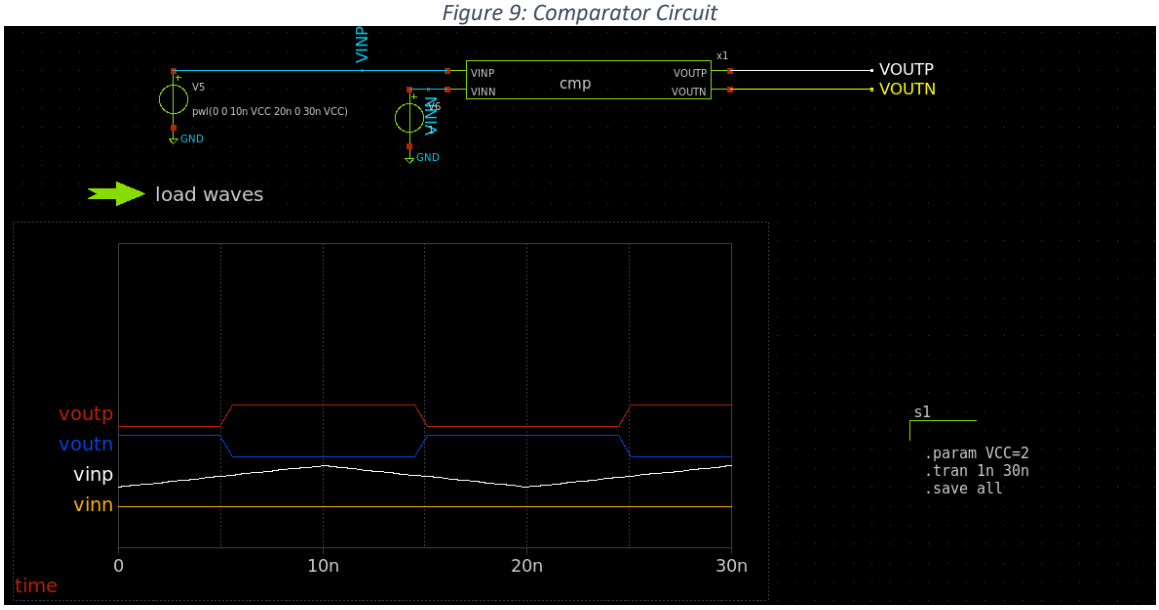

Figure 10: : Comparator Testbench

2: SAR Logic

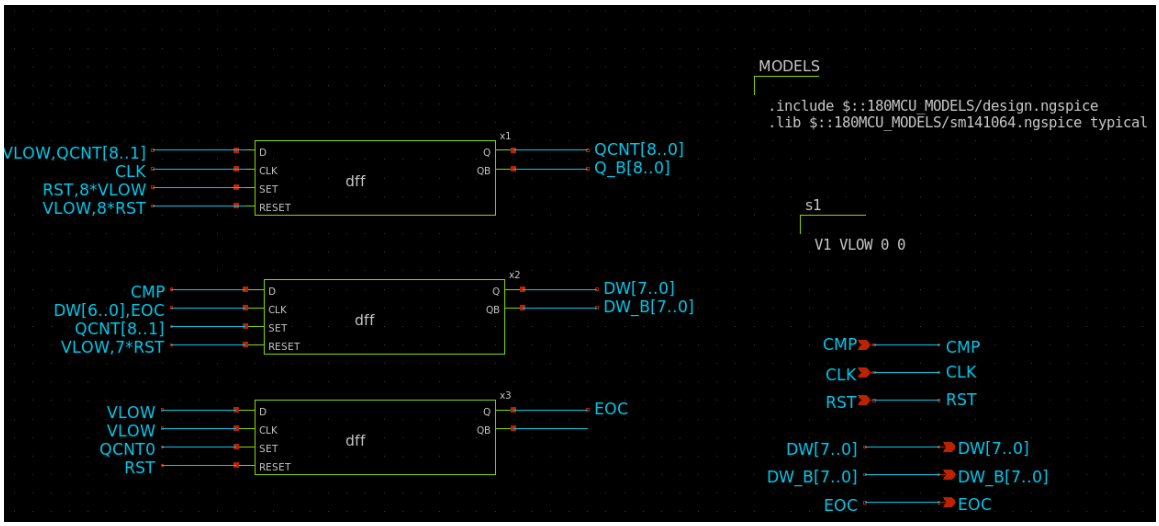

Figure 11: SAR Logic Circuit

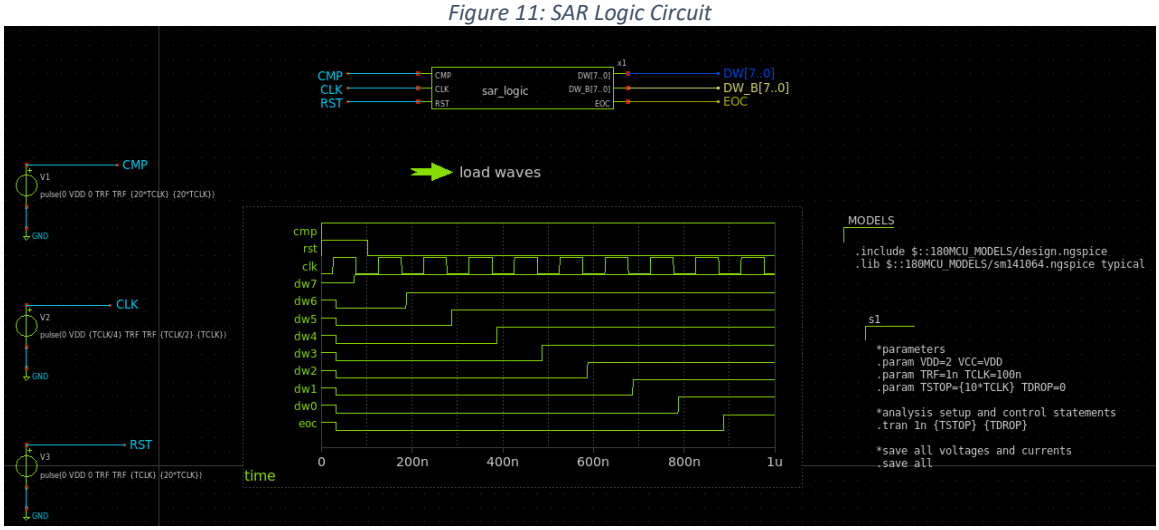

Figure 12: SAR testbench when CMP all ones

Cycle	DW<7>	DW<6>	DW<5>	DW<4>	DW<3>	DW<2>	DW<1>	DW<0>	CMP
1 (reset)	1	0	0	0	0	0	0	0	
2	1	0	0	0	0	0	0	0	1
3	1	1	0	0	0	0	0	0	1
4	1	1	1	0	0	0	0	0	1
5	1	1	1	1	0	0	0	0	1
6	1	1	1	1	1	0	0	0	1
7	1	1	1	1	1	1	0	0	1
8	1	1	1	1	1	1	1	0	1
9	1	1	1	1	1	1	1	1	1
10	1	1	1	1	1	1	1	1	

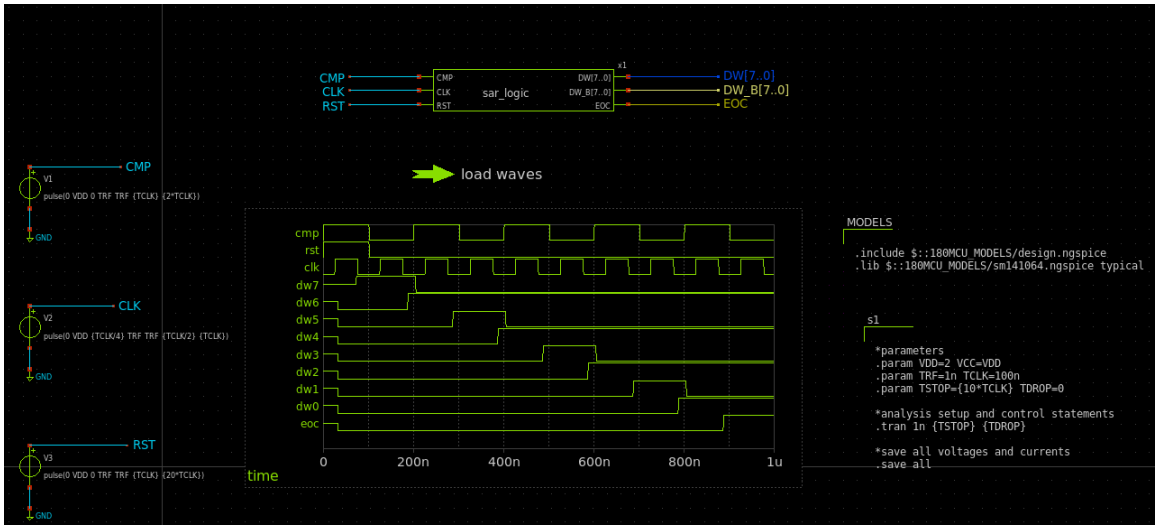

Figure 13: SAR testbench when CMP alternating (0 VDD)

Cycle	DW<7>	DW<6>	DW<5>	DW<4>	DW<3>	DW<2>	DW<1>	DW<0>	CMP
1 (reset)	1	0	0	0	0	0	0	0	
2	1	0	0	0	0	0	0	0	1
3	1	1	0	0	0	0	0	0	0
4	1	0	1	0	0	0	0	0	1
5	1	0	1	1	0	0	0	0	0
6	1	0	1	0	1	0	0	0	1
7	1	0	1	0	1	1	0	0	0
8	1	0	1	0	1	0	1	0	1
9	1	0	1	0	1	0	1	1	0
10	1	0	1	0	1	0	1	0	

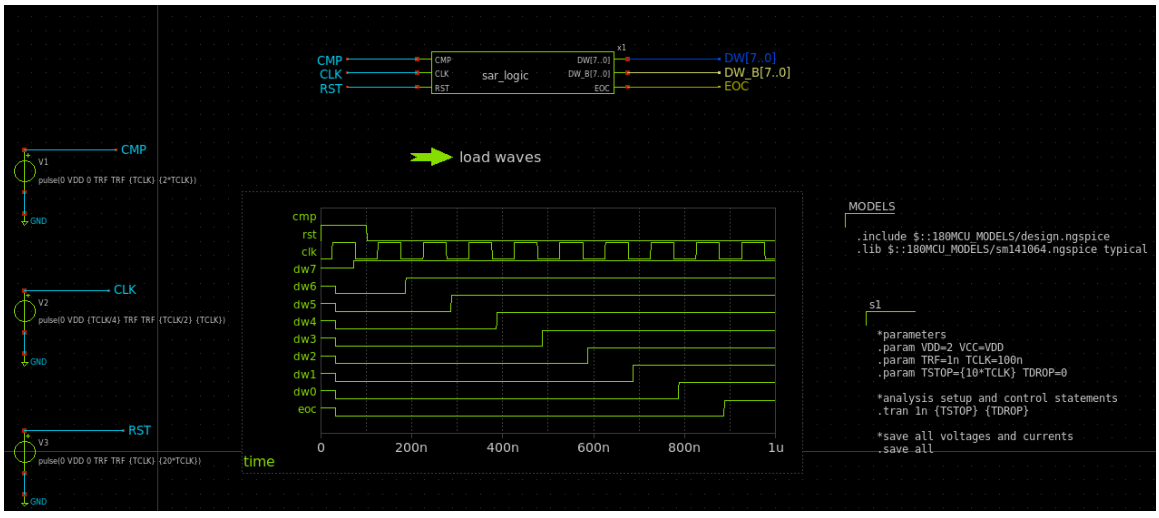

Figure 14: SAR testbench when CMP all zeros

Cycle	DW<7>	DW<6>	DW<5>	DW<4>	DW<3>	DW<2>	DW<1>	DW<0>	CMP
1 (reset)	1	0	0	0	0	0	0	0	
2	1	0	0	0	0	0	0	0	0
3	0	1	0	0	0	0	0	0	0
4	0	0	1	0	0	0	0	0	0
5	0	0	0	1	0	0	0	0	0
6	0	0	0	0	1	0	0	0	0
7	0	0	0	0	0	1	0	0	0
8	0	0	0	0	0	0	1	0	0
9	0	0	0	0	0	0	0	1	0
10	0	0	0	0	0	0	0	0	

Explanation:

The Successive Approximation Register (SAR) algorithm begins by setting the most significant bit (MSB) to 1 and comparing the Digital-to-Analog Converter (DAC) output with the input voltage. If the input voltage is higher than the DAC output, the bit remains 1; otherwise, it is reset to 0. This process continues iteratively for each subsequent bit, refining the digital approximation step by step until reaching the least significant bit (LSB).

At each stage, the algorithm determines whether to retain or clear the bit based on a comparison between the DAC output and the input voltage. It starts by testing the midscale value—if the input voltage exceeds it, the MSB remains 1; otherwise, it is set to 0. The algorithm then proceeds through a structured sequence, evaluating progressively smaller bit positions, such as (x1xx xxxx), (xx1x xxxx), and so forth, until the full digital representation of the input voltage is achieved. This method ensures an accurate digital approximation through successive comparisons.

Part 3: Transmission Gate

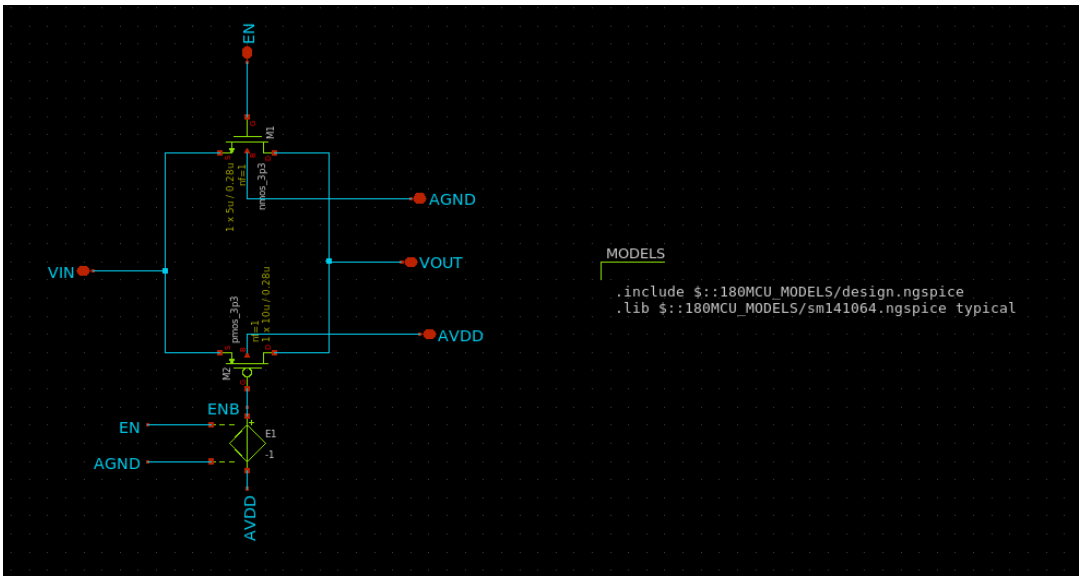

Figure 15: Transmission Gate Circuit

Part 4: Bottom Plate

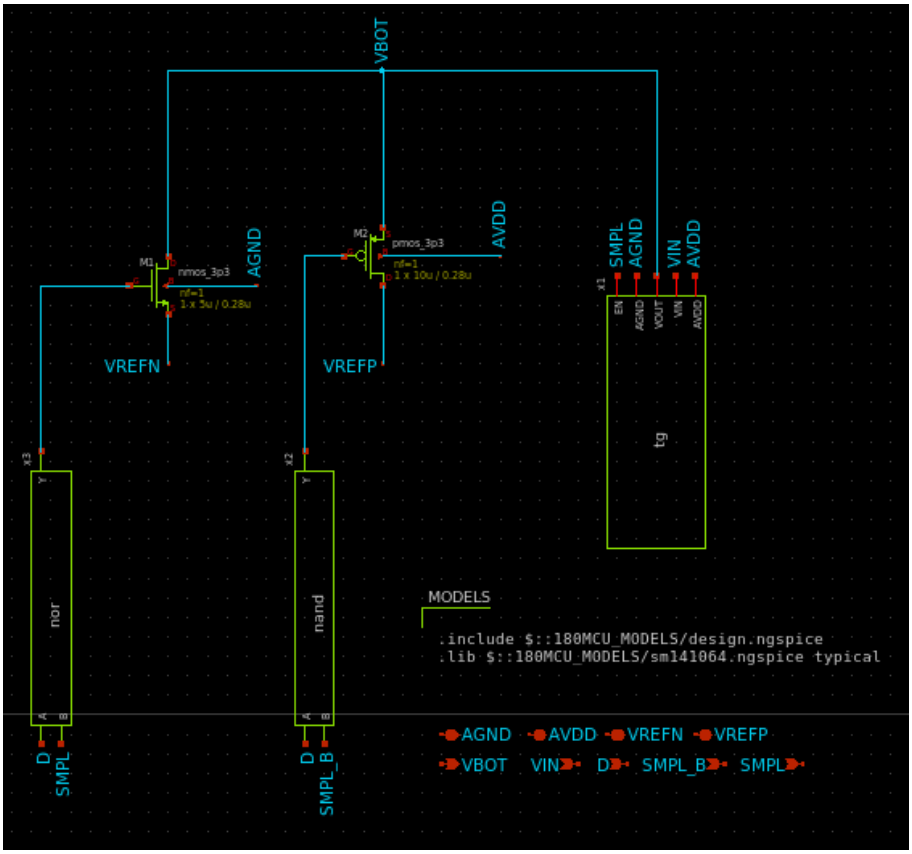

Figure 16: Bottom Plate Circuit

Part 5: SAR ADC Design

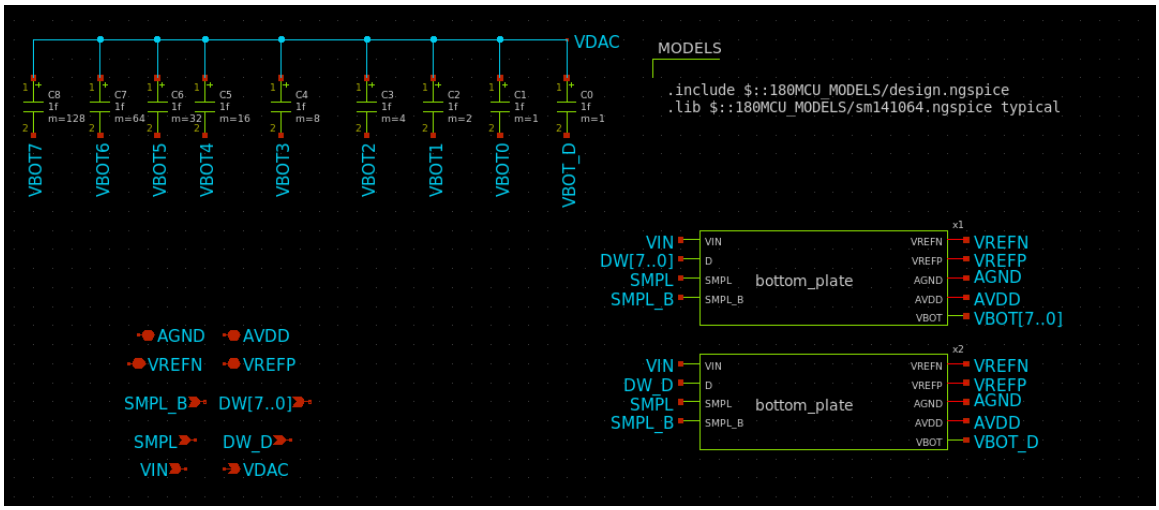

Figure 17: Cap DAC Circuit

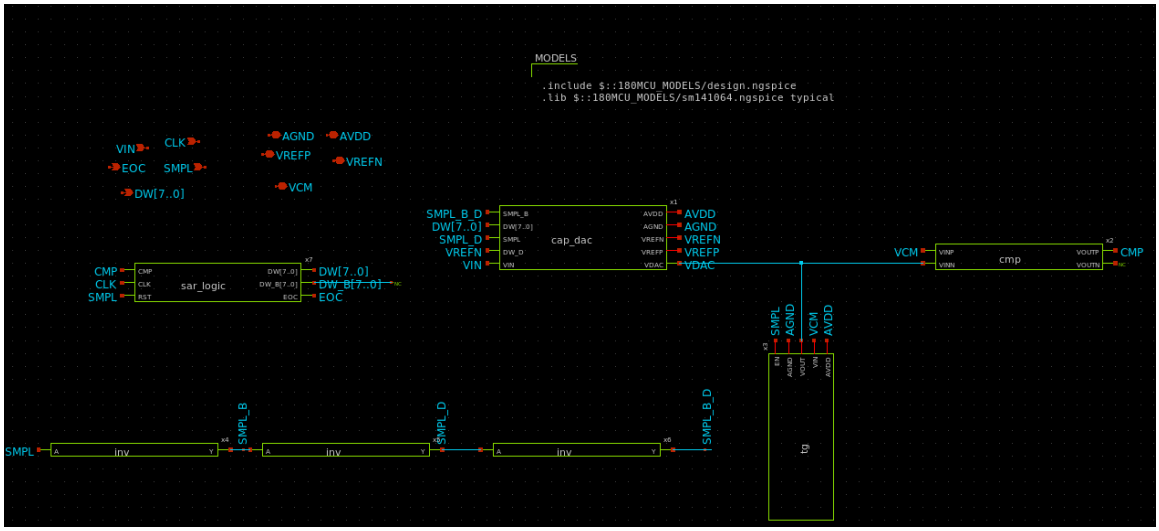

Figure 18: SAR ADC Circuit

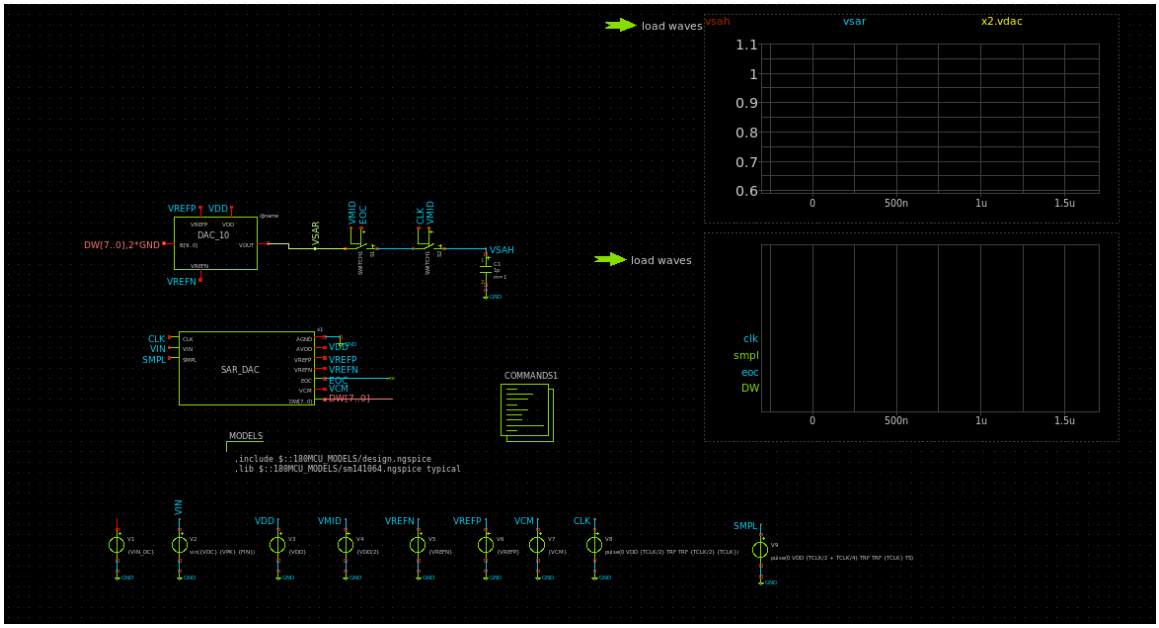

Figure 19: SAR ADC Final Testbench

Part 6: DC Functional Test

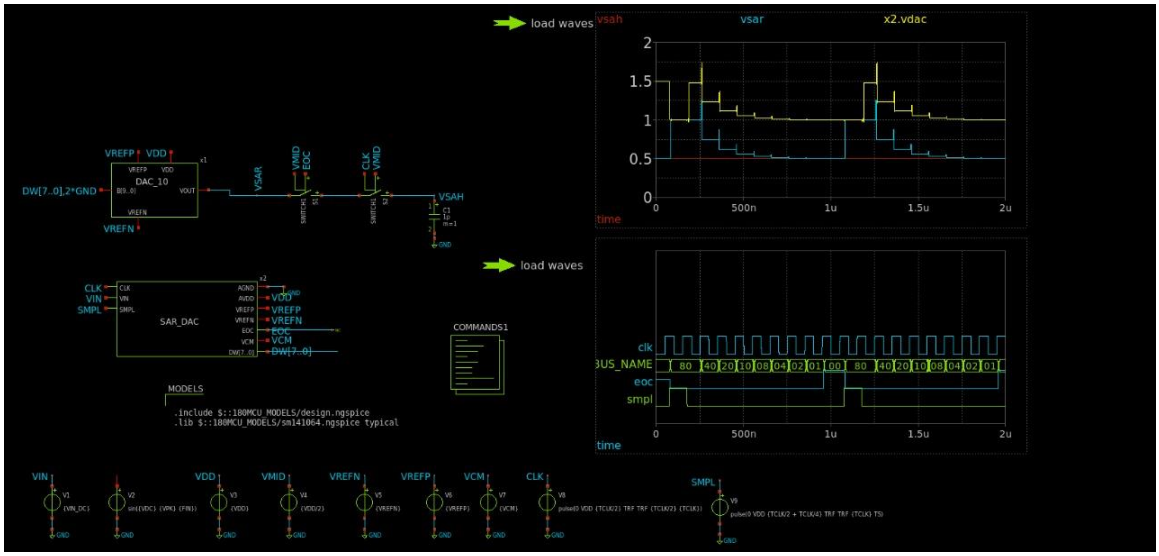

Figure 20: SAR ADC DC Test

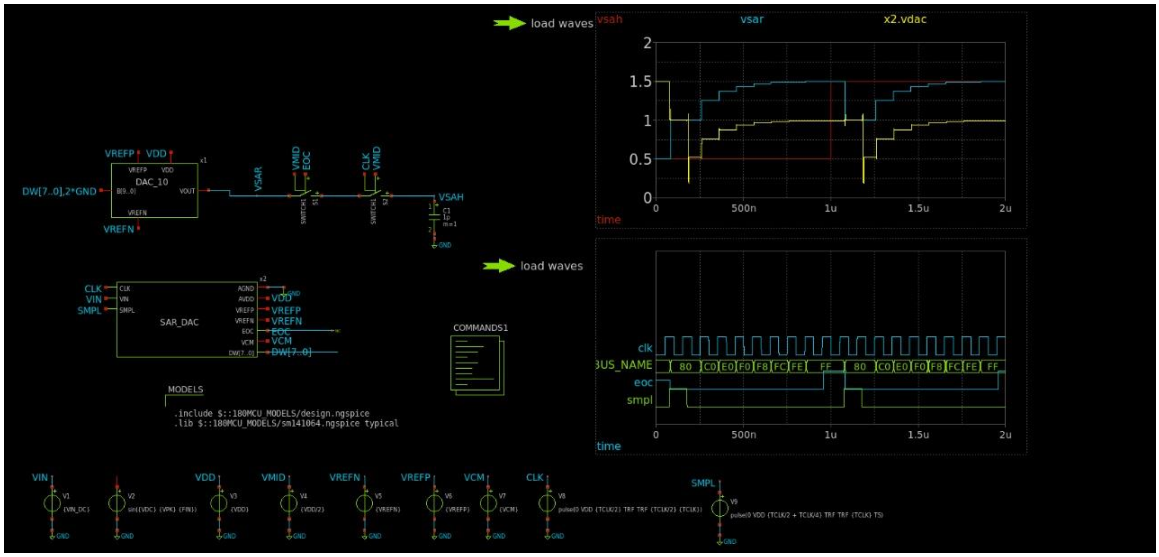

Figure 21: SAR ADC DC Test CTD

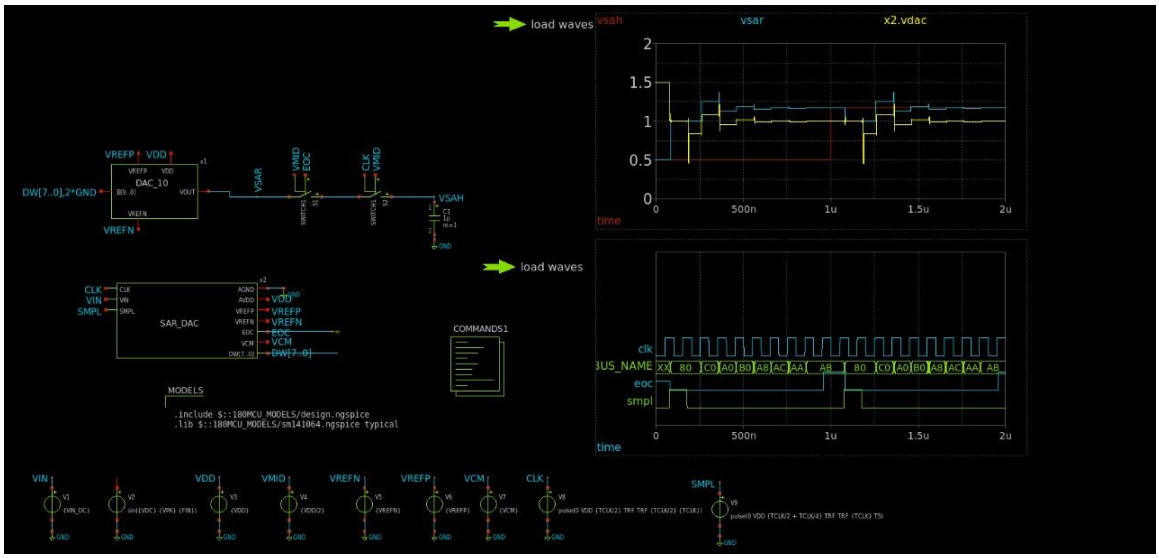

Figure 22: SAR ADC DC Test last shot

Part 7: Sine Wave Test

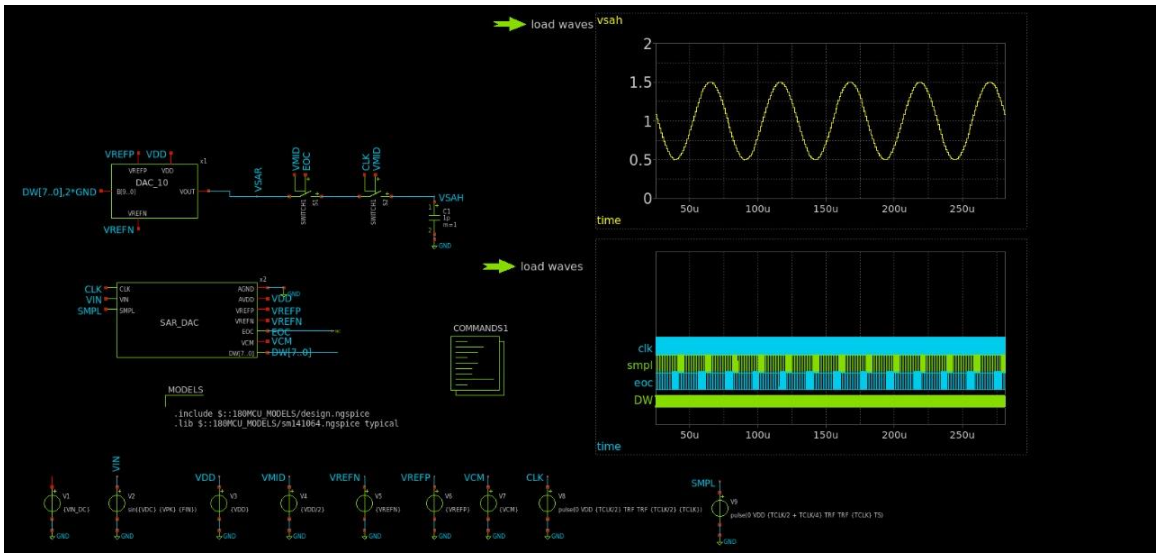

Figure 23: SAR ADC SIN Test

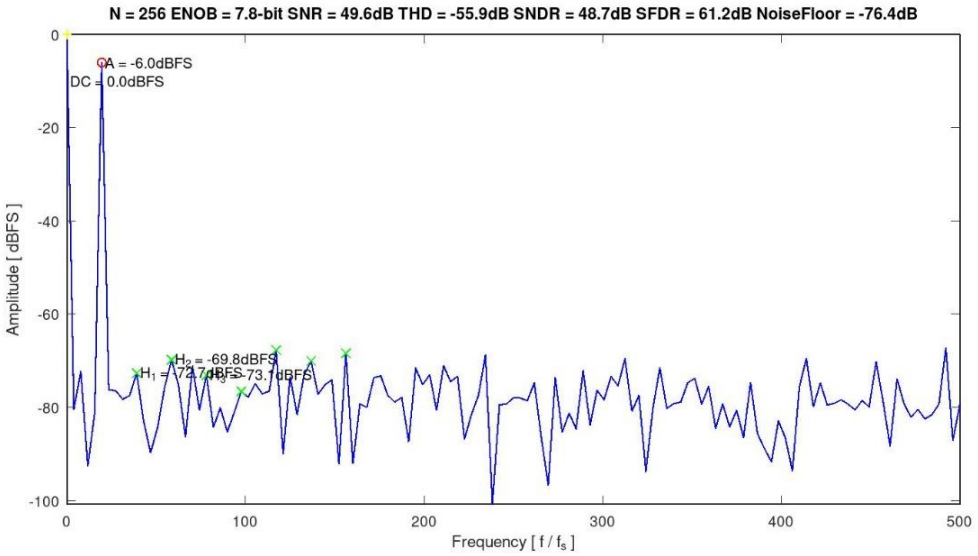

Figure 24: Octave VSAH Output

Analysis of Spectrum and Reported Specifications

The given spectrum plot and results provide key performance metrics for the system under test. Below is a summary of the reported specifications and their implications:

1. **Effective Number of Bits (ENOB):**
   - Reported value: **7.8 bits**
   - ENOB indicates the actual resolution of the system, considering noise and distortions. A value close to 8 bits suggests that the system is performing near the ideal 8-bit resolution but is slightly affected by noise and distortions.
2. **Signal-to-Noise and Distortion Ratio (SINAD):**
   - Reported value: **56.4 dB**
   - SINAD measures the total signal quality by considering both noise and harmonic distortions. A higher value indicates better performance. This value suggests a relatively clean signal with minimal distortion.
3. **Signal-to-Noise Ratio (SNR):**
   - Reported value: **49.5 dB**
   - SNR quantifies the ratio of signal power to noise power, excluding distortion. A value of 49.5 dB suggests that noise is relatively low but still present in the system.
4. **Spurious-Free Dynamic Range (SFDR):**
   - Reported value: **48.7 dB**
   - SFDR represents the ratio between the fundamental signal and the largest spurious (unwanted) tone. A value of 48.7 dB indicates that the highest spurious component is significantly lower than the main signal, meaning good spectral purity.
5. **Total Harmonic Distortion (THD):**
   - Reported value: **-56.4 dB**
   - THD quantifies the distortion introduced by harmonics in the system. A value of -56.4 dB (negative because it's typically represented as a power ratio) indicates minimal harmonic distortion, which is desirable.
6. **Signal Power:**
   - The signal power is -9 **dBFS** (6 dB + 3 dB(Equals multiplying by 2 in linear domain) as we took half of the frequency range only), By analysis: 20log(0.5^2 /4)=9dB.
7. **DC Power:**
   - The DC component is shown as **0 dBFS**, meaning it is at the full-scale level. A high DC component can indicate unwanted offsets in the system, which might need compensation.