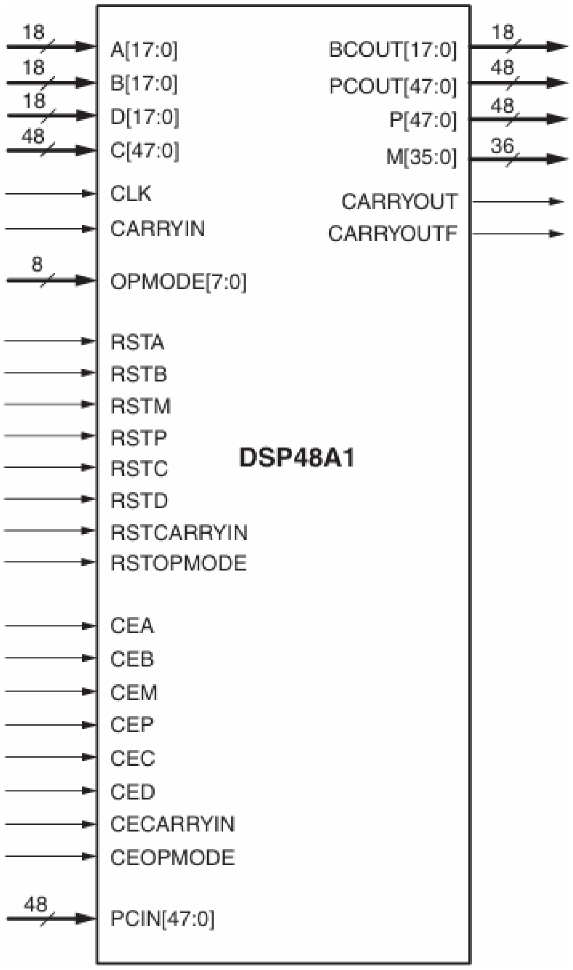
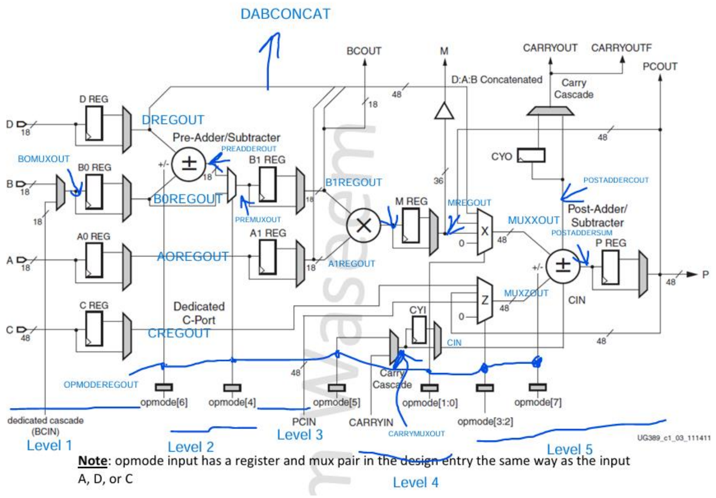
Spartan6 - DSP48A1

By : Khaled Ahmed Hamed

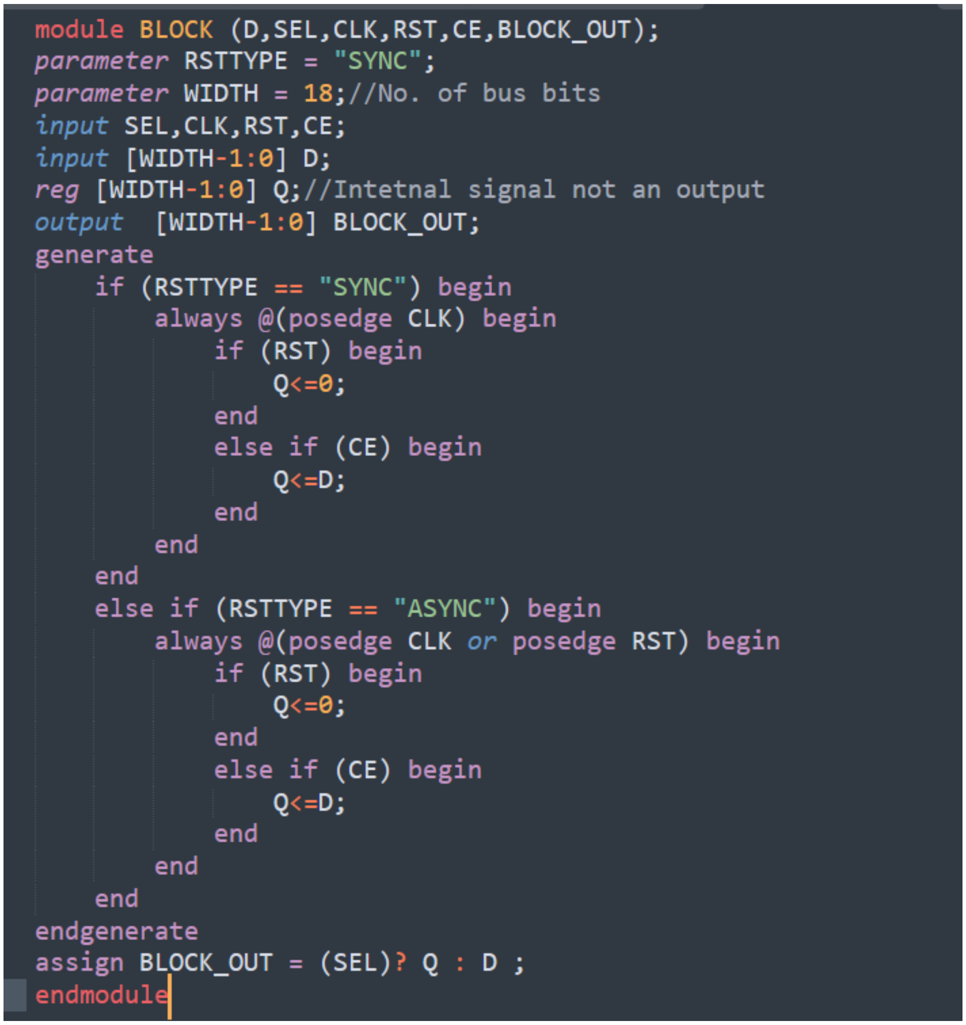


Target Schematic Design:



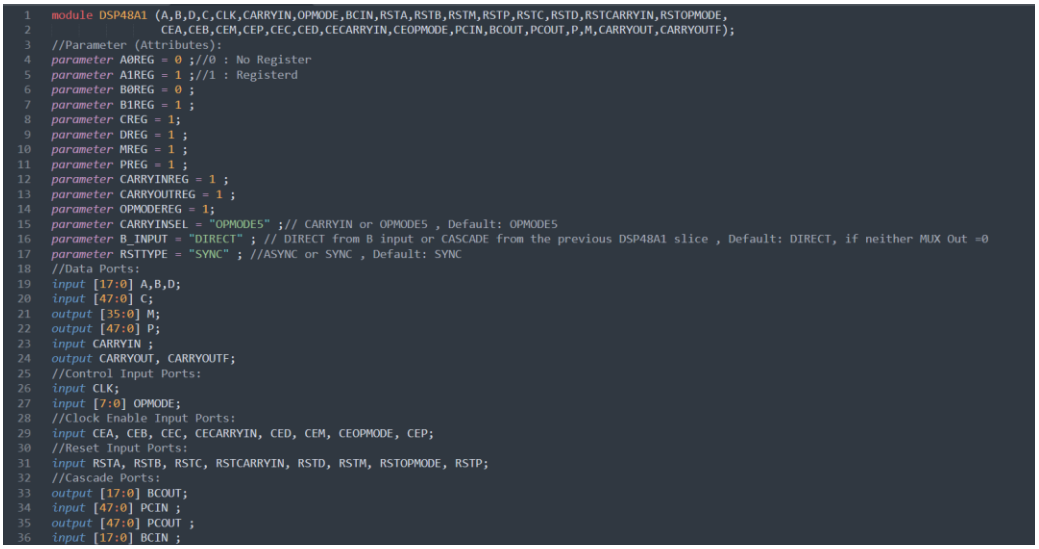
Note: opmode input has a register and mux pair in the design entry the same way as the input A, D, or C

Building Block RTL Snippet:

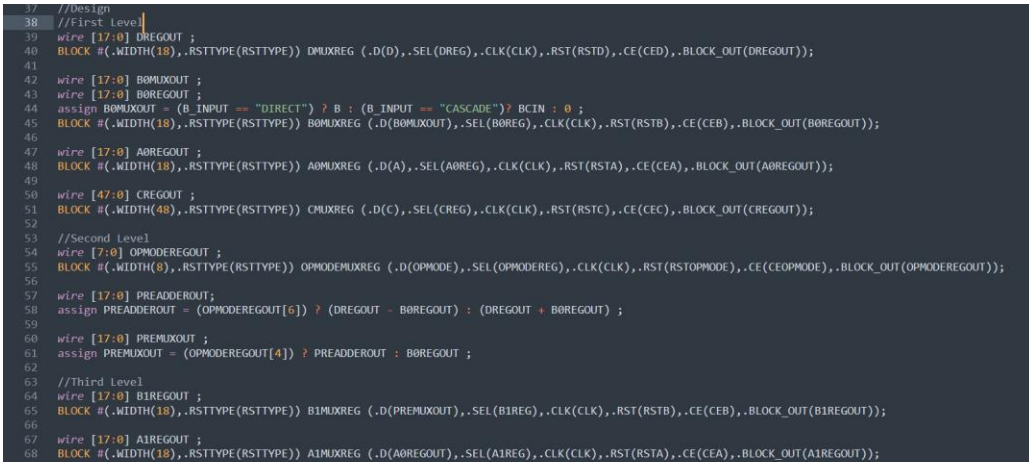


```
module BLOCK (D,SEL,CLK,RST,CE,BLOCK_OUT);
parameter RSTTYPE = "SYNC";
parameter WIDTH = 18;//No. of bus bits
input SEL,CLK,RST,CE;
input [WIDTH-1:0] D;
reg [WIDTH-1:0] Q;//Intetnal signal not an output
output  [WIDTH-1:0] BLOCK_OUT;
generate
    if (RSTTYPE == "SYNC") begin
        always @(posedge CLK) begin
            if (RST) begin
                Q<=0;
            end
            else if (CE) begin
                Q<=D;
            end
        end
    end
    else if (RSTTYPE == "ASYNC") begin
        always @(posedge CLK or posedge RST) begin
            if (RST) begin
                Q<=0;
            end
            else if (CE) begin
                Q<=D;
            end
        end
    end
endgenerate
assign BLOCK_OUT = (SEL)? Q : D ;
endmodule
```

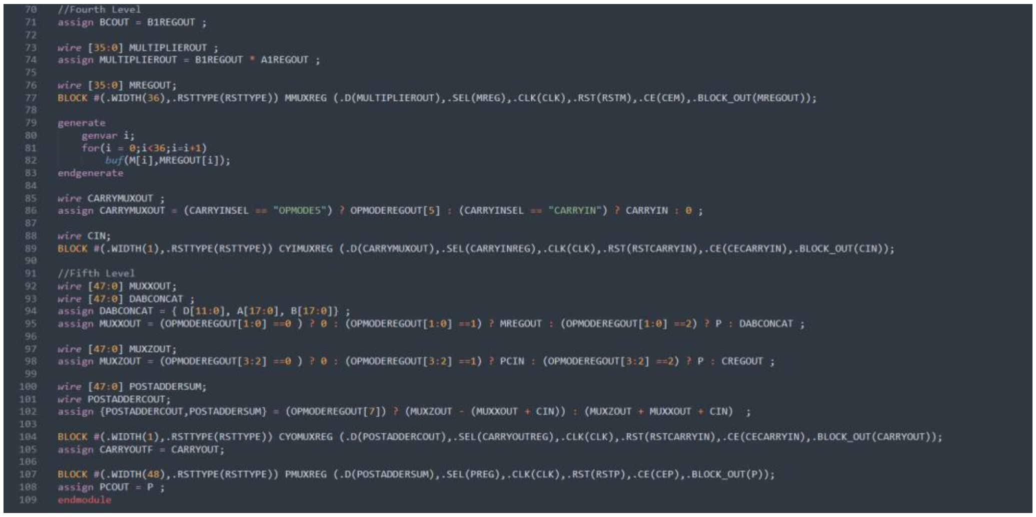
RTL Code Snippets (Top Module):



```verilog
module DSP48A1 (A,B,D,C,CLK,CARRYIN,OPMODE,BCIN,RSTA,RSTB,RSTM,RSTP,RSTC,RSTD,RSTCARRYIN,RSTOPMODE,
                CEA,CEB,CEM,CEP,CEC,CED,CECARRYIN,CEOPMODE,PCIN,BCOUT,PCOUT,P,M,CARRYOUT,CARRYOUTF);
//Parameter (Attributes):
parameter A0REG = 0 ;//0 : No Register
parameter A1REG = 1 ;//1 : Registerd
parameter B0REG = 0 ;
parameter B1REG = 1 ;
parameter CREG = 1;
parameter DREG = 1 ;
parameter MREG = 1 ;
parameter PREG = 1 ;
parameter CARRYINREG = 1 ;
parameter CARRYOUTREG = 1 ;
parameter OPMODEREG = 1;
parameter CARRYINSEL = "OPMODE5" ;// CARRYIN or OPMODE5 , Default: OPMODE5
parameter B_INPUT = "DIRECT" ; // DIRECT from B input or CASCADE from the previous DSP48A1 slice , Default: DIRECT, if neither MUX Out =0
parameter RSTTYPE = "SYNC" ; //ASYNC or SYNC , Default: SYNC
//Data Ports:
input [17:0] A,B,D;
input [47:0] C;
output [35:0] M;
output [47:0] P;
input CARRYIN ;
output CARRYOUT, CARRYOUTF;
//Control Input Ports:
input CLK;
input [7:0] OPMODE;
//Clock Enable Input Ports:
input CEA, CEB, CEC, CECARRYIN, CED, CEM, CEOPMODE, CEP;
//Reset Input Ports:
input RSTA, RSTB, RSTC, RSTCARRYIN, RSTD, RSTM, RSTOPMODE, RSTP;
//Cascade Ports:
output [17:0] BCOUT;
input [47:0] PCIN ;
output [47:0] PCOUT ;
input [17:0] BCIN ;
```

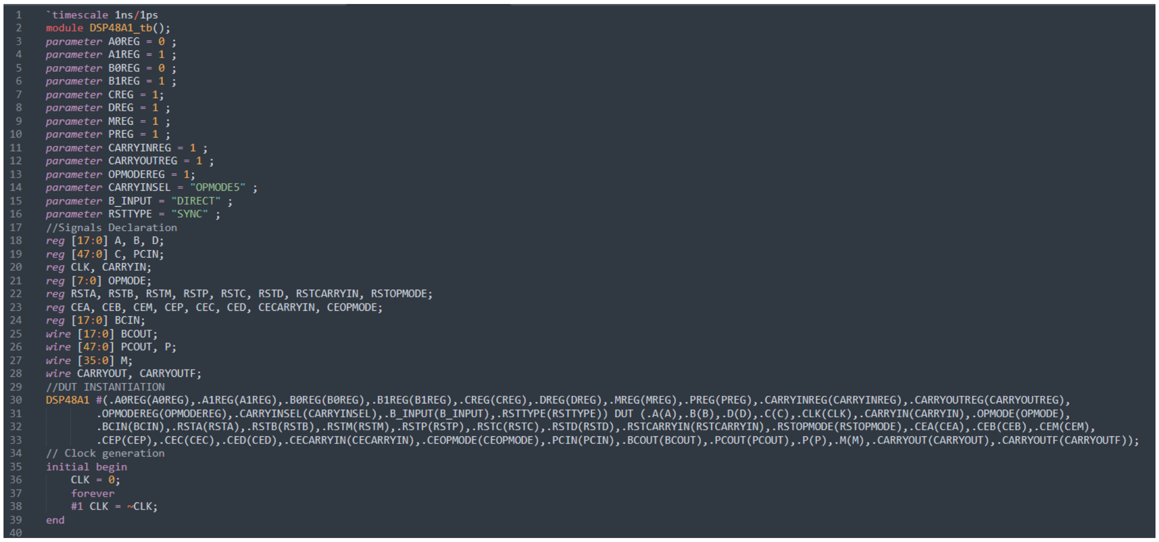


```verilog
//Design
//First Level
wire [17:0] DREGOUT ;
BLOCK #(.WIDTH(18),.RSTTYPE(RSTTYPE)) DMUXREG (.D(D),.SEL(DREG),.CLK(CLK),.RST(RSTD),.CE(CED),.BLOCK_OUT(DREGOUT));

wire [17:0] B0MUXOUT ;
wire [17:0] B0REGOUT ;
assign B0MUXOUT = (B_INPUT == "DIRECT") ? B : (B_INPUT == "CASCADE")? BCIN : 0 ;
BLOCK #(.WIDTH(18),.RSTTYPE(RSTTYPE)) B0MUXREG (.D(B0MUXOUT),.SEL(B0REG),.CLK(CLK),.RST(RSTB),.CE(CEB),.BLOCK_OUT(B0REGOUT));

wire [17:0] A0REGOUT ;
BLOCK #(.WIDTH(18),.RSTTYPE(RSTTYPE)) A0MUXREG (.D(A),.SEL(A0REG),.CLK(CLK),.RST(RSTA),.CE(CEA),.BLOCK_OUT(A0REGOUT));

wire [47:0] CREGOUT ;
BLOCK #(.WIDTH(48),.RSTTYPE(RSTTYPE)) CMUXREG (.D(C),.SEL(CREG),.CLK(CLK),.RST(RSTC),.CE(CEC),.BLOCK_OUT(CREGOUT));

//Second Level
wire [7:0] OPMODEREGOUT ;
BLOCK #(.WIDTH(8),.RSTTYPE(RSTTYPE)) OPMODEMUXREG (.D(OPMODE),.SEL(OPMODEREG),.CLK(CLK),.RST(RSTOPMODE),.CE(CEOPMODE),.BLOCK_OUT(OPMODEREGOUT));

wire [17:0] PREADDEROUT;
assign PREADDEROUT = (OPMODEREGOUT[6]) ? (DREGOUT - B0REGOUT) : (DREGOUT + B0REGOUT) ;

wire [17:0] PREMUXOUT ;
assign PREMUXOUT = (OPMODEREGOUT[4]) ? PREADDEROUT : B0REGOUT ;

//Third Level
wire [17:0] B1REGOUT ;
BLOCK #(.WIDTH(18),.RSTTYPE(RSTTYPE)) B1MUXREG (.D(PREMUXOUT),.SEL(B1REG),.CLK(CLK),.RST(RSTB),.CE(CEB),.BLOCK_OUT(B1REGOUT));

wire [17:0] A1REGOUT ;
BLOCK #(.WIDTH(18),.RSTTYPE(RSTTYPE)) A1MUXREG (.D(A0REGOUT),.SEL(A1REG),.CLK(CLK),.RST(RSTA),.CE(CEA),.BLOCK_OUT(A1REGOUT));
```

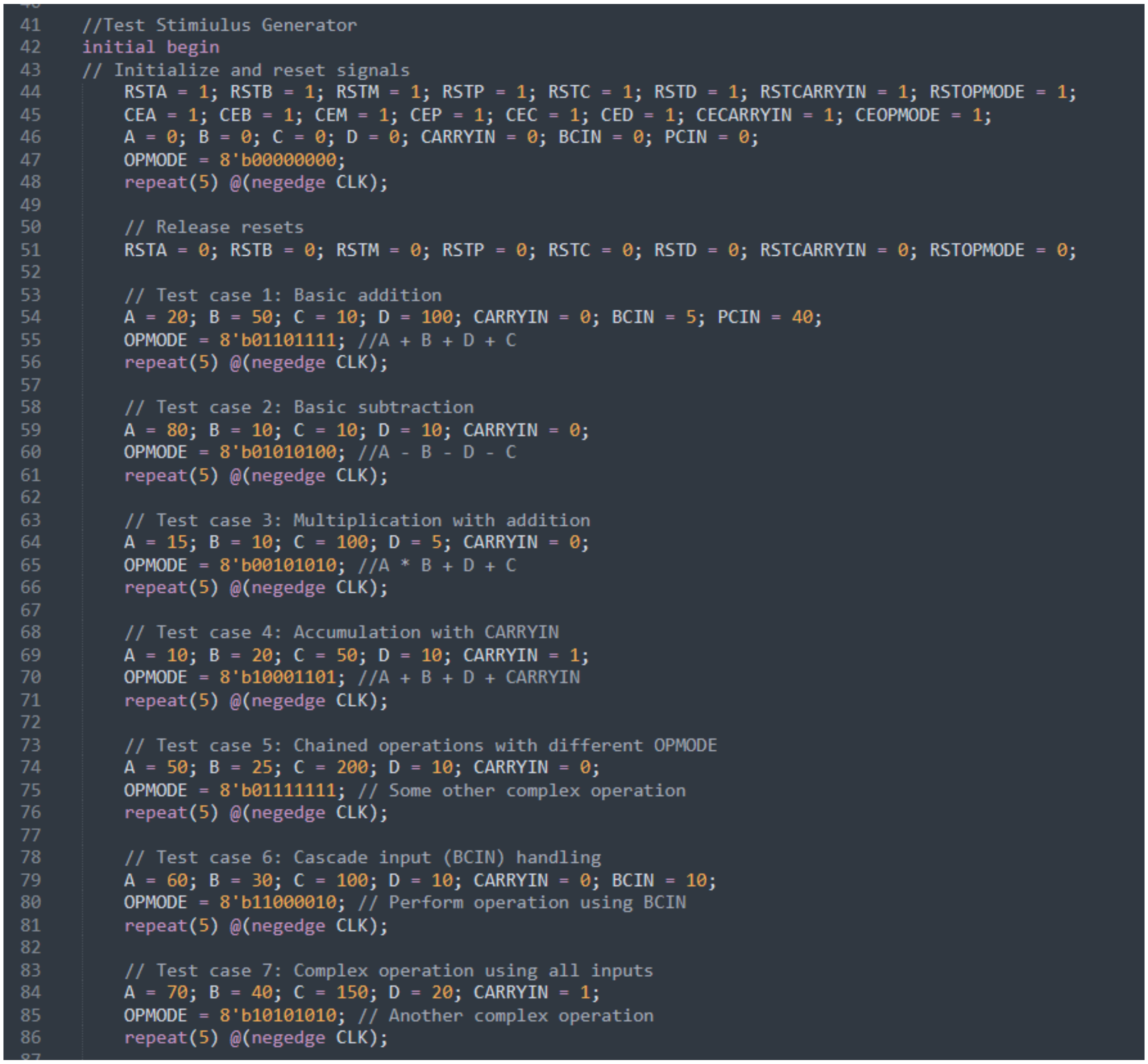


```verilog
//Fourth Level
assign BCOUT = B1REGOUT ;

wire [35:0] MULTIPLIEROUT ;
assign MULTIPLIEROUT = B1REGOUT * A1REGOUT ;

wire [35:0] MREGOUT;
BLOCK #(.WIDTH(36),.RSTTYPE(RSTTYPE)) MMUXREG (.D(MULTIPLIEROUT),.SEL(MREG),.CLK(CLK),.RST(RSTM),.CE(CEM),.BLOCK_OUT(MREGOUT));

generate
    genvar i;
    for(i = 0;i<36;i=i+1)
        buf(M[i],MREGOUT[i]);
endgenerate

wire CARRYMUXOUT ;
assign CARRYMUXOUT = (CARRYINSEL == "OPMODE5") ? OPMODEREGOUT[5] : (CARRYINSEL == "CARRYIN") ? CARRYIN : 0 ;

wire CIN;
BLOCK #(.WIDTH(1),.RSTTYPE(RSTTYPE)) CYIMUXREG (.D(CARRYMUXOUT),.SEL(CARRYINREG),.CLK(CLK),.RST(RSTCARRYIN),.CE(CECARRYIN),.BLOCK_OUT(CIN));

//Fifth Level
wire [47:0] MUXXOUT;
wire [47:0] DABCONCAT ;
assign DABCONCAT = { D[11:0], A[17:0], B[17:0]} ;
assign MUXXOUT = (OPMODEREGOUT[1:0] ==0 ) ? 0 : (OPMODEREGOUT[1:0] ==1) ? MREGOUT : (OPMODEREGOUT[1:0] ==2) ? P : DABCONCAT ;

wire [47:0] MUXZOUT;
assign MUXZOUT = (OPMODEREGOUT[3:2] ==0 ) ? 0 : (OPMODEREGOUT[3:2] ==1) ? PCIN : (OPMODEREGOUT[3:2] ==2) ? P : CREGOUT ;

wire [47:0] POSTADDERSUM;
wire POSTADDERCOUT;
assign {POSTADDERCOUT,POSTADDERSUM} = (OPMODEREGOUT[7]) ? (MUXZOUT - (MUXXOUT + CIN)) : (MUXZOUT + MUXXOUT + CIN)  ;

BLOCK #(.WIDTH(1),.RSTTYPE(RSTTYPE)) CYOMUXREG (.D(POSTADDERCOUT),.SEL(CARRYOUTREG),.CLK(CLK),.RST(RSTCARRYIN),.CE(CECARRYIN),.BLOCK_OUT(CARRYOUT));
assign CARRYOUTF = CARRYOUT;

BLOCK #(.WIDTH(48),.RSTTYPE(RSTTYPE)) PMUXREG (.D(POSTADDERSUM),.SEL(PREG),.CLK(CLK),.RST(RSTP),.CE(CEP),.BLOCK_OUT(P));
assign PCOUT = P ;
endmodule
```

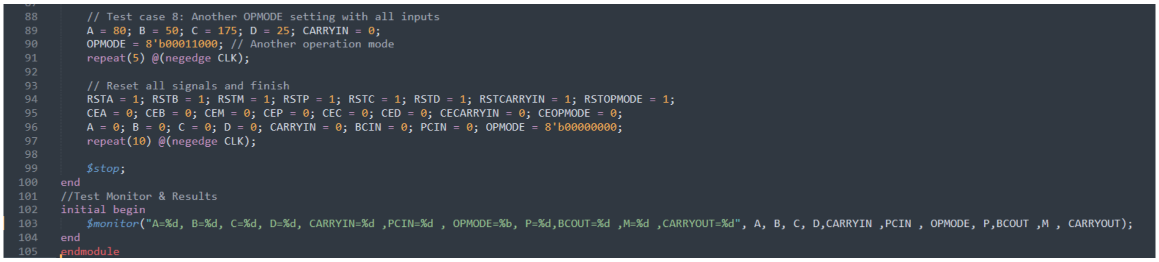
Testbench Code Snippets:



```verilog
`timescale 1ns/1ps
module DSP48A1_tb();
parameter A0REG = 0 ;
parameter A1REG = 1 ;
parameter B0REG = 0 ;
parameter B1REG = 1 ;
parameter CREG = 1;
parameter DREG = 1 ;
parameter MREG = 1 ;
parameter PREG = 1 ;
parameter CARRYINREG = 1 ;
parameter CARRYOUTREG = 1 ;
parameter OPMODEREG = 1;
parameter CARRYINSEL = "OPMODE5" ;
parameter B_INPUT = "DIRECT" ;
parameter RSTTYPE = "SYNC" ;
//Signals Declaration
reg [17:0] A, B, D;
reg [47:0] C, PCIN;
reg CLK, CARRYIN;
reg [7:0] OPMODE;
reg RSTA, RSTB, RSTM, RSTP, RSTC, RSTD, RSTCARRYIN, RSTOPMODE;
reg CEA, CEB, CEM, CEP, CEC, CED, CECARRYIN, CEOPMODE;
reg [17:0] BCIN;
wire [17:0] BCOUT;
wire [47:0] PCOUT, P;
wire [35:0] M;
wire CARRYOUT, CARRYOUTF;
//DUT INSTANTIATION
DSP48A1 #(.A0REG(A0REG),.A1REG(A1REG),.B0REG(B0REG),.B1REG(B1REG),.CREG(CREG),.DREG(DREG),.MREG(MREG),.PREG(PREG),.CARRYINREG(CARRYINREG),.CARRYOUTREG(CARRYOUTREG),
        .OPMODEREG(OPMODEREG),.CARRYINSEL(CARRYINSEL),.B_INPUT(B_INPUT),.RSTTYPE(RSTTYPE)) DUT (.A(A),.B(B),.D(D),.C(C),.CLK(CLK),.CARRYIN(CARRYIN),.OPMODE(OPMODE),
        .BCIN(BCIN),.RSTA(RSTA),.RSTB(RSTB),.RSTM(RSTM),.RSTP(RSTP),.RSTC(RSTC),.RSTD(RSTD),.RSTCARRYIN(RSTCARRYIN),.RSTOPMODE(RSTOPMODE),.CEA(CEA),.CEB(CEB),.CEM(CEM),
        .CEP(CEP),.CEC(CEC),.CED(CED),.CECARRYIN(CECARRYIN),.CEOPMODE(CEOPMODE),.PCIN(PCIN),.BCOUT(BCOUT),.PCOUT(PCOUT),.P(P),.M(M),.CARRYOUT(CARRYOUT),.CARRYOUTF(CARRYOUTF));
// Clock generation
initial begin
    CLK = 0;
    forever
    #1 CLK = ~CLK;
end

```

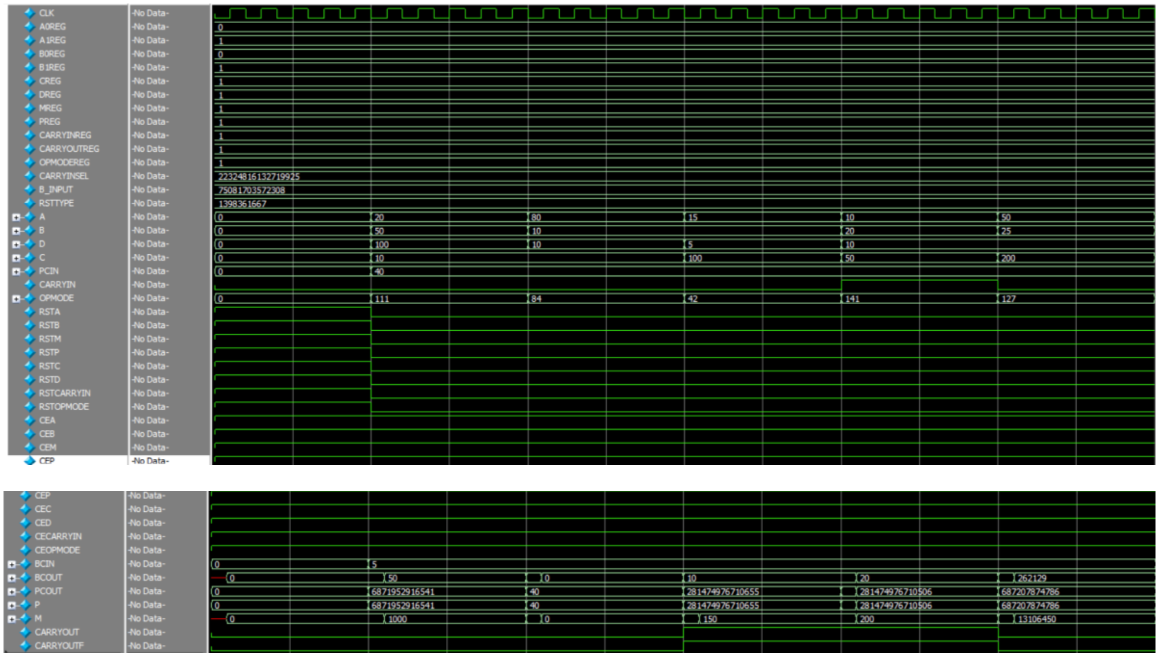


```verilog
//Test Stimiulus Generator
initial begin
// Initialize and reset signals
    RSTA = 1; RSTB = 1; RSTM = 1; RSTP = 1; RSTC = 1; RSTD = 1; RSTCARRYIN = 1; RSTOPMODE = 1;
    CEA = 1; CEB = 1; CEM = 1; CEP = 1; CEC = 1; CED = 1; CECARRYIN = 1; CEOPMODE = 1;
    A = 0; B = 0; C = 0; D = 0; CARRYIN = 0; BCIN = 0; PCIN = 0;
    OPMODE = 8'b00000000;
    repeat(5) @(negedge CLK);

    // Release resets
    RSTA = 0; RSTB = 0; RSTM = 0; RSTP = 0; RSTC = 0; RSTD = 0; RSTCARRYIN = 0; RSTOPMODE = 0;

    // Test case 1: Basic addition
    A = 20; B = 50; C = 10; D = 100; CARRYIN = 0; BCIN = 5; PCIN = 40;
    OPMODE = 8'b01101111; //A + B + D + C
    repeat(5) @(negedge CLK);

    // Test case 2: Basic subtraction
    A = 80; B = 10; C = 10; D = 10; CARRYIN = 0;
    OPMODE = 8'b01010100; //A - B - D - C
    repeat(5) @(negedge CLK);

    // Test case 3: Multiplication with addition
    A = 15; B = 10; C = 100; D = 5; CARRYIN = 0;
    OPMODE = 8'b00101010; //A * B + D + C
    repeat(5) @(negedge CLK);

    // Test case 4: Accumulation with CARRYIN
    A = 10; B = 20; C = 50; D = 10; CARRYIN = 1;
    OPMODE = 8'b10001101; //A + B + D + CARRYIN
    repeat(5) @(negedge CLK);

    // Test case 5: Chained operations with different OPMODE
    A = 50; B = 25; C = 200; D = 10; CARRYIN = 0;
    OPMODE = 8'b01111111; // Some other complex operation
    repeat(5) @(negedge CLK);

    // Test case 6: Cascade input (BCIN) handling
    A = 60; B = 30; C = 100; D = 10; CARRYIN = 0; BCIN = 10;
    OPMODE = 8'b11000010; // Perform operation using BCIN
    repeat(5) @(negedge CLK);

    // Test case 7: Complex operation using all inputs
    A = 70; B = 40; C = 150; D = 20; CARRYIN = 1;
    OPMODE = 8'b10101010; // Another complex operation
    repeat(5) @(negedge CLK);
```

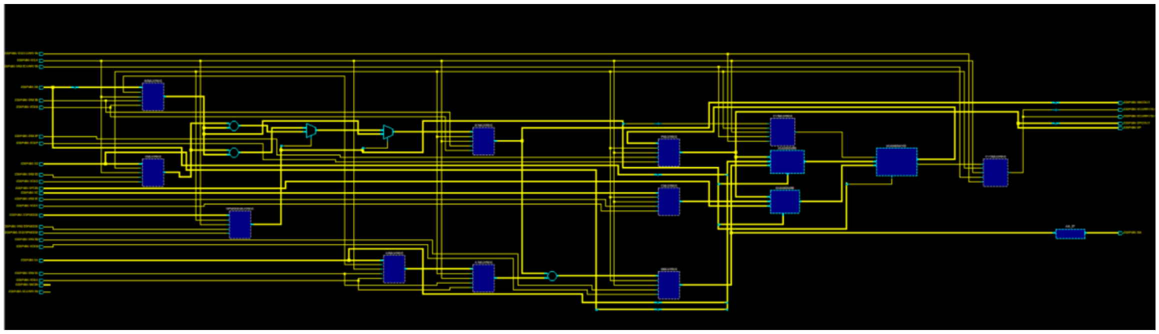


```
    // Test case 8: Another OPMODE setting with all inputs
    A = 80; B = 50; C = 175; D = 25; CARRYIN = 0;
    OPMODE = 8'b00011000; // Another operation mode
    repeat(5) @(negedge CLK);

    // Reset all signals and finish
    RSTA = 1; RSTB = 1; RSTM = 1; RSTP = 1; RSTC = 1; RSTD = 1; RSTCARRYIN = 1; RSTOPMODE = 1;
    CEA = 0; CEB = 0; CEM = 0; CEP = 0; CEC = 0; CED = 0; CECARRYIN = 0; CEOPMODE = 0;
    A = 0; B = 0; C = 0; D = 0; CARRYIN = 0; BCIN = 0; PCIN = 0; OPMODE = 8'b00000000;
    repeat(10) @(negedge CLK);

    $stop;
end
//Test Monitor & Results
initial begin
    $monitor("A=%d, B=%d, C=%d, D=%d, CARRYIN=%d ,PCIN=%d , OPMODE=%b, P=%d,BCOUT=%d ,M=%d ,CARRYOUT=%d", A, B, C, D,CARRYIN ,PCIN , OPMODE, P,BCOUT ,M , CARRYOUT);
end
endmodule
```

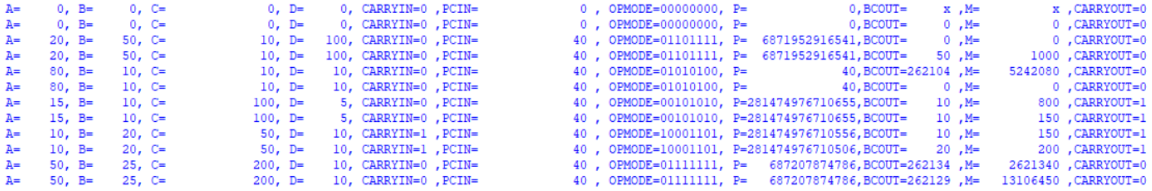
Verification (Testbench Simulation Using QuestaSim):



Schematic (Using QuestaSim):



Transcript Snippet:



```
A=     0, B=     0, C=              0, D=     0, CARRYIN=0 ,PCIN=          0 , OPMODE=00000000, P=              0,BCOUT=     x ,M=        x ,CARRYOUT=0
A=     0, B=     0, C=              0, D=     0, CARRYIN=0 ,PCIN=          0 , OPMODE=00000000, P=              0,BCOUT=     0 ,M=        0 ,CARRYOUT=0
A=    20, B=    50, C=             10, D=   100, CARRYIN=0 ,PCIN=         40 , OPMODE=01101111, P=  6871952916541,BCOUT=     0 ,M=        0 ,CARRYOUT=0
A=    20, B=    50, C=             10, D=   100, CARRYIN=0 ,PCIN=         40 , OPMODE=01101111, P=  6871952916541,BCOUT=    50 ,M=     1000 ,CARRYOUT=0
A=    80, B=    10, C=             10, D=    10, CARRYIN=0 ,PCIN=         40 , OPMODE=01010100, P=             40,BCOUT=262104 ,M=  5242080 ,CARRYOUT=0
A=    80, B=    10, C=             10, D=    10, CARRYIN=0 ,PCIN=         40 , OPMODE=01010100, P=             40,BCOUT=     0 ,M=        0 ,CARRYOUT=0
A=    15, B=    10, C=            100, D=     5, CARRYIN=0 ,PCIN=         40 , OPMODE=00101010, P=281474976710655,BCOUT=    10 ,M=      800 ,CARRYOUT=1
A=    15, B=    10, C=            100, D=     5, CARRYIN=0 ,PCIN=         40 , OPMODE=00101010, P=281474976710655,BCOUT=    10 ,M=      150 ,CARRYOUT=1
A=    10, B=    20, C=             50, D=    10, CARRYIN=1 ,PCIN=         40 , OPMODE=10001101, P=281474976710556,BCOUT=    10 ,M=      150 ,CARRYOUT=1
A=    10, B=    20, C=             50, D=    10, CARRYIN=1 ,PCIN=         40 , OPMODE=10001101, P=281474976710506,BCOUT=    20 ,M=      200 ,CARRYOUT=1
A=    50, B=    25, C=            200, D=    10, CARRYIN=0 ,PCIN=         40 , OPMODE=01111111, P=   687207874786,BCOUT=262134 ,M=  2621340 ,CARRYOUT=0
A=    50, B=    25, C=            200, D=    10, CARRYIN=0 ,PCIN=         40 , OPMODE=01111111, P=   687207874786,BCOUT=262129 ,M= 13106450 ,CARRYOUT=0
```

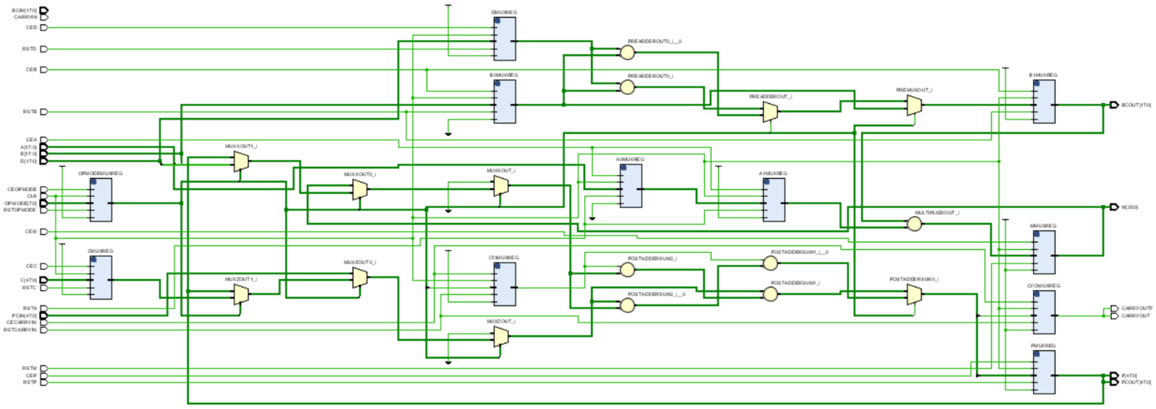
Do file Snippet:

```
vlib work
vlog BLOCK.V DSP48A1.v DSP48A1_tb.v
vsim -voptargs=+acc work.DSP48A1_tb
add wave *
run -all
#quit -sim
```

Snippets From Vivado:

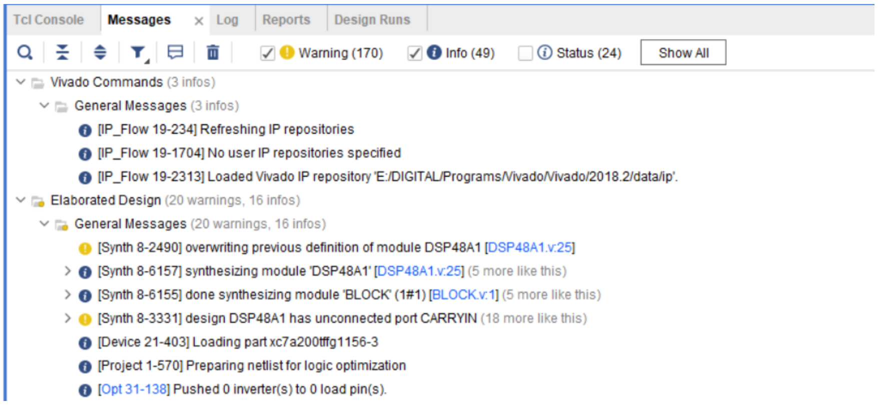
Elaboration:

Schematic:



Messages Tab:

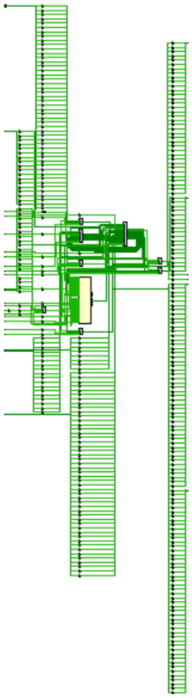
No critical warning

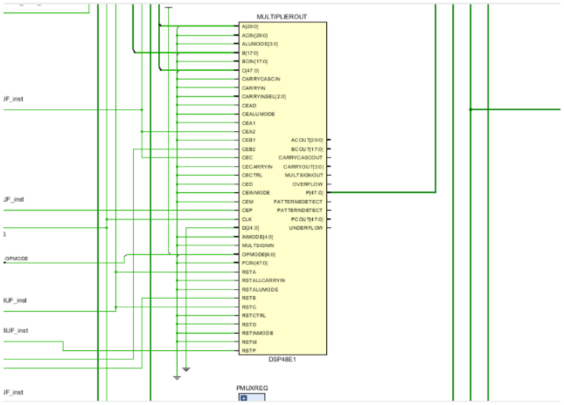


```
Vivado Commands (3 infos)
  General Messages (3 infos)
    [IP_Flow 19-234] Refreshing IP repositories
    [IP_Flow 19-1704] No user IP repositories specified
    [IP_Flow 19-2313] Loaded Vivado IP repository 'E:/DIGITAL/Programs/Vivado/Vivado/2018.2/data/ip'.
Elaborated Design (20 warnings, 16 infos)
  General Messages (20 warnings, 16 infos)
    [Synth 8-2490] overwriting previous definition of module DSP48A1 [DSP48A1.v:25]
  > [Synth 8-6157] synthesizing module 'DSP48A1' [DSP48A1.v:25] (5 more like this)
  > [Synth 8-6155] done synthesizing module 'BLOCK' (1#1) [BLOCK.v:1] (5 more like this)
  > [Synth 8-3331] design DSP48A1 has unconnected port CARRYIN (18 more like this)
    [Device 21-403] Loading part xc7a200tffg1156-3
    [Project 1-570] Preparing netlist for logic optimization
    [Opt 31-138] Pushed 0 inverter(s) to 0 load pin(s).
```

Synthesis:

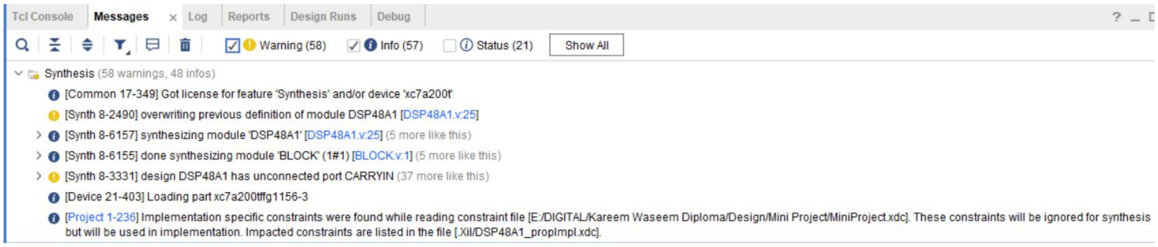
Schematic:





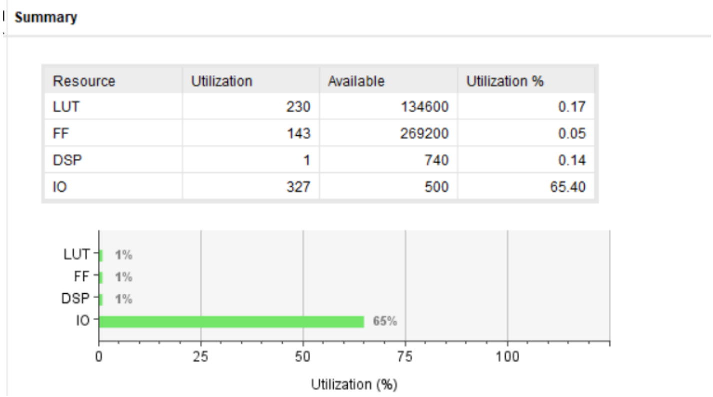
Messages Tab:

No Critical Warning



```
Synthesis (58 warnings, 48 infos)
    [Common 17-349] Got license for feature 'Synthesis' and/or device 'xc7a200t'
    [Synth 8-2490] overwriting previous definition of module DSP48A1 [DSP48A1.v:25]
  > [Synth 8-6157] synthesizing module 'DSP48A1' [DSP48A1.v:25] (5 more like this)
  > [Synth 8-6155] done synthesizing module 'BLOCK' (1#1) [BLOCK.v:1] (5 more like this)
  > [Synth 8-3331] design DSP48A1 has unconnected port CARRYIN (37 more like this)
    [Device 21-403] Loading part xc7a200tffg1156-3
    [Project 1-236] Implementation specific constraints were found while reading constraint file [E:/DIGITAL/Kareem Waseem Diploma/Design/Mini Project/MiniProject.xdc]. These constraints will be ignored for synthesis
    but will be used in implementation. Impacted constraints are listed in the file [.Xil/DSP48A1_propImpl.xdc].
```

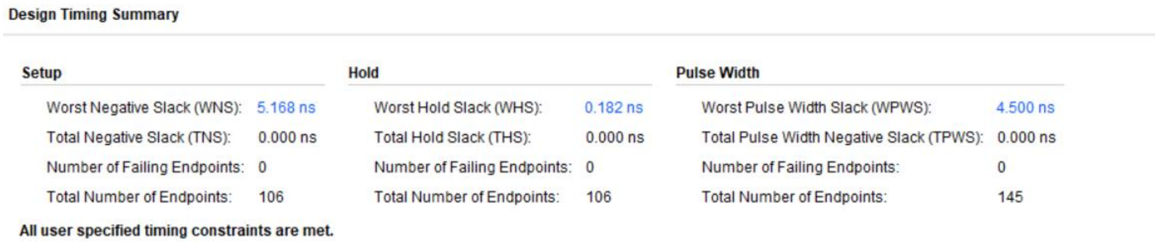
Utilization Report:



Summary

Resource	Utilization	Available	Utilization %
LUT	230	134600	0.17
FF	143	269200	0.05
DSP	1	740	0.14
IO	327	500	65.40

Timing Summary Report:



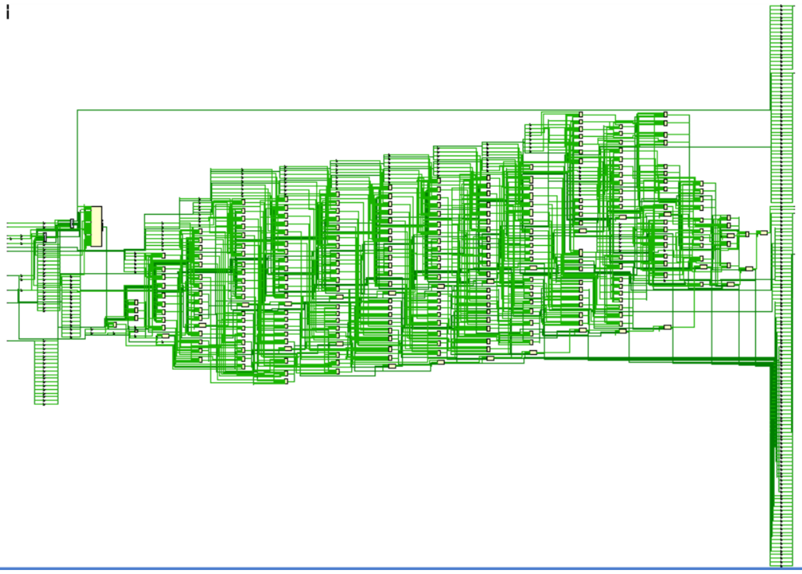
Design Timing Summary

Setup		Hold		Pulse Width	
Worst Negative Slack (WNS):	5.168 ns	Worst Hold Slack (WHS):	0.182 ns	Worst Pulse Width Slack (WPWS):	4.500 ns
Total Negative Slack (TNS):	0.000 ns	Total Hold Slack (THS):	0.000 ns	Total Pulse Width Negative Slack (TPWS):	0.000 ns
Number of Failing Endpoints:	0	Number of Failing Endpoints:	0	Number of Failing Endpoints:	0
Total Number of Endpoints:	106	Total Number of Endpoints:	106	Total Number of Endpoints:	145

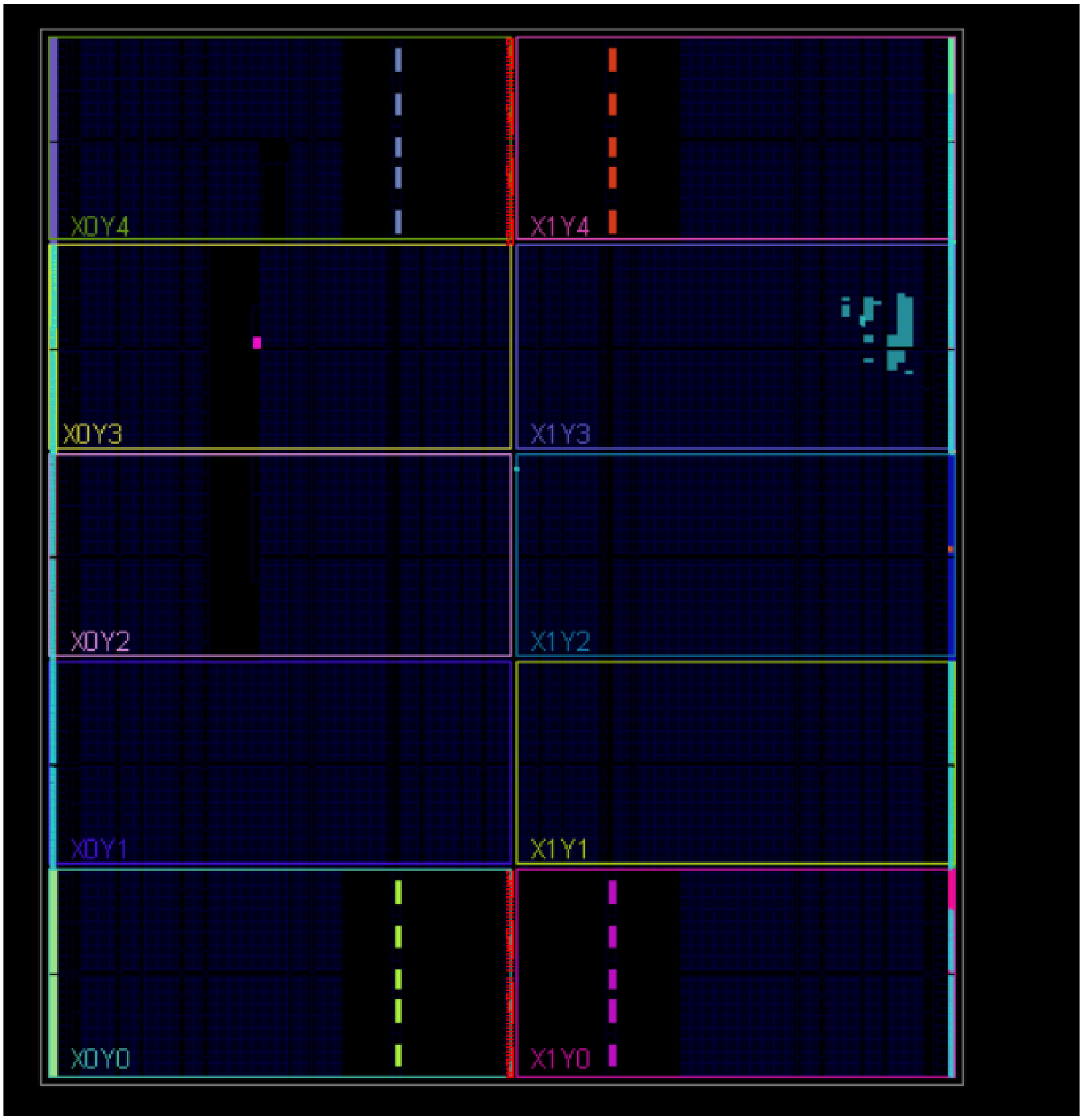
All user specified timing constraints are met.

implementation:

Schematic:

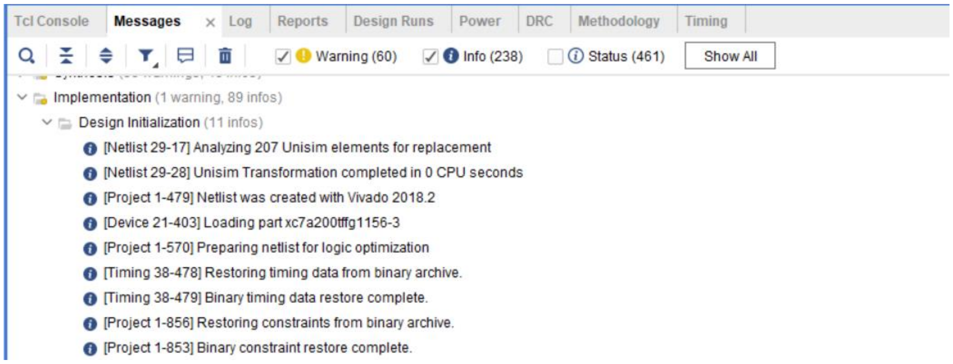


Device:



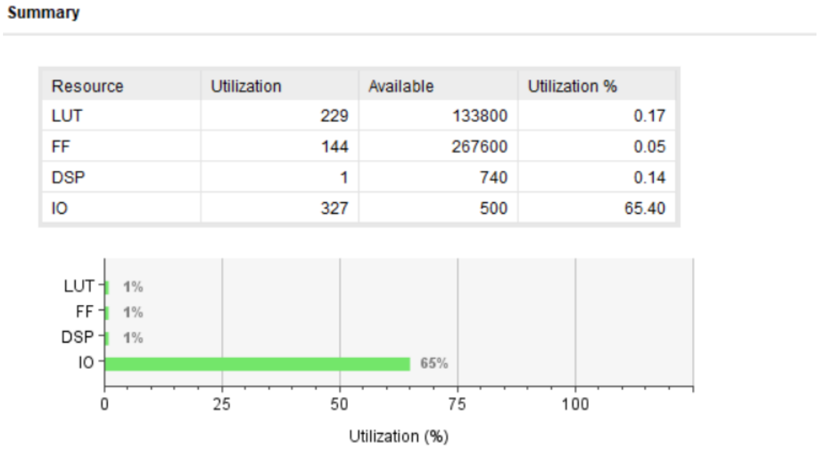
Messages Tab:

No critical warning



```
Implementation (1 warning, 89 infos)
  Design Initialization (11 infos)
    [Netlist 29-17] Analyzing 207 Unisim elements for replacement
    [Netlist 29-28] Unisim Transformation completed in 0 CPU seconds
    [Project 1-479] Netlist was created with Vivado 2018.2
    [Device 21-403] Loading part xc7a200tffg1156-3
    [Project 1-570] Preparing netlist for logic optimization
    [Timing 38-478] Restoring timing data from binary archive.
    [Timing 38-479] Binary timing data restore complete.
    [Project 1-856] Restoring constraints from binary archive.
    [Project 1-853] Binary constraint restore complete.
```

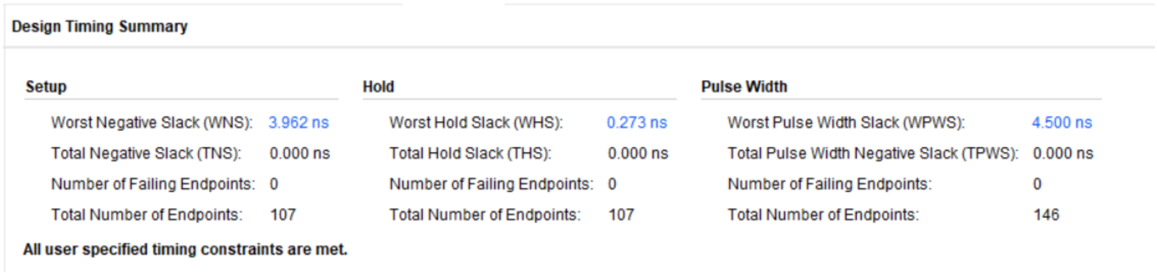
Utilization Report:



Summary

Resource	Utilization	Available	Utilization %
LUT	229	133800	0.17
FF	144	267600	0.05
DSP	1	740	0.14
IO	327	500	65.40

Timing Summary Report:

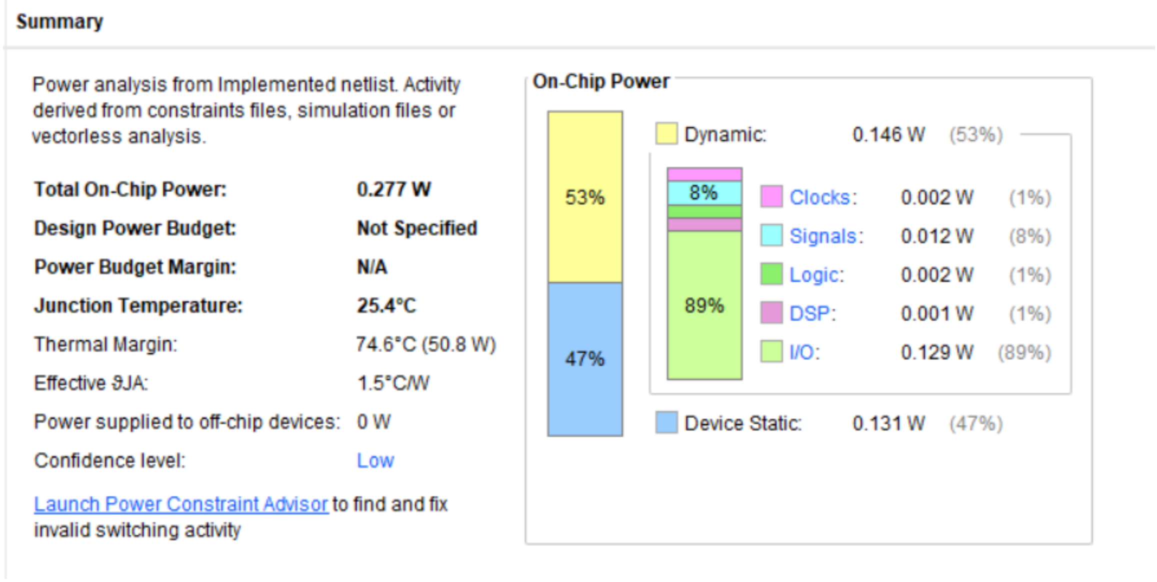


Design Timing Summary

Setup		**Hold**		**Pulse Width**	
Worst Negative Slack (WNS):	3.962 ns	Worst Hold Slack (WHS):	0.273 ns	Worst Pulse Width Slack (WPWS):	4.500 ns
Total Negative Slack (TNS):	0.000 ns	Total Hold Slack (THS):	0.000 ns	Total Pulse Width Negative Slack (TPWS):	0.000 ns
Number of Failing Endpoints:	0	Number of Failing Endpoints:	0	Number of Failing Endpoints:	0
Total Number of Endpoints:	107	Total Number of Endpoints:	107	Total Number of Endpoints:	146

All user specified timing constraints are met.

Power Report:



Summary

Power analysis from Implemented netlist. Activity derived from constraints files, simulation files or vectorless analysis.

Total On-Chip Power:	**0.277 W**
Design Power Budget:	**Not Specified**
Power Budget Margin:	**N/A**
Junction Temperature:	**25.4°C**
Thermal Margin:	74.6°C (50.8 W)
Effective ϑJA:	1.5°C/W
Power supplied to off-chip devices:	0 W
Confidence level:	Low

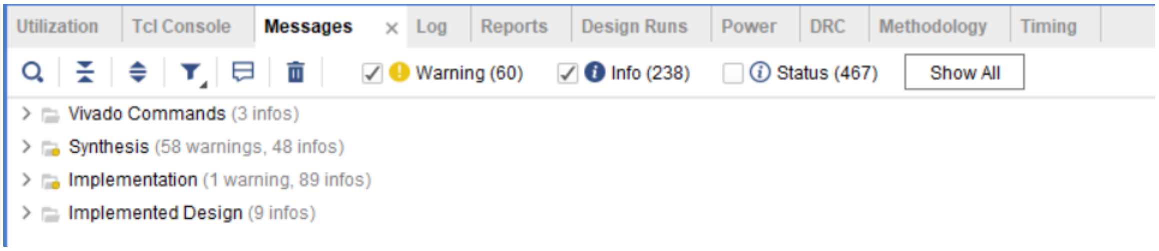
Launch Power Constraint Advisor to find and fix invalid switching activity

On-Chip Power

🟨	Dynamic:	0.146 W	(53%)
🟪	Clocks:	0.002 W	(1%)
🟦	Signals:	0.012 W	(8%)
🟩	Logic:	0.002 W	(1%)
🟪	DSP:	0.001 W	(1%)
🟩	I/O:	0.129 W	(89%)
🟦	Device Static:	0.131 W	(47%)

Messages tab after the whole flow:

No critical warning

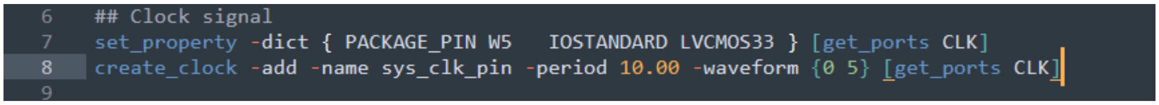


☑ Warning (60) ☑ Info (238) ☐ Status (467)

- Vivado Commands (3 infos)
- Synthesis (58 warnings, 48 infos)
- Implementation (1 warning, 89 infos)
- Implemented Design (9 infos)

Constraints File:

constraint file that has only timing constraint which defines the clock frequency to 100 MHz to pin W5:



```
## Clock signal
set_property -dict { PACKAGE_PIN W5   IOSTANDARD LVCMOS33 } [get_ports CLK]
create_clock -add -name sys_clk_pin -period 10.00 -waveform {0 5} [get_ports CLK]
```

Appendix:

https://drive.google.com/drive/u/0/folders/1CnSlv8lkYDRzgwfwNz1HUHx4fkogawn9