King
CS 331
03 December 2020

Alternative Cache Designs Assessment

Purpose

The purpose of this quiz is twofold:

- To provide you with additional opportunities to review and retrieve information from your memory, thereby strengthening these memories,
- To help you measure your level of familiarity and proficiency in the following skills & knowledge that are essential to your success in this course and professional life beyond school,
- Understand alternatives in cache design and their impact on cost/performance.

Question

Consider a sequence of memory references of word addresses:

22, 25, 24, 56, 40, 24, 20

Cache size is 8 words and assume the LRU replacement strategy.
Mark each reference as a hit (h) or miss (m) and show the final content of the cache for different cache organizations.

Direct Mapped, block size: 1 word

Block address	Binary address	Cache index	Hit/miss	Block 0	Block 1	Block 2	Block 3	Block 4	Block 5	Block 6	Block 7
22	0001 0110	6	Miss							Mem[22]	
25	0001 1001	1	Miss		Mem[25]					Mem[22]	
24	0001 1000	0	Miss	Mem[24]	Mem[25]					Mem[22]	
56	0011 1000	0	Miss	Mem[56]	Mem[25]					Mem[22]	
40	0010 1000	0	Miss	Mem[40]	Mem[25]					Mem[22]	
24	0001 1000	0	Miss	Mem[24]	Mem[25]					Mem[22]	
20	0001 0100	4	Miss	Mem[24]	Mem[25]			Mem[20]		Mem[22]	

Number of cache blocks = 8 words/1 word = 8
Cache index = (block address) % (number of cache blocks)

Final memory references:
22 (m), 25 (m), 24 (m), 56 (m), 40 (m), 24 (m), 20 (m).

Final cache contents:

Block 0	Block 1	Block 2	Block 3	Block 4	Block 5	Block 6	Block 7
Mem[24]	Mem[25]	-	-	Mem[20]	-	Mem[22]	-

2-Way Set Associative, block size: 2 words

Block address	Binary address	Cache index	Hit/miss	Block 0 Set 0	Block 1 Set 0	Block 2 Set 1	Block 3 Set 1
22	0001 0110	0	Miss	Mem[22]			
25	0001 1001	1	Miss	Mem[22]		Mem[25]	
24	0001 1000	0	Miss	Mem[22]	Mem[24]	Mem[25]	
56	0011 1000	0	Miss	Mem[56]	Mem[24]	Mem[25]	
40	0010 1000	0	Miss	Mem[56]	Mem[40]	Mem[25]	
24	0001 1000	0	Miss	Mem[24]	Mem[40]	Mem[25]	
20	0001 0100	0	Miss	Mem[24]	Mem[20]	Mem[25]	

Number of cache blocks = 8 words/2 words = 4
Cache index = (block address) % (number of sets)
Replacement rule: Least recently used

Final memory references:
22 (m), 25 (m), 24 (m), 56 (m), 40 (m), 24 (m), 20 (m).

Final cache contents:

Block 0 Set 0	Block 1 Set 0	Block 2 Set 1	Block 3 Set 1
Mem[24]	Mem[20]	Mem[25]	-

Fully Associative, block size: 1 word

Block address	Binary address	Hit/miss	Block 0	Block 1	Block 2	Block 3	Block 4	Block 5	Block 6	Block 7
22	0001 0110	Miss	Mem[22]							
25	0001 1001	Miss	Mem[22]	Mem[25]						
24	0001 1000	Miss	Mem[22]	Mem[25]	Mem[24]					
56	0011 1000	Miss	Mem[22]	Mem[25]	Mem[24]	Mem[56]				
40	0010 1000	Miss	Mem[22]	Mem[25]	Mem[24]	Mem[56]	Mem[40]			
24	0001 1000	Hit	Mem[22]	Mem[25]	Mem[24]	Mem[56]	Mem[40]			
20	0001 0100	Miss	Mem[22]	Mem[25]	Mem[24]	Mem[56]	Mem[40]	Mem[20]		

Number of cache blocks = 8 words/1 word = 8

Final memory references:
22 (m), 25 (m), 24 (m), 56 (m), 40 (m), 24 (h), 20 (m).

Final cache contents:

Block 0	Block 1	Block 2	Block 3	Block 4	Block 5	Block 6	Block 7
Mem[22]	Mem[25]	Mem[24]	Mem[56]	Mem[40]	Mem[20]	-	-