

Overview of B.Tech Thesis

ABSTRACT

Nanotechnology and VLSI fabrication have a reflective productivity, The growth of one, demands for the growth of another. The expanding and thriving advancements in the field of electronics significantly demand of extremely enhanced technology to be put at use. Quantum-dot Cellular Automata (QCA) secures as the best alternative for replacement of Complementary Metal-Oxide Semiconductor (CMOS) technology for IC fabrication. Advantages such as small size (nanometers), ultra-low power consumption, clock rate (terahertz range) in Quantum Dot Cellular Automata (QCA) as a remarkable innovation for the next generation of digital systems and is being widely utilized as a part of advanced frameworks. Majority gate and inverter (NOT) gate are considered to be the two most fundamental building blocks of QCA. Cell is the name given to the fundamental unit of Quantum dot cellular automata QCA. The dissertation presents an integration of the two domains wherein a novel ultra-efficient, multi-operative 3×3 universal reversible gate, SKV-QCA, is proposed and implemented in QCA. Aiming optimization, the gate is redesigned and restructured using precise QCA cell interaction. The proposed SKV-QCA gate, then, is used for implementation of all the basic logic gates to validate its universality. The multi-operation nature of the gate is established by implementation of all the 13 standard Boolean functions using SKV-QCA. SKV-QCA is then used for designing of half adder and full adder in QCA. The designs are extensively compared with previous such attempts and are found to be ultra-efficient and more robust than all of them. Also, the energy dissipation analysis of the designs has also been presented for varying setups; the analysis establishes minimum energy dissipation by the designs endorsing them for the applicability in ultra-high efficiency designing.

Chapter 1

Introduction

1.1 Performance Parameters in QCA Nanotechnology

Various parameters are pertinent to define the efficiency of the circuit design in QCA technology. The main parameters taken into account whilst determining the efficiency of QCA system are:

1. Cell Count
2. Total Area Covered by the design
3. Area Covered by cells
4. Latency of design
5. Complexity of design
6. Power Dissipation

An overview of these parameters is presented as follows.

1. Cell count:

The cell count of the electronic circuit is defined as the total number of cells that have been put into use for the implementation of the design. The cell count should be minimal to ensure that the design is compact so as to ensure miniaturization of the design.

2. Cell area:

Cell area of a design is defined as the total area occupied by the cells in the design of electronic circuit. This parameter in turn is dependent on the number of cells used and the area occupied by each cell. However, the spacing between the cells is not taken into account and is therefore considered unused.

$$\text{Cell Area} = \text{Size of a Cell} \times \text{Number of Cells.}$$

3. Total area:

It is in fact the most important parameter considered in case of the optimization of the design. It is defined as the total area occupied by the design irrespective of placement of the cells. The total area is greater than the cell area as it takes into account gaps between cells and the unused space on the chip. It is hence dependent on the horizontal and the vertical cell coverage.

4. Latency:

It is the parameter responsible for the computation of delay in design of the circuit. In case of QCA, latency can be described as the number of clock phases required for the attainment of the output result that is implementation of the design circuit. The lower the latency of the circuit the more efficient the circuit is considered.

5. Complexity:

The complexity of the circuit is described as the number of crossovers required and the type of the crossovers used in the formulation of the electronic circuit.

6. Power Dissipation

Power dissipation is an important factor in determining the efficiency of the QCA design. The power dissipation analysis is performed by QCAPro tool. Wherein we are able to obtain the heat maps for various kink energy values and at different temperatures.

Chapter 2

Proposed Designs

In this work, a novel universal logic gate called as SKV-QCA Gate has been proposed. Although a large number of reversible gates have already been proposed in the literature, a new gate is designed because the implementation of the existing gates in the QCA is costly. The equations at the outputs have been modified in accordance with the ease in implementation of the various logical functions. Moreover, the design of this gate in the Quantum Dot Cellular Automata Nano-Technology is our prime focus and is obtained by the use of 37 cells.

The proposed gate is a 3-input, 3-output gate with an input-vector (I_v) and an output-vector (O_v) as:

$$I_v = (A, B, C);$$

$$O_v = (P = A \oplus B, Q = A \ominus C, R = AB + BC + CA)$$

The block diagram of the proposed SKV-QCA Gate is shown in the figure 2.1 and the truth table verifying the outputs is shown in the table 1.

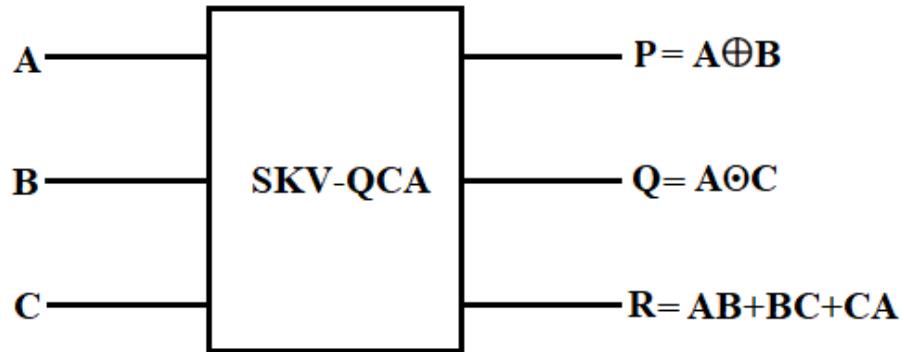


Figure 2.1: Block Diagram Representation of SKV-QCA

Table 1: Truth Table of SKV-QCA

Input Encoding	Input			Output			Output Encoding
	A	B	C	P	Q	R	
0	0	0	0	0	1	0	2
1	0	0	1	0	0	0	0
2	0	1	0	1	1	0	6
3	0	1	1	1	0	1	5
4	1	0	0	1	0	0	4
5	1	0	1	1	1	1	7
6	1	1	0	0	0	1	1
7	1	1	1	0	1	1	3

The above table proves the reversible nature of the SKV-QCA gate. As it can be seen from the table that the one on one mapping holds good in the system, that means for a particular set of inputs the output encoding is unique. This reversibility in the system is achieved by selecting a particular set of outputs for the system. The encoding of the input and that of the output is different as seen from the table.

2.1 SKV-QCA using Explicit Interaction of Cells

For obtaining the best possible design for the SKV-QCA Gate, the gate is redesigned using the best approach available in the literature. The method used for redesigning the system is the explicit interaction of cells. The final design thus obtained is more efficient than that of the designs using the majority voter approach. This shift in the nature of design highly effects the optimization of the designs. No crossover is required in the optimized design of the SKV-QCA gate. The cell count is 37 cells and there is satisfactory improvement in the total area of the design. The simulated design uses some of the majority gates for performing the logical AND and OR operation.

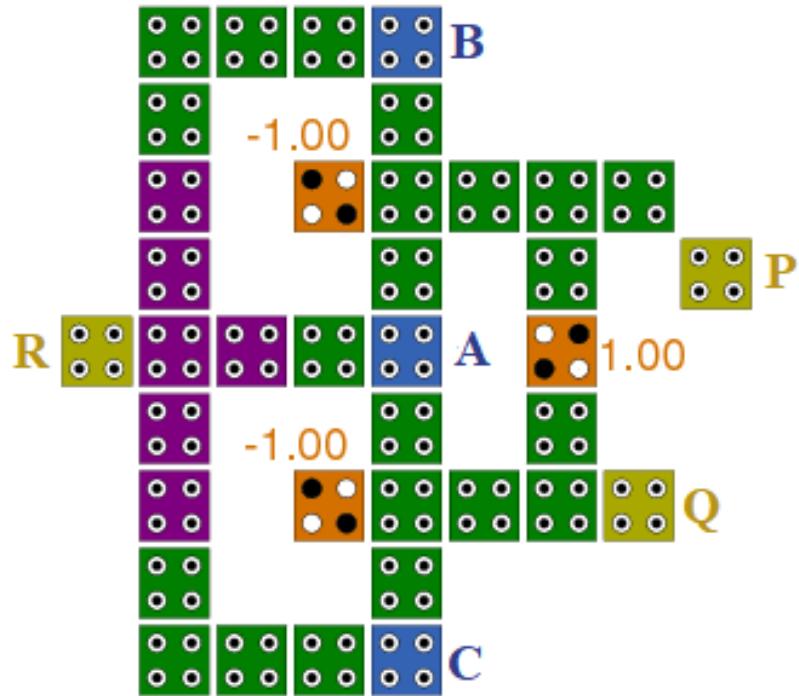


Figure 2.2: Proposed SKV-QCA Using Interaction of Cells

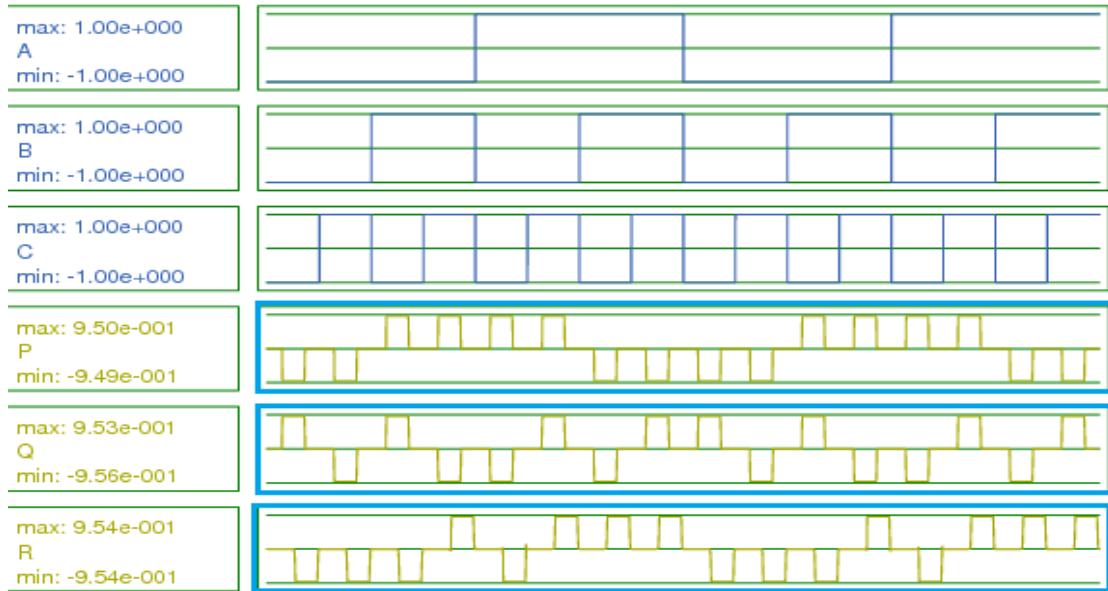


Figure 2.3: Simulation Result for proposed SKV-QCA gate.

The performance parameters.

I. Cell Count: 37 Cells.

$$\begin{aligned}
 \text{II. Cell Area} &= \frac{\text{No. of cells} \times \text{Dimension of the cell}}{10^6} \mu\text{m}^2 \\
 &= \frac{37 \times 18 \times 18}{10^6} \mu\text{m}^2 \\
 &= 0.01198 \mu\text{m}^2
 \end{aligned}$$

$$\begin{aligned}
 \text{III. Total Area} &= \frac{\text{Horizontal cells} \times \text{Vertical Cells} \times \text{Dimension of the cell}}{10^6} \mu\text{m}^2 \\
 &= \frac{9 \times 9 \times 18 \times 18}{10^6} \mu\text{m}^2 \\
 &= 0.02624 \mu\text{m}^2
 \end{aligned}$$

IV. Latency = 0.5

V. Complexity = 0 Crossover used

2.2 SKV-QCA as a Universal Gate

The functionalities of a gate are prime factor that defines its efficiency. This defines the basic number of operations which this gate can perform. A gate is defined to be universal in nature if it is capable of implementing all the basic seven-Boolean functions. The SKV-QCA can work as a universal gate by changing the different inputs of the gate. The inputs are changed in accordance to the requirements which lead to the necessary framing of the equation.

If the SKV-QCA is used as an inverter i.e. NOT gate then the desired input whose compliment is to be achieved is applied at the input A and a logic 1 is applied to input B. If the input C is set to logic zero, AND operation can be performed for the inputs A and B; If the compliments of A and B are applied, NOR operation can be realized. If on the other hand the input C is set to one, OR function can be implemented; if the compliments of A and B are applied, NAND operation can be realized. XOR and XNOR are the intrinsic outputs of the SKV-QCA gate. The implementation of NOT, NAND, AND, OR, EXOR AND XNOR Gates using SKV-QCA gate is achieved as shown below.

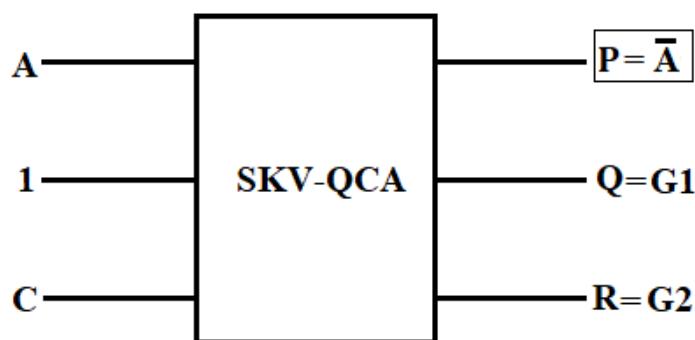


Figure 2.4: SKV-QCA Gate as NOT gate.

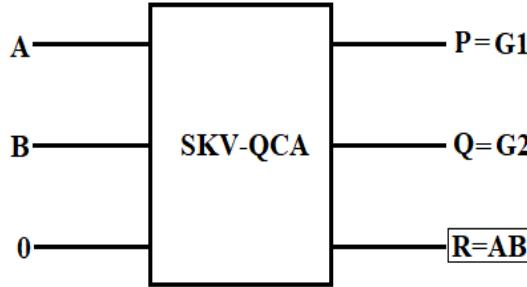


Figure 2.5: SKV-QCA Gate as AND gate

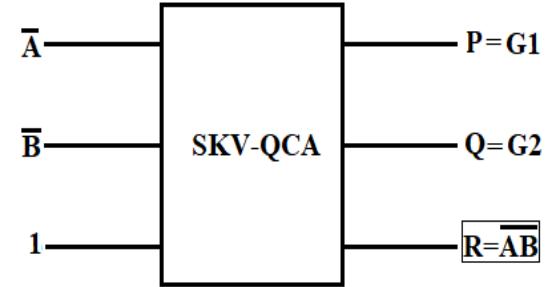


Figure 2.6: SKV-QCA Gate as NAND gate

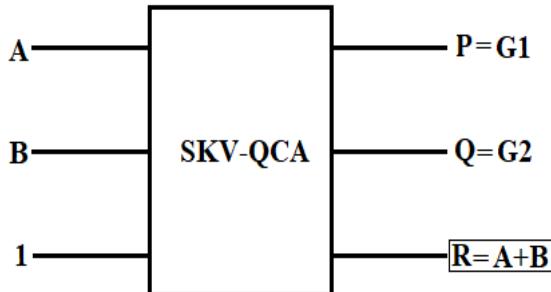


Figure 2.7: SKV-QCA Gate as OR gate.

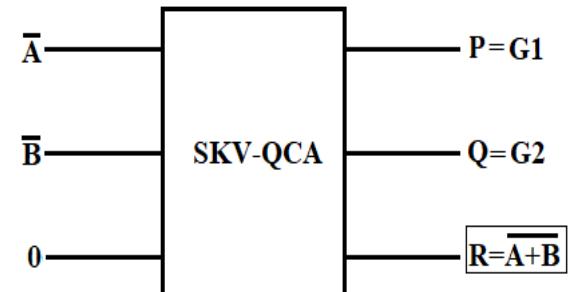


Figure 2.8: SKV-QCA Gate as NOR gate.

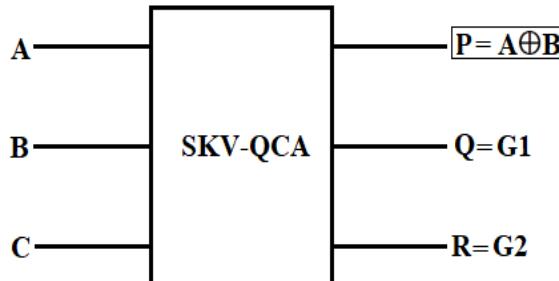


Figure 2.9: SKV-QCA Gate as XOR gate.

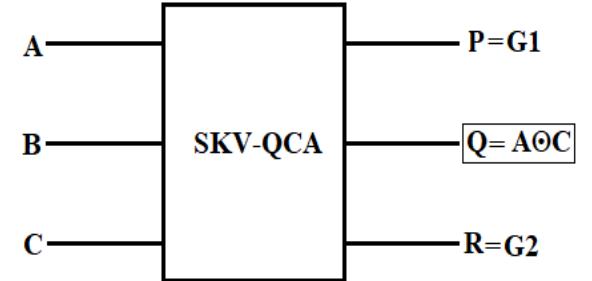


Figure 2.10: SKV-QCA Gate as XNOR gate

2.3 Hardware Complexity of SKV-QCA

In case of reversible circuits, one of the main parameters for the measurement of the complexity of the proposed design is defined by the number of XOR Gates and the number of ‘AND’ and ‘NOT’ operations required to perform the output functions of the gate. The logical calculation of XOR operation is calculated by ‘ α ’, of the ‘AND’ operation the logical calculation is done by ‘ β ’ and for ‘NOT’ operation the logical calculation is done by ‘ γ ’. From the outputs of the SKV-QCA we can see that the outputs can be changed to include only three operations without any change relative to the truth table of the given gate as shown below

$$P = A \oplus B$$

$$Q = \overline{A \oplus C}$$

$$R = (A \oplus B)C \oplus AB$$

From the shown equations we can see that there is a slight change in the outputs Q and R, however any of these variations do not stimulate changes in the truth table of the SKV- QCA Gate and thus can be used interchangeably with the previous output equations of the SKV-QCA Gate.

Now the total complexity of the gate can be calculated as the number of ‘XOR’, ‘AND’ and ‘NOT’ operations performed in the system.

Total logical calculation is shown as:

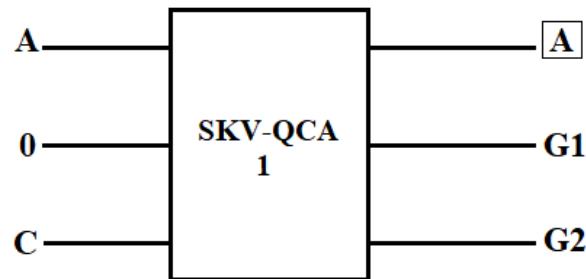
$$3\alpha + 2\beta + \gamma$$

Where ‘ α ’, ‘ β ’ and ‘ γ ’ is the logical calculations of the ‘XOR’, ‘AND’ and ‘NOT’ operation.

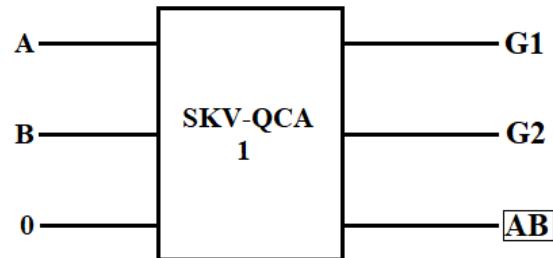
2.4 Implementing 13 standard functions using SKV-QCA

The effectiveness of the SKV-QCA is evaluated by the implementation of 13 standard functions. The 13-standard functions represent the 256 3-variable Boolean functions. Since any 3 variable Boolean functions can be converted to one of the thirteen- standard functions, The thirteen functions represent the multi-operative nature of the gate.. The total gates, garbage output and constant inputs are mentioned in table 2.

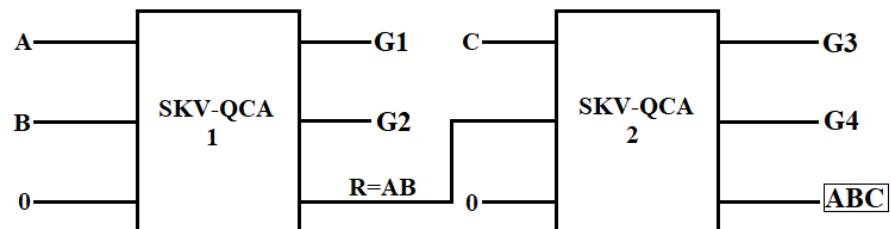
1) $F = A$



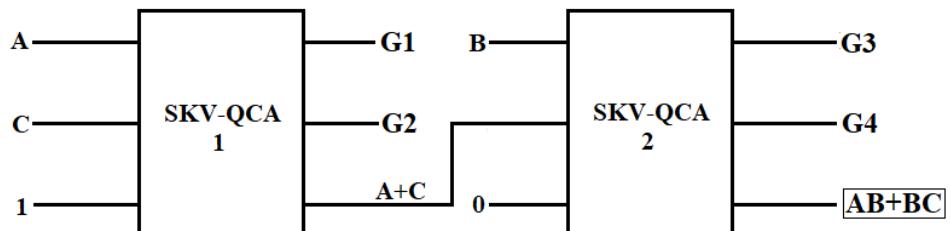
2) $F = AB$



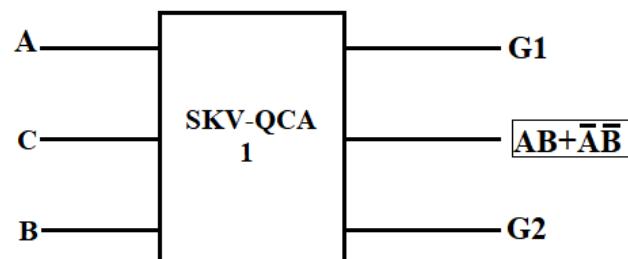
3) $F = ABC$



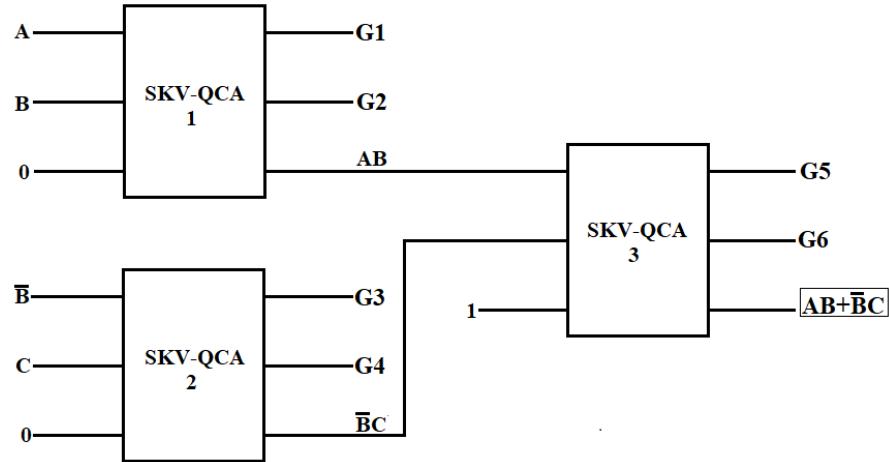
4) $F = AB + BC$



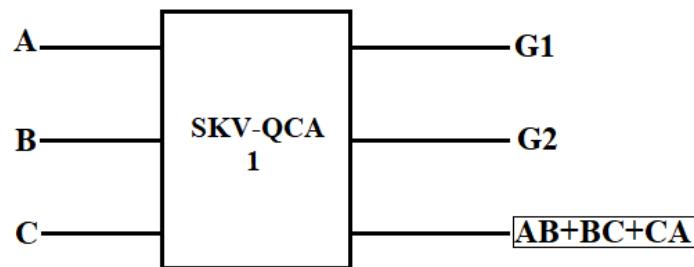
5) $AB + \bar{A}\bar{B}$



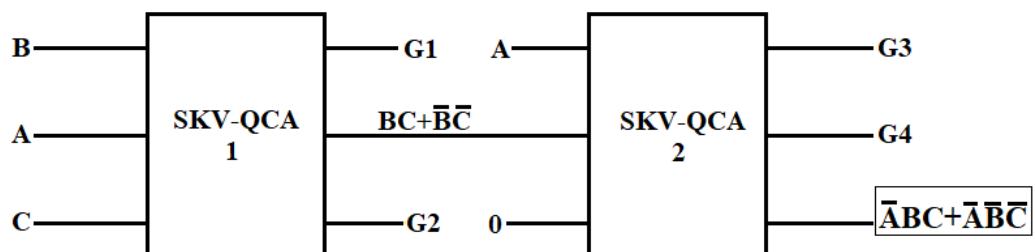
$$6) \quad F = AB + \bar{B}C$$



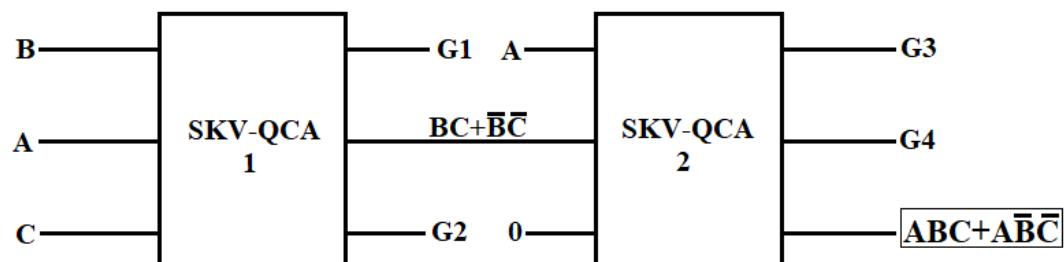
$$7) \quad F = AB + BC + CA$$



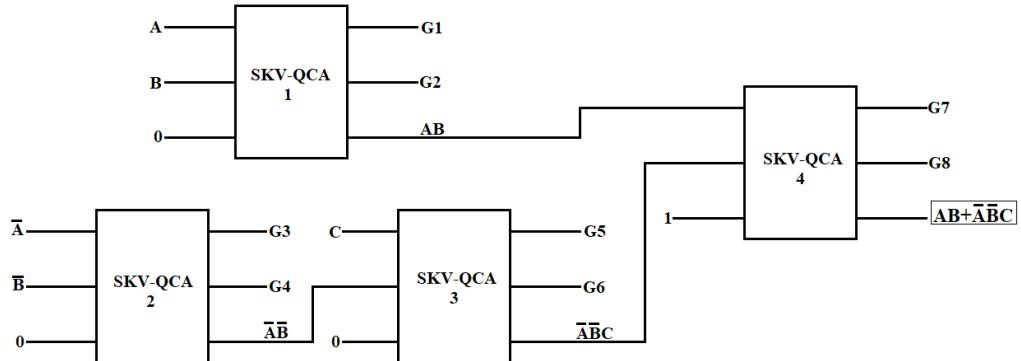
$$8) \quad F = \bar{A}BC + \bar{A}\bar{B}\bar{C}$$



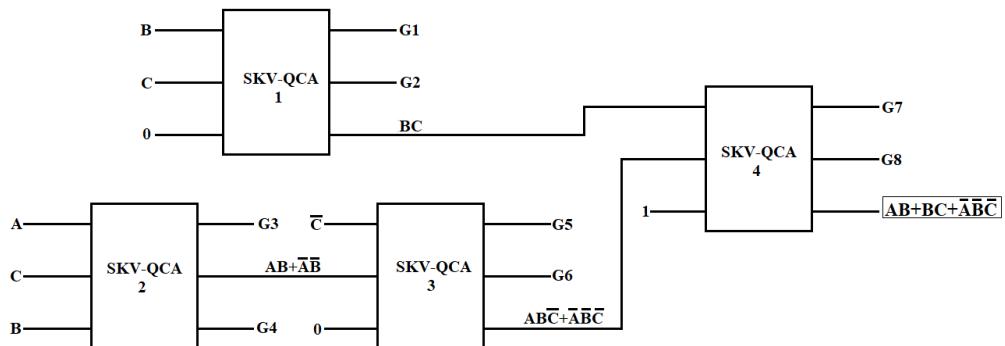
$$9) \quad F = ABC + A\bar{B}\bar{C}$$



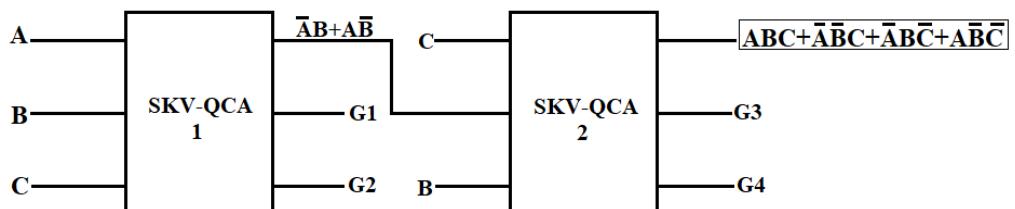
$$10) F = AB + \bar{A}\bar{B}C$$



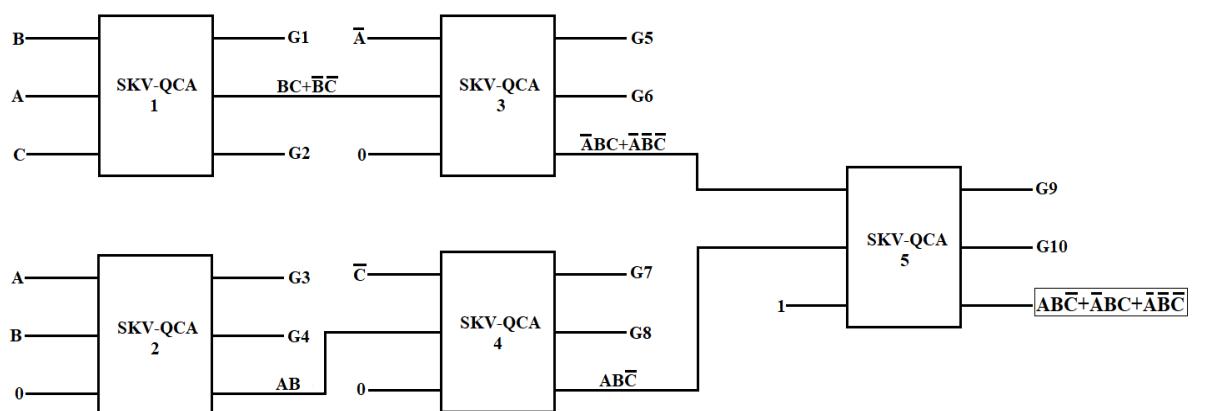
$$11) F = AB + BC + \bar{A}\bar{B}\bar{C}$$



$$12) F = ABC + \bar{A}\bar{B}C + \bar{A}\bar{B}\bar{C} + A\bar{B}\bar{C}$$



$$13) F = AB\bar{C} + \bar{A}BC + \bar{A}\bar{B}\bar{C}$$



S. No.	Function	Number of gates	Fixed input	Garbage output
1	A	1	1	2
2	AB	1	1	2
3	ABC	2	2	4
4	AB + BC	2	2	4
5	AB + $\bar{A}\bar{B}$	1	0	2
6	AB + $\bar{B}C$	3	3	6
7	AB + BC + CA	1	0	2
8	$\bar{A}BC + \bar{A}\bar{B}\bar{C}$	2	1	4
9	$ABC + A\bar{B}\bar{C}$	2	1	4
10	$AB + \bar{A}\bar{B}C$	4	4	8
11	$AB + BC + \bar{A}\bar{B}\bar{C}$	4	3	8
12	$ABC + \bar{A}\bar{B}C + \bar{A}B\bar{C} + AB\bar{C}$	2	0	4
13	$AB\bar{C} + \bar{A}BC + \bar{A}\bar{B}\bar{C}$	5	4	10
14	Total	30	22	60

Table 2: Implementation of 13 logical expressions using SKV-QCA gate.

2.5 Adder Designs Using SKV-QCA

By the extensive literature review that we have performed on the reversible circuits and QCA, we have realized the need of the optimized designs of the reversible circuits of the Half-Adder and the Full-Adder circuits in the Quantum Dot Cellular Automata. Adders are the main logic components of the various digital circuits that comprise of the microprocessors, DSP Processors and the filter circuits. The overall design performance of the systems depends on the functionalities of the components that is the adders that are incorporated in it. So the design of the adders has been used as the test benches for the evaluation of the functionalities and performance of the proposed gate SKV-QCA.

2.5.1 Half Adder Design Using SKV-QCA

The SKV-QCA has been designed in the manner that the design of the various logic circuits by the use of SKV-QCA uses minimum number of gates. The half-adder design thus uses only one SKV-QCA gate for its realization with the input C maintained at a

constant 0. The output P gives the sum and the output R gives the carry while the output Q acts as a garbage output.

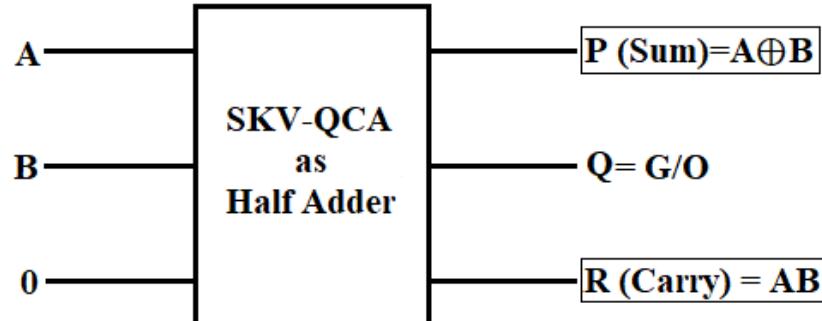


Figure 2.11: SKV-QCA as Half Adder.

Table 3: Truth Table of Half Adder

A	B	Sum	Carry
0	0	0	0
0	1	1	0
1	0	1	0
1	1	0	1

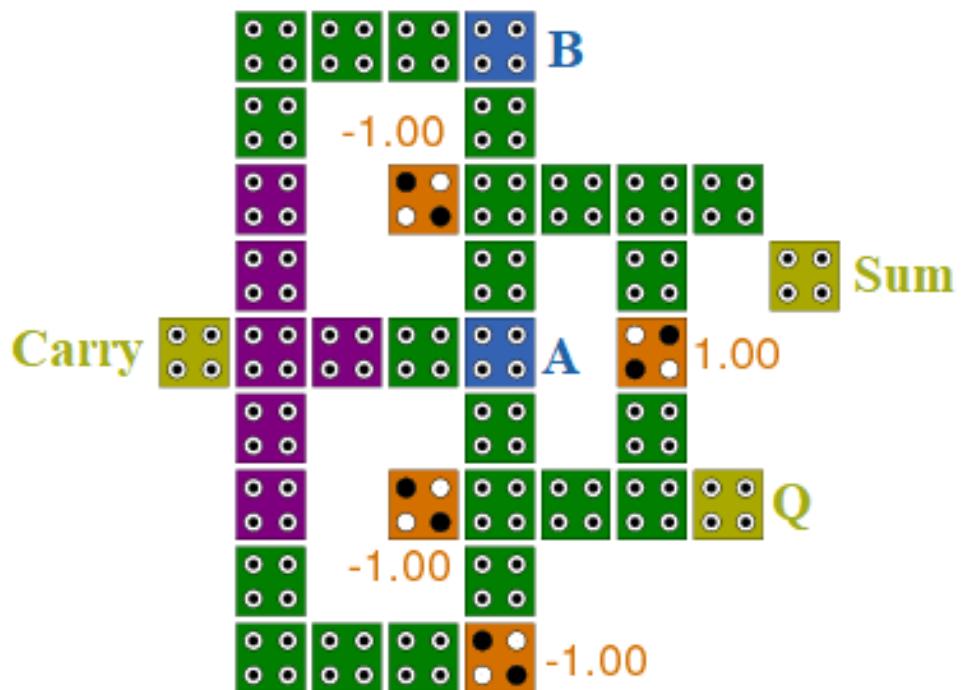


Figure 2.12: QCA implementation of SKV-QCA gate as Half Adder

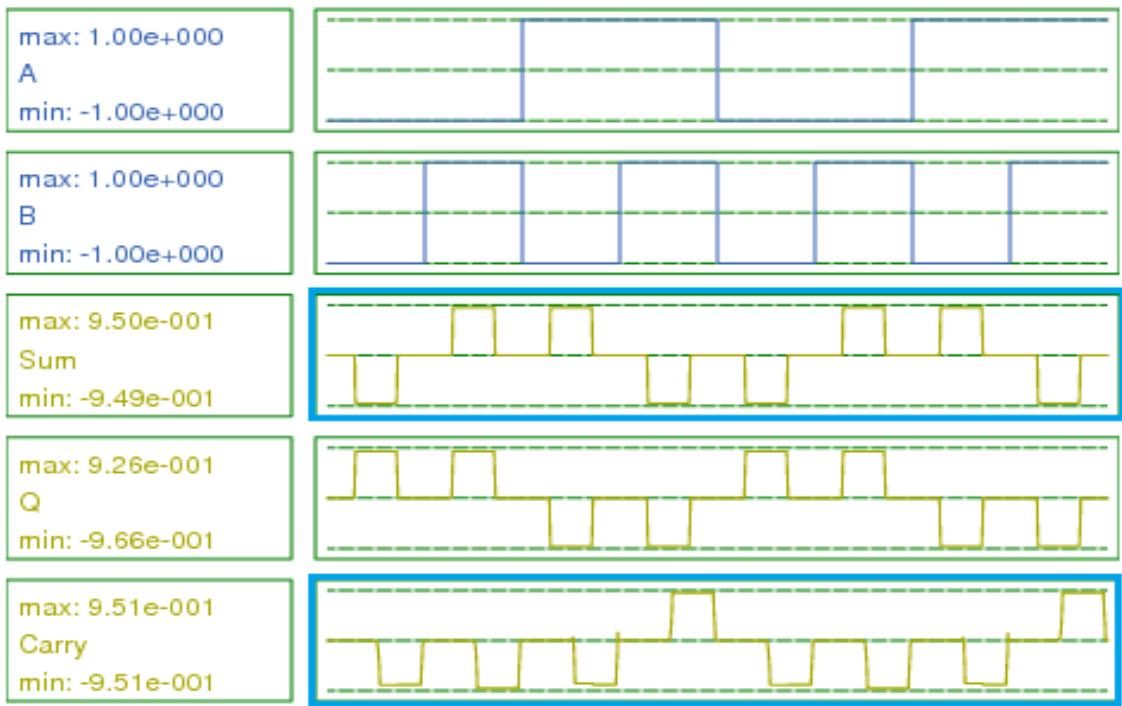


Figure 2.13: Simulation results for QCA implementation of SKV-QCA gate as Half Adder

Reversible Parameters:

Gate Count = 1

Constant Input = 1

Garbage Output = 1

Calculation of QCA Parameters

I. Cell Count: 37 Cells.

$$\text{II. Cell Area} = \frac{\text{No. of cells} \times \text{Dimension of the cell}}{10^6} \mu\text{m}^2$$

$$= \frac{37 \times 18 \times 18}{10^6} \mu\text{m}^2$$

$$= 0.01198 \mu\text{m}^2$$

$$\text{III. Total Area} = \frac{\text{Horizontal cells} \times \text{Vertical Cells} \times \text{Dimension of the cell}}{10^6} \mu\text{m}^2$$

$$= \frac{9 \times 9 \times 18 \times 18}{10^6} \mu\text{m}^2$$

$$= 0.02624 \mu\text{m}^2$$

IV. Latency = 0.5

V. Complexity = 0 Crossover used

2.5.2 Full-Adder Circuit Design using SKV-QCA Gate

For the design implementation of a Full Adder circuit two SKV-QCA gates are required. This leads us to a result that gives us 3-garbage outputs and needs no constant input. The first SKV-QCA produces one garbage output while the second SKV-QCA gate produces two garbage outputs using no constant input. The following shows the block diagram representation of full adder using SKV-QCA gate, its implemented design in the QCA nanotechnology and the simulation results which can be verified from the truth table for full adder given in table 4.

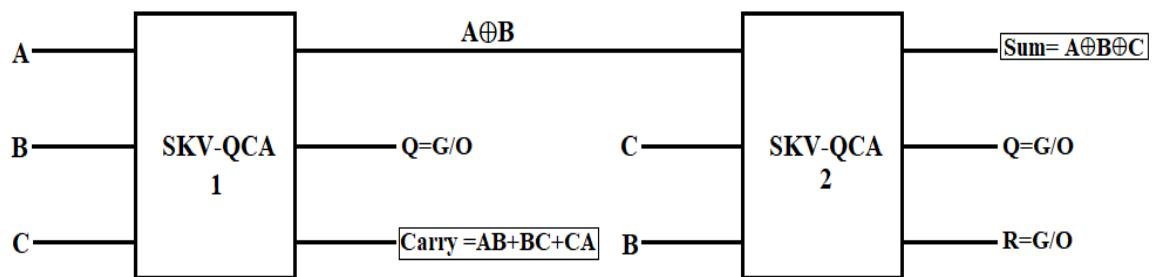


Figure 2.14: Block diagram representation for Full Adder using SKV-QCA gate

Table 4: Truth table for full adder

A	B	C	Sum	Carry
0	0	0	0	0
0	0	1	1	0
0	1	0	1	0
0	1	1	0	1
1	0	0	1	0
1	0	1	0	1
1	1	0	0	1
1	1	1	1	1

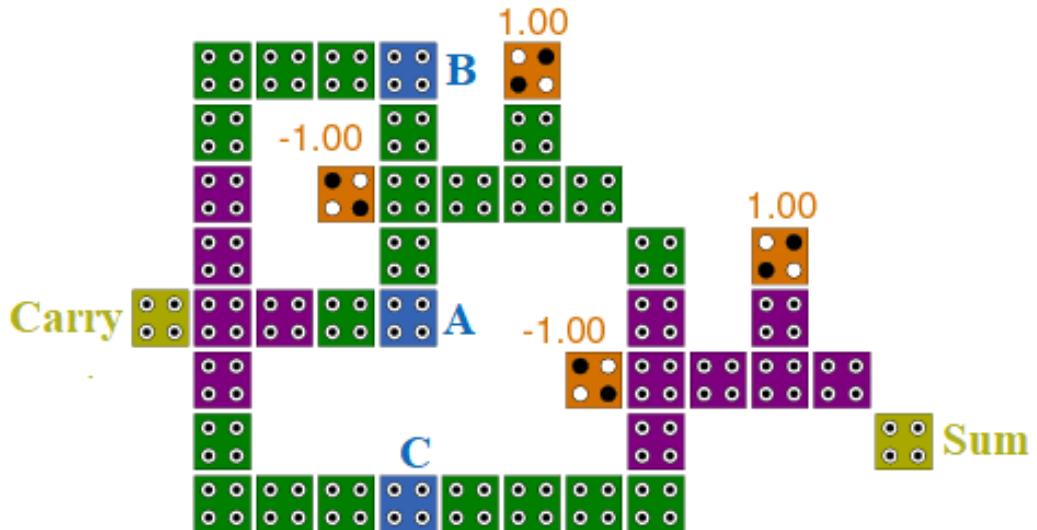


Figure 2.15: QCA implementation of reversible full adder using SKV-QCA gate

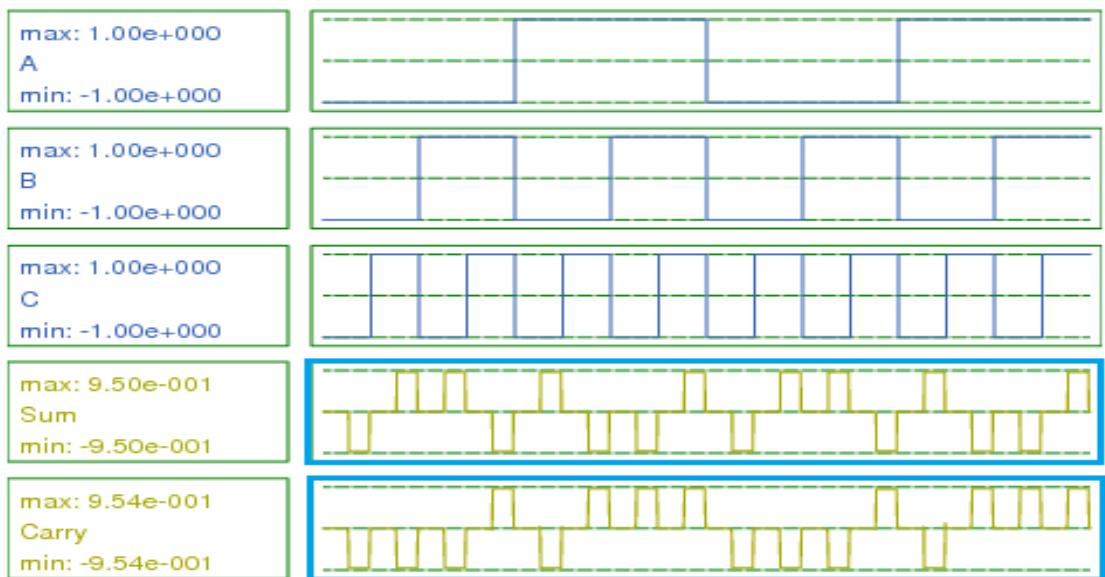


Figure 2.16: Simulation results for full adder using SKV-QCA gate.

Reversible Parameters:

Gate Count = 2

Constant Input = 0

Garbage Output = 3

Calculation of QCA Parameters

I. Cell Count: 42 Cells.

$$\begin{aligned}
 \text{II. Cell Area} &= \frac{\text{No. of cells} \times \text{Dimension of the cell}}{10^6} \mu\text{m}^2 \\
 &= \frac{42 \times 18 \times 18}{10^6} \mu\text{m}^2 \\
 &= 0.013608 \mu\text{m}^2
 \end{aligned}$$

$$\begin{aligned}\text{III. Total Area} &= \frac{\text{Horizontal cells} \times \text{Vertical Cells} \times \text{Dimension of the cell}}{10^6} \mu\text{m}^2 \\ &= \frac{12 \times 8 \times 18 \times 18}{10^6} \mu\text{m}^2 \\ &= 0.031104 \mu\text{m}^2\end{aligned}$$

IV. Latency = 0.5

V. Complexity = 0 Crossover used

Chapter 3

Results and Discussions

The design and implementation of the proposed reversible gate, fault tolerant gate and the adder circuits is verified through the simulation in the QCA designer tool 2.0.3. The design of the circuit is done by the use of best approach by using minimum number of cells possible for the design. Using these techniques, we have been able to optimize various parameters such as the cell count, cell area and the total area of the design and hence have successfully achieved better designs than the present designs in the literature. Most of the simulations have been done by using the bi-stable approximation engine in the QCA designer tool in which each cell is modelled as a simple two-state system. Some of the details about the QCA designer tool have been given in the section below.

3.1 Proposed SKV-QCA Simulation Results

The proposed SKV-QCA was simulated in QCA designer 2.0.3 to verify the correct working and reversibility according to the truth table of the gate. The desired results verifying the truth table are highlighted in the graph below:

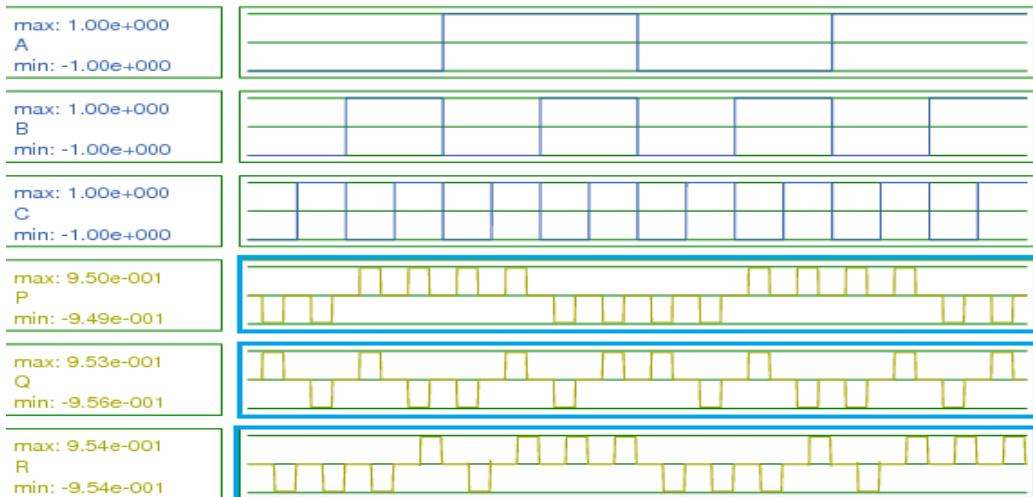


Figure 3.1: Simulation Result for proposed SKV-QCA gate.

To prove the functionality of the SKV-QCA gate, the universality of the gate is proved in chapter 4. It is seen that SKV-QCA can be modified to act as any gate by manipulating the inputs of the proposed gate. Further the reversible parameters of SKV-

QCA as universal gate are also found to be optimum with reduced garbage values and ancilla inputs. The results of the simulation using the QCA Designer 2.0.3 were found to be in according with the truth table of the proposed gate.

SKV-QCA as NOT Gate

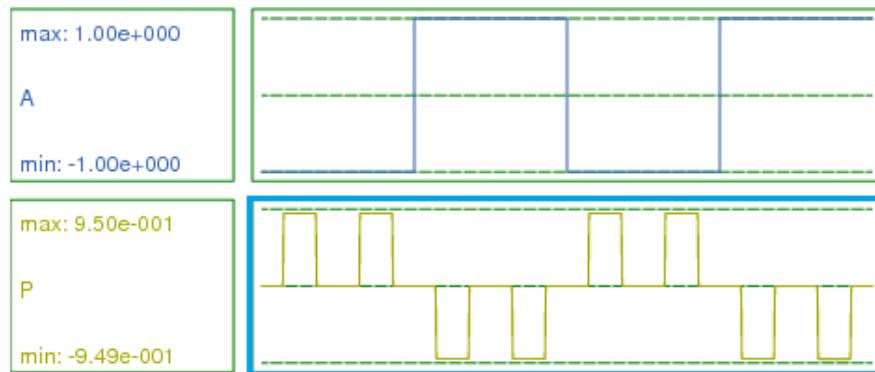


Figure 3.2: Simulation Results of SKV-QCA as NOT Gate

The highlighted portion of the graph shows the inversion of input A being achieved at P.

SKV-QCA as AND Gate

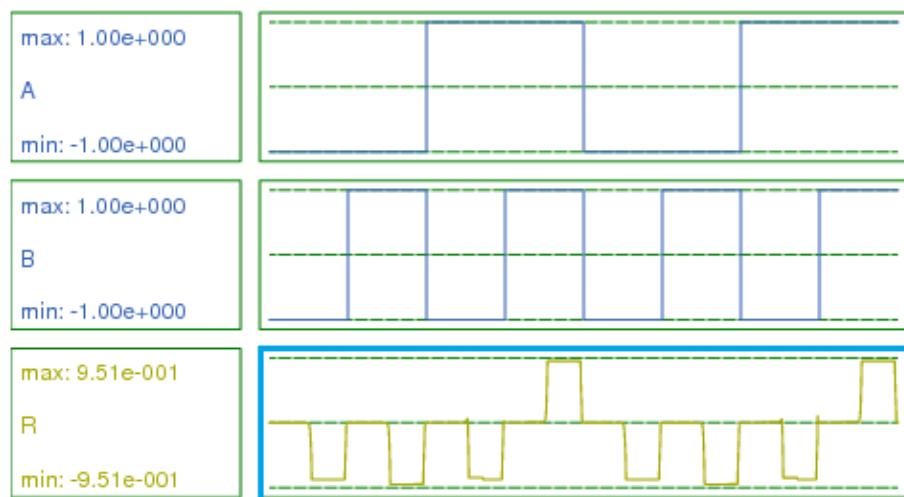


Figure 3.3: Simulation Results of SKV-QCA as AND Gate

SKV-QCA as NAND Gate

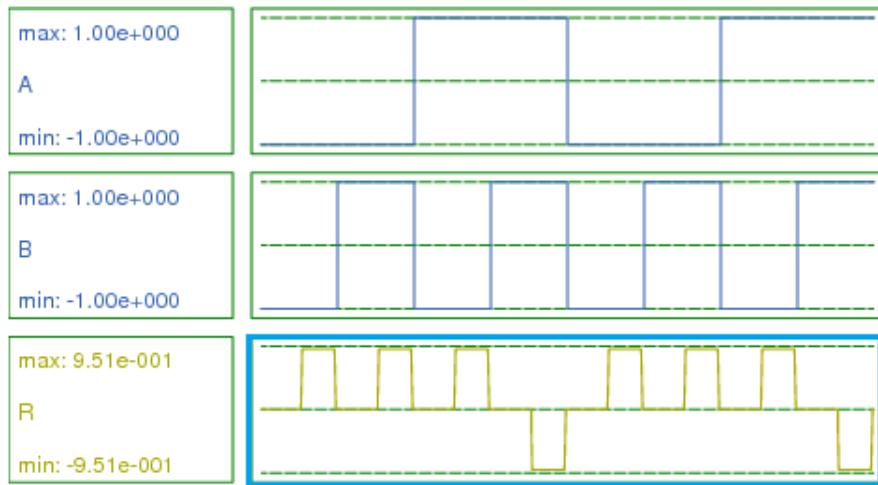


Figure 3.4: Simulation Results of SKV-QCA as NAND Gate

The desired output (AB)' which represents the equation of a NAND Gate is obtained at the output Q.

SKV-QCA as OR Gate

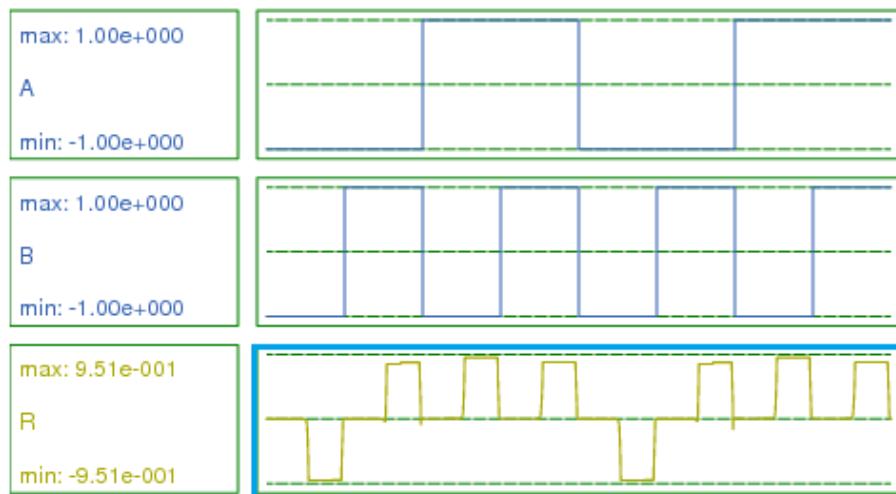


Figure 3.5: Simulation Results of SKV-QCA as OR Gate

SKV-QCA as NOR Gate

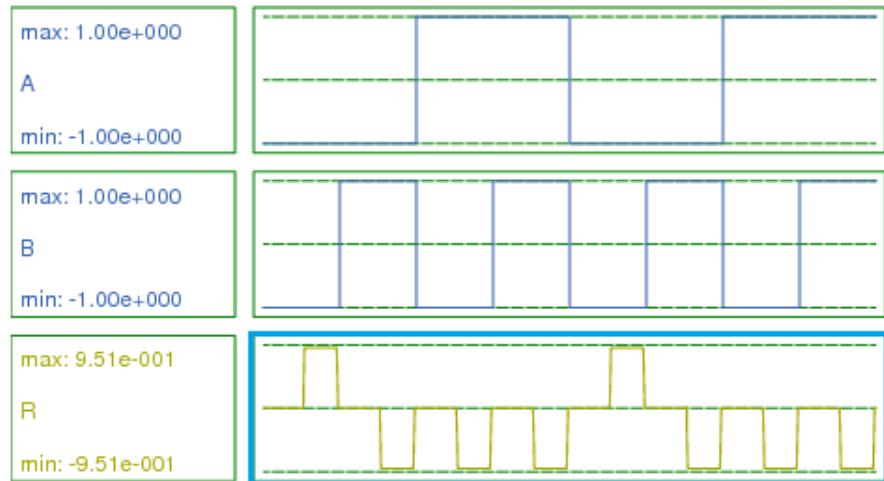


Figure 3.6: Simulation Results of SKV-QCA as NOR Gate

The highlighted portion of the graph shows the logic of NOR Gate at output R.

SKV-QCA as XOR Gate

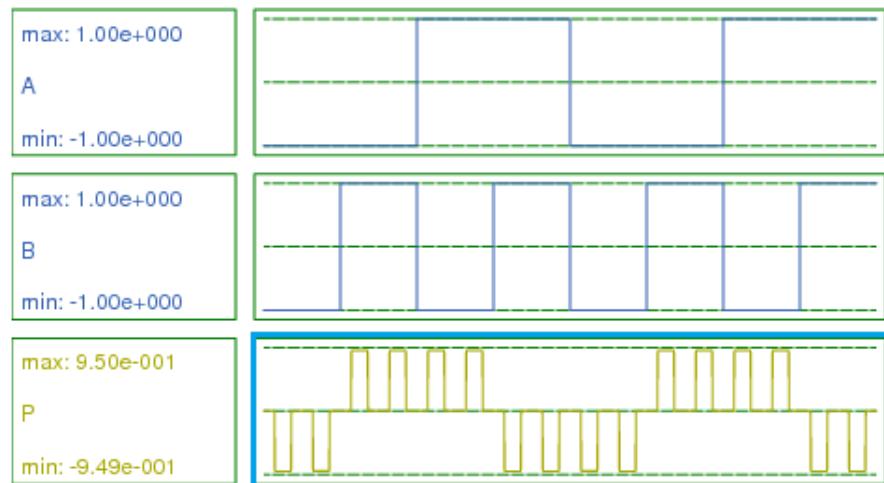


Figure 3.7: Simulation Results of SKV-QCA as E-XOR Gate

SKV-QCA as XNOR Gate

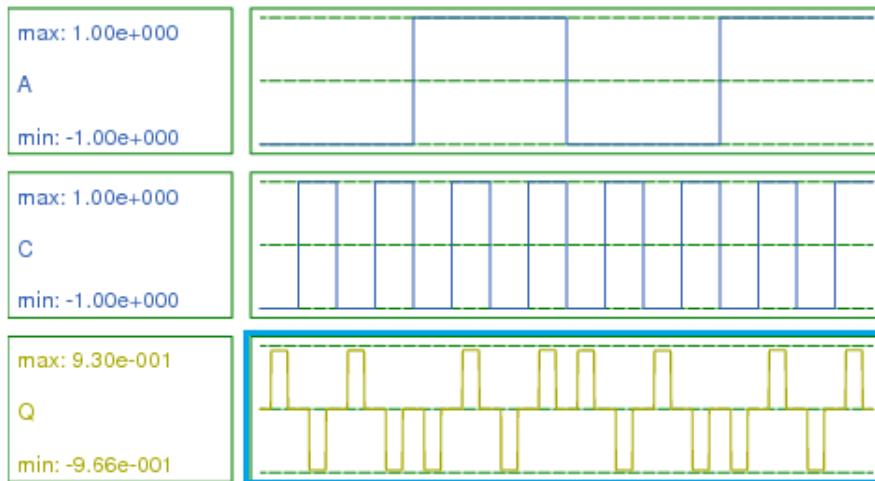


Figure 3.8: Simulation Results of SKV-QCA as EX-NOR Gate

3.2 Half and Full Adder Simulation

The efficiency of the gate can be calculated by the various circuits that can be implemented using the particular gate. The half adder circuit was simulated using bi-stable engine. The outputs of the half adder and full adder are verified by the simulations

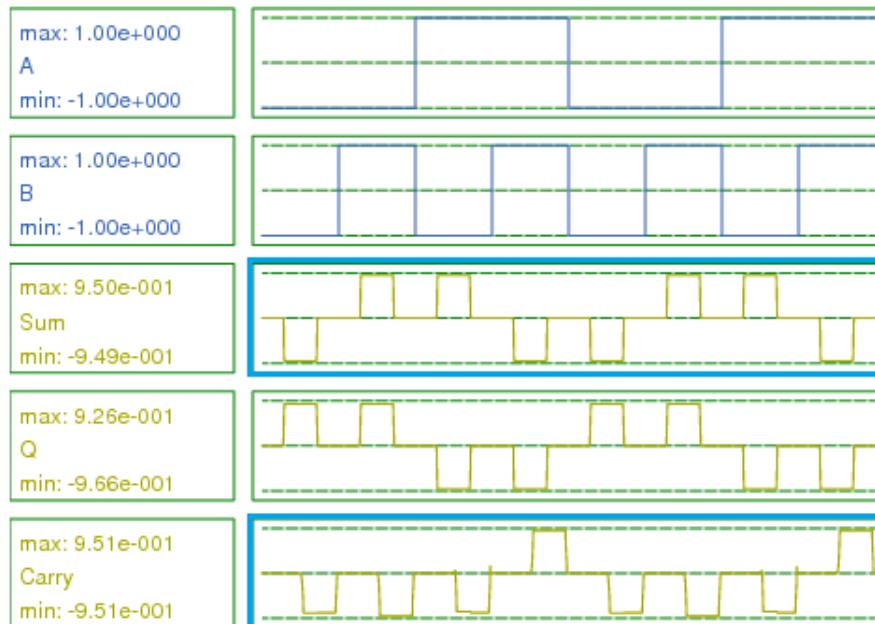


Figure 3.9: Simulation Results of Half Adder using SKV-QCA

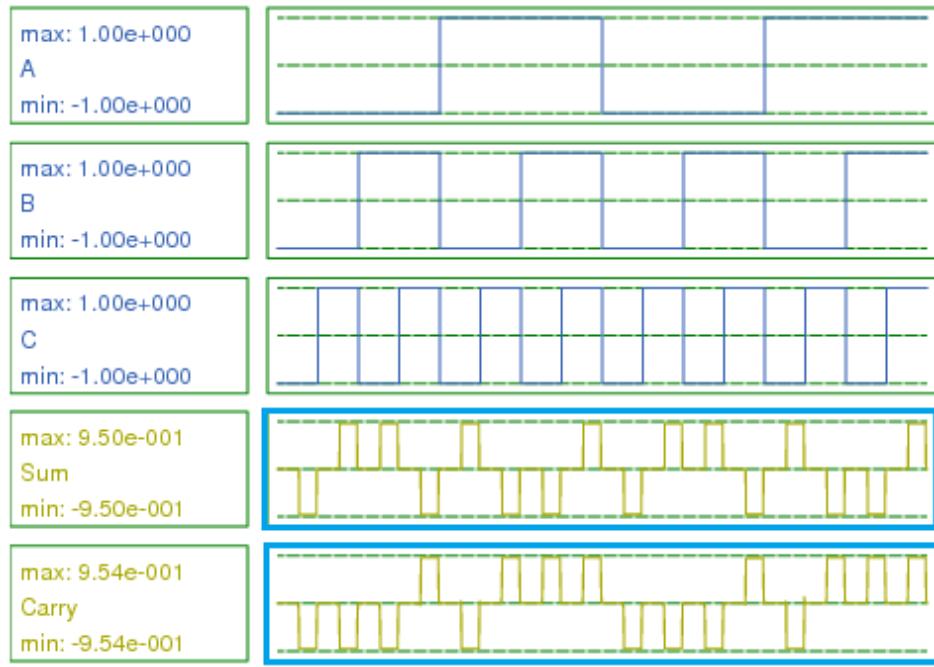


Figure 3.10: Simulation Results of Full Adder using SKV-QCA

3.3 Power Dissipation Analysis.

The proposed designs have been tested for power dissipation [28], at temp =2K, for the kink energy values of 0.5,1 and 1.5. The power dissipation maps are shown below for respective designs.

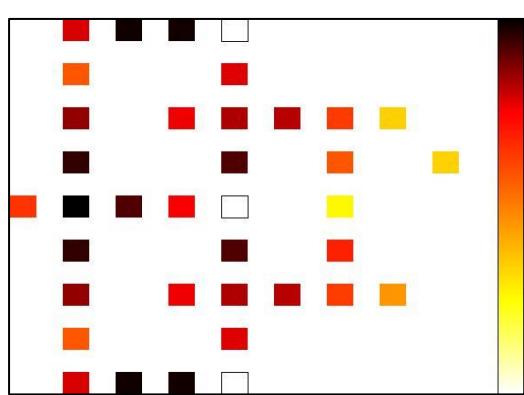


Figure 3.11 Heat map of SKV-QCA at 0.5 Ek

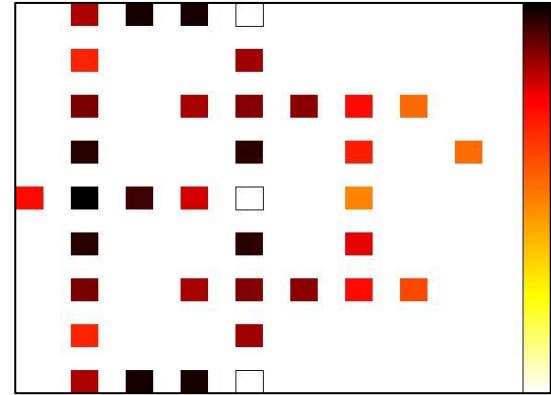


Figure 3.12 Heat map of SKV-QCA at 1 Ek

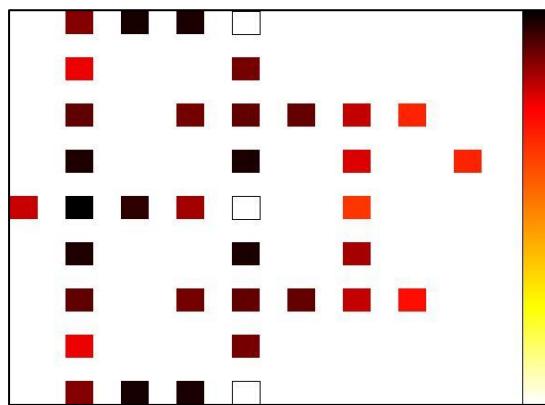


Figure 3.13: Heat map of SKV-QCA at 1.5 E_k

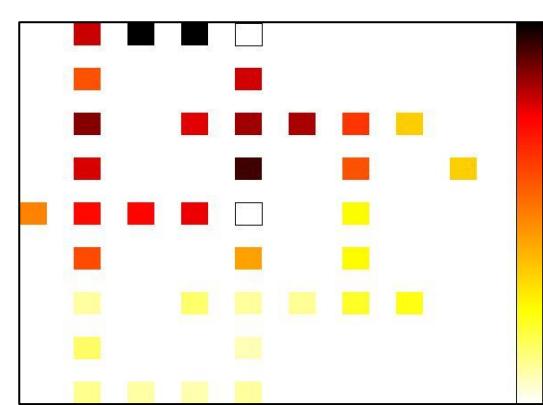


Figure 3.14: Heat map of half adder at 0.5 E_k

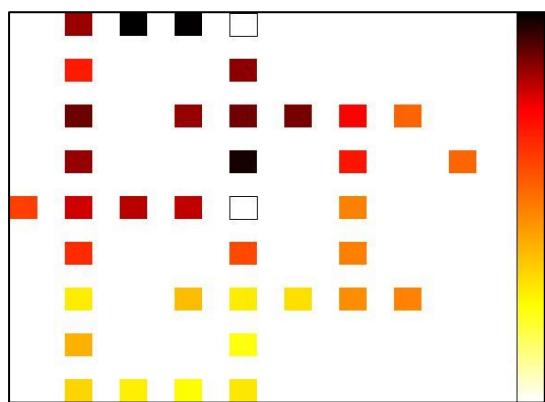


Figure 3.15: Heat map of half adder at 1 E_k

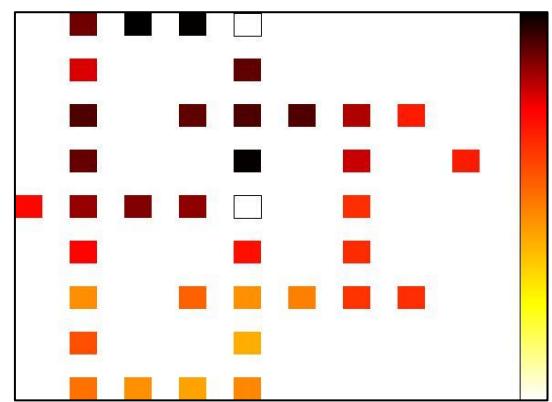


Figure 3.16: Heat map of half adder at 1.5 E_k

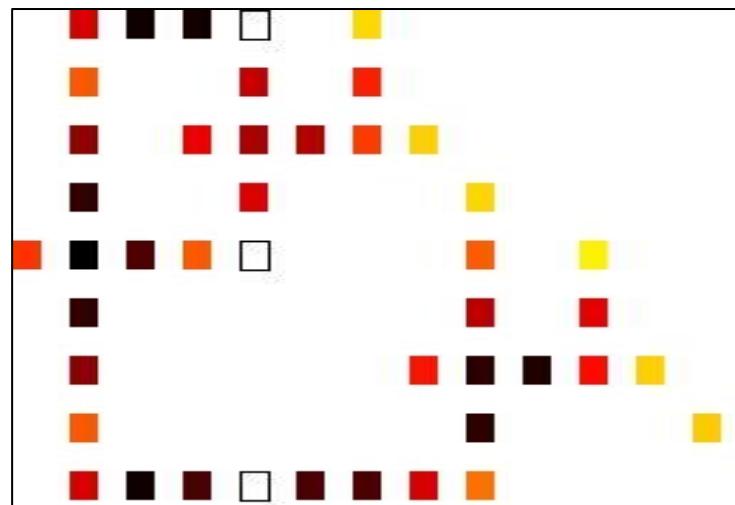


Figure 3.17: Heat map of full adder using SKV-QCA at 0 E_k

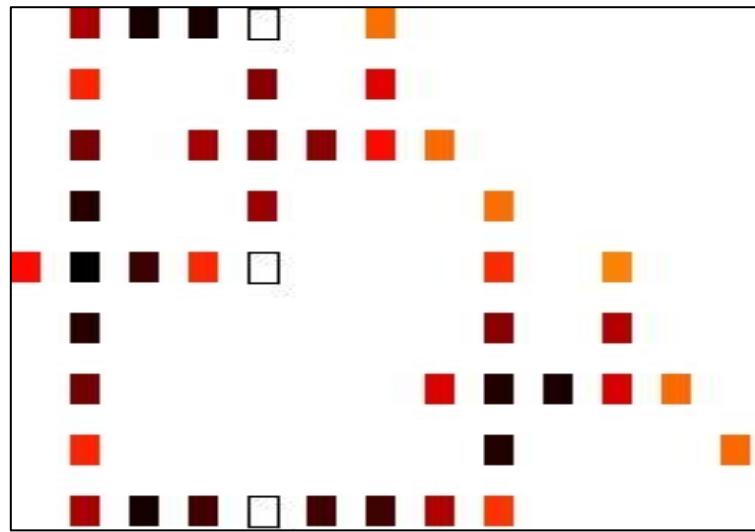


Figure 3.18: Heat map of full adder using SKV-QCA at 1 Ek

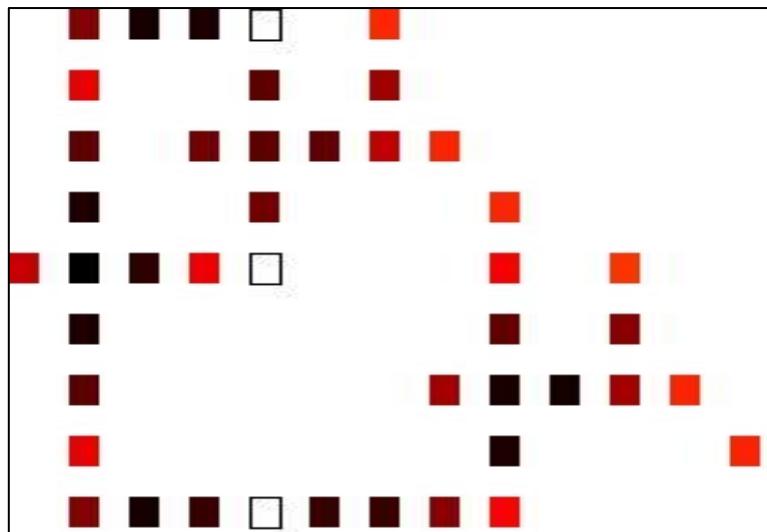


Figure 3.19: Heat map of full adder using SKV-QCA at 1.5 Ek.

Chapter 4

State of Art Comparison

In this chapter we have presented the comparison of the already existing 3*3 reversible universal gates available with the proposed SKV-QCA universal reversible gate. The comparison is based on the parameters that are deemed highly pertinent to defining the efficiency of the QCA reversible universal gates. Table 5 compares the novel 3*3 reversible gate SKV-QCA with the existing 3*3 gates in the literature[29-34]. The parameters of the proposed gate are found to be optimal and thus SKV-QCA is better gate for circuit designing in QCA technology.

Table 5: Comparison of SKV-QCA with existing 3*3 Reversible Gates

S. No	Parameter	Fredkin gate	RUG	PPRG	MX- CQCA	R- CQCA	RG- QCA	Proposed SKV-QCA
1	N_{MVG}	6	7	6	5	6	4	1
2	N_{INV}	8	2	6	0	9	2	0
3	Cell Count	246	211	171	218	177	143	37
4	Cell Area (μm^2)	0.079	0.068	0.055	0.070	0.057	0.046	0.01198
5	Total Area (μm^2)	0.37	0.27	0.19	0.35	0.24	0.14	0.02624
6	Latency	4	3	3	-	2.25	1.75	0.5
7	Area Delay Product	1.48	0.81	0.57	-	0.54	0.245	0.01213
8	Area Usage (%)	21.35	25.18	28.94	20	23.47	32.84	45.6

Since full adder circuit is designated as a benchmark for the determination of the efficiency of the reversible universal gates owing to their presence in almost every electronic device, we have presented a comparison of the design of the full adder circuit using the proposed SKV-QCA gate with the already existing full adders available in the literature[]. The table 6 shows the comparison results of the full adder circuit using the SKV- QCA Gate with the existing full adder circuits using different gates. It is seen that the adder designed using the SKV-QCA uses only two gates and optimizes the circuit in terms of almost all parameters.

Table 6: Comparison of Full Adder Using SKV-QCA with Existing Designs

S. No	Paramter	Fredkin Gate	Toffoli Gate	QCA 1	RUG	PPRG	RQCA	RG-QCA	Proposed SKV-QCA
1	Gate Count	5	4	3	2	3	3	2	2
2	Cell Count	955	672	438	594	513	582	375	42
3	Cell Area μm^2	0.309	0.2177	0.141	0.192	0.166	0.188	0.121	0.0136 08
4	Total Area μm^2	1.85	1.48	0.48	0.92	0.57	-	0.37	0.0311 04
5	Area Utilization (%)	16.7	14.7	29.56	20.91	29.13	-	32.83	43.75

Table 7 enlists the power dissipation values of various reversible gates, as is evident from the table [28], [30], [33], [34], [35]; SKV-QCA is the most efficient of all these.

Table 7: Power dissipation comparison of reversible gates

Structure	Average Leakage Energy dissipation (eV)			Average Switching Energy Dissipation (eV)			Total Energy Dissipation (eV)		
	0.5E _k	1E _k	1.5E _k	0.5E _k	1E _k	1.5E _k	0.5E _k	1E _k	1.5E _k
PRG [24]	0.042	0.131	0.237	0.227	0.197	0.168	0.269	0.328	0.405
RM [23]	0.117	0.318	0.534	0.309	0.251	0.205	0.426	0.569	0.739
Fredkin[19]	0.101	0.283	0.482	0.213	0.175	0.143	0.314	0.458	0.625
SKV-QCA	0.01117	0.03281	0.05807	0.05390	0.04695	0.04027	0.06507	0.07976	0.09834

Chapter 5

Conclusion and Future Scope

5.1 Conclusion

This dissertation discusses the possible alternatives to overcome the limitations faced by the CMOS technology. The focus of this dissertation is on two main paradigms namely Reversible Logic and Quantum dot Cellular Automata Nanotechnology. The basics of both the paradigms have been discussed in detail which is followed by the literature survey of the various reversible and the irreversible gates that are present in the literature. A new 3*3 reversible logic gate has been proposed in the dissertation which has universal functionalities that is all the 13 standard functions can be implemented using the proposed gate named SKV-QCA Gate.. The performance of both the SKV-QCA gate has been tested using the adder circuit test benches. The adder circuits designed using the SKV-QCA gate are found to be optimal and efficient as compared to the other adder circuits present in the literature. It is concluded that the proposed designs are optimal for design of various digital circuits.

5.2 Future Scope

In the dissertation the two paradigms that are discussed are new and in the pre- mature phase. Thus a huge scope lies in the research and development of these two paradigms, so as to take the digital designs to a commercial level[36],[37]. The future work may include the use of the proposed design for implementation of larger complex circuits such as multipliers and ALU's. There is a scope to explore new topologies for design in QCA Nano-technology[38]. The power analysis of the QCA designs can be performed and compared with the other designs such as C-MOS technology. Molecular QCA that shows the performance analysis at the room temperature is also a budding area of research. Research can be done on the lagging parts of the technology such as reading the outputs of the system. Further the designs with least cell count need research and innovation. The proposition of better fabrication techniques is also an area that remains under explored and needs huge efforts in research so as to develop easily affordable chips so as to develop faster, adroit and economically viable gadgets and computers[39].