Technical Product Description
SMI230

Inertial Sensor (6DoF) for Non-Safety Automotive Applications

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1 Product identification

- Product Designation: SMI230
- Type Designation: Inertial Sensor
- Product Part Number: 0273 142 144
- This Product is intended for use in: Non-Safety Automotive Applications

Main Functions and Properties

1.1 The SMI230 is a combined triaxial accelerometer (ACC) and triaxial gyroscope (GYR) for non-safety related applications, e.g. for in-dash navigation in the passenger compartment. Within one package, the SMI230 offers the detection of acceleration and angular rate for the x-, y-, and z-axis. The digital standard serial peripheral interface (SPI) of the SMI230 allows for bi-directional data transmission. To increase flexibility, both gyroscope and accelerometer can be operated individually, but can also be tied together for data synchronization purposes.

Key Features

1.2

Key Feature	Description
2 inertial sensors in one device	Advanced triaxial 16 bit gyroscope and a versatile, leading edge triaxial 16 bit accelerometer for reduced PCB space and simplified signal routing
Small package	LGA, 16 pins, footprint 3.0 x 4.5 mm², height 0.95 mm
Common voltage supplies	VDD voltage range: 2.4 ... 3.6 V
Digital interface	SPI, TWI (compatible with I^2C)
Smart operation and integration	Gyroscope and accelerometer can be operated individually or synchronized
Consumer electronics suite	MSL1, RoHS compliant, halogen-free
Operating temperature	-40 ... +105 °C
Programmable functionality	Acceleration and rate ranges selectable Low-pass filter bandwidths selectable
On-chip temperature sensor	-104 °C ... 150 °C factory trimmed, 11 bit, typical

Provided that SMI230 is used within the conditions (environment, application, installation, loads) as described in this TCD and the corresponding agreed upon documents, Bosch ensures that the product complies with the agreed properties. Agreements beyond this require the written approval from Bosch. The product is considered fit for the intended use when the product successfully has passed the tests in accordance with the TCD and agreed upon documents.

It is the responsibility of the customer to ensure the proper application of the product in the overall system/vehicle.

Bosch does not assume any responsibility for changes to the environment of the product that deviate from the TCD and the agreed upon documents as well all applications not released by Bosch.

2 General product description

Mechanical Design

The inertial sensor SMI230 is based upon a combined two-chip stacked concept. The accelerometer and gyroscope sensing parts consist of sensitive micro-mechanical sensing elements (MEMS) mounted side-by-side on the PCB. The read out ASICs are stacked on top of the respective sensing elements. All of these elements are packed in one LGA package.

2.1

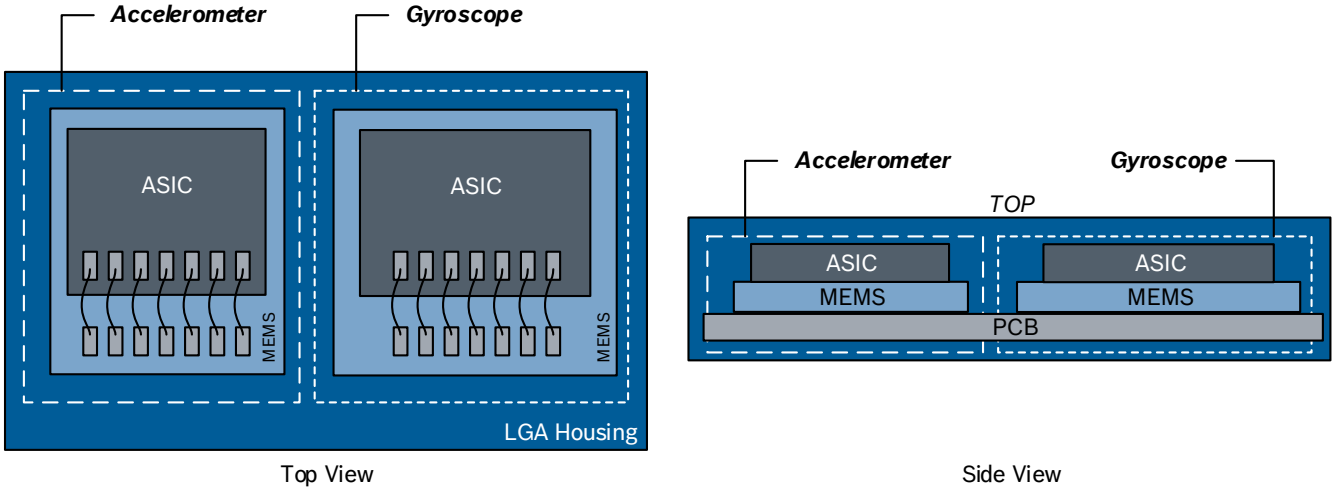


Figure 1 Schematics of the SMI230 mechanical design (left: top view; right: side view)

2.2 Sensor Data

The data width of the gyroscope and accelerometer sensor is 16 bits (11 bits for the temperature sensor) given in two´s complement representation.

The bits for each axis are split into an MSB upper part and an LSB lower part. Reading the sensor data registers always starts with the LSB part. In order to ensure the integrity of the sensor data, the content of the MSB register is locked by reading the corresponding LSB register (shadowing procedure).

The **burst read access** mechanism provides an efficient way to read out the angular rate or acceleration data in TWI or SPI mode. During a burst read access, the sensor automatically increments the starting read address after each byte. The burst read access allows data to be transferred over the TWI bus with an up to 50 % reduced data density. The sensor data (angular rate or acceleration data) in all read-out registers is locked as long as the burst read access is active. Reading the sensor data registers of each gyroscope and accelerometer part in burst read access mode ensures that the sensor values in all readout registers belong to the same time stamp.

2.3

Block Diagram

Figure 2 shows the basic building blocks of the SMI230. As stated in Figure 2, the accelerometer and the gyroscope MEMS elements are each evaluated by their own ASIC. Both sensing elements detect voltage (V) variations, feeding into the analog-digital converter (ADC). The digital signals are further processed and accessible via SPI or TWI.

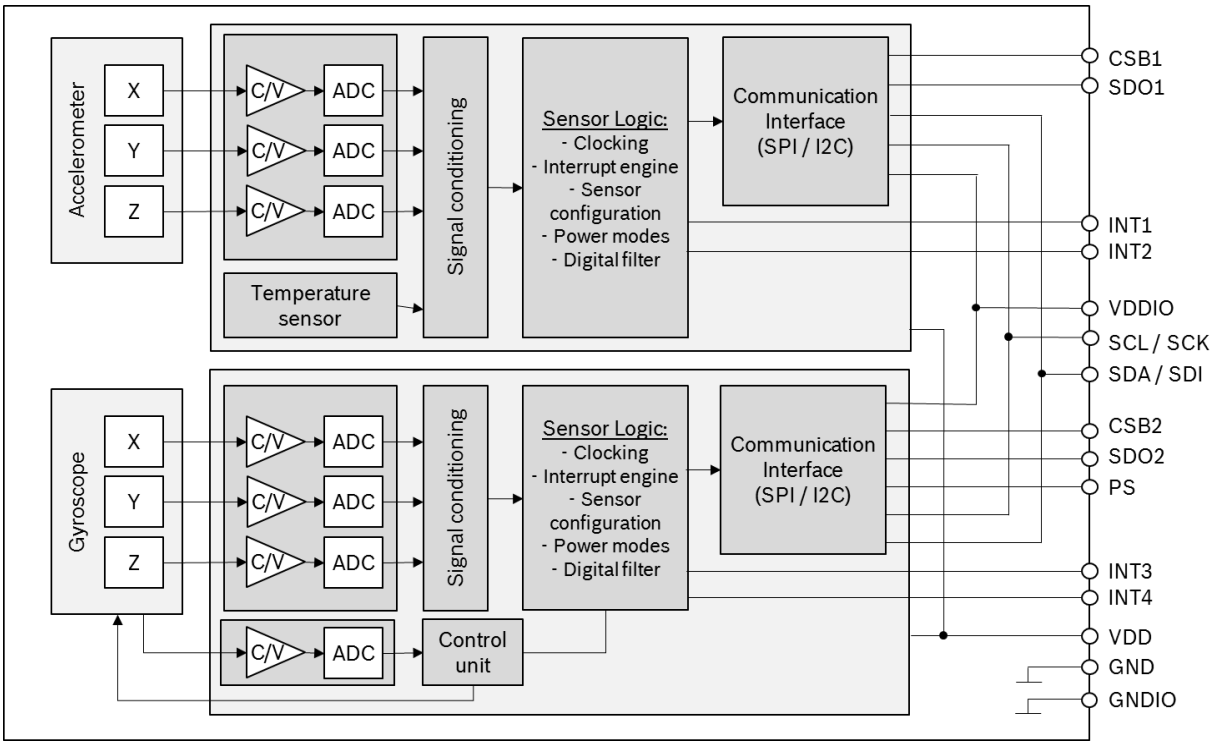


Figure 2 Simplified block diagram of the SMI230

2.4 Signal Path

2.4.1 Accelerometer

The accelerometer offers temperature and acceleration data for all three spatial dimensions. For the latter, the differential capacitance change (C) of the corresponding sensing element is detected. These signals correspond to the voltage (V) entering the hybrid algorithmic analog-digital-converter (ADC), translating the formerly analog signals into digital serial bit streams at a rate of 400 kHz. Then, the detected signal is translated into a data word of max. 16 bits and enters the digital signal processor (DSP).

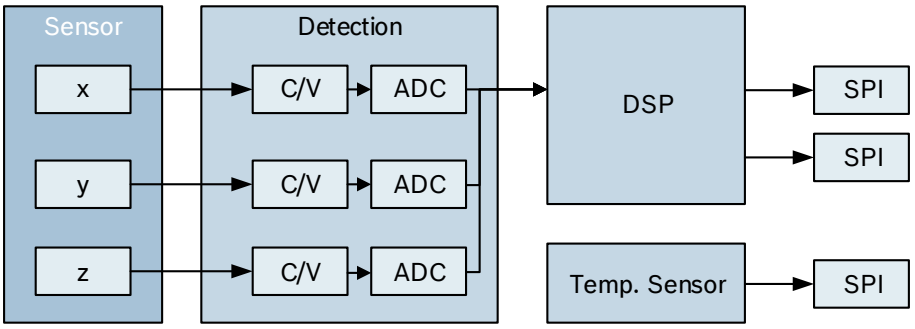


Figure 3 Simplified signal path of the accelerometer

Within the DSP (see Figure 4), the data is corrected for the analog-digital conversion as well as gain and offset. A low-pass filter provides an adjustable data bandwidth. Here, the sampling rate is directly connected with the selected bandwidth.

The low-pass filter can be bypassed so that unfiltered data is accessible.

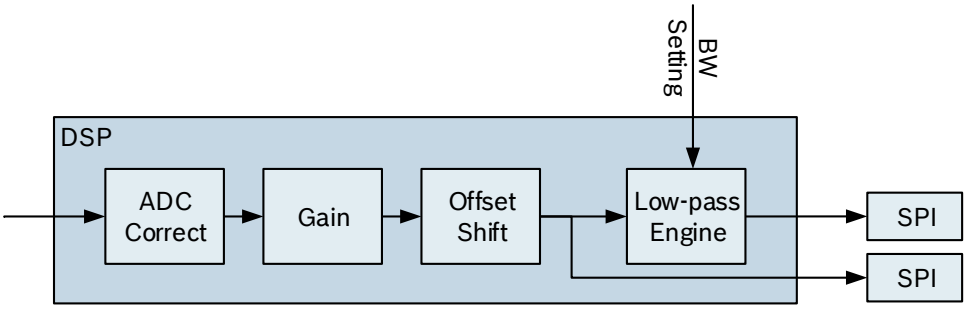


Figure 4 Simplified signal path of the accelerometer

2.4.2 Gyroscope

The signal path of the gyroscope is sketched in Figure 5. For proper data acquisition, five blocks are necessary for each rate axis, i.e., the drive, the (MEMS) sensor, the detection, the controller & demodulator, and the digital signal processor (DSP). In addition, a temperature signal is provided by the temperature sensor.

The drive is a closed-loop system that actively moves each sensor element at ~25 kHz.

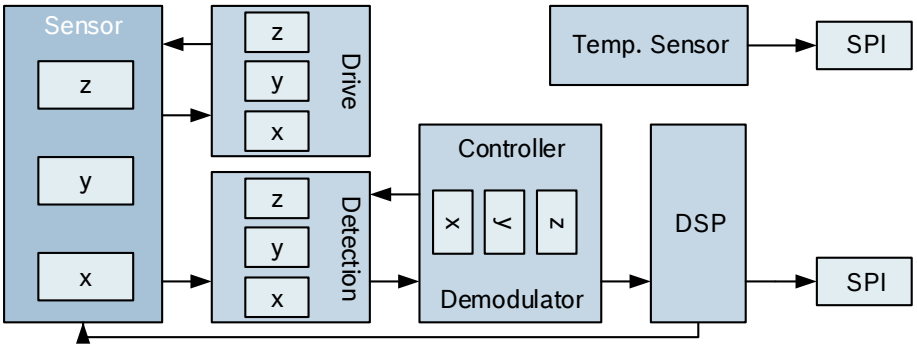


Figure 5 Simplified signal path of the gyroscope

Data acquisition is independent from the drive and the temperature sensor. A more detailed sketch of the signal path of one axis is given in Figure 6.

The block ‘Detection’ corresponds to the analog part of the SMI230. The differential capacitance change (C) of each sensing element corresponds to the rate data of the respective sensing axis. The latter corresponds to the voltage (V) entering the 25 kHz filter which is equal to the drive frequency. The 1-bit Σ/Δ-converter (ADC) translates the signal into a digital serial bit stream at a rate of 400 kHz.

This bit stream is fed into both the common mode controller and the demodulator. The first back-couples to ‘C/V’ in order to negate mass deviation of the sensor element. The latter demodulates the 25 kHz data signal which then enters the DSP.

In the DSP, the signal is both fed into the quadrature correction and the offset shift. Afterwards, it passes a fine gain block and low pass filter before being accessible via e.g. SPI.

The block ‘Quad. Corr.’ back-couples onto distinctive pads on the sensing element to compensate for possible deviations from the oscillation axis.

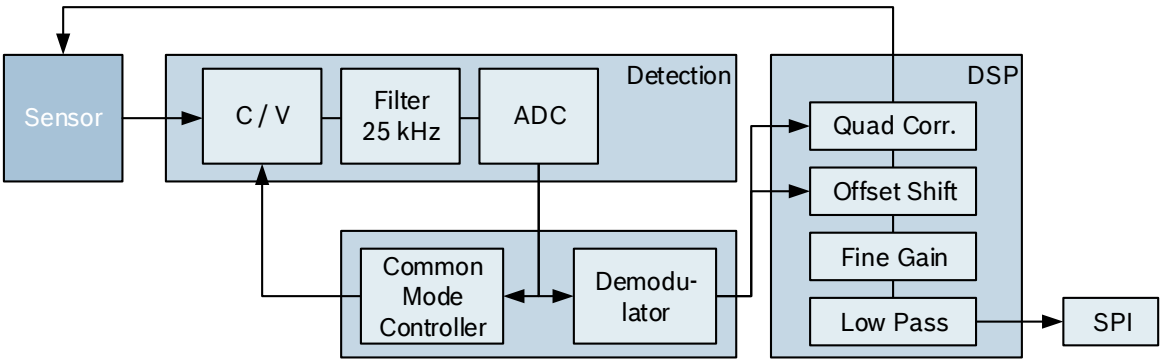


Figure 6 Path of the detection signal for one axis (gyroscope)

Orientation of the Sensing Axes

2.5

If the sensor is accelerated and/or rotated in the indicated directions, the corresponding channels of the device will deliver a positive acceleration and/or yaw rate signal (dynamic acceleration). If the sensor is at rest without any rotation, and the force of gravity is acting contrary to the indicated directions, the output of the corresponding acceleration channel will be positive and the output of the corresponding gyroscope channel will be 'zero' (static acceleration).

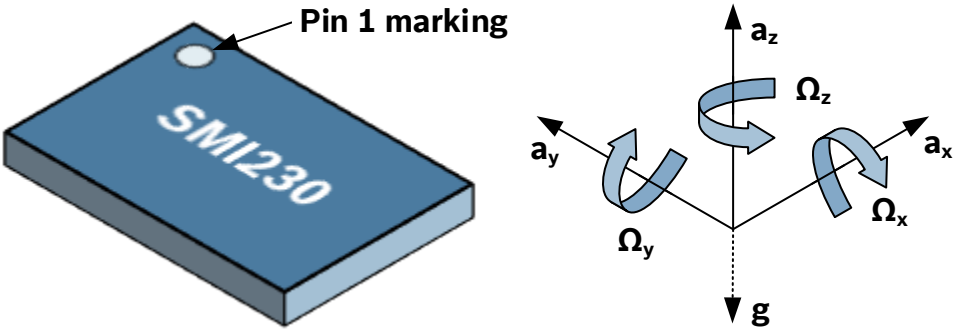
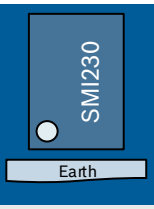
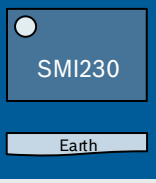
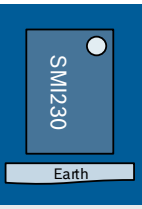


Figure 7 Sensing axis orientation

Example:
According to Figure 7, if the sensor is at rest, or at uniform motion in a gravity field, the output signals are:

- ±0 g for the ACC x-channel ±0 g for the GYR Ω_X-channel
- ±0 g for the ACC y-channel ±0 g for the GYR Ω_Y-channel
- +1 g for the ACC z-channel ±0 g for the GYR Ω_Z-channel

The table below lists all corresponding output signals of x, y, and z, and Ω_x, Ω_y, and Ω_z, while the sensor is at rest, or at uniform motion in a gravity field. This assumes a ±2 g accelerometer range setting and a top down gravity vector as shown above.

Sensor Orientation						
Output Signal x	0 0	+1 g +1024 LSB	0 0	-1 g -1024 LSB	0 0	0 0
Output Signal y	-1 g -1024 LSB	0 0	+1 g +1024 LSB	0 0	0 0	0 0
Output Signal z	0 0	0 0	0 0	0 0	+1 g +1024 LSB	-1 g -1024 LSB
Output Signal Ω_x	0 0	0 0	0 0	0 0	0 0	0 0
Output Signal Ω_y	0 0	0 0	0 0	0 0	0 0	0 0
Output Signal Ω_z	0 0	0 0	0 0	0 0	0 0	0 0

3 Hardware Interface Description and Packaging

3.1 Package Parameters

Parameter	Value	Unit
Width	3.00	mm
Length	4.50	mm
Height	0.95	mm
Weight	27.48	mg

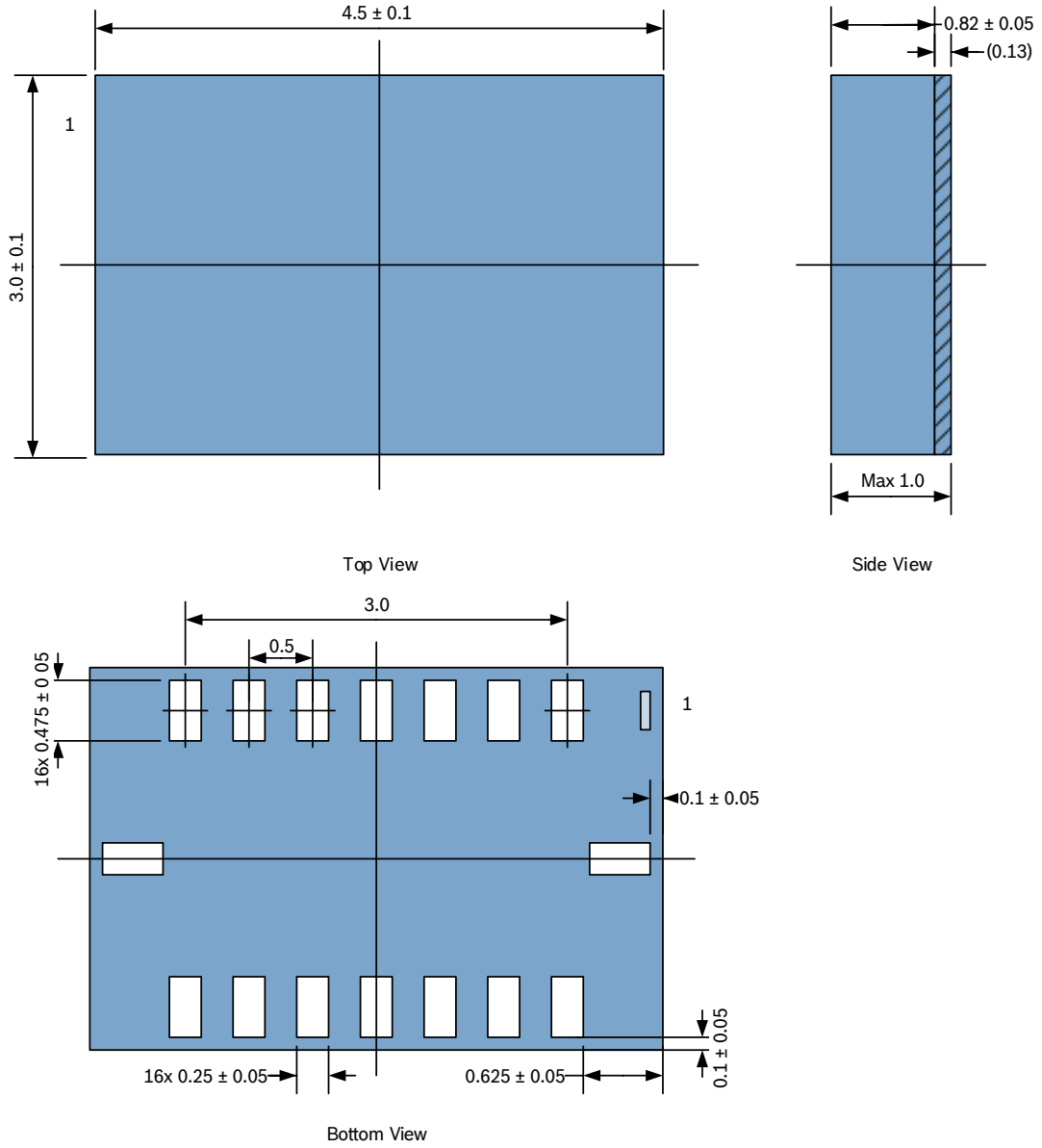


Figure 8 SMI230 package outline drawing

The dimensions are given in mm. Unless otherwise specified, the tolerance is ± 0.05 mm.

The SMI230 sensor meets the requirements of the EC restriction of hazardous substances (RoHS) directive, see also:

Directive 2002/95/EC of the European Parliament and of the Council of 27 January 2003 on the restriction of the use of certain hazardous substances in electrical and electronic equipment.

The sensor module is recyclable according to the norm WEEE - 2012/19/EU.

The sensor housing is a standard LGA package.

Halogen content:

The SMI230 is halogen-free. For more details on the analysis results, please contact your Bosch representative.

Transport Package

3.2.1 Tape on Reel Specification

The SMI230 is shipped in a standard cardboard box.

The box dimensions for one reel are L x W x H = 35 cm x 35 cm x 6 cm.
SMI230 quantity: 5000 pcs per reel. Please handle with care.

3.2

3.2.2 Tape Dimensions

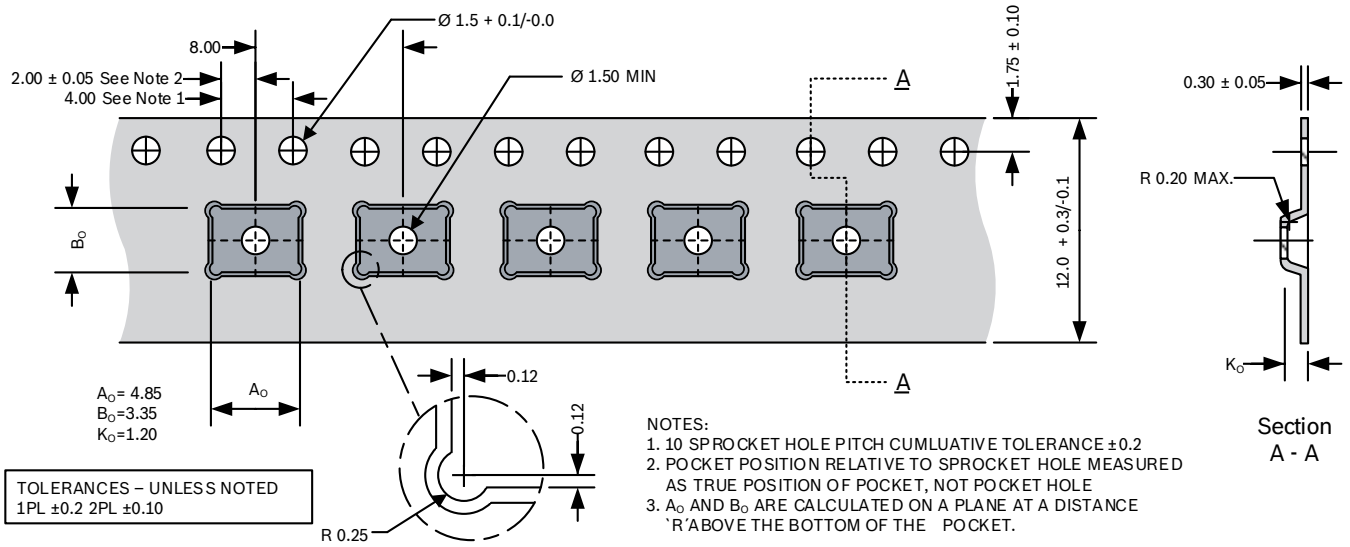


Figure 9 Tape dimensions in mm

3.2.3 Reel Dimensions

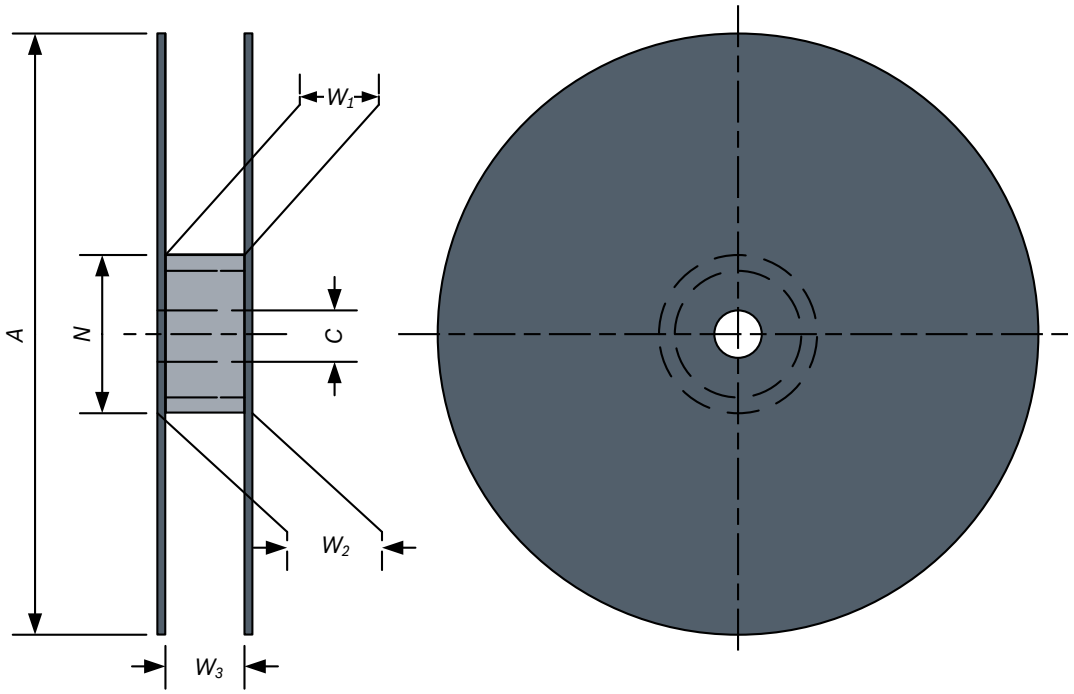


Figure 10 Reel dimensions

Parameter	Meaning	Dimensions [mm]
W (not depicted)	tape width	12
A	reel diameter	330
N	hub diameter	100
W_1	inner width of reel	12.4+2
W_2	total width of reel	18.4
W_3, min	inner width of reel, minimum	11.9
W_3, max	inner width of reel, maximum	15.4

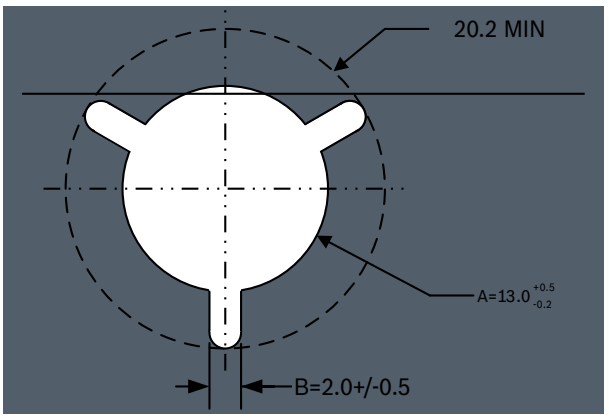


Figure 11 Details on hub hole dimension C in mm

3.2.4 Orientation within Reel

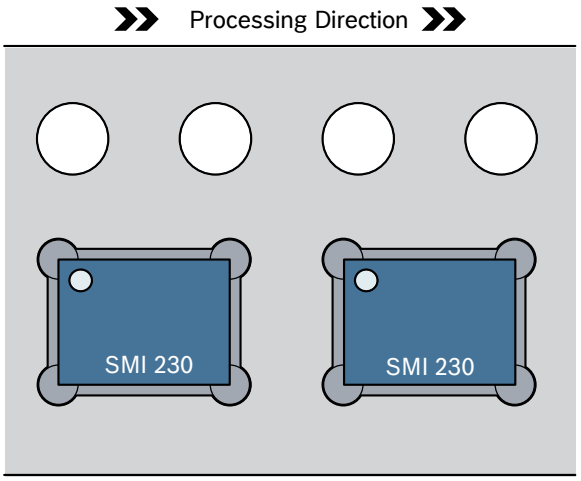


Figure 12 Orientation of the SMI230 devices relative to the tape

3.3 Labelling of the product

Labeling	Name	Symbol	Remark
	Product number	xxx	3 numeric digits, fixed to identify product type (“144”)
	Sub-con ID	A	1 alphanumeric digit, variable to identify sub-con
	Date code	YYWW	4 numeric digits, fixed to identify YY: “year”, WW: “working week”
	Counter ID	CCC	3 numeric digits, variable to generate trace-code
	Pin 1 identifier	●	--

3.4 Pinning

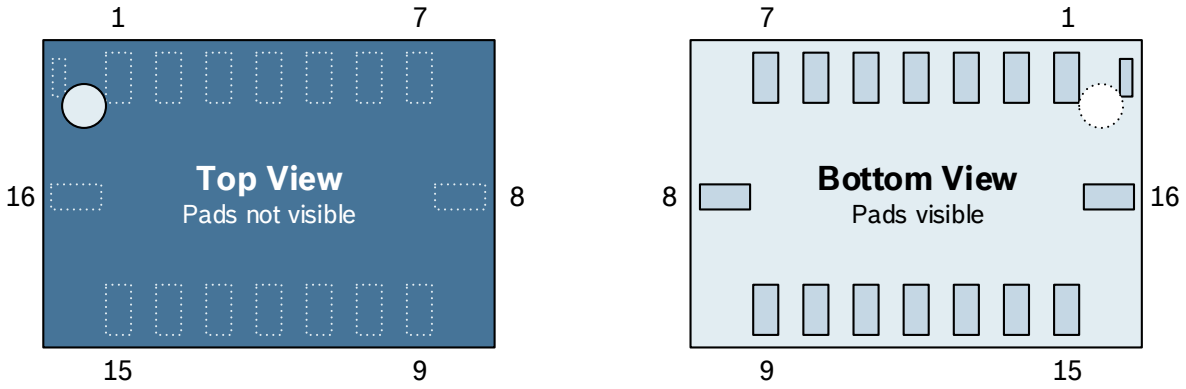


Figure 13 Pin-out top (left) and bottom (right) view

Pin	Name	I/O Type	Description	Connect to - SPI -	Connect to - TWI -
1	INT2	Digital I/O	Interrupt pin (ACC #2)	INT2 / DNC	INT2 / DNC
2	NC	--	--	GND	GND
3	VDD	Supply	Power supply analog & digital domain	VDD	VDD
4	GNDA	Ground	Ground for analog domain	GND	GND
5	CSB2	Digital in	SPI chip select GYR	CSB2	DNC (float)
6	GNDIO	Ground	Ground for I/O	GND	GND
7	PS	Digital in	Protocol select	GND	VDDIO
8	SCx	Digital in	Serial clock	SCK	SCL
9	SDx	Digital I/O	SPI: serial data in; TWI: serial data in/out	SDI	SDA
10	SDO2	Digital out	SPI: serial data out GYR	SDO2	SDO2
11	VDDIO	Supply	Digital I/O supply voltage	VDDIO	VDDIO
12	INT3	Digital I/O	Interrupt pin (GYR int #1)	INT3 / DNC	INT3 / DNC
13	INT4	Digital I/O	Interrupt pin (GYR int #2)	INT4 / DNC	INT4 / DNC
14	CSB1	Digital in	SPI chip select ACC	CSB1	DNC (float)
15	SDO1	Digital out	SPI: serial data out ACC	SDO1	SDO1
16	INT1	Digital I/O	Interrupt pin 1 (ACC int #1)	INT1 / DNC	INT1 / DNC

DNC: Do not connect
INTx: If not needed, DNC

Soldering

The moisture sensitivity level (MSL) of BOSCH SMI230 corresponds to JEDEC Level 1, see also

- IPC/JEDEC J-STD-020C “Joint Industry Standard: Moisture/Reflow Sensitivity Classification for non-hermetic Solid State Surface Mount Devices”
- IPC/JEDEC J-STD-033A “Joint Industry Standard: Handling, Packing, Shipping and Use of Moisture/Reflow Sensitivity Surface Mount Devices”

3.5 The sensor IC fulfils the lead-free soldering requirements of the above-mentioned IPC/JEDEC standard, i.e. reflow soldering with a peak temperature up to 260 °C.

Repair and manual soldering of the sensor is not permitted.

3.5.1 Reflow Soldering Recommendation for Sensors in LGA Package

Please make sure that the edges of the LGA substrate of the sensor are free of solder material. Avoid solder material forming a high meniscus covering the edge of the LGA substrate (see Figure 14).

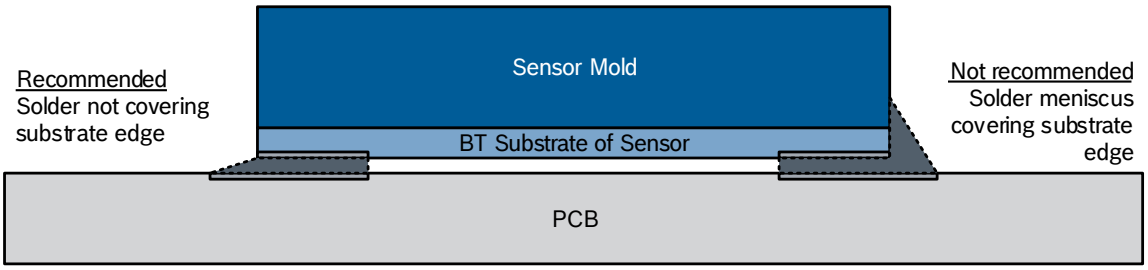


Figure 14 Reflow soldering recommendation

3.5.2 Classification Reflow Profile

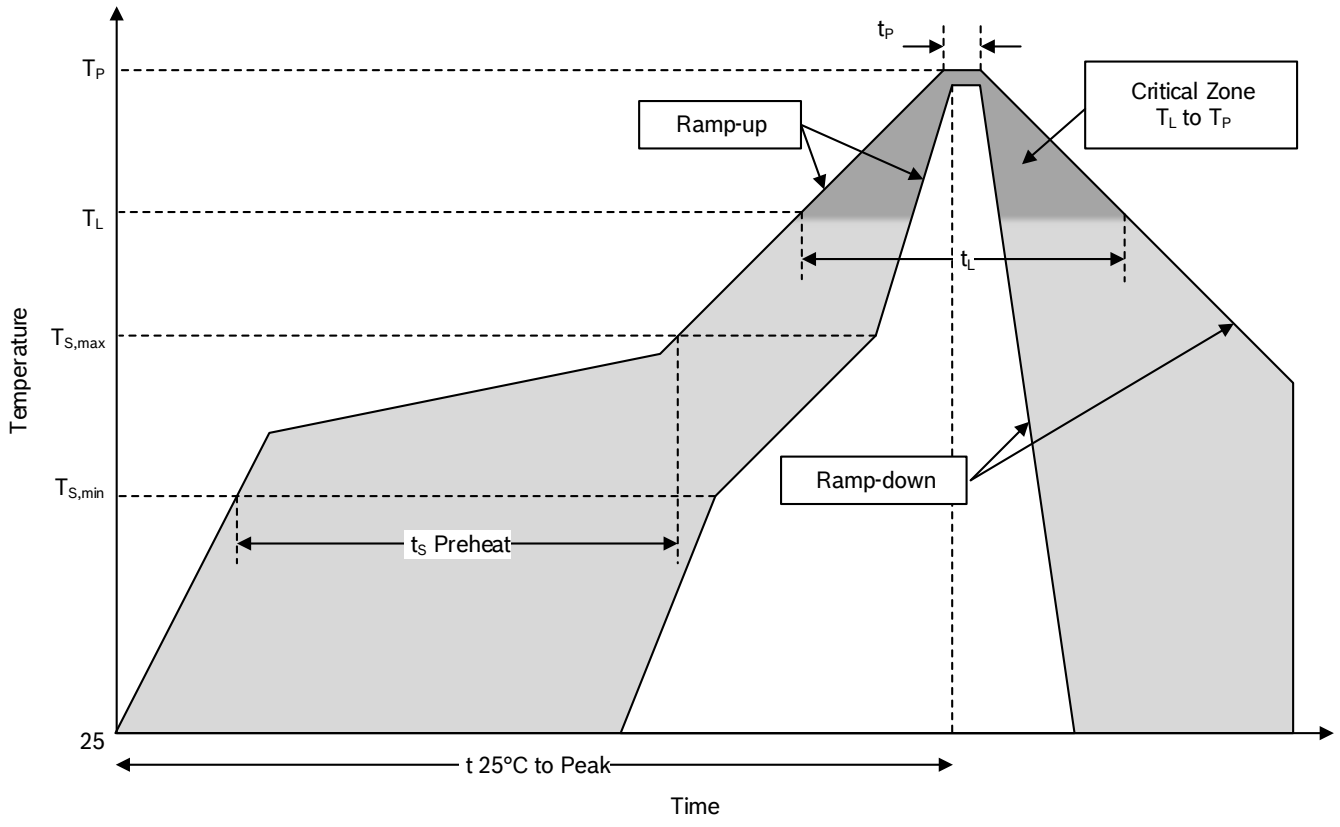


Figure 15 Soldering profile

Profile Feature	Pb-Free Assembly
Average ramp-up rate (T_{Smax} to T_p)	3 °C/s max.
Preheat Temperature min (T_{Smin}) Temperature max (T_{Smax}) Time (t_{Smin} to t_{Smax})	 150 °C 200 °C 60 – 180 s
Time maintained above: Temperature (T_L) Time (t_L)	 217 °C 60 s – 150 s
Peak classification temperature (T_P)	260 °C
Time within 5 °C of actual peak temperature (t_p)	20 s – 40 s
Ramp-down rate	6 °C/s max.
Time °C to peak temperature	8 min max.

Note All temperatures refer to the topside of package, measured on the package body surface.

3.5.3 Multiple Reflow Soldering Cycles

The product can withstand up to 3 reflow soldering cycles in total. This could be a situation where a PCB is mounted with devices from both sides (i.e. 2 reflow cycles necessary) or where, in the next step, an additional re-work cycle could be required (1 reflow).

3.6 Mounting Recommendations

In general, MEMS sensors are high-precision measurement devices which consist of electronic as well as mechanical structures. Bosch sensor devices are designed for precision, efficiency, and mechanical robustness.
However, in order to achieve best possible results of your design, the following recommendations should be taken into consideration when mounting the sensor on a printed circuit board (PCB).

In order to evaluate and optimize the considered placement position of the sensor on the PCB, it is recommended to use additional tools during the design in phase, e.g. regarding:

- Thermal aspects: infrared camera
- Mechanical stress: warpage measurements and/or FEM-simulations
- Shock robustness: drop test after soldering on the target application PCB

It is recommended to keep a reasonable distance between the sensor mounting location on the PCB and the critical points described in the following examples. The exact value for a “reasonable distance” depends on many customer specific variables and must therefore be determined case by case.

- It is generally recommended to minimize the PCB thickness, since a thin PCB shows less intrinsic stress, e.g. during bending. (Recommendation ≤ 0.8 mm)
- It is *not* recommended to place the sensor directly under or next to push-button contacts as this can result in mechanical stress.
- It is *not* recommended to place the sensor in direct vicinity of extremely hot spots regarding temperature (e.g. a µController or a graphic chip) as this can result in heating up the PCB and consequently also of the sensor.
- It is *not* recommended to place the sensor in direct vicinity of a mechanical stress maximum (e.g. in the center of a diagonal crossover). Mechanical stress can lead to bending of the PCB and the sensor.
- Do not mount the sensor too closely to a PCB anchor point where the PCB is attached to a shelf (or similar) as this could also result in mechanical stress. To reduce potential mechanical stress, minimize redundant anchor points and/or loosen respective screws.
- Avoid mounting the sensor in areas where resonant amplitudes (vibrations) of the PCB are likely or to be expected.

- Please avoid partial coverage of the sensor by any kind of (epoxy) resin, as this can possibly result in mechanical stress.
- Avoid mounting (and operating) the sensor in the vicinity of strong magnetic, strong electric, and/or strong infrared (IR) radiation fields.
- Avoid electrostatic charging of the sensor and of the device in which the sensor is mounted.

In case you have any questions regarding the mounting of the sensor on your PCB or the evaluation and/or optimization of the considered placement position of the sensor on your PCB, please contact your Bosch representative.

If the above mentioned recommendations cannot be realized appropriately, a specific in-line offset-calibration after the placement of the device onto your PCB might help to minimize potentially remaining effects.

The SMI230 is designed to sense angular rates with high accuracy even at low amplitudes and contains highly sensitive structures inside the sensor element. The MEMS sensor can tolerate mechanical shocks up to several thousand g's. However, these limits might be exceeded in conditions with extreme shock loads such as a hammer blow on or next to the sensor, dropping the sensor onto hard surfaces, etc.

We strongly recommend to avoid any g-forces beyond the limits specified in the data sheet during transport, handling, and mounting of the sensors in a defined and qualified installation process.

This device has built-in protections against high electrostatic discharges and electric fields (2 kV HBM); however, anti-static precautions should be taken as for any other CMOS component.

Unless otherwise specified, proper operation can only occur when all terminal voltages are kept within the supply voltage range. Unused inputs must always be connected to a defined logic voltage level.

3.7 Recommendations for PCB Layout

For the design of the landing patterns, the dimensioning as shown in Figure 16 is recommended. The dimensions are given in mm.

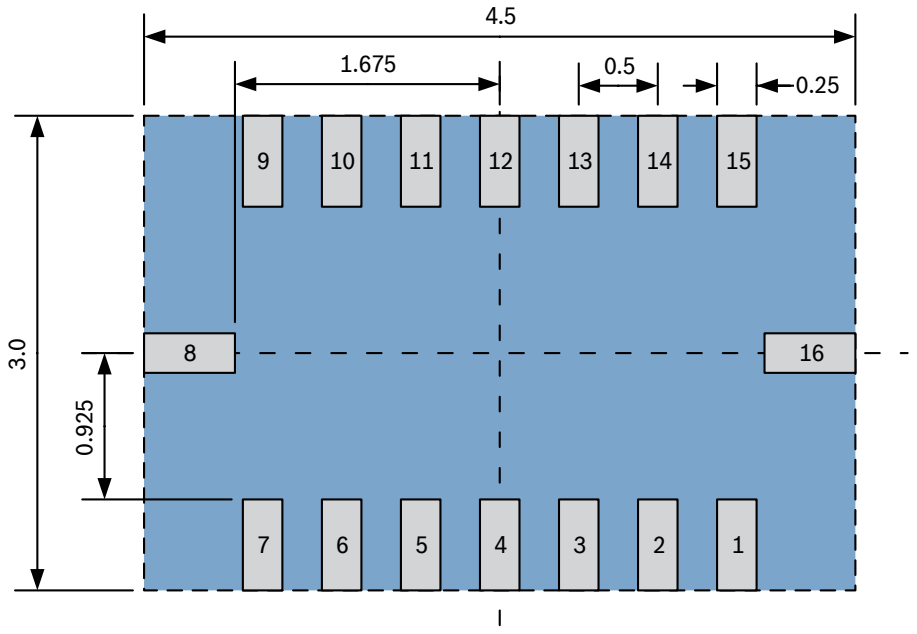


Figure 16 SMI230 footprint

4 Environment Specification

Absolute Maximum Ratings

Any values beyond the given ratings may seriously damage the device. The sensor must be discarded when exceeding these limits.

4.1

Parameter	Condition	Min	Max	Unit
Voltage at supply pin	VDD pin	-0.3	4	V
Voltage at supply pin	VDDIO pin	-0.3	4	V
Voltage at any logic pin	non-supply pin	-0.3	VDDIO +0.3	V
Passive storage temp. range	≤ 65 % rel. H.	-50	+150	°C
Mechanical shock	duration ≤ 200 µs		10000	g
Mechanical shock	duration ≤1 ms		2000	g
Mechanical shock	Free fall onto hard surfaces		1.2	m
ESD	HBM, any pin		2	kV
ESD	CDM		500	V
ESD	MM		200	V

Operating Conditions

4.2

Parameter	Symbol	Condition	Min	Typical	Max	Unit
Operating temperature	T		-40		105	°C

Lifetime Conditions

4.3

Lifetime conditions are according to AEC-Q100 grade 2 requirements.

Environmental Safety

4.4

RoHS

The SMI230 sensor meets the requirements of the *Restriction of Hazardous Substances* (RoHS) directive 2002/95/EC of the European Parliament and of the Council of 27 January 2003 (on the *Restriction of the use of certain Hazardous Substances in electrical and electronic equipment)*.

Halogen content

The SMI230 is halogen-free. For more details on the analysis results, please contact your Bosch representative.

5 Parameter Specification

Power Supply

The SMI230 has two distinct power supply pins:

- VDD is the main power supply for the internal blocks
- VDDIO is a separate power supply pin mainly used for the supply of the interface

5.1

Parameter	Symbol	Condition	Min	Typical	Max	Unit
Supply voltage internal domains	VDD		2.4	3.3	3.6	V
Supply voltage I/O domain	VDDIO		1.62	3.3	3.6	V
Voltage input low level	V_{IL}				0.3 VDDIO	-
Voltage input high level	V_{IH}		0.7 VDDIO			-
Voltage output low level	V_{OL}	I_{OL} ≤ 2 mA, SPI			0.23 VDDIO	-
Voltage output high level	V_{OH}	I_{OH} ≤ 2 mA, SPI	0.8 VDDIO			-

There are no limitations on the voltage levels of both pins relative to each other, as long as each of them lies within its operating range. Furthermore, the device can be completely switched off (VDD = 0 V) while keeping the VDDIO supply on (VDDIO > 0 V) or vice versa.

In the case that the VDDIO supply is off, all interface pins (CSB, SDI, SCK, PS) must be kept close to GNDIO potential.

The SMI230 provides a **power-on reset (POR)** generator. It resets the logic part and the register values after powering-on VDD and VDDIO. This means that all application specific settings which are not equal to the default settings must be changed back to their designated values after POR.

The POR resets also the interface. For the gyroscope part, the interface is defined by the voltage level on the PS pin. The interface of the accelerometer part is defined by the voltage level of the CSB1 pin at the moment when the POR is initiated (see chapter 2.4).

5.2

Technical data

The data in the following section, unless otherwise noted, apply for the valid operation conditions given in section 4.2. All following figures include voltage, temperature, and lifetime effects if not noted otherwise. All figures, except sensitivity, are only valid without an external stimulus applied. All figures except for the noise itself exclude noise effects.

5.2.1 Accelerometer

Unless otherwise specified, the sensor is configured with the default settings. The measurement range is set to 2 g and the bandwidth is set to 40.5 Hz (100 Hz ODR).

Parameter	Symbol	Condition / Comment	Typical	Max[1]	Unit
Supply current in Normal mode	I_{DD}	VDD = VDDIO = 3.0 V, 25 °C, g_{FS4g}	170		µA
Supply current in Suspend mode	I_{DDsum}	VDD = VDDIO = 3.0 V, 25°C	3		µA
Start-up time	$t_{s,up}$	time to first valid sample from suspend mode			ms
Measurement range	g_{FS}	selectable	±2 ±4 ±8 ±16		g

Resolution		g_{FS2g}, T_A = 25 °C g_{FS4g}, T_A = 25 °C g_{FS8g}, T_A = 25 °C g_{FS16g}, T_A = 25 °C	16384 8192 4096 2048	LSB / g
Sensitivity tolerance		including temperature and lifetime effects	1	%
Sensitivity temperature drift	TCS		±0.004	% / K
Zero-g offset		including temperature and lifetime effects	20	mg
Zero-g offset temperature drift		nominal VDD supply, over full temperature range	±0.2	mg / K
Output data rate	ODR	selectable between	12.5 - 1600	Hz
Bandwidth	BW	3dB cutoff frequency of the accelerometer depends on ODR and OSR	5.06 – 684 (max. 353 for Z axis)	Hz
Nonlinearity	NL	best fit straight line, no life-time	10	mg
Noise rms	n_{rms}	T_A = 25 °C, nominal VDD supply no lifetime		mg
Cross axis sensitivity	S	relative contribution between any two of the three axes	±1	%
Alignment error	E_A	relative to package outline	0.5	°
Temperature sensor Measurement range			-104...+150	°C
Temperature sensor slope			0.125	K / LSB
Temperature sensor offset error		T_A = 25 °C	±1	K

[1]For specified maximum values, please refer to the Technical Customer Documentation.

5.2.2 Gyroscope

Unless otherwise specified, the sensor is configured with default settings. The measurement range is set to 2000 °/s and the bandwidth is set to 47 Hz.

Parameter	Symbol	Condition / Comment	Typical	Max[1]	Unit
Measurement range	R_{FS}	selectable	±125 ±250 ±500 ±1000 ±2000		°/s
Supply current in Normal mode	I_{DD}	VDD = VDDIO = 3.0 V, 25°C	5		mA
Supply current in Suspend mode	I_{DDSum}	VDD = VDDIO = 3.0 V, 25°C	25		µA
Supply current in Deep suspend mode	I_{DDdsum}	VDD = VDDIO = 3.0 V, 25°C	<5		µA
Start-up time	$t_{s,up}$	POR			s
Resolution		$g_{FS2000dps}$, T_A = 25 °C $g_{FS1000dps}$, T_A = 25 °C $g_{FS500dps}$, T_A = 25 °C $g_{FS240dps}$, T_A = 25 °C $g_{FS125dps}$, T_A = 25 °C	16.38 32.77 65.54 131.07 262.14		LSB / °/s
Sensitivity tolerance		including temperature and lifetime effects			%
Sensitivity tolerance		T = 25 °C over lifetime	±1		%
Sensitivity temperature drift	TCS	nominal VDD supply, over full temperature range	±0.03		% / K
Zero-rate offset		lifetime and temperature effects	±0.5		°/s
Zero-rate offset		T = 25 °C over lifetime			°/s
Zero-rate offset temperature drift		nominal VDD supply, over full temperature range	±0.015		°/s / K
Bandwidth	BW		12, 23, 32, 47, 64, 116, 230, 523 (unfiltered)		Hz
Nonlinearity BW: 23 Hz; range: ±125 °/s	NL	best fit straight line, no life-time			°/s
Noise rms		T = 25 °C, nominal VDD supply no lifetime	0.1		°/s
Temperature sensor slope			0.5		K / LSB
Temperature sensor offset		T = 25 °C	±5		K
Cross axis sensitivity		including temperature and lifetime effects	±2		%

[1]For specified maximum values, please refer to the Technical Customer Documentation.

6 Software Interface Description

Serial Peripheral Interface (SPI)

6.1.1 SPI Connection

For communication, the SMI230 supports the SPI 4-wire protocol as a slave with a host device. The connection diagram is shown in Figure 17. The mapping for the interface of both accelerometer and gyroscope is given in the table below:

6.1

Pin	Name	Description
15	SDO1	ACC data output
10	SDO2	GYR data output
9	SDx	SDI serial data in
14	CSB1	ACC chip select (enable)
5	CSB2	GYR chip select (enable)
8	SCx	SCK serial clock

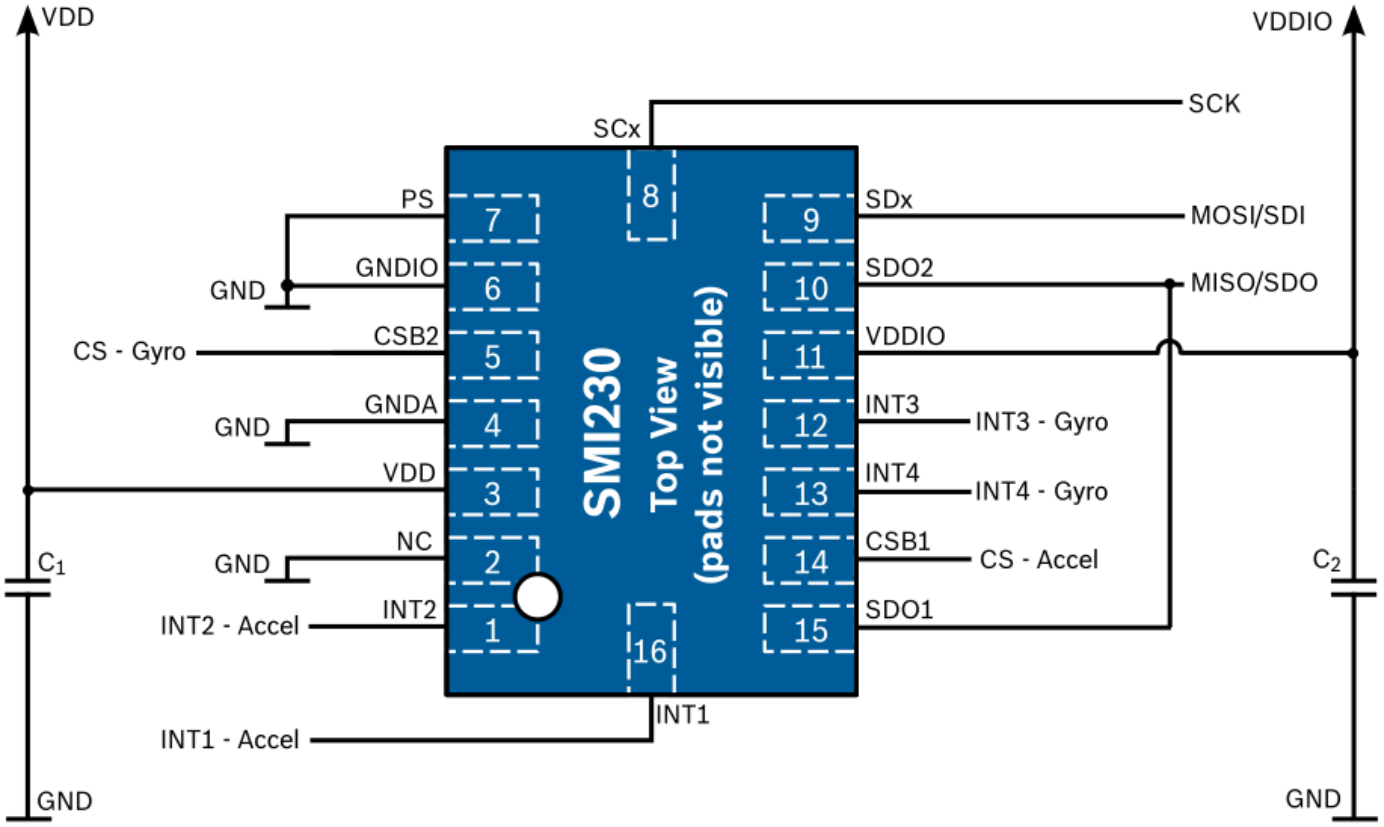


Figure 17 SPI connection diagram

C_1, C_2: 100 nF

INT1, INT2: see register ACC 0x53, 0x54

INT3, INT4: see register GYR 0x16

Note:

For a proper functionality, defined voltage levels at SDI, SDO and SCK are required. In case this cannot be guaranteed by the SPI controller, additional pull-up or pull-down resistors are required.

6.1.2 SPI Timing

The SPI timing specification of the SMI230 is given in the following table:

Parameter	Symbol	Condition	Min	Max	Units
Clock frequency	f_{SPI}	max. load on SDI or SDO = 25 pF		10	MHz
SCK low pulse	t_{SCKL}		20		ns
SCK high pulse	t_{SCKH}		48		ns
SDI setup time	t_{SDI_setup}		20		ns
SDI hold time	t_{SDI_hold}		20		ns
SDO output delay	t_{SDO_OD}	load = 25 pF		40	ns
		load = 250 pF, VDDIO = 2.4 V		40	ns
CSB setup time	t_{CSB_setup}		20		ns
CSB hold time	t_{CSB_hold}		40		ns
Idle time between write accesses	$t_{IDLE\_wacc\_nm}$		2		µs

Figure 18 shows the definition of the SPI timing.

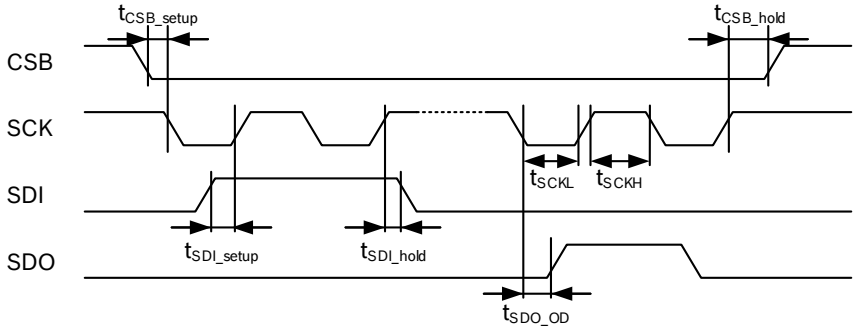


Figure 18 SPI timing diagram

The SPI interface of the SMI230 is compatible with two modes: 00 and 11. The automatic selection between [CPOL = 0 and CPHA = 0] and [CPOL = 1 and CPHA = 1] is controlled based on the value of SCK after a falling edge of CSB (1 or 2). For single byte read as well as write operations, 16 bit protocols are used. The SMI230 also supports multiple byte read operations (burst read).

For standard SPI configuration, the pins CSB (1 or 2 - chip select low active), SCK (serial clock), SDI (serial data input), and SDO (1 or 2 - serial data output) are used. The communication starts when CSB (1 or 2) is pulled low by the SPI master and stops when CSB (1 or 2) is pulled high. SCK is also controlled by the SPI master. SDI and SDO (1 or 2) are driven at the falling edge of SCK and should be captured at the rising edge of SCK.

The basic write operation waveform for the 4-wire configuration is depicted in Figure 19. During the full write cycle, SDO remains in high-impedance state.

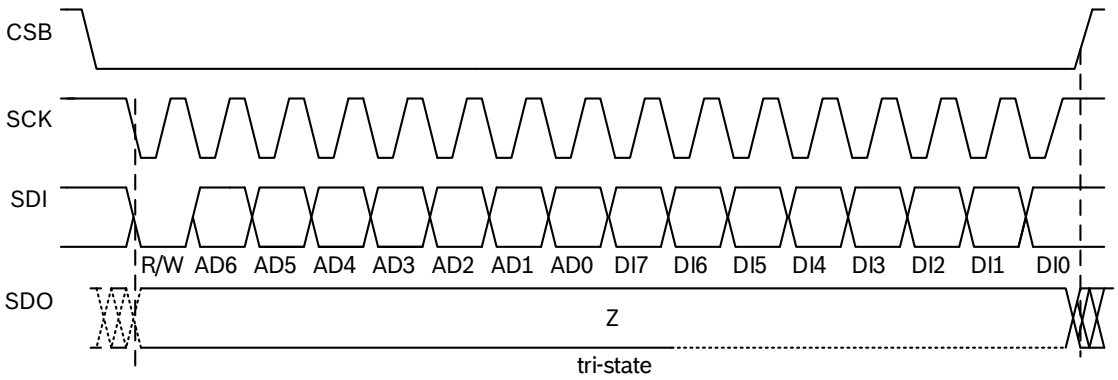


Figure 19 4-wire basic SPI write sequence (mode 11)

The basic read operation waveform for the 4-wire configuration is depicted in Figure 20.

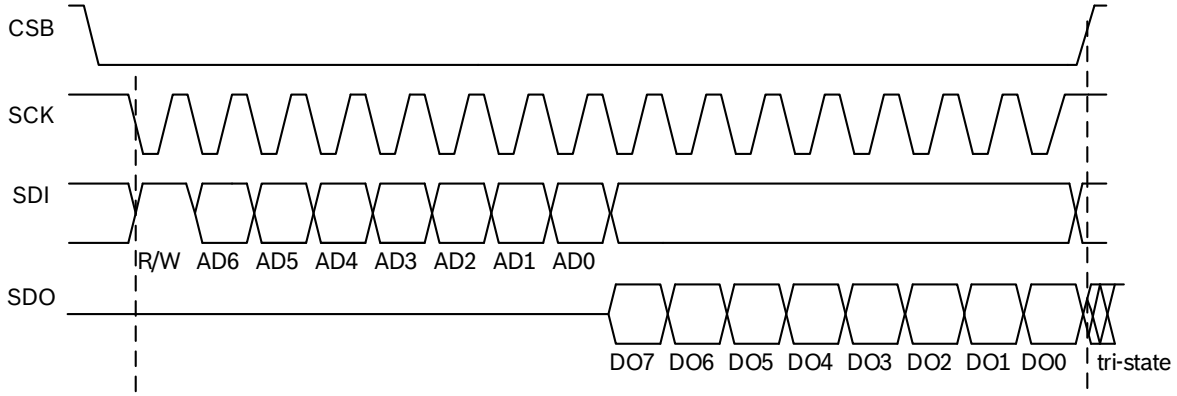


Figure 20 4-wire basic SPI read sequence (mode 11)

The data bits are used as follows:

Bit <15>: Read/write bit. When 0, the data SDI is written into the chip. When 1, the data SDO from the chip is read.

Bits <14:8>: Address AD (6:0)

Bits <7:0>: In write mode, these bits are the data SDI which will be written into the address. In read mode, these bits are the data SDO which are read from the address.

Multiple read operations (burst read access) are possible by keeping CSB low and continuing the data transfer. Only the first register address has to be written. Addresses are automatically incremented after each read access as long as CSB stays active low.

The principle of multiple read is shown in Figure 21.

	Control Byte								Data Byte								Data Byte								Data Byte								
Start	RW	Register address (02h)							Data register – address 02h								Data register – address 03h								Data register – address 04h								Stop
CSB = 0	1	0	0	0	0	0	1	0	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	CSB = 1

Figure 21 SPI multiple read

6.1.3 SPI Interface of Accelerometer

During read operation of the accelerometer part the **requested data is not immediately sent. Instead, a dummy byte is sent first** followed by the actual requested register content.

This means that – in contrast to the description in section 5.1.2– a **single byte read operation requires to read 2 bytes in burst read access mode**, in which the first received byte can be discarded, while the second byte contains the desired data.

The same applies to burst read access operations. For example, to read the accelerometer values in SPI mode, the user has to read 7 bytes, starting from address 0x12 (ACC data). From these bytes the user must discard the first byte and finds the acceleration information in byte 2 – 7 (corresponding to the content of the addresses 0x12 – 0x17).

Two-wire Interface (TWI)

With some exceptions, the TWI interface of the SMI230 is compatible to the I²C specification UM10204 Rev. 03 (19 June 2007), available at http://www.nxp.com.

- The SMI230 supports the I²C standard and fast mode, but only the 7-bit address mode.
- For VDDIO = 1.2 ... 1.8 V the granted voltage output levels are slightly relaxed compared to the specification.
- The internal data hold time (t_{HDDAT}) of 300 ns is not met under all operation conditions. The device achieves a minimum value of 120 ns across process corners and temperature.
- The minimum data fall time (t_F) of 20 ns cannot be met.
- Only single byte write is supported.
- Detection of a stop condition is not supported. All data transfer protocols are fully operational by means of detecting the start condition only.
- The device does not support the high-impedance mode while VDDIO is tied to GND.
- The device does not perform clock stretching, i.e. clock frequencies may not exceed the one specified in the parameter section and wait times between subsequent write accesses (as specified in section 0) have to be ensured by the bus master.

6.2

6.2.1 TWI Connection

The TWI interface uses the SCL (= SCx pin, serial clock) and SDA (= SDx pin, serial data input and output) signal lines. Both lines are connected to VDDIO externally via pull-up resistors so that they are pulled high when the bus is free.

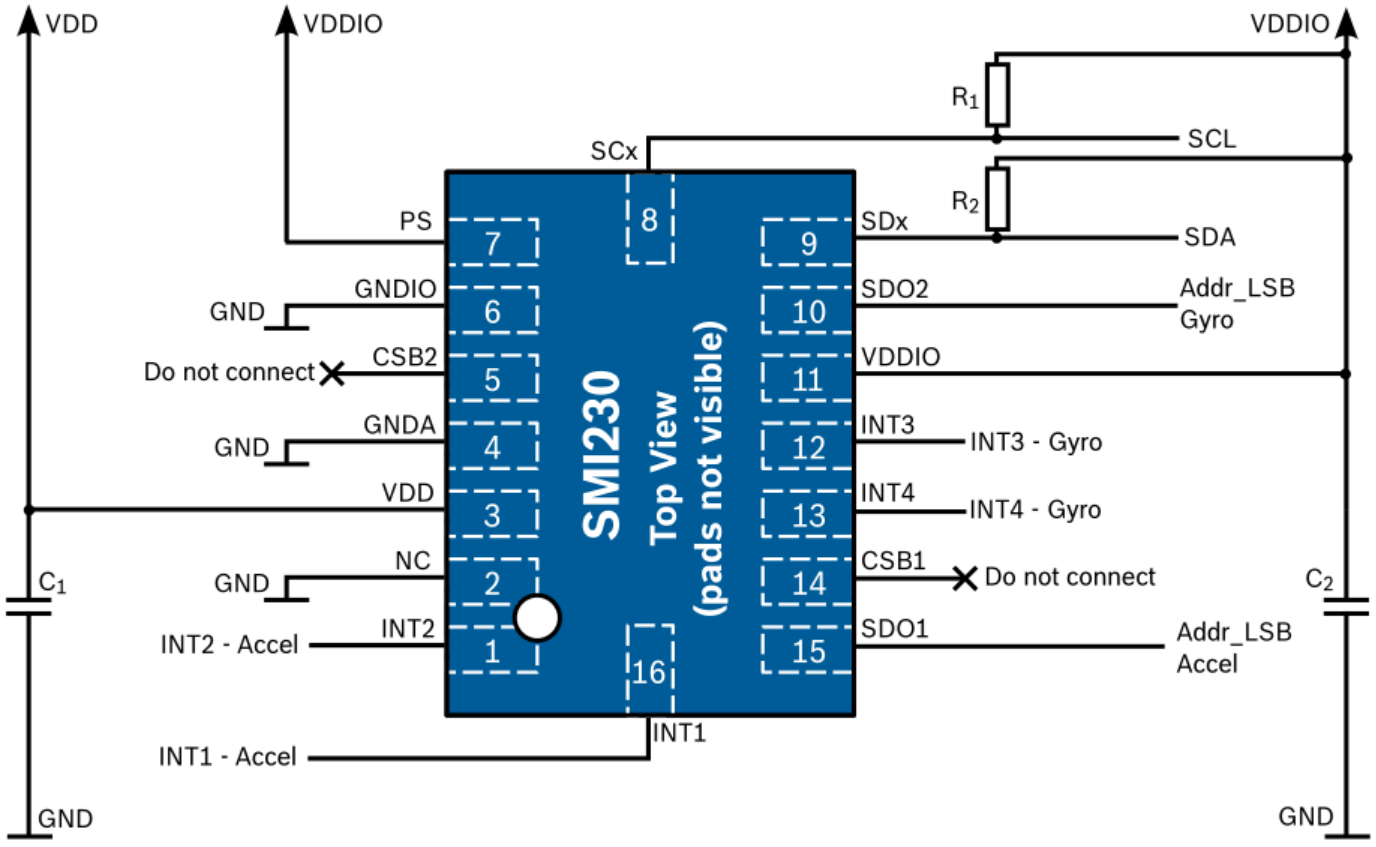


Figure 22 TWI connection diagram

C_1, C_2: 100 nF

R_1, R_2: pull-up resistors

INT1, INT2: see register GYR 0x16

INT3, INT4: see registers ACC 0x53, 0x54

SDO1 and SDO2 are used to define the TWI address of accelerometer and gyroscope. The default TWI address of the SMI230 accelerometer is 0x18 and gyroscope is 0x68. It is used if both SDO pins are pulled to GND. The alternative address is selected by pulling the corresponding SDO pin to VDDIO.

	Accelerometer address	Gyroscope address
SDO1 and SDO2 to GND	0x18 (ACC: 0011000)	0x68 (GYR: 1101000)
SDO1 and/or SDO2 to VDDIO	0x19 (ACC: 0011001)	0x69 (GYR: 1101001)

6.2.2 TWI Timing

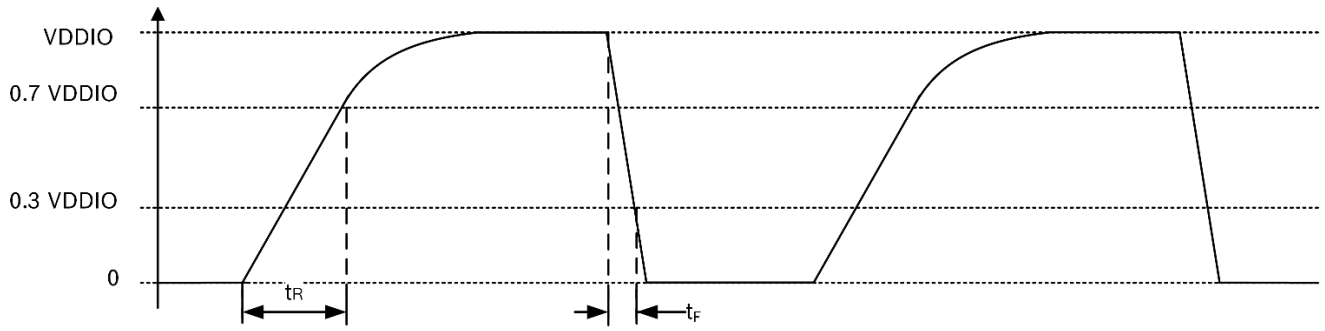


Figure 23 Definition of rise and fall time of TWI signals

TWI timing specification of the SMI230 is given in the table below.

Parameter	Symbol	Min	Max	Units
Clock frequency	f_{SCL}	0	400	kHz
SCL low period	t_{LOW}	1.3		µs
SCL high period	t_{HIGH}	0.6		
SDA setup time	t_{SUDAT}	0.1		
SDA hold time	t_{HDDAT}	0.0		
Setup time for a repeated start condition	t_{SUSTA}	0.6		
Hold time for a start condition	t_{HDSTA}	0.6		
Setup time for a stop condition	t_{SUSTO}	0.6		
Time before a new transmission can start	t_{BUF}	1.3		
Idle time between write accesses normal mode	$t_{IDLE\ wacc\ nm}$	2		
Fall time	t_F	0	300	ns
Rise time (determined by external pull-up resistance)	t_R	20	300	ns

Figure 24 shows the definition of TWI timing given in the table above.

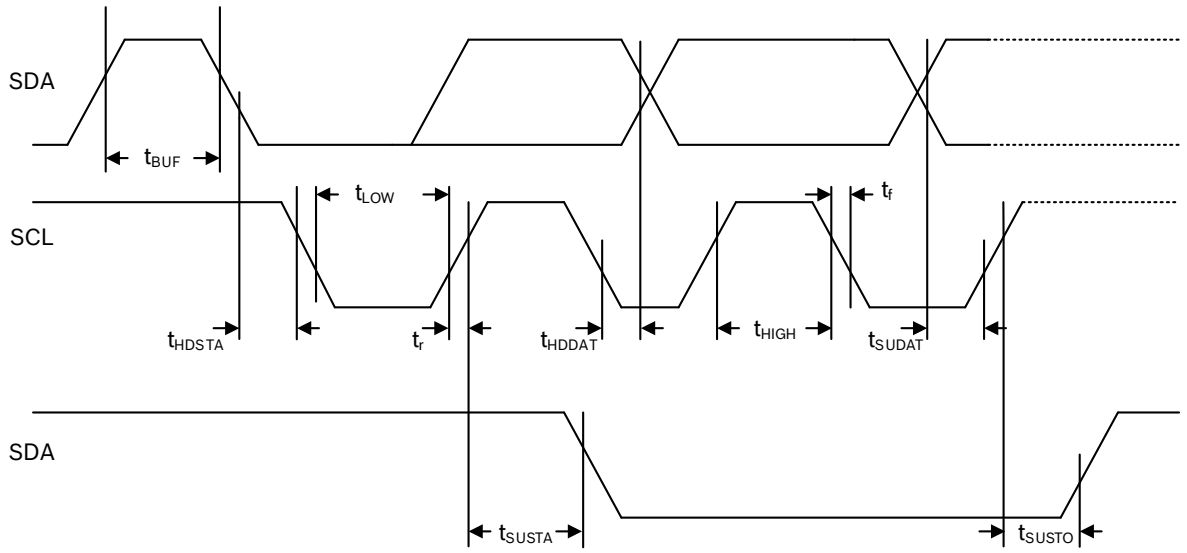


Figure 24 SMI230 TWI timing specification

The TWI protocol works as follows:

Mode	Description
START:	Data transmission on the bus begins with a high to low transition on the SDA line while SCL is held high (start condition (S) indicated by the TWI bus master). Once the start signal is transferred by the master, the bus is considered busy.
STOP:	Each data transfer should be terminated by a stop signal (P) generated by the master. The stop condition is a low to high transition on the SDA line while SCL is held high.
ACK:	Each byte of data transferred must be acknowledged. It is indicated by an acknowledge bit sent by the receiver. The transmitter must release the SDA line (no pull down) during the acknowledge pulse while the receiver must then pull the SDA line low so that it remains stable low during the high period of the acknowledge clock cycle.

In the following diagrams, these abbreviations are used:

S	Start	**P**	Stop
ACKS	Acknowledge by slave	**ACKM**	Acknowledge by master
NACKM	Not acknowledge by master	**RW**	Read / Write
Sr	Repeated start		

A start (S) immediately followed by a stop (P) (without SCL toggling from VDDIO to GND) is not supported and not recognized by the SMI230.

TWI write access can be used to write a data byte in one sequence.

The sequence begins with a start condition generated by the master, followed by 7 bits of the slave address and a write bit (RW = 0). The slave sends an acknowledge bit (ACK = 0) and releases the bus. Then the master sends the one-byte register address. The slave again acknowledges the transmission and waits for the 8 bits of data, which shall be written to the specified register address. After the slave acknowledges the data byte, the master generates a stop signal and terminates the writing protocol. Figure 25 shows an example of a TWI write access to the accelerometer.

										Control Byte									Data Byte								
Start	Slave Address							RW	ACKS	Register Address (0x10)								ACKS	Data (0x09)								ACKS	Stop
S	1	1	0	1	0	0	0	0		0	0	0	1	0	0	0	0		X	X	X	X	X	X	X	X		P

Figure 25 Example of a TWI write access to the accelerometer

TWI read access can be used to read one or multiple data bytes in one sequence.

A read sequence consists of a one-byte TWI write phase followed by the TWI read phase. Both parts of the transmission must be separated by a repeated start condition (Sr). TWI write phase addresses the slave and sends the register address to be read. After the slave acknowledges the transmission, the master again generates a start condition and sends the slave address together with a read bit (RW = 1). Then the master releases the bus and waits for the data bytes to be read out from the slave. After each data byte, the master has to generate an acknowledge bit (ACK = 0) to enable further data transfer. A NACKM (ACK = 1) from the master stops the data being transferred from the slave. The slave releases the bus so that the master can generate a stop condition and terminate the transmission.

The register address is automatically incremented. Hence, more than one byte can be sequentially read out. Once a new data read transmission starts, the start address will be set to the register address specified in the latest TWI write command. By default, the start address is set as 0x00. In this way, repetitive multi-byte reads from the same starting address are possible.

In order to prevent the TWI slave from locking the TWI bus, a watchdog timer (WDT) is implemented. The WDT observes internal I2C signals and resets the TWI interface if the bus is locked up. The activity and timer period of the WDT can be configured via bits 2 (*i2c_wdt_en*) and 1 (*i2c_wdt_sel*) in register ACC 0x70 (NV_CONF) and GYR 0x34 (*BGW_SPI3_WDT_FIFO*).

- Writing 1 (0) to *i2c_wdt_en* activates (de-activates) the WDT
- Writing 0 (1) to *i2c_wdt_se* sets a timer period of
  - 1.25ms (40ms) for ACC 0x70
  - 1 ms (50 ms) for GYR 0x34

Figure 26 shows an example of a TWI read access to the accelerometer.

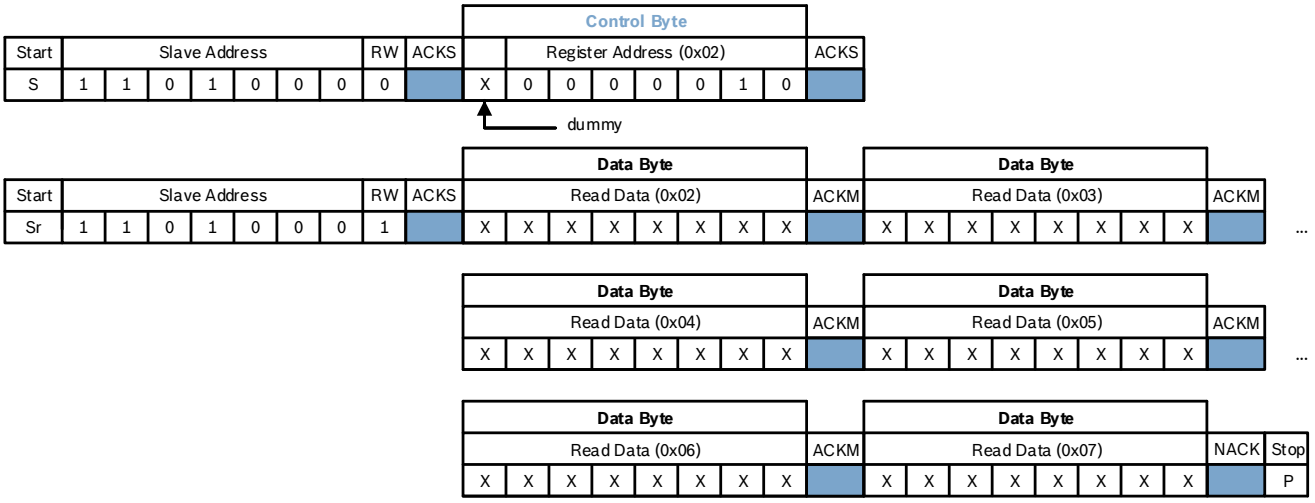


Figure 26 Example of a TWI read access

Note (Gyroscope soft reset):

The SMI230 shows a specific behavior after performing a soft reset of the gyroscope. After carrying out the soft reset, the TWI slave is reset. This releases the bus before completing the command and a NACK is sent instead of an ACK. The user may ignore the first NACK after a soft reset of the gyroscope.

Access Restrictions (SPI and TWI)

In order to allow for the correct internal synchronization of data written to the SMI230, certain access restrictions apply for consecutive write accesses or a write/read sequence through the SPI and TWI interface.

As illustrated in Figure 27, an interface idle time of at least 2 µs is required following a write operation when the device operates in normal mode. In suspend mode an interface idle time of least 450µs is required.

6.3

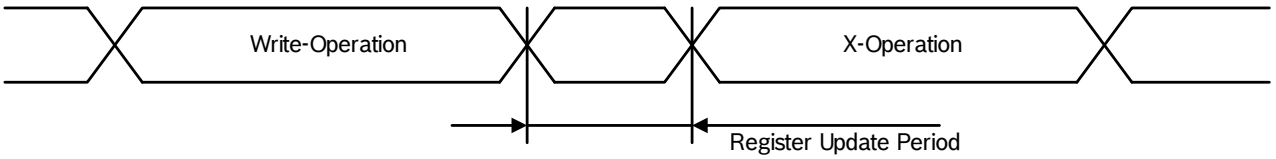


Figure 27 Post-write access timing constraints

7 Application Details

In Figure 28 the basic flow chart for the sensor application is shown. Three different categories of functional elements are shown:

- Required: these blocks are mandatory for a proper sensor functionality and retrieving data (e.g. read data)
- Recommended: these blocks are useful to detect potential sensor failure and allows further setup of the sensor (e.g. self-test, sensor setup)
- Optional: depending on the customer specific application, these blocks might be required (e.g. interrupt configuration)

The functional elements are described in the following sections. Proper function of the sensor in the overall system must be validated by the customer.

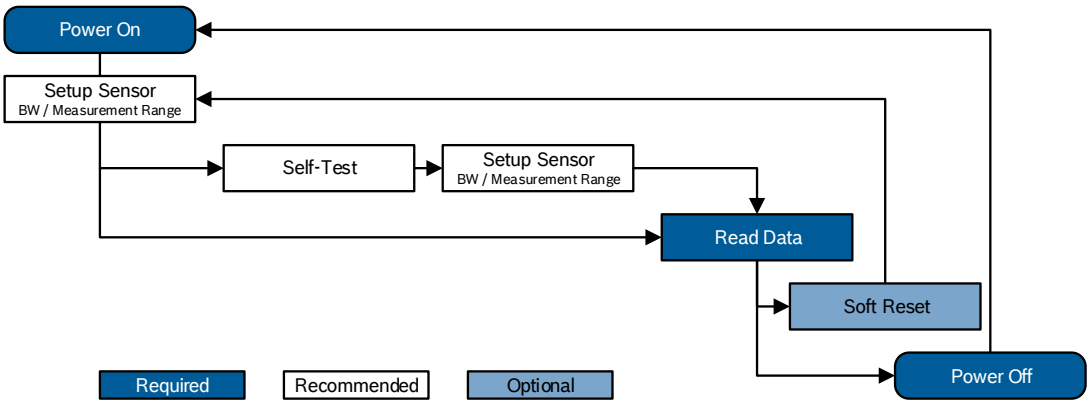


Figure 28 Basic flow chart for SMI230 application with key functional elements

7.1 Device Initialization

For a proper device initialization, the following steps need to be considered:

- The user must decide on the interface (TWI or SPI) already during hardware design: with the PS pin the user determines which interface the sensor should listen to.
- The gyroscope part of the SMI230 initializes its I/O pins according to the selection given by the PS pin.
  The accelerometer part starts in TWI mode. It will stay in TWI mode until it detects a rising edge on the CSB1 pin (chip select of the accelerometer), on which the accelerometer part switches to SPI mode and stays in this mode until the next power-on-reset (POR). To change the sensor to SPI mode in the initialization phase, the user has to perform a dummy SPI read or write operation, e.g. reading of register ACC_CHIP_ID. Any obtained value will be invalid.
- After the POR the gyroscope is in normal mode, while the accelerometer is in suspend mode. To switch the accelerometer into normal mode, the user must perform the following steps:
  a. Power up the sensor
  b. Wait for 1 ms
  c. Enter normal mode by writing ‘4’ to ACC_PWR_CTRL
  d. Wait for 50 ms

Sensor Settings

The basic sensor setup includes the selection of the bandwidth and measurement range for accelerometer and gyroscope.

7.2.1 Accelerometer

The **bandwidth** (3db cutoff frequency) of the digital low-pass filter depends on the chosen ODR as well as on the over sampling ratio (OSR). Both can be configured in register ACC 0x40 (*ACC_CONF*). The following table lists the possible options:

7.2

Accelerometer ODR [Hz]	3dB cutoff frequency [Hz]		
	Normal	OSR = 2	OSR = 4
12.5	5.06	3	1
25	10.12	5	3
50	20.25	10	5
100	40.5	20	10
200	80	41	20
400	162 (155 for Z channel)	80	41
800	324 (252 for Z channel)	162 (155 for Z channel)	80
1600	684 (353 for Z channel)	324 (262 for Z channel)	162

The acceleration measurement **range** can be selected via bits <1:0> (*acc_range*) in register ACC 0x41 (*ACC_RANGE*) according to the table below.

acc_range <1:0>	Measurement Range	Resolution
00	± 2 g	16384 LSB/g
01	± 4 g	8192 LSB/g
10	± 8 g	4096 LSB/g
11	± 16 g	2048 LSB/g

7.2.2 Gyroscope

The **bandwidth** of filtered rate data is determined by setting bits <3:0> (*bw*) in register GYR 0x10 (*BW*) as shown in the following table.

bw <3:0>	Filter Bandwidth [Hz]	ODR [Hz]	Decimation Factor
0111	32	100	20
0110	64	200	10
0101	12	100	20
0100	23	200	10
0011	47	400	5
0010	116	1000	2
0001	230	2000	0
0000	523 (unfiltered)	2000	0
1xxx	reserved	reserved	reserved

The rate measurement **range** can be selected via bits <2:0> (*range*) in register GYR 0x0F (*RANGE*) according to the table below.

range <2:0>	Measurement Range	Resolution
000	±2000 °/s	16.38 LSB/°/s
001	±1000 °/s	32.77 LSB/°/s
010	±500 °/s	65.54 LSB/°/s
011	±250 °/s	131.07 LSB/°/s
100	±125 °/s	262.14 LSB/°/s
others	reserved	-

Power Modes

7.3.1 Power Modes Accelerometer

7.3 The power state of the SMI230 accelerometer is controlled through the register ACC_PWR_CTRL. The register ACC_PWR_CTRL enables and disables the accelerometer and the temperature sensor.

To enter **normal mode**, the value 0x04 must be written to ACC_PWR_CTRL.

To enter **suspend mode**, the register ACC_PWR_CTRL must be cleared.

The SMI230 accelerometer is in suspend mode after reset (POR or soft-reset), thus the user actively needs to enter normal mode in order to obtain acceleration values.

For the procedure of changing the power mode, please refer to 7.1 Device Initialization. Any communication with the sensor during this time should be avoided.

7.3.2 Power Modes Gyroscope

The gyroscope has 3 different power modes. Besides **normal mode**, which represents the fully operational state of the device, there are 2 energy saving modes: suspend mode and deep suspend mode.

After power-up the gyro is in normal mode so that all parts of the device are held powered-up and data acquisition is performed continuously.

In **suspend mode** the whole analog part is powered down. No data acquisition is performed. While in suspend mode the latest rate data and the content of all configuration registers are kept. The registers can still be read (though they are not updated).

The suspend mode is entered by writing 0x80 to the register GYRO_LPM1. It can be left by writing 0x00 to GYRO_LPM1 or by a soft reset.

Although write access to registers is supported at the full interface clock speed (SCL or SCK), a waiting period must be inserted between two consecutive write cycles.

In **deep suspend mode** the device reaches the lowest possible power consumption. Only the interface section is kept alive. No data acquisition is performed and the content of the configuration registers is lost.

The deep suspend mode is entered by writing 0x20 to the register GYRO_LPM1. It can be left by writing 0x00 to GYRO_LPM1 or by a soft reset.

Please note, that all application specific settings, which are not equal to the default settings, must be re-set to their designated values after leaving deep suspend mode.

After POR or soft reset, or when switching between the different power modes, the gyroscope sensor needs up to 200 ms time to reach the new state. Any communication with the sensor during this time should be avoided.

Application Support Software

A Linux driver for SPI and TWI interface is available for SMI230 at https://github.com/boschmemssolutions.

New Data Interrupt

7.4

Both the accelerometer and gyroscope sensor offer a new data interrupt, which fires whenever a new data sample set is complete and made available in the corresponding sensor data registers. This allows for a low latency data readout.

7.5

7.5.1 Acceleration

The new data interrupt flag can be found in the register ACC_INT_STAT_1 (bit 7). It is set whenever new data is available in the data registers and cleared automatically.

The interrupt can be mapped to the interrupt pins INT1 and/or INT2 in register INT1_INT2_MAP_DATA.

Both interrupt pins INT1 and INT2 can be configured regarding their electrical behavior (see INT1_IO_CONF and INT2_IO_CONF).

New data interrupt function of the accelerometer part is always active. ACC_STATUS can be read whenever new data is available. If the interrupt is mapped to the interrupt pin properly, then ACC_INT_STAT_1 can be read out to see if new data arrived to that pin.

7.5.2 Gyroscope

The new data interrupt flag can be found in the register INT_STATUS_1 (bit 7). It is set whenever a new data is available in the data register and cleared automatically.

The gyroscope provides a new data interrupt, which will generate an interrupt every time after storing a new value of z-axis angular rate data in the data register. The interrupt is cleared automatically after 280-400 µs.

In contrast to the accelerometer part, for the gyro the new data interrupt must be explicitly enabled by writing 0x80 to the register INT_EN_0.

The interrupt status is stored in the register INT_STATUS_1.

7.6

The interrupt can be mapped to the interrupt pins INT3 and/or INT4 in register INT_MAP_1.

Both interrupt pins INT3 and INT4 can be configured regarding their electrical behavior (see INT_EN_1).

FIFO Operation

The SMI230 offers two integrated FIFO buffers (FIFO = First In, First Out) for accelerometer and gyroscope sensor signals, helping the user to reduce or even omit time critical read access to the sensor in order to obtain data with a high timing precision.

7.6.1 FIFO operating modes

The FIFO can be operated in different modes: FIFO (or stop-at-full) mode and STREAM mode.

- **FIFO or stop-at-full mode:** In FIFO or stop-at-full mode, the sensor values are stored in the FIFO buffer subsequently until it is full.

- **STREAM mode**: The FIFO logic deletes the oldest frame if a FIFO overflow event has been detected. All other data will be shifted accordingly.

7.6.2 FIFO interrupts

The FIFO buffers support two different types of interrupts:

- **Watermark interrupt:** Triggered, when the fill level of the FIFO buffer reaches a user-defined level.
- **FIFO-full interrupt:** Triggered, when the FIFO is full.

Accelerometer sensor FIFO buffer

The accelerometer part of SMI230 has an integrated 1024 byte data FIFO. The FIFO captures data from the data registers in frames, and each frame contains only one sample of a sensor.

7.7.1 Enabling FIFO and selecting the mode

FIFO for accelerometer sensor data is enabled by setting bit #6 in register 0x49 FIFO_CONFIG_1.

7.7

7.7.1.1 Mode selection

When STREAM mode is desired, than the bit #0 in register 0x48 FIFO_CONFIG_0 has to be cleared (set to '0', default value on power up reset).

For FIFO or stop-at-full mode, bit #0 has to be set to '1' in register 0x48.

7.7.1.2 FIFO data sampling rate

The input data rate to FIFO is the same as the configured ODR of the sensor. However, it can be reduced selecting a down-sampling factor of 2^k with k=[0, 1, ... 7]. The factor k must be written to bits #4-6 of register 0x45 FIFO_DOWNS.

7.7.1.3 FIFO synchronization with external interrupts (tag application) for the accelerometer

If the INT1 and/or INT2 pin is configured as input pin (by setting int2_io in register INT2_IO_CTRL and/or setting int1_io in register INT1_IO_CTRL), signals on these pins can also be recorded in the FIFO, and the frames are "tagged" accordingly. Therefore, the pins need to be activated for FIFO recording in register 0x49 FIFO_CONFIG_1.

7.7.2 Data format in FIFO

FIFO captures data in frames. The first byte is a header byte, defining the type of frame. From this, the number of consecutive bytes and their content can be derived.

The header byte consist of the header signature (first 6 bits) and two bits indicating the status of the interrupt pins INT1 and INT2 if configured accordingly.

7.7.2.1 Acceleration Sensor Data Frame

- Frame length: 7 bytes (1 byte header + 6 bytes payload)
- Header:

Bit	7	6	5	4	3	2	1	0
0 / 1	1	0	0	0	0	1	[INT2 tag]	[INT1 tag]

- Payload: the next bytes contain the sensor data in the same order as defined in the register map (addresses 0x12 – 0x17).

7.7.2.2 Skip Frame

In the case of FIFO overflows, in both FIFO and STREAM mode, a Skip Frame is prepended to the FIFO content, when read out next time. A skip frame does not consume memory in the FIFO.

- Frame length: 2 bytes (1 byte header + 1 byte payload)
- Header:

Bit	7	6	5	4	3	2	1	0
0 / 1	0	1	0	0	0	0	reserved	reserved

- Payload: one byte containing the number of skipped frames. When more than 0xFF frames have been skipped, 0xFF is returned.

7.7.2.3 Sensortime Frame

A Sensortime frame is only sent if the FIFO becomes empty during the burst read. A Sensortime frame does not consume memory in the FIFO.

- Frame length: 4 bytes (1 byte header + 3 bytes payload)
- Header:

Bit	7	6	5	4	3	2	1	0
0 / 1	0	1	0	0	0	1	reserved	reserved

- Payload: Sensortime (content of registers 0x18 – 0x1A), taken when the last byte of the last frame is read.

7.7.2.4 FIFO Input Config Frame

Whenever the filter configuration or the range of the accelerometer sensor is changed, a FIFO Input Config frame is inserted into the FIFO, before the configuration change becomes active. E.g. when the bandwidth for the accelerometer filter is changed in Register ACC_CONF, a FIFO Input Config frame is inserted before the first frame with accelerometer data with the new bandwidth configuration.

- Frame length: 2 bytes (1 byte header + 1 byte payload)
- Header:

Bit	7	6	5	4	3	2	1	0
0 / 1	0	1	0	0	1	0	reserved	reserved

- Payload: The FIFO Input Config frame contains one byte of data, of which the following bits have a meaning (the content of the other bits can safely be ignored):
  - Bit #1: indicates that a configuration change through register ACC_RANGE becomes active (means for example that the range of the accelerometer was changed).
  - Bit #0: indicates that a configuration change through the registers ACC_CONF or FIFO_DOWNS becomes active (means of example that the filter settings where changed or the FIFO sampling rate was modified).

7.7.2.5 Sample Drop Frame

After a reconfiguration, indicated by the FIFO Input Config frame, the next sample may be dropped, until the sensor delivers valid data again. Instead, a Sample Drop frame is inserted at the ODR tick at which a sample was to be expected without reconfiguration.

- Frame length: 2 bytes (1 byte header + 1 byte payload)
- Header:

Bit	7	6	5	4	3	2	1	0
0 / 1	0	1	0	1	0	0	reserved	reserved

- Payload: The Sample Drop frame contains one byte of data, whose content can be ignored.

7.7.2.6 FIFO partial frame reads and over reading

When a frame is only partially (incompletely) read through the register 0x26 FIFO_DATA it will be repeated completely with the next access. In the case of a FIFO overflow between the first partial read and the second read attempt, the frame may be deleted.

When more data is read from the FIFO than it contains valid data, 0x8000 is returned.

7.7.3 FIFO Interrupts

FIFO supports two interrupts, a FIFO full interrupt and a watermark interrupt:

- FIFO full interrupt is issued when the FIFO fill level is above the full threshold. The full threshold is reached just before the last two frames are stored in the FIFO. The status of the FIFO full interrupt may be read back through the address 0x1D bit 0 (ffull_int) status bit.
- FIFO watermark is issued when the FIFO fill level is superior or equal to the watermark level defined in register FIFO_WTM (0x46 and 0x47). The status of the FIFO watermark interrupt may be read back through the address 0x1D bit 1 (fwm_int) status bit.

In order to enable/use the FIFO full or watermark interrupts they need to be mapped on the desired interrupt pin via INT1_INT2_MAP_DATA (0x58).

Both interrupts are suppressed when a read operation on the register FIFO_DATA is ongoing.

Latched FIFO interrupts will only get cleared if the status register gets read and the fill level is below the corresponding FIFO interrupt (full or watermark).

7.7.4 FIFO Reset

The user can trigger a FIFO reset by writing 0xB0 to ACC_SOFTRESET (register 0x7E).

Gyroscope sensor FIFO buffer

The gyroscope part of SMI230 features an integrated FIFO memory capable of storing up to 100 frames of data in FIFO mode. Each frame consists of three 16-bit rate_x,y,z data words, and 16 bits of interrupt data sampled at the same point in time.

7.8.1 Enabling FIFO and selecting the mode

7.8 FIFO for gyroscope sensor data is enabled by setting the appropriate FIFO mode in Register 0x3E: FIFO_CONFIG_1.

7.8.1.1 FIFO data sampling rate

The input data rate to the FIFO is the same as the configured ODR of the sensor.

7.8.1.2 FIFO synchronization using external interrupts (tag application) for the gyroscope

FIFO of the gyroscope features a mode that allows the precise synchronization of external events with the gyroscope angular rate saved in the FIFO. This synchronization can be used for example for image and video stabilization applications.

For such a synchronization, either gyroscope interrupt pin INT3 or INT4 can be configured as input pin (register 0x34 BGW_SPI3_WDT_FIFO, bit 4). For this pin, the tag mode has to be enabled (register 0x34 BWG_SPI3_WDT_FIFO, bit 5). The working principle is shown in below figure:

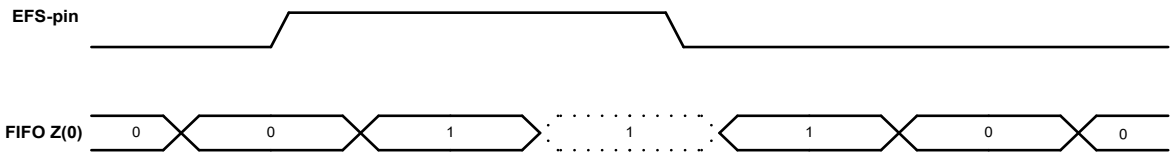


Figure 29 Timing diagram for external FIFO synchronization

EFS-pin is the Interrupt pin configured as input pin to capture external events. FIFO Z(0) is the least significant bit of the z-axis gyro data stored in the FIFO.

In this tag mode, the least significant bit of the z-axis is used as a tag-bit, therefore losing its meaning as gyroscope data bit. The remaining 15 bits of the z-axis gyroscope data keep the same meaning as in standard mode.

Once the pin, which is configured as input pin for the tag mode, is set to high level, the next FIFO word will be marked with a tag (z-axis LSB = 1). While this pin is kept at a high level, the corresponding FIFO words will continuously be tagged. After the pin is reset to low level, the immediate next FIFO word could still be tagged, and only after this word, the next tag will be reset (z-axis LSB=0). This is shown in the above diagram.

The tag synchronizes external events with the same time precision as the FIFO update rate. Therefore update rate of the tag is determined by the output data rate.

7.8.2 FIFO Data Readout

FIFO stores the data that are also available at the read-out registers 0x02-0x07. Thus, all configuration settings apply to the FIFO data as well as the data readout registers. FIFO read out is possible through Register 0x3F: FIFO_DATA. The readout can be performed using burst mode. A single burst can read out one or more frames at a time. If a frame is not read completely due to an incomplete read operation, the remaining part of the frame is lost. In this case the FIFO aligns to the next frame during the next read operation.

The data format is described in register 0x3F FIFO_DATA.

7.8.2.1 Interface speed requirements for Gyroscope FIFO use

In order to use FIFO effectively, larger blocks of data need to be read out quickly. Depending on the output data rate of the sensor, this can impose requirements on the interface.

The output data rate of the gyroscope is determined by the filter configuration (see the data sheet of the sensor). What interface speed is required depends on the selected rate.

- For a TWI speed of 400 kHz, every filter mode can be used.
- For a TWI speed of 200 kHz, only modes with an output data rate of 1 KHz and below are recommended.
- For a TWI speed of 100 kHz, only modes with an output data rate of 400 Hz and below are recommended.

7.8.3 FIFO Frame Counter and Overrun Flag

The frame counter (address 0x0E bits<6:0>, FIFO_STATUS) indicates the current fill level of the buffer. If additional frames are written to the buffer although FIFO is full, the overrun flag (register 0x0E bit 7) is set. If FIFO is reset, the FIFO fill level indicated in the frame_counter<6:0> is set to ‘0’ and the overrun flag is reset each time a write operation happens to the FIFO configuration registers.

Note: the overrun bit is not reset when FIFO fill level frame_counter<6:0> has decremented to ‘0’ due to reading from the FIFO_DATA register, but only when a write operation is performed on FIFO configuration registers.

7.8.4 FIFO Interrupts

FIFO supports two interrupts, a FIFO full interrupt and a watermark interrupt:

- **FIFO full interrupt** is issued when the buffer has been fully filled with samples. In FIFO mode this occurs after 100 samples, and in STREAM mode after 99 samples, have been stored in a previously empty FIFO.
  The status of FIFO-full interrupt may be read back through the status bit in INT_STATUS_1 register 0x0A.
- The **watermark interrupt** is issued when the fill level in the buffer has reached the frame number defined by the water mark level trigger in 0x3D. The status of the watermark may be read back through the address 0x0A bit 4 (fifo_int) status bit. Writing to water mark level trigger in register 0x3D clears the FIFO buffer.

Interrupt Features

For the SMI230, different features can be enabled by loading a specific binary file (*smi230_features_config.bin*) into the processing unit of the accelerometer part. The upload is described in section 7.9.1.

Activated features:

7.9

- DataSync
- Any-motion / Slope
- High-g
- Low-g
- Orientation
- No-motion

The functionality of these features is described from section 7.10 to 7.15 .

7.9.1 Upload of the config file

1. Load Config file
    a. Download config from Bosch MEMS Sensors · GitHub
    b. Load *smi230_features_config.bin* to an uint8 smi230_cfg_data array
2. Initialize ACC Asic to uploading
    a. Send Soft-Reset to the sensor, Reg: 0x7E, Value: 0xB6 then wait for 0.15 sec
    b. Set ACC_PWR_CTRL, Reg: 0x7D, Value: 0x00
    c. Set ACC_PWR_CONF, Reg: 0x7C, Value: 0x00
    d. Set INIT_CTRL, Reg 0x59, Value 0x00
    e. Perform a short sleep in program code, sleep 0.15 sec
3. Upload config
    a. Send smi230_cfg_data array via I2C/SPI in for loop.
    b. Start index of loop is 0 (i = 0), step size is 2 (step = 2).
    Start index of config pointer is 0 (BIN_pointer = 0), step size is 1 (BIN_pointer++)
        i. Send actual BIN_pointer_MSB, Reg: 0x5C, Value: (BIN_pointer >> 4)
        ii. Send actual BIN_pointer_LSB, Reg: 0x5B, Value: (BIN_pointer & 0x0F)
        iii. Use „burst-write” in I2C/SPI write function
            1. Send two bytes from smi230_cfg_data (next two element) into ACC_FEATURE_CFG register
            2. ACC_FEATURE_CFG, Reg: 0x5E, Value: [smi230_cfg_data[i], smi230_cfg_data[i+1]]
        iv. Increment BIN_pointer to next index (BIN_pointer++)
        v. End of for loop
    c. Step size of loop could be set to any higher value, but make sure it is a power of 2 number and adjust the config pointer index step to it. ex.: step = 32,
    d. config_step = 16.
4. Finalize and check config upload
    a. Set INIT_CTRL, Reg 0x59, Value 0x01
    b. Perform a short sleep in program code, sleep 0.15 sec
    c. Read and check config status register
        i. Config_STATUS_MASK = 0x1F
        ii. Config_STATUS, Reg: 0x2A
        iii. (Value & Config_STATUS_MASK) should be 1 in result
        iv. 1 -> ASIC initialization is OK
5. Set ACC_PWR_CTRL, Reg: 0x7D, Value 0x04
6. Perform a short sleep in program code, sleep 0.15 sec

7.9.2 Read and write feature configurations

To read the feature configuration settings from the SMI230 or to change the feature configurations, the register 0x5E (ACC_FEATURE_CFG) is used.

Note that data in the ACC_FEATURE_CFG is always in 16 bit words, therefore transaction must be in even numbers of bytes. Thus, it is also mandatory to support burst-read/-write of at least 2 bytes. For example, a burst-read of 4 bytes on ACC_FEATURE_CFG register will read two 16 bit words from the INT registers, i.e. INT_ANYMOT_TH (0x000) and INT_ANMOT_EN (0x001).

Generally, for changing a configuration in any INT register 0x00α (for $\alpha = 0,1,\dots 9,A,\mathrm{B},\mathrm{C}$), the following procedure has to be followed:

1) Create uint16 array `feature_reg` [$\alpha + 1$]
2) Burst-Read feature configuration register 0x5E up to [(0x00α +1)*2] bytes and store in feature_reg array
3) Change content of desired register
4) Burst-Write back `feature_reg` to 0x5E

For SPI, Reading from and writing to register 0x5E is only supported in multiples of 16bit words, therefore writing to it would be minimum (8bit R/W+address + 16bit data) and reading from it would be minimum (8bit R/W+address + 8bit dummy + 16bit data).

7.9.3 Example

Case: Enable Any-motion interrupt feature for all axis for the default duration 100 ms with the default threshold (124 mg for 16 g range setting) after successful upload of the configuration file.

Default content of INT register 0x000 and 0x001 (see register map):

Register	MSB content <15:8>	LSB <7:0>	Comment
0x000	0x00	0xAA	feature disabled (bit <11> = 0), default threshold is set
0x001	0xE0	0x05	x/y/z axes are activated for the feature, default duration is set

Target register content after configuration:

Register	MSB content <15:8>	LSB <7:0>	Comment
0x000	0x08	0xAA	feature enabled (bit <11> = 1), default threshold is set
0x001	0xE0	0x05	x/y/z axes are activated for the feature, default duration is set

1) Create uint16_t `feature_reg[2]`// create array with 2 elements
2) Read feature configuration register 0x5E up to 4 bytes [(0x001+1)*2] // read 0x5E (4 bytes) burst read

   Output: (note, that MSB-part and LSB-part are switched)

```
DE            AA00              05E0          // Read 0x5E
SPI start     feature_reg[0]    feature_reg[1]    //Default values
              0x00AA            0xE005
```

3) Set `feature_reg[0]` to 0x08AA
4) Write back feature_reg[] array to register 0x5E

```
5E00          AA08                05E0
SPI start     feature_reg[0]      feature_reg[1]
              0x08AA              0xE005
```

7.10 Data Synchronization

To achieve data synchronization on SMI230, the signal from the gyroscope of the SMI230 needs to be connected to one of the interrupt pins of the SMI230 accelerometer (which can be configured as input pins). The internal signal processing unit of the accelerometer uses the data ready signal from the gyroscope to synchronize and interpolate the data of the accelerometer, considering the group delay of the sensors. The accelerometer part can then notify the host of available data. With this technique, it is possible to achieve synchronized data and provide accelerometer data at an ODR up to
2 kHz. The data synchronization feature supports 400 Hz, 1 kHz and 2 kHz data rates.

7.10.1 Concept

Synchronized data means that the acquisition of the gyroscope and accelerometer data is happening at the same time and the signals have the same propagation time. The time between a motion and the register read-out depends on the sensor-specific physical propagation time, which is mainly caused by the signal filtering path and the analog-to-digital conversion. The typical group delay of the gyroscope and accelerometer signals is disclosed in the tables below.

Accelerometer output data rate (Hz)	Group delay (ms)
1600	typ. 0.625
800	typ. 1.25
400	typ. 2.5

Gyroscope output data rate (Hz)	Group delay (ms)
2000	typ. 1.5
1000	typ. 2.5
400	typ. 7.0

The synchronization between accelerometer and gyroscope data to a common point of time and a common group delay can be realized with the help of the internal processing unit of the accelerometer. This unit measures the timestamp of the accelerometer analog-to-digital conversion data ready signal and the timestamp of the gyroscope data ready signal. Finally, it interpolates the acceleration data by using the timestamp difference and the known group delay of every signal path, stores the synchronized data in the general purpose register and sets the interrupt data ready pin to high. The synchronized sensor data can then be read from the accelerometer and gyroscope data registers by the host. The refresh rate of the registers is linked to the gyroscope data rate (400 Hz, 1 kHz, 2 kHz).

7.10.2 Application schematic

The typical application circuit diagram for using the SMI230 synchronized data output is shown in the figure 30 below. The SMI230 interrupt pins INT1 (ACC) and INT3 (GYR) have to be connected externally on the PCB. The GYR new data interrupt needs to be mapped to INT3, while INT1 needs to be configured as an input pin, see section 7.10.3. For a data ready host notification, the interrupt pin INT2 (ACC) shall be used.

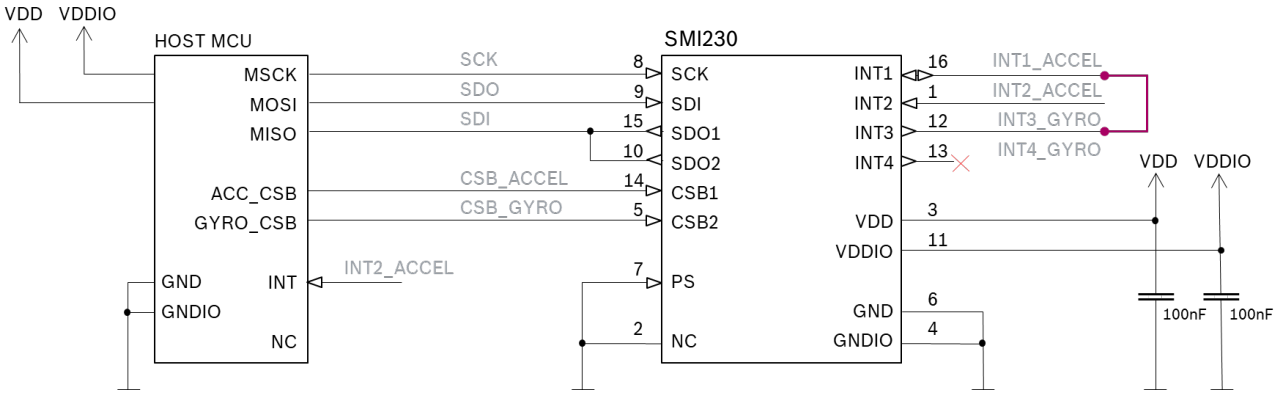


Figure 30 Typical application diagram for using the SMI230 synchronized data

The DataSync feature can be activated for different sampling rates of 400 Hz / 1000 Hz / 2000 Hz. It is activated by writing 0x1 / 0x2 / 0x3 in register 0x002 (INT_DATASYNC). To deactivate DataSync, write 0x0 to register 0x002.

The interrupt status is stored in bit 0 (*data_sync_out*) in register 0x1C (INT_STATUS_0).

As soon as the host will be notified by the SMI230 new data interrupt (INT2), the synchronized IMU data can be read from the data registers. The angular rate data can be read from data registers (0x02 – 0x07) of the gyroscope part, while the synchronized acceleration data can be found in the general purpose data registers (0x1E/0x1F, 0x20/0x21, and 0x27/0x28) of the accelerometer part. In addition to the synchronized data, the raw acceleration data and if required the sensor time can be read from the appropriate registers. The acceleration data is stored in the following data registers of the accelerometer part:

1) Raw sensor data at 0x12 (length 6 bytes: *ax, ay, az*)
2) Synchronized accelerometer data
   - *ax*: 0x1E (LSB) and 0x1F (MSB)
   - *ay*: 0x20 (LSB) and 0x21 (MSB)
   - *az*: 0x27 (LSB) and 0x28 (MSB)

The sensor time can be read out at 0x18 (length = 3 bytes).

7.10.3 Sensor configuration

In order to use the data synchronization feature of the SMI230, several sensor configuration steps are required and have to be applied after every power on reset (POR) or soft reset. Besides the actual sensor configuration, it is furthermore required to load a specific binary code (*smi230_features_config.bin*) into the processing unit of the accelerometer part.

smi230_features_config.bin is under BSD license and can be downloaded from the following link: https://github.com/boschmemssolutions

1. **Enable Data-synchronization mode**
   a. Set BIN_pointer to 0x0102 (BIN_pointer = 0x0102)
   b. Send BIN_pointer_MSB, Reg: 0x5C, Value: (BIN_pointer >> 4)
   c. Send BIN_pointer_LSB, Reg: 0x5B, Value: (BIN_pointer & 0x0F)
   d. Use „burst-write" in I2C/SPI write function
      i. Send Settings_1 = 0x0003 into ACC_FEATURE_CFG register to enable synchronization in 2000Hz

ii. ACC_FEATURE_CFG, Reg: 0x5E, Value: [Settings_1_LSB, Settings_1_MSB]

2. **Configure ACC and GYRO interrupts**
   a. ACC sync input config
      i. Configure INT1, Reg: 0x53, Value: 0x13 // Active high, push-pull, enable INT1 as input pin
   b. ACC sync data ready config
      i. Reg: 0x57, Value: 0x01 // Map synchronized data ready to INT2 pin
      ii. Configure INT2, Reg: 0x54, Value: 0x0A // Active high, push-pull, enable INT2 as output pin
   c. GYRO new data interrupt INT3 config
      i. Reg: 0x18, Value: 0x01 // Map new data interrupt to INT3 pin
      ii. Configure INT3, Reg: 0x16, Value: 0x1 // Active high, push-pull

7.10.4 Synchronization Feature Timings

Parameter	Time	Notes
Gyroscope sampling time	typ. 500 us	
Accelerometer sampling time	typ. 625 us	
Accelerometer synchronized data sampling time	typ. 500 us	synchronized to gyroscope new data interrupt
Accelerometer data ready latency	typ. 25 us	latency between gyroscope new data interrupt and accelerometer new data interrupt
Synchronization accuracy	typ. < 100 us	
Latency / group delay of synchronized data (motion-to-data ready)	typ. 1.5 ms @ 2 kHz ODR typ. 2.5 ms @ 1 kHz ODR typ. 7 ms @ 400 Hz ODR	

7.11 Any-Motion / Slope Detection

Any-motion /slope detection uses the slope between the current input and acceleration reference samples to detect the motion status of the device. This feature can be used with wake-up. An interrupt is generated when the slope exceeds a configurable, preset threshold. The reference acceleration sample is updated only when the any-motion interrupt is triggered. It is cleared as soon as the slope falls below the threshold.

The principle of the slope / any-motion interrupt is shown in Figure 31.

7.11.1 Configuration settings

1. Enable Anymotion mode in BIN_pointer = 0x0100 to 0x101
   a. Set BIN_pointer to 0x0100 (BIN_pointer = 0x0100)
      i. Send BIN_pointer_MSB, Reg: 0x5C, Value: (BIN_pointer >> 4)
      ii. Send BIN_pointer_LSB, Reg: 0x5B, Value: (BIN_pointer & 0x0F)
   b. Use „burst-write" in I2C/SPI write function to configure default settings and enable anymotion
      i. Send Settings_1 = 0x08AA and Settings_2 = 0xE005 into ACC_FEATURE_CFG register
      ii. ACC_FEATURE_CFG, Reg: 0x5E, Value: [Settings_1_LSB, Settings_1_MSB, Settings_2_LSB, Settings_2_MSB]
2. ACC Anymotion INT2 config
   a. ACCEL_INT2_MAP -> uc_intb = 1, Send Reg: 0x57, Value: 0x02
   b. ACCEL_INT2_IO_CONF -> Active high, Enable INT2 as output pin

Any-motion /slope detection is enabled by writing 1 to bit 11 (*anymot_en*) in register 0x000 (INT_ANYMOT_TH). The feature can be enabled (disabled) for each axis separately by writing 1 (0) to bits 13 (*en_x*), 14 (*en_y*) or 15 (*en_z*) in register 0x001 (INT_ANYMOT_EN).

The any-motion threshold is defined through register 0x000 (INT_ANYMOT_TH), bits <10:0> (*anymot_th*). For a set ACC range of 16 g, the threshold range is 0 to 1.5 g. For other ACC ranges, the threshold range adapts accordingly, as described in the following table. The default value of *anymot_th* is 0xAA.

ACC range	Corresponding resolution of anymot_*th*	max value of *anymot_th*
2 g	16384 LSB/g	187.5 mg
4 g	8192 LSB/g	375 mg
8 g	4096 LSB/g	750 mg
16 g	2048 LSB/g	1500 mg

The any-motion duration (*anymot_dur)* defines the number of consecutive data points for which the threshold condition must be respected for interrupt assertion. It is expressed in 50 Hz samples (20 ms). The range of *anymot_dur* is 0 to 163 s. It needs to be ensured, that ACC ODR ≥ 50 Hz to use this feature.

The relationship between the content of *anymot_dur* and the actual delay of the interrupt generation is given by the following equation.

$$\text{delay [ms]} = \textit{anymot\_dur} \cdot 20 \text{ ms}$$

The any-motion duration is defined through register 0x001 (INT_ANYMOT_EN), bits <12:0> (*anymot_dur*).

It can be reset to the default value (100 ms) by writing 0x5 to register 0x001.

The interrupt is generated if the slope of any of the enabled axes exceeds the threshold *anymot_th* for *anymot_dur* consecutive times. As soon as the slopes of all enabled axes fall or stay below this threshold for *anymot_dur* consecutive times, the interrupt is cleared.

The interrupt status is stored in bit 1 (*any_mot_out*) in register 0x1C (INT_STATUS_0).

Note: When any-motion interrupt is active and accelerometer is disabled and re-enabled, a false positive interrupt is triggered after re-enable. Therefore the feature should be disabled before the accelerometer is disabled.

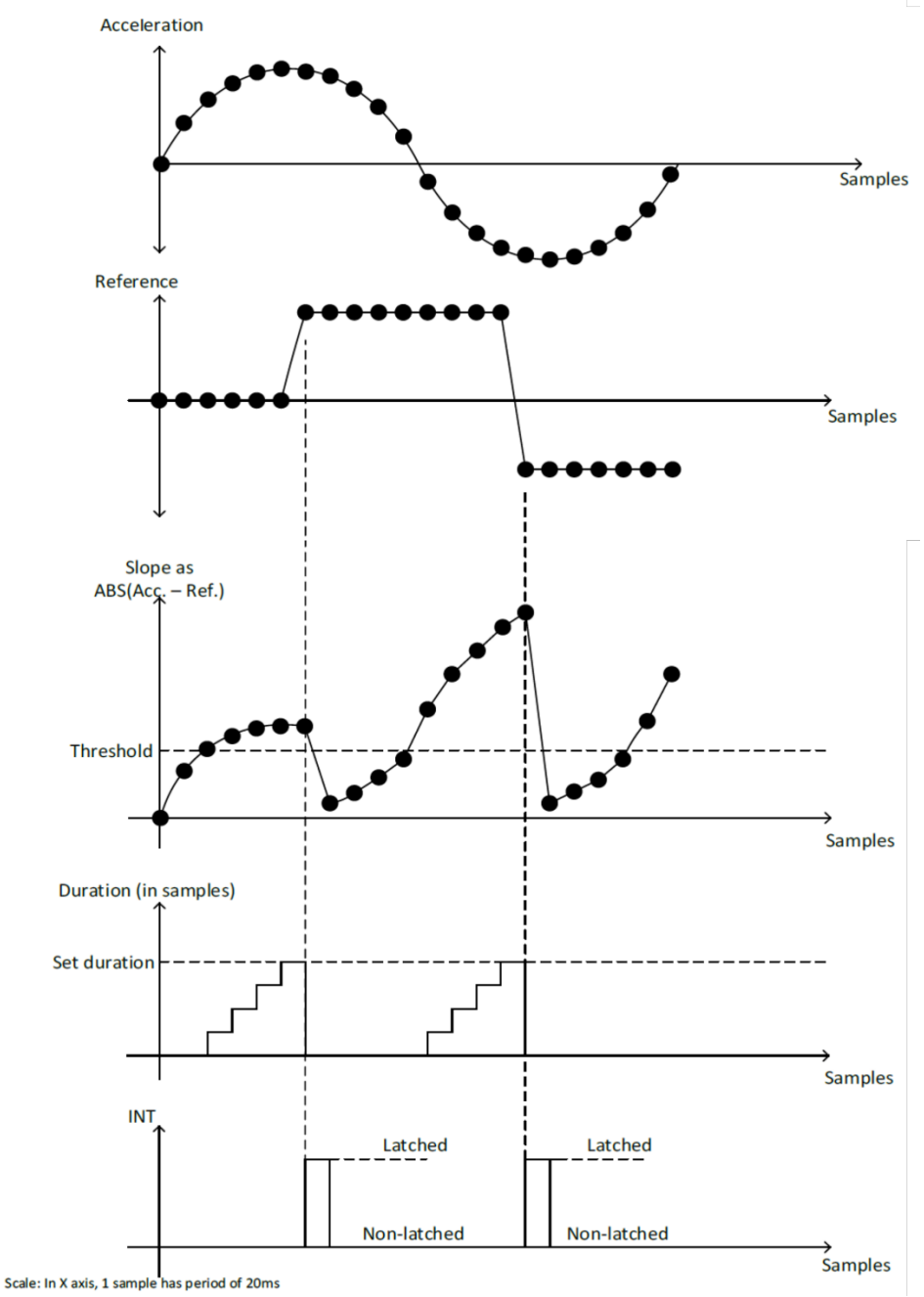


Figure 31 Principle of the slope / any-motion detection

High-g Interrupt

The high-g interrupt is based on the comparison of acceleration data against a high-g threshold for the detection of wake-up, shock, or other high-acceleration events. The interrupt is triggered if the absolute value of acceleration data of at least one enabled axis exceeds the programmed threshold and lasts as long as the set duration.

7.12.1 Configuration settings

7.12

1. Enable High-g mode in BIN_pointer = 0x0103 to 0x0105
    a. Set BIN_pointer to 0x0103 (BIN_pointer = 0x0103)
    b. Send BIN_pointer_MSB, Reg: 0x5C, Value: (BIN_pointer >> 4)
    c. Send BIN_pointer_LSB, Reg: 0x5B, Value: (BIN_pointer & 0x0F)
    d. Use „burst-write" in I2C/SPI write function to configure default settings and enable High-g
        i. Send Settings_1 = 0x0C00, Settings_2 = 0xF3E8, Settings_3 = 0x0004 into ACC_FEATURE_CFG register
        ii. ACC_FEATURE_CFG, Reg: 0x5E, Value: [Settings_1_LSB, Settings_1_MSB, Settings_2_LSB, Settings_2_MSB, Settings_3_LSB, Settings_3_MSB]
2. ACC High-g INT2 config
    a. ACCEL_INT2_MAP -> uc_intc = 1, Send Reg: 0x57, Value: 0x04
    b. ACCEL_INT2_IO_CONF -> Active high, Enable INT2 as output pin

The high-g interrupt is generally enabled (disabled) by writing 1 (0) in bit 15 (*high_en*) in register 0x004 (INT_HIGH_EN). Then, for each axis the high-g interrupt can be selected on a per axis base by writing 1 (0) to the respective bits 12 (*en_x*), 13 (*en_y*) or 14 (*en_z*) in register 0x004.

The high-g threshold is set via bits <14:0> (*high_th*) in register 0x003 (INT_HIGH_TH).

Default high-g threshold value is 0xC00.

The maximum threshold value depends on the set ACC range in the SMI230.

ACC range	Corresponding resolution of *high_th*	max value of *high_th*
2 g	16384 LSB/g	2 g
4 g	8192 LSB/g	4 g
8 g	4096 LSB/g	8 g
16 g	2048 LSB/g	16 g

A hysteresis can be selected by setting bits <11:0> (*high_hyst*) in register 0x004 (INT_HIGH_EN).

For a set ACC range of 16 g, the hysteresis range is 0 to 2 g. For other ACC ranges, the hysteresis range adapts accordingly, as described in the following table. The default value of *high_hyst* is 0x3E8.

ACC range	Corresponding resolution of *high_hyst*	max value of *high_hyst*
2 g	16384 LSB/g	250 mg
4 g	8192 LSB/g	500 mg
8 g	4096 LSB/g	1 g
16 g	2048 LSB/g	2 g

The high-g interrupt is generated if the absolute value of the acceleration of at least one of the selected axes ("or" relation) is higher than the threshold for at least the time defined by the bits <11:0> (*high_dur*) in register 0x005 (INT_HIGH_DUR). The relation between the content of *high_dur* and the actual delay of the interrupt generation is given by the following equation.

$$\text{delay [ms]} = \textit{high\_dur} \cdot 5 \text{ ms}$$

Thus, possible delay times range from 0 to 20 sec in 200 Hz samples (5 ms). It can be reset to the default value (20 ms) by writing 0x4 to register 0x005. It needs to be ensured that ACC ODR ≥ 200 Hz to use this feature.

Once the absolute value of acceleration data is lower than the threshold minus hysteresis or if the sign of acceleration value changes, the interrupt will reset immediately.

If any axis is parallel to gravitational vector, then that axis will repot ±1 g as output. In this case, it is recommended to have (threshold - hysteresis) greater than 1 g. If (threshold – hysteresis) is less than 1 g, then after high-g g interrupt is triggered, the interrupt will not get cleared if any axis is parallel to the gravitational vector, since that axis will be already at 1 g.

The interrupt status is stored in bit 2 (*high_g_out*) in register 0x1C (INT_STATUS_0). The high-g interrupt will be cleared immediately once the acceleration is lower than the threshold defined in *high_th*.

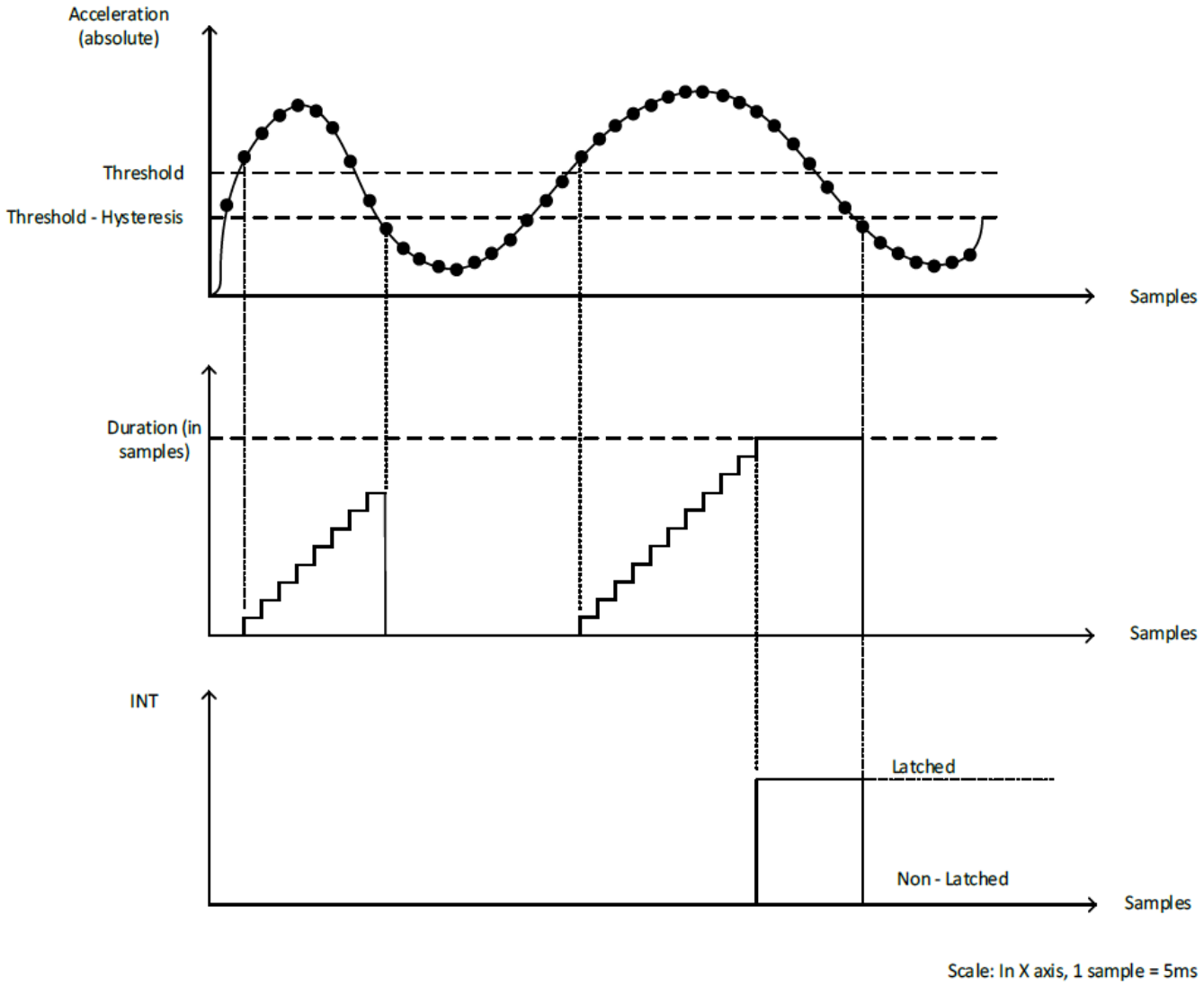


Figure 32 Principle of the high-g interrupt

Low-g Interrupt

The low-g interrupt is based on the comparison of acceleration data against a low-g threshold, which is most useful for free-fall detection. An interrupt is generated when the acceleration value goes below the set low-g threshold.

7.13.1 Configuration settings

7.13

1. Enable Low-g mode in BIN_pointer = 0x0106 to 0x0108
    a. Set BIN_pointer to 0x0106 (BIN_pointer = 0x0106)
    b. Send BIN_pointer_MSB, Reg: 0x5C, Value: (BIN_pointer >> 4)
    c. Send BIN_pointer_LSB, Reg: 0x5B, Value: (BIN_pointer & 0x0F)
    d. Use „burst-write" in I2C/SPI write function to configure default settings and enable Low-g
        i. Send Settings_1 = 0x0200, Settings_2 = 0x1100, Settings_3 = 0x0000 into ACC_FEATURE_CFG register
        ii. ACC_FEATURE_CFG, Reg: 0x5E, Value: [Settings_1_LSB, Settings_1_MSB, Settings_2_LSB, Settings_2_MSB, Settings_3_LSB, Settings_3_MSB]
2. ACC Low-g INT2 config
    a. ACCEL_INT2_MAP -> uc_intd = 1, Send Reg: 0x57, Value: 0x08
    b. ACCEL_INT2_IO_CONF -> Active high, Enable INT2 as output pin

The low-g interrupt is enabled (disabled) by writing 1 (0) to bit 12 (*low_en*) in register 0x007 (INT_LOW_EN).

The low-g threshold is set via bits <14:0> (*low_th*) in register 0x006 (INT_LOW_TH). The maximum range is 1 g. The resolution [LSB/g] of *low_th* directly relies on the set ACC range in the SMI230.

ACC measurement range	Corresponding scaling of *low_th*
2 g	16384 LSB/g
4 g	8192 LSB/g
8 g	4096 LSB/g
16 g	2048 LSB/g

A hysteresis can be selected by setting the bits <11:0> (*low_hyst*) in register 0x007 (INT_LOW_EN). The maximum range is 0 to 2 g. Recommended range for the user is 0 to 0.5 g. The resolution [LSB/g] of *low_hyst* directly relies on the set ACC range in the SMI230.

ACC measurement range	Corresponding scaling of *low_hyst*
2 g	16384 LSB/g
4 g	8192 LSB/g
8 g	4096 LSB/g
16 g	2048 LSB/g

The low-g interrupt is generated if the magnitude A of the acceleration values of all axes is lower than the threshold *low_th* for at least the time defined by the bits <11:0> (*low_dur*) in register 0x008 (INT_LOW_DUR).

$$A = \sqrt{a_x^2 + a_y^2 + a_z^2}$$

The relation between the content of *low_dur* and the actual delay of the interrupt generation is given by the following equation.

$$\text{delay [ms]} = \textit{low\_dur} \cdot 20 \text{ ms}$$

Therefore, possible delay times range from 0 ms to 82 s in 50 Hz samples (20 ms).

The interrupt is reset if the absolute value of the acceleration A is higher than the threshold plus the hysteresis for at least one data acquisition.

The interrupt status is stored in bit 3 (*low_g_out*) in register 0x1C (INT_STATUS_0).

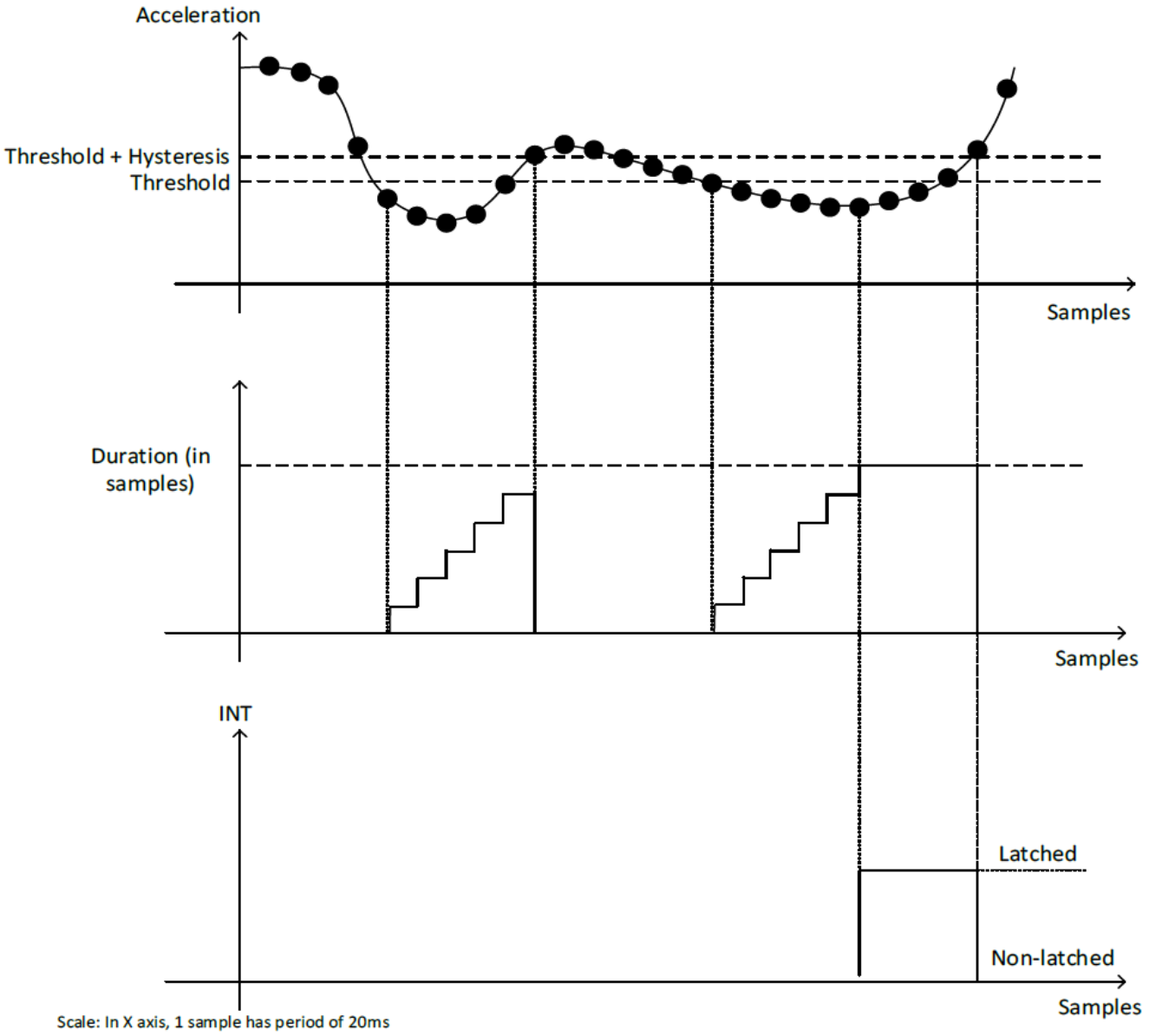


Figure 33 Principle of low-g interrupt

Orientation Detection

The orientation detection feature gives information on an orientation change of the SMI230 with respect to the gravitational field vector g. There are the orientations face up / face down, and orthogonal to that portrait upright, landscape left, portrait upside down and landscape right.

The sensor orientation is defined by the angle phi and theta (phi φ is rotation around the stationary z axis, theta θ is rotation around the stationary y axis). The measured acceleration vector components with respect to the gravitational field are defined in Figure 34.

7.14

7.14.1 Configuration settings

1. Enable Orientation mode in BIN_pointer = 0x0109 to 0x010A
    a. Set BIN_pointer to 0x0109 (BIN_pointer = 0x0109)
    b. Send BIN_pointer_MSB, Reg: 0x5C, Value: (BIN_pointer >> 4)
    c. Send BIN_pointer_LSB, Reg: 0x5B, Value: (BIN_pointer & 0x0F)
    d. Use „burst-write" in I2C/SPI write function to configure default settings and enable Orientation
        i. Send Settings_1 = 0x0A30 and Settings_2 = 0x0080 into ACC_FEATURE_CFG register
        ii. ACC_FEATURE_CFG, Reg: 0x5E, Value: [Settings_1_LSB, Settings_1_MSB, Settings_2_LSB, Settings_2_MSB]
2. ACC Orientation INT2 config
    a. ACCEL_INT2_MAP -> uc_inte = 1, Send Reg: 0x57, Value: 0x10
    b. ACCEL_INT2_IO_CONF -> Active high, Enable INT2 as output pin

The orientation recognition is activated (deactivated) by writing 1 (0) to bit 0 in register 0x009 (INT_ORIENT_EN). The interrupt for face up / face down may be enabled separately through bit 1 (*ud_en*) in register 0x009 (INT_ORIENT_EN).

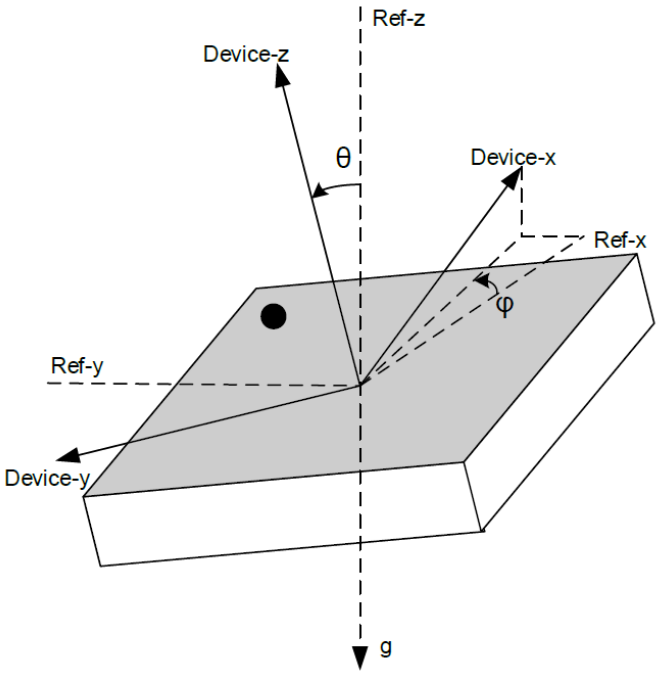


Figure 34 Definition of the coordinate system with respect to pin marker 1

The calculation of the magnitudes of the different acceleration vectors is given by the following equations:

$$acc_x = 1\,\mathrm{g} \cdot \sin\theta \cdot \cos\varphi$$

$$acc_y = -1\,\mathrm{g} \cdot \sin\theta \cdot \sin\varphi$$

$$acc_z = 1\,\mathrm{g} \cdot \cos\theta$$

$$\frac{acc_y}{acc_x} = -\tan\varphi$$

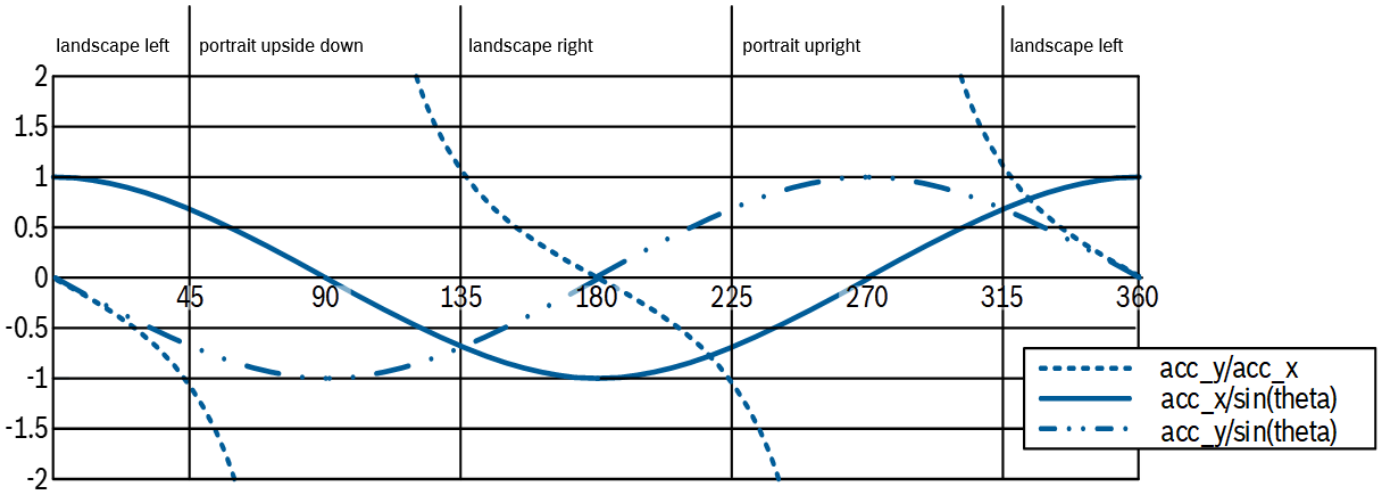


Figure 35 Typical orientation switching conditions without hysteresis

Depending on the magnitudes of the acceleration vectors, the orientation of the SMI230 is determined and stored in bits <2:0> in register 0x29 (INT_ORIENT_RES).

There are three orientation calculation modes with different thresholds for switching between different orientations: symmetrical, high-asymmetrical and low-asymmetrical mode. The mode is selected by setting the bits <3:2> (*orient_mode*) in register 0x009 (INT_ORIENT_EN) as given in the following table. Default value is Bit 2 = Bit 3 = 0.

Bit 3	Bit 2	Orientation Mode
0	0	symmetrical
0	1	high-asymmetrical
1	0	low-asymmetrical
1	1	symmetrical

The output *orient_pl* (portrait/landscape, bits <1:0> in register 0x29 (INT_ORIENT_RES)) has the following meaning depending on the switching mode, shown in the following tables for the symmetrical, high-asymmetrical, and low-asymmetrical mode.

Symmetrical Mode

orient_pl	Name	Angle	Condition 1 AND Condition 2	
x01	landscape left	315° < φ < 45°	$\lvert acc_y \rvert < \lvert acc_x \rvert$	$acc_x \geq 0$
x11	landscape right	135° < φ < 225°	$\lvert acc_y \rvert < \lvert acc_x \rvert$	$acc_x < 0$
x10	portrait upside down	45° < φ < 135°	$\lvert acc_y \rvert \geq \lvert acc_x \rvert$	$acc_y < 0$
x00	portrait upright	225° < φ < 315°	$\lvert acc_y \rvert \geq \lvert acc_x \rvert$	$acc_y \geq 0$

High-Asymmetrical Mode

orient_pl	Name	Angle	Condition 1 AND Condition 2	
x01	landscape left	297° < φ < 63°	$\lvert acc_y \rvert < 2 \cdot \lvert acc_x \rvert$	$acc_x \geq 0$
x11	landscape right	117° < φ < 243°	$\lvert acc_y \rvert < 2 \cdot \lvert acc_x \rvert$	$acc_x < 0$
x10	portrait upside down	63° < φ < 117°	$\lvert acc_y \rvert \geq 2 \cdot \lvert acc_x \rvert$	$acc_y < 0$
x00	portrait upright	243° < φ < 297°	$\lvert acc_y \rvert \geq 2 \cdot \lvert acc_x \rvert$	$acc_y \geq 0$

Low-Asymmetrical Mode

orient_pl	Name	Angle	Condition 1 AND Condition 2	
x01	landscape left	333° < φ < 27°	$\lvert acc_y \rvert < 0.5 \cdot \lvert acc_x \rvert$	$acc_x \geq 0$
x11	landscape right	153° < φ < 207°	$\lvert acc_y \rvert < 0.5 \cdot \lvert acc_x \rvert$	$acc_x < 0$
x10	portrait upside down	27° < φ < 153°	$\lvert acc_y \rvert \geq 0.5 \cdot \lvert acc_x \rvert$	$acc_y < 0$
x00	portrait upright	207° < φ < 333°	$\lvert acc_y \rvert \geq 0.5 \cdot \lvert acc_x \rvert$	$acc_y \geq 0$

For upside or downside orientation, the respective bit of the output *orient_fud* (face up/down), bit 2 in register 0x29 (INT_ORIENT_RES)) has the definition:

orient_fud	acc_z
value 0 = face up	270° < θ < 90° → acc_z ≥ 0
value 1 = face down	90° < θ < 270° → acc_z < 0

Value after device initialization is 0x0 i.e. face up.

Both portrait/landscape and face up/down recognition use a hysteresis. The hysteresis for portrait/landscape definition is configurable and applies to all conditions as described in the tables below.

Symmetrical Mode

orient_pl	Name	Angle	Condition 1 AND Condition 2	
x01	landscape left	315° +hyst < φ < 45° - hyst	$\lvert acc_y \rvert < \lvert acc_x \rvert$ - hyst	$acc_x \geq 0$
x11	landscape right	135° + hyst < φ < 225° - hyst	$\lvert acc_y \rvert < \lvert acc_x \rvert$ - hyst	$acc_x < 0$
x10	portrait upside down	45° + hyst < φ < 135° - hyst	$\lvert acc_y \rvert \geq \lvert acc_x \rvert$ + hyst	$acc_y < 0$
x00	portrait upright	225° + hyst < φ < 315° - hyst	$\lvert acc_y \rvert \geq \lvert acc_x \rvert$ + hyst	$acc_y \geq 0$

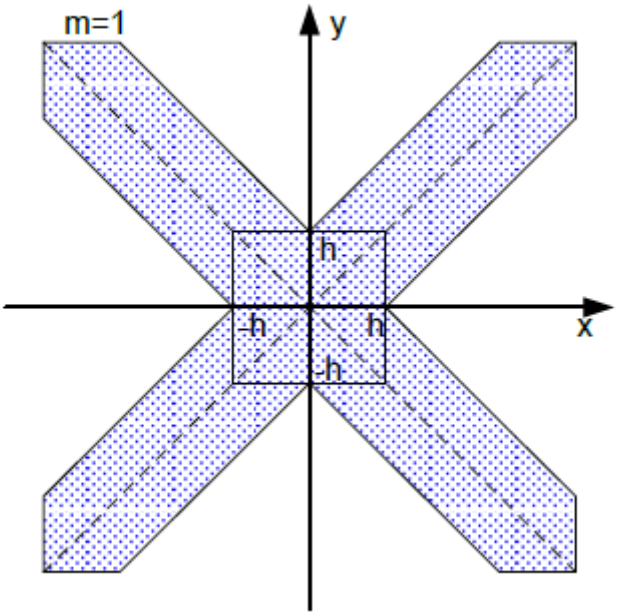


Figure 36 Hysteresis in symmetrical mode

High-Asymmetrical Mode

orient_pl	Name	Angle	Condition 1 AND Condition 2	
x01	landscape left	297° + hyst < φ < 63° - hyst	$\lvert acc_y \rvert < 2 \cdot (\lvert acc_x \rvert$ - hyst)	$acc_x \geq 0$
x11	landscape right	117° + hyst < φ < 243° - hyst	$\lvert acc_y \rvert < 2 \cdot (\lvert acc_x \rvert$ - hyst)	$acc_x < 0$
x10	portrait upside down	63° + hyst < φ < 117° - hyst	$\lvert acc_y \rvert \geq 2 \cdot \lvert acc_x \rvert$ + hyst	$acc_y < 0$
x00	portrait upright	243° + hyst < φ < 297° - hyst	$\lvert acc_y \rvert \geq 2 \cdot \lvert acc_x \rvert$ + hyst	$acc_y \geq 0$

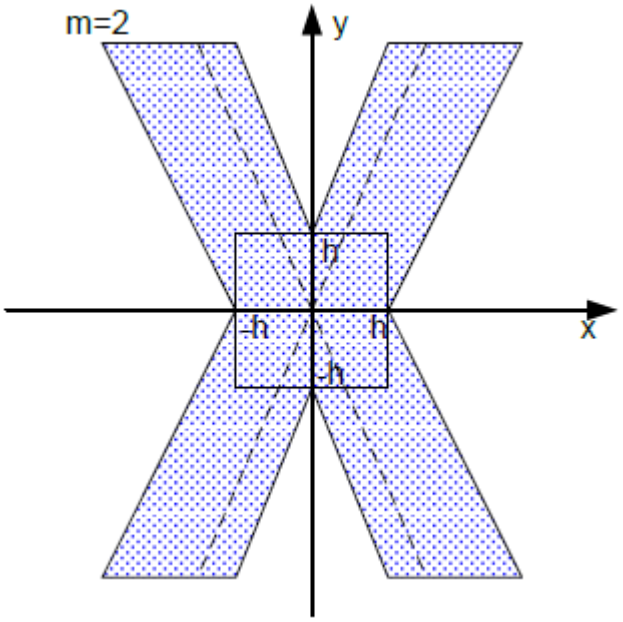


Figure 37 Hysteresis in high asymmetrical mode

Low-Asymmetrical Mode

orient_pl	Name	Angle	Condition 1 AND Condition 2	
x01	landscape left	333° + hyst < φ < 27° - hyst	$\lvert acc_y \rvert < 0.5 \cdot (\lvert acc_x \rvert$ - hyst)	$acc_x \geq 0$
x11	landscape right	153° hyst < φ < 207° - hyst	$\lvert acc_y \rvert < 0.5 \cdot (\lvert acc_x \rvert$ - hyst)	$acc_x < 0$
x10	portrait upside down	27° + hyst < φ < 153° - hyst	$\lvert acc_y \rvert \geq 0.5 \cdot \lvert acc_x \rvert$ + hyst	$acc_y < 0$
x00	portrait upright	207° + hyst < φ < 333° - hyst	$\lvert acc_y \rvert \geq 0.5 \cdot \lvert acc_x \rvert$ + hyst	$acc_y \geq 0$

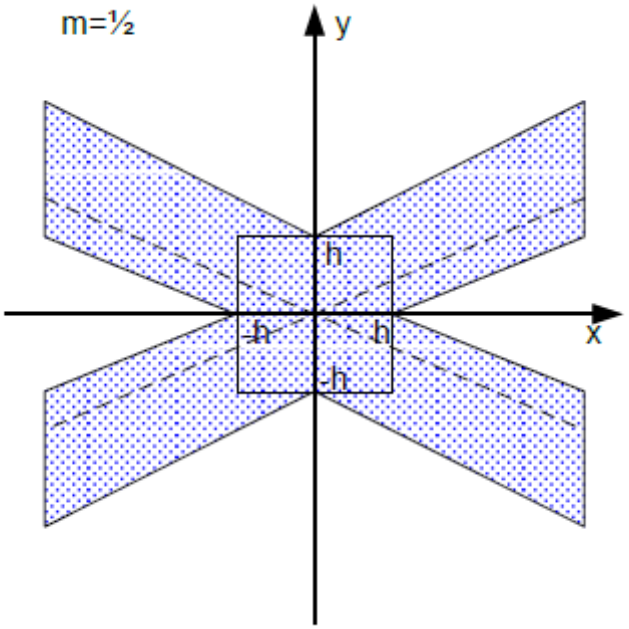


Figure 38 Hysteresis in low asymmetrical mode

In these tables, the parameter *hyst* stands for a hysteresis that can be selected by setting the bits <10:0> (*orient_hyst*) in register 0x00A (INT_ORIENT_HYST). Please note that by using a hysteresis ≠ 0, the actual switching angles become different from the angles given in the tables above since there is an overlap between the different orientations. Default value of *orient_hyst* is 0x80.

ACC measurement range	Corresponding scaling of *orient_hyst*	max value of *orient_hyst*
2 g	16384 LSB/g	125 mg
4 g	8192 LSB/g	250 mg
8 g	4096 LSB/g	500 mg
16 g	2048 LSB/g	1000 mg

The hysteresis for upside / downside *orient_fud* ((face up/down), bit 2 in register 0x29 (INT_ORIENT_RES)) detection is fixed to 11.5° which is ~ 200 mg

orient_fud	Angle	Condition
value 0 = face up	281.5° < θ < 78.5°	acc_z > 200 mg (|acc_z| > 200 mg and acc_z ≥ 0)
value 1 = face down	101.5° < θ < 258°	acc_z < -200 mg (|acc_z| < 200 mg and acc_z < 0)

Blocking mode:

The orientation blocking mode feature may be used to avoid undesired orientation change detection e.g. if the device is nearly flat or in motion. The configuration of the blocking mode is done via bits <5:4> (*orient_blocking*) in register 0x009 (INT_ORIENT_EN) as shown in the following table. The default value is 0x3 (Bit 4 = Bit 5 = 1).

orient_blocking		Conditions
Bit 5	Bit 4	
0	0	no blocking
0	1	theta blocking (interrupt blocked if device close to horizontal position) or acceleration in any axis > 1.5 g
1	0	theta blocking (interrupt blocked if device close to horizontal position) or acceleration slope in any axis > 0.2 g or acceleration in any axis > 1.5 g
1	1	theta blocking (interrupt blocked if device close to horizontal position) or acceleration slope in any axis > 0.4 g or acceleration in any axis > 1.5 g or another change within 100 ms (In this mode, to trigger the interrupt, the detected orientation has to remain the same (stable) until the timer for 100 ms expires. The timer starts to count when orientation changes between two consecutive samples. If the orientation changes while the timer is still counting, the timer is restarted.)

The theta blocking is defined by the following inequality: theta = 64 * (tan(angle)^2)

It denotes the coded vale of the threshold angle with the horizontal plane, used in the blocking modes. Default value is 40, equivalent to 38 degree angle.

The interrupt status is stored in bit 4 (*orient_out*) in register 0x1C (INT_STATUS_0).

Per default, an orientation interrupt is triggered when any of the *orient* bits (bits <2:0> in register 0x29 (INT_ORIENT_EN) change their state.

The SMI230 can be configured to trigger orientation interrupts only when the device position changes in the x-y-plane while orientation changes with respect to the z-axis are ignored. A change of the orientation of the z-axis and hence a state change of bit 2 (*orient_fud*) in register 0x29 is ignored (considered) when bit 1 (*ud_en*) in register 0x009 (INT_ORIENT_EN) is set to 0 (1). The default value of *ud_en* is 0.

No-Motion Detection

No-motion detection uses the slope between two consecutive acceleration signal samples to detect the static state of the device. In no-motion mode, an interrupt is generated if the slope of all enabled axes remains smaller than a configurable threshold for a configurable duration. The signals and timings relevant to the no-motion interrupt functionality are depicted in Figure 39.

7.15.1 Configuration settings

7.15

1. Enable No-motion mode in BIN_pointer = 0x010B to 0x10C
    a. Set BIN_pointer to 0x010B (BIN_pointer = 0x010B)
    b. Send BIN_pointer_MSB, Reg: 0x5C, Value: (BIN_pointer >> 4)
    c. Send BIN_pointer_LSB, Reg: 0x5B, Value: (BIN_pointer & 0x0F)
    d. Use „burst-write" in I2C/SPI write function to configure default settings and enable No-motion
        i. Send Settings_1 = 0x08AA and Settings_2 = 0xE005 into ACC_FEATURE_CFG register
        ii. ACC_FEATURE_CFG, Reg: 0x5E, Value: [Settings_1_LSB, Settings_1_MSB, Settings_2_LSB, Settings_2_MSB]
2. ACC No-motion INT2 config
    a. ACCEL_INT2_MAP -> uc_intf = 1, Send Reg: 0x57, Value: 0x20
    b. ACCEL_INT2_IO_CONF -> Active high, Enable INT2 as output pin

The feature is enabled by writing 1 to bit 11 (*not_mot_en)* in register 0x00B (INT_NO_MOT_TH). The feature can be enabled for each axis individually via bits 13 (*en_x*), 14 (*en_y*) and 15 (*en_z*) in register 0x00C (INT_NO_MOT_EN).

The threshold can be configured by means of bits <10:0> (*no_mot_th)* in register 0x00B (INT_NO_MOT_TH).

For a set ACC range of 16 g, the threshold range is 0 to 1 g. For other ACC ranges, the threshold range adapts accordingly, as described in the following table. The default value of *no_mot_th* ix 0xAA.

ACC range	Corresponding resolution of anymot_*th*	max value of *no_mot_th*
2 g	16384 LSB/g	125 mg
4 g	8192 LSB/g	250 mg
8 g	4096 LSB/g	500 mg
16 g	2048 LSB/g	1000 mg

The no-motion duration (*no_mot_dur)* defines the number of consecutive data points for which the slope of the enabled axis must be smaller than the threshold for an interrupt to be asserted. It is expressed in 50 Hz samples (20 ms). The range of *no_mot_dur* is 0 to 163 s. It needs to be ensured that ACC ODR ≥ 50 Hz to use this feature.

The relation between the content of *no_mot_dur* and the actual delay of the interrupt generation is given by the following equation.

$$\text{delay [ms]} = \textit{no\_mot\_dur} \cdot 20 \text{ ms}$$

The no-motion duration is defined through register 0x00C (INT_NO_MOT_EN), bits <12:0> (*no_mot_dur*).

It can be reset to the default value (100 ms) by writing 0x5 to register 0x00C (INT_NO_MOT_EN).

The interrupt status is stored in bit 5 (*no_motion_out*) in register 0x1C (INT_STATUS_0).

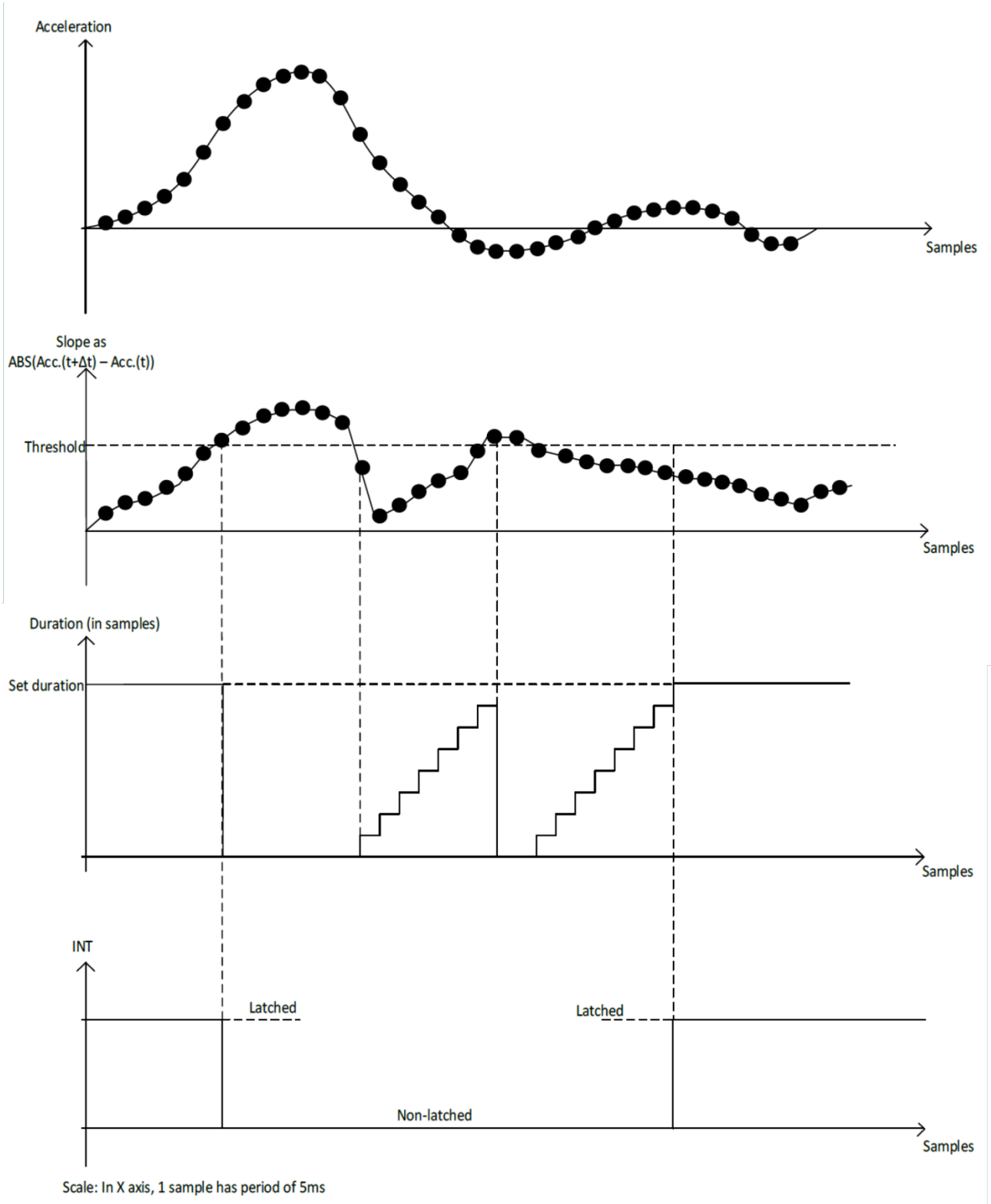


Figure 39 Timing of the no-motion interrupt

Self-test

7.16.1 Accelerometer

The self-test feature allows for checking the sensor functionality by applying electrostatic forces to the sensor core instead of external accelerations. By physically deflecting the seismic mass, the entire signal path of the sensor is tested. Activation of the self-test results in a static offset in the acceleration data. Any external acceleration or gravitational force that is applied to the sensor during a self-test will be observed in the sensor output as a superposition of the acceleration and the self-test signal.

7.16

The recommended self-test procedure is as follows:

1) Set ±16 g range by writing 0x03 to register ACC_RANGE (0x41)
2) Set ODR=1.6 kHz, continuous sampling mode, “normal mode” (norm_avg4) by writing 0xAC to register ACC_CONF (0x40)
3) Wait for > 2 ms
4) Enable the positive self-test polarity by writing 0x0D to register ACC_SELF_TEST (0x6D)
5) Wait for > 50 ms
6) Read the accelerometer offset values for each axis (positive self-test response)
7) Enable the negative self-test polarity by writing 0x09 to register ACC_SELF_TEST (0x6D)
8) Wait for > 50 ms
9) Read the accelerometer offset values for each axis (negative self-test response)
10) Disable the self-test by writing 0x00 to register ACC_SELF_TEST (0x6D)
11) Calculate the difference of positive and negative self-test response and compare with the expected values (see table below)
12) Wait for > 50 ms to let the sensor settle to normal mode steady state operation

The minimum difference for each axis is shown in the table below. The measured signal differences can be significantly larger.

	x-axis	y-axis	z-axis
minimum difference signal	1000 mg	1000 mg	500 mg

After performing a self-test, a reset of the device is recommended. If the reset cannot be performed, the following sequence must be kept to prevent unwanted interrupt generation:

- **A.** Disable interrupts
- **B.** Change parameters of interrupts
- **C.** Wait for at least 50 ms
- **D.** Enable desired interrupts

Note: An external stimulus during the self-test procedure might lead to wrong sensor reading for the specific axis. This might result in a failure of the self-test. A repetition of the self-test is recommended in this case.

7.16.2 Gyroscope

A built-in self-test (BIST) has been implemented, which provides a quick way to determine if the gyroscope is operational within the specifications.

The BIST uses three parameters for the evaluation of proper device operation:

- Drive voltage regulator
- Sense frontend offset regulator of x-, y- and z-channel
- Quad regulator for x-, y- and z-channel

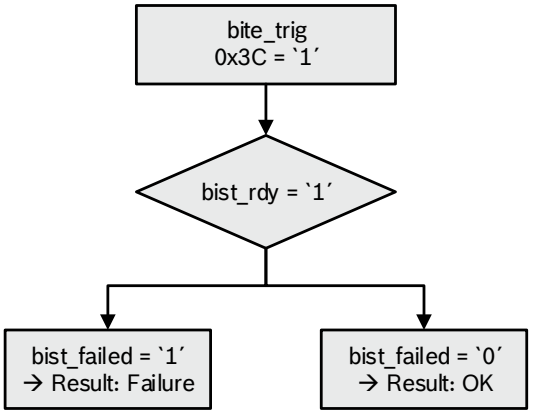


Figure 40 SMI230 BIST sequence

If any of the three parameters is not within the limits, the BIST results in a ‘fail’.

To trigger the BIST, set bit 0 (*trig_bist*) in register GYR 0x3C (*BIST*) to 1.

Two bits (read-only) have to be checked in register GYR 0x3C (*BIST*):

- bit 1(*bist_rdy*)
- bit 2 (*bist_fail*)

bist_rdy = 1 indicates that a test was performed. *bist_fail* contains the result of the BIST. *bist_fail* = 1 corresponds to a ‘fail’.

A simple option to check for the sensor status is to read out bit 4 (*rate_ok*) in register GYR 0x3C (*BIST*). No trigger is needed for this, and proper sensor function is indicated by a 1.

A waiting time of 50 ms is mandatory after enabling the self-test.

Note: In contrast to the self-test of the accelerometer, the BIST of the gyroscope is fully decoupled from the sensing element. This means that the MEMS element is not deflected, and the current state of the MEMS element (e.g. its orientation) has no influence on the result of the BIST.

Reading Data

7.17.1 Accelerometer

For each axis the sensor output is stored as a signed 16-bit number in 2's complement format in each 2 registers, split into a MSB upper part (bits <15:8> of acceleration data) and a LSB lower part (bits <7:0> of acceleration data). From the registers, the acceleration values can be calculated as follows:

7.17 Accel_X_int16 = ACC_X_MSB * 256 + ACC_X_LSB
Accel_Y_int16 = ACC_Y_MSB * 256 + ACC_Y_LSB
Accel_Z_int16 = ACC_Z_MSB * 256 + ACC_Z_LSB

An example for the range setting of ±2 g is shown in the table below.

LSB	1111 1111		0000 0000		0000 0000
MSB	0111 1111		0000 0000		1000 0000
LSB + MSB [bin]	0111 1111 1111 1111		0000 0000 0000 0000		1000 0000 0000 0000
LSB + MSB [dec]	+32767	...	0	...	-32768
Acceleration value	+2 g	...	0 g	...	-2 g

When a register is read containing the LSB value of an acceleration value, the corresponding MSB register is locked internally, until it is read. By this mechanism, it is ensured that both LSB and MSB values belong to the same acceleration value and are not updated between the readouts of the individual registers. Therefore is recommended to always start reading out the LSB register first followed by the corresponding MSB register. Acceleration data may be read out from register LSB and/or MSB at any time except during power-up.

7.17.2 Gyroscope

For each axis the sensor output is stored as signed 16-bit number in 2's complement format in each 2 registers, split into a MSB upper part (bits <15:8> of rate data) and a LSB lower part (bits <7:0> of rate data). From the registers, the acceleration values can be calculated as follows:

Rate_X_int16: RATE_X_MSB * 256 + RATE_X_LSB
Rate_Y_int16: RATE_Y_MSB * 256 + RATE_Y_LSB
Rate_Z_int16: RATE_Z_MSB * 256 + RATE_Z_LSB

An example for the range setting of ±125 °/s is shown in the table below.

LSB	1111 1111		0000 0000		0000 0000
MSB	0111 1111		0000 0000		1000 0000
LSB + MSB [bin]	0111 1111 1111 1111		0000 0000 0000 0000		1000 0000 0000 0000
LSB + MSB [dec]	+32767	...	0	...	-32768
Angular rate value	+125 °/s	...	0 °/s	...	-125 °/s

When a register is read containing the LSB value of a rate value, the corresponding MSB register is locked internally, until it is read. By this mechanism, it is ensured that both LSB and MSB values belong to the same rate value and are not updated between the readouts of the individual registers. Therefore it is recommended to always start reading out the LSB register first followed by the corresponding MSB register. Rate data may be read from register LSB and/or MSB at any time except during power-up.

7.17.3 Temperature Sensor

The temperature sensor data is stored in an 11-bit value in 2's complement format in 2 registers, split into a MSB upper part (bits <10:3> of temperature data) and a LSB lower part (bits <2:0> of temperature data). The resolution is 0.125 °C / LSB, the temperature values can be calculated as follows:

```
Temp_uint11 = (TEMP_MSB * 8) + (TEMP_LSB / 32)
if Temp_uint11 > 1023:
        Temp_int11 = Temp_uint11 – 2048
else:
     Temp_int11 = Temp_uint11
Temperature = Temp_int11 * 0,125°C/LSB + 23°C
```

An example for the temperature values is shown in the table below.

LSB	111x xxxx		000x xxxx		000x xxxx	xxxx xxxx
MSB	0111 1111		0000 0000		1000 0001	1000 000
LSB + MSB [bin]	0111 1111 111		0000 0000 000		1000 0001 000	1000 0000 xxx
LSB + MSB [dec]	+1023	...	0	...	-1016	-1017...-1024
Temperature value	+150 °C	...	23 °C	...	-104 °C	Invalid

Note: If the MSB register of the temperature data is 0x80, regardless of the value of the LSB register, the temperature value is invalid.

The temperature sensor data is updated every 1.28 s.

7.18 Soft Reset

A soft reset causes all user configuration settings to be overwritten with their default value and the sensor to enter normal mode. A waiting time of 200 ms after a soft reset of the SMI230 accelerometer and gyroscope is recommended.

7.18.1 Accelerometer

A soft reset is initiated by writing the value 0xB6 to register ACC 0x7E (ACC_*SOFTRESET*).

7.18.2 Gyroscope

A soft reset is initiated by writing the value 0xB6 to register GYR 0x14 (*GYRO_SOFTRESET*).

Accelerometer Register Description

The entire communication with the device is performed by reading from and writing to registers. Registers have a width of 8 bits and are mapped to an 8-bit address space. Within this range some registers are either completely or partially marked as ‘reserved’. Any reserved bit is ignored when it is written and no specific value is guaranteed when the bit is read. It is recommended not to use registers which are completely marked as ‘reserved’. Furthermore, it is recommended to mask out (logical and with zero) reserved bits of registers which are partially marked as ‘reserved’.

7.19

Registers with addresses from ACC 0x00 up to ACC 0x23 are read-only. Any attempt to write to these registers will be ignored. There are bits within some registers which trigger internal sequences. These bits are configured for write-only access and read as 0. An example for such a write-only access is the entire register ACC 0x7E (ACC_*SOFTRESET*).

The following table shows the register map of the SMI230 accelerometer.

Reg. Addr.	Register Name	Reset Value	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
0x7E	ACC_SOFTRESET	0x00	softreset							
0x7D	ACC_PWR_CTRL	0x00	acc_enable							
0x7C	ACC_PWR_CONF	0x03	pwr_save_mode							
0x70	NV_CONF	0x00						i2c_wdt_en	I2c_wdt_sel	
0x6D	ACC_SELF_TEST	0x00	acc_self_test							
0x5E	ACC_FEATURE_CFG	0x00	acc_feature_cfg							
0x5C	BIN_pointer_MSB	0x00	bin_pointer_msb							
0x5B	BIN_pointer_LSB	0x00	bin_pointer_lsb							
0x59	INT_CTRL	0x00								Int_ctrl
0x58	INT1_INT2_MAP_DATA	0x00		Int2_drdy	Int2_fwm	Int2_ffull		Int1_drdy	Int1_fwm	Int1_ffull
0x57	INT2_MAP	0x00			no_mot_out	orient_out	low_g_out	high_g_out	any_mot_out	data_sync_out
0x56	INT1_MAP				no_mot_out	orient_out	low_g_out	high_g_out	any_mot_out	data_sync_out
0x55	INT_LATCH									int_latch
0x54	INT2_IO_CTRL	0x00				int2_in	int2_out	int2_od	int2_lvl	
0x53	INT1_IO_CTRL	0x00				int1_in	int1_out	int1_od	int1_lvl	
0x49	FIFO_CONFIG_1	0x10		acc_en		1	int1_en	int2_en		
0x48	FIFO_CONFIG_0	0x02							1	mode
0x47	FIFO_WTM_1	0x02			fifo_water_mark					
0x46	FIFO_WTM_0	0x00	fifo_water_mark							
0x45	FIFO_DOWNS	0x80	1	fifo_downs						

0x41	ACC_RANGE	0x01						acc_range	
0x40	ACC_CONF	0xA8	1	acc_bwp			acc_odr		
0x2A	INT_CFG_STATUS	0x00					message		
0x29	INT_ORIENT_RES					orient_fud	orient_pl1	orient_pl0	
0x28	INT_SYNC_Z_MSB		sync_z_msb						
0x27	INT_SYNC_Z_LSB		sync_z_lsb						
0x26	FIFO_DATA	0x00	fifo_data						
0x25	FIFO_LENGTH_1	0x00		fifo_byte_counter					
0x24	FIFO_LENGTH_0	0x00	fifo_byte_counter						
0x23	TEMP_LSB	0x00	temperature[2:0]						
0x22	TEMP_MSB	0x00	temperature[10:3]						
0x21	INT_SYNC_Y_MSB		sync_y_msb						
0x20	INT_SYNC_Y_LSB		sync_y_lsb						
0x1F	INT_SYNC_X_MSB		sync_x_msb						
0x1E	INT_SYNC_X_LSB		sync_x_lsb						
0x1D	ACC_INT_STAT_1	0x00	acc_drdy_int					fwm_int	ffull_int
0x1C	INT_STATUS_0	0x00		no_mot_out	orient_out	low_g_out	high_g_out	any_mot_out	data_sync_out
0x1A	SENSORTIME_2	0x00	sensor_time[23:16]						
0x19	SENSORTIME_1	0x00	sensor_time[15:8]						
0x18	SENSORTIME_0	0x00	sensor_time[7:0]						
0x17	ACC_Z_MSB	0x00	acc_z[15:8]						
0x16	ACC_Z_LSB	0x00	acc_z[7:0]						
0x15	ACC_Y_MSB	0x00	acc_y[15:8]						
0x14	ACC_Y_LSB	0x00	acc_y[7:0]						
0x13	ACC_X_MSB	0x00	acc_x[15:8]						
0x12	ACC_X_LSB	0x00	acc_x[7:0]						
0x03	ACC_STATUS	0x10	acc_drdy						
0x02	ACC_ERR_REG	0x00			error_code				fatal_err
0x00	ACC_CHIP_ID	0x1F	acc_chip_id						

	read / write
	write only
	read only
	reserved

All shown registers are common w/r registers:
Application specific settings which are not equal to the default settings, must be re-set to its designated values after POR, soft-reset and wake up from deep suspend.

7.19.1 ACC Register 0x00 (*ACC_CHIP_ID*)

This register contains the chip identification code.

0x00	ACC_CHIP ID							
Bit	7	6	5	4	3	2	1	0
Read/Write	R	R	R	R	R	R	R	R
Reset Value	n/a	n/a	n/a	n/a	n/a	n/a	n/a	n/a
Content	*chip_id* <7:0>							

Register	Description
chip_id <7:0>	Fixed value 10001111 = 1F

7.19.2 ACC Register 0x02 (*ACC_ERR_REG*)

This register contains the error conditions of SMI230.

0x02	ACC_ERR_REG							
Bit	7	6	5	4	3	2	1	0
Read/Write	R	R	R	R	R	R	R	R
Reset Value	n/a	n/a	n/a	0	0	0	n/a	0
Content				*error_code*				*fatal_err*

Register	Description
error_code <4:2>	Error codes for persistent errors: 000: no error 001: error occurred in accelerometer configuration (invalid data in register ACC_CONF)
fatal_err <0>	0: no error 1: fatal error, chip is not in operation state. Reset by POR or soft reset.
undefined	Random data, to be ignored

7.19.3 ACC Register 0x03 (*ACC_STATUS*)

This register contains the data ready flag of acceleration registers.

0x03	ACC_STATUS							
Bit	7	6	5	4	3	2	1	0
Read/Write	R	R	R	R	R	R	R	R
Reset Value	0	n/a	n/a	n/a	n/a	n/a	n/a	n/a
Content	acc_drdy							

Register	Description
acc_drdy <7>	0: acceleration data is being updated 1: data ready for accelerometer. Reset when one acceleration data register is read out
undefined	Random data, to be ignored

7.19.4 ACC Register 0x12 (*ACC_X_LSB*)

This register contains the least significant bits of the x-channel acceleration readout.

0x12	ACC_X_LSB							
Bit	7	6	5	4	3	2	1	0
Read/Write	R	R	R	R	R	R	R	R
Reset Value	n/a	n/a	n/a	n/a	n/a	n/a	n/a	n/a
Content	*acc_x_lsb* <7:0>							

Register	Description
acc_x_lsb <7:0>	Least significant 8 bits of acceleration x-channel read-back value (two's complement format)

7.19.5 ACC Register 0x13 (*ACC_X_MSB*)

This register contains the most significant bits of x-channel acceleration readout value.

0x13	*ACC_X_MSB*							
Bit	7	6	5	4	3	2	1	0
Read/Write	R	R	R	R	R	R	R	R
Reset Value	n/a	n/a	n/a	n/a	n/a	n/a	n/a	n/a
Content	*acc_x_msb* <15:8>							

Register	Description
acc_x_msb <15:8>	Most significant 8 bits of acceleration x-channel read-back value (two's complement format)

7.19.6 ACC Register 0x14 (*ACC_Y_LSB*)

This register contains the least significant bits of y-channel acceleration readout value.

0x14	*ACC_Y_LSB*							
Bit	7	6	5	4	3	2	1	0
Read/Write	R	R	R	R	R	R	R	R
Reset Value	n/a	n/a	n/a	n/a	n/a	n/a	n/a	n/a
Content	*acc_y_lsb* <7:0>							

Register	Description
acc_y_lsb <7:0>	Least significant 8 bits of acceleration y-channel read-back value (two's complement format)

7.19.7 ACC Register 0x15 (*ACC_Y_MSB*)

This register contains the most significant bits of y-channel acceleration readout value.

0x15	*ACC_Y_MSB*							
Bit	7	6	5	4	3	2	1	0
Read/Write	R	R	R	R	R	R	R	R
Reset Value	n/a	n/a	n/a	n/a	n/a	n/a	n/a	n/a
Content	*acc_y_msb* <15:8>							

Register	Description
acc_y_msb <15:8>	Most significant 8 bits of acceleration y-channel read-back value (two's complement format)

7.19.8 ACC Register 0x16 (*ACC_Z_LSB*)

This register contains the least significant bits of z-channel acceleration readout value.

0x16	ACC_Z_LSB							
Bit	7	6	5	4	3	2	1	0
Read/Write	R	R	R	R	R	R	R	R
Reset Value	n/a	n/a	n/a	n/a	n/a	n/a	n/a	n/a
Content	*acc_z_lsb* <7:0>							

Register	Description
acc_z_lsb <7:0>	Least significant 8 bits of acceleration z-channel read-back value (two's complement format)

7.19.9 ACC Register 0x17 (*ACC_Z_MSB*)

This register contains the most significant bits of z-channel acceleration readout value.

0x17	ACC_Z_MSB							
Bit	7	6	5	4	3	2	1	0
Read/Write	R	R	R	R	R	R	R	R
Reset Value	n/a	n/a	n/a	n/a	n/a	n/a	n/a	n/a
Content	*acc_z_msb* <15:8>							

Register	Description
acc_z_msb <15:8>	Most significant 8 bits of acceleration z-channel read-back value (two's complement format)

7.19.10 ACC Register 0x18 (*SENSORTIME_0*)

This register contains the lower 8 bits value of the internal 24-bit counter. This register is incremented every 39.0625 µs.

0x18	SENSORTIME_0							
Bit	7	6	5	4	3	2	1	0
Read/Write	R	R	R	R	R	R	R	R
Reset Value	n/a	n/a	n/a	n/a	n/a	n/a	n/a	n/a
Content	*sensortime_0* <7:0>							

Register	Description
sensortime_0 <7:0>	Lower 8 bits of internal counter

7.19.11 ACC Register 0x19 (*SENSORTIME_1*)

This register contains the middle 8 bits value of the internal 24-bit counter. This register is incremented on SENSORTIME_0 overflow, which is every 10 ms.

0x19	SENSORTIME_1							
Bit	7	6	5	4	3	2	1	0
Read/Write	R	R	R	R	R	R	R	R
Reset Value	n/a	n/a	n/a	n/a	n/a	n/a	n/a	n/a
Content	*sensortime_1* <15:8>							

Register	Description
sensortime_1 <15:8>	Middle 8 bits of internal counter

7.19.12 ACC Register 0x1A (*SENSORTIME_2*)

This register contains the higher 8 bits value of the internal 24-bit counter. This register is incremented on SENSORTIME_1 overflow, which is every 2.56 s.

0x1A	*SENSORTIME_2*							
Bit	7	6	5	4	3	2	1	0
Read/Write	R	R	R	R	R	R	R	R
Reset Value	n/a	n/a	n/a	n/a	n/a	n/a	n/a	n/a
Content	*sensortime_2* <23:16>							

Register	Description
sensortime_2 <23:16>	Higher 8 bits of internal counter

7.19.13 ACC Register 0x1C (INT_STATUS_0)

This register stores the interrupt statuses (cleared on read).

0x1C	INT_STATUS_0							
Bit	7	6	5	4	3	2	1	0
Read/Write	R	R	R	R	R	R	R	R
Reset Value	0	0	0	0	0	0	0	0
Content	reserved		*no_mot_out*	*orient_out*	*low_g_out*	*high_g_out*	*any_mot_out*	*data_sync_out*

Bit	Description
data_sync_out	set to 1 when DataSync interrupt is generated by the device
any_mot_out	set to 1 when any-motion interrupt is generated by the device
high_g_out	set to 1 when high-g interrupt is generated by the device
low_g_out	set to 1 when low-g interrupt is generated by the device
orient_out	set to 1 when a change of orientation is detected by the device. Change of orientation means: - Output bit 2 is modified in reg. 0x29, i.e. face-up to face-down or vice versa - Output bits 0/1 are modified in reg. 0x29, i.e. change in portrait/landscape orientation
no_mot_out	set to 1 when no-motion interrupt is generated by the device

7.19.14 ACC Register 0x1D (*ACC_INT_STAT_1*)

This register contains the new data and FIFO interrupt status.

0x1D	*ACC_INT_STAT_1*							
Bit	7	6	5	4	3	2	1	0
Read/Write	R	R	R	R	R	R	R	R
Reset Value	0	n/a	n/a	n/a	n/a	n/a	n/a	n/a
Content	acc_drdy_int						*fwm_int*	*ffull_int*

Register	Description
acc_drdy_int <7>	0: Acceleration new data interrupt inactive. 1: Acceleration new data interrupt active. Cleared on read of this register.
fwm_int <1>	0: FIFO watermark interrupt condition is inactive. 1: FIFO watermark interrupt condition is active.
ffull_int <0>	0: FIFO full interrupt condition is inactive. 1: FIFO full interrupt condition is active.
Undefined	Random data, to be ignored

7.19.15 ACC Register 0x1E (INT_SYNC_X_LSB)

This register stores the synchronized x-data (lower 8 bits).

0x1E	INT_SYNC_X_LSB							
Bit	7	6	5	4	3	2	1	0
Read/Write	R	R	R	R	R	R	R	R
Reset Value	0	0	0	0	0	0	0	0
Content	*sync_x_lsb<7:0>*							

7.19.16 ACC Register 0x1F (INT_SYNC_X_MSB)

This register stores the synchronized x-data (upper 8 bits).

0x1F	INT_SYNC_X_MSB							
Bit	7	6	5	4	3	2	1	0
Read/Write	R	R	R	R	R	R	R	R
Reset Value	0	0	0	0	0	0	0	0
Content	*sync_x_msb<7:0>*							

7.19.17 ACC Register 0x20 (INT_SYNC_Y_LSB)

This register stores the synchronized y-data (lower 8 bits).

0x20	INT_SYNC_Y_LSB							
Bit	7	6	5	4	3	2	1	0
Read/Write	R	R	R	R	R	R	R	R
Reset Value	0	0	0	0	0	0	0	0
Content	*sync_y_lsb<7:0>*							

7.19.18 ACC Register 0x21 (INT_SYNC_Y_MSB)

This register stores the synchronized y-data (upper 8 bits).

0x21	INT_SYNC_Y_MSB							
Bit	7	6	5	4	3	2	1	0
Read/Write	R	R	R	R	R	R	R	R
Reset Value	0	0	0	0	0	0	0	0
Content	*sync_y_msb<7:0>*							

7.19.19 ACC Register 0x22 (*TEMP_MSB*)

This register contains the most significant 8 bits of the 11-bit internal temperature sensor.

0x22	*TEMP_MSB*							
Bit	7	6	5	4	3	2	1	0
Read/Write	R	R	R	R	R	R	R	R
Reset Value	n/a	n/a	n/a	n/a	n/a	n/a	n/a	n/a
Content	*temp_msb* <10:3>							

Register	Description
temp_msb <10:3>	Most significant 8 bits of temperature channel (two's complement format)

7.19.20 ACC Register 0x23 (*TEMP_LSB*)

This register contains the most significant 8 bits of the 11-bit internal temperature sensor.

0x23	TEMP_LSB							
Bit	7	6	5	4	3	2	1	0
Read/Write	R	R	R	R	R	R	R	R
Reset Value	n/a	n/a	n/a	n/a	n/a	n/a	n/a	n/a
Content	*temp_lsb* <2:0>							

Register	Description
temp_lsb <2:0>	Least significant 3 bits of temperature channel (two's complement format
undefined	Random data, to be ignored

7.19.21 ACC Register 0x24 (*FIFO_LENGTH_0*)

This register contains FIFO byte counter together with 0x25

0x24	FIFO_LENGTH_0							
Bit	7	6	5	4	3	2	1	0
Read/Write	R	R	R	R	R	R	R	R
Reset Value	0	0	0	0	0	0	0	0
Content	*fifo_byte_counter* <7:0>							

Please see ACC Register 0x25 for the detailed description.

7.19.22 ACC Register 0x25 (*FIFO_LENGTH_1*)

This register contains FIFO byte counter together with 0x24

0x25	FIFO_LENGTH_1							
Bit	7	6	5	4	3	2	1	0
Read/Write	R	R	R	R	R	R	R	R
Reset Value	n/a	n/a	0	0	0	0	0	0
Content			*fifo_byte_counter* <13:8>					

The FIFO length registers FIFO_LENGTH_1 and FIFO_LENGTH_0 contain the 14 bit FIFO byte counter. The counter represents the current fill level of the FIFO buffer.

An empty FIFO corresponds to 0x8000. A FIFO content reset can be triggered by reading out all frames from the FIFO buffer or by writing 0xB0 into register 0x7E. The byte counter is updated when a complete frame is read or written.

7.19.23 ACC Register 0x26 (*FIFO_DATA*)

This register contains FIFO data.

0x26	FIFO_DATA							
Bit	7	6	5	4	3	2	1	0
Read/Write	R	R	R	R	R	R	R	R
Reset Value	0	0	0	0	0	0	0	0
Content	*fifo_data*							

7.19.24 ACC Register 0x27 (INT_SYNC_Z_LSB)

This register stores the synchronized z-data (lower 8 bits).

0x27	INT_SYNC_Z_LSB							
Bit	7	6	5	4	3	2	1	0
Read/Write	R	R	R	R	R	R	R	R
Reset Value	0	0	0	0	0	0	0	0
Content	*sync_z_lsb*<7:0>							

7.19.25 ACC Register 0x28 (INT_SYNC_Z_MSB)

This register stores the synchronized z-data (upper 8 bits).

0x28	INT_SYNC_Z_MSB							
Bit	7	6	5	4	3	2	1	0
Read/Write	R	R	R	R	R	R	R	R
Reset Value	0	0	0	0	0	0	0	0
Content	*sync_z_msb<7:0>*							

7.19.26 ACC Register 0x29 (INT_ORIENT_RES)

This register stores the orientation output of the orientation detection feature.

0x29	INT_ORIENT_RES							
Bit	7	6	5	4	3	2	1	0
Read/Write	R	R	R	R	R	R/W	R/W	R/W
Reset Value	0	0	0	0	0	0	0	0
Content	reserved					*orient_fud*	*orient_pl<1:0>*	

Bit	Description
orient_fud	Reflects the orientation face-up (0) / face-down (1), only if *ud_en* is enabled in reg. 0x009. If host disables this feature with *ud_en=0*, then the output bit is not valid until *ud_en* is set to 1 again.
orient_pl	Orientation portrait/landscape: 00 portrait upright 01 landscape left 10 portrait upside down 11 landscape right

7.19.27 ACC Register 0x2A (INT_CFG_STATUS)

This register reports internal status messages about the ASIC initialization by the config file.

0x2A	INT_CGF_STATUS							
Bit	7	6	5	4	3	2	1	0
Read/Write	R	R	R	R	R	R	R	R
Reset Value	0	0	0	0	0	0	0	0
Content	reserved					*message<2:0>*		

Bit	Value	Name	Description
message	0x0	not_init	ASIC is not initialized
	0x1	init_ok	ASIC initialized
	0x2	init_err	Initialization error
	0x3	dvr_err	Invalid driver
	0x4	sns_stop	Sensor stopped

7.19.28 ACC Register 0x40 (*ACC_CONF*)

This register contains the accelerometer BW and ODR configuration.

0x40	*ACC_CONF*							
Bit	7	6	5	4	3	2	1	0
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset Value	1	0	1	0	1	0	0	0
Content	*reserved*	*acc_bwp*			*acc_odr*			

Register	Description
reserved <7>	This bit must always be '1'.
acc_bwp <6:4>	This parameter influences the bandwidth of the accelerometer low pass filter.

acc_bwp	filter setting
000	OSR4 (4-fold oversampling)
001	OSR2 (2-fold oversampling)
010	Normal
011…111	*reserved*

acc_odr <3:0>	This parameter sets the output data rate ODR.

acc_odr	ODR in Hz
0000…0100	*reserved*
0101	12.5
0110	25
0111	50
1000	100
1001	200
1010	400
1011	800
1100	1600
1101…1111	*reserved*

7.19.29 ACC Register 0x41 (*ACC_RANGE*)

This register allows for the selection of the accelerometer g-range.

0x41	*ACC_RANGE*							
Bit	7	6	5	4	3	2	1	0
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset Value	n/a	n/a	n/a	n/a	n/a	n/a	0	1
Content	*reserved*						*acc_range* <1:0>	

Register	Description
acc_range <1:0>	Selection of the accelerometer g-range

range <1:0>	g-range	Resolution [LSB / g]
00	±2 g	16384
01	±4 g	8192
10	±8 g	4096
11	±16 g	2048

reserved	write 0

7.19.30 ACC Register 0x45 (*FIFO_DOWNS*)

This register contains the information regarding the FIFO sampling rate reduction factor.

0x45	FIFO_DOWNS							
Bit	7	6	5	4	3	2	1	0
Read/Write	R/W	R	R	R	R	R	R	R
Reset Value	1	0	0	0	n/a	n/a	n/a	n/a
Content	*1*	*fifo_downs*			*reserved*			

Register	Description
reserved <7>	This bit must always be '1'
fifo_downs	Reduction of sample rate by a factor 2**fifo_downs. Example: fifo_downs=5 will reduce the FIFO sampling rate by a factor of 2**5=32 in relation to the chosen ODR of the sensor signal.

7.19.31 ACC Register 0x46 (*FIFO_WTM_0*)

This register contains FIFO water mark level value together with 0x47.

0x46	FIFO_WTM_0							
Bit	7	6	5	4	3	2	1	0
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset Value	0	0	0	0	0	0	0	0
Content	*fifo_wtm_0*							

Please see ACC Register 0x47 for the detailed description.

7.19.32 ACC Register 0x47 (*FIFO_WTM_1*)

This register contains FIFO water mark level value together with 0x46.

0x47	FIFO_WTM_1							
Bit	7	6	5	4	3	2	1	0
Read/Write	R	R	R	R/W	R/W	R/W	R/W	R/W
Reset Value	n/a	n/a	n/a	0	0	0	0	0
Content	*reserved*			*fifo_wtm_1*				

0x46 and 0x47 registers contain the 13 bit FIFO watermark level value. A FIFO water mark interrupt signal is active if the FIFO fill level is equal or greater than fifo_water_mark[12:0] (unit of the fifo water mark is one byte).

7.19.33 ACC Register 0x48 (*FIFO_CONFIG_0*)

This register sets the FIFO mode.

0x48	FIFO_CONFIG_0							
Bit	7	6	5	4	3	2	1	0
Read/Write	R	R	R	R	R	R	R/W	R/W
Reset Value	n/a	n/a	n/a	n/a	n/a	n/a	1	0
Content	*reserved*						*1*	*mode*

Register	Description
reserved <1>	This bit must always be 1
mode	This parameter sets the FIFO mode 0: STREAM mode 1: FIFO mode

7.19.34 ACC Register 0x49 (*FIFO_CONFIG_1*)

This register contains FIFO configuration

0x49	*FIFO_CONFIG_1*							
Bit	7	6	5	4	3	2	1	0
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset Value	n/a	0	0	1	0	0	0	0
Content	*reserved*	*acc_en*	*reserved*		*int1_en*	*int2_en*	*reserved*	

Register	Description
acc_en	enables storing of accelerometer sensor data
reserved <4>	this bit must always be '1'
Int1_en	enable storing of captured interrupt events at pin INT1 (pin needs to be configured as input pin accordingly)
Int2_en	enable storing of captured interrupt events at pin INT2 (pin needs to be configured as input pin accordingly)

7.19.35 ACC Register 0x53 (*INT1_IO_CONF*)

This register allows for the configuration of the input/output pin INT1.

0x53	*INT1_IO_CONF*							
Bit	7	6	5	4	3	2	1	0
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset Value	0	0	0	0	0	0	0	0
Content	*reserved*			*int1_in*	*int1_out*	*int1_od*	*int1_lvl*	*reserved*

Register	Description
reserved <7:5>	write 0
int1_in	enable INT1 as input pin 0: disable 1: enable
int1_out	enable INT1 as output pin 0: disable 1: enable
int1_od	configures pin behavior of INT1 pin 0: push-pull 1: open-drain
int1_lvl	configures active state of INT1 pin 0: active low 1: active high
reserved <0>	write 0

7.19.36 ACC Register 0x54 (*INT2_IO_CONF*)

This register allows for the configuration of the input/output pin INT2.

0x54	*INT2_IO_CONF*							
Bit	7	6	5	4	3	2	1	0
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset Value	0	0	0	0	0	0	0	0
Content	*reserved*			*int2_in*	*int2_out*	*int2_od*	*int2_lvl*	*reserved*

Register	Description
reserved <7:5>	write 0
int2_in	enable INT2 as input pin 0: disable 1: enable
int2_out	enable INT2 as output pin 0: disable 1: enable
int2_od	configures pin behavior of INT2 pin 0: push-pull 1: open-drain
int2_lvl	configures active state of INT2 pin 0: active low 1: active high
reserved <0>	write 0

7.19.37 ACC Register 0x55 (INT_LATCH)

Configuration of interrupt mode

0x55	INT_LATCH							
Bit	7	6	5	4	3	2	1	0
Read/Write	R	R	R	R	R	R	R	R/W
Reset Value	0	0	0	0	0	0	0	0
Content	reserved							*int_latch*

Bit	Description
int_latch	0 Non latched 1 Latched

7.19.38 ACC Register 0x56 (INT1_MAP)

Interrupt/Feature mapping on INT 1.

0x56	INT1_MAP							
Bit	7	6	5	4	3	2	1	0
Read/Write	R	R	R/W	R/W	R/W	R/W	R/W	R/W
Reset Value	0	0	0	0	0	0	0	0
Content	reserved		*no_mot_out*	*orient_out*	*low_g_out*	*high_g_out*	*any_mot_out*	*data_sync_out*

Register	Description
no_mot_out	map no motion interrupt to INT1 pin 0: disable 1: enable
orien_out	map orientation interrupt to INT1 pin 0: disable 1: enable
low_g_out	map low g interrupt to INT1 pin 0: disable 1: enable
high_g_out	map high g interrupt to INT1 pin 0: disable 1: enable
any_mot_out	map any motion interrupt to INT1 pin 0: disable 1: enable
data_sync_out	map data sync to INT1 pin 0: disable 1: enable

7.19.39 ACC Register 0x57 (INT2_MAP)

Interrupt/Feature mapping on INT 2.

0x57	INT2_MAP							
Bit	7	6	5	4	3	2	1	0
Read/Write	R	R	R/W	R/W	R/W	R/W	R/W	R/W
Reset Value	0	0	0	0	0	0	0	0
Content	reserved		*no_mot_out*	*orient_out*	*low_g_out*	*high_g_out*	*any_mot_out*	*data_sync_out*

Register	Description
no_mot_out	map no motion interrupt to INT2 pin 0: disable 1: enable
orien_out	map orientation interrupt to INT2 pin 0: disable 1: enable
low_g_out	map low g interrupt to INT2 pin 0: disable 1: enable
high_g_out	map high g interrupt to INT2 pin 0: disable 1: enable
any_mot_out	map any motion interrupt to INT2 pin 0: disable 1: enable
data_sync_out	map data sync to INT2 pin 0: disable 1: enable

7.19.40 ACC Register 0x58 (*INT1_INT2_MAP_DATA*)

This register controls the various interrupt signals to be mapped to output pin INT1 and/or INT2.

0x58	*INT1_INT2_MAP_DATA*							
Bit	7	6	5	4	3	2	1	0
Read/Write	R	R/W	R/W	R/W	R	R/W	R/W	R/W
Reset Value	n/a	0	0	0	n/a	0	0	0
Content	*reserved*	*int2_drdy*	*Int2_fwm*	*Int2_fful*	*reserved*	*Int1_drdy*	*Int1_fwm*	*Int1_fful*

Register	Description
Int2_drdy	map new data interrupt to INT2 pin 0: disable 1: enable
Int2_fwm	map FIFO watermark interrupt to INT2 pin 0: disable 1: enable
Int2_fful	map FIFO full interrupt to INT2 pin 0: disable 1: enable
int1_drdy	map new data interrupt to INT1 pin 0: disable 1: enable
Int1_fwm	map FIFO watermark interrupt to INT1 pin 0: disable 1: enable
Int1_fful	map FIFO full interrupt to INT1 pin 0: disable 1: enable

7.19.41 ACC Register 0x59 (INT_CTRL)

This register is used to enable the initialization of the configuration file

0x59	*INT_CTRL*							
Bit	7	6	5	4	3	2	1	0
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset Value	0	0	0	0	0	0	0	0
Content	*reserved*							*Int_ctrl*

Register	Description
reserved <7:1>	write 0
Int_ctrl <0>	Enable the initialization of the configuration file 0: enable the mode for accepting the configuration file 1: enable the sensor feature after loading the configuration fie Please note that the commands should not be used more than once after POR or soft reset, and the initialization process, described in section 7.4.3 should be strictly followed.

7.19.42 ACC Register 0x5B (BIN_pointer_LSB)

This register is related to the interrupt feature configuration.

0x5B	*BIN_pointer_LSB*							
Bit	7	6	5	4	3	2	1	0
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset Value	0	0	0	0	0	0	0	0
Content	*Bin_pointer_LSB*							

7.19.43 ACC Register 0x5C (BIN_pointer_MSB)

This register is related to the interrupt feature configuration.

0x5C	BIN_pointer_MSB							
Bit	7	6	5	4	3	2	1	0
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset Value	0	0	0	0	0	0	0	0
Content	Bin_pointer_MSB							

7.19.44 ACC Register 0x5E (ACC_FEATURES_CFG)

This register is the interrupt feature configuration read/write port

0x5E	ACC_FEATURES_CFG							
Bit	7	6	5	4	3	2	1	0
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset Value	0	0	0	0	0	0	0	0
Content	acc_features_cfg<7:0>							

7.19.45 ACC Register 0x6D (*ACC_SELF_TEST*)

This register enables the sensor self-test signal, occurring as a steady offset to the sensor output. Note that the self-test needs to be switched off actively by the user.

0x6D	ACC_SELF_TEST							
Bit	7	6	5	4	3	2	1	0
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset Value	0	0	0	0	0	0	0	0
Content	acc_self_test							

Register	Description
acc_self_test <7:0>	enable or disable self-test 0x00: self-test is switched off 0x0D: enable positive self-test signal 0x09: enable negative self-test signal

7.19.46 ACC Register 0x70 (*NV_CONF*)

This register contains settings for the digital interfaces.

0x70	NV_CONF							
Bit	7	6	5	4	3	2	1	0
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset Value	0	0	0	0	0	0	0	0
Content	reserved					i2c_wdt_en	i2c_wdt_sel	reserved

Register	Description
i2c_wdt_en	Watchdog timer at the SDA pin in TWI mode 0: disable 1: enable
i2c_wdt_sel	Watchdog timer period 0: 1.25 ms 1: 40 ms
reserved	Write 0

7.19.47 ACC Register 0x7C (*ACC_PWR_CONF*)

This register enables the accelerometer to be switched into suspend mode for saving power. In this mode the data acquisition is stopped.

0x7c	ACC_PWR_CONF							
Bit	7	6	5	4	3	2	1	0
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset Value	0	0	0	0	0	0	1	1
Content	*acc_pwr_save*							

Register	Description
acc_pwr_save <7:0>	switches the accelerometer into suspend or normal mode 0x03: suspend mode 0x00: normal mode

7.19.48 ACC Register 0x7D (*ACC_PWR_CTRL*)

This register enables the accelerometer to be switched on or off (suspend mode). Required to do after every reset in order to obtain acceleration values.

0x7D	ACC_PWR_CTRL							
Bit	7	6	5	4	3	2	1	0
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset Value	0	0	0	0	0	0	0	0
Content	*acc_pwr_ctrl*							

Register	Description
acc_pwr_ctrl <7:0>	switches the accelerometer on or off 0x00: accelerometer off (suspend mode) 0x04: accelerometer on

7.19.49 ACC Register 0x7E (*ACC_SOFTRESET*)

This register controls the user triggered reset of the sensor.

0x7E	ACC_SOFTRESET							
Bit	7	6	5	4	3	2	1	0
Read/Write	W	W	W	W	W	W	W	W
Reset Value	0	0	0	0	0	0	0	0
Content	*softreset*							

Register	Description
softreset	Writing 0xB6 to the register triggers a reset. Writing 0xB0 to the register clears all data in the FIFO. Other values are ignored. After a delay, all user configuration settings are overwritten with their default values. Please note that all application specific settings which are not equal to the default settings must be reconfigured to their designated values.

Interrupt Engine Register Description

The entire communication with the device is performed by reading from and writing to registers. Registers have a width of 16 bits and are mapped to 12-bit address space. Within this range some registers are either completely or partially marked as ‘reserved’. Any reserved bit is ignored when it is written and no specific value is guaranteed when the bit is read. It is recommended not to use registers which are completely marked as ‘reserved’. Furthermore, it is recommended to mask out (logical and with zero) reserved bits of registers which are partially marked as ‘reserved’.

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The following table shows the register map of the interrupt engine.

Reg. Addr.	Register Name	Reset Value	bit 15	bit 14	bit 13	bit 12	bit 11	bit 10	bit 9	bit 8	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
0x00C	INT_NO_MOT_EN	0xE005	en_z	en_y	en_x	no_mot_dur												
0x00B	INT_NO_MOT_TH	0x00AA					no_mot_en	no_mot_th										
0x00A	INT_ORIENT_HYST	0x0080						orient_hyst										
0x009	INT_ORIENT_EN	0x0A30					orient_theta						orient_blocking		orient_mode		ud_en	enable
0x008	INT_LOW_DUR	0x0000					low_dur											
0x007	INT_LOW_EN	0x0100				low_en	low_hyst											
0x006	INT_LOW_TH	0x0200		low_th														
0x005	INT_HIGH_DUR	0x0004					high_dur											
0x004	INT_HIGH_EN	0x73E8	enable	en_z	en_y	en_x	high_hyst											
0x003	INT_HIGH_TH	0x0C00		high_th														
0x002	INT_DATA SYNC	0x0000															sync	
0x001	INT_ANYMOT_EN	0xE005	en_z	en_y	en_x	anymot_dur												
0x000	INT_ANYMOT_TH	0x00AA					anymot_mot_en	anymot_th										

	read / write
	write only
	read only
	reserved

7.20.1 INT Register 0x000 (INT_ANYMOT_TH)

RESET: 0x00AA

This register sets the threshold for any-motion / slope detection.

0x000	INT_ANYMOT_TH							
Bit	15	14	13	12	11	10	9	8
Read/Write	R	R	R	R	R/W	R/W	R/W	R/W
Reset Value	0	0	0	0	0	0	0	0
Content	reserved				*anymot_en*	*anymot_th <10:8>*		

0x000	INT_ANYMOT_TH							
Bit	7	6	5	4	3	2	1	0
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset Value	1	0	1	0	1	0	1	0
Content	*anymot_th <7:0>*							

Bit	Description
anymot_en	Enables the feature
anymot_th	Defines the any-motion/slope threshold

7.20.2 INT Register 0x001 (INT_ANYMOT_EN)

RESET: 0xE005

This register enables the any-motion / slope detection feature and set the duration.

0x001	INT_ANYMOT_EN							
Bit	15	14	13	12	11	10	9	8
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset Value	1	1	1	0	0	0	0	0
Content	*en_z*	*en_y*	*en_x*	*anymot_dur <12:8>*				

0x001	INT_ANYMOT_EN							
Bit	7	6	5	4	3	2	1	0
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset Value	0	0	0	0	0	1	0	1
Content	*anymot_dur <7:0>*							

Bit	Description
en_x	Enables the feature on a per-axis basis: x axis
en_y	Enables the feature on a per-axis basis: y axis
en_z	Enables the feature on a per-axis basis: z axis
anymot_dur	Defines the number of consecutive data points for which the threshold condition must be respected for interrupt assertion. It is expressed in 50 Hz samples (20 ms). Range is 0 to 163 s. Default value is 0x5 ≙ 100 ms.

7.20.3 INT Register 0x002 (INT_DATASYNC)

RESET: 0x0000

This register enables data synchronization between ACC and GYRO data.

0x002	INT_DATASYNC							
Bit	15	14	13	12	11	10	9	8
Read/Write	R	R	R	R	R	R	R	R
Reset Value	0	0	0	0	0	0	0	0
Content	reserved							

0x002	INT_DATASYNC							
Bit	7	6	5	4	3	2	1	0
Read/Write	R	R	R	R	R	R	R/W	R/W
Reset Value	0	0	0	0	0	0	0	0
Content	reserved						*sync <1:0>*	

Bit	Description
sync	00 DataSync deactivated 01 DataSync activated for 400 Hz sampling rate 10 DataSYnc activated for 1 kHz sampling rate 11 DataSYnc activated for 2 kHz sampling rate

7.20.4 INT Register 0x003 (INT_HIGH_TH)

RESET: 0x0C00

This register sets the high-g interrupt threshold.

0x003	INT_HIGH_TH							
Bit	15	14	13	12	11	10	9	8
Read/Write	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset Value	0	0	0	0	1	1	0	0
Content	reserved	*high_th <14:8>*						

0x003	INT_HIGH_TH							
Bit	7	6	5	4	3	2	1	0
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset Value	0	0	0	0	0	0	0	0
Content	*high_th* <7:0>							

Bit	Description
high_th	The acceleration threshold above which the high-g interrupt is triggered

7.20.5 INT Register 0x004 (INT_HIGH_EN)

RESET: 0x73E8

This register enables the high-g interrupt and hysteresis.

0x004	INT_HIGH_TH							
Bit	15	14	13	12	11	10	9	8
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset Value	0	1	1	1	0	0	1	1
Content	*enable*	*en_z*	*en_y*	*en_x*	*high_hyst <11:8>*			

0x004	INT_HIGH_TH							
Bit	7	6	5	4	3	2	1	0
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset Value	1	1	1	0	1	0	0	0
Content	*high_hyst <7:0>*							

Bit	Description
enable	Enable high-g interrupt feature
en_z	Enables the feature on a per-axis basis: z axis
en_y	Enables the feature on a per-axis basis: y axis
en_x	Enables the feature on a per-axis basis: x axis
high_hyst	Hysteresis value for high-g feature

7.20.6 INT Register 0x005 (INT_HIGH_DUR)

RESET: 0x0004

This register sets the high-g interrupt duration.

0x005	INT_HIGH_DUR							
Bit	15	14	13	12	11	10	9	8
Read/Write	R	R	R	R	R/W	R/W	R/W	R/W
Reset Value	0	0	0	0	0	0	0	0
Content	reserved				*high_dur <11:8>*			

0x005	INT_HIGH_DUR							
Bit	7	6	5	4	3	2	1	0
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset Value	0	0	0	0	0	1	0	0
Content	*high_dur <7:0>*							

Bit	Description
high_dur	Defines the number of consecutive data points for which the threshold condition must be respected for interrupt assertion. It is expressed in 200 Hz samples (5 ms). Range is 0 to 20 s. Default value is 0x4 ≙ 20 ms.

7.20.7 INT Register 0x006 (INT_LOW_TH)

RESET: 0x0200

This register sets the threshold for the low-g interrupt.

0x006	INT_LOW_TH							
Bit	15	14	13	12	11	10	9	8
Read/Write	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset Value	0	0	0	0	0	0	1	0
Content	reserved	*low_th <14:8>*						

0x006	INT_LOW_TH							
Bit	7	6	5	4	3	2	1	0
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset Value	0	0	0	0	0	0	0	0
Content	*low_th <7:0>*							

Bit	Description
low_th	The acceleration threshold below which the low-g interrupt is triggered

7.20.8 INT Register 0x007 (INT_LOW_EN)

RESET: 0x0100

This register enables the low-g interrupt and the hysteresis.

0x007	INT_LOW_EN							
Bit	15	14	13	12	11	10	9	8
Read/Write	R	R	R	R/W	R/W	R/W	R/W	R/W
Reset Value	0	0	0	0	0	0	0	1
Content	reserved			*low_en*	*low_hyst <11:8>*			

0x007	INT_LOW_EN							
Bit	7	6	5	4	3	2	1	0
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset Value	0	0	0	0	0	0	0	0
Content	*low_hyst <7:0>*							

Bit	Description
low_en	Enables the feature
low_hy <11:0>	Hysteresis value for low_g feature. Recommended range is 0 to 0.5 g. Default value is 256.

7.20.9 INT Register 0x008 (INT_LOW_DUR)

RESET: 0x0000

This register sets the low-g interrupt duration.

0x008	INT_LOW_DUR							
Bit	15	14	13	12	11	10	9	8
Read/Write	R	R	R	R	R/W	R/W	R/W	R/W
Reset Value	0	0	0	0	0	0	0	1
Content	reserved				*low_dur <11:8>*			

0x008	INT_LOW_DUR							
Bit	7	6	5	4	3	2	1	0
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset Value	0	0	0	0	0	0	0	0
Content	*low_dur <7:0>*							

Bit	Description
low_dur	Defines the number of consecutive data points for which the threshold condition must be respected for interrupt assertion. It is expressed in 50 Hz samples (20 ms). Range is 0 to 82 s. Default value is 0x0 ≙ 0 ms.

7.20.10 INT Register 0x009 (INT_ORIENT_EN)

RESET: 0x0A30

This register enables the orientation interrupt and sets mode, blocking mode and threshold angle.

0x009	INT_ORIENT_EN							
Bit	15	14	13	12	11	10	9	8
Read/Write	R	R	R	R	R/W	R/W	R/W	R/W
Reset Value	0	0	0	0	1	0	1	0
Content	reserved				*orient_theta <11:8>*			

0x009	INT_ORIENT_EN							
Bit	7	6	5	4	3	2	1	0
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset Value	0	0	1	1	0	0	0	0
Content	*orient_theta <7:6>*		*orient_blocking <5:4>*		*orient_mode <3:2>*		*ud_en*	*enable*

Bit	Description
orient_theta	Coded value of the threshold angle with the horizontal plane, used in blocking modes. theta = 64*(gan(angle)^2); default value is 40, equivalent to 38 degrees angle
orient_blocking	Sets the blocking mode. If blocking is set, no orientation interrupt will be triggered. Default value is 3 – the most restrictive blocking mode
orient_mode	Sets the mode: symmetrical (values 0 or 3), high asymmetrical (value 1) or low asymmetrical (value 2)
ud_en	Enables the upside / downside detection in addition to landscape/portrait detection
enable	Enables the feature

7.20.11 INT Register 0x00A (INT_ORIENT_HYST)

RESET: 0x0080

This register configures the hysteresis of the orientation feature.

0x00A	INT_ORIENT_HYST							
Bit	15	14	13	12	11	10	9	8
Read/Write	R	R	R	R	R	R/W	R/W	R/W
Reset Value	0	0	0	0	0	0	0	0
Content	reserved					*orient_hyst <10:8>*		

0x00A	INT_ORIENT_HYST							
Bit	7	6	5	4	3	2	1	0
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset Value	1	0	0	0	0	0	0	0
Content	*orient_hyst <7:0>*							

Bit	Description
orient_hyst	Acceleration hysteresis for orientation detection.

7.20.12 INT Register 0x00B (INT_NO_MOT_TH)

RESET: 0x00AA

This register configures the no-motion interrupt threshold.

0x00B	INT_NO_MOT_INT							
Bit	15	14	13	12	11	10	9	8
Read/Write	R	R	R	R	R/W	R/W	R/W	R/W
Reset Value	0	0	0	0	0	0	0	0
Content	reserved				*no_mot_en*	*no_mot_th <10:8>*		

0x00B	INT_NO_MOT_INT							
Bit	7	6	5	4	3	2	1	0
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset Value	1	0	1	0	1	0	1	0
Content	*no_mot_th <7:0>*							

Bit	Description
no_mot_en	Enables the feature
no_mot_th	Defines the no-motion threshold

7.20.13 INT Register 0x00C (INT_NO_MOT_EN)

RESET: 0xE005

This register enables the no-motion feature and set the duration.

0x00C	INT_NO_MOT_EN							
Bit	15	14	13	12	11	10	9	8
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset Value	1	1	1	0	0	0	0	0
Content	*en_z*	*en_y*	*en_x*	*no_mot_dur <12:8>*				

0x00C	INT_NO_MOT_EN							
Bit	7	6	5	4	3	2	1	0
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset Value	0	0	0	0	0	1	0	1
Content	*no_mot_dur <7:0>*							

Bit	Description
en_x	Enables the feature on a per-axis basis: x axis
en_y	Enables the feature on a per-axis basis: y axis
en_z	Enables the feature on a per-axis basis: z axis
no_mot_dur	Defines the number of consecutive data points for which the threshold condition must be respected for interrupt assertion. It is expressed in 50 Hz samples (20 ms). Range is 0 to 163 s. Default value is 0x5 ≙ 100 ms.

7.21 Gyroscope Register Description

The entire communication with the device is performed by reading from and writing to registers. Registers have a width of 8 bits and are mapped to a common space of 64 addresses from GYR 0x00 up to GYR 0x3C. Within this range some registers are either completely or partially marked as ‘reserved’. Any reserved bit is ignored when it is written and no specific value is guaranteed when the bit is read. It is recommended not to use registers which are completely marked as ‘reserved’. Furthermore, it is recommended to mask out (logical and with zero) reserved bits of registers which are partially marked as ‘reserved’.

Registers with addresses from GYR 0x00 up to GYR 0x0E are read-only. Any attempt to write to these registers will be ignored. There are bits within some registers which trigger internal sequences. These bits are configured for write-only access and read as 0. An example for such a write-only access is the entire register GYR 0x14 (*BGW_SOFTRESET*).

The following table shows the register map of the SMI230 gyroscope.

Reg. Addr.	Register Name	Reset Value	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
0x3F	FIFO_DATA	n/a	fifo_data_output_register							
0x3E	FIFO_CONFIG_1	0x00	fifo_mode							
0x3D	FIFO_CONFIG_0	0x00		fifo_water_mark_level_trigger_retain						
0x3C	BIST	0x00				rate_ok		bist_fail	bist_rdy	trig_bist
0x34	BGW_SPI3_WDT_FIFO	0x00			ext_fifo_s_en	ext_fifo_s_sel		i2c_wdt_en	i2c_wdt_sel	
0x1E	FIFO_WM_EN	0x00	fifo_watermark_enable							

0x18	INT3_INT4_IO_MAP	0x00	int4_data		int4_fifo			int3_fifo		int3_data					
0x16	INT_EN_1	0x0F							int4_od	int4_lvl	int3_od	int3_lvl			
0x15	INT_EN_0	0x00	data_en	fifo_en											
0x14	BGW_SOFTRESET	0x00	softreset_cmd (0xb6)												
0x13	RATE_HBW	0x00	data_ high_bw	shadow_ dis											
0x11	GYRO_LPM1	0x00	power_mode [7:4]												
0x10	BW	0x80							bw [3:0]						
0x0F	RANGE	0x00								range [2:0]					
0x0E	FIFO_STATUS		fifo_overr un	fifo_frame_counter											
0x0A	INT_STATUS_1	0x00	data_int				fifo_int								
0x08	TEMP	0x00	temp [7:0]												
0x07	RATE_Z_MSB	0x00	rate_z_msb [15:8]												
0x06	RATE_Z_LSB	0x00	rate_z_lsb [7:0]												
0x05	RATE_Y_MSB	0x00	rate_y_msb [15:8]												
0x04	RATE_Y_LSB	0x00	rate_y_lsb [7:0]												
0x03	RATE_X_MSB	0x00	rate_x_msb [15:8]												
0x02	RATE_X_LSB	0x00	rate_x_lsb [7:0]												
0x00	CHIP_ID	0x0F	chip_id [7:0]												

	read / write
	write only
	read only
	reserved

All shown registers are common w/r registers:
Application specific settings which are not equal to the default settings must be re-set to their designated values after POR, soft reset and wake up from deep suspend.

7.21.1 GYR Register 0x00 (*CHIP_ID*)

This register contains the chip identification code.

0x00	*CHIP_ID*							
Bit	7	6	5	4	3	2	1	0
Read/Write	R	R	R	R	R	R	R	R
Reset Value	n/a	n/a	n/a	n/a	n/a	n/a	n/a	n/a
Content	*chip_id* <7:0>							

Register	Description
chip_id <7:0>	Fixed value 00001111 = 0x0F

7.21.2 GYR Register 0x02 (*RATE_X_LSB*)

This register contains the least significant bits of x-channel angular rate readout value (see section 7.17.2).

0x02	*RATE_X_LSB*							
Bit	7	6	5	4	3	2	1	0
Read/Write	R	R	R	R	R	R	R	R
Reset Value	n/a	n/a	n/a	n/a	n/a	n/a	n/a	n/a
Content	*rate_x_lsb* <7:0>							

Register	Description
rate_x_lsb <7:0>	Least significant 8 bits of rate x-channel read-back value (two's complement format)

7.21.3 GYR Register 0x03 (*RATE_X_MSB*)

This register contains the most significant bits of x-channel angular rate readout value (see section 7.17.2).

0x03	*RATE_X_MSB*							
Bit	7	6	5	4	3	2	1	0
Read/Write	R	R	R	R	R	R	R	R
Reset Value	n/a	n/a	n/a	n/a	n/a	n/a	n/a	n/a
Content	*rate_x_msb* <15:8>							

Register	Description
rate_x_msb <15:8>	Most significant 8 bits of rate x-channel read-back value (two's complement format)

7.21.4 GYR Register 0x04 (*RATE_Y_LSB*)

This register contains the least significant bits of y-channel angular rate readout value (see section 7.17.2).

0x04	*RATE_Y_LSB*							
Bit	7	6	5	4	3	2	1	0
Read/Write	R	R	R	R	R	R	R	R
Reset Value	n/a	n/a	n/a	n/a	n/a	n/a	n/a	n/a
Content	*rate_y_lsb* <7:0>							

Register	Description
rate_y_lsb <7:0>	Least significant 8 bits of rate y-channel read-back value (two's complement format)

7.21.5 GYR Register 0x05 (*RATE_Y_MSB*)

This register contains the most significant bits of y-channel angular rate readout value (see section 7.17.2).

0x05	*RATE_Y_MSB*							
Bit	7	6	5	4	3	2	1	0
Read/Write	R	R	R	R	R	R	R	R
Reset Value	n/a	n/a	n/a	n/a	n/a	n/a	n/a	n/a
Content	*rate_y_msb* <15:8>							

Register	Description
rate_y_msb <15:8>	Most significant 8 bits of rate y-channel read-back value (two's complement format)

7.21.6 GYR Register 0x06 (*RATE_Z_LSB*)

This register contains the least significant bits of z-channel angular rate readout value (see section 7.17.2).

0x06	*RATE_Z_LSB*							
Bit	7	6	5	4	3	2	1	0
Read/Write	R	R	R	R	R	R	R	R
Reset Value	n/a	n/a	n/a	n/a	n/a	n/a	n/a	n/a
Content	*rate_z_lsb* <7:0>							

Register	Description
rate_z_lsb <7:0>	Least significant 8 bits of rate z-channel read-back value (two's complement format)

7.21.7 GYR Register 0x07 (*RATE_Z_MSB*)

This register contains the most significant bits of z-channel angular rate readout value (see section 7.17.2).

0x07	*RATE_Z_MSB*							
Bit	7	6	5	4	3	2	1	0
Read/Write	R	R	R	R	R	R	R	R
Reset Value	n/a	n/a	n/a	n/a	n/a	n/a	n/a	n/a
Content	*rate_z_msb* <15:8>							

Register	Description
rate_z_msb <15:8>	Most significant 8 bits of rate z-channel read-back value (two's complement format)

7.21.8 GYR Register 0x08 (*TEMP*)

This register contains the current chip temperature (see section 0)

0x08	*TEMP*							
Bit	7	6	5	4	3	2	1	0
Read/Write	R	R	R	R	R	R	R	R
Reset Value	0	0	0	0	0	0	0	0
Content	*temp* <7:0>							

Register	Description
temp <7:0>	Temperature value (two's complement format) 00000010 corresponds to 25 °C

7.21.9 GYR Register 0x0A (*INT_STATUS_1*)

This register contains the interrupt status information.

0x0A	*INT_STATUS_1*							
Bit	7	6	5	4	3	2	1	0
Read/Write	R	R	R	R	R	R	R	R
Reset Value	n/a	n/a	n/a	n/a	n/a	n/a	n/a	n/a
Content	*data_int*	*reserved*		*fifo_int*	*reserved*			

Register	Description
data_int	New data interrupt status 0: inactive 1: active
fifo_int	FIFO interrupt status 0: inactive 1: active

7.21.10 GYR Register 0x0E (*FIFO_STATUS*)

This register contains the FIFO status information

0x0E	*FIFO_STATUS*							
Bit	7	6	5	4	3	2	1	0
Read/Write	R	R	R	R	R	R	R	R
Reset Value	n/a	n/a	n/a	n/a	n/a	n/a	n/a	n/a
Content	*fifo_overrun*	*fifo_frame_counter*						

Register	Description
fifo_overrun	If set, FIFO overrun condition has occurred. Note: flag can only be cleared by writing to the FIFO configuration register FIFO_CONFIG_1
fifo_frame_counter	Current fill level of FIFO buffer. An empty FIFO corresponds to 0x00. The frame counter can be cleared by reading out all frames from the FIFO buffer or writing to the FIFO configuration register FIFO_CONFIG_1.

7.21.11 GYR Register 0x0F (*RANGE*)

This register allows for the selection of the gyroscope angular rate measurement range.

0x0F	*RANGE*							
Bit	7	6	5	4	3	2	1	0
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset Value	0	0	0	0	0	0	0	0
Content	*reserved*					*range* <2:0>		

Register	Description
range <2:0>	Selection of the gyroscope angular rate range Resolution

range <2:0>	rate range	Resolution [LSB / °/s]
000	±2000 °/s	16.38
001	±1000 °/s	32.77
010	±500 °/s	65.54
011	±250 °/s	131.07
100	±125 °/s	262.14

All other settings are reserved (do not use)

reserved	Write 0

7.21.12 GYR Register 0x10 (*BW*)

This register allows for the selection of the rate data filter bandwidth.

0x10	BW							
Bit	7	6	5	4	3	2	1	0
Read/Write	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset Value	1	0	0	0	0	0	0	0
Content	*reserved*				*bw* <3:0>			

Register	Description
bw <3:0>	Selection of the data filter bandwidth

bw <3:0>	Bandwidth	*bw* <3:0>	Bandwidth
0111	32 Hz	0011	47 Hz
0110	64 Hz	0010	116 Hz
0101	12 Hz	0001	230 Hz
0100	23 Hz	0000	unfiltered (523 Hz)

All other settings are reserved (do not use)

reserved	Write 0

7.21.13 GYR Register 0x11 (GYRO_LPM1)

This register allows for the selection of the power mode.

0x11	GYRO_LPM1							
Bit	7	6	5	4	3	2	1	0
Read/Write	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset Value	0	0	0	0	0	0	0	0
Content	*power mode*				*reserved*			

Register	Description
power mode <7:4>	Selection of power mode 0x00: normal mode 0x80: suspend mode 0x20: deep suspend mode
reserved	Write 0

7.21.14 GYR Register 0x13 (*RATE_HBW*)

This register controls the angular rate data acquisition and data output format.

0x13	RATE_HBW							
Bit	7	6	5	4	3	2	1	0
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset Value	0	0	0	0	0	0	0	0
Content	*data_high_bw*	*shadow_dis*	*reserved*					

Register	Description
data_high_bw	Data-read from the rate data registers 1: unfiltered 0: filtered
shadow_dis	Shadowing mechanism for the rate data output registers 1: disable 0: enable
reserved	Write 0

7.21.15 GYR Register 0x14 (*BGW_SOFTRESET*)

This register controls the user triggered reset of the sensor.

0x14	*BGW_SOFTRESET*							
Bit	7	6	5	4	3	2	1	0
Read/Write	W	W	W	W	W	W	W	W
Reset Value	0	0	0	0	0	0	0	0
Content	*softreset<7:0>*							

Register	Description
softreset<7:0>	Writing 0xB6 to the register triggers a reset. Other values are ignored. After a delay, all user configuration settings are overwritten with their default values. Please note that all application specific settings which are not equal to the default settings must be reconfigured to their designated values.

7.21.16 GYR Register 0x15 (*GYRO_INT_CTRL*)

This register enables the new data interrupt and FIFO interrupt. See register GYR 0x0A (*INT_STATUS_1*).

0x15	*GYRO_INT_CTRL*							
Bit	7	6	5	4	3	2	1	0
Read/Write	R/W	R/W	R	R	R	R	R	R
Reset Value	0	0	0	0	0	0	0	0
Content	*data_en*	*fifo_en*	*reserved*					

Register	Description
data_en	enables the new data interrupt 0: disabled 1: enabled
fifo_en	enables the FIFO interrupt 0: disabled 1: enabled

7.21.17 GYR Register 0x16 (*INT_EN_1*)

This register contains interrupt pin configurations.

0x16	*INT_EN_1*							
Bit	7	6	5	4	3	2	1	0
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset Value	0	0	0	0	1	1	1	1
Content	*reserved*				*int4_od*	*int4_lvl*	*int3_od*	*int3_lvl*

Register	Description
int4_od	Behavior for INT4 pin 0: push-pull 1: open drain
int4_lvl	Active level for INT4 pin 0: disabled 1: enabled
int3_od	Behavior for INT3 pin 0: push-pull 1: open drain
int3_lvl	Active level for INT3 pin 0: disabled 1: enabled
reserved	Write 0

7.21.18 GYR Register 0x18 (*INT3_INT4_IO_MAP*)

This register controls if interrupt signals are mapped to the INT3 / INT4 pin.

0x18	*INT3_INT4_IO_MAP*							
Bit	7	6	5	4	3	2	1	0
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset Value	0	0	0	0	0	0	0	0
Content	*int4_data*	*reserved*	*int4_fifo*	*reserved*		*int3_fifo*	*reserved*	*int3_data*

Register	Description
int4_data	Map new data interrupt to the INT4 pin 0: disabled 1: enabled
int4_fifo	Map FIFO interrupt to the INT4 pin 0: disabled 1: enabled
Int3_fifo	Map FIFO interrupt to the INT3 pin 0: disabled 1: enabled
int3_data	Map new data interrupt to the INT3 pin 0: disabled 1: enabled

7.21.19 GYR Register 0x1E (*FIFO_WM_ENABLE*)

This register enables FIFO watermark level or FIFO full interrupt.

0x1E	*FIFO_WM_ENABLE*							
Bit	7	6	5	4	3	2	1	0
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset Value	0	0	0	0	1	0	0	0
Content	*fifo_wm_enable*							

Register	Description
fifo_wm_enable	Enables FIFO watermark level or FIFO full interrupt 0x08: FIFO full is used 0x88: FIFO watermark is used

7.21.20 GYR Register 0x34 (*BGW_SPI3_WDT_FIFO*)

This register contains settings for the digital interfaces.

0x34	*BGW_SPI3_WDT_FIFO*							
Bit	7	6	5	4	3	2	1	0
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset Value	0	0	0	0	0	0	0	0
Content	*reserved*		*ext_fifo_s_en*	*ext_fifo_s_sel*	*reserved*	*i2c_wdt_en*	*i2c_wdt_sel*	*reserved*

Register	Description
ext_fifo_s_en	Enables external FIFO synchronization mode 0: disable 1: enable
ext_fifo_s_sel	selects source for external FIFO synchronization 0: source is INT3 pin 1: source is INT4 pin
i2c_wdt_en	Watchdog timer at the SDA pin in TWI mode 0: disable 1: enable
i2c_wdt_sel	Watchdog timer period 0: 1 ms 1: 50 ms

7.21.21 GYR Register 0x3C (*BIST*)

This register contains the built-in self-test (BIST) options (see section 0).

0x3C	*BIST*							
Bit	7	6	5	4	3	2	1	0
Read/Write	R/W	R/W	R/W	R	R/W	R	R	W
Reset Value	0	0	0	0	0	0	0	0
Content	*reserved*			*rate_ok*	*reserved*	*bist_fail*	*bist_rdy*	*trig_bist*

Register	Description
rate_ok	1: indicates proper sensor function, no trigger is needed for this
bist_fail	Contains the fail flag, needs to be evaluated together with *bist_rdy*
bist_rdy	Status of BIST, needs to be evaluated together with *bist_fail* *bist_rdy* | *bist_fail* | Status 0 | - | BIST not finished 1 | 0 | BIST ok, sensor ok 1 | 1 | BIST not ok, sensor values not in expected range
trig_bist	Write 1: perform the BIST
reserved	Write 0

7.21.22 GYR Register 0x3D (*FIFO_CONFIG_0*)

This register defines the FIFO watermark level.

0x3D	*fifo_config_0*							
Bit	7	6	5	4	3	2	1	0
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset Value	0	0	0	0	0	0	0	0
Content	*reserved*	*fifo_water_mark_level_trigger_retain*						

Register	Description
fifo_water_mark_level_trigger_retain	fifo_water_mark_level_trigger_retain <6:0> defines the FIFO watermark level. An interrupt will be generated, when the number of entries in the FIFO exceeds fifo_water_mark_level_trigger_retain<6:0>. Writing to this register clears the FIFO buffer.

7.21.23 GYR Register 0x3E (*FIFO_CONFIG_1*)

This register contains FIFO configuration settings.

0x3E	*FIFO_CONFIG_1*							
Bit	7	6	5	4	3	2	1	0
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset Value	0	0	0	0	0	0	0	0
Content	*fifo_mode*		*reserved*					

Register	Description
fifo_mode	Contains FIFO configuration settings. The FIFO buffer memory is cleared and the fifo-full flag is cleared when writing to FIFO_CONFIG_1 register. In addition, the FIFO overrun flag is cleared (if overrun occurred before). 0x40: FIFO mode - data collection stops once buffer is full (i.e. filled with 100 frames) 0x80: STREAM mode - sampling continues when buffer is full (i.e. filled with 99 frames); old is discarded else: reserved

7.21.24 GYR Register 0x3F (*FIFO_DATA*)

This register contains the FIFO data readout.

0x3F	*FIFO_DATA*							
Bit	7	6	5	4	3	2	1	0
Read/Write	R	R	R	R	R	R	R	R
Reset Value	n/a	n/a	n/a	n/a	n/a	n/a	n/a	n/a
Content	*fifo_data_output_register*							

The format of the LSB and MSB components corresponds to that of the angular rate data readout registers. Read burst access may be used since the address counter will not increment when the read burst is started at the address of FIFO_DATA. The entire frame is discarded when a fame is only partially read out.

The format of the data read-out from register 0x3F is as follows:

Figure 41 Format of the data read-out from register 0x3F

8 Safety Concept

Not applicable.

9 Functional and Lifetime Qualification Test Plan

The SMI230 passed the following qualification: AEC-Q100 grade 2.

10 Disclaimer

In order to ensure proper functionality during operation, it is the responsibility of the customer to evaluate:

- The proper function of the sensor in the overall system.
- The mechanical stability of each system design including the sensor.
- The electrical stability, e.g. power supply and EMC, of each system design including the sensor.

Safety and warning notes

Please note that the sensor may be seriously damaged or sensor performance might be influenced by:

- Exceeding the maximum operating conditions. The sensor must be discarded when exceeding these limits.
- Electrostatic discharge. A proper ESD environment during handling and processing of the sensor has to be in place.
- Exceeding the qualification reflow profile. The maximum soldering profile as well as the maximum number of reflow cycles must be observed.
- Exceeding the mission profile: In case a different mission profile than the referred one shall be applied, it needs to be verified whether this profile is still covered by the qualification.
- Improper mechanical connection between the sensor and the PCB and any measure that alters the mechanical stress imposed on the sensor (such as, e.g. soldering, potting, coating, overmolding, etc.). Any measure on application level is considered to be application specific and has to be chosen with care by and in responsibility of the customer

Target market: The product is described by Bosch for the intended application (cf. Chapter 1) and released on the basis of the legal and normative requirements relevant to the Bosch product for use in the following target markets as follows:

The sensor complies with all statutory regulations regarding restriction of hazardous substances and recyclability which are in the scope of IMDS, insofar as such restrictions of hazardous substances and recyclability are regarded, the target market of the sensor is worldwide.

Functional Safety: Bosch points out that the system/product does not implement any ASIL-classified requirements (in the sense of ISO 26262). Therefore, it has not been approved by Bosch for applications in which Bosch delivered system/product has an ASIL related (above QM) role.

This implies the following limitations:

- The SMI230 must not be used if it influences safety goals with ratings higher than ASIL QM. Safety goals are defined in the overall system.
- Bosch cannot provide any quantitative failure analysis (e.g. FTA or FMEDA) for the SMI230.
- The SMI230 does not provide a CRC to check communication errors within a SPI/I2C frame.
- The SMI230 does not provide error flags to detect malfunctions of the ASIC.

Repair of the product is not possible. Manual soldering of sensors is not permitted.
Sensors must not be handled as bulk goods.
Sensors with visible damages (housing, connectors, pins, etc.) and sensors which might have exceeded the absolute maximum ratings must not be mounted in the vehicle. These sensors must be scrapped.

Data Security: The sensor only contains the explicitly stated characteristics for product, data and information security. It is the responsibility of the system integrator to verify and validate on system level, if the stated characteristics comply with and fulfil the requirements of the product.

Assessment of Products Returned from Field: Returned products are considered good if they fulfill the specifications / test data for 0-mileage and field listed in this document.

Due to the measurement principle, the sensor is sensitive to mechanical disturbances, such as shocks, vibrations or stress. Therefore, the printed circuit board (PCB) has to be designed in such a way, as to suppress any of these influences and ensure the proper functionality in each application.

The sensor elements have to be protected against extreme shock loads such as e.g. hammer blows on or next to the sensor elements, vibrations of a power wrench when fixing bolts, dropping of the sensor elements onto hard surfaces, etc.. Sensor modules which have been dropped must not be used and have to be scrapped. We recommend the avoidance of g-forces beyond the maximum rating during transport, handling and mounting of the sensors resulting in a defined and qualified installation process. As the sensor is sensitive to mechanical stress, any bending or torsion of the PCB close to the sensor, e.g during forcing in, has to be avoided.

Engineering Samples: Engineering samples are marked with (e) or (E). Samples may vary from the valid technical specifications of the series product contained in this data sheet. Therefore, they are not intended or fit for resale to third parties or for use in end products. Their sole purpose is internal client testing. The testing of an engineering sample may in no way replace the testing of a series product. Bosch assumes no liability for the use of engineering samples. The purchaser shall indemnify Bosch from all claims arising from the use of engineering samples.

11 Changes

This TPD is on basis of SMI230 Technical Customer Documentation (TCD) 1 279 929 990 Rev. 2.1.

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