VLSI Assignment 2 Report

Konsoulas Konstantinos

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Contents

1 Introduction

In this assignment we are tasked to create the I-V characteristics of MOSFETS, measure the transistor's resistance by using different techniques, consider the voltage drop that transistors can cause and its connection to VT and last but not least examine the inverter and its behaviour for different values of voltage. The simulations were performed for level 3 transistors MOSIS-TSMC 0.25μm with dimensions W = 3μm, L = 2μm. Below we dive into each subject in detail.

2 Exercise I

2.1 I-V Characteristics of NMOS / PMOS

Using Ngspice we created the I-V characteristics of NMOS and PMOS. The blue line at figures 1 ,2 represent the Vds = Vgs-Vt points for every value of Vgs. Those points split the characteristics into linear and saturation regions (left and right side respectively).

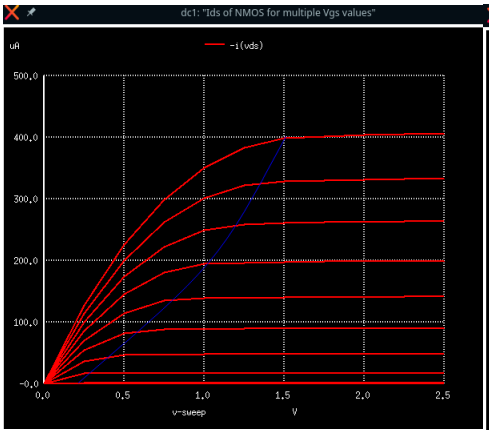


Figure 1: NMOS I-V Characteristics

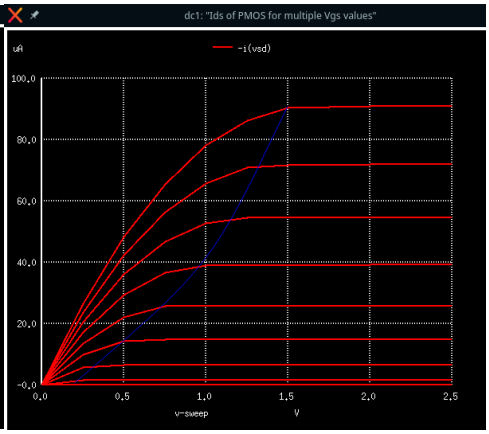


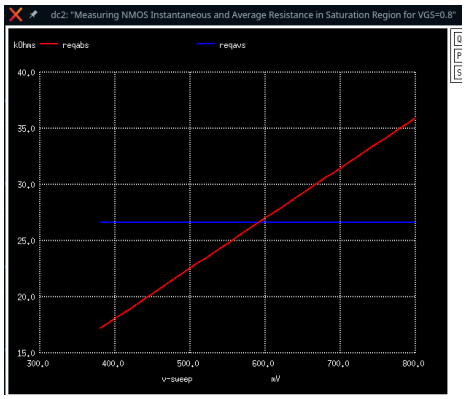
Figure 2: PMOS I-V Characteristics

From the above figures we can observe that even though Vgs increases by a constant amount from one characteristic to another the distance between saturation regions is not fixed but it is increasing. Additionally velocity-saturation causes the devices to saturate for substantially smaller values of Vds.

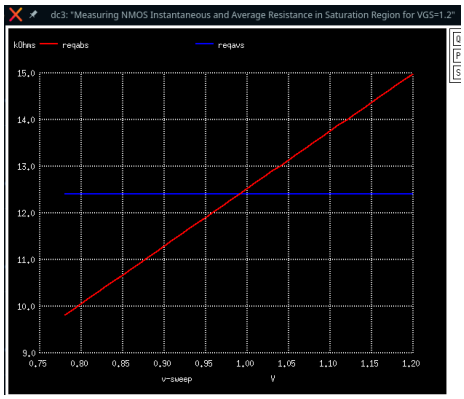
2.2 Instantaneous & Mean MOSFET Resistance in Saturation Region

Looking at any plot we can examine that as we are increasing V_{ds} the MOSFET's instantaneous Resistance increases linearly. As we are in saturation region increasing V_{gs} has no effect on Ids so according to Ohm's law $R_{mosfet} = V_{ds}/I_{ds}$ we can justify this linear increase.

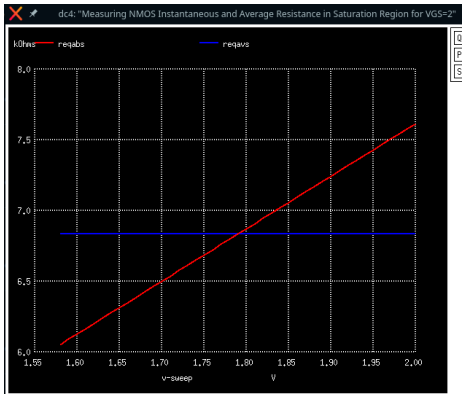
Except from that we can observe that increasing V_{gs} drastically decreases the resistance. That can be explained by the I_{ds} -V_{gs} relationship in the I-V characteristics of the mosfets.



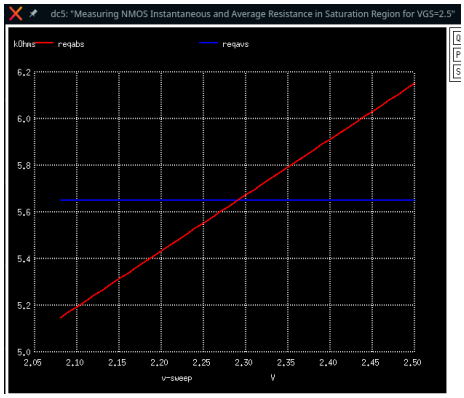
(a) Vgs = 0.8



(b) Vgs = 1.2



(c) Vgs = 2

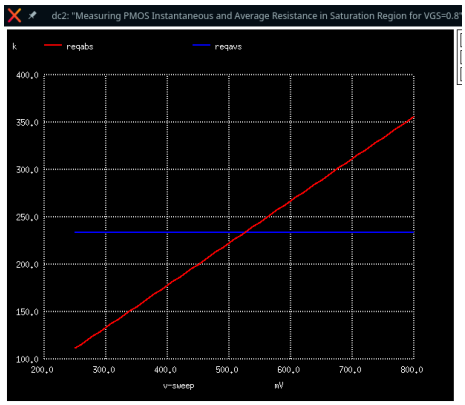


(d) Vgs = 2.5

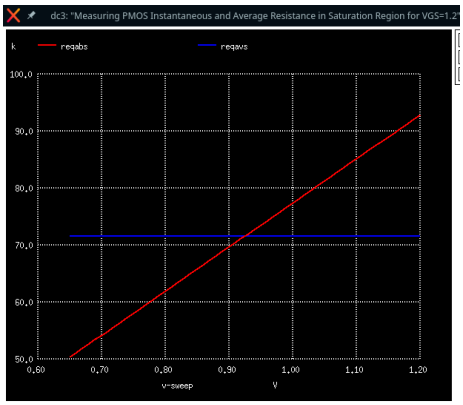
Figure 3: Instantaneous & Mean NMOS Resistance for Multiple Vgs

We have measured the following mean resistances of NMOS transistor for different values of Vgs:

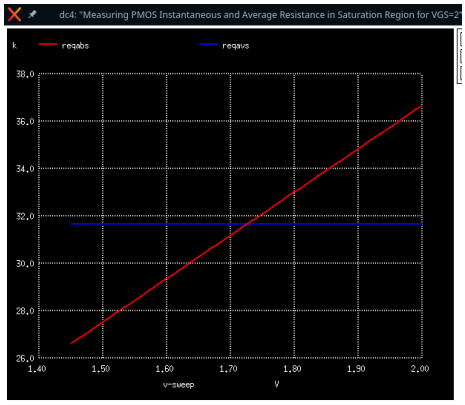
- $Vgs = 0.8 \rightarrow R_{mean} = 2.659175e + 04$ Ohm
- $Vgs = 1.2 \rightarrow R_{mean} = 1.240539e + 04$ Ohm
- $Vgs = 2 \rightarrow R_{mean} = 6.835110e + 03$ Ohm
- $Vgs = 2.5 \rightarrow R_{mean} = 5.649810e + 03$ Ohm



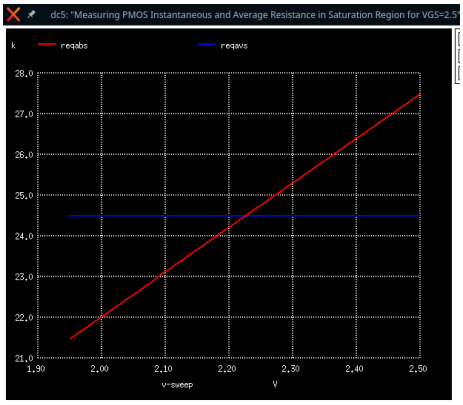
(a) Vgs = 0.8



(b) Vgs = 1.2



(c) Vgs = 2



(d) Vgs = 2.5

Figure 4: Instantaneous & Mean PMOS Resistance for Multiple Vgs

Similarly we have measured the mean resistances of PMOS transistor for different values of Vgs:

- $Vgs = 0.8 \rightarrow R_{mean} = 2.337480e + 05$ Ohm
- $Vgs = 1.2 \rightarrow R_{mean} = 7.162026e + 04$ Ohm
- $Vgs = 2 \rightarrow R_{mean} = 3.164524e + 04$ Ohm
- $Vgs = 2.5 \rightarrow R_{mean} = 2.448629e + 04$ Ohm

2.3 Equivalent RC Transistor Resistance

After discharging and charging an 0.1pF Capacitor with NMOS and PMOS respectively we were able to calculate the equivalent resistance using $t_p = ln(2) * \tau = 0.69 * R_{eq} * C_L$ formula.

- $NMOS \rightarrow R_{mean} = 5.953588e + 03$ Ohm
- $PMOS \rightarrow R_{mean} = 2.668672e + 04$ Ohm

Evaluating the measurements we can point out that the PMOS transistor has approximately 4 times larger resistance than the NMOS one. That is not surprising as we know that generally PMOS transistors have a worse carrier mobility than their NMOS counterparts . Additionally the current measurements are more pessimistic than the previous ones for the same V_{gs} . Below are given the corresponding plots.

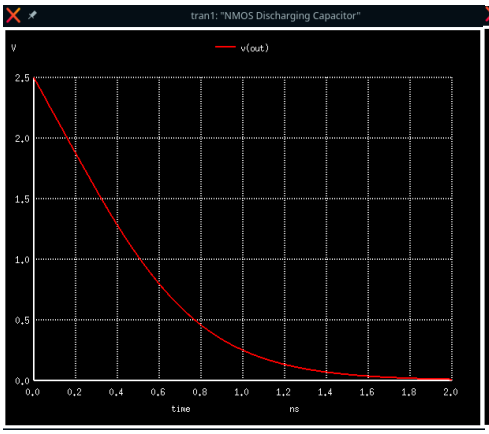


Figure 5: NMOS Discharging Capacitor

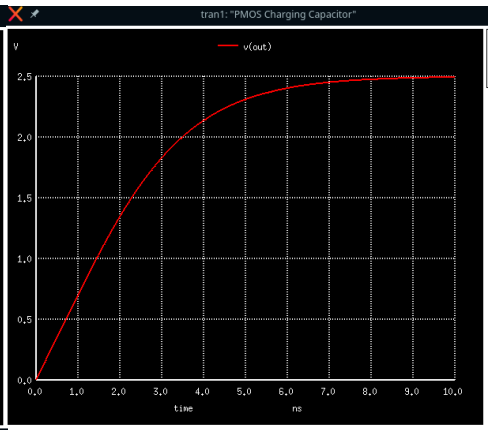


Figure 6: PMOS Charging Capacitor

3 Exercise II

In the following exercise we were instructed to measure V_T by simulating the Voltage drop that transistors can cause. Using Ngspice we were able to perform transient analysis and extract data and plots for both kinds of transistors. The following figures present the plots showing the voltage drop of one NMOS and 2 NMOS transistors in series.

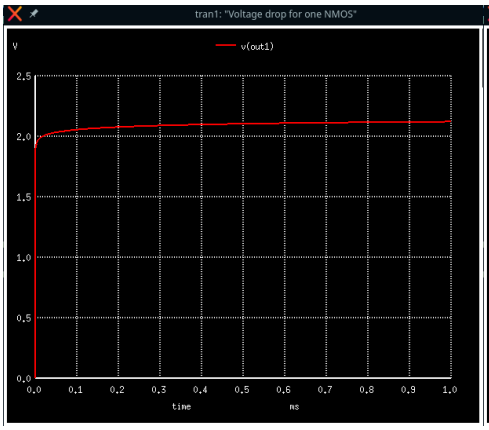


Figure 7: NMOS Voltage Drop

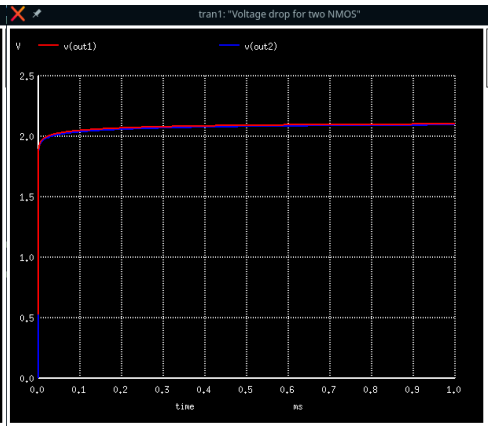


Figure 8: NMOS in Series Voltage Drop

The NMOS transistor / transistors in series are charging a capacitor in order to make visible the voltage drop. At the end of the plot (after 1ms of time) we measure V(out1)= 2.120477e+00 V / V(out1)= 2.102046e+00 V , V(out2)= 2.095181e+00 V respectively.

The reason why the voltage drops approximately at around the V_T is because NMOS transistors are on only on when $V_{gs} \geq V_T$. When the source reaches a certain amount of Voltage therefore the transistor turns off and stops charging the capacitor. This will be the case regardless of how many transistors are connected in series. Below are also given the respective plots for the PMOS transistors.

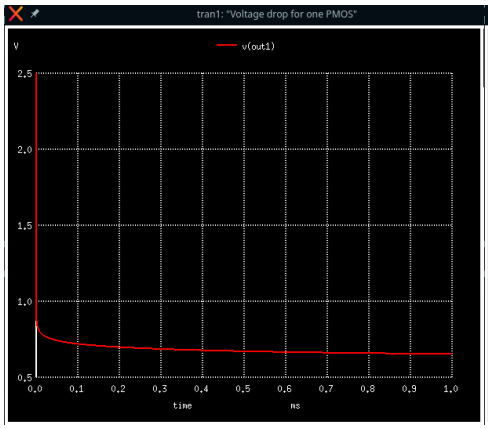


Figure 9: PMOS Voltage Drop

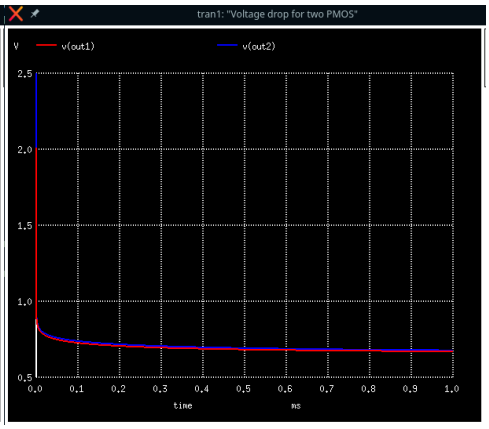


Figure 10: PMOS in Series Voltage Drop

The PMOS transistor / transistors in series are discharging a capacitor in order to make visible the voltage drop. At the end of the plot (after 1ms of time) we measure V(out1)= 6.529077e-01 V / V(out1)= 6.698341e-01 V , V(out2)= 6.772350e-01 V respectively. The same explanation why this happens can be given to PMOS as well with the adjustment that $|V_{gs}| \geq |V_T|$ is required to keep the transistors on.

4 Exercise III

4.1 Inverter Voltage Transfer Characteristics

In this exercise we were tasked to simulate an inverter with Ngspice, plot the voltage transfer characteristics and compute based on that the $V_{IL}, V_{OL}, V_{IH}, V_{OH}, V_M$ and the noise margins. Below in figure 11 is given the plot as extracted from spice.

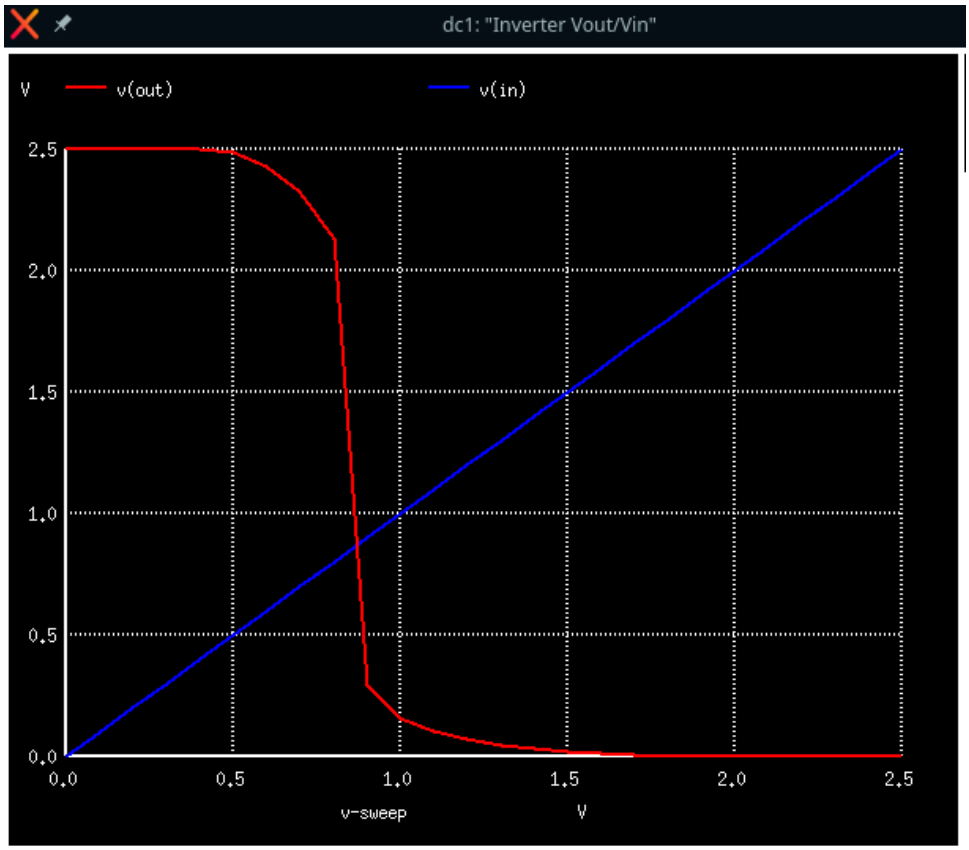


Figure 11: Inverter Voltage Transfer Characteristics

Based on that we calculated the desired values:

- V_{IL} = 6.298162e-01 V
- V_{OH}= 2.400618e+00 V
- V_{IH} = 9.995089e-01 V
- V_{OL} = 1.577376e-01 V
- V_M = 8.687006e-01 V
- Margin High = 1.500491e+00 V
- Margin Low = 6.298162e-01 V

Following it is requested to modify the size of the transistors in order to make the noise margins as symmetrical as possible. The lower mobility of holes compared to electrons makes the pull up network much weaker than the pull down one and it is needed to balance them. To achieve that we enlarge the PMOS transistor's width to allow more current to pass through. Below in figure 12 is given the plot of the balanced inverter as extracted from spice.

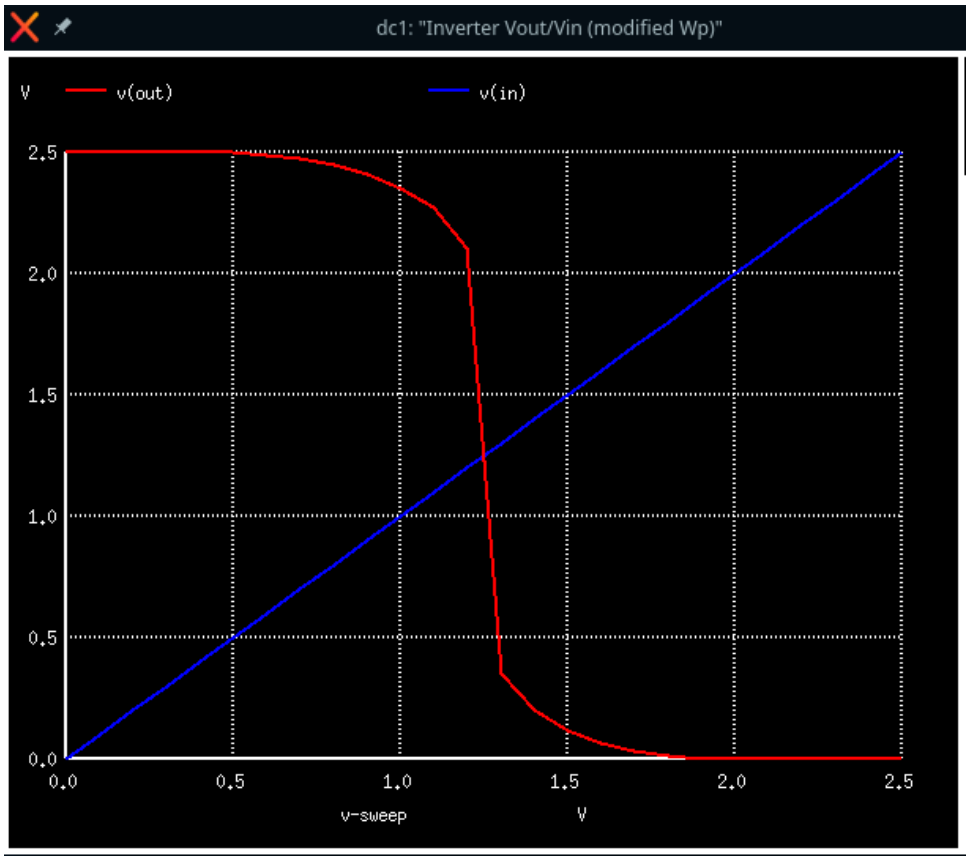


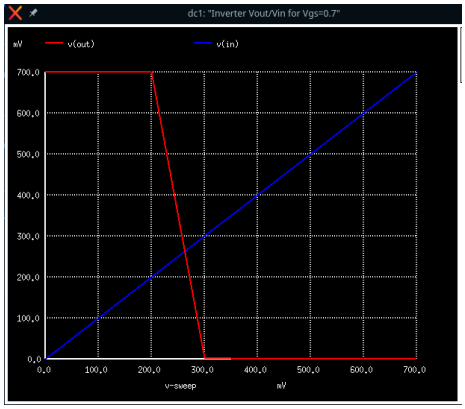
Figure 12: Inverter Voltage Transfer Characteristics (Balanced)

Based on that we once again calculated the desired values:

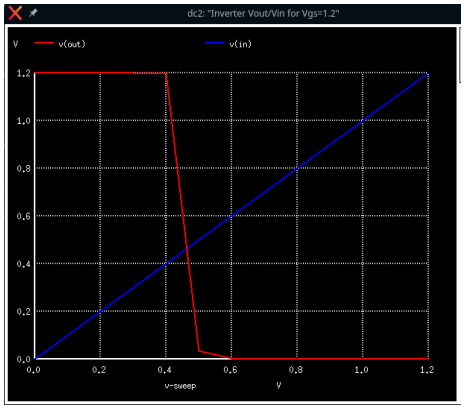
- V_{IL} = 1.055396e+00 V
- V_{OH}= 2.307527e+00 V
- V_{IH} = 1.433366e+00 V
- V_{OL} = 1.741941e-01 V
- V_M = 1.248797e+00 V
- Margin High = 1.066634e+00 V
- Margin Low = 1.055396e+00 V

4.2 Effects of Voltage Scaling

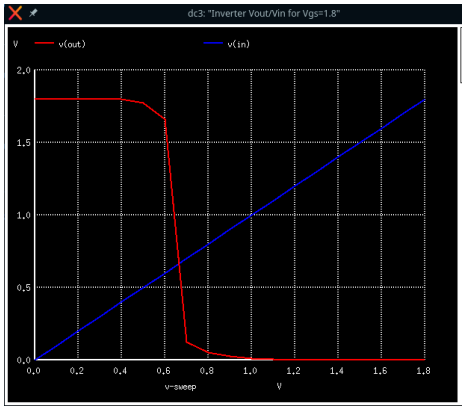
Scaling the voltage of V_{gs} to the values {0.7, 1.2, 1.8} we can observe possible changes at the noise margins, current and power. The characteristics are given in figure 13



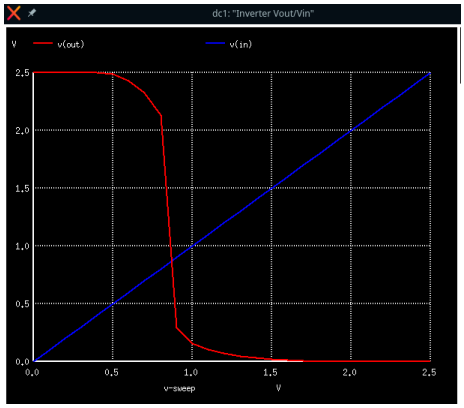
(a) Vgs = 0.7



(b) Vgs = 1.2



(c) Vgs = 1.8



(d) Vgs = 2.5

Figure 13: Inverter Voltage Transfer Characteristics for Multiple Vgs

In the following table are given the corresponding measurements:

Vgs(V)	M_{high}(V)	M_{low}(V)	I(A)	P(W)
0.7	3.283114e-01	1.286066e-01	1.917420e-10	1.342194e-10
1.2	6.143443e-01	3.168787e-01	8.839240e-08	1.060709e-07
1.8	1.006718e+00	5.039203e-01	1.622608e-06	2.920695e-06
2.5	1.500491e+00	6.298162e-01	6.684952e-06	1.671238e-05

We can examine that margins tend to get less uneven while we are scaling down the voltage but that trend falls short when the voltage reaches 0.7V. To be more exact M_{high} is getting proportionally smaller and M_{low} proportionally larger.The total margin space portion seems to get smaller proportionally to V_{dd} . Decreasing the Voltage also decreases the current and the power consumed. At the figure below is given the power graph for the different values of V_{gs}

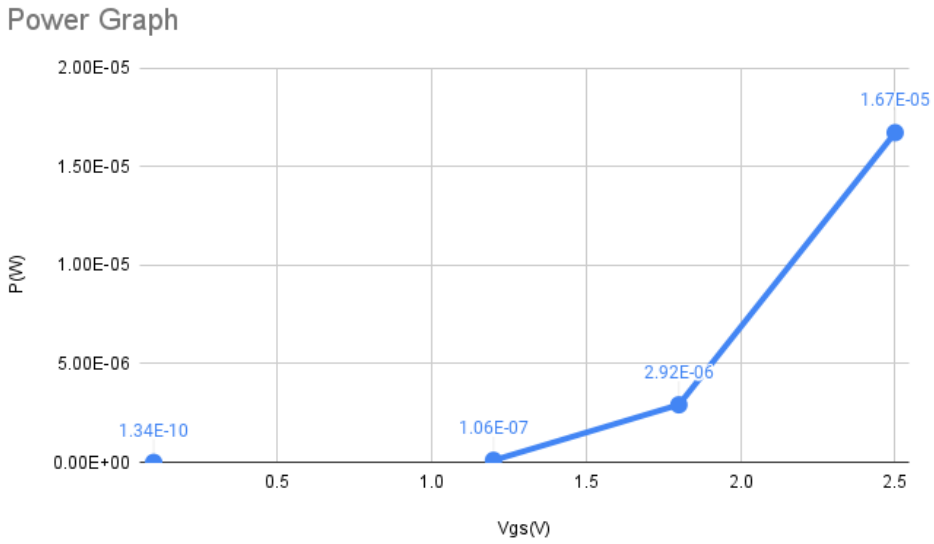


Figure 14: Power for different values of Vgs