VLSI Assignment 4 Report

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1 Introduction

In this assignment we are tasked to create an **active low static latch** using *Ngspice* electronic circuit simulator. Thenceforth we are required to put the circuit in all the possible states in order to verify it's correct operation. In addition it is assigned to repeat the same process for a **negative edge Flip-Flop** while performing some required measurements.

2 Active Low Static Latch

2.1 Ngspice Circuit Design & Verification

At this part of the assignment we have to model the **active low static latch** described by the following schematic:

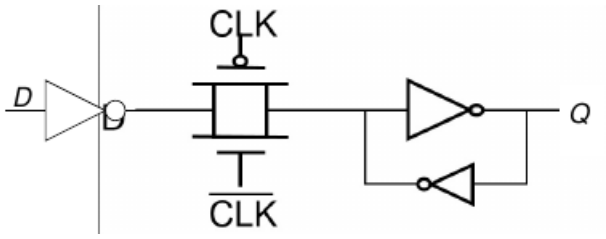

Figure 1: Active Low Static Latch Schematic

The circuit has the following truth table:

CLK	Q'
0	D
1	Q

Which can be expanded into the next truth table:

CLK	D	Q'
0	0	0
0	1	1
1	0	Q
1	1	Q

After implementing the circuit into *Ngspice* we performed the necessary testing simulation and extracted the graph required to prove the circuit's correct operation. The graph is given below:

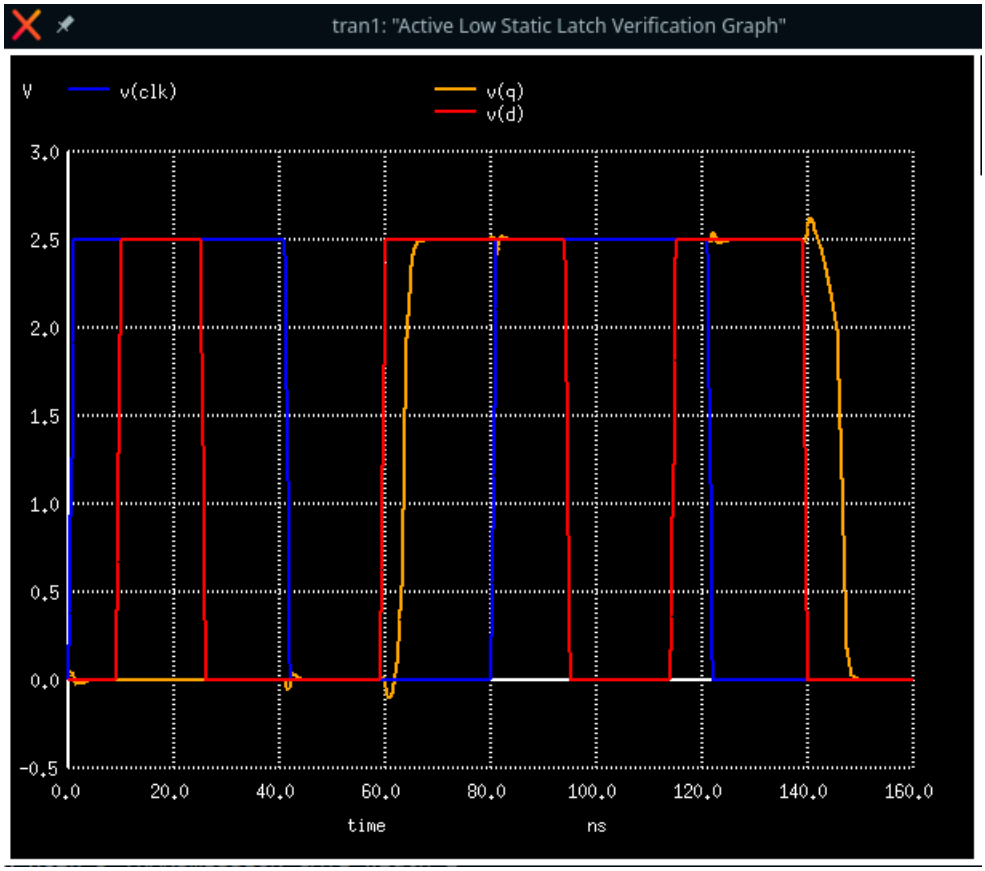

Figure 2: Active Low Static Latch Verification Graph

It can be easily observed that the circuit behaves as described by the truth table. The output (V(q)) matches the input (V(d)) when the clock (V(clk)) is 0 but is non responsive when the clock is set to high.

3 Negative Edge Flip-Flop

3.1 Ngspice Circuit Design & Verification

Similar to the first part it is required to model the **negative edge Flip-Flop** described by the following schematic:

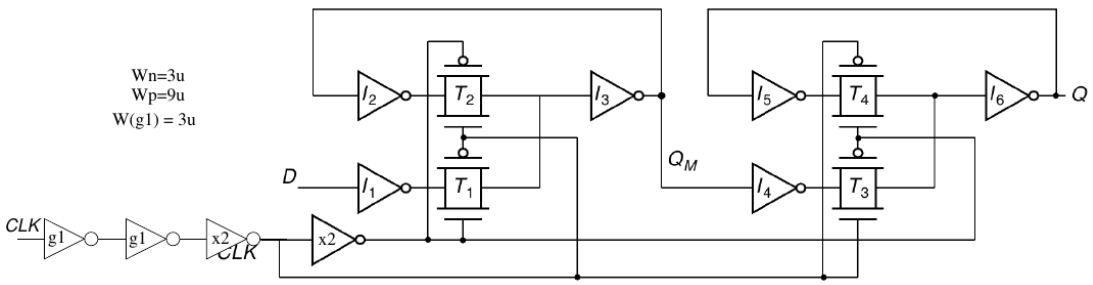

Figure 3: Negative Edge Flip-Flop Schematic

The circuit has the following truth table:

CLK	Q'
↓	D
X	Q

Which can be expanded into the next one:

CLK	D	Q'
↓	0	0
↓	1	1
X	0	Q
X	1	Q

Following the Ngspice implementation, the necessary testing was performed in order to prove the circuit's correct operation. The following graph as extracted from Ngspice can verify the circuit's truth table:

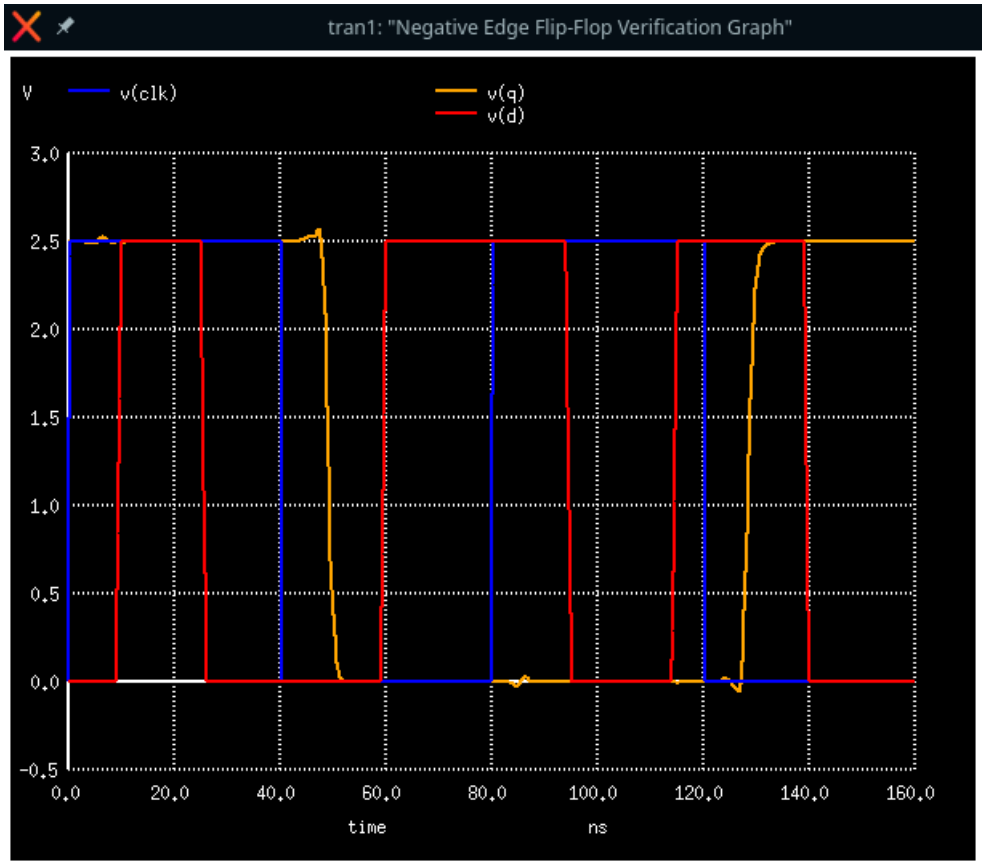

Figure 4: Negative Edge Flip-Flop Verification Graph

It can be easily observed that the circuit behaves as described by the truth table. The output (V(q)) matches the input (V(d)) shortly after the negative edge of the clock but is non responsive when the clock is set to any other value. The reasoning about this phenomenon will be given in the measurements part.

3.2 Essential Measurements

Having assembled successfully the circuit and verifying it's correct operation we ought to perform some basic measurements. Being more specific we have to measure $CLK \rightarrow Q$ delay (1), the rise (t_r) and fall (t_f) delays of QM and Q nodes (2) and finally the setup and hold time of our Flip-Flop (3). It should be noted that all the measurements were performed for $t_{rf}(CLK) = 0.2ns$. The table containing (1), (2) measurements is given below :

$\{t_{rf}(D), C_Q\}$	$t_{CLK\to Q}(fall)$	$t_{CLK\to Q}(rise)$	$t_f(QM)$	$t_r(QM)$	$t_f(Q)$	$t_r(Q)$
{200ps , Cg1}	10.31ns	10.20ns	3.81ns	7.45ns	3.97ns	3.53ns
{200ps , 2Cg1}	11.07ns	11.35ns	3.76ns	7.67ns	5.18ns	4.51ns
{400ps , Cg1}	10.63ns	10.08ns	3.76ns	7.99ns	4.08ns	3.60ns
{400ps , 2Cg1}	11.27ns	11.20ns	3.84ns	8.09ns	5.38ns	4.61ns

The current table is able to provide insight in our Flip-Flop. Specifically an increase in capacitance at the output (Q) can increase the $CLK \to Q$ delay and the $t_{rf}(Q)$ delays. This is natural as a greater capacitance at the output requires more electric charge to reach the same voltage and therefore more time to charge. The $t_{rf}(QM)$ delay also seems to be positively correlated although the data is not clear enough.

The $t_{rf}(D)$ delay variations do not provide clear data for the current table. The $t_{rf}(Q)$ delays seem to be positively correlated but that should be the cause of the setup and hold time changes measured (3) provided at the table below:

$\{t_{rf}(D), C_Q\}$	Setup Time	Hold Time
{200ps , Cg1}	0	3.6ns
{200ps , 2Cg1}	0	3.6ns
{400ps , Cg1}	0	3.4ns
{400ps , 2Cg1}	0	3.4ns

Examining the data provided from this table we can immediately notice that the required setup time measured is actually 0 seconds. This is happening as our Flip-Flop is not sensing our external clock but it's own delayed internal clock. This delay is actually allowing our input signal to have enough time to change the circuit's state even if it arrives right at the edge of the external clock. Therefore the "true" clock of the circuit is actually its internal clock and according to it changes the state of the circuit (thus the large delays visualised at the verification graph).

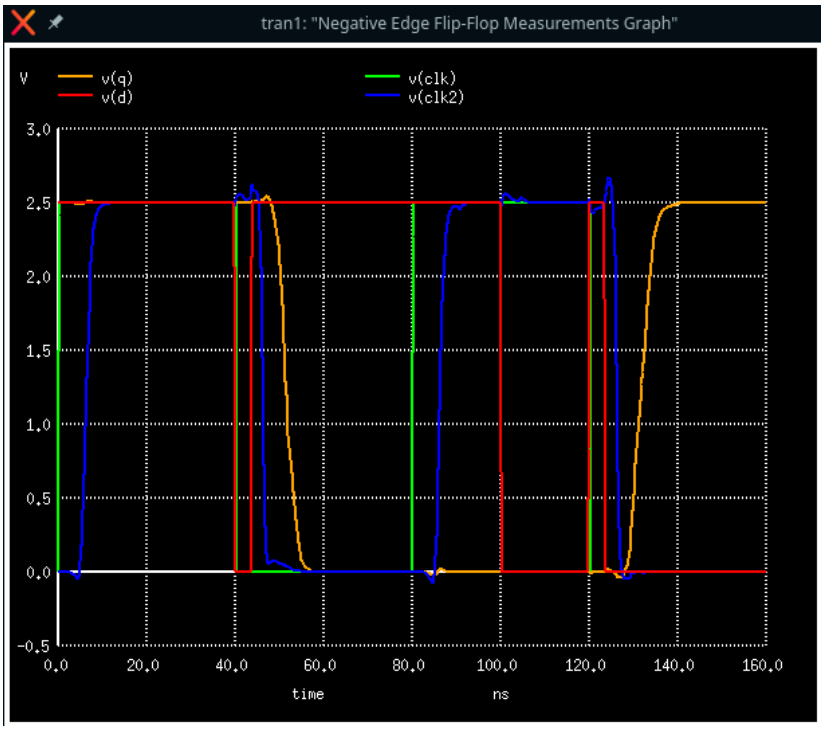

Figure 5: Negative Edge Flip-Flop Measurements Graph

Finally utilising the graph above we were able using the old fashioned trial & error method to figure out the minimum hold time required by each combination. The input is required to be stable long enough in order to not change the circuit's state before the internal clock can validate it. Increasing the $t_{rf}(D)$ delay allows a slower change in the circuit's state therefore decreasing the required hold time.