VLSI Assignment 3 Report

Konsoulas Konstantinos

December 2022

Contents

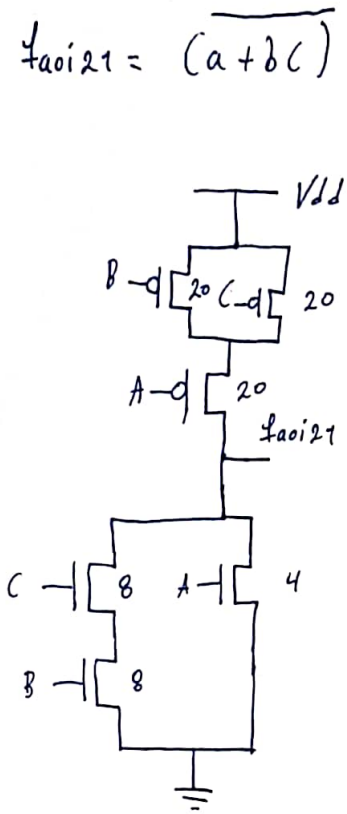
1 Introduction

In this assignment we were tasked to design schematics, stick diagrams and magic layouts for various logic gates. Additionally it was required to convert those layouts into spice circuits and verify their correct operation. Lastly we were assigned to calculate the diffusion capacitances and perform delay analysis for one logic gate.

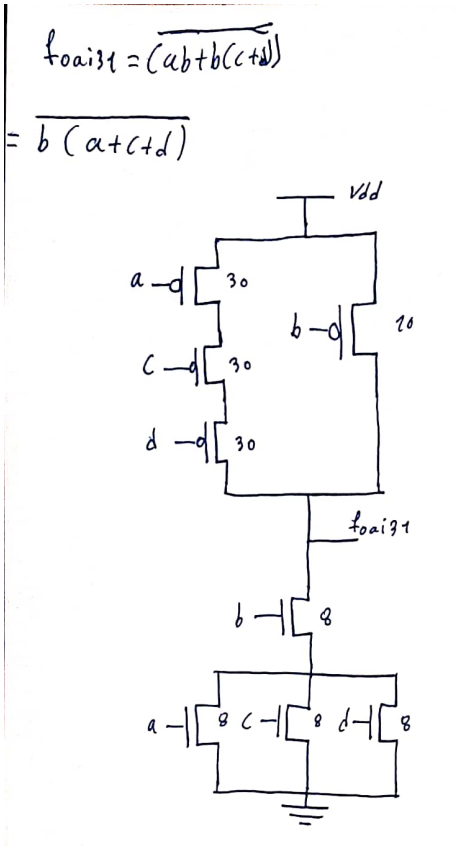
2 Schematic Design with Size Assignment & Stick Diagrams

The logic gates accompanied with their schematics (that include the dimension of each transistor) and their stick diagrams are the following:

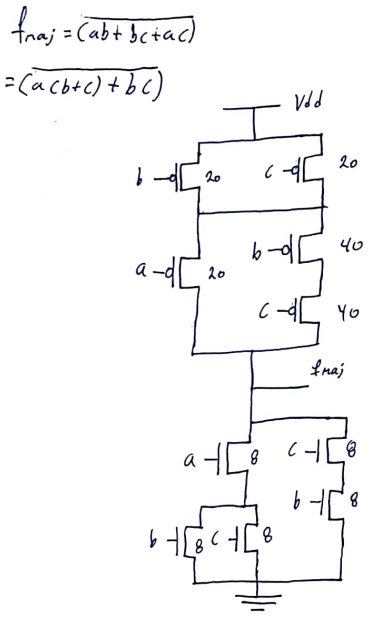
Logic Gate	Function	Schematic	Stick Diagram
f_{aoi21}	(a + bc)'	1a	2a
f_{oai31}	(ab + b(c + d))'	1b	2b
f_{maj}	(ab + bc + ac)'	1c	2c
f_{aoi22}	(ac + bd)'	1d	2d



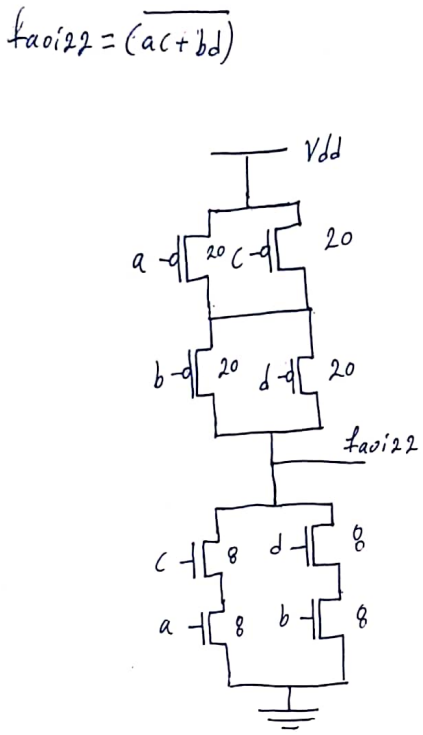
(a) f_{aoi21}



(b) f_{oai31}

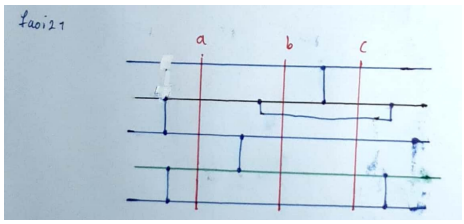


(c) f_{maj}

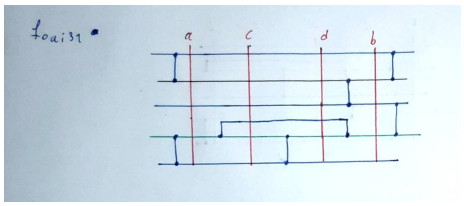


(d) f_{aoi22}

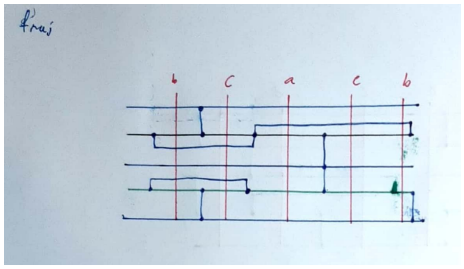
Figure 1: Schematics of Logic Gates



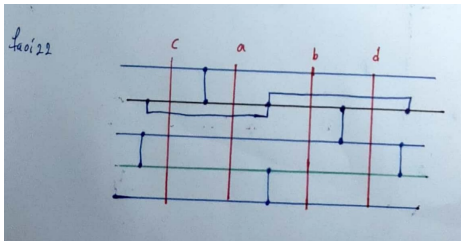
(a) f_{aoi21}



(b) f_{oai31}



(c) f_{maj}

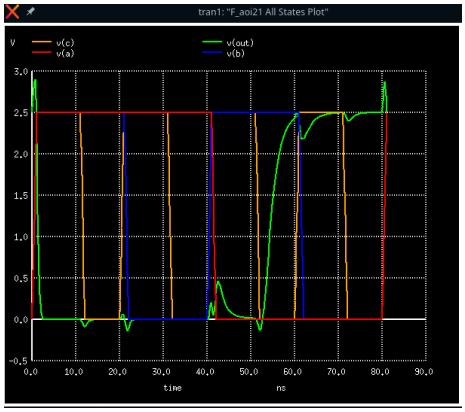


(d) f_{aoi22}

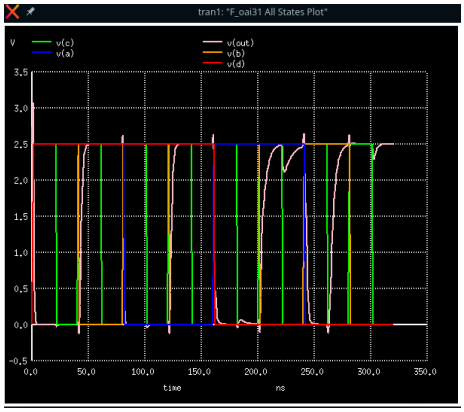
Figure 2: Stick Diagrams of Logic Gates

3 Layout Design Using Magic EDA

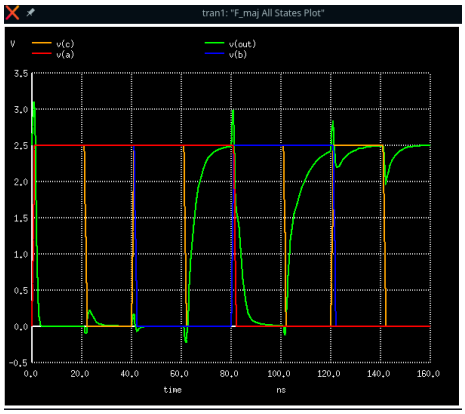
The magic layouts for each logic gate are stored into the respective .mag file. Running simulations for each one we test all the possible inputs making sure the truth table is correct (thus verifying their correct operation) while collecting the resulting plots. Below the plot for each logic gate is presented :



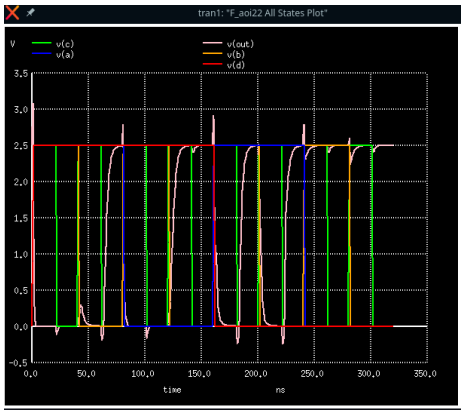
(a) f_{aoi21}



(b) f_{oai31}



(c) f_{maj}



(d) f_{aoi22}

Figure 3: Plots of Logic Gates for Every State

4 Capacitance Analysis of f_{aoi21} Logic Gate

In this part of the assignment it is required to measure the area and the perimeter of every transistor that the f_{aoi21} logic gate's layout has .Afterwards we have to calculate the diffusion capacitance for output $1 \rightarrow 0$ transition. We are able to calculate C_{diff} for each drain/source using the formula $C_{diff} = C_j \cdot K_{\#j} \cdot A_* + C_{jsw} \cdot K_{\#jsw} \cdot P_*$ where # is the type of the transistor and * is the drain or the source which we measure the capacitance. Note that when two transistors have a common drain / source we split it into two equal parts. Having that said below are presented measured figures of the transistor's layout and the corresponding table containing all the essential and required measurements.

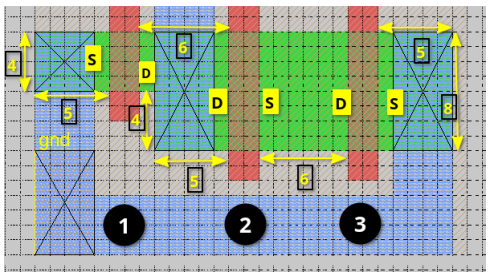


Figure 4: f_{aoi21} NMOS transistors (measured)

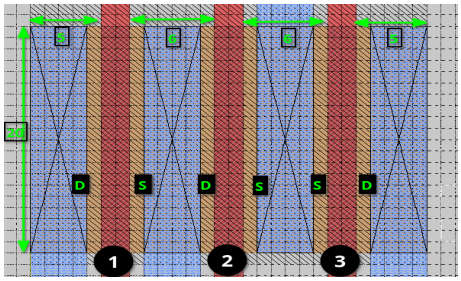


Figure 5: f_{aoi21} PMOS transistors (measured)

Transistor	A_S	A_D	P_S	P_D	Source C_{diff}	Drain C_{diff}	Total C_{diff}
NMOS 1	20	20	14	10	0.65515	0.56975	1.2249
NMOS 2	24	24	6	6	0.5556	0.5556	1.1112
NMOS 3	40	24	18	6	1.0968	0.5556	1.6524
PMOS 1	60	100	6	30	1.66185	3.37175	5.0336
PMOS 2	60	60	6	6	1.66185	1.66185	3.3237
PMOS 3	60	100	6	30	1.66185	3.37175	5.0336

Area is calculated in λ^2, the perimeter in λ and the capacitance in fF for $\lambda = 0.125\mu m$. Also note that the capacitances attached to ground / Vdd are not affecting the delay of the gate in any way.

5 PDN Elmore Delay of f_{aoi21} Logic Gate

In order to calculate the elmore delay we have to choose the longest path of the PDN. We are tasked to drive the capacitance of four identical gates at the output. Magic has exported the capacitance of each input equal to 5.66 fF so the total capacitance of each gate equals to 16.98 fF. Also at the output we have the drain capacitance of PMOS 1 at 3.37115 fF, the drain capacitance of NMOS 1,2 at 0.56975 fF and 0.5556 fF respectively. In total we have $4 \cdot 16.98 + 3.37115 + 0.56975 + 0.5556 = 72.4165fF$ at the output. Between transistor 2,3 we have a $0.5556 + 0.5556 = 1.1112fF$ capacitance. Moreover note that R1 = R2 = 3.25 $k\Omega$ in order to satisfy the assignment's requirement for the PDN to be 6.5 $k\Omega$. The following figure contains a schematic representation :

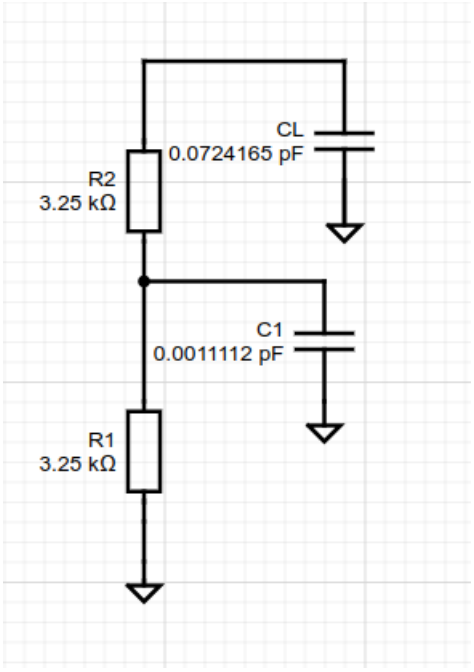


Figure 6: Elmore Representation Schematic

Based on the schematic $\tau = R_1 \cdot (C_1 + C_L) + R_2 \cdot C_L = 4.7431865e^{-10}$ so the elmore delay is $t = 0.69 \cdot \tau = 0.69 \cdot 4.7431865e^{-10} = 3.2727987e^{-10}$ seconds.