VLSI Assignment 1 Report

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November 2022

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1 Introduction

In this assignment we were tasked to create a minimum size CMOS inverter in the VLSI layout tool named Magic. Afterwards we had to verify the inverter's correct operation, measure the propagation delays high-low and low-high and the rise and fall transition times.

2 Implementation

2.1 Magic Layout Design

The Magic software tool provided the means necessary to design the CMOS inverter as shown in figure 1 and extract from it the spice code capable of modeling it.

2.2 Modeling and Measurements

Using the 250nm MOSIS models and the code extracted from magic we were able to model the CMOS inverter and measure the propagation delays high-low and low-high and the rise and fall transition times. The measurements are presented down below and the spice code is given in figure 2 .

- high-to-low = thtl = 3.958399e-10 targ= 2.495840e-09 trig= 2.100000e-09
- low-to-high = tlth = 1.597154e-09 targ= 9.697154e-09 trig= 8.100000e-09
- rise transition = trise = 2.325577e-09 targ= 1.121800e-08 trig= 8.892425e-09
- fall transition = tfall = 5.098153e-10 targ= 2.824262e-09 trig= 2.314447e-09

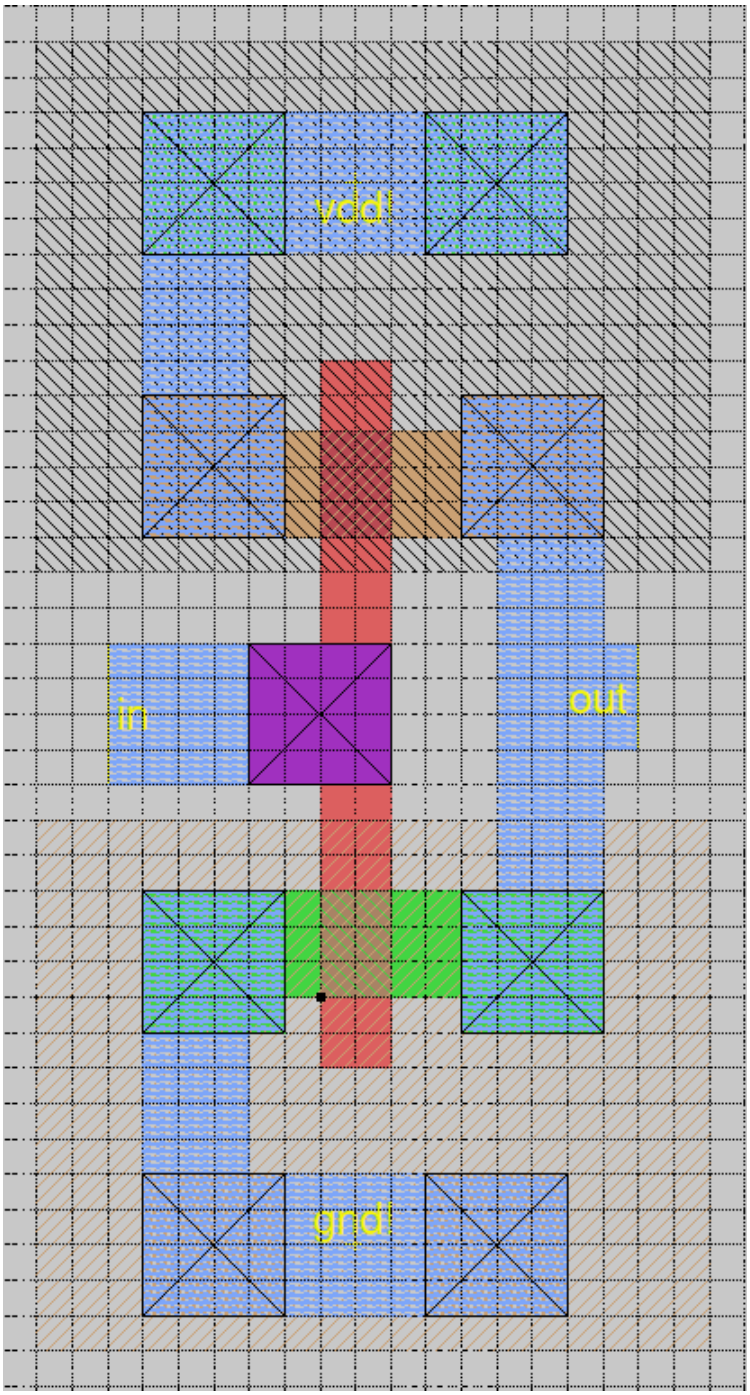

Figure 1: Inverter Layout in Magic

```
*Basic Inverter Measurements
.include 025_models.spice


.option scale=1u

M1000 out in vdd vdd CMOSP w=3 l=2
+  ad=22 pd=20 as=19 ps=18
M1001 out in 0 0 CMOSN w=3 l=2
+  ad=22 pd=20 as=19 ps=18
C0 in 0 3.05fF

vvdd vdd 0 2.5V DC
vin in 0 DC pwl
+0ns  0v
+2ns 0v
+2200ps  2.5v
+8ns  2.5v
+8200ps  0v
+12ns 0v

.tran 10ps 15ns

*high -> low
.meas tran thtl
+ trig v(in) val=1.25 rise=1
+ targ v(out) val=1.25 fall=1

*low -> high
.meas tran tlth
+ trig v(in) val=1.25 fall=1
+ targ v(out) val=1.25 rise=1

*rise transition time
.meas tran trise
+trig v(out) val=0.25 rise=1
+targ v(out) val=2.25 rise=1

*fall transition time
.meas tran tfall
+trig v(out) val=2.25 fall=1
+targ v(out) val=0.25 fall=1

.end
```

Figure 2: Inverter Spice Simulation Code