HLS Assignment 1(KANEKAL KOUSAR[FWC2022063])

Q) Design an 8bit * 8bit multiplier using HLS. There will be two 8bit inputs (use char data type) and one 16bit output (use short data type). Use ap_none interface for the port interfaces. Write an HLS testbench to verify the output of the design. Pass 10 pair of input values to design and collect the output, and display inputs and outputs as part of the testbench. Verify if your design is working using C simulation first. Run HLS synthesis. Now, verify the design again using C/RTL co-simulation. Report your design and tb code, C simulation printed outputs, HLS resource consumption, HLS timing report, and C/RTL cosimulation printed outputs

code:

1)header file

```
#ifndef MUL
#define MUL

#include <stdio.h>
#define N 10

typedef char dinA; //8-bit
typedef char dinB; //8-bit
typedef short dout; //16-bit

#endif
```

2)c code

```
# include "mul2.h"

void mul_8(dinA A,dinB B,dout *C)
                {
      *C=A*B; //multiplier
}
```

3)test-bench

```
# include "mul2.h"
int main(){
      dinA a;
      dinB b;
      dout c;
      int i;
      for (i=0;i<N;i++){
            //creating input data
            a=i+4;
            b=i+5;
            mul_8(a,b,&c);
            printf("%dX%d=%d\n",a,b,c);
      }
}
```

4)simulation report

mul8.c | mul8_tb.c | Synthesis(solution1) | mul_8_csim.log

```
INFO: [SIM 2] *************** CSIM start ***************
INFO: [SIM 4] CSIM will launch GCC as the compiler.
   Compiling(apcc) ../../../mul8_tb.c in debug mode
INFO: [HLS 200-10] Running 'e:/Vivado/2017.4/bin/unwrapped/win64.o/apcc.exe'
INFO: [HLS 200-10] For user 'sumu' on host 'desktop-c9ts4io' (Windows NT_amd64 version 6.2) on Tue Mar 14 19:47:31 +0530 2023
INFO: [HLS 200-10] In directory 'C:/Users/sumu/Desktop/HLS_intro/assignment1/solution1/csim/build'
INFO: [APCC 202-3] Tmp directory is apcc_db
INFO: [APCC 202-1] APCC is done.
   Generating csim.exe
4X5=20
5X6=30
6X7=42
7X8=56
8X9=72
9X10=90
10X11=110
11X12=132
12X13=156
13X14=182
INFO: [SIM 1] CSim done with 0 errors.
INFO: [SIM 3] *************** CSIM finish ***************

```

5)synthesis report

Synthesis Report for 'mul_8'

General Information

Date:	Tue Mar 14 19:51:58 2023
Version:	2017.4 (Build 2086221 on Fri Dec 15 21:13:33 MST 2017)
Project:	assignment1
Solution:	solution1
Product family:	zynq
Target device:	xc7z020clg484-1

Performance Estimates

Timing (ns)

Summary

Clock	Target	Estimated	Uncertainty
ap_clk	10.00	4.17	1.25

Latency (clock cycles)

Summary

Latency		Interval		
min	max	min	max	Type
0	0	0	0	none

Detail

- Instance
- Loop

Utilization Estimates

Summary

Name	BRAM_18K	DSP48E	FF	LUT
DSP	-	-	-	-
Expression	-	0	0	41
FIFO	-	-	-	-
Instance	-	-	-	-
Memory	-	-	-	-
Multiplexer	-	-	-	-
Register	-	-	-	-
Total	0	0	0	41
Available	280	220	106400	53200
Utilization (%)	0	0	0	~0

Detail

- Instance
- DSP48
- Memory
- FIFO
- Expression
- Multiplexer
- Register

Interface

Summary

RTL Ports	Dir	Bits	Protocol	Source Object	C Type
ap_start	in	1	ap_ctrl_hs	mul_8	return value
ap_done	out	1	ap_ctrl_hs	mul_8	return value
ap_idle	out	1	ap_ctrl_hs	mul_8	return value
ap_ready	out	1	ap_ctrl_hs	mul_8	return value
A	in	8	ap_none	A	scalar
B	in	8	ap_none	B	scalar
C	out	16	ap_none	C	pointer

Export the report(.html) using the Export Wizard

Open Analysis Perspective Analysis Perspective

6)co-simulation output and report

Cosimulation Report for 'mul_8'

Result

		Latency			Interval		
RTL	Status	min	avg	max	min	avg	max
VHDL	NA	NA	NA	NA	NA	NA	NA
Verilog	Pass	0	0	0	0	0	0

Export the report(.html) using the Export Wizard

```
INFO: [Common 17-206] Exiting xsim at Wed Mar 15 14:14:39 2023...
INFO: [COSIM 212-316] Starting C post checking ...
4X5=20
5X6=30
6X7=42
7X8=56
8X9=72
9X10=90
10X11=110
11X12=132
12X13=156
13X14=182
INFO: [COSIM 212-1000] *** C/RTL co-simulation finished: PASS ***
INFO: [COSIM 212-210] Design is translated to an combinational logic. II and Latency
will be marked as all 0.
Finished C/RTL cosimulation.
```