Synthesis Report for 'mul_8'

General Information

Date: Tue Mar 14 19:32:41 2023
Version: 2017.4 (Build 2086221 on Fri Dec 15 21:13:33 MST 2017)
Project: assignment1
Solution: solution1
Product family: zynq
Target device: xc7z020clg484-1

Performance Estimates

- **Timing (ns)**
  - **Summary**

Clock	Target	Estimated	Uncertainty
ap_clk	10.00	4.17	1.25

- **Latency (clock cycles)**
  - **Summary**

Latency		Interval		Type
min	max	min	max	
0	0	0	0	none

  - **Detail**
    - **Instance**

N/A

    - **Loop**

N/A

Utilization Estimates

- **Summary**

Name	BRAM_18K	DSP48E	FF	LUT
DSP	-	-	-	-
Expression	-	0	0	41
FIFO	-	-	-	-

Instance	-	-	-	-
Memory	-	-	-	-
Multiplexer	-	-	-	-
Register	-	-	-	-
Total	0	0	0	41
Available	280	220	106400	53200
Utilization (%)	0	0	0	~0

- **Detail**
  - **Instance**

    N/A
  - **DSP48**

    N/A
  - **Memory**

    N/A
  - **FIFO**

    N/A
  - **Expression**

Variable Name	Operation	DSP48E	FF	LUT	Bitwidth P0	Bitwidth P1
C	*	0	0	41	8	8
Total	1	0	0	41	8	8

  - **Multiplexer**

    N/A
  - **Register**

    N/A

Interface

- **Summary**

RTL Ports	Dir	Bits	Protocol	Source Object	C Type
ap_start	in	1	ap_ctrl_hs	mul_8	return value

ap_done	out	1	ap_ctrl_hs	mul_8	return value
ap_idle	out	1	ap_ctrl_hs	mul_8	return value
ap_ready	out	1	ap_ctrl_hs	mul_8	return value
A	in	8	ap_none	A	scalar
B	in	8	ap_none	B	scalar
C	out	16	ap_none	C	pointer