LinoSPAD Camera Factsheet

Samuel Burri

samuel.burri@epfl.ch

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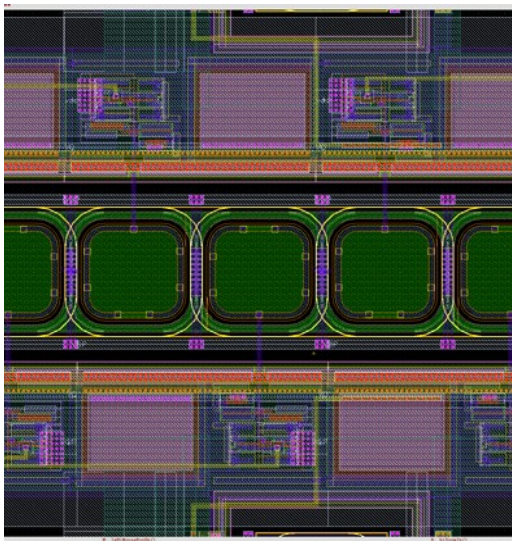
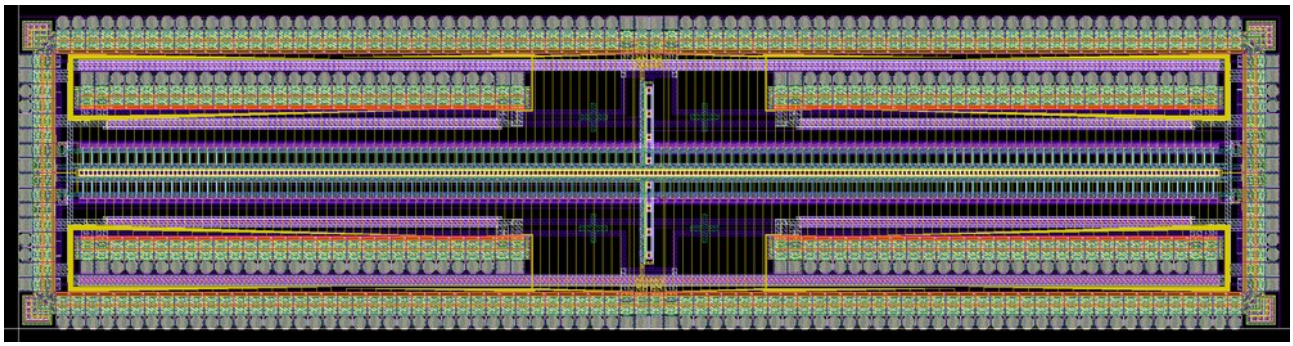
ÉCOLE POLYTECHNIQUE
FÉDÉRALE DE LAUSANNE

Sensor specification:

Chip size:	6.8 x 1.68 mm²
Technology:	AMS HV 0.35µm 4M
Resolution:	256 x 1 (+8)
Pixel pitch:	24 µm
Sensitive area diameter:	~17.3 µm
Fill factor:	~41%
Dead time:	Est. 100 ns
Median DCR @ 20°C:	~2.5 kHz
Target wavelength:	400-850 nm
Light incidence:	< 45° from normal



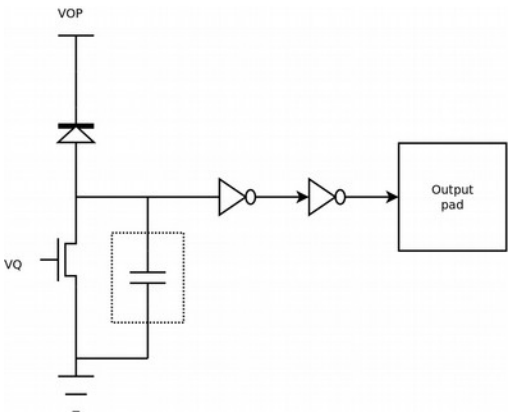
Close-up of SPADs



Full layout

LinoSPAD is a simple sensor with a line of SPADs implemented in a standard high-voltage CMOS process. (AMS 0.35µm)

The chip size is 6.8 x 1.68 mm² and there are 256 SPADs with a pitch of 24µm. A total of eight alignment markers are distributed around the center of symmetry of the chip. There is a secondary line of 8 detectors with a pitch of 127µm vertically. The SPADs are rounded rectangles with an approximate fill factor of 41% in the line. All SPADs connect directly to outputs as seen in the pixel schematic.



Pixel schematic

Camera mainboard:

FPGA:	Xilinx Spartan 6 LX 150 (FGG676)
Interfaces:	• Standard Xilinx JTAG • Cypress FX3 USB 3.0 transceiver (tested over 250 MB/s between FPGA and PC)
Memories:	• S25FL128S 128 Mbit SPI flash for FPGA configuration (Xilinx Impact supported) • M25P16 SPI flash for FX3 configuration
Power:	5V main power input, two dual 8A regulators for 1.2V, 1.8V, 2.5V and 3.3V on board. FPGA I/O voltages jumper selectable.
FPGA Clocks:	48 MHz oscillator and 100 MHz clock from FX3. 2 SMA on 2.5V I/O and 2 on 1.8V – 3.3V I/O. (Differential input possible.)
Extension:	FMC daughter card connector on the back to connect to other Xilinx FPGA boards.
Sensor I/O:	296 FPGA I/O and 4 voltages on two SAMTEC GFZ 40x10 connector arrays. I/O voltage selectable between 1.8V and 3.3V. Three voltages brought in through screw terminal.

Camera mainboard

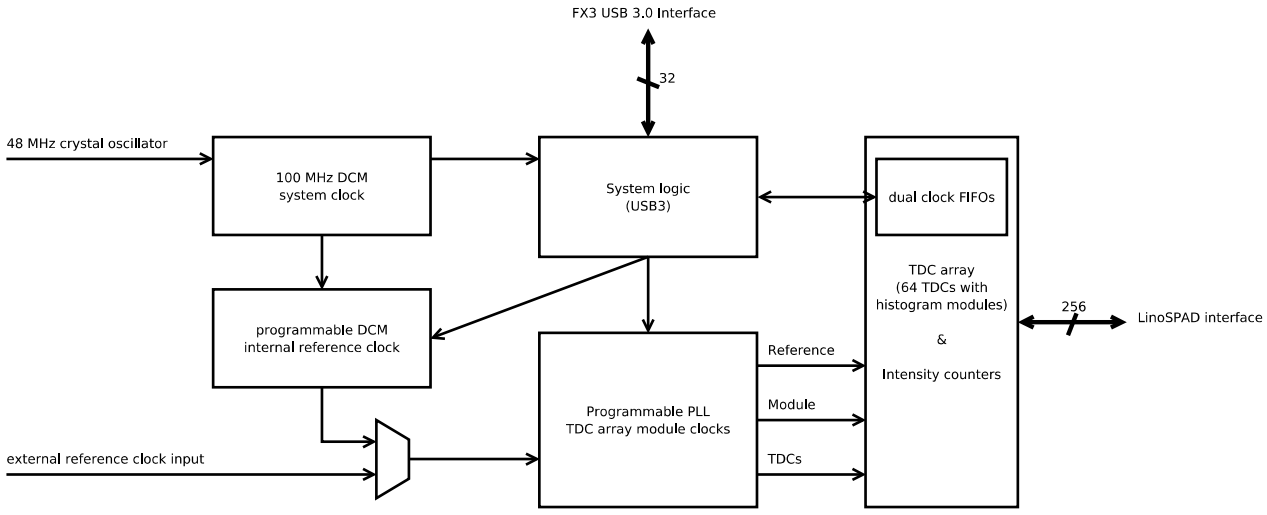
Standard firmware:

The FX3 USB 3.0 transceiver is used as transparent FIFO between the computer and the FPGA. Transfer speeds over 250 MB/s are reached with the current firmware-software combination.

The FPGA firmware as shown in the schematic below implements 64 TDCs with histogram modules that are assigned to the pixels in time-division multiplexing mode. Intensity counters are connected in parallel and always active on all pixels.

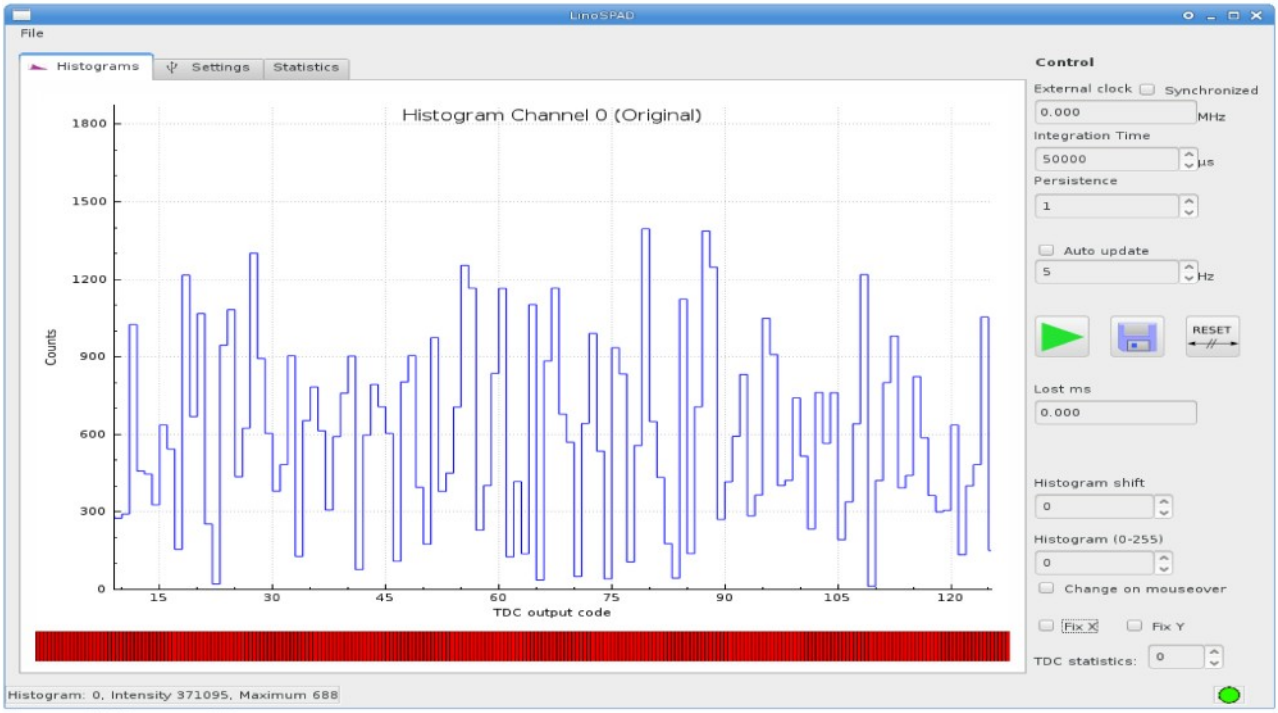
Photon event are accumulated in histograms referenced to an external signal. The firmware can transmit up to 200k histograms of 1024x16bit per second (400 MB/s) though generally a data-rate about 200 MB/s is sustained permanently provided that the computer can handle the data. The histograms can be processed during readout to reduce non-linearity from the FPGA delay line implementation.

For the reference signal any signal recognized by the FPGA can be used or it can be generated by the FPGA. The standard firmware supports reference frequencies of 20, 25, 33, 40, 50, 66, 80 and 100 MHz.



Standard firmware schematic

Software:



Sensor GUI using QT

The software used to characterize the chip is written in C++ using the QT GUI libraries. For the USB communication libusb-1.0 is used. The communication with the FPGA is abstracted to a stream of 32 bit words. Upon this stream a high-level protocol with 4 bit addresses is added to send commands to different modules inside the FPGA. The host computer is always the master of the communication and requests data from the camera.

The software presents the configuration options of the camera in a user-friendly way and implements simple statistics functions to make use of the post-processing pipeline in the FPGA firmware. It is expected that custom data acquisition sequences and output functions need to be added for future applications.

To use our software as is and make modifications a computer running a recent Linux distribution is required.

List of equipment:

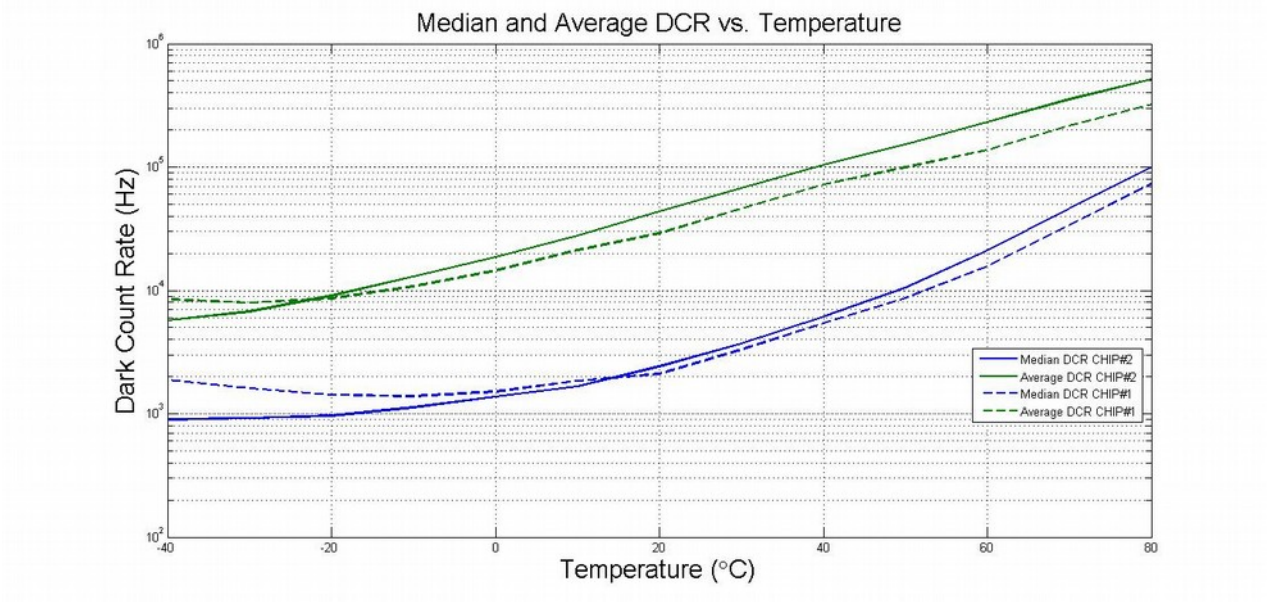
The following is necessary to use the LinoSPAD camera:

- LinoSPAD camera assembly consisting of mainboard, camera and board-to-board connectors
- Linux computer with USB 3.0 and micro USB 3.0 cable
- Xilinx JTAG programmer
- Dual lab power supply: 0-3V / 1A and 0-30V / 1A
- Standard IEC power cable for FPGA and cables from the lab supply to the screw terminal
- Any cables and level shifters necessary to provide or receive a reference clock to or from the FPGA
- Any optical components

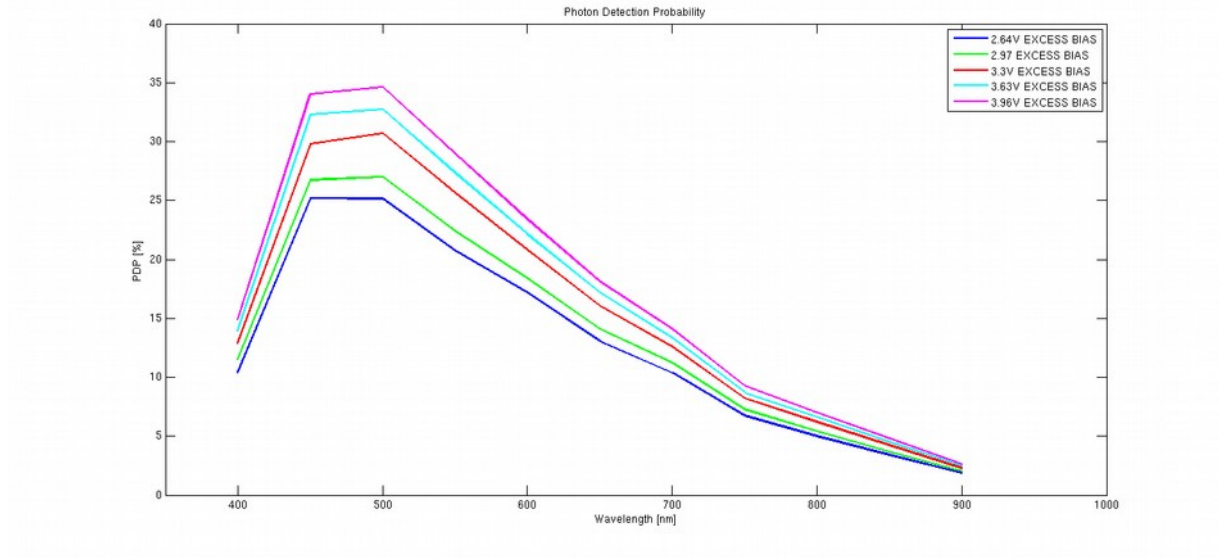
The camera assembly as seen on the title is provided with a 3D-printed frame and tube on the chip. The tube diameter is 30mm and the camera can be supported by a tube-holder for this size. A hardware manual with more mechanical (and electronic) details is available.

Performance:

The LinoSPAD chip has been characterized for noise (DCR) and sensitivity (PDP) as shown in the following plots.

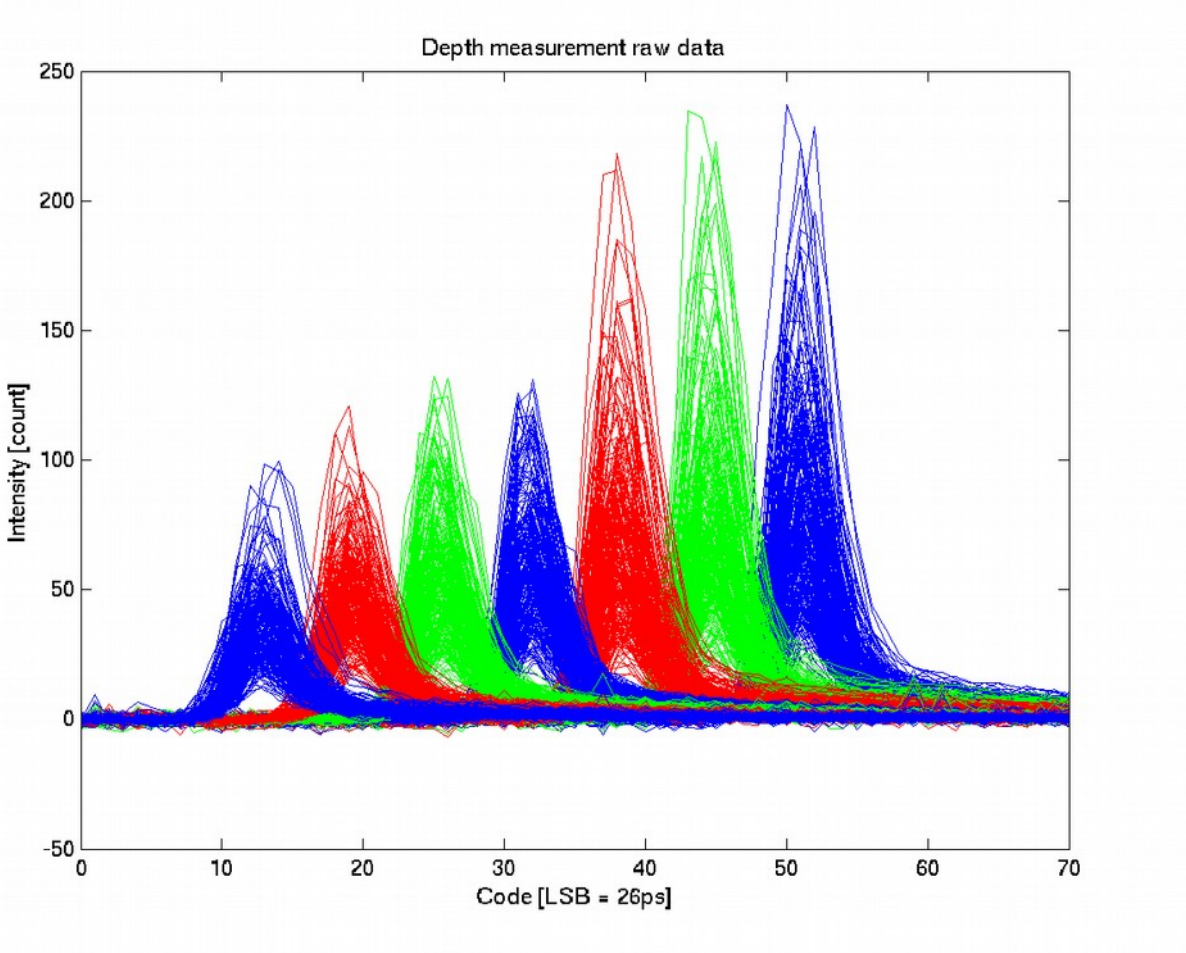


Median and average dark count rate for two tested chips.



Photon detection probability versus wavelength for different excess bias voltages.

Furthermore the timing performance for the camera is being characterized. The result below is a summary of the current state. It is a series of measurements from a pico-second laser-pulse reflected on a target moved by steps of 25mm. This is the data delivered from the FPGA after calibration has been performed. Only the different base-lines of the curves due to different noise on the pixels has been aligned on the computer. A simple operation that could be offloaded to the FPGA as well at some point.



Sensor data (after FPGA filter) for time-of-flight with a reflective target.

From the picture we see that all pixels are working and are usable for time-resolved measurements regardless of their individual DCR.