Hardware Characterization

Required measurements

http://ra.ziti.uni-heidelberg.de/pages/student_work/seminar/ws0304/richard_sohnius/praesentation.pdf

Transition times. Characterized and measured between 30 % and 70 %. Standardized reporting between 10 % and 90 %.

- area
- power
- timing contstraints (setup/Hold time, recovery/removal time)
- propagation delay time
- input capacitance

Power:

- Dynamic power (switching power)
- Static power (leakage power)
- Passive power (internal power. power used by sequential cells when inputs change without output change)

Delay:

https://www.csee.umbc.edu/~cpatel2/links/641/slides/lect05_LIB.pdf

- sum of intrinsic delay, slope delay, transition delay and connect delay
- intrinsic delay is fixed value independent of surroundings
- slope delay is produced by the slew of the input signal
- transition delay is the time required to change the capacitance of the next stage input pins
- connect delay is delay caused by the wire between output and next input pins

Delay model of Liberate (.lib) is the CMOS Non-Linear Delay Model.

- Delay and transition time are modeled as function of Input slew and Output load
- Data is stored in a 2D LUT (look-up table)
- Intermediate values are interpolated
- Data points are usually not equidistant

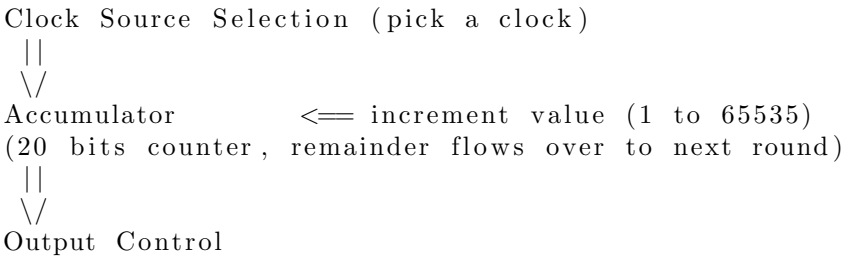
solutions

feedback loop with a counter?

Testbenches

Numerically Controlled Oscillator

Numerically controlled oscillator


Clock Source Selection (pick a clock)
||
\/
Accumulator <== increment value (1 to 65535)
(20 bits counter, remainder flows over to next round)
||
\/
Output Control