Hardware Characterization

Required measurements

http://ra.ziti.uni-heidelberg.de/pages/student_work/seminar/ws0304/richard_sohnius/praesentation.pdf

Transition times. Characterized and measured between 30 % and 70 %. Standardized reporting between 10 % and 90 %.

- area
- power
- timing contstraints (setup/Hold time, recovery/removal time)
- propagation delay time
- input capacitance

Power:

- Dynamic power (switching power)
- Static power (leakage power)
- Passive power (internal power. power used by sequential cells when inputs change without output change)

Delay:

https://www.csee.umbc.edu/~cpatel2/links/641/slides/lect05_LIB.pdf

- sum of intrinsic delay, slope delay, transition delay and connect delay
- intrinsic delay is fixed value independent of surroundings
- slope delay is produced by the slew of the input signal
- transition delay is the time required to change the capacitance of the next stage input pins
- connect delay is delay caused by the wire between output and next input pins

Delay model of Liberate (.lib) is the CMOS Non-Linear Delay Model.

- Delay and transition time are modeled as function of Input slew and Output load
- Data is stored in a 2D LUT (look-up table)
- Intermediate values are interpolated
- Data points are usually not equidistant

solutions

feedback loop with a counter?

Solutions

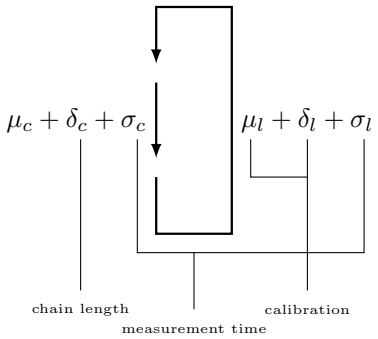


Figure 1: math

$$t_{meas} = \frac{1}{acc_{\%}} \cdot T = \frac{1}{acc_{\%}} \cdot (noC \cdot \tau_C + \tau_x)$$
$$t_{meas} = \frac{\tau_C}{acc_t} \cdot T = \frac{\tau_C}{acc_t} \cdot (noC \cdot \tau_C + \tau_x)$$

$$\text{Count} = 200 \qquad \text{for } t_{meas} = 1\,\mu s$$
$$T = \frac{t_{meas}}{\text{Count}} = 5\,ns$$
$$\tau_C = \frac{T - \tau_x}{noC} = 37.5\,ps \qquad \text{for } tau_x = 200\,ps, noC = 128$$

Table 1: Requirements for $1\,ps$ resolution

ring size	1	1	8	8	64	64	512	512
component delay	$50\,ps$	$100\,ps$	$50\,ps$	$100\,ps$	$50\,ps$	$100\,ps$	$50\,ps$	$100\,ps$
Period (T)	$50\,ps$	$100\,ps$	$400\,ps$	$800\,ps$	$3.2\,ns$	$6.4\,ns$	$25.6\,ns$	$51.2\,ns$
max counts	50	100	50	100	50	100	50	100
measurement time (t_{meas})	$2.5\,ns$	$10\,ns$	$20\,ns$	$80\,ns$	$160\,ns$	$640\,ns$	$1.28\,\mu s$	$5.12\,\mu s$

for N the number of elements in the Ring Oscillator

$$\Delta t_c = \mathcal{N}(\mu_c, \sigma_c^2)$$
$$\Delta t_{RO} = \mathcal{N}(N\mu_c, \sqrt{N}\sigma_c^2)$$
$$\frac{\Delta t_{RO}}{N} = \mathcal{N}(\mu_c, \frac{\sigma_c^2}{\sqrt{N}})$$

for N the number of elements in the Ring Oscillator
for C the number of counts

$$
\begin{aligned}
t_c &= \mathcal{N}(\Delta t_c, \sigma_d^2) \\
t_{RO} &= \mathcal{N}(C\Delta t_{RO}, \sqrt{NC}\sigma_d^2) \\
\frac{t_{RO}}{NC} &= \mathcal{N}(\frac{\Delta t_{RO}}{N}, \frac{\sigma_d^2}{\sqrt{NC}})
\end{aligned}
$$

Testbenches

Numerically Controlled Oscillator

Control when the accumulator flows over. Needs a very fast counter. Overflow amount gets carried over to next cycle.

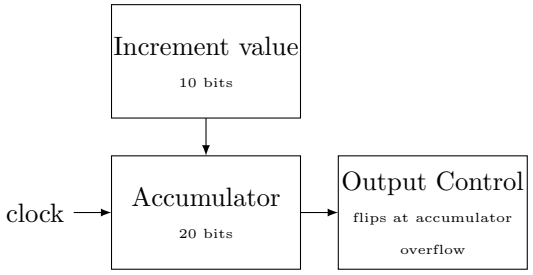


Figure 2: NCO

Time to Digital Converter (TDC)

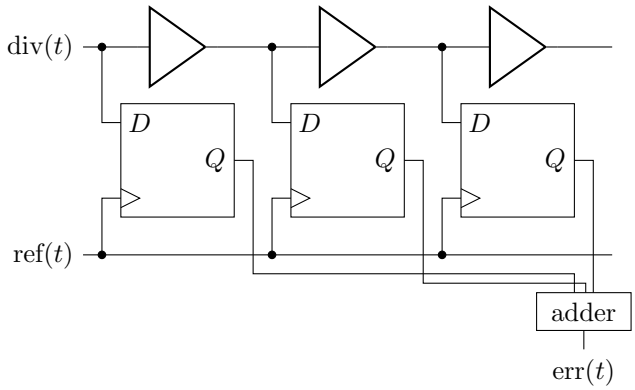


Figure 3: TDC

Phase Detector

The phase detector produces a 1 between the time the reference signal switches to a one, and the divider switches to a one.

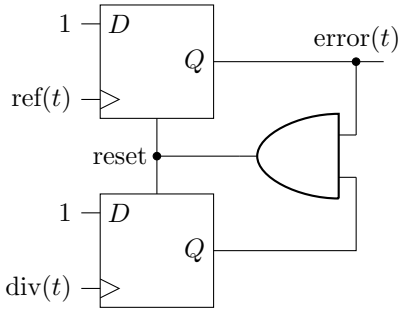


Figure 4: Phase detector

Digitally controlled oscillator

Uses digitally controlled switches to change the output load

Grey Counter

8-bit grey counter designed with Alex

Digital Divider

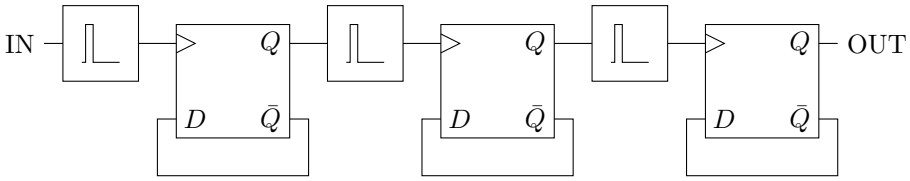


Figure 5: Digital divider

4-bit Multiplexer and Demultiplexer

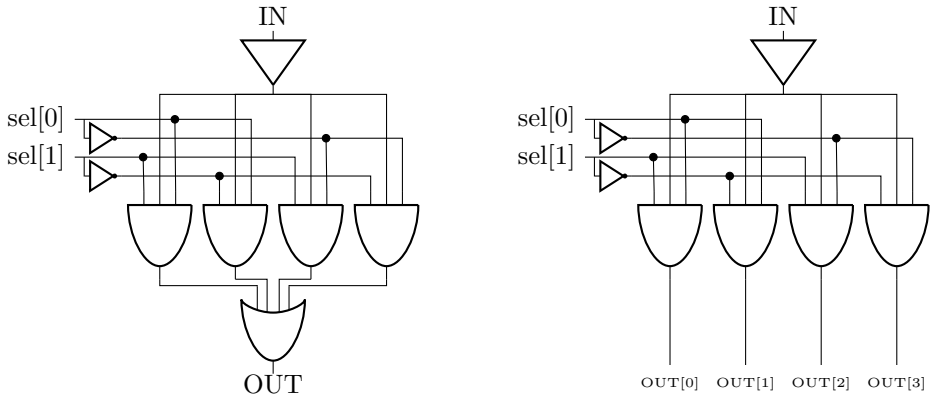


Figure 6: MUX

Changable Ring Oscillator

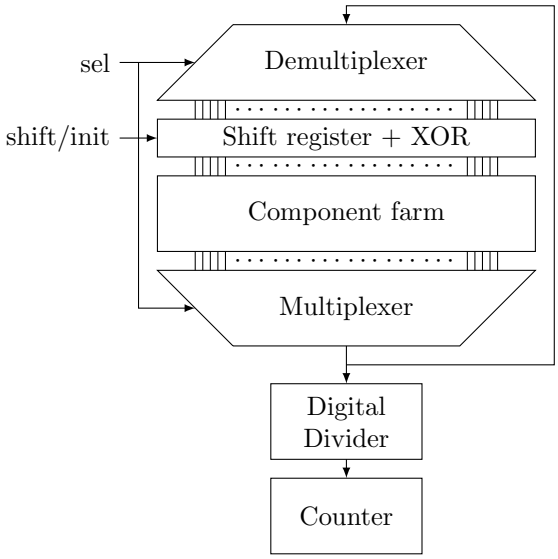


Figure 7: Changable Ring Oscillator

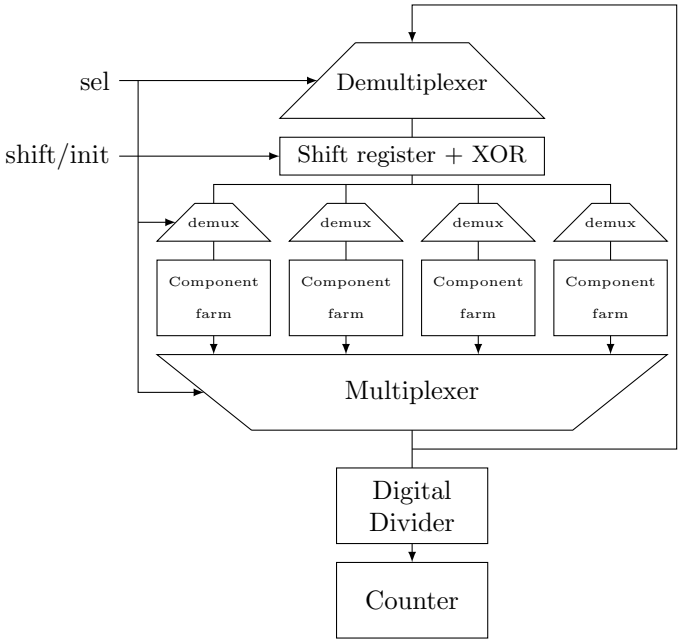


Figure 8: Changable Ring Oscillator 2

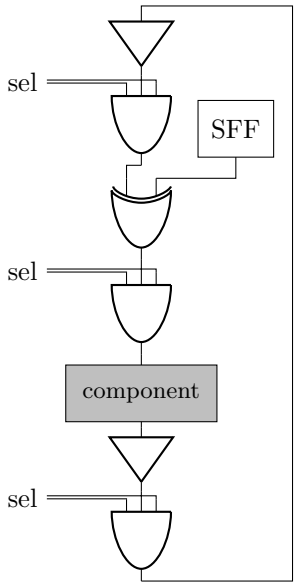


Figure 9: critical path of dynamic ring oscillator

counter with scan chain

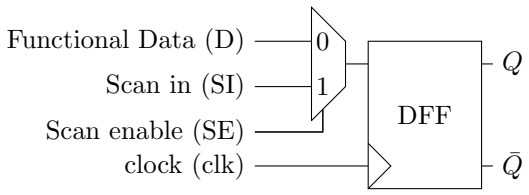


Figure 10: Scan Flipflop (SFF)

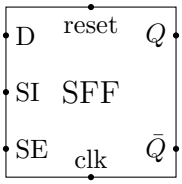


Figure 11: Symbol Scan Flipflop (SFF)

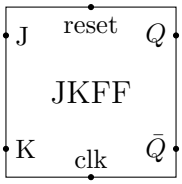


Figure 12: Symbol JK-Flipflop (JKFF)

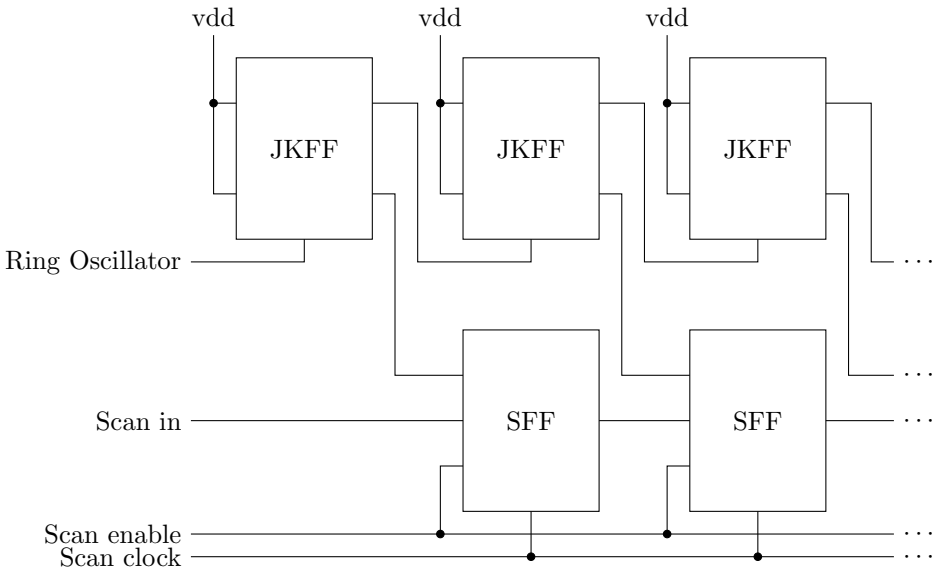


Figure 13: Counter with Shift register

SFF = 10 gates
JKFF = 10 gates

example: 16 gates + swappable ring oscillator, $1\,ps$ resolution

$$\text{ring size} = 16 + 8 = 24\text{gates} \tag{1}$$
$$T = 1.2\,ns \tag{2}$$
$$\text{counts} = 1200 \tag{3}$$
$$t_{meas} = 1.44\,\mu s \tag{4}$$
$$bits = 11 \tag{5}$$
$$gates = 11 \cdot 20 + 41 + 16 \cdot 16 = 517 \tag{6}$$

separate rings

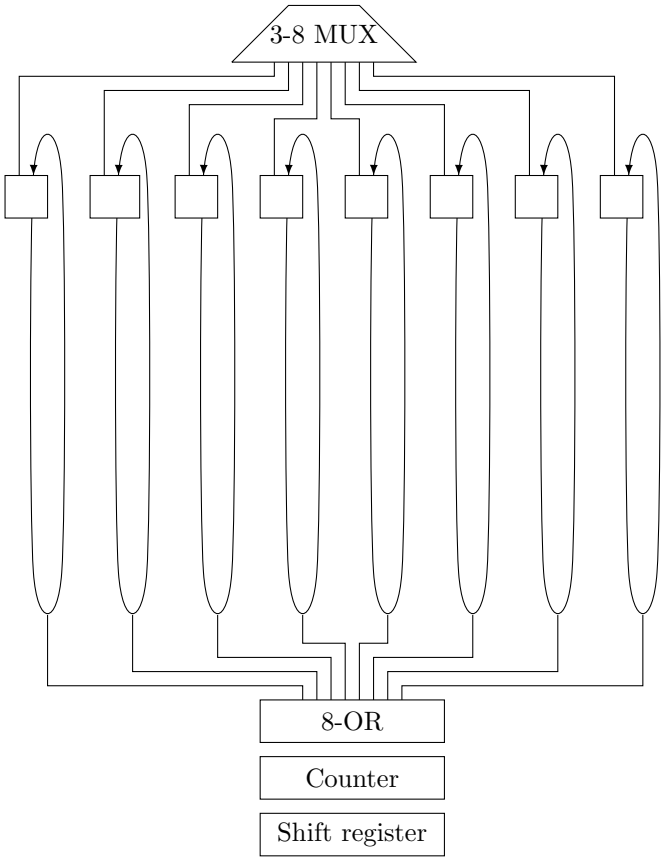


Figure 14: solution with multiple rings and a single counter

Optimized seperate ring design

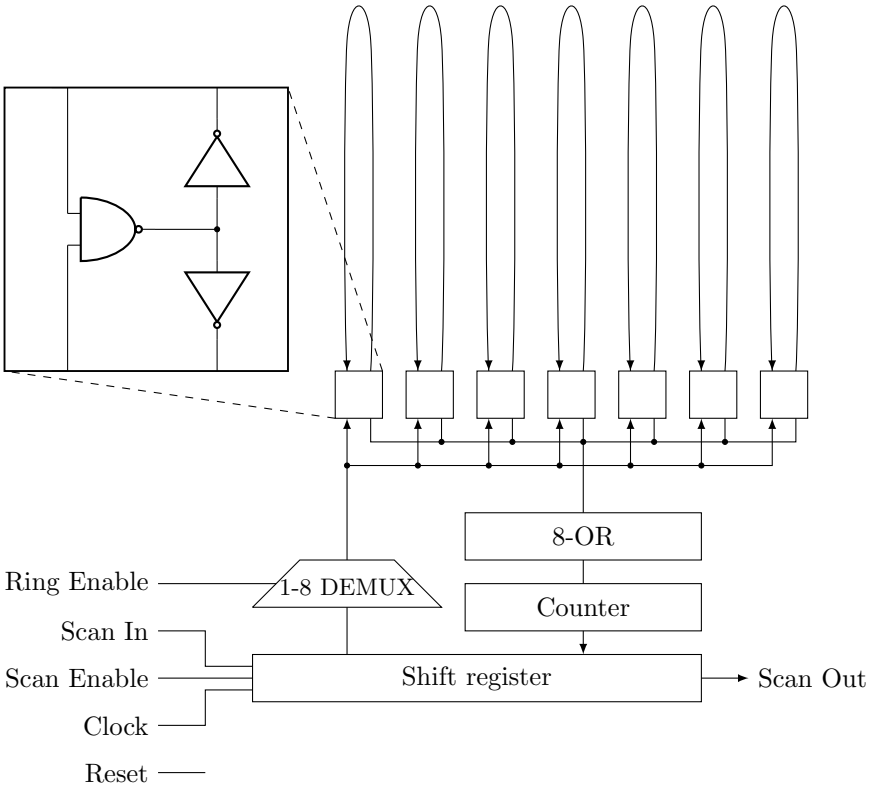


Figure 15: optimized seperate ring design

Sequential characterization

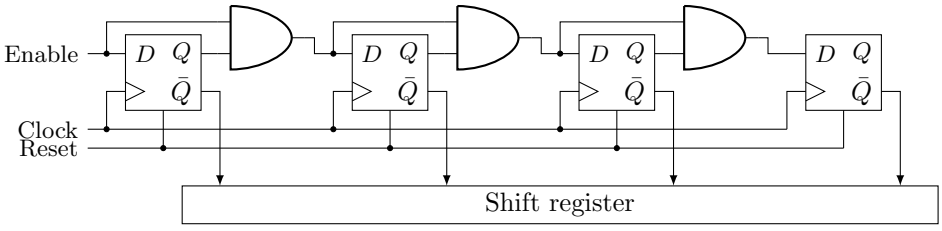


Figure 16: sequential characvterization design

Scan asynchronous counter

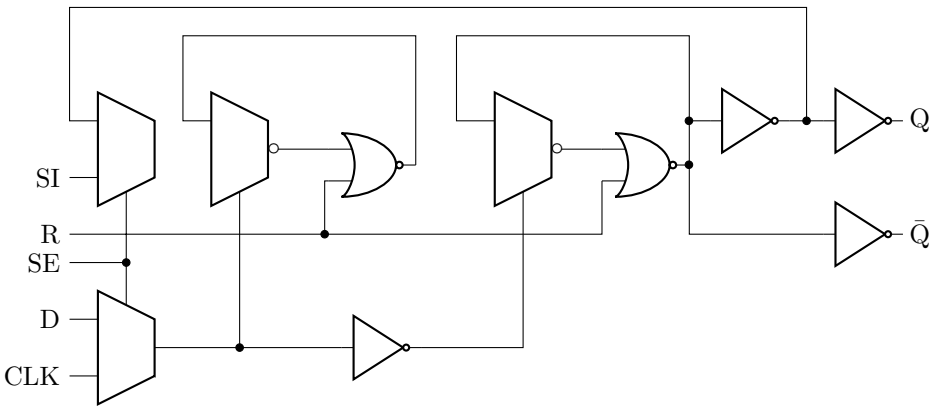


Figure 17: Block of a scan asynchronous counter

Examples of ring components

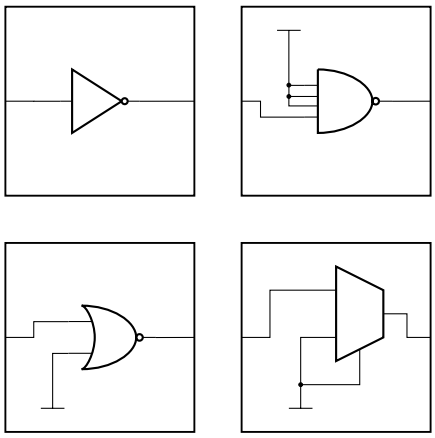
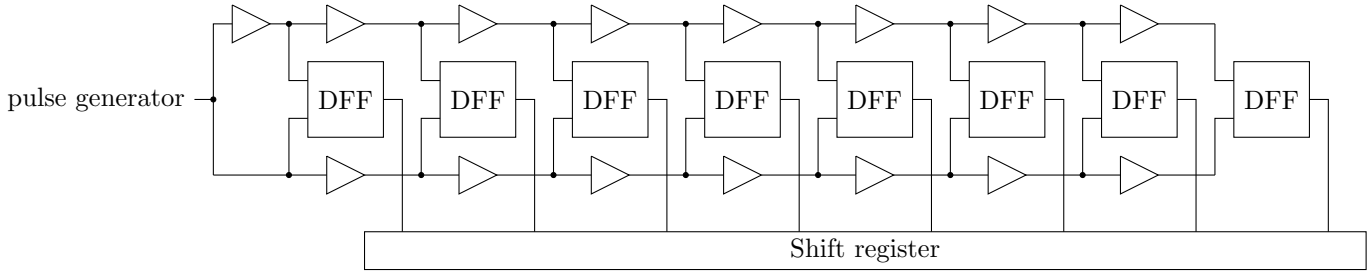


Figure 18: examples of ring components



Elaborated sequential characterization design

Indian concept for setup/hold time characterization

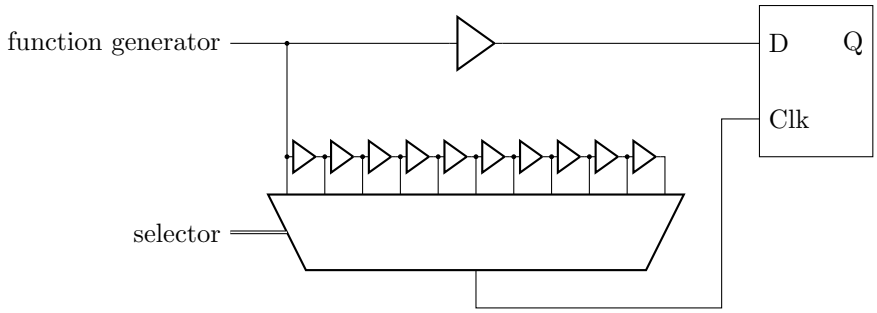
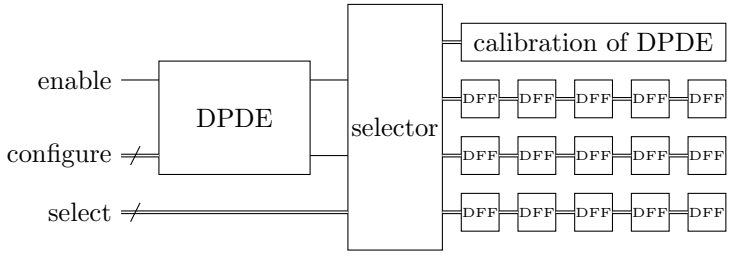
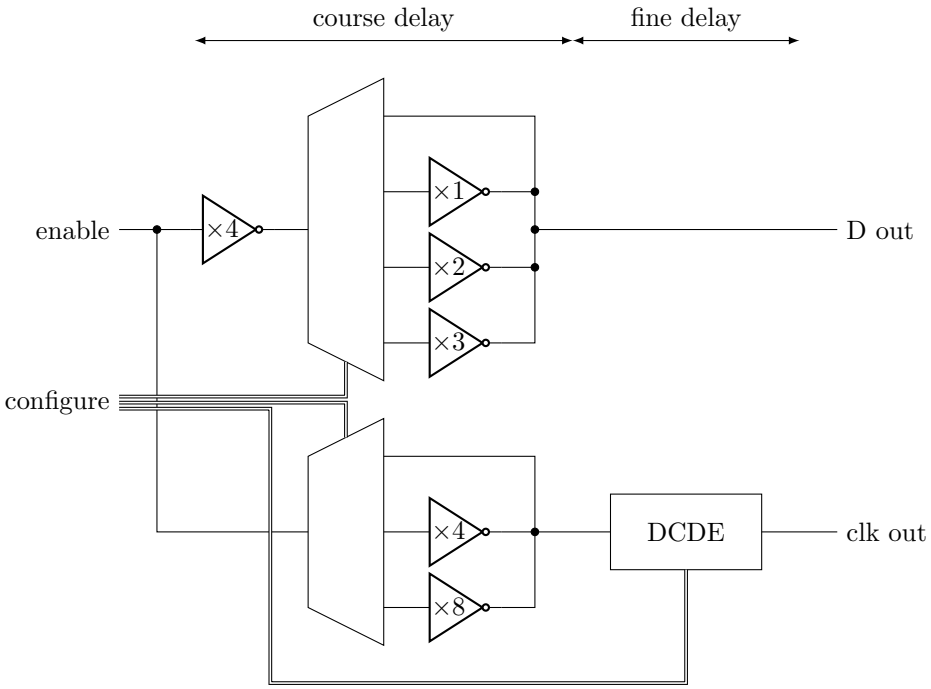


Figure 19: Setup/hold time characterization concept

Sequential characterization proposal



DPDE


course delay
fine delay
enable
×4
×1
×2
×3
D out
configure
×4
×8
DCDE
clk out