On-Silicon Testbench to Validate Soft Logic Cell Libraries

by:

Hardware for Dynamic Quantum Computing

By: Colm A. Ryan

This paper derscribes hardware, gateware and software used for dynamic quantum information processing experiments on superconducting qubits. There is both a forward and backward channel. Most of the controls are done through FPGA's.

An experimental Micro architecture for a Superconducting Quantum computer

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Goal: build a flexible control micro architecture (QuMA) supporting quantum-classical mixed code for a superconducting quantum processor. Three main elements

1. a codeword-based event control scheme
2. queue-based precise event timing control
3. a flexible multilevel instruction decoding mechanism for control

Also a set of quantum microinstructions (QuMIS) is proposed to allow flexible control of quantum operations with precise timing.

The concept is successfully implemented on an FPGA that controls transmon qubits.

Host processor fetches binary instructions for the quantum coprocessor.

The codeword triggered operations is based on a simple lookup table (with binary addresses), to let short binary codes represent elementary quantum operations. Changing the lookup table would leave the overall structure intact while maybe improving and capitalizing on future research.

The queue based timing control is there to merge the classical and quantum parts of the system. The classical side uses an as fast as possible approach, while the quantum side uses deterministic, perfectly timed commands based on the contents of the queue.

An instruction set is proposed for the execution controller, the Quantum Microinstruction buffer (QMB), the Micro-operations and the Measurement discrimination unit.

Example for physical CNOT

```
1 Pulse {qt}, Ym90
2 Wait 4
3 Pulse {qt, qc}, CZ
4 Wait 8
5 Pulse {qt}, Y90
6 Wait 4
```