Hardware Characterization

Required measurements

http://ra.ziti.uni-heidelberg.de/pages/student_work/seminar/ws0304/richard_sohnius/praesentation.pdf

Transition times. Characterized and measured between 30 % and 70 %. Standardized reporting between 10 % and 90 %.

- area
- power
- timing contstraints (setup/Hold time, recovery/removal time)
- propagation delay time
- input capacitance

Power:

- Dynamic power (switching power)
- Static power (leakage power)
- Passive power (internal power. power used by sequential cells when inputs change without output change)

Delay:

https://www.csee.umbc.edu/~cpatel2/links/641/slides/lect05_LIB.pdf

- sum of intrinsic delay, slope delay, transition delay and connect delay
- intrinsic delay is fixed value independent of surroundings
- slope delay is produced by the slew of the input signal
- transition delay is the time required to change the capacitance of the next stage input pins
- connect delay is delay caused by the wire between output and next input pins

Delay model of Liberate (.lib) is the CMOS Non-Linear Delay Model.

- Delay and transition time are modeled as function of Input slew and Output load
- Data is stored in a 2D LUT (look-up table)
- Intermediate values are interpolated
- Data points are usually not equidistant

solutions

feedback loop with a counter?

Solutions

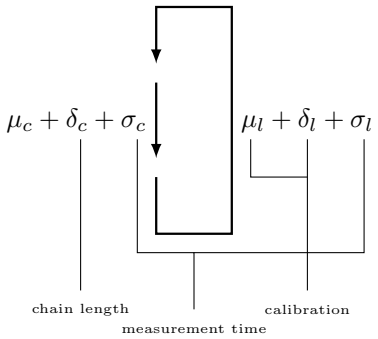

Figure 1: math

$$\sigma_{tot} = \sqrt{\frac{\sigma_{c,s}^2}{\text{components}} + \frac{\sigma_{c,d}^2 + \sigma_{l,d}^2}{\text{counts}}}$$

$$\begin{aligned} LSB &= \frac{T}{\text{counts}} \\ t_{meas} &= T \cdot \text{counts} = \frac{T^2}{LSB} \\ bits &= \lceil \log_2(\text{counts}) \rceil \end{aligned}$$

for 50 components with $\approx 50\,ps$ delay, and $1\,ps$ resolution requirement

$$\begin{aligned} T &= 2500\,ps \\ \text{counts} &= 2500 \\ t_{meas} &= 6.25\,\mu s \\ bits &= 12 \end{aligned}$$

for 10 components with $\approx 50\,ps$ delay, and $1\,ps$ resolution requirement

$$\begin{aligned} T &= 500\,ps \\ \text{counts} &= 500 \\ t_{meas} &= 250\,ns \\ bits &= 9 \end{aligned}$$

Testbenches

Numerically Controlled Oscillator

Control when the accumulator flows over. Needs a very fast counter. Overflow amount gets carried over to next cycle.

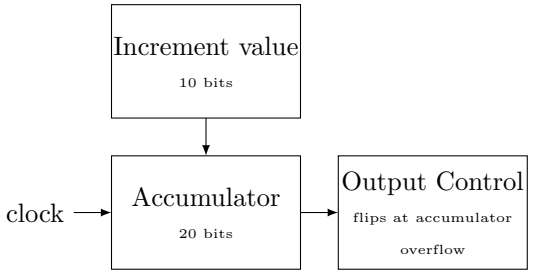

Figure 2: NCO

Time to Digital Converter (TDC)

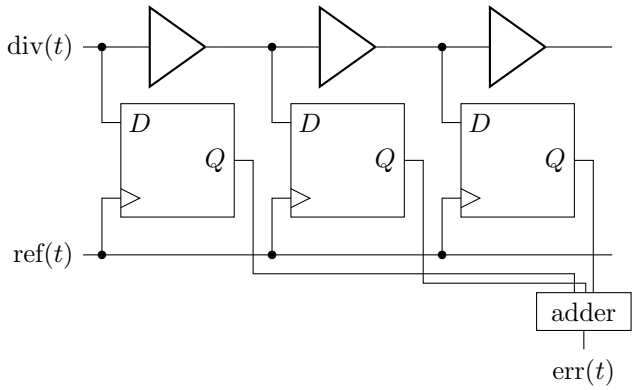

Figure 3: TDC

Phase Detector

The phase detector produces a 1 between the time the reference signal switches to a one, and the divider switches to a one.

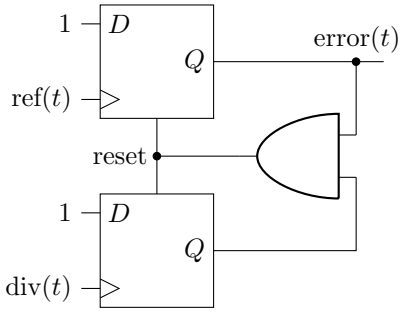

Figure 4: Phase detector

Digitally controlled oscillator

Uses digitally controlled switches to change the output load

Grey Counter

8-bit grey counter designed with Alex

Digital Divider

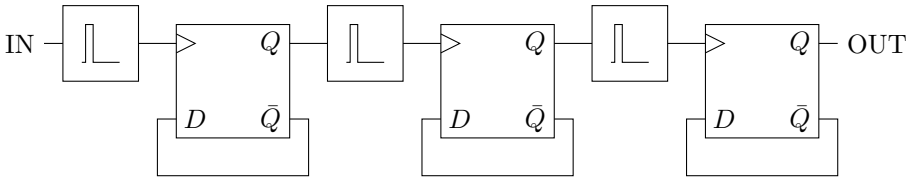

Figure 5: Digital divider

4-bit Multiplexer and Demultiplexer

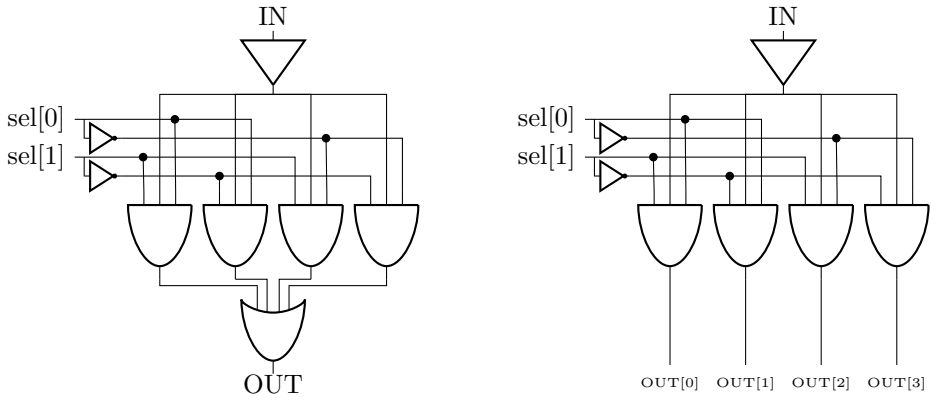

Figure 6: MUX

Changable Ring Oscillator

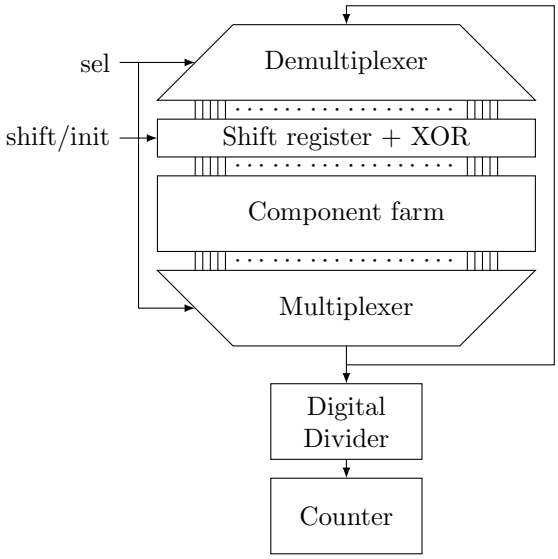

Figure 7: Changable Ring Oscillator

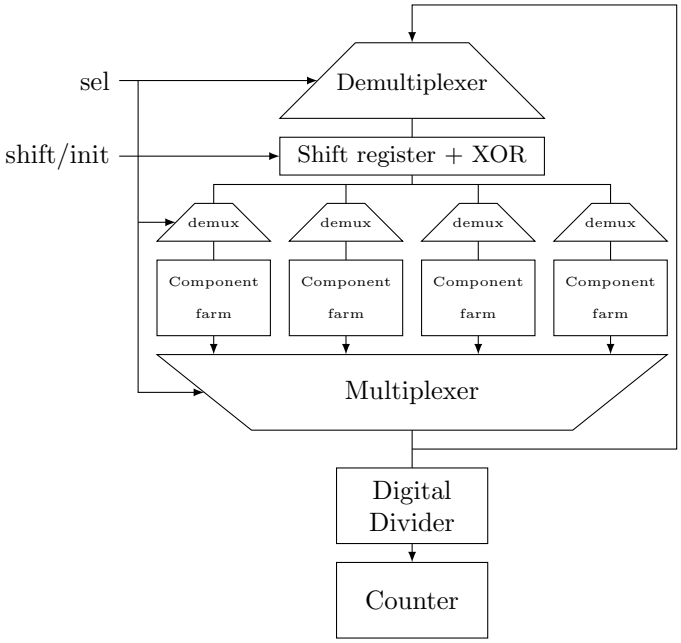

Figure 8: Changable Ring Oscillator 2

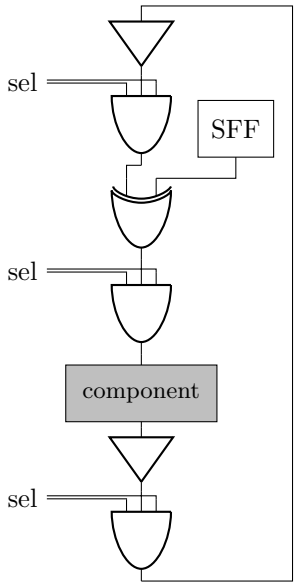

Figure 9: critical path of dynamic ring oscillator

counter with scan chain

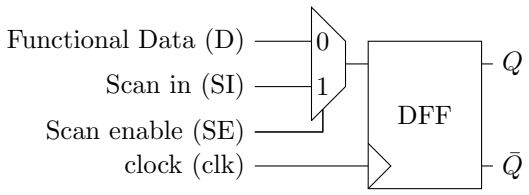

Figure 10: Scan Flipflop (SFF)

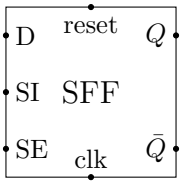

Figure 11: Symbol Scan Flipflop (SFF)

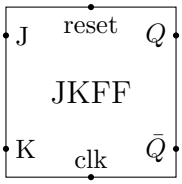

Figure 12: Symbol JK-Flipflop (JKFF)

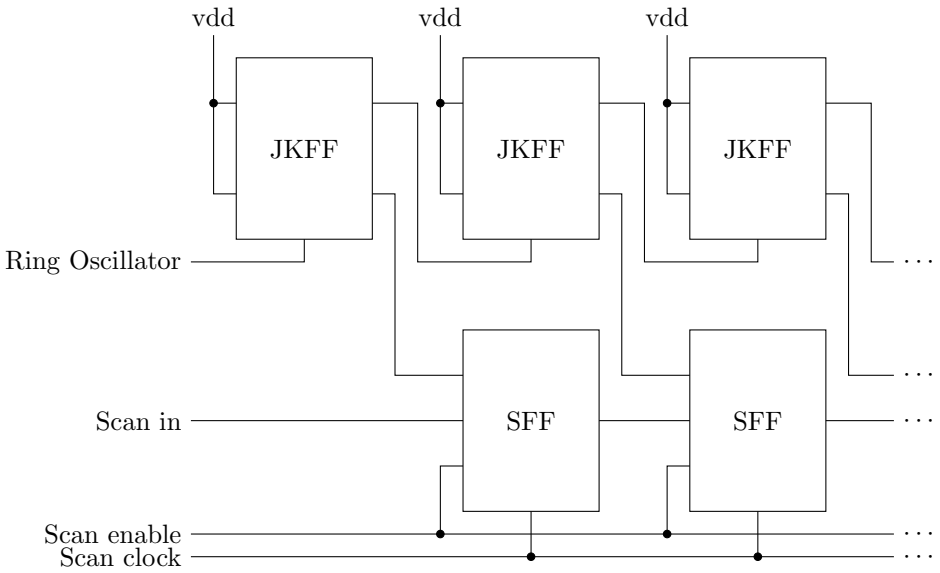

Figure 13: Counter with Shift register

SFF = 10 gates
JKFF = 10 gates

example: 16 gates + swappable ring oscillator, $1\,ps$ resolution

$$\text{ring size} = 16 + 8 = 24\text{gates} \tag{1}$$
$$T = 1.2\,ns \tag{2}$$
$$\text{counts} = 1200 \tag{3}$$
$$t_{meas} = 1.44\,\mu s \tag{4}$$
$$bits = 11 \tag{5}$$
$$gates = 11 \cdot 20 + 41 + 16 \cdot 16 = 517 \tag{6}$$

separate rings

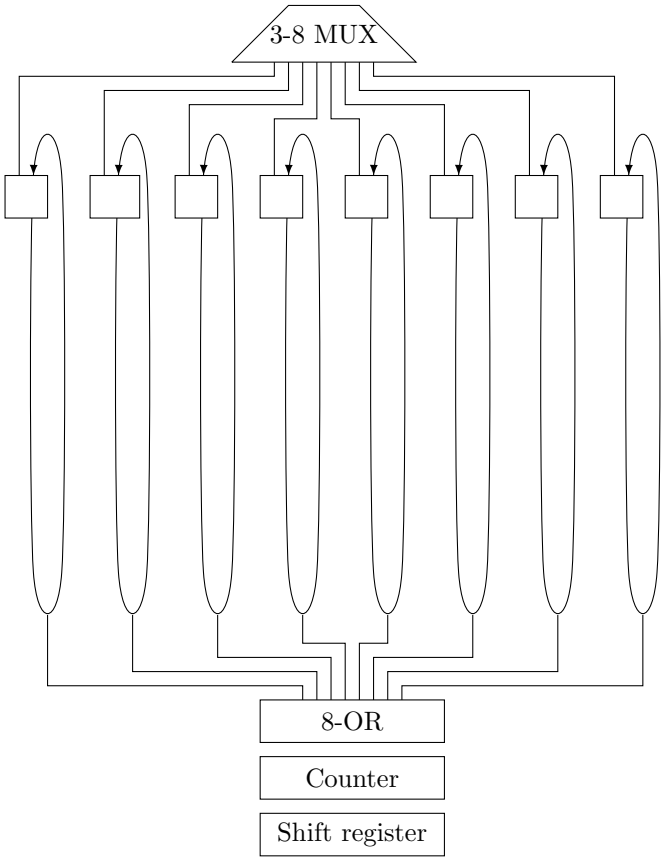

Figure 14: solution with multiple rings and a single counter