An 8-bit 4fs-step Digitally Controlled Delay Element with Two Cascaded Delay Units

Weizhen Wang[1], Hao Zhou[1], Fan Ye[1]*, Junyan Ren[1]

[1]State Key Laboratory of ASIC and Systems, Fudan University, Shanghai 200433, China
* Email: fanye@fudan.edu.cn

Abstract

To meet the rapidly growing demands of ADC speed and resolution, time-interleaved ADC (TI-ADC) is one of the hot topics. However, there are intrinsic problems such as clock skew and gain error between channels. As a key element of TI-ADC to overcome these problems, a high resolution and linearity Digitally Controlled Delay Element (DCDE) is designed. The DCDE consists of two-level cascaded delay units, coarse tuning and fine tuning, controlled by 32 bits thermal code and 8 bits binary code respectively, with about 4fs step size and 30ps full scale. The circuit is simulated and realized in TSMC 65nm CMOS process, with area of $790\times650\mu m^2$ and low power dissipation, which varies with input frequency and consumes 2.3mW at 8GHz clock rate.

1. Introduction

Along with the development of communication technology, traditional single-channel ADCs are far from meeting the requirement of high resolution and speed. TI-ADC is a new structure performing well in these aspects which operates with multi sub-ADCs. However, timing error between channels is becoming a remarkable problem. The proposed DCDE is designed to reduce the offset by generating specific delays for each channel.

The basic way to generate delay in a clock chain is to add a delay cell in the chain and then change the parameters on the delay path. Methods include: changing the bulk voltage of the PMOS transistor in some of the inverters, using gate [1][2] or drain capacitors [3] as varactor load, connecting voltage controlled transistors in charging or discharging path as variable resistors [7]. Some of the circuits use two stages of delay units. All the control signals can be digital, but the step size, linearity and tuning range vary a lot from each other. The most suitable methods used in each tuning unit are discussed.

In this paper, a delay unit is designed for a 12-bit, 2.5GS/s, 8 channels TI-ADC. This DCDE is the key element to reduce the sample time mismatches among the channels and to increase the resolution and linearity. Section 2 gives an overall description of the architecture of the DCDE, and then each part is discussed in detail. Section 3 and 4 present the simulation and test results respectively. And Section 5 concludes the work.

2. Circuit Architecture

The overall architecture of the proposed delay circuit is shown in figure 1. The DCDE is inserted in the clock chain. SPI conveys the digital control signal generated by the phase detecting circuit. Two-level cascaded delay units are applied to obtain the delay. The Coarse Delay Unit (CDU) is controlled by the digits directly. The Fine Delay Unit (FDU) is controlled by the analog signal, converted by the DAC and the operational amplifier. The type of control signals going to the delay units is determined by the design of the circuits, which will be discussed in the later part of the section. Therefore, given the input CKin, we will get an output CKout with exact delay required. Applied in a multi-channel ADC, the delay element can calibrate clocks in each channel to get the more suitable sample time.

In the proposed DCDE, CDU is used to provide a relatively large delay range while FDU provides high resolution and linearity. The two-stage architecture helps to improve the performance of the delay line in both aspects with lower power and smaller area.

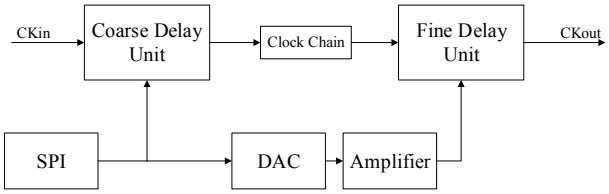

Figure 1. Delay unit architecture

2.1 Review on Delay Line Implementation

As introduced in the first section, plenty of researches are carried in delay line. The delay in a clock chain can be evaluated by parameters of loads [4]:

$$t_p = \frac{t_{pHL} + t_{pLH}}{2} = 0.69C_L\left(\frac{R_{eqn} + R_{eqp}}{2}\right) \quad (1)$$

Therefore, the basic method to generate a delay is to change the loads in the clock chain. Generally, they can be summed up in three methods.

(1) PMOS transistor with changing bulk voltage

As we all know, the bulk voltage can influence threshold voltage of a transistor

$$V_T = V_{T0} + \gamma\left(\sqrt{\left|2\Phi_F + V_B\right|} - \sqrt{\left|2\Phi_F\right|}\right) \quad (2)$$

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When the input and output of an inverter are equal [4], and V_{DD} is big enough for velocity saturate, then the currents of the two transistors are equal

$$k_n V_{DSATn}(V_M - V_{Tn} - \frac{V_{DSATn}}{2}) + k_p V_{DSATp}(V_M - V_{DD} - V_{Tp} - \frac{V_{DSATp}}{2}) = 0 \quad (3)$$

The switching threshold of the inverter can be deducted:

$$V_M = \frac{(V_{Tn} + \frac{V_{DSATn}}{2}) + r(V_{DD} + V_{Tp} + \frac{V_{DSATp}}{2})}{1 + r} \quad (4)$$

where $r = \frac{k_p V_{DSATp}}{k_n V_{DSATn}} = \frac{v_{satp} W_p}{v_{satn} W_n}$ is determined by the size of transistors. And the saturate current is

$$I_{DSAT} = k \frac{W}{L}[(V_{GS} - V_{TH})V_{DSAT} - \frac{V_{DSAT}^2}{2}] \quad (5)$$

When the current increases, the resistance decreases, so that the rising time will decrease. From the above, it is obvious that when bulk voltage of a PMOS is getting smaller, the threshold voltage reduces, the switching threshold increases and rising time decreases.

The effect of bulk voltage to delay is found out by simulation. The delay scale is quite small because of leakage and limited linearity range.

(2) Varactor load

When the source and drain are connected together with load voltage, a transistor works as a varactor. Or the drain of another transistor connected with such a varactor is a capacitor, which can be controlled by the voltage of drain.The scale of delay generated by varactors is much larger than the last method. And it keeps high linearity.

(3) Voltage controlled transistors

On charging and discharging path of an inverter, the speed of charge movement can be affected by resistors. If a transistor's gate voltage is changeable, the resistance of it can be controlled.

The transistor acting as a resistor must work in sub-threshold, so the resistance and control voltage range are limited.

The analysis and simulation suggest two methods suitable for the two units according to the different functions.

2.2 Coarse Delay Unit (CDU)

To reach a large range of delay, varactors are applied in coarse tuning. The control voltage on the drain and source is programmable digits from SPI.

Figure 2 shows the architecture of the proposed CDU. The value of W/L of transistors is made small to reduce the step size while the number of transistors is increased to reach a large range. There are 32 thermal codes which can control the varactors because they are equivalent to each other in changing the load in the clock chain. Therefore, the unit can generate 32 different delays.

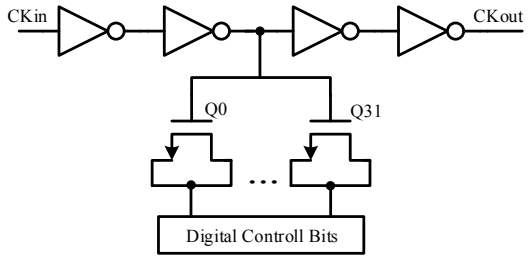


Figure 2. Coarse Delay Unit (CDU)

2.3 Fine Delay Unit (FDU)

The FDU is required to provide high resolution and linearity while the range can be small. So a PMOS transistor with changing bulk voltage is applied in this unit, which is shown in figure 3.

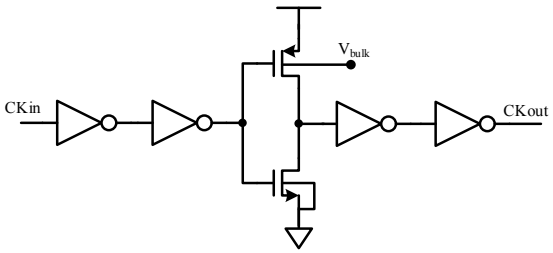


Figure 3. Fine Delay Unit (FDU)

The bulk voltage needs to be controlled by analog signal because the delay is linearly dependent to the bulk voltage in a specific range. The analog voltage is provided by the DAC and the operational amplifier. The performance of the three units determines the resolution of DCDE.

2.4 Serial Peripheral Interface (SPI)

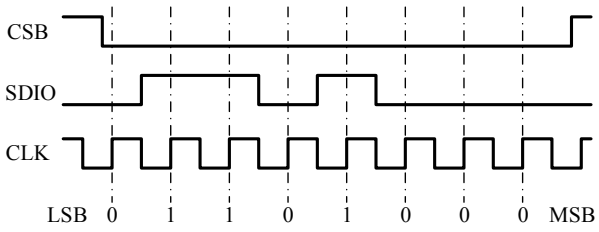


Figure 4. Timing diagram of SPI

The SPI unit is the bridge of programmable digits and the corresponding delay we want. In this circuit SPI has three inputs: reference clock CLK, chip select CSB and data SDIO. The unit converts a serial signal into parallel signals so that the digits can control the delay units at the same time. When CSB is 0, SPI samples according to CLK and then data is transferred bit by bit and stored in a shift register.

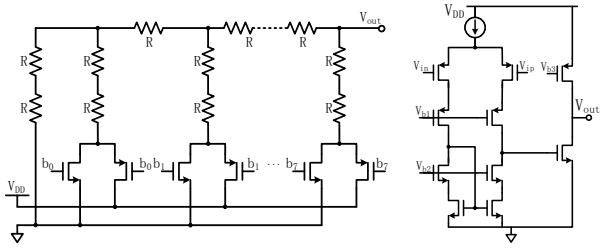
In order to avoid overlap, the data is generated at falling edge and sampled at rising edge. As shown in figure 4, the control signal transmitted by the SDIO is 00010110.

2.5 8-bit DAC

The DAC in the delay element uses R-2R resistor ladder to convert 8-channel feedback into analog signals [5], shown in figure 5 (a). The architecture is simple and works fast. An 8-bit R-2R DAC uses only 24 resistors. If the input is $\{b_{n-1}, b_{n-2}, \ldots, b_1, b_0\}$, the output is

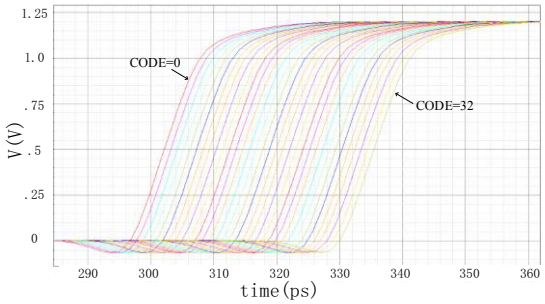
$$V_{out} = \frac{V_{ref}}{2} b_{n-1} + \frac{V_{ref}}{4} b_{n-2} + \cdots + \frac{V_{ref}}{2^{n-1}} b_1 + \frac{V_{ref}}{2^n} b_0 \quad (6)$$

The arms switching between reference voltage and ground are transmission gates, controlled by the input.



(a) (b)

Figure 5. (a)DAC structure; (b) Operational amplifier structure



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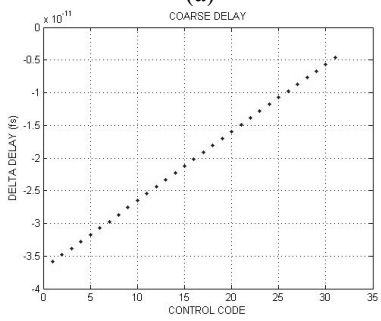

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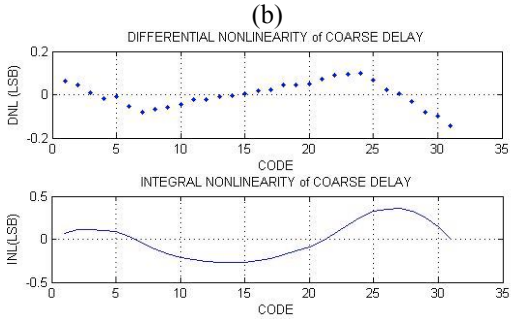
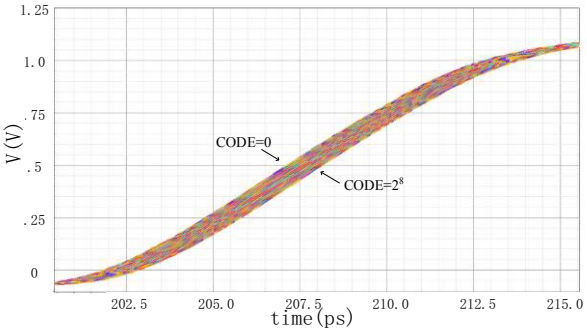


(c)

Figure 6. (a) Simulated timing; (b) relation of delay and code; (c) DNL &INL of CDU

2.6 Operational Amplifier

The output of DAC is driven by the two-stage operational amplifier. This unit consists of a telescopic cascode amplifier and a single cascode amplifier. The structure is shown in figure 5(b).



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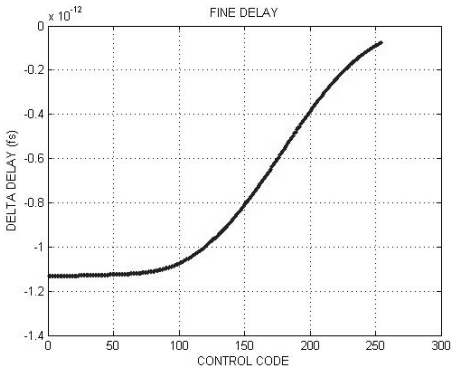

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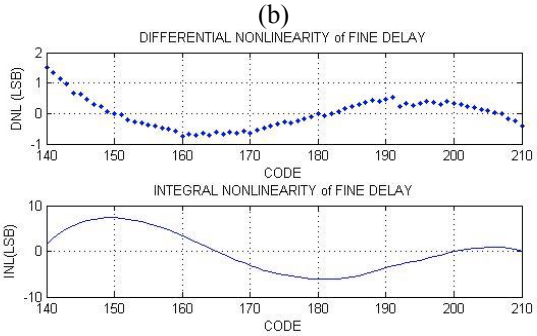


(c)

Figure 7. (a) Simulated timing; (b) relation of delay and code; (c) DNL &INL of FDU

3 Simulation Result

The proposed circuit is realized in TSMC 65nm CMOS process. Here presents the performance of the two units respectively.

The simulation result of CDU is shown in figure 6. For 32 bits thermal codes, there are altogether 32 delays. The largest delay is 31.22ps. Step size is 0.9756ps. The DNL & INL in figure 6 (c) shows the well behavior in linearity.

The performance of FDU is shown in figure 7. For 8 bits binary codes, there are altogether 2^8 delays. The scale is 1.056ps. Step size is 4.125fs.

The unit is controlled by the output of operational amplifier, which cannot reach full scale from GND to VDD or keep the linearity. And the delay generated by changing bulk voltage is linear only in part as discussed. The results of code 140 to 210 are taken for fitting. The DNL and INL show high linearity in a specific section.

4 Experimental Result

The proposed delay element is designed and fabricated in TSMC 65nm CMOS process. The layout is shown in figure 8. The total area is 790×650μm^2.

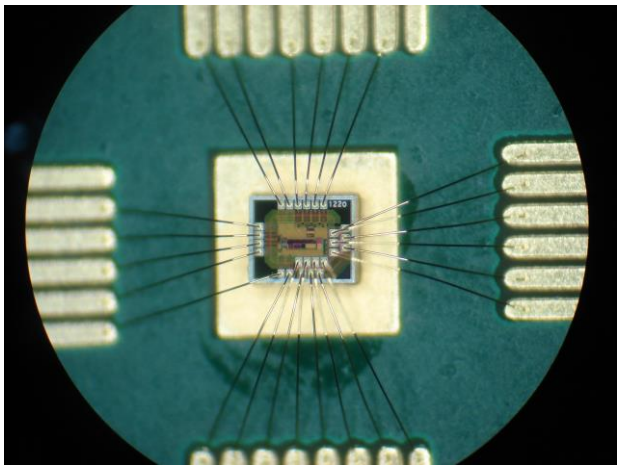
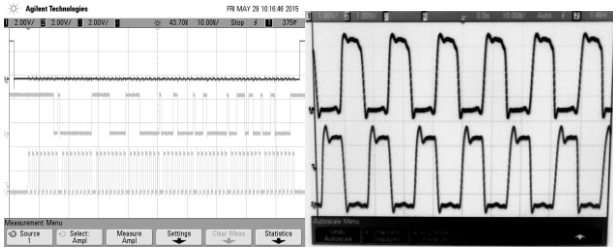


Figure 8. Layoutof the proposed DCDE



(a) (b)

Figure 9. Test results (a) SPI timing; (b) two channels with input and output of 1GHz and different delays

The SPI unit works as shown in figure 9(a). Compared with figure 4, it transmits the input SDIO signal at 64 periods of CLK when CSB is 0. The output, partly shown in figure 9(b), keeps the frequency of input while the delay is controlled by the SPI, which can realize about 4fs step size and 30ps full scale as designed. The power dissipation varies with clock rate and reaches 2.3mW at 8GHz.

5 Conclusion

The proposed digitally controlled delay element consists of two level cascaded delay units, which adjust delay in large range and high resolution respectively. The coarse delay unit provides tuning scale of more than 30ps, while the fine delay units provides step size of about 4fs. The circuits is simulated and realized in TSMC 65nm CMOS process. with area of 790 × 650μm^2 and power dissipation of 2.3mW at 8GHz clock rate.

Acknowledgments

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