# Statistical Characterization of Hold Time Violations in 130nm CMOS Technology

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***Abstract*—Statistical process variations are a critical issue for circuit design strategies to ensure high yield in sub-100nm technologies. In this work we present an on-chip measurement technique to characterize hold time violations of flip-flops in short logic paths, which are generated by clock-edge uncertainties in synchronous designs. Using a precise programmable clock-to-data skew generation circuit, a measurement resolution of ~1ps is achieved to emulate race conditions. Statistical variations of hold time violations are measured in a 130nm low-power CMOS technology for various register-to-register configurations and show 3σ die-to-die standard deviations of up to 15%.**

## I. INTRODUCTION

Modern synchronous digital designs necessarily include a large amount of flip-flops (FF) in pipeline stages to improve data throughput. FF timing is determined by the CLK-Q propagation time, setup time and hold time. The setup time is the amount of time that the data input must be ready before the clock edge, while the hold time is the amount of time the flip-flop input data must remain stable after the clock edge. The variation of the propagation time due to process variability has been already investigated by Monte Carlo simulation [1]. While statistical variations of setup and propagation times in critical paths are essential for maximum chip performance, a violation of the hold time in short FF-logic-FF paths leads to a chip failure due to a generation of races in the pipeline. Race conditions are caused by the combination of short paths, clock skew, and jitter between sending and receiving FFs, and process variations. The internal race immunity is a figure of merit to characterize the robustness of a FF against race conditions and is defined as the difference between clock-to-Q delay and hold time. Hence, the race immunity can vary greatly between different FF types [2].

Since modern digital CMOS designs, such as microprocessors, DSP cores, and dedicated hardware accelerators typically comprise thousands of FFs, a statistical analysis of the internal race immunity in combination with with clock uncertainties is mandatory. Especially scan chains for DFT schemes [3], where FFs are connected in a serial fashion to build up a shift register during test mode, are sensitive since no logic is placed between the FFs. Therefore, several techniques for diagnosis of single or even multiple hold time failures in scan chains are proposed [3-6]. There are also techniques to diagnose these failures in generic short logic paths [7] and buffer insertion to increase the delay of these paths. For example, hold time fixing, or padding, is typically done during chip design [8]. However, depending on the design and FF properties, without detailed analysis of the critical clock skew and process variability, the extra delay introduced during hold-time fixing can be over or under estimated.

In this work, we therefore present a statistical analysis of the critical clock skew in several test paths, due to process variability in a 130nm CMOS technology. To facilitate an on-wafer test a measurement circuit with a precision compatible to the speed of the technology is needed.

The paper is organized as follows: section II describes the test circuits used and the timing issues. Section III introduces measurement scheme for a precise FF characterization. Section IV contains experimental results measured on a test circuit fabricated in a 130nm low power CMOS technology. Finally, the paper is concluded in section V.

## II. TEST CIRCUIT AND TIMING ISSUES

To evaluate the impact of statistical variations on hold time violations four different logic paths are considered. The two basic configurations are two simple pipeline stages with

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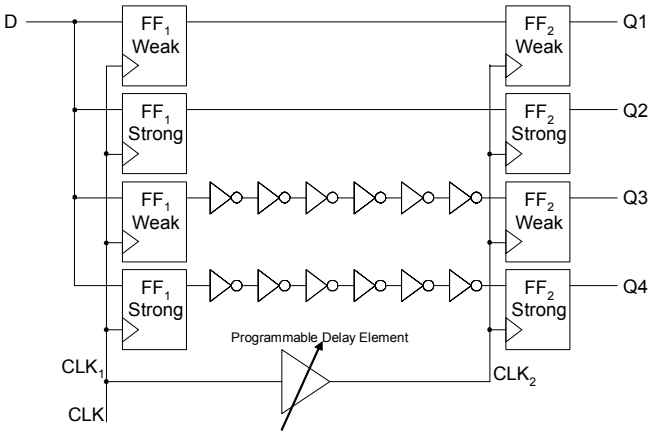


Figure 1. Different test circuits with sensitivity to race conditions.

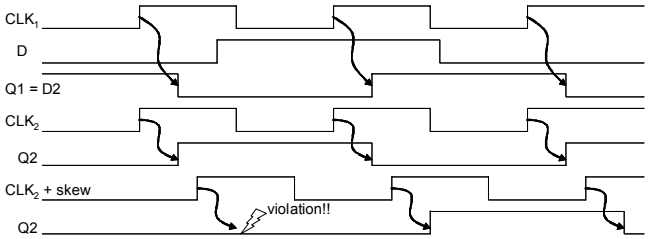


Figure 2. Timing diagram showing hold time violation.

two master-slave edge-triggered FFs without logic between them, representing one stage of a scan chain. Further pipelines including six small inverters between the FFs, represent short logic paths. The FFs used in this work are conventional rising edge-triggered master-slave FFs composed of CMOS transmission gates in the forward propagation path and $C^2$MOS latches in the feedback loops [9] with typical library extensions such as input and output node isolations and local clock buffers.

For each configuration a version with the weakest FF of the standard cell library, i.e. smallest transistor sizes and hence largest sensitivity to process variations, and a version with 8x increased driving strength is used. Comparing the results of both it is possible to analyze the impact of different transistor dimensions on the variability. The inverters used in both versions are of the minimum size, since these configurations represent typical non-critical paths where large driving capability is not required.

To emulate clock uncertainties, the sending and receiving FFs are controlled by different clock signals. The clock signal CLK2 of the receiving FFs is generated by a programmable delay line as shown in fig. 1. If this artificial clock skew is large enough, i.e. CLK2 arrives after CLK1 and exceeds the internal race immunity $t_{CLK\text{-}Q}$-$t_{HOLD}$ of the FF, a race is produced and detected if the output of both FFs are of same value at same time (Q1(t)=Q2(t)). The violation can be detected by initializing the FFs with opposite values, and applying a pulse in the data input, as shown in fig. 2. As long as Q1(t)≠Q2(t) pipeline operation is correct. Equation (1) describes the timing conditions in the case of a violation.

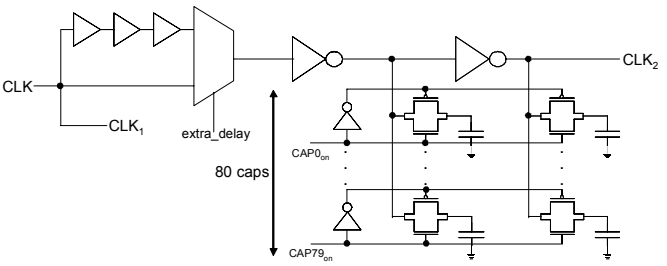


Figure 3. Schematics of the programmable delay line for the clock skew emulation.

Especially, fast FFs with large hold times are sensitive to hold time violations. $\Delta t_{var}$ includes variations from different sources.

$$t_{CLK-Q} - t_{hold} - t_{CLKskew} - \Delta t_{\text{var}} < 0 \qquad (1)$$

It is possible to see that the possibility of a hold time violation receives contribution of the FF race immunity (that is inherent to the FF type and size used in the design), the maximum clock skew found in the circuit, and process variations. If the clock uncertainty is very well controlled and race immunity is large enough, process variability plays a minor role, but this is not the case of the majority of semi-custom designs that have to meet a short time-to-market. Usually, the clock uncertainty and race immunity are of about the same order of magnitude.

## III. Measurement Scheme

To specify the critical clock skew producing a hold time violation, the artificial skew is programmable over a wide range of 80 steps corresponding to a resolution of ~1ps. The delay line is composed of two inverters, and 80 NMOS/PMOS gate capacitances as load elements connected to the inverters via pass transistors. The capacitances and transistors have been carefully designed to be able to achieve steps of the desired resolution.

Programming is done using an 80-stage shift register to control the inputs of the pass transistors. For coarse-grain clock skew shifting a multiplexer to enable or disable a further buffer chain is added. It is needed because the versions with 0 or 6 inverters have very different critical clock skews. Fig. 3 shows the implemented circuit.

To measure the absolute time produced by a specific setting of the programmable delay line, it is additionally placed in the middle of a ring oscillator. The ring oscillator is connected to an 11-stage frequency divider to monitor the output frequency. Thus, it is possible to determine the programmed delay based on measuring and comparing the frequencies achieved with different numbers of capacitances. Fig. 4 shows the final layout of the different circuits.

For the measurement, first the settings for all combinations of the 80 capacitances are written into the shift register. Then the frequencies of the ring oscillator are measured for all configurations to calibrate the programmable skews. For measurement of the delay variations of the logic path, the

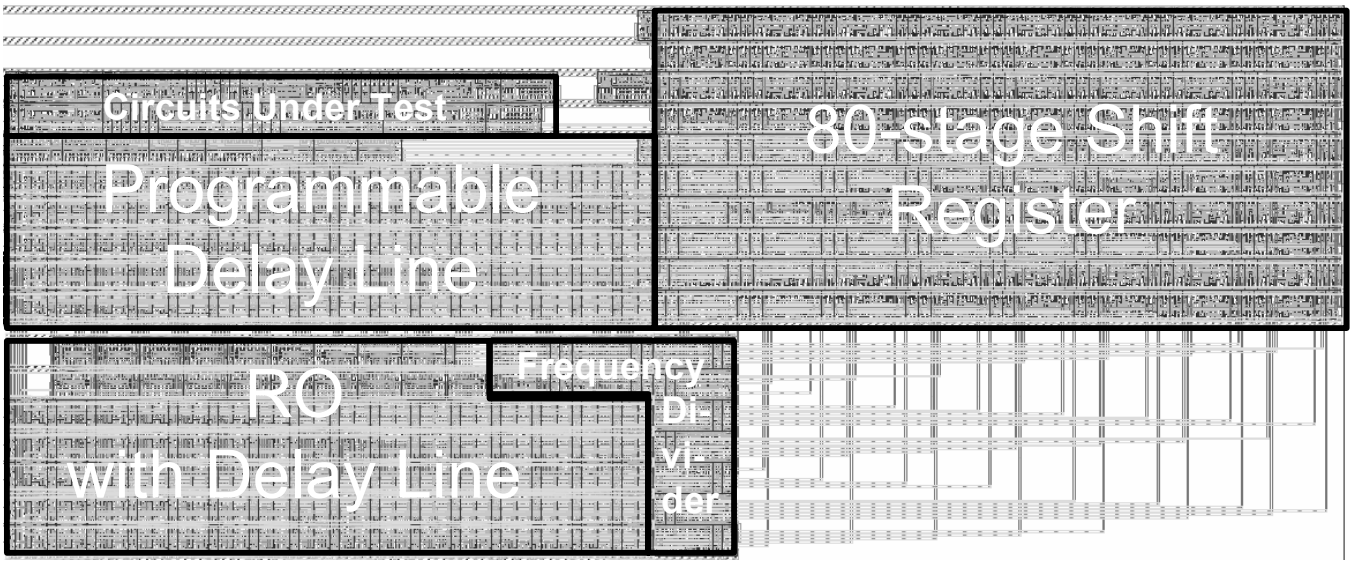


Figure 4. Final Layout

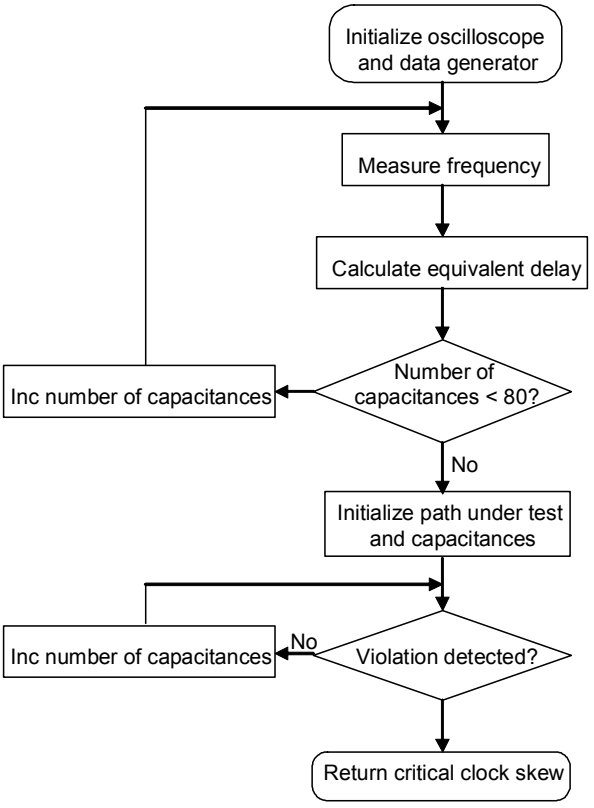


Figure 5. Measurement flow

delay line is initialized with minimum delay, and the delay is stepwise increased until a violation in the pipeline is detected. The corresponding delay estimated from the ring oscillator measurements is the critical clock skew for the given die and operating conditions. The procedure is repeated for each of the 4 test circuits considering the rising and falling input transitions. Fig. 5 shows the measurement flow.

## IV. Experimental Results

The circuits are fabricated in a 130nm low power CMOS technology, and 182 chips are measured on one wafer. The total size of the chip is 180 x 71µm. The measurements are done at 25°C and for $V_{dd}$ = 1.5V.

First, the variability of the ring oscillator frequency over the wafer is analyzed, showing a typical global wafer variation with slower dies in the center of the wafer (fig. 6). The frequencies are normalized to a given value, to omit derivation in the absolute speed values of the technological data. The faster circuits achieve resolutions less than 1ps, while none of the chips had a resolution of more than 1.2ps.

Fig. 7 shows the distribution of the critical clock skew for 0-1 transitions in all 4 test circuits. The expected Gaussian curve for normal distributions is observed. Based on this data and repeating the measurement procedure for 1-0 transitions, the mean critical clock skew and the standard deviation are extracted. Table I summarizes these results. The results are normalized again.

The 3σ deviation of the delay can be up to 15% of the nominal value. The critical skews are in the range of the clock skew that can be expected in circuits using the same technology, showing that these statistical effects have to be considered during hold-time fixing at the end of the layout generation. It is important to note that using larger FFs, the absolute variation of the critical skew decreases, but the relative value remains similar, since these circuits are faster. This indicates that larger FFs have an increased probability of violation, since the clock skew needed to provoke the failure is smaller.

The test circuits with extra inverters have an expected larger absolute variability, but relatively it is smaller, showing that the FFs are more sensitive to process variations than the inverters, or a large number of inverters average the variability.

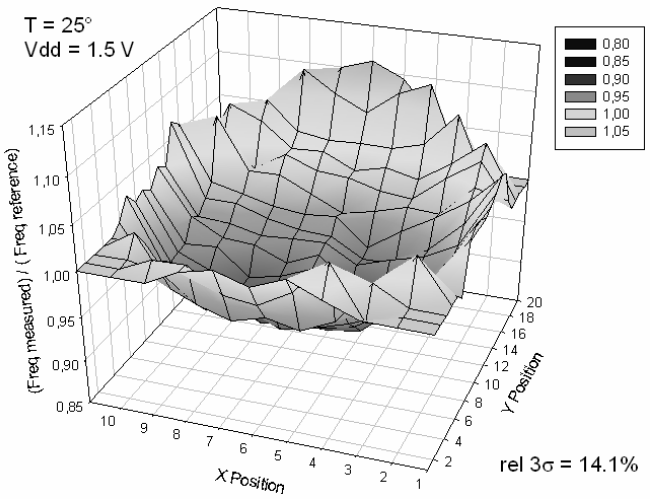


Figure 6. Normalized frequency variability of the RO over the wafer.

TABLE I. NORMALIZED HOLD TIME VIOLATIONS AT $V_{DD}$=1.5V AND T=25°

| Circuit | Transition | μ | 3σ | 3σ / μ (%) |
|---|---|---|---|---|
| weak FFs, no inverters | Rising | 100.00 | 14.88 | 14.88 |
| | Falling | 109.95 | 14.60 | 13.28 |
| strong FFs, no inverters | Rising | 88.87 | 12.06 | 13.57 |
| | Falling | 95.00 | 12.28 | 12.93 |
| weak FFs, 6 inverters | Rising | 181.70 | 23.76 | 13.08 |
| | Falling | 192.71 | 23.19 | 12.04 |
| strong FFs, 6 inverters | Rising | 170.54 | 22.44 | 13.16 |
| | Falling | 177.52 | 22.22 | 12.51 |

Another important point is that the master-slave FFs used in the experiment typically have a small or even negative hold time, and consequently larger race immunity. Repeating the experiments for faster FFs that are used in high-speed designs and have larger hold times, the results would be even more critical.

## V. CONCLUSION

This work presents an experimental analysis of the variability of hold time violations of edge-triggered master-slave FFs due to process variations in a 130nm low power CMOS technology. For accurate on-wafer characterization, a test circuit and a measurement technique with ~1ps resolution are presented. The presented methodology provides detailed information about the circuit robustness of FFs under realistic operating conditions. This precise FF characterization then enables designers to perform hold-time fixing for short paths considering statistical variations of FFs as well as delay increasing inverters during buffer insertion. Moreover, during standard cell library development, the methodology is beneficial to optimize the FF portfolio, i.e. to balance race immunity and clock-to-Q propagation delay for various cell driving strengths and different FF topologies.

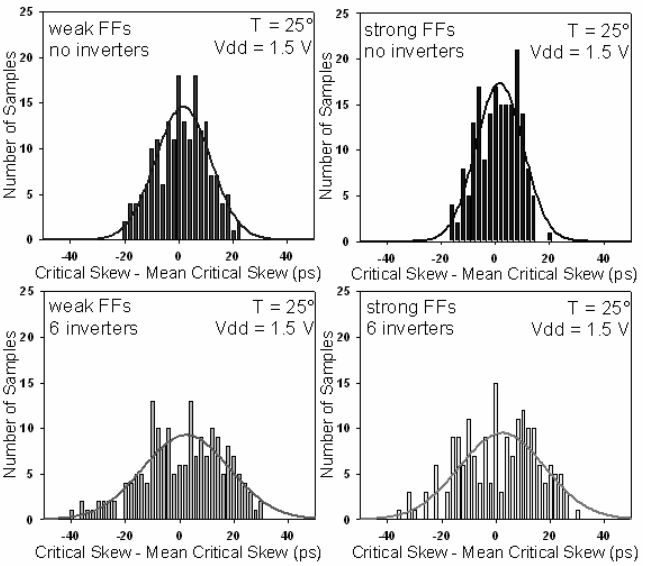


Figure 7. Measured distribution of the critical clock skews for rising transitions. The nominal case (mean critical skew) is set to 0ps.

The proposed technique can be extended to characterize other timing constraints. Finally, statistical timing violations in edge-triggered master-slave flip flops are investigated experimentally. Future work includes the investigation of the impact of different temperature and supply voltage on variability, comparison to other technologies, and isolation of global and local variations.

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