# Hardware Characterization

## Required measurements

http://ra.ziti.uni-heidelberg.de/pages/student_work/seminar/ws0304/richard_sohnius/praesentation.pdf

Transition times. Characterized and measured between 30 % and 70 %. Standardized reporting between 10 % and 90 %.

- area
- power
- timing contstraints (setup/Hold time, recovery/removal time)
- propagation delay time
- input capacitance

**Power**:

- Dynamic power (switching power)
- Static power (leakage power)
- Passive power (internal power. power used by sequential cells when inputs change without output change)

**Delay**:

https://www.csee.umbc.edu/~cpatel2/links/641/slides/lect05_LIB.pdf

- sum of intrinsic delay, slope delay, transition delay and connect delay
- intrinsic delay is fixed value independent of surroundings
- slope delay is produced by the slew of the input signal
- transition delay is the time required to change the capacitance of the next stage input pins
- connect delay is delay caused by the wire between output and next input pins

Delay model of Liberate (.lib) is the CMOS Non-Linear Delay Model.

- Delay and transition time are modeled as function of Input slew and Output load
- Data is stored in a 2D LUT (look-up table)
- Intermediate values are interpolated
- Data points are usually not equidistant

## solutions

feedback loop with a counter?

# Solutions

Timing: use frequency divider (Alex's grey counter) and a ring oscillator can characterize 64 cells? only needs to change a single cell and wait for a while.

Power: simply switch of the counter, let the ring oscillator run and measure the power. The only changes are within the ring oscillator, so over time the power gets more precise.

Area is of no concern

# Testbenches

## Numerically Controlled Oscillator

Control when the accumulator flows over. Needs a very fast counter. Overflow amount gets carried over to next cycle.

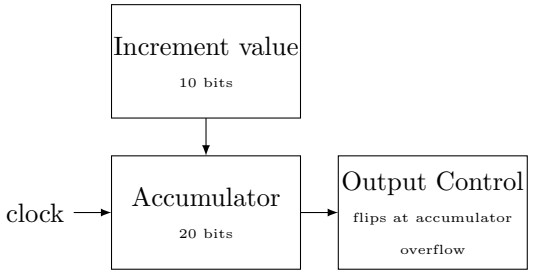


Figure 1: NCO

## Time to Digital Converter (TDC)

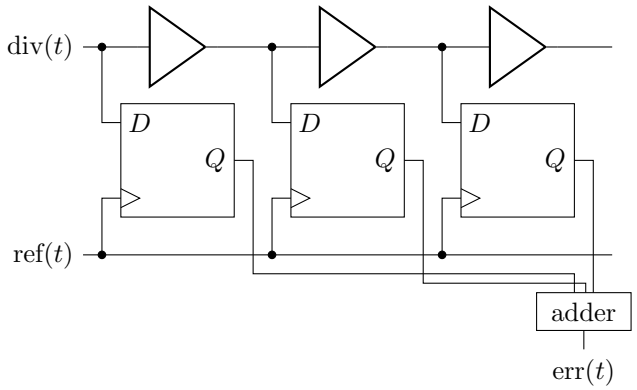


Figure 2: TDC

## Phase Detector

The phase detector produces a 1 between the time the reference signal switches to a one, and the divider switches to a one.

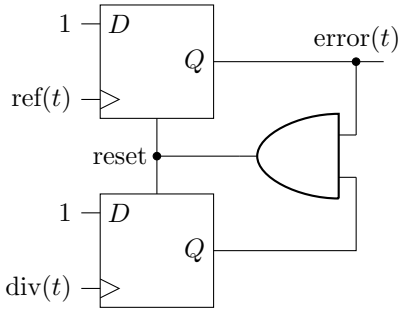


Figure 3: Phase detector

## Digitally controlled oscillator

Uses digitally controlled switches to change the output load

## Grey Counter

8-bit grey counter designed with Alex

## Digital Divider

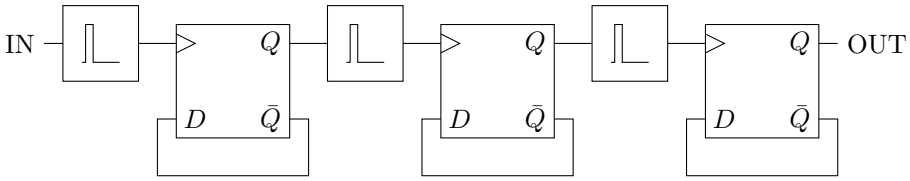


Figure 4: Digital divider

## 4-bit Multiplexer and Demultiplexer

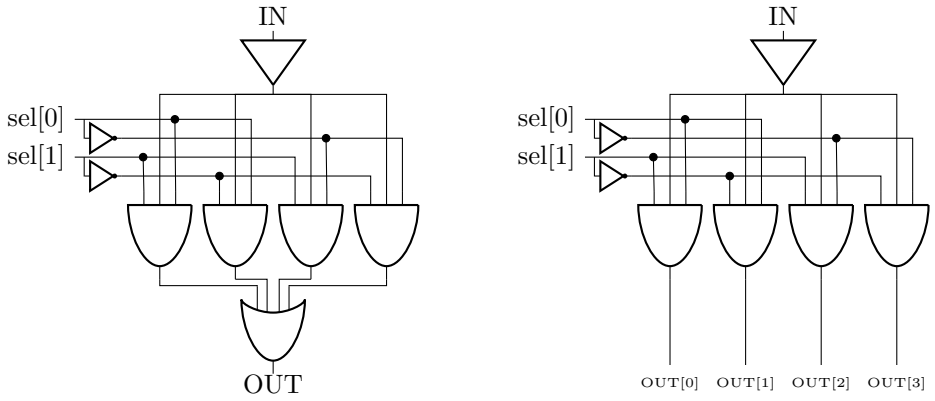


Figure 5: MUX

## Changable Ring Oscillator

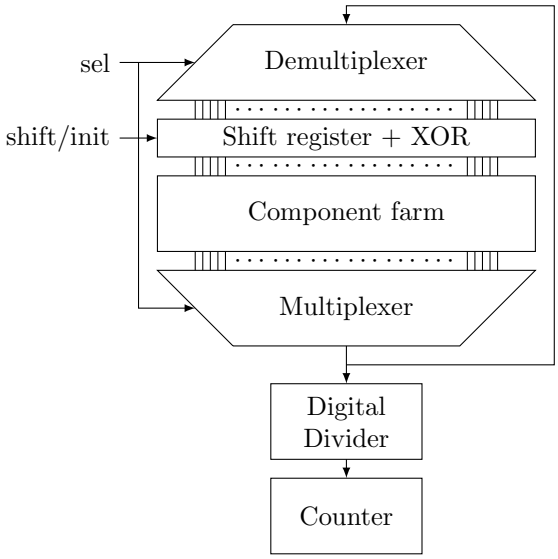


Figure 6: Changable Ring Oscillator

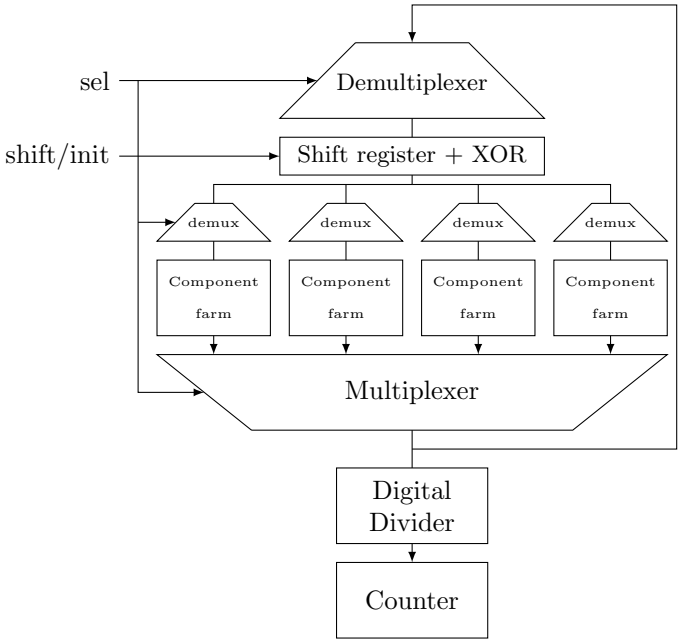


Figure 7: Changable Ring Oscillator 2

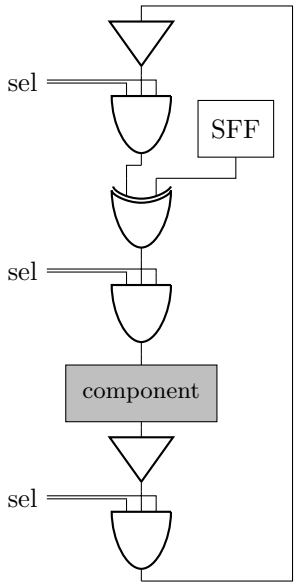


Figure 8: critical path of dynamic ring oscillator