Test circuit for accurate measurement of setup/hold and access time of memories

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***Abstract*- This paper will examine the latest developments in the field of designing the test circuits for accurate measurement of setup/hold and access time of memory IPs. Measurement across all voltage domain and temperature corners, by way of the architecture discussed, has a fine resolution of just two inverter delay and correlates well with silicon within permissible range.**

Keywords—memory, test chip, setup, hold, access

I. INTRODUCTION

Intellectual property (IP) characterization test chips play a pivotal role in determining the silicon correlation of IPs before they can be used on a real system-on-chip (SOC). With the advancement in technology, the challenge of designing test structures for test chips is twofold –

- Accurately measuring the various IP parameters (functionality, timing, power, etc.)
- Silicon correlation of the measured parameters within permissible range.

Test circuits that were good enough to accurately measure the various IP parameters in 65nm and older technology nodes do not hold good for newer technology nodes like 14nm [1]. Memories in particular are specialized IPs requiring focused attention [2]. For all memory IP compilers under test, memory instance sizes and capabilities are chosen in such a way so as to ensure that the design performs across a wide range of possible configurations. A test circuitry is put in place for indirect measurement of the various IP parameters. Some instances of each memory type are connected to timing circuitry for the measurement of setup, hold, and access times. All of the memory blocks are connected to control pins to which appropriate test patterns are applied. Back annotated numbers are extracted from the implemented test chip and are then compared with the actual measured values on silicon.

The test circuits that are put in place for the testing of various IP parameters have undergone numerous improvements with time in order to be in tune with the smaller technology nodes. This paper focuses specifically on the test circuits for measurement of setup, hold and access time of memory IPs which have been tested up to 14nm technology node.

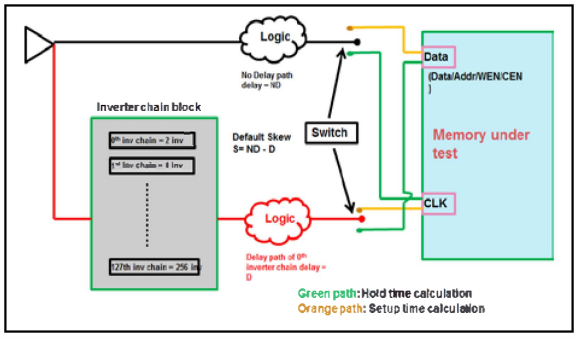

Fig. 1. Setup/Hold measurement basic architecture

II. SETUP/HOLD TIME MEASUREMENT

In order to correlate library characterized setup/hold values with silicon data, a test circuitry is put in place. This is because these values cannot be directly measured on silicon due to tester limitations. Indirect measurement of these values is made by carefully controlling skew between clock and another pin (e.g. address or data) and shmooing this skew value until the memory fails [Fig. 1]. The two delay points between which the memory gives a transition define the upper and lower bound of the setup/hold time of the memory. The difference between the upper and lower bound is the least count of measurement which corresponds to two inverter delay for the test circuitry discussed in the paper.

The test circuitry can be used for measurement of setup0, setup1, hold0 and hold1 [Fig. 2]. Where Setup0 is the time required for data to be stable before the clock edge after it has settled at level 0 and vice-versa for Setup1. Similarly, Hold0 is the time required for data to be stable at level 0 after the clock edge and vice-versa for Hold1. The delay block and the signal control block are the two main blocks required for the measurement.

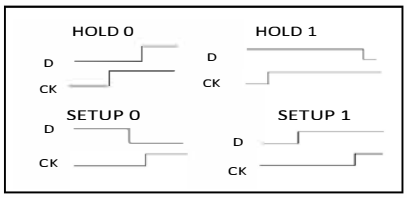

Fig. 2. Setup0/Hold0/Setup1/Hold1 basic definition

A. *Setup/Hold Delay block*

The purpose of the delay block is to introduce a skew between clock and the other pin for which setup/hold is to be measured. Inputs of the block are-

- Design clock
- Control signals to select between setup0/setup1/hold0/hold1 measurement
- Skew control to select between varying amount of controlled delay

The outputs of the setup/hold delay block are DATA_OUT and CLK_OUT. For setup testing, DATA_OUT has the no-delay and CLK_OUT has the controlled delay [Fig. 3]. For hold testing, DATA_OUT has the controlled delay and CLK_OUT has the no-delay [Fig. 4]. This controlled delay is generated with a chain of 256 back-to-back connected inverters. Output after every two inverters is tapped and passes through a mux tree and skew control determines which output to drive out 0 being the shortest delay and 127 being the longest.

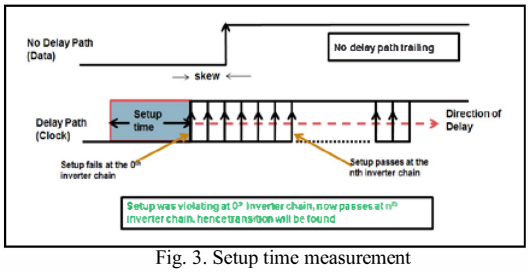

Fig. 3. Setup time measurement

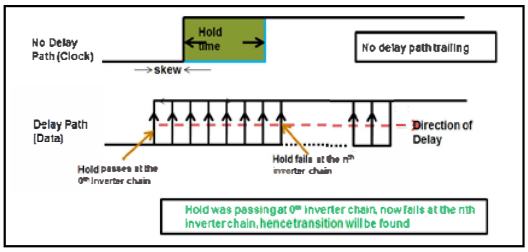

Fig. 4. Hold time measurement

In addition to providing a controlled delay signal there is also a static delay signal which has a small delay of 40 to 80 inverters marked as "No delay path" [Fig. 1]. The choice of the number of inverters is dependent on the technology. For a 14nm FinFET technology, since the cells have smaller delays, no-delay path comprises of 80 inverters. For correlation and on chip variation (OCV) measurement, delay chain inverters are formed as a ring oscillator. The oscillator output passes through a frequency divider circuit to reduce the frequency to a tester-measurable limit and then taken to the pad to measure.

B. *Signal control block*

Signal control block manages the memory input mux based on setup/hold control inputs [Fig. 5]. Here, primary inputs are driven through input-output (IO) pads. The delay block generated no-delay (NODLY) and controlled delay (DLY) inputs, along with primary inputs drive these muxes. This configures the mode of the delay block circuitry i.e. for setup measurement or hold measurement and for which pin of the memory (address/data/write enable WEN/chip enable CEN).

Two things to note with respect to Setup/Hold measurement circuitry are:

- Least count of the measurement can be as small as "two inverter" delay. This is achieved by way of the architecture and by placing the delay chain inverters abutted in the physical world to minimize the interconnect delay.
- The delay chain is controlled to form a ring oscillator for OCV measurement. This means that it does not require any extra circuitry for OCV measurement.

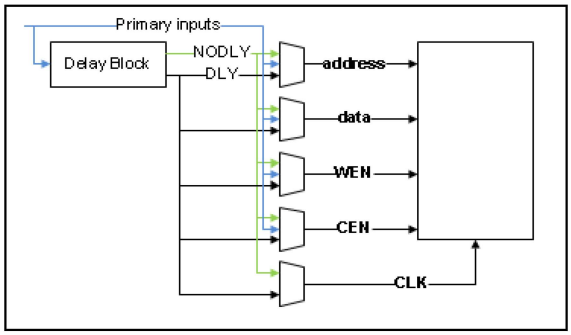

Fig. 5. Setup/Hold signal control block

Table 1 gives the setup/hold comparison of back-annotated (BA) numbers, versus the silicon measured data for a 14nm FinFET technology for different timing arcs of a memory instance. The results are for three silicon samples at slow-slow (SS) corner when memory periphery is working at 0.66V and its bitcells are working at 0.72V. None of the numbers listed in the table is absolute. For eg if BA is "a" then for SS Sample#1, Lower value is a+0.008. Lower and upper denote the respective bound between which the transition occurred on silicon. PASS criteria for the memory characterized value is that the BA should be greater than the measured lower value. The sections marked green fulfilled the PASS criteria whereas the sections marked red failed the PASS criteria. The difference between upper and lower bounds of the measured data on silicon, gives the "two inverter delay" resolution.

TABLE 1: BA v/s measured data for memory setup/hold circuit

Timing arc	BA	SS VDDPE:0.660V VDDCE:0.720V -25°C					
		Measured data in range					
		Sample SS#1		Sample SS#2		Sample SS#3	
		Lower	Upper	Lower	Upper	Lower	Upper
CLK->D hold0	a	a+0.008	a+0.026	a-0.057	a-0.032	a-0.034	a-0.006
CLK->D hold1	b	b-0.099	b-0.066	b-0.093	b-0.061	b-0.039	b-0.009
CLK->CEN setup0	c	c+0.085	c+0.104	c-0.036	c-0.004	c+0.015	c+0.045
CLK->CEN hold0	d	d-0.136	d-0.096	d-0.179	d-0.154	d-0.192	d-0.163
CLK->A setup0	e	e-0.046	e-0.013	e-0.121	e-0.097	e-0.174	e-0.141
CLK->A setup1	f	f-0.165	f-0.13	f-0.199	f-0.179	f-0.23	f-0.193
CLK->A hold0	g	g-0.041	g-0.007	g-0.159	g-0.137	g-0.139	g-0.102
CLK->A hold1	h	h-0.171	h-0.138	h-0.163	h-0.135	h-0.112	h-0.075
CLK->WEN setup0	i	i-0.233	i-0.201	i-0.208	i-0.181	i-0.253	i-0.224
CLK->WEN setup1	j	j-0.014	j+0.022	j-0.074	j-0.041	j-0.102	j-0.076
CLK->WEN hold0	k	k+0.012	k+0.044	k-0.134	k-0.11	k-0.122	k-0.095

III. ACCESS TIME MEASUREMENT

In order to correlate library characterized access time values with silicon data, a test circuitry is put in place. This is because these values cannot be directly measured on silicon due to tester limitations. Indirect measurement of access time is done by latching the output of the memory DATA into a series of flip-flops whose clock is delayed by a known controlled delay. The number of delay elements determines the access time of the memory [Fig. 6].

The controlled delay is generated by a chain of back to back connected inverters. Output after every two inverters is tapped and fed to the series of flip-flops. If the delay-chain delay is faster than the clock to Q delay, output of the flip-flop is the memory's previous value. Whenever a flip-flop generates the expected value, the delay of that flop and that of the previous flop gives the upper and lower bounds of the access time of the memory. The placement of the access block inverters and flops is abutted ensuring minimum interconnect delay.

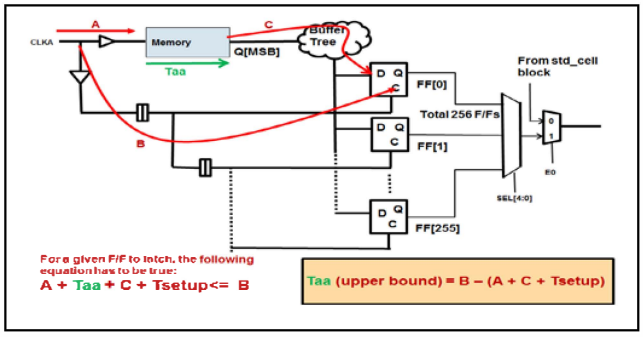

Fig. 6. Access time measurement basic architecture

Like in setup test circuitry, for correlation and on chip variation measurement, delay chain inverters are formed as a ring oscillator. The oscillator output passes through a frequency divider circuit to reduce the frequency to a tester-measurable limit and then taken to the pad to measure.

Table 2 gives the access time comparison of back-annotated (BA) numbers, versus the silicon measured data for a 14nm FinFET technology for 6 memory instances. The results are for three silicon samples at fast-fast (FF) corner when memory periphery and bitcells are working at 0.95V. None of the numbers listed in the table is absolute. For eg if BA is "a" then for FF Sample#1, lower value is a+0.40. Lower and upper denote the respective bound between which the transition occurred on silicon. PASS criteria for the memory characterized value is that the BA should be lesser than the measured lower value. All the three samples listed in table 2 fulfill the PASS criteria.

TABLE 2: BA v/s measured data for memory access circuit

Memory Instance	BA	Measured data in range					
		FF VDDPE:0.95V VDDCE:0.95V -25°C					
		Sample SS#1		Sample SS#2		Sample SS#3	
		Lower	Upper	Lower	Upper	Lower	Upper
1	a	a+0.40	a+0.43	a+0.42	a+0.44	a+0.41	a+0.43
2	b	b+0.46	b+0.48	b+0.47	b+0.50	b+0.47	b+0.49
3	c	c+0.29	c+0.31	c+0.29	c+0.32	c+0.29	c+0.32
4	d	d+0.23	d+0.25	d+0.21	d+0.23	d+0.21	d+0.23
5	e	e+0.22	e+0.25	e+0.22	e+0.25	e+0.23	e+0.26
6	f	f+0.30	f+0.33	f+0.30	f+0.34	f+0.31	f+0.35

IV. CONCLUSION

Methodologies required for accurate measurement and close silicon correlation of various timing parameters of memories, enumerate some of the issues faced by members of testing community today. The methodologies presented in this paper have been tested up to 14nm technology node. Future work involves testing in for 10nm and further lower nodes and bringing in required enhancements.

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