

Preethi's ROIC analysis

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1 setup

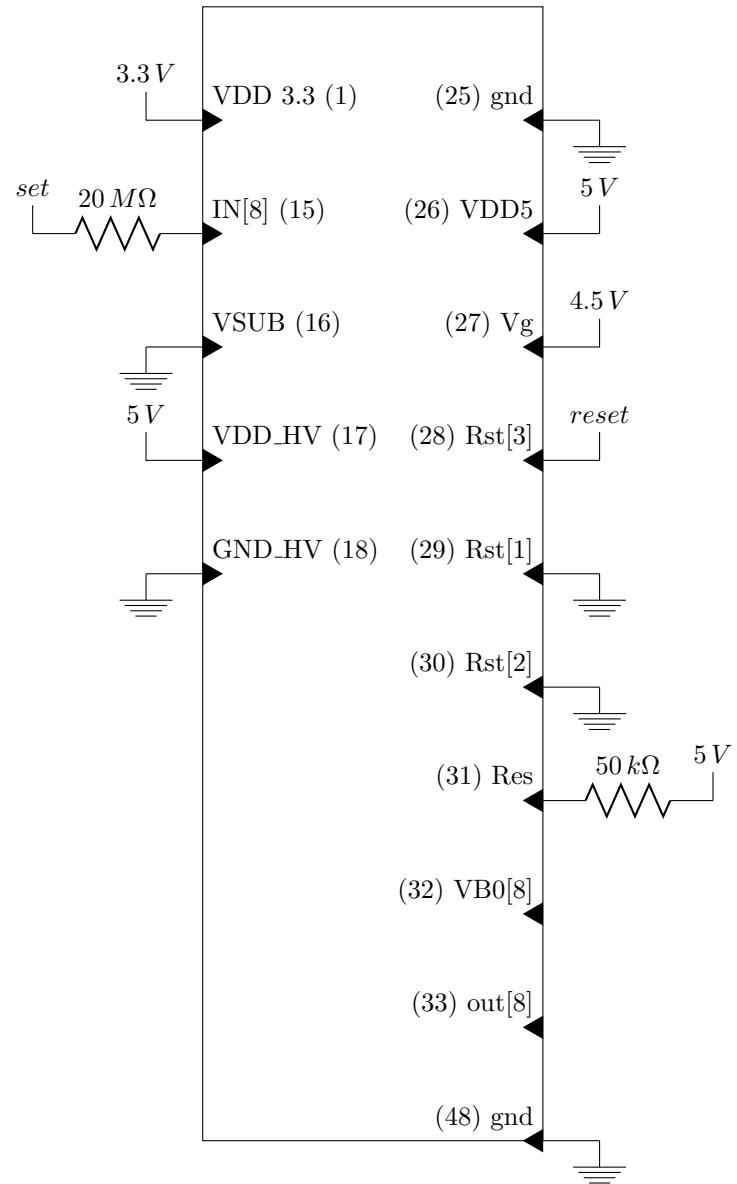


Figure 1: Schematic of breadboard

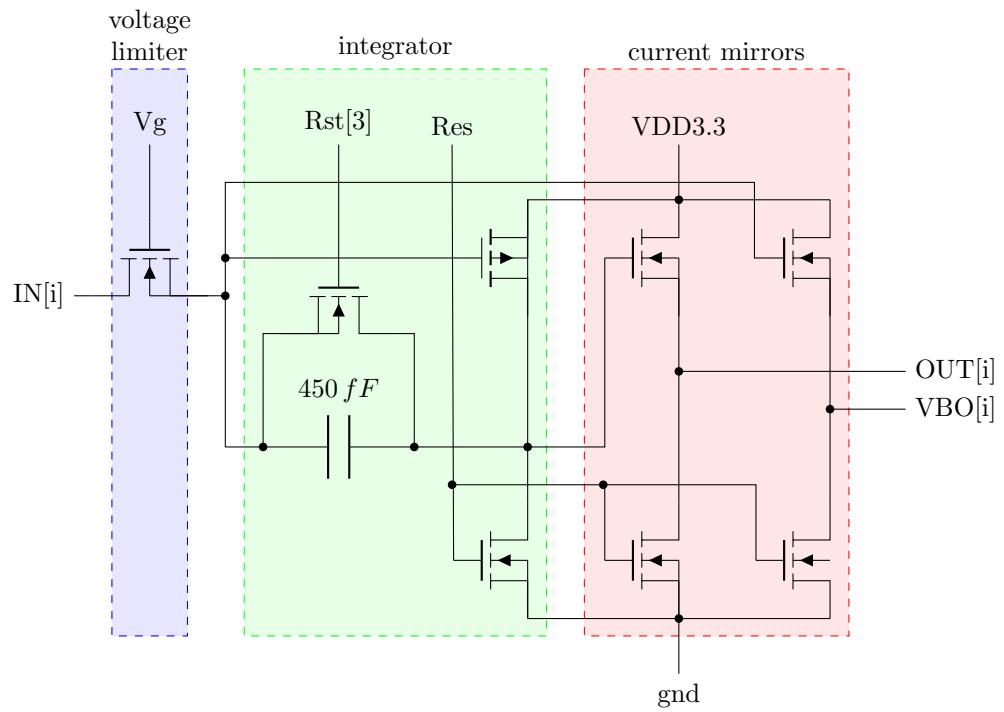


Figure 2: Schematic of ROIC channel

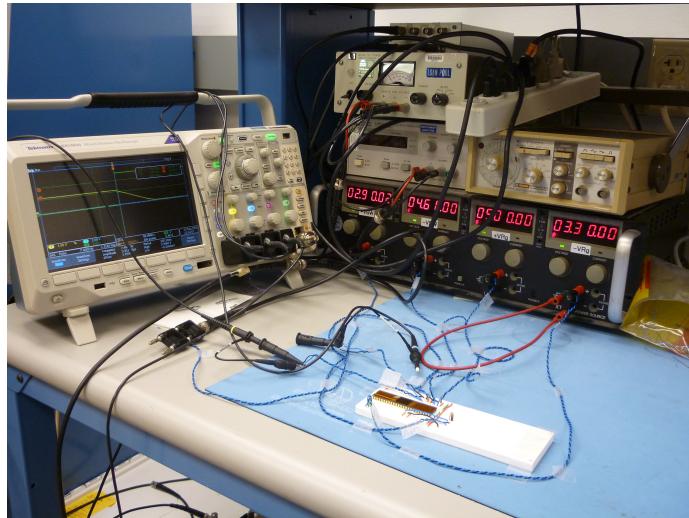


Figure 3: setup overview

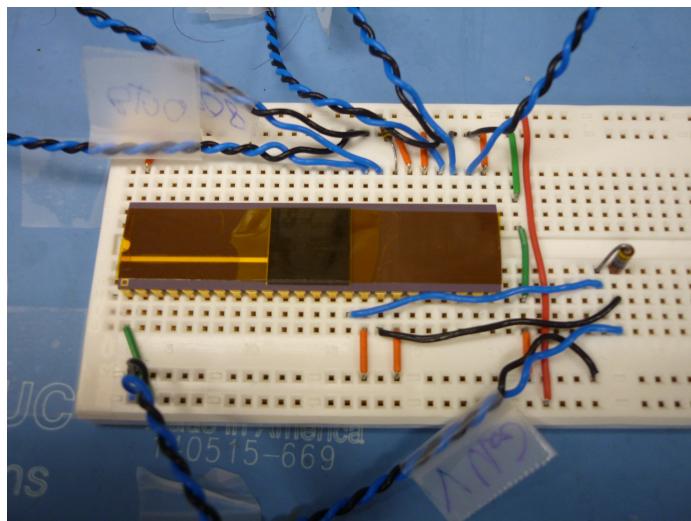


Figure 4: close-up

2 Characterization for high impedance voltage source

This section aims to characterize the behavior of the ROIC while exposed to a voltage source with a high resistance in the order of several $M\Omega$. A focus is put onto the performance in reset state, the relationship between input current and output voltage, and the current limiting properties of the input transistor.

2.1 Reset

This measurement addresses the behavior of the circuit in reset mode. Figure 5 shows the measured values during reset mode. Note that the input voltage is 2.4 V, which is important when calculating the input current.

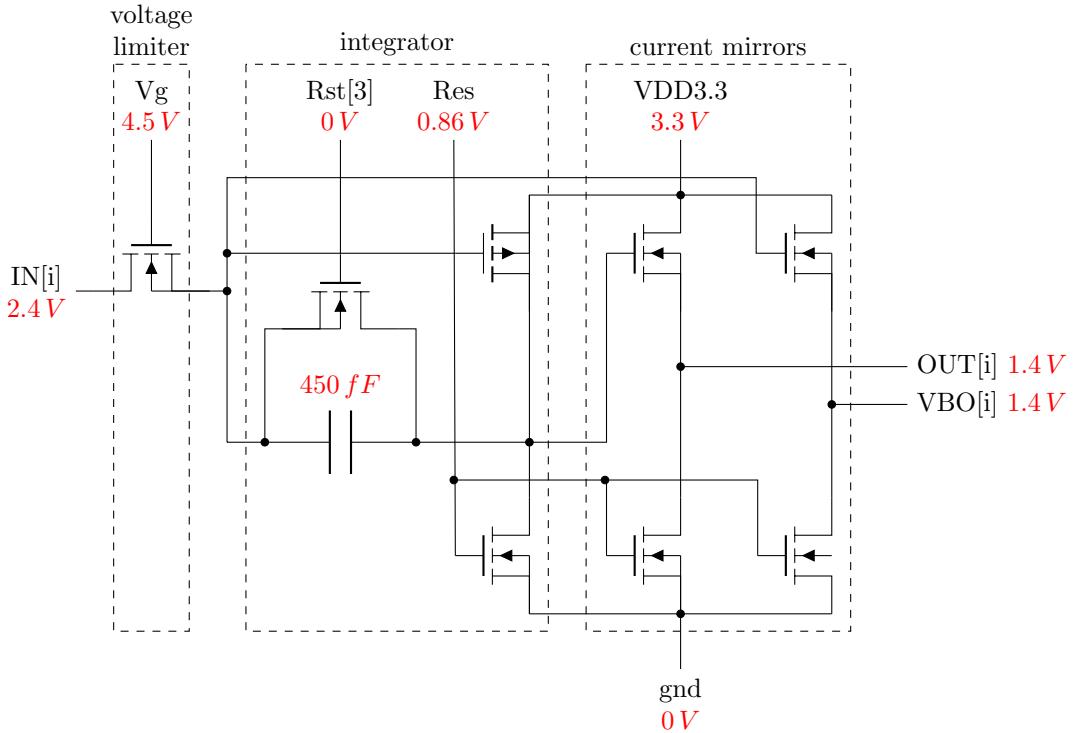


Figure 5: Schematic of ROIC channel template

2.2 Source follower

There are two identical source followers per lane. We can use the VBO source follower to characterise both. This because the input can be directly controlled, and the output directly read. Figure 6 shows both the measured data and a fitted line with the formula $v_{bo} = 0.827v_{in} - 0.624$. It will be assumed that this line characterises the performance of both source followers for $1 < v_{in} < 4$.

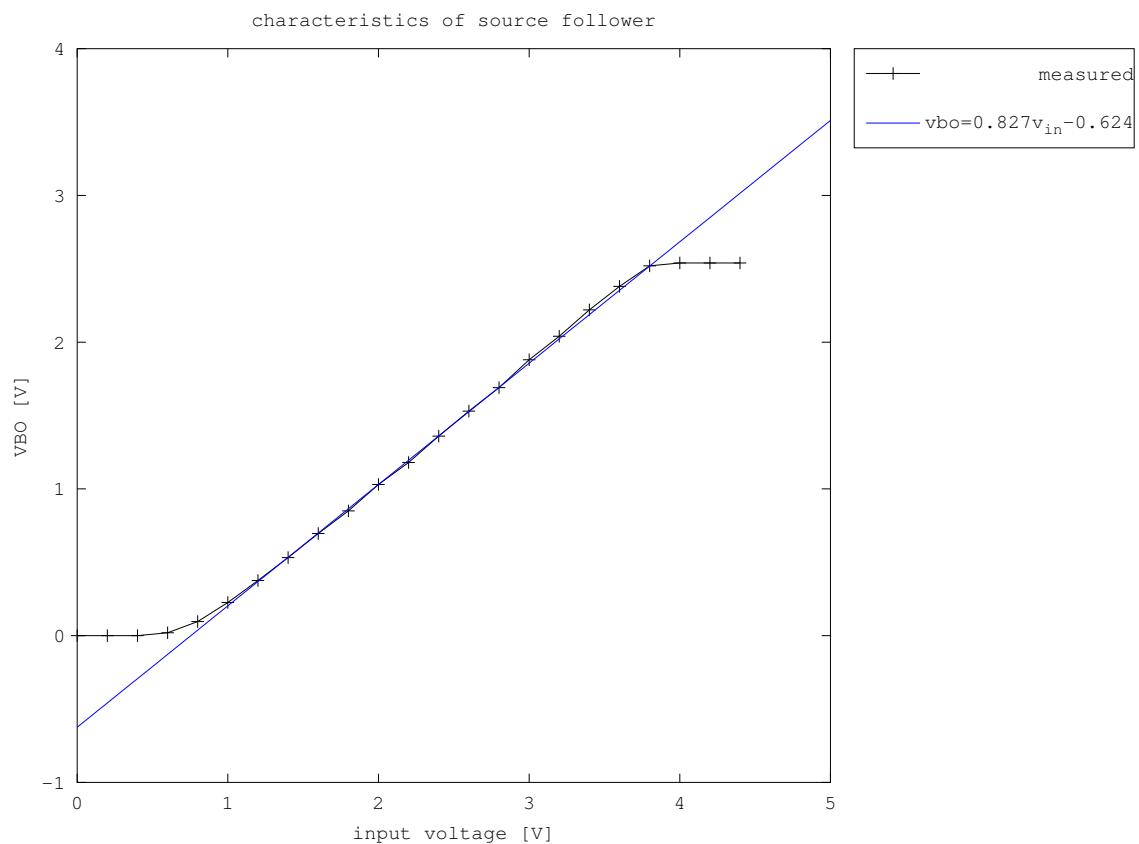


Figure 6: plot of the input voltage against VBO. This plot shows the characteristics of the voltage follower

2.3 Standard performance

This test aims to address the basic relationship between input current and output voltage. Figure 7 shows the setup used for this test. Channel 8 was used, so the end of the $20 M\Omega$ resistor is connected to IN[8], and probes are connected to OUT[8] and VBO[8].

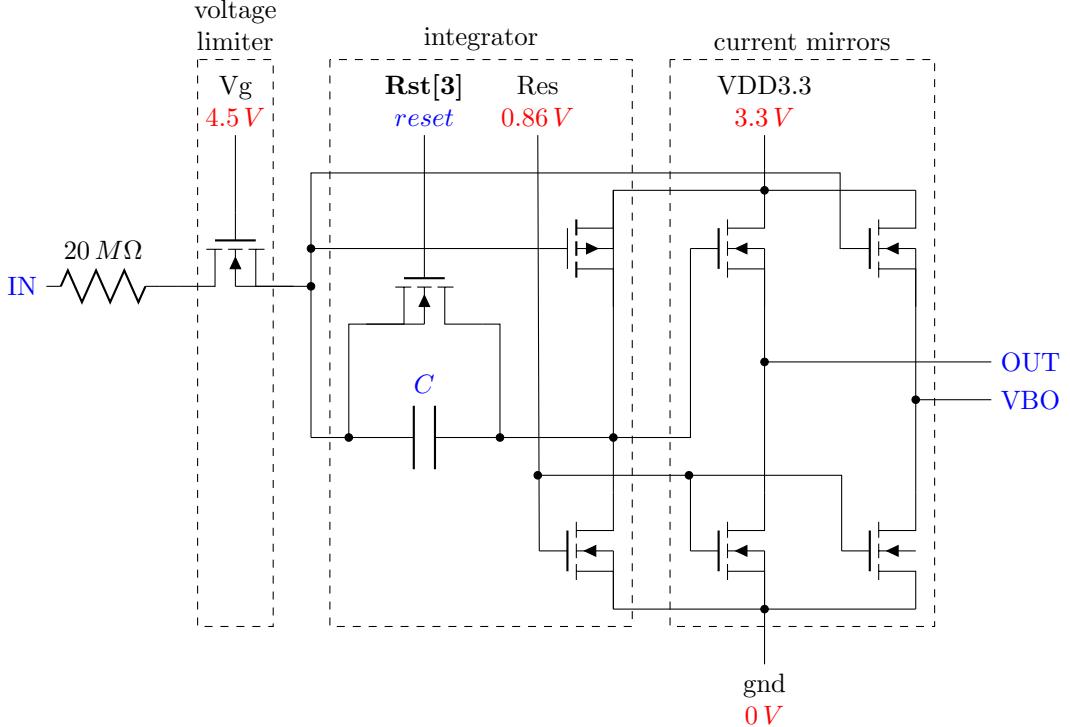


Figure 7: Schematic of ROIC channel template

Figure 8 shows the time versus voltage plot of both the VBO and OUT for a constant input voltage. The rising and falling slopes are the VBO and OUT respectively. The timescale of this plot does not allow for much noise in VBO, but it does show some interesting results for the behavior of OUT. When the reset switches, the input node immediately loses some charge. Note that the oscilloscope matches the rising edge of the rset signal to time is $0 s$, so this drop is at $0 s$. It is interesting to observe that the slope is constant for all input voltages. The slope is much slower than the time necessary for the reset transistor to switch, so the observed slope is not limited by the reset transistor, but by the source follower that tries to keep up. This observed slope is therefore the maximum rate at which the output node can be pulled down in the current set-up. Also note that the slope gets steeper when the integrator capacitance decreases. This is to be expected. However also note that the maximum slopes across the different capacitances are all identical.

Figure 9 shows the same plot as fig. 8, but now the x axis is scaled with input current. This shows for fig. 8a and 8b that the relationship between output voltage and charge is equal across different input voltages. For fig. 8c and 8d however, one can see that the higher voltages lose this

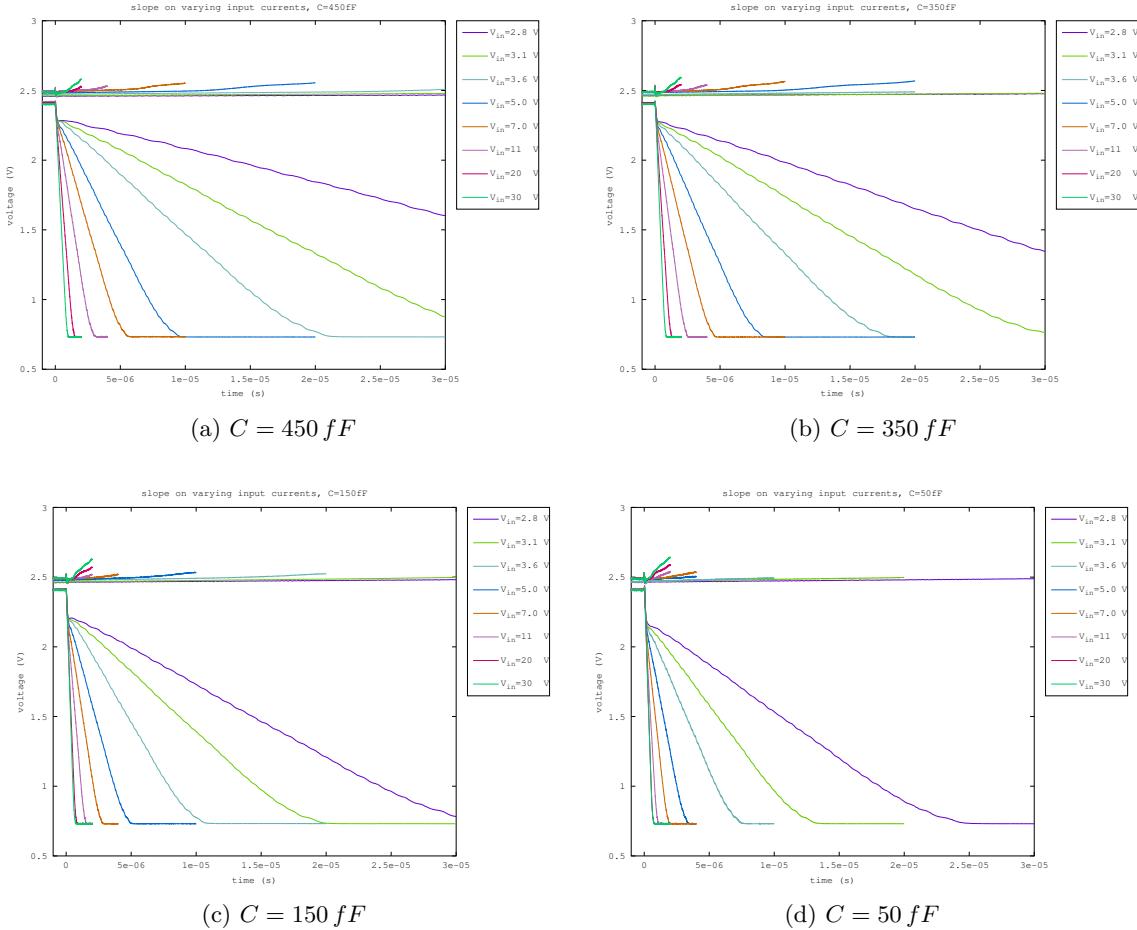


Figure 8: Expected versus measured charge up times for different input voltages. The input voltage is connected to the input through a resistor of $20 \text{ M}\Omega$

property. Another interesting observation is that when one looks closely at the plot, one can observe a small oscillation with a period that is constant with charge. Also the period is constant across different voltages. A hypothesis explaining this behavior has yet to be found.

Figure 10 shows the $\delta Q/\delta V$ against charge plots. Note that $\delta Q/\delta V$ is the capacitance. One can observe that while the capacitance is charging, the full value of the capacitance can be observed, and when the capacitance is completely discharged, it behaves as if it is not there. One can use these plots to estimate the integration capacitance. The capacitance for fig. 9a, 9b, 9c and 9d are approximately 450 fF , 350 fF , 220 fF and 180 fF respectively.

Figure 11 shows $\delta V/\delta t$ against input voltage for all capacitances. One can observe that all four have different slopes at first, but there appears to be a trend that they all converge to a value of $\delta V/\delta t \approx 3.2 \cdot 10^6$.

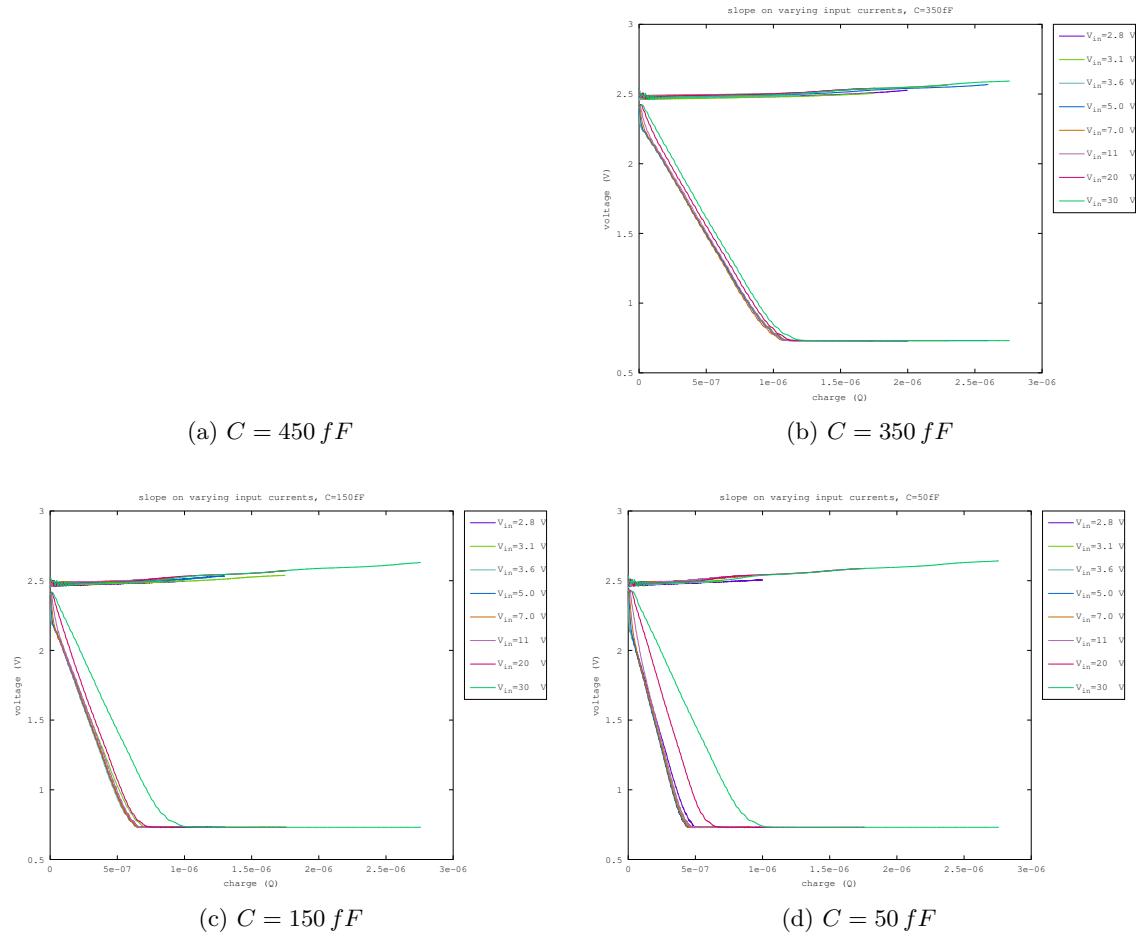


Figure 9: This plot is showing charge versus voltage

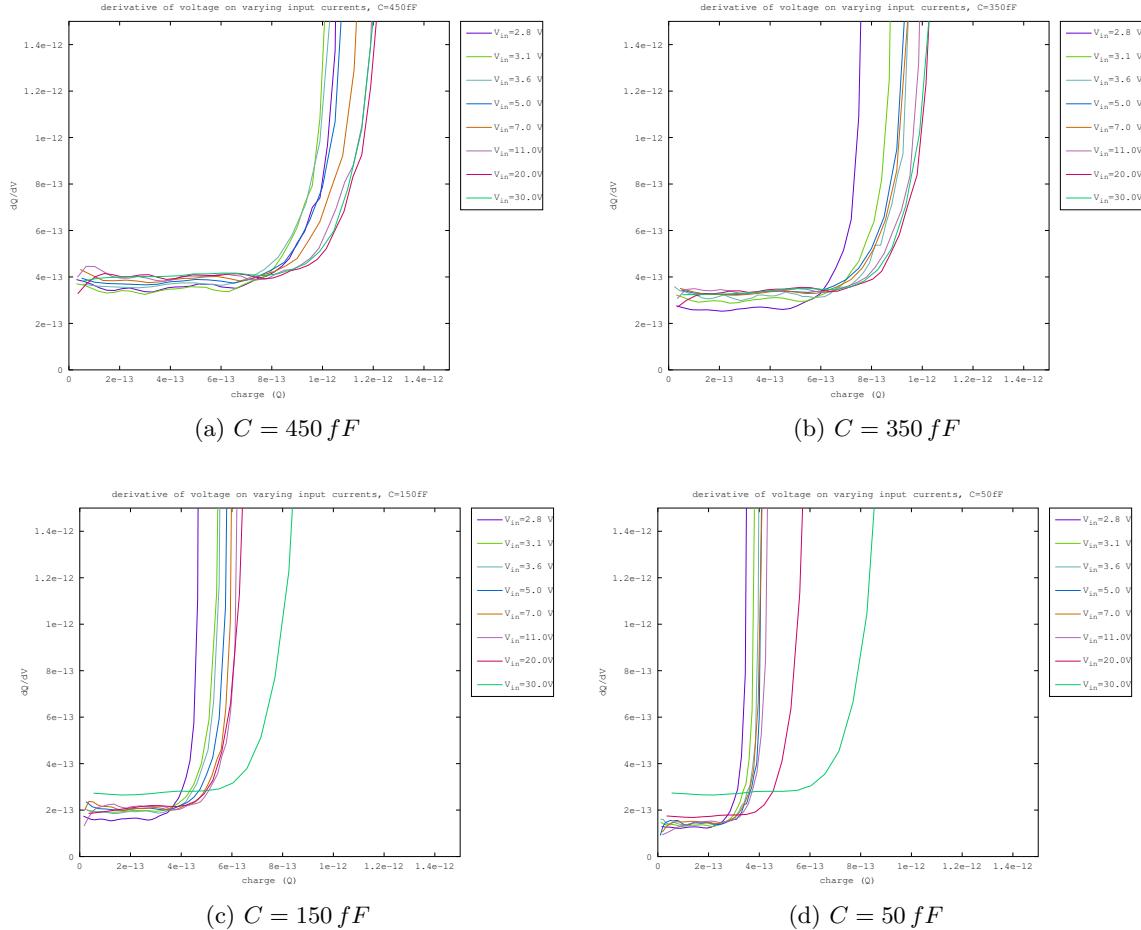


Figure 10: The plot shows dv/dt against time. The plot is in log scale, which allows for an easy read on the maximum slope and the time needed to discharge the integrator capacitance.

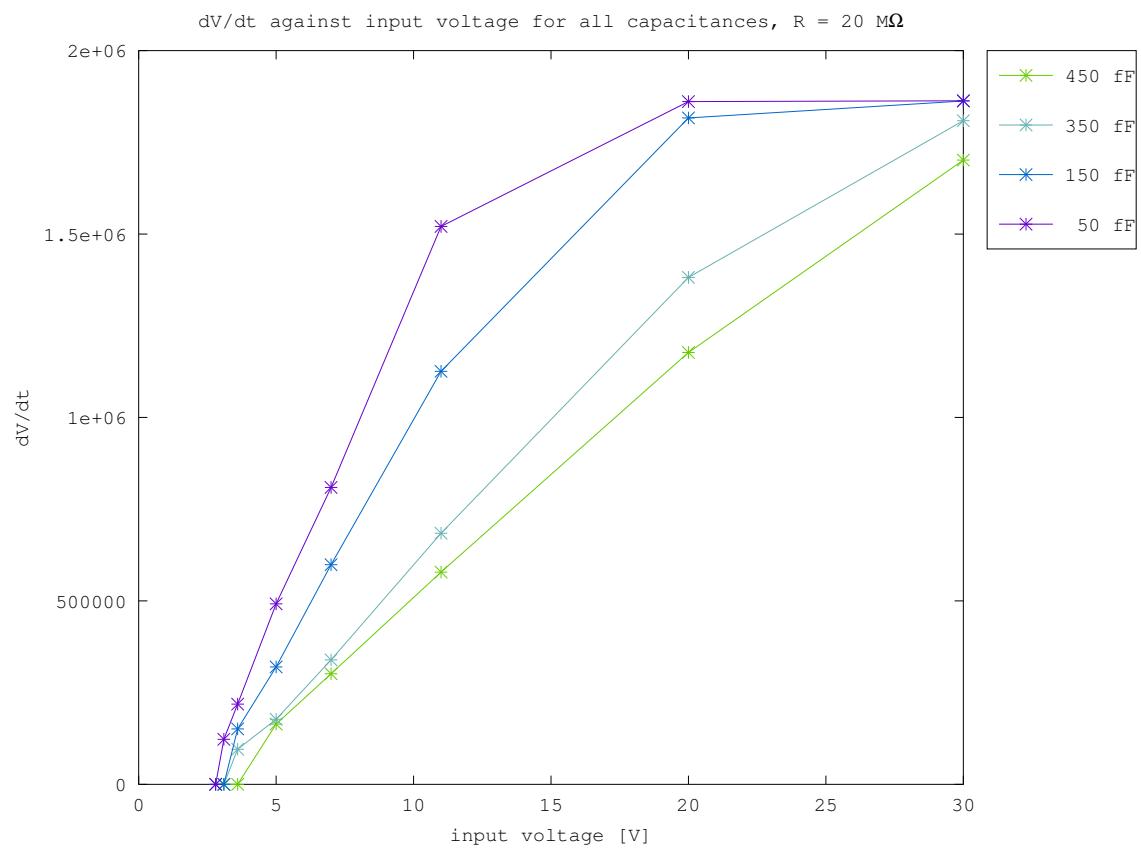


Figure 11: dV/dt against input voltage for all four capacitances. The x indicate the measurements.

2.4 large current performance

In this section the $20 M\Omega$ input resistor is replaced with a $4 M\Omega$ resistor. The main goal is to observe the ROIC for very large currents.

Figure 12 shows the same plot as fig. 8, but this time with larger currents. Where a minimum slope could be observed at fig. 8, it is more prevalent here. This also shows more information about the behavior of VBO. For small voltages the VBO does not increase, but as the voltages get larger, one can observe that the voltages of VBO start rising when the OUT is done with discharging. It is also interesting to note that VBO seems to be not affected by the minimum slope at OUT. This gives rise to the hypothesis that the OUT is limited by the source follower.

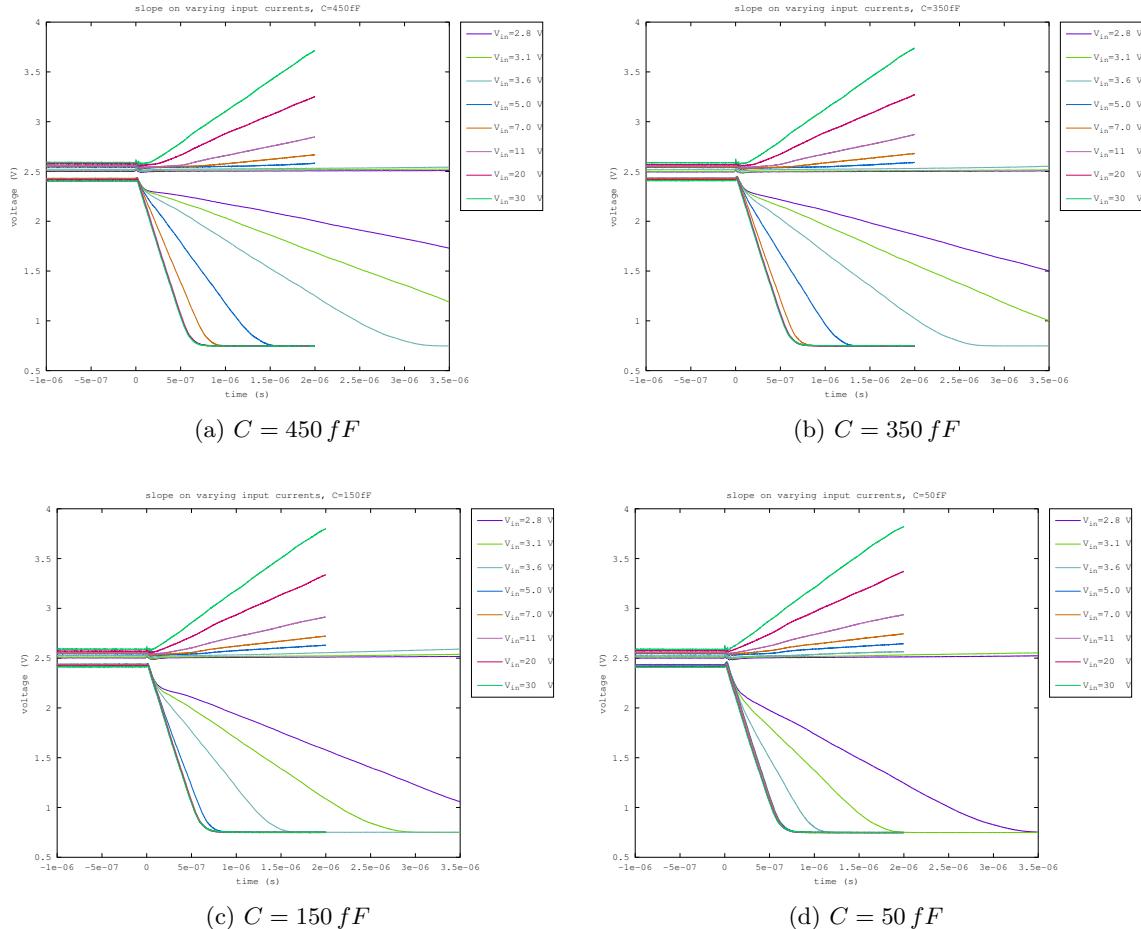


Figure 12: Expected versus measured charge up times for different input voltages. The input voltage is connected to the input through a resistor of $4 M\Omega$

Figure 13 shows a similar plot as in fig. 9 but with higher currents. In fig. 9 one could observe that all currents fitted to the same line, but deviated at higher currents. This effect is also observed here, but in a stronger form. Which is to be expected.

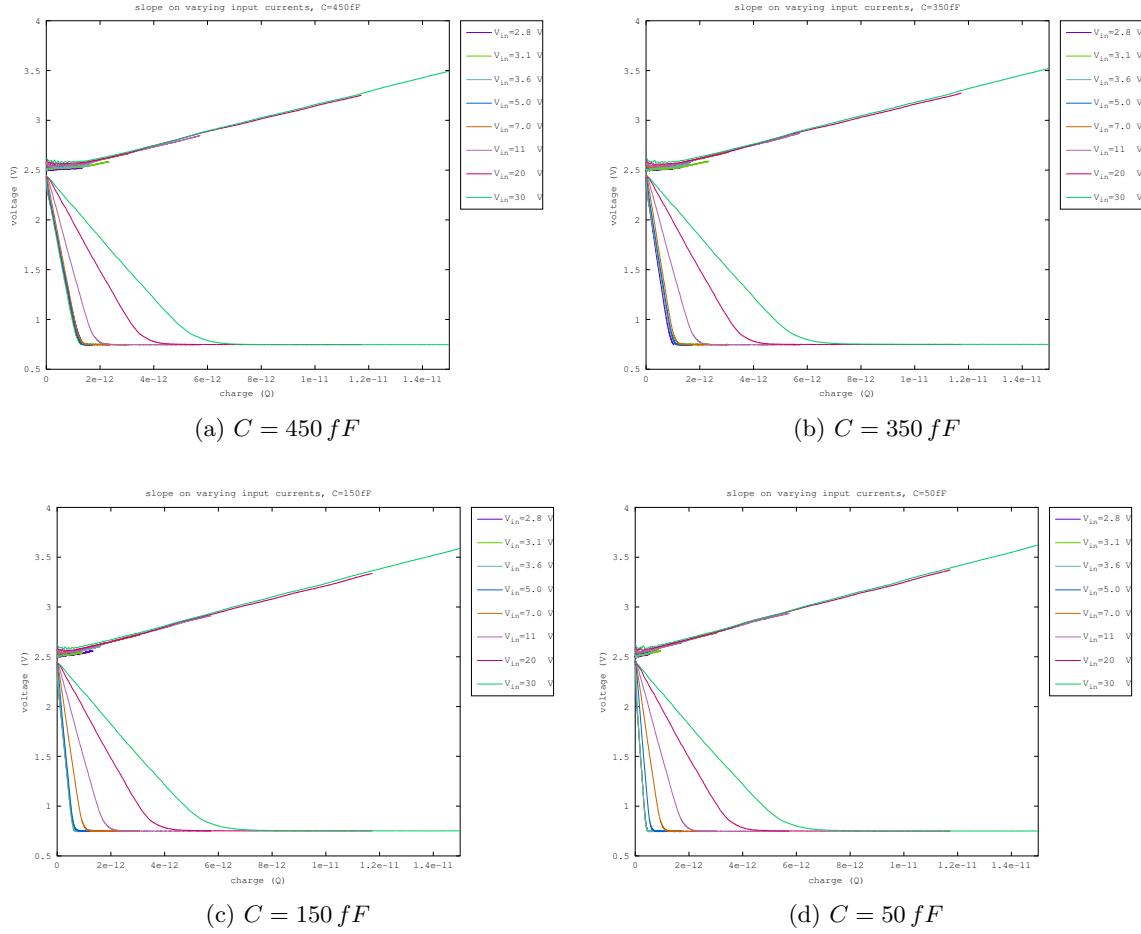


Figure 13: This plot is showing charge versus voltage

Figure 14 shows a plot of $\delta V/\delta Q$ against charge. Note that the behavior for the low voltages differ across the different capacitances, but that the high voltages are not affected by a change in capacitance. This observation agrees with the hypothesis that the output is not limited by the input current, but by the speed of the source follower at the output.

Figure 15 shows the same plot as fig. 11, but with higher current. This plot clearly shows that all four capacitance configurations saturate at a $\delta V\delta t \approx 3.1 \text{ V}$. This cannot be a limit applied to the input, because the capacitances are different. Therefore the output is limiting this, conform previous observations.

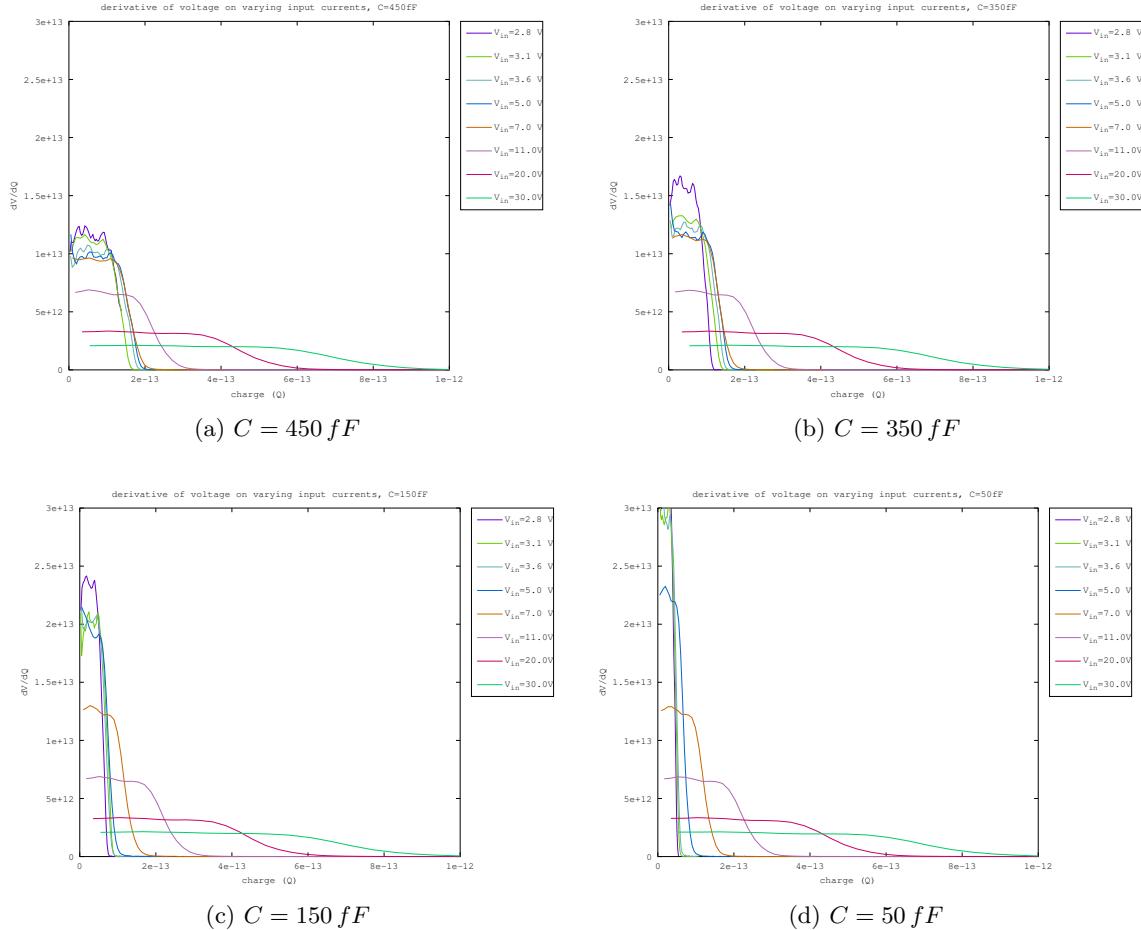


Figure 14: The plot shows dv/dt against time. The plot is in log scale, which allows for an easy read on the maximum slope and the time needed to discharge the integrator capacitance.

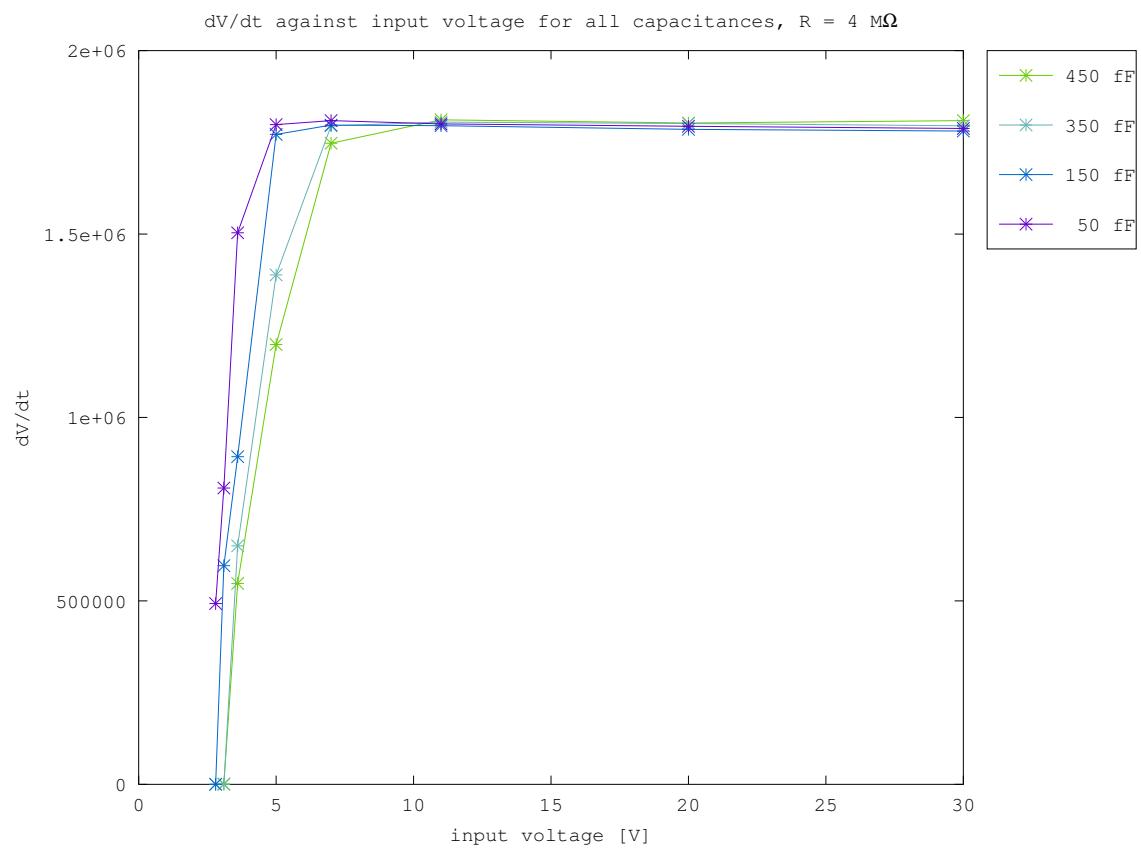


Figure 15: dV/dt against input voltage for all four capacitances. The x indicate the measurements.

2.5 Voltage limiter

This section focusses on the output of the source follower that is directly connected to the output of the high voltage transistor connected to the input of the ROIC. The setup is identical to section 2.3, but the time scale is different to observe the slower behavior of VBO.

Figure 16 shows the time against voltage plot. This are a couple of important observations that can be made from these plots. First and foremost: the behavior of the VBO is almost not affected by the capacitance. The behavior is fairly similar. There is a difference however, in that the VBO starts rising as the OUT reaches zero. This means that the VBO for 450 fF is slightly delayed when compared to 50 fF for example. It is also interesting to observe that VBO never increases above 2.6 V . This behavior is most likely due to the high voltage input transistor doing its job as a current limiter. Finally one can observe that for very low currents, VBO does not reach 2.6 V . The reason for this is that the input reaches the voltage level of the power supply before the current limiter kicks in.

Figure 17 shows the plots of voltage against charge. One can observe that increasing the current causes the behavior to converge to a line with a linear slope that is constant with Q , and a saturation at 2.6 V .

Figure 18 shows $\delta V/\delta Q$ for the VBO. The main observation one can make from these plots is that the behavior of VBO is almost entirely unaffected by the integration capacitance.

Figure 19 shows the $\delta V/\delta t$ against input voltage for VBO across all capacitances. For large voltages seem to behave in a normal linear fashion. The startup shows a scene that looks as if the 450 fF and 350 fF setup behave identical, and that the 150 fF and 50 fF setup behave identical. This might be due to the lack of measurement points, but is worth investigating further.

Figure 25 shows the relationship between V_g and the voltage limit posed by the high voltage transistor at the input.

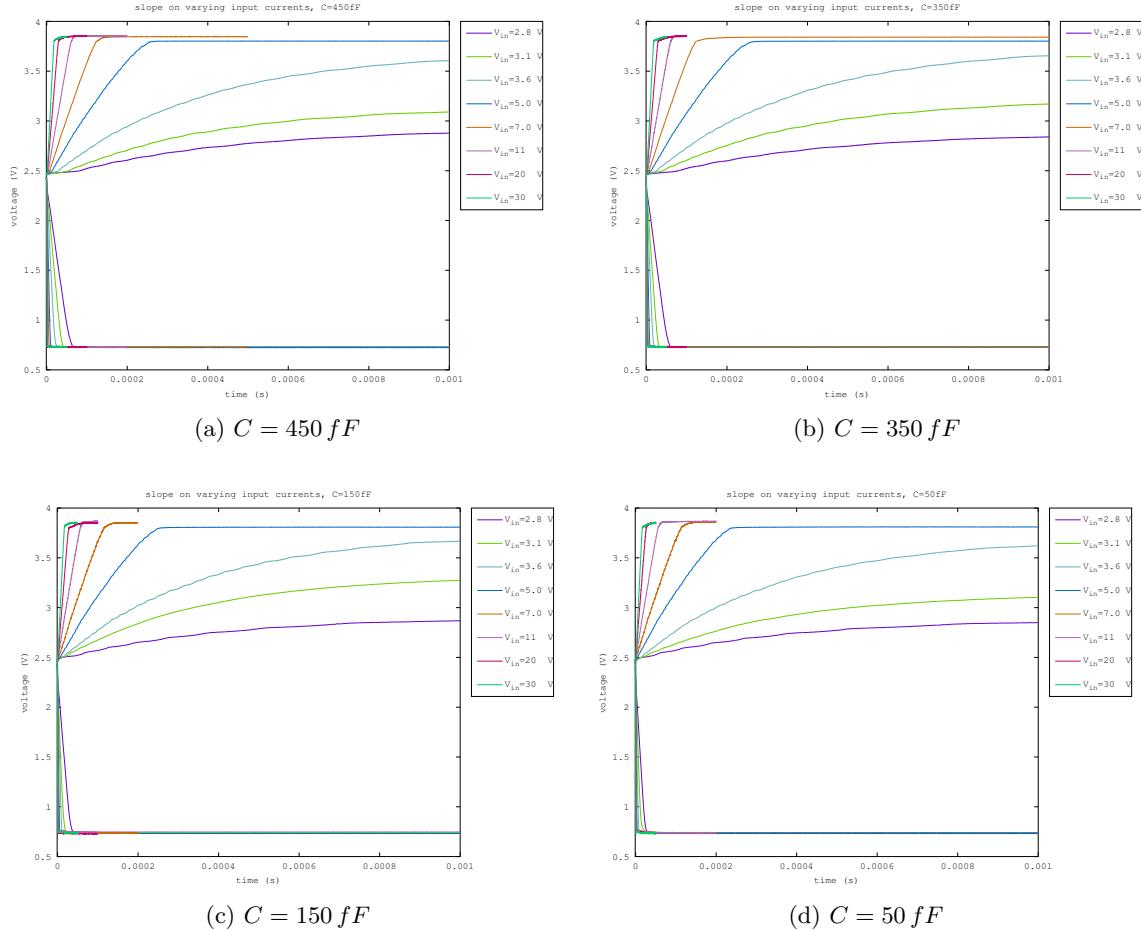


Figure 16: Expected versus measured charge up times for different input voltages. The input voltage is connected to the input through a resistor of $20 \text{ M}\Omega$

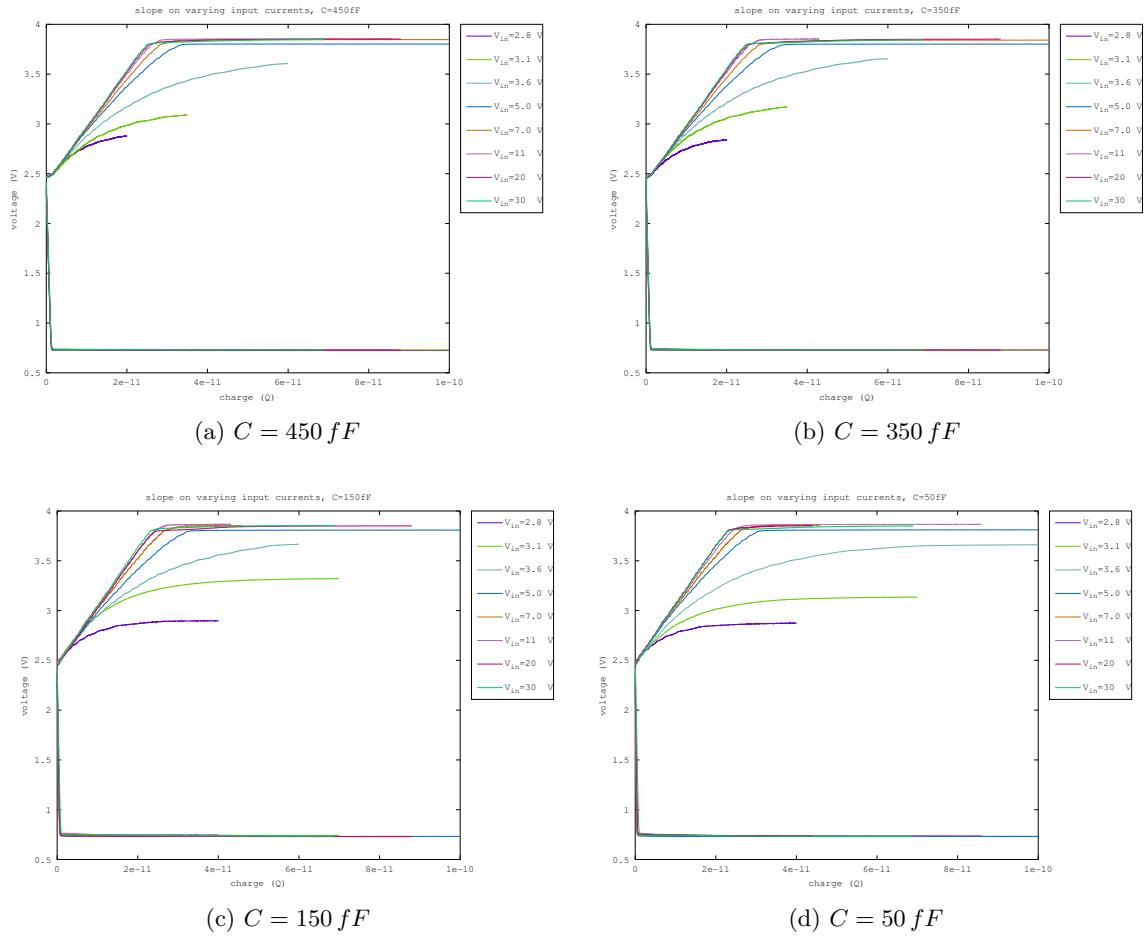


Figure 17: This plot is showing charge versus voltage

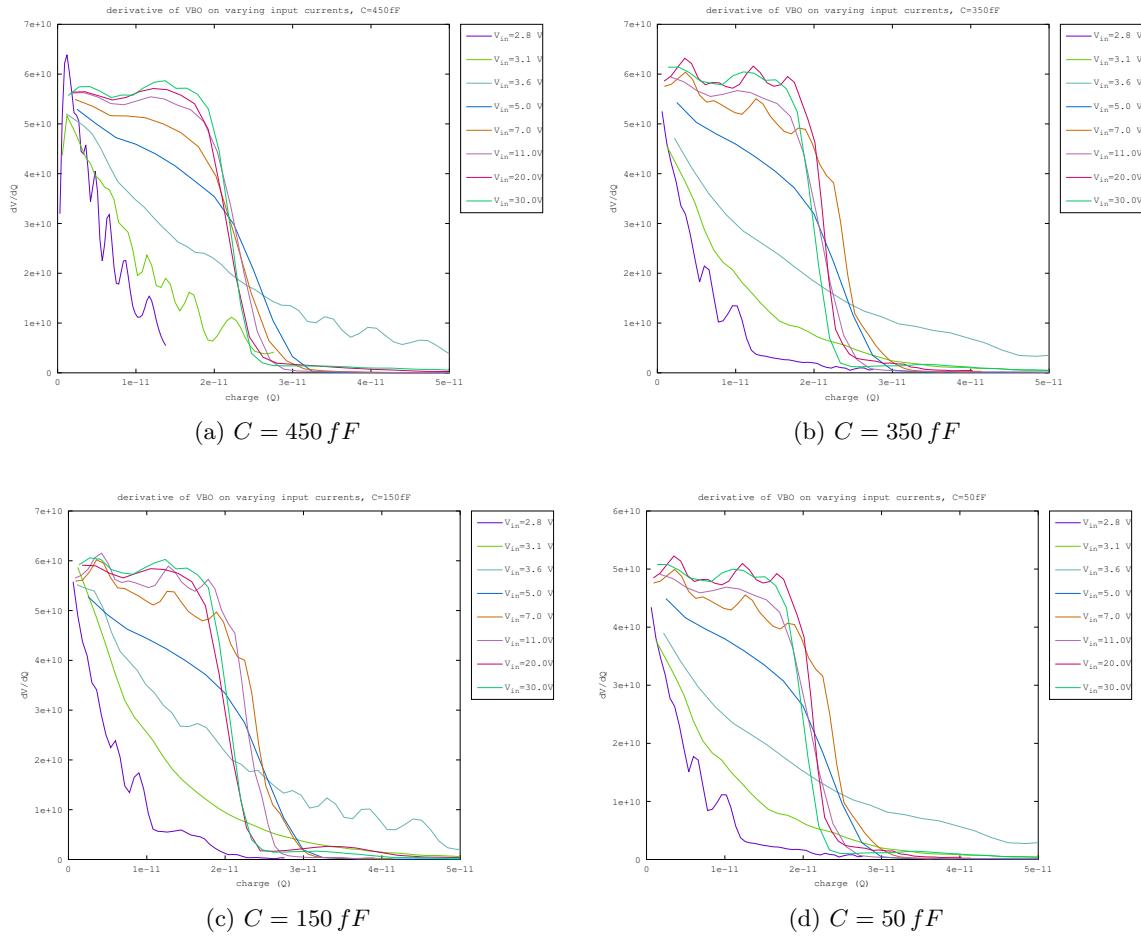


Figure 18: The plot shows dv/dt against time of the vbo.

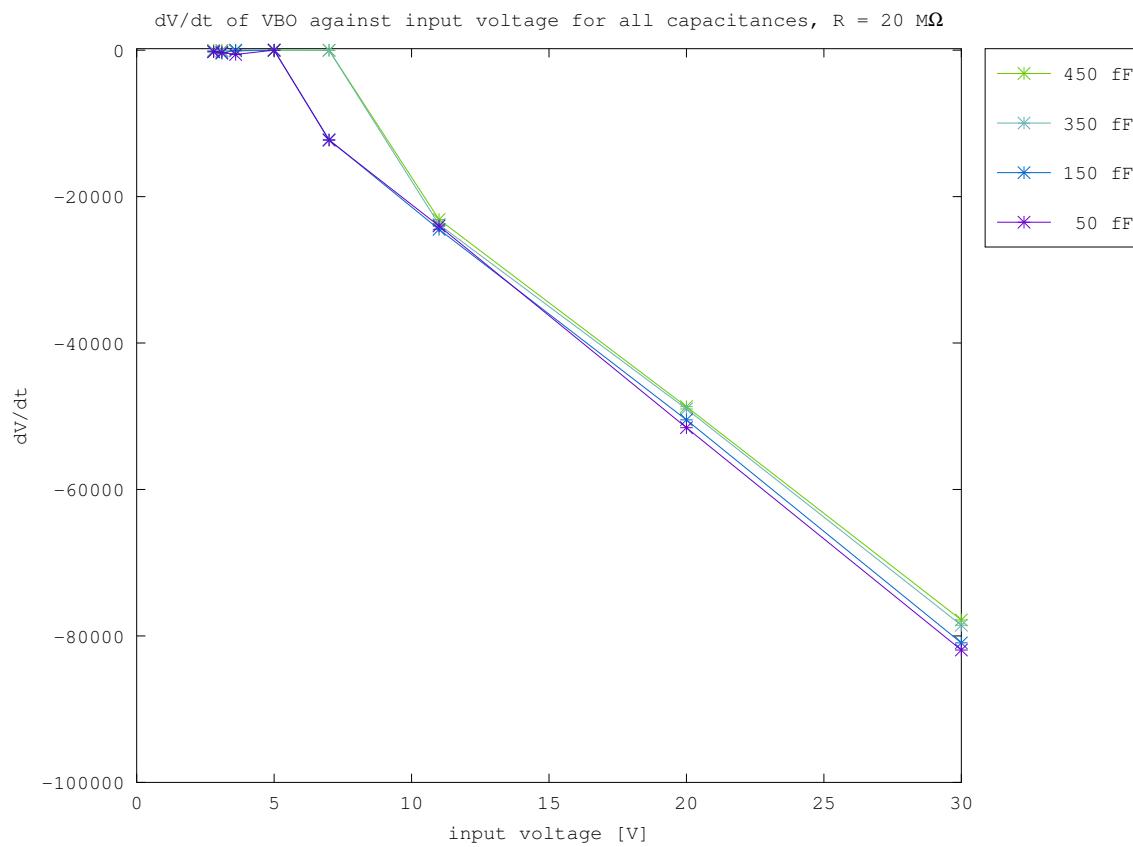


Figure 19: dV/dt of VBO against input voltage for all four capacitances. The x indicate the measurements.

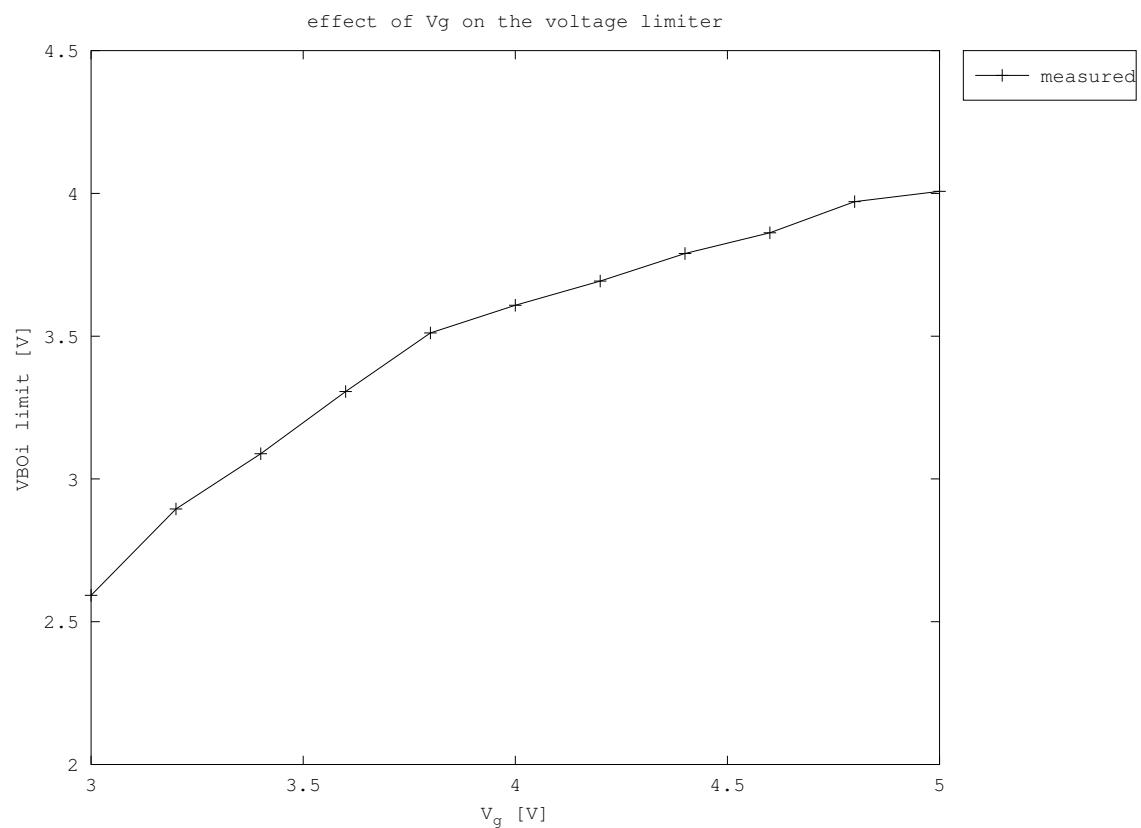


Figure 20: voltage limit as a function of V_g

3 Characterization of GaN sensors

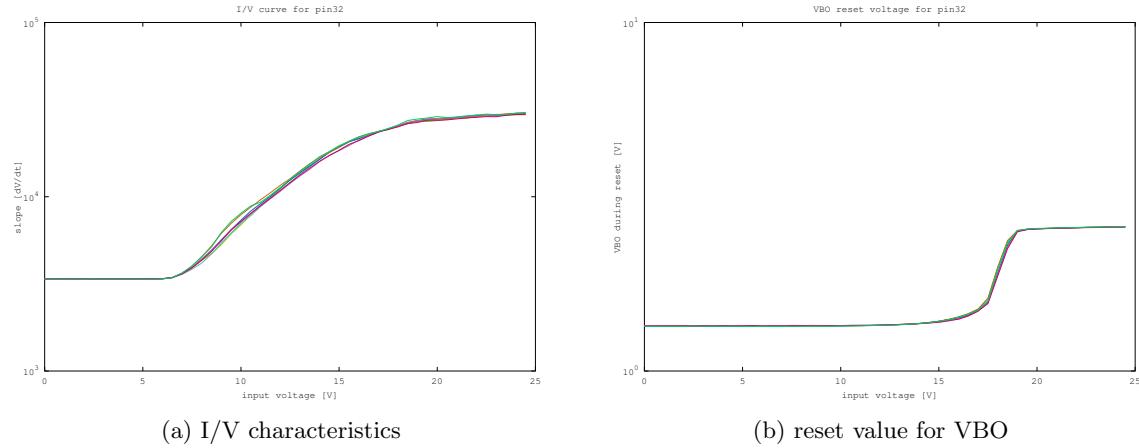


Figure 21: The slope and reset values for the VBO of pin32 repeated multiple times to test variance across measurements

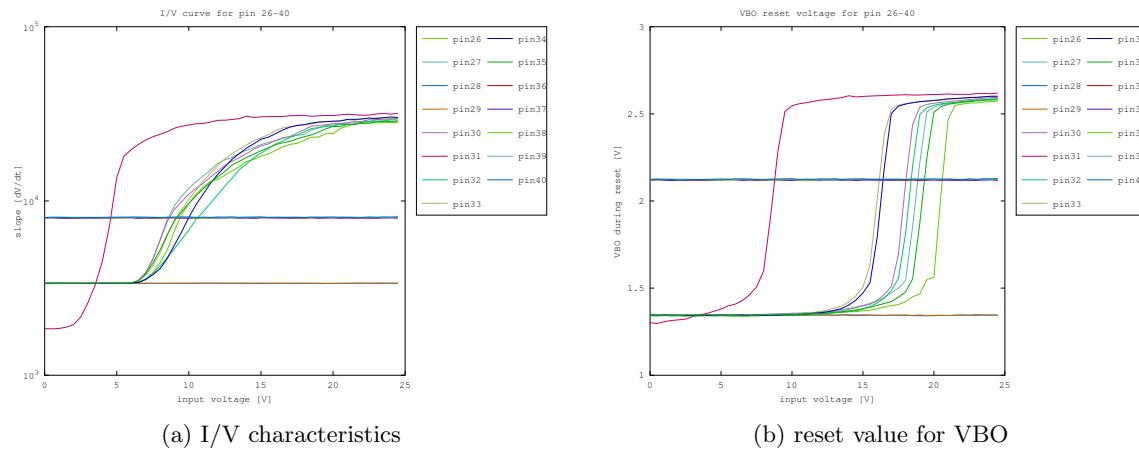


Figure 22: The slope and reset values for the VBO of pin26-40

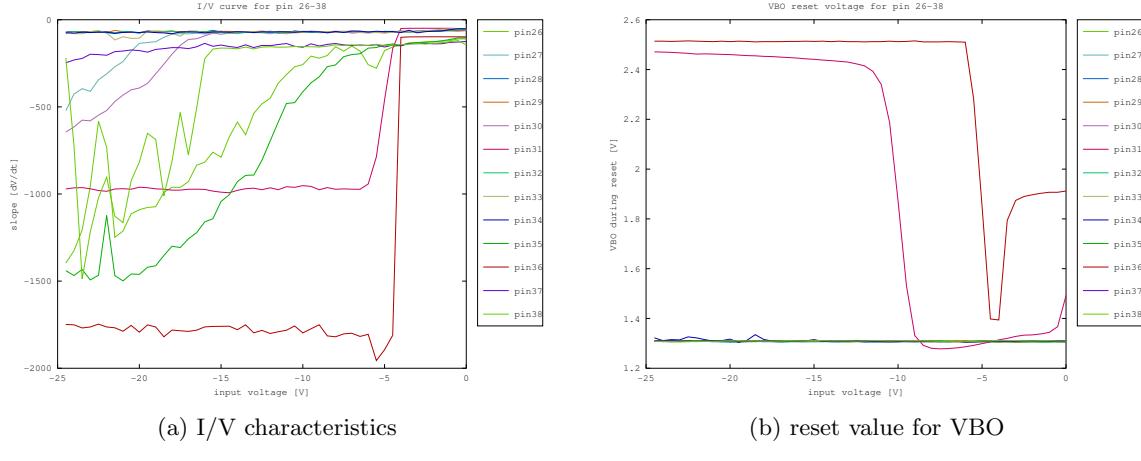


Figure 23: The slope and reset values for the OUT of pin26-38

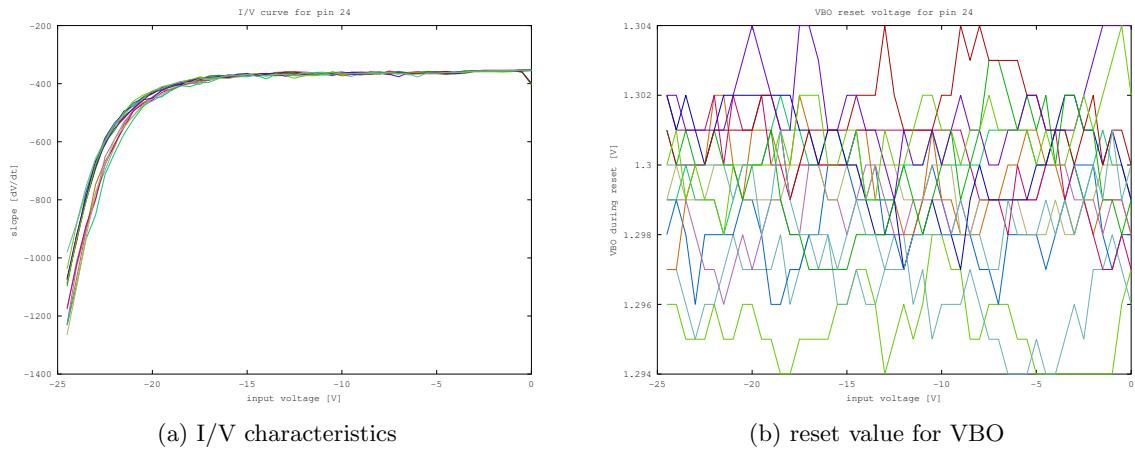


Figure 24: The slope and reset values for the OUT of pin24

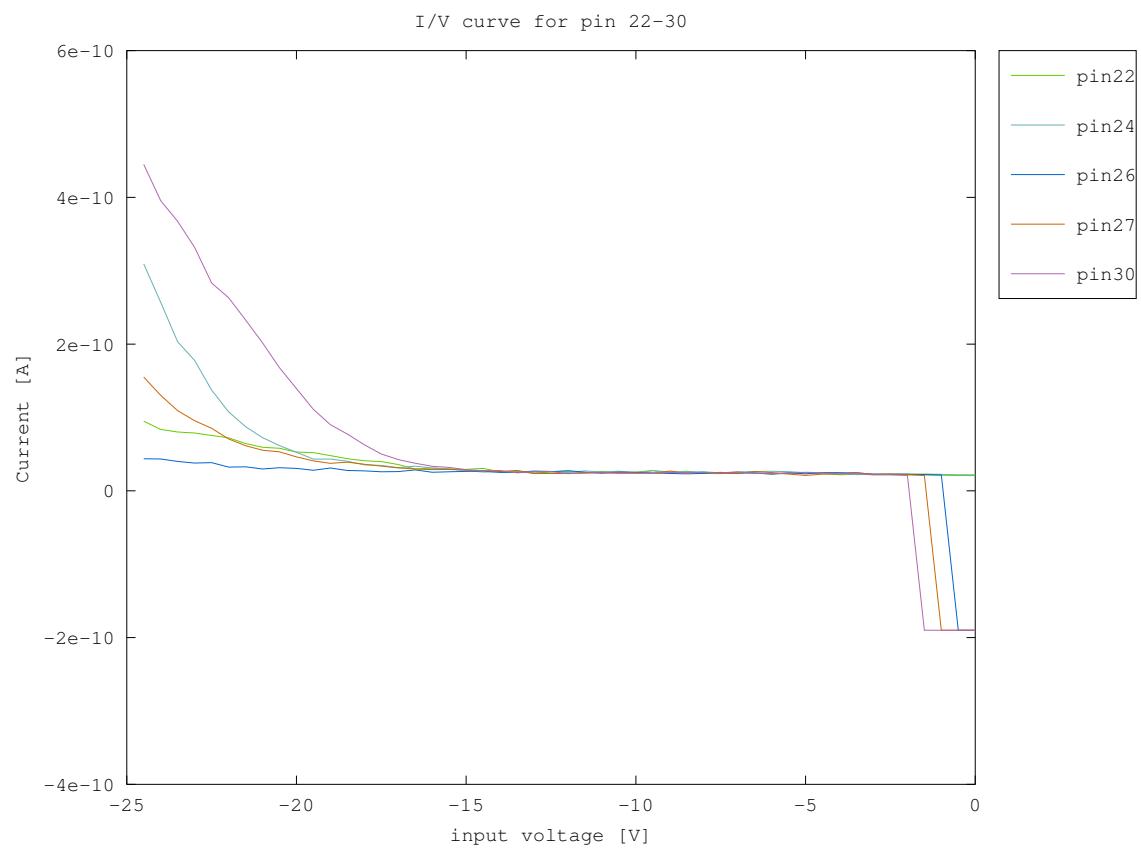


Figure 25: voltage limit as a function of Vg