

Preethis ROIC analysis

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1 setup

3.0.1a

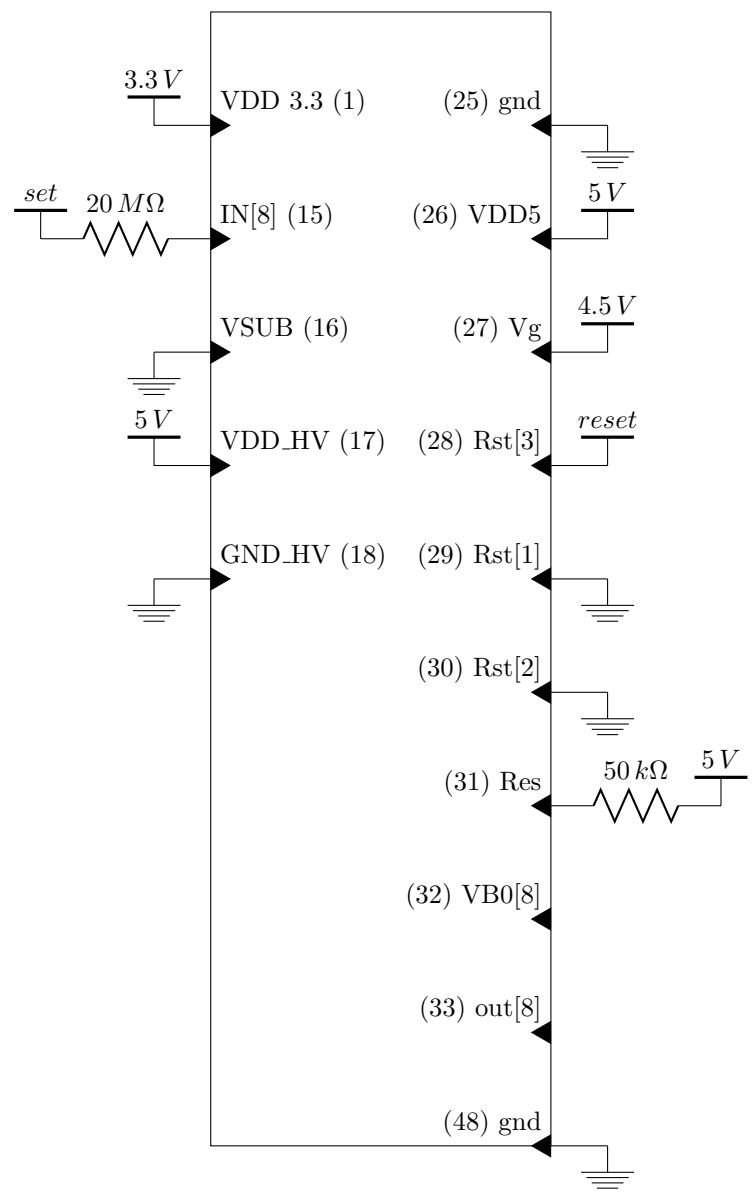


Figure 1: Schematic of breadboard

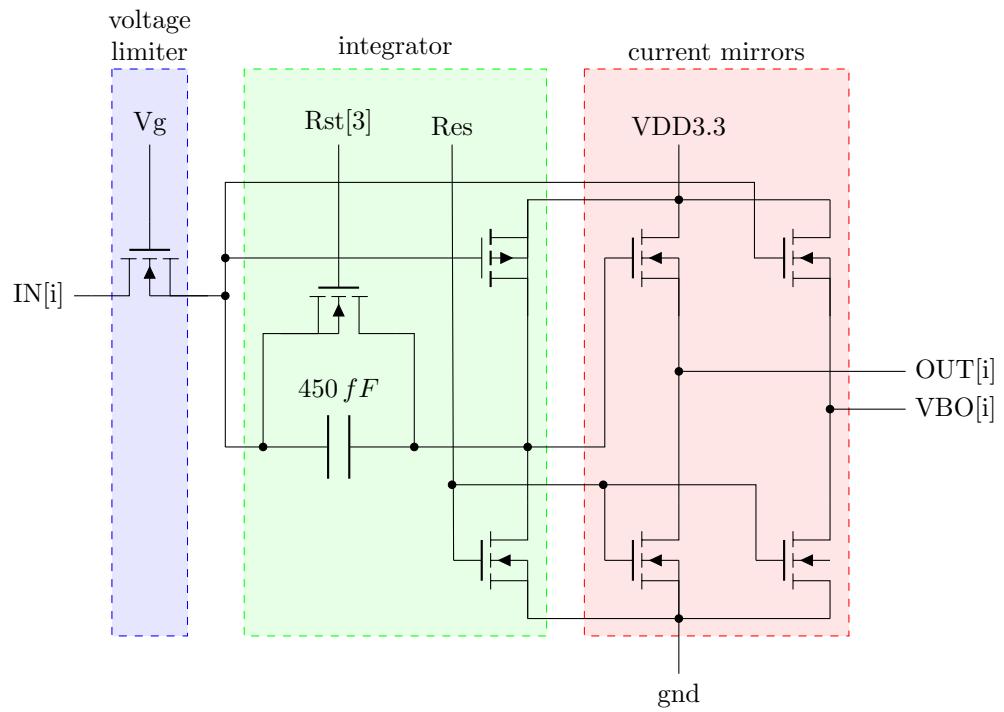


Figure 2: Schematic of ROIC channel

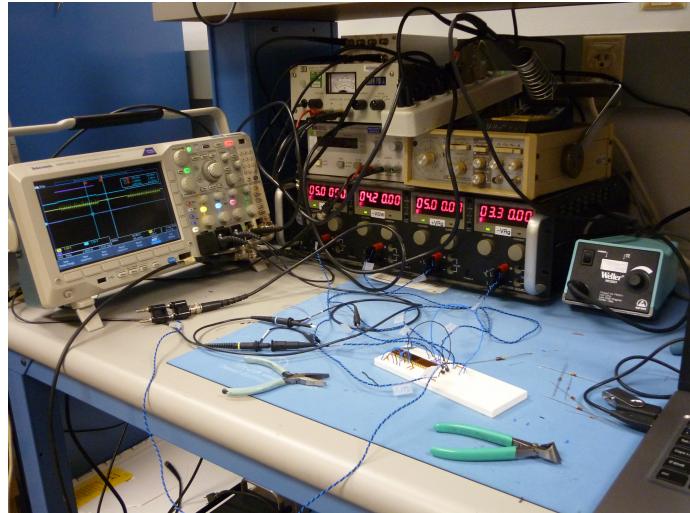


Figure 3: setup overview

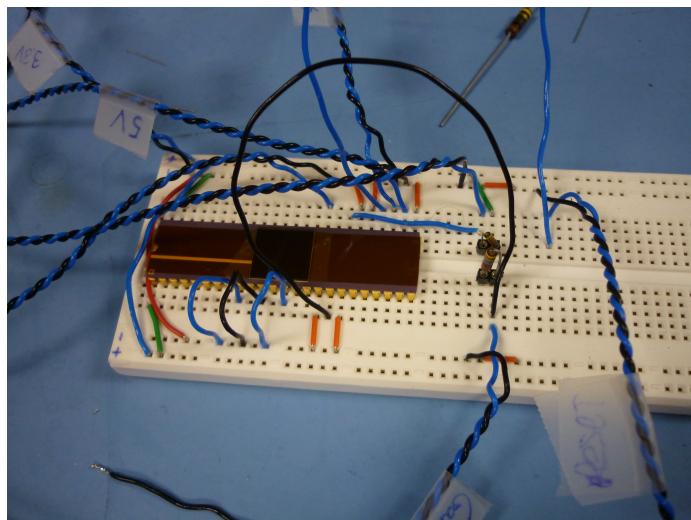


Figure 4: close-up

2 Reset mode

This test addresses the behavior of the circuit in reset mode.

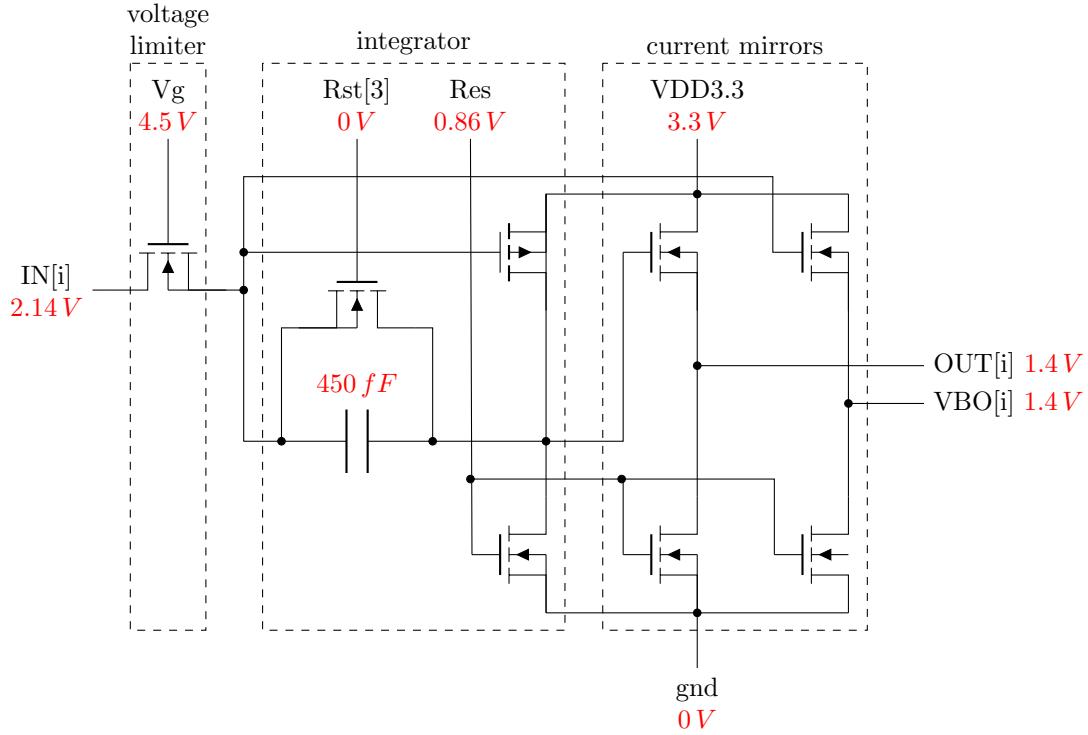


Figure 5: Schematic of ROIC channel template

3 Normal operation mode

This test aims to observe the integration process. It was quite a tedious process to get this to work. It turned out that the amount of current supplied was several orders of magnitude off. To limit the input channel the V_g was reduced to 2.5 V . The result of this is a nice integration that can be observed for several specific input voltages. Note that the plotted IN , is the actual voltage at the input of the ROIC, and the listed IN at the title of the plot is the voltage supply connected to a $20\text{ M}\Omega$ resistor to the input of the ROIC.

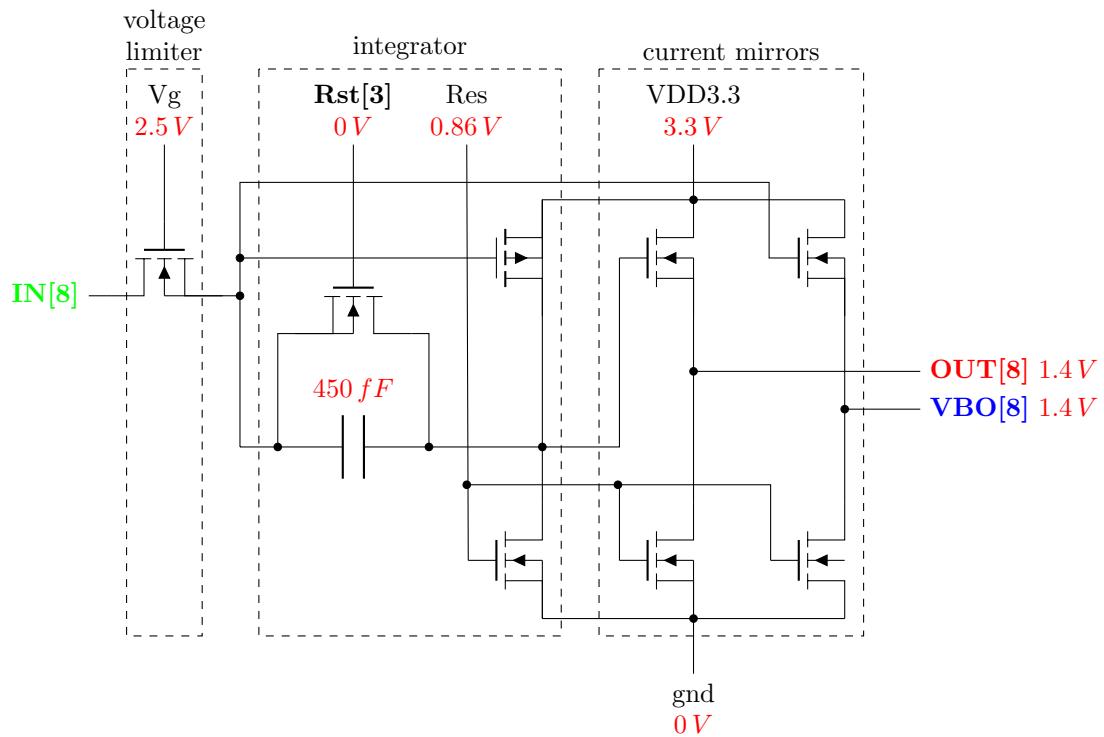


Figure 6: Schematic of ROIC channel template

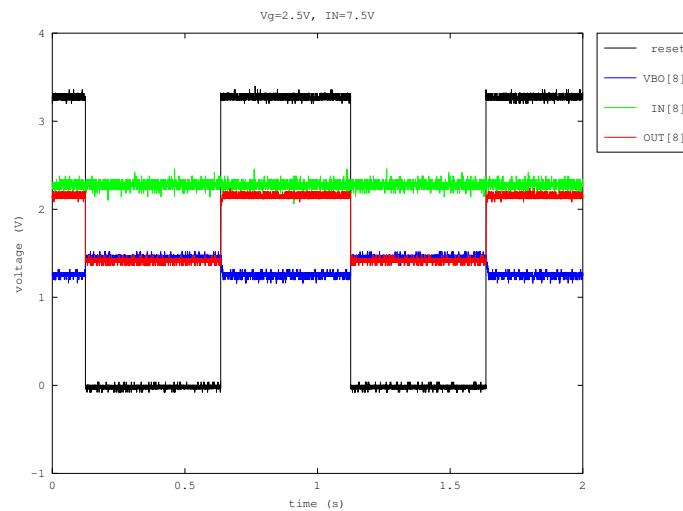


Figure 7: Behavior of a single channel at a lowered V_g

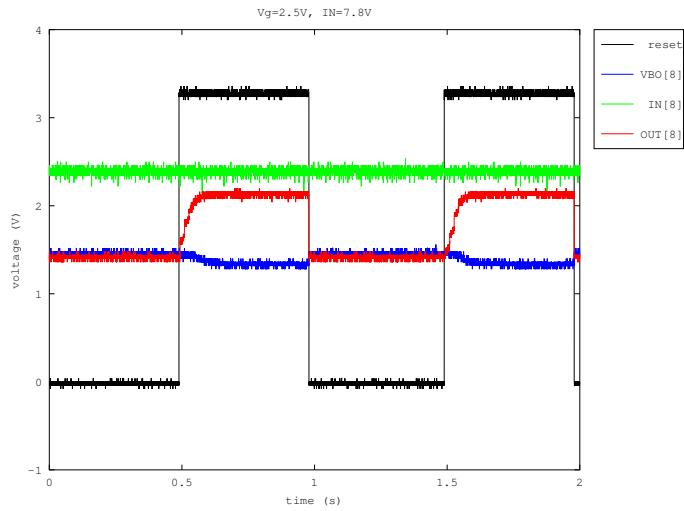


Figure 8: Behavior of a single channel at a lowered V_g

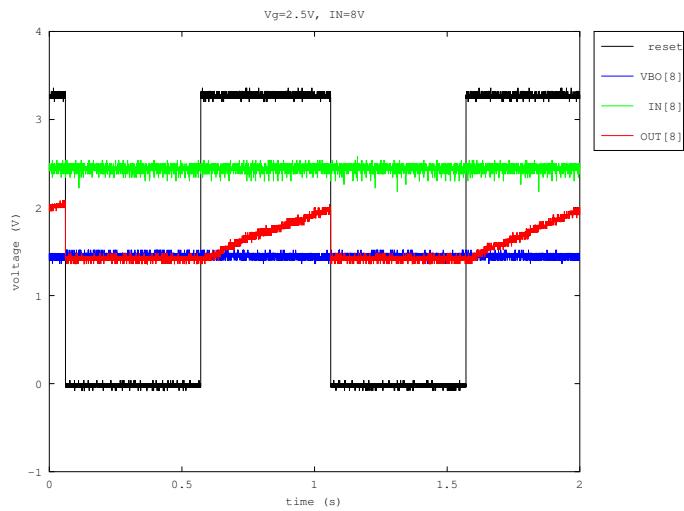


Figure 9: Behavior of a single channel at a lowered V_g

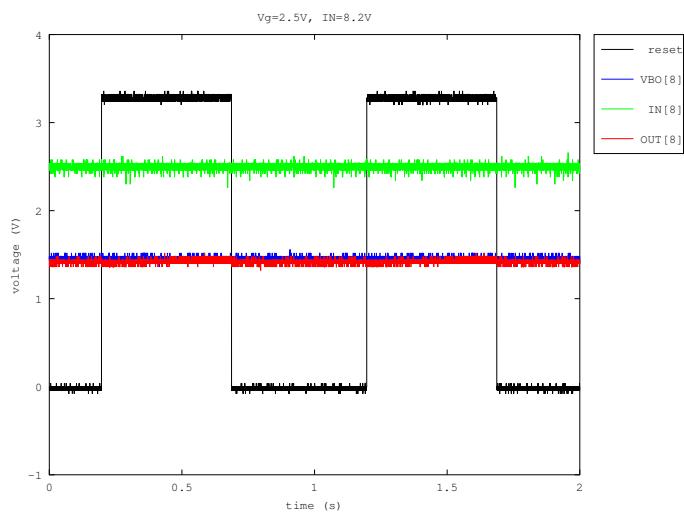


Figure 10: Behavior of a single channel at a lowered V_g