

Preethis ROIC analysis

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1 setup

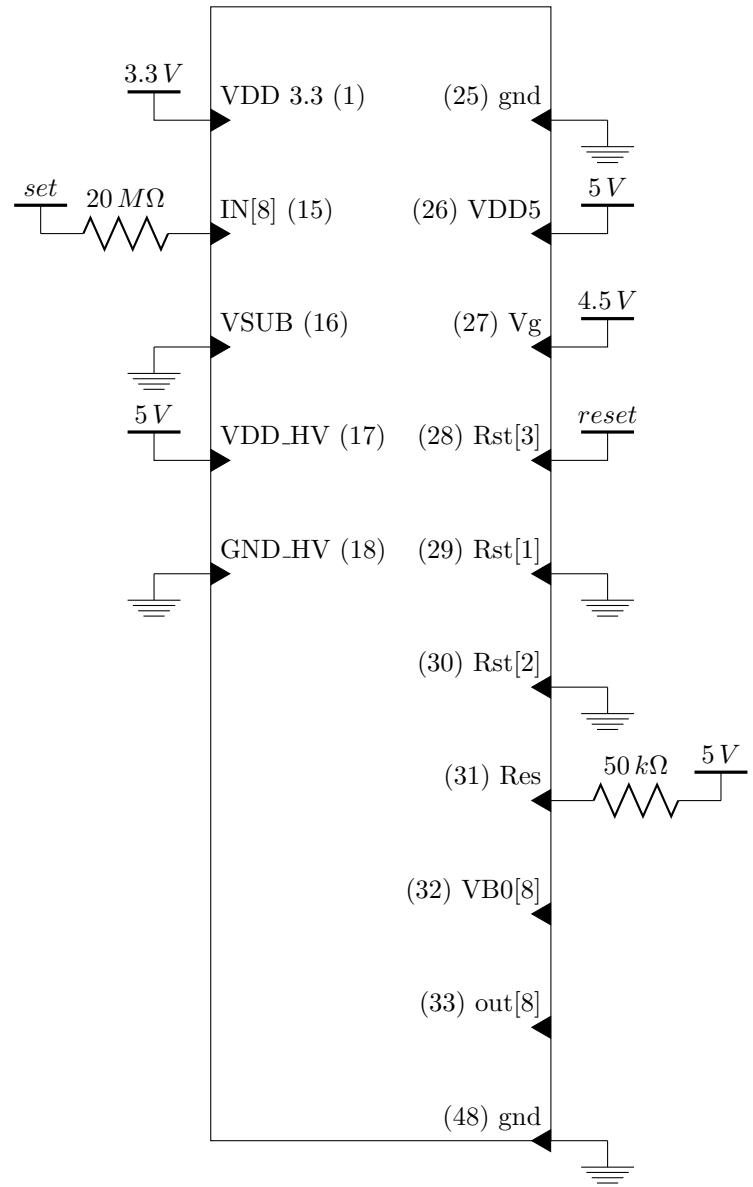


Figure 1: Schematic of breadboard

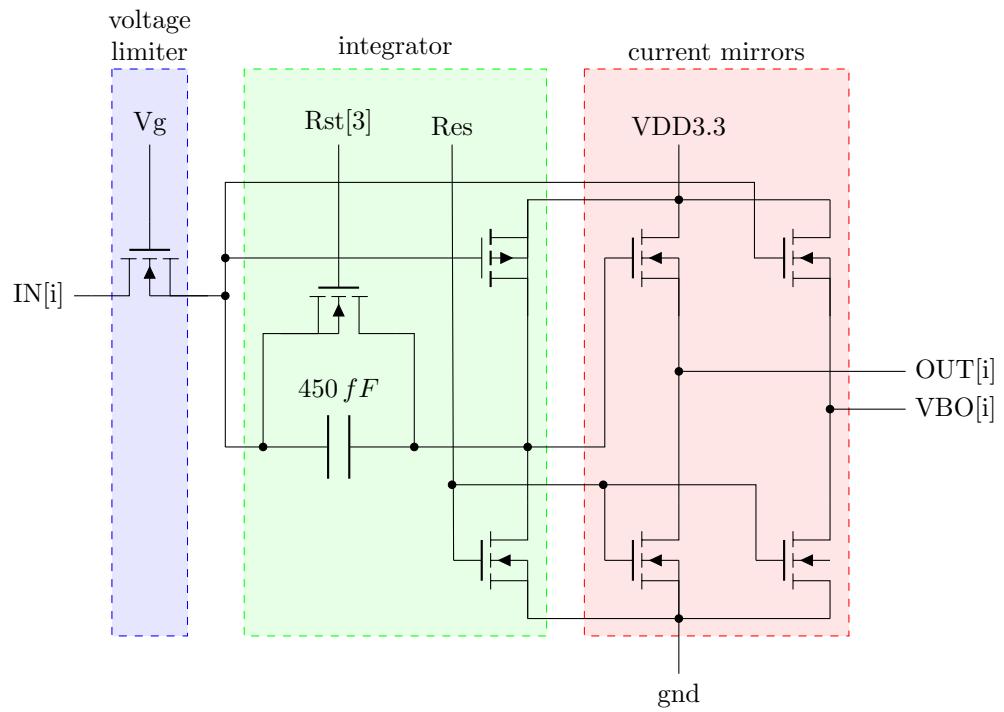


Figure 2: Schematic of ROIC channel

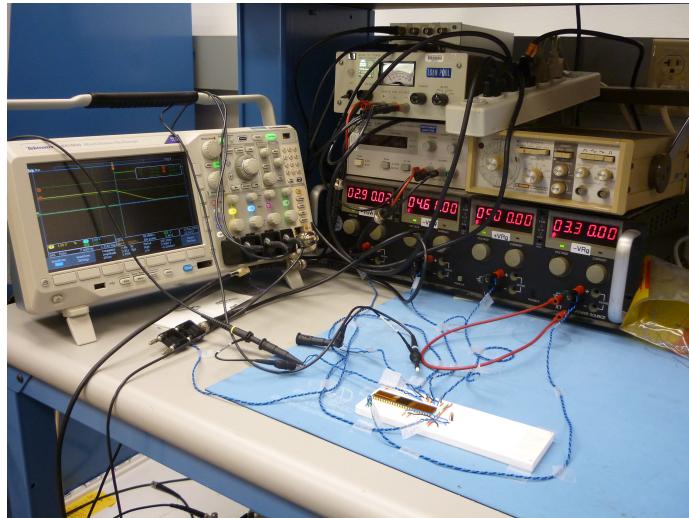


Figure 3: setup overview

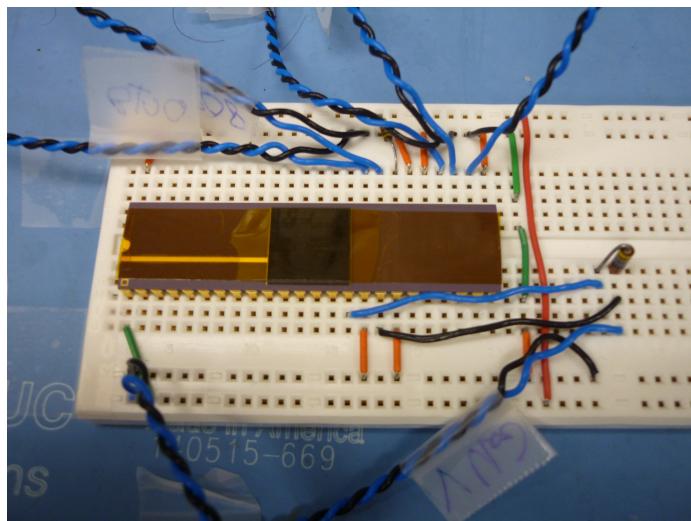


Figure 4: close-up

2 Reset mode

This test addresses the behavior of the circuit in reset mode. Figure 5 shows the measured values during reset mode. Note that the input voltage is 2.4 V, which is important when calculating the input current.

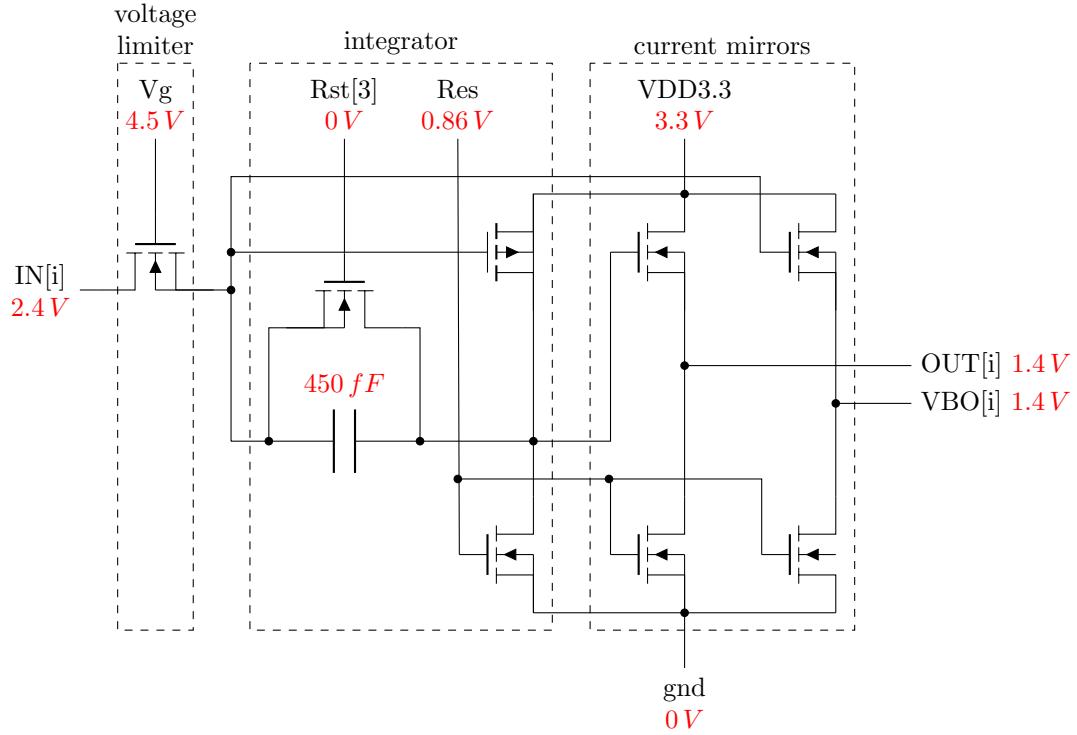


Figure 5: Schematic of ROIC channel template

3 Integrator

This section aims to address the performance of the integrator. Figure 6 shows the setup used for this test. Channel 8 was used, so the end of the $100\text{ M}\Omega$ resistor is connected to IN[8], and the probe is connected to OUT[8].

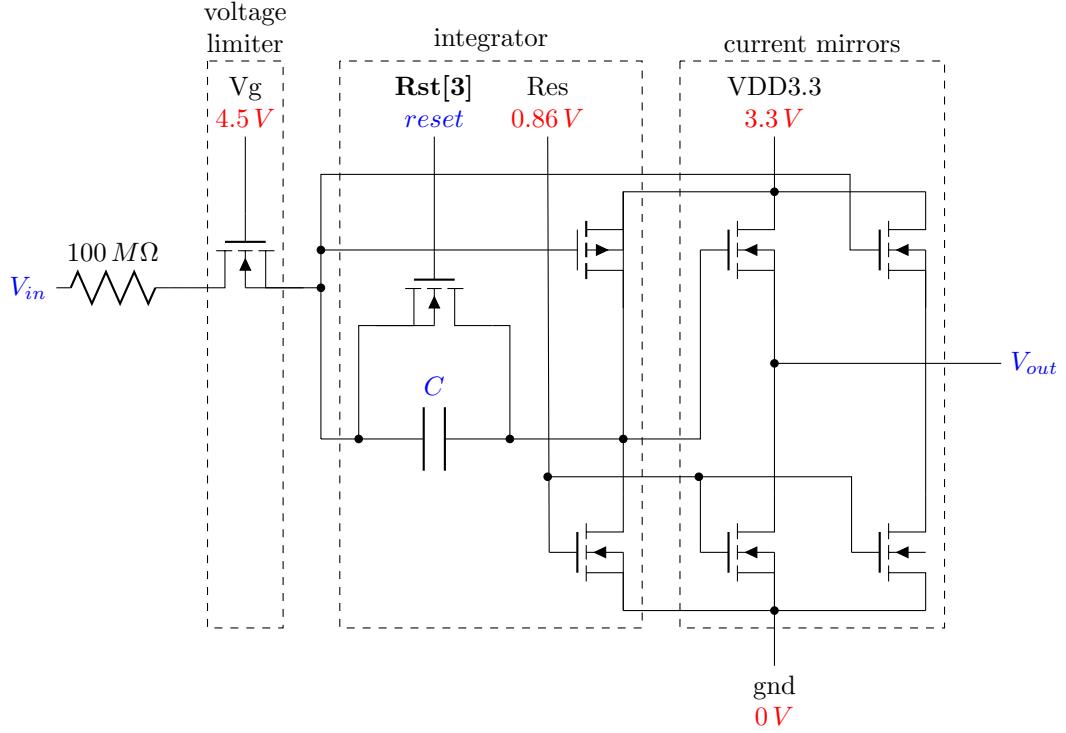


Figure 6: Schematic of ROIC channel template

One can calculate the expected performance of the integrator using eq. (4). The expected time to discharge the capacitance versus the measured time is plotted in fig. 7. The expected and measured values don't quite match. After playing around with some values I found that assuming a parasitic capacitance of 250 fF gave the best match. The expected performance with added parasitic capacitance versus measured is shown in fig. 8.

$$q = C \cdot V \quad (1)$$

$$I = \frac{V_{in} - V_0}{R} \quad (2)$$

$$t = \frac{q}{I} \quad (3)$$

$$t = \frac{CVR}{V_{in} - V_0} \quad (4)$$

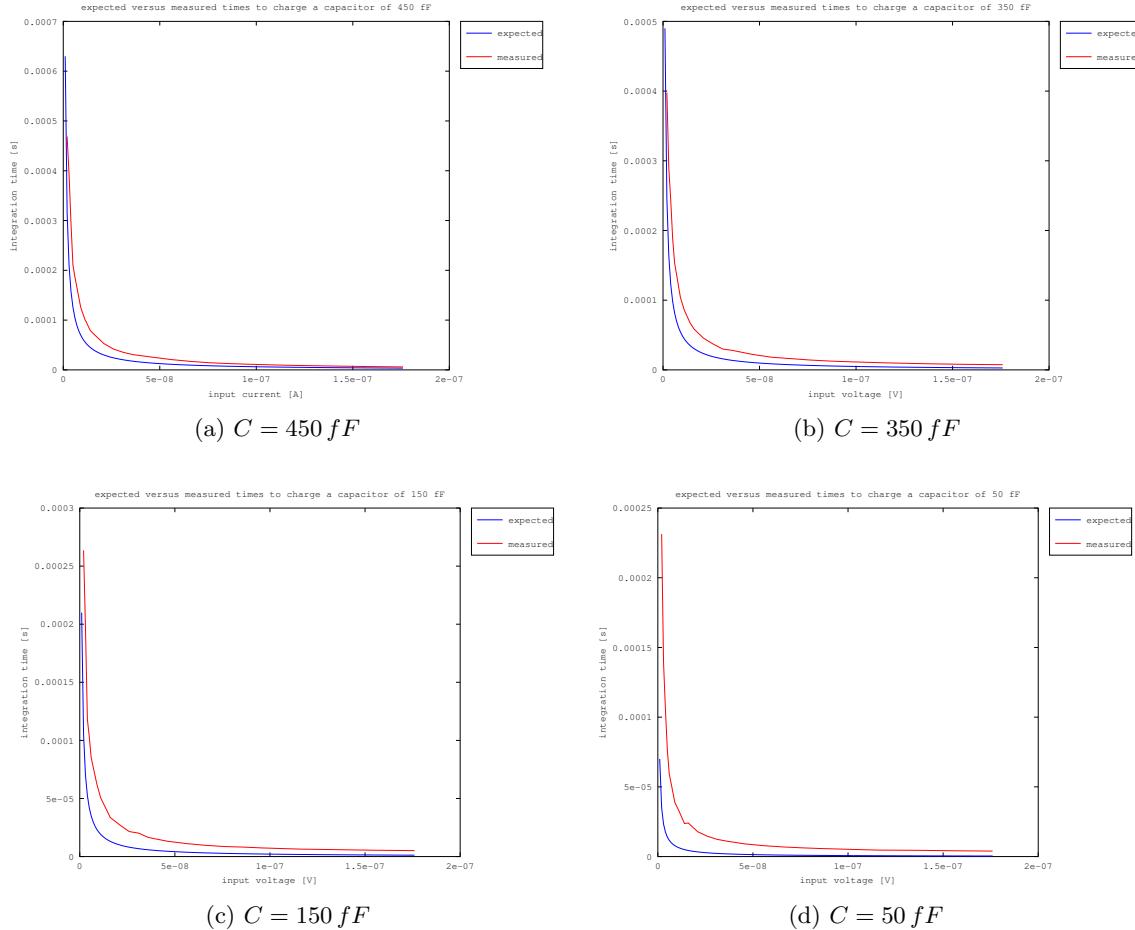


Figure 7: Expected versus measured charge up times for different input voltages. The input voltage is connected to the input through a resistor of $100 \text{ M}\Omega$

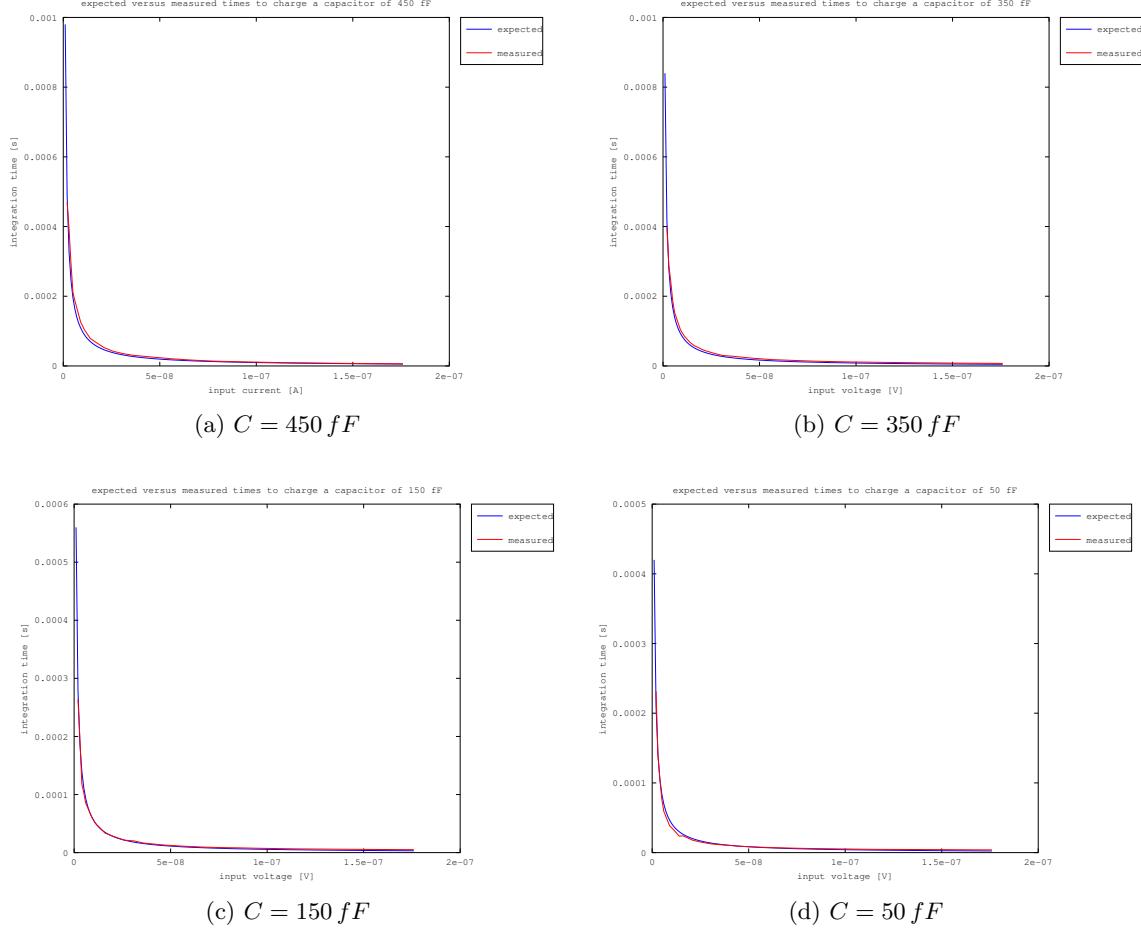


Figure 8: Expected versus measured charge up times for different input voltages. The expected performance is modified by assuming a 250 fF parasitic capacitance. The input voltage is connected to the input through a resistor of $100 \text{ M}\Omega$