

Summer Internship (July-September 2016)  
Characterization and testing of CMOS Readout circuit for  
GaN photodiodes

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## 1 Acknowledgements

In the summer of 2016 I was invited to contribute to research in NASA's Jet Propulsion Laboratory (JPL), which is a dream come true. After I participated in the course Digital IC Design, Dr. Edoardo Charbon provided me with the amazing opportunity to go to JPL and do a research project in the group of Dr Shouleh Nikzad. I would like to thank Dr. Edoardo Charbon and Shouleh Nikzad for giving me this opportunity. I would also like to thank Dr. Douglas Bell, who supported me throughout the project and taught me valuable lessons through his knowledge and experience. I would like to thank Dr. Bruce Hancock, who shared his experience and thought process in numerous occasions. He taught me how to analyse the imperfections and side effects that can occur in real devices, and what kind of considerations are made during the design process to address those issues. I would like to thank the entire group, Advanced Detectors, Systems and Nanoscience, who generously shared their experience in both research and living in LA. They provided a safe and comfortable work environment that made me enjoy my stay without tension or pressure. I hope to collaborate with this group again in the future.

## 2 Introduction

### 2.1 Motivation

UV sensors have numerous applications including oberservation during assembly and the oberservation of outer space. One of the challenges of UV sensors is to deal with sensitivity to visible light, which is the main product of solar irradiation. Gallium Nitride (GaN) has intrinsic solar blindness, which makes it a prime candidate for UV sensors. Furthermore, the material can still be used in solid state devices, and utilize the advantages that come with that . This research project focusses on the nontrivial task of designing and characterizing a suitable readout circuit for a GaN sensor. The project builds on the work of Padmanabhan et al. [4]. who designed a first version of a Readout Integrated Circuit (ROIC). The main goal of this project is to characterize this ROIC, evaluate it's performance when coupled with GaN sensors, and propose improvements for future ROICs.

### 2.2 Gallium Nitride photodiode

Avalange photodiodes (APD) are sensitive semiconductor devices that exploit the so called photoelectric effect to convert light into electricity. The photovoltaic effect is the production of free electrons when light is obserbed in a material. If these electrons are created in the intrinsic region of a PN junction, where there is an electric field, a current will be generated. In linear gain mode, the APD is reverse biased by a small voltage. The increase in current is measured and used a measure of light intensity. Another mode of operation is the geiger mode, where the reverse bias voltage is much higher. In this region the APD operates above breakdown. Breakdown is the point where a free electron can gain enough speed to create other free electrons, causing an avalange. The multiplication eventually becomes so high that ithe current caused by a single photons is large enough to be detected.

One of the big challenges for making UV sensors, is the sensitivity to visible light, which is much more prevalent and acts as a large source of noise. Especially the sun irradiates a lot more visible light than UV. In order to address this issue, Gallium Nitride is used as a material instead of Silicon. The mean reason being it's large bandgap of  $3.4\text{ V}$ . The energy required to create a free electron in this material is more than the energy carried by a single photon in the visible light spectrum. Therefore Gallium Nitride is intrinsic solarblind.

However there are downsides to using GaN. Current gen GaN production introduces a lot of efects. This means that the dark current of a GaN APD is orders of magnitude larger than Si APDs. Secondly the breakdown voltage of GaN is much higher than Si at  $80 - 100\text{ V}$  reverse bias. Furthermore this breakdown voltage varies a lot accross different GaN devices due to the defects in the material.

More information on the state of art GaN photodiodes can be found in [3]. The work in [2], [5] and [1] show the performance of various GaN photodiode designs.

## 3 Readout design

The ROIC used in this project is designed and manufactured by Padmanabhan et al. [4]. The design features three main components. A voltage limiter, an integrator, and two source followers. A schematic of the circuit is shown in fig. 1.

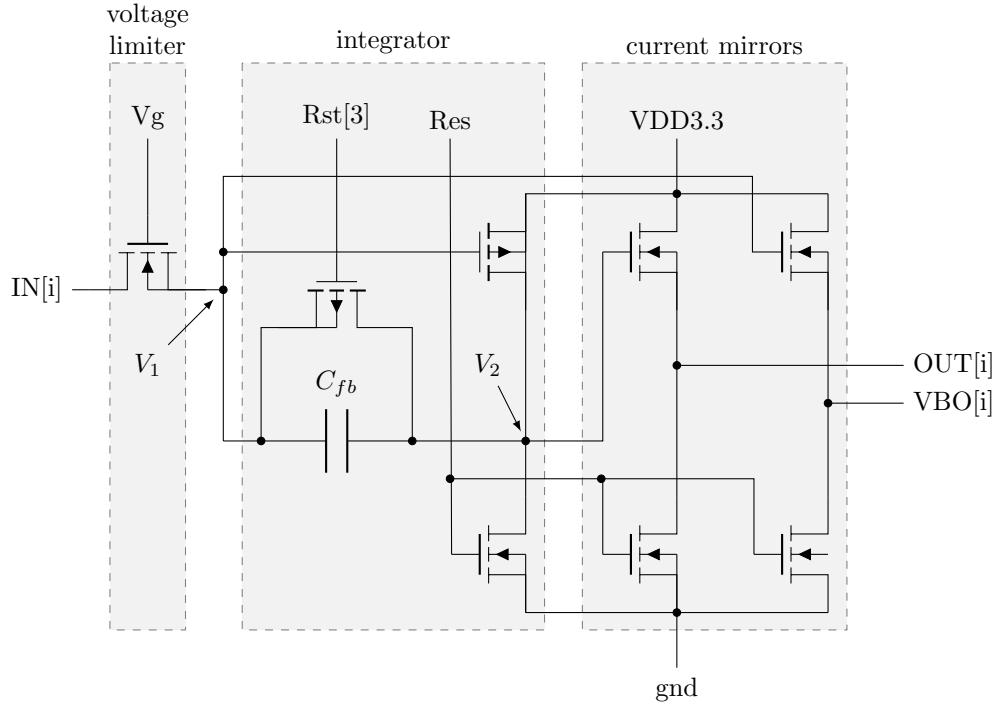


Figure 1: Schematic of ROIC channel

There are two important nodes that will be referred to throughout this documents. These nodes are the in and output of the integrator. They will be referred to as  $V_1$  and  $V_2$  for the in and output of the integrator respectively. This is also shown in fig. 1.

The voltage limiter limits the maximum voltage in the ROIC to protect both the ROIC and the GaN sensors from too much power dissipation. The integrator translates the accumulative amount of charge that has entered the device into an output voltage. The source followers allow for an external readout without affecting the behavior of the ROIC. Section 3.1-3.3 describe the different components in more detail.

### 3.1 Voltage limiter

The voltage limiter consists of a single transistor with a gate voltage  $V_g$  that can be controlled externally. The limiting effect uses the property of cutoff when  $V_{GS} \leq V_t$ . This means that  $V_S \leq V_G - V_T$ . A  $V_T \approx 0.7$  and a  $V_G = 4.5\text{ V}$  for example, would yield a maximum  $V_S \approx 3.8\text{ V}$ . The performance of the voltage limiter in practise will be investigated in section 5.5.

### 3.2 Integrator

The integrator transforms the accumulated amount of charge at the input into a change in output voltage. The change in output voltage can be calculated using eq. (1). A schematic of the circuit

is shown in eq. (1)

$$\Delta V_{out} = \frac{-1}{C} \int_0^T I dt = \frac{-q}{C} \quad (1)$$

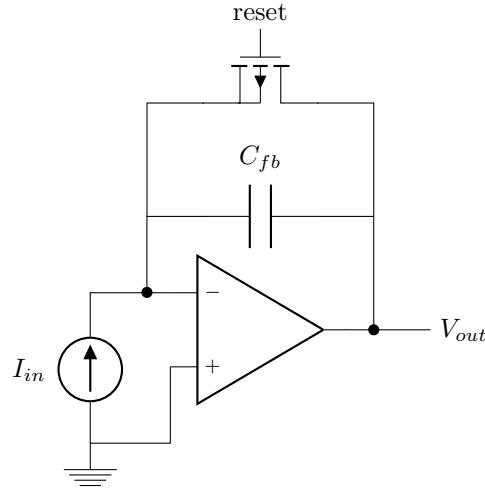


Figure 2: schematic of integrator

The input of the integrator is connected to the ouput of the voltage limiter. The reset switch is controlled externally and used to reset the integration capacitance  $C_{fb}$ . Note that the relationship between change in voltage and input current is negative. This means that the output voltage drops with a positive input current. The behavior of the integrator is further investigated in section 5.4.

### 3.3 Source follower

The source followers protect the circuit from external influences. There is one source follower connected to  $V_1$  and the other to  $V_2$  to be able to obeserve both in an unintrusive manner. A schematic overview of a the source followers is shown in fig. 3. Note that the relationship between  $V_{in}$  and  $V_{out}$  is non-linear. Also note that the speed at which the source follower can change slope is limited by the bias current for both the pull up and pull down. It is therefore possible that the input rises or falls at a faster speed than the source follower can keep up with. The behavior of the source followers is further investigated in section 5.3.

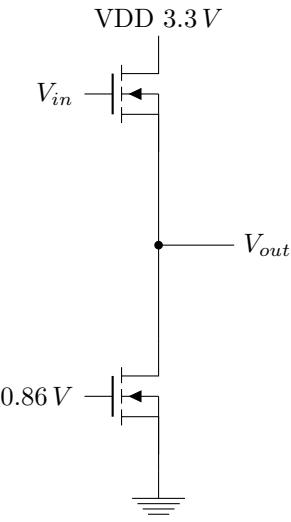


Figure 3: Schematic of source follower

## 4 Steady state ROIC characterization

The first part of the characterization process is the behavior in steady state. In particular the period where the reset is on. This state has no time component in it, and therefore can be observed with a relatively simple setup.

### 4.1 Setup

The first version of the setup consists of a breadboard with the ROIC, several voltage sources, and an oscilloscope. The layout of the breadboard is shown in fig. 4. All pins on the ROIC that are non listed are floating.

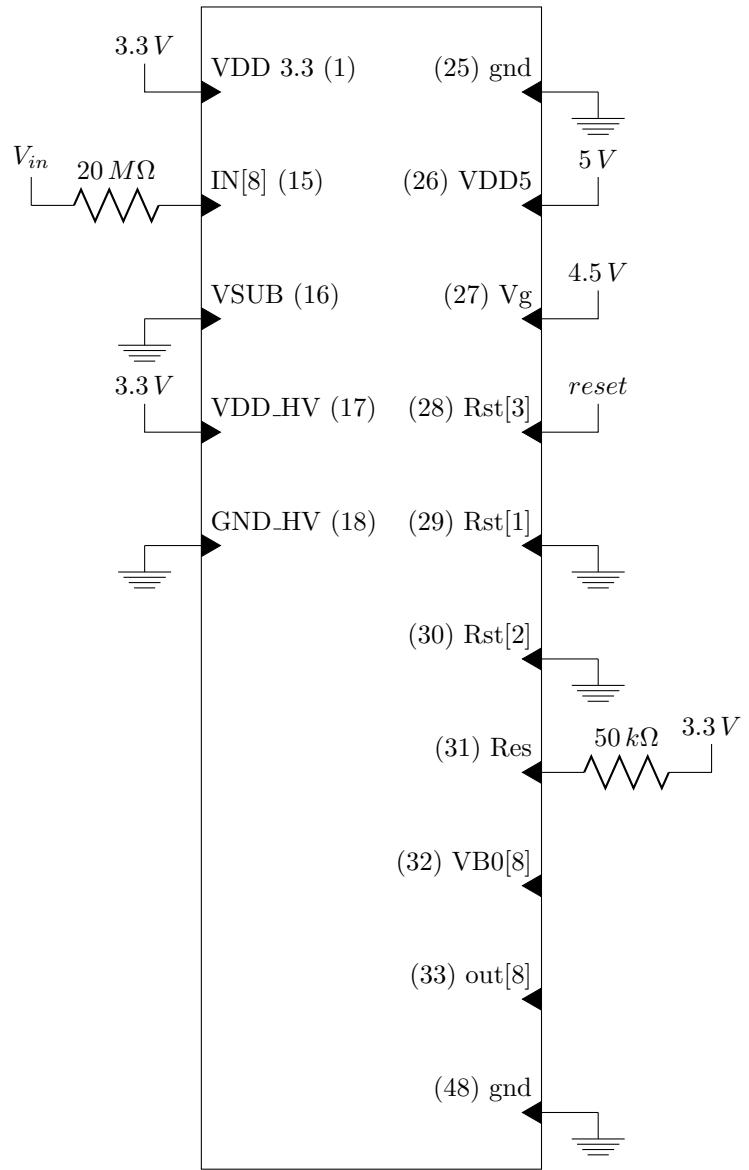


Figure 4: Schematic of breadboard

## 4.2 Correct voltage on HDD\_HV

During the first stages of the setup there were problems with the correct settings for the HDD\_HV input, because of a misunderstanding with the manufacturer. The instructions for the ROIC stated that the HDD\_HV should be connected to the input voltage of the GaN sensors, but the correct value for HDD\_HV is actually 3.3 V. If the HDD\_HV value is raised to much, the ROIC is destroyed.

### 4.3 Behavior during reset

Because a PMOS reset transistor, the circuit is in reset mode when  $\text{reset} = 0 \text{ V}$ . The measured voltages in this state are shown in fig. 5. The measured values match with the simulation results performed by Padmanabhan et al. [4]. Note that the input voltage is  $2.4 \text{ V}$ . This is an important value, for it is used to determine the input current, when a voltage source and resistor are used for input. Also note that the output voltage of  $\text{VBO}$  is  $1.4 \text{ V}$ , while the input is  $2.4 \text{ V}$ . This already shows that the source followers don't reproduce the input 1:1. This will be further investigated in section 5.3.

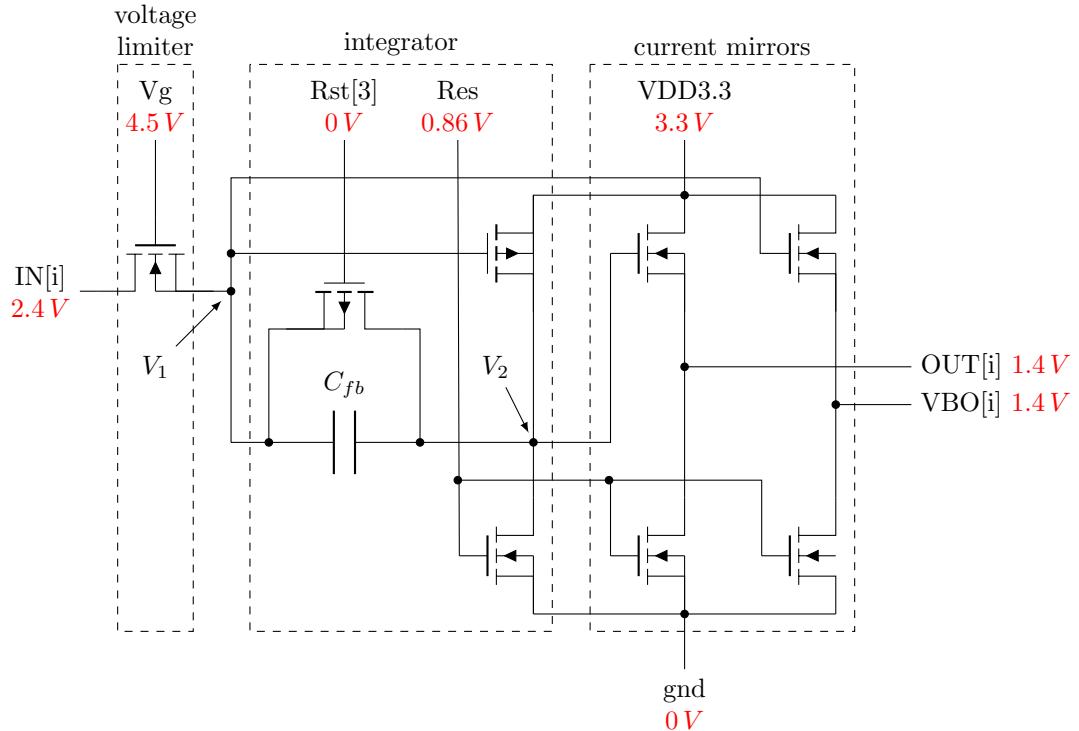


Figure 5: Schematic of ROIC channel template

## 5 Dynamic ROIC characterization

The next step is to look at the dynamic behaviour of the ROIC under varying input currents. The aim of this section is to characterize the dynamic behavior of the three different components of the ROIC separately: The source followers, integrator and voltage limiter respectively. In order to observe accurate changes on a small timescale, a more sophisticated setup is required.

### 5.1 Setup

The desired measurements require a lot of samples and in order to observe a slope, waveforms. Also the device needs to be reset in order to observe the dynamic behavior of the integrator. In order to address all those issues, the function generator in the oscilloscope is used to create a periodic pulse for the reset. The trigger function of the oscilloscope is used to observe the period around the rising edge of the reset. The averaging function on the oscilloscope is used to reduce the effect of noise. The input voltage is manually controlled through a voltage source. The observed waveforms are stored to a usb and transported to a computer. On the computer, these waveforms are further processed in `octave-cli` (octave command line interface), which generates plots out of the measurement data.

This setup provides a convenient method of processing a lot of measurements, without an insurmountable amount of manual labor.

### 5.2 Calculation of current

The calculation of the slope can be tackled in many different ways. Throughout the project, multiple calculation methods were used. For all measurements in this setup the same method is used. First on the oscilloscope with a trigger an averaging of 128 is used. This is done to eliminate noise that is prevalent in this setup. At a later stage in the project it was discovered that certain components connected to the power grid caused the majority of this noise. To estimate the slope two points on the middle of the slope are taken, and used to calculate the slope between the two. The calculated slope estimates the steepest part in the waveform.

The voltages on the chosen points in the waveform are first altered to compensate for the behavior of the source followers. Finally, to go from slope to current, the slope will be divided by the integration capacitance.

### 5.3 Source followers

The design of the source follower is described in section 3.3. In order to characterize the behavior of the source follower, a voltage source is directly connected to the input of the ROIC. This forces the output of the voltage limiter to the same value as the source follower, as long as the voltage limiter is not triggered. The input of the source follower connected to the VBO output, is directly connected to this output, and is therefore fully controllable. The output of this source follower can be directly observed. This means that the characteristics of the source follower can be measured directly. Note that the source follower connected to the output of the integrator is identical, which means that only one needs to be characterized. Figure 6 shows both the measured data and a fitted line with the formula  $v_{out} = 0.827v_{in} - 0.624$ . In order to avoid pile-up it will be assumed that this formula characterizes the performance of both source followers.

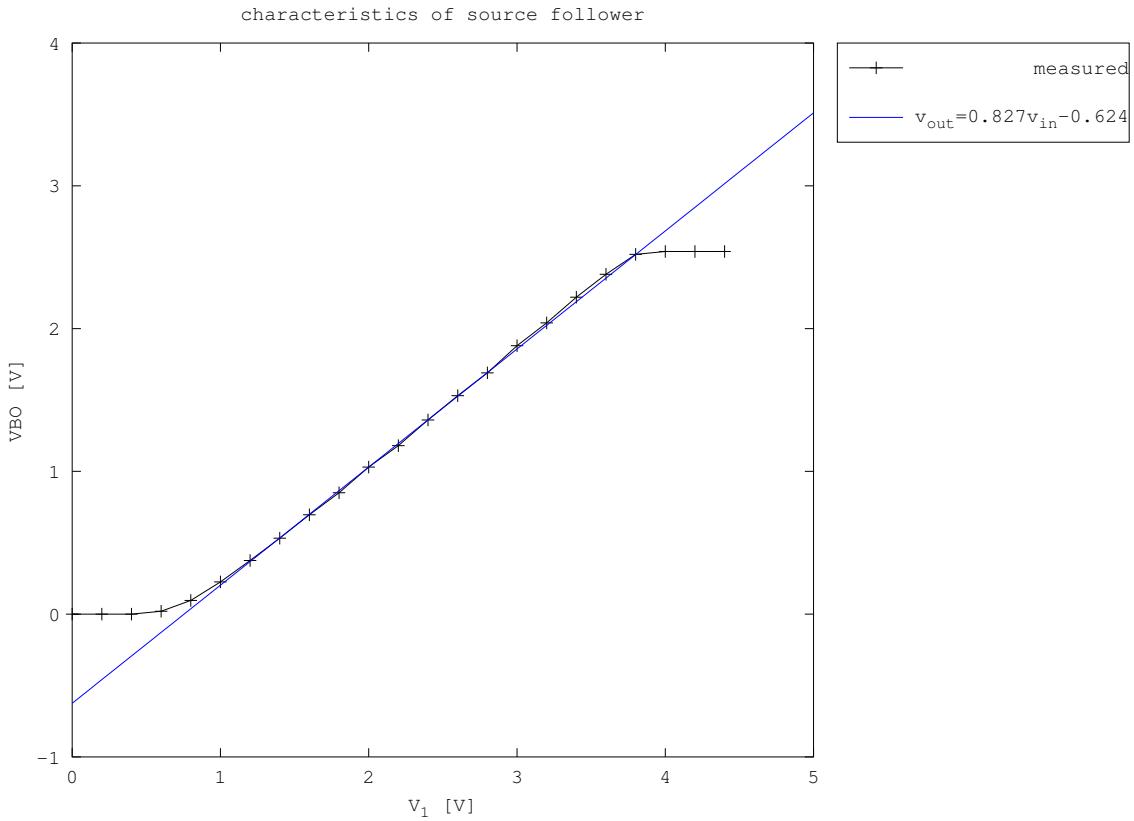


Figure 6: plot of the input voltage against VBO. This plot shows the characteristics of the voltage follower

## 5.4 Integrator

The measurements of the behavior of the integrator are divided into three sections. Section 5.4.1 will focus on the output of the ROIC for low currents. Section 5.4.2 will do the same, but this time for currents that are a lot higher. Finally section 5.4.3 will look at the behavior of VBO, and investigate the viability of using the source follower connected to  $V_1$  as a secondary readout. Note that all plots are not what is directly observed at the output. All results have compensation for the behavior of the source followers.

### 5.4.1 Standard behavior

This test aims to address the basic relationship between input current and output voltage. Figure 7 shows the setup used for this test. Channel 8 was used, so the end of the  $20 M\Omega$  resistor is connected to IN[8], and probes are connected to OUT[8] and VBO[8].

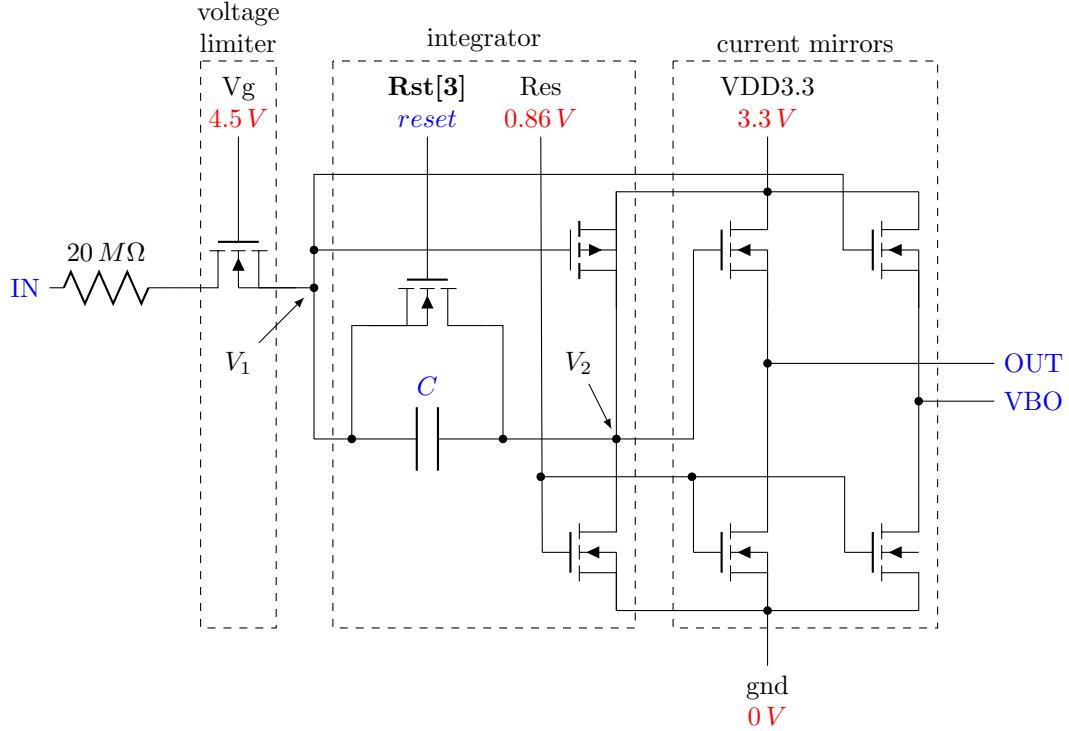


Figure 7: Schematic of ROIC channel template

Figure 8 shows the time versus voltage plot of both the VBO and OUT for a constant input voltage. The rising and falling slopes are the VBO and OUT respectively. The timescale of this plot does not allow for much insight in the behavior of VBO, but it does show some interesting results for the behavior of the integrator. When the reset switches, the input node immediately loses some charge. Note that the oscilloscope matches the rising edge of the reset signal to time is 0 s. When the reset is switched, a capacitance is removed almost instantly. It is interesting to observe that the slope immediately after the rising edge of the reset is constant for all input voltages. This means that the observed slope is not limited by the reset transistor, but by the source follower that tries to keep up. This observed slope is therefore the maximum rate at which the output node can be pulled down in the current set-up. Also note that the slope gets steeper when the integrator capacitance decreases. This matches the expected behavior of  $\Delta V = \frac{-q}{C}$ .

Figure 9 shows the same plot as fig. 8, but now the x axis is scaled with input current. This shows for fig. 8a and 8b that the relationship between output voltage and charge is equal across different input voltages. For fig. 8c and 8d however, one can see that the higher voltages lose this property. Another interesting observation is that when one looks closely at the plot, one can observe a small oscillation with a period that is constant with charge. Also the period is constant across different voltages. At a later stage it was discovered that several voltage sources introduced the noise to the system. Removing these devices also removed the observed noise. There was at that point no time left to redo all the measurements however.

Figure 10 shows the  $\delta Q/\delta V$  against charge plots. Note that  $\delta Q/\delta V$  is the capacitance. One can

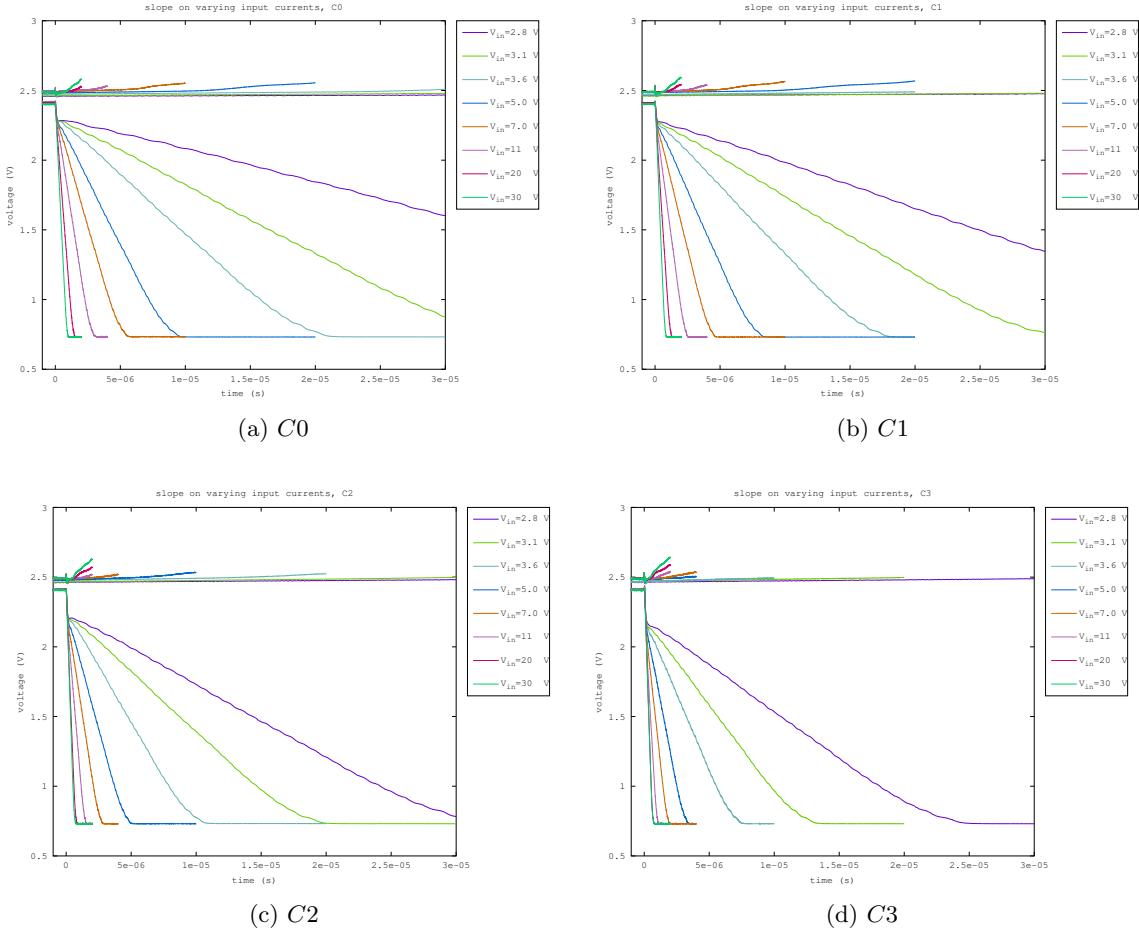


Figure 8: Expected versus measured charge up times for different input voltages. The input voltage is connected to the input through a resistor of  $20 M\Omega$

observe that while the capacitance is charging, the full value of the capacitance can be observed, and when the capacitance is completely discharged, it behaves as if it is not there. One can use these plots to estimate the integration capacitance. The capacitance for fig. 9a, 9b, 9c and 9d are approximately  $400 fF$ ,  $350 fF$ ,  $200 fF$  and  $150 fF$  respectively. These values are used for all calculations that involve the integration capacitance throughout the rest of the report.

Figure 11 shows  $\delta V/\delta t$  against input voltage for all capacitances. One can observe that all four have different slopes at first, but there appears to be a trend that they all converge to a value of  $\delta V/\delta t \approx 3.2 \cdot 10^6$ .

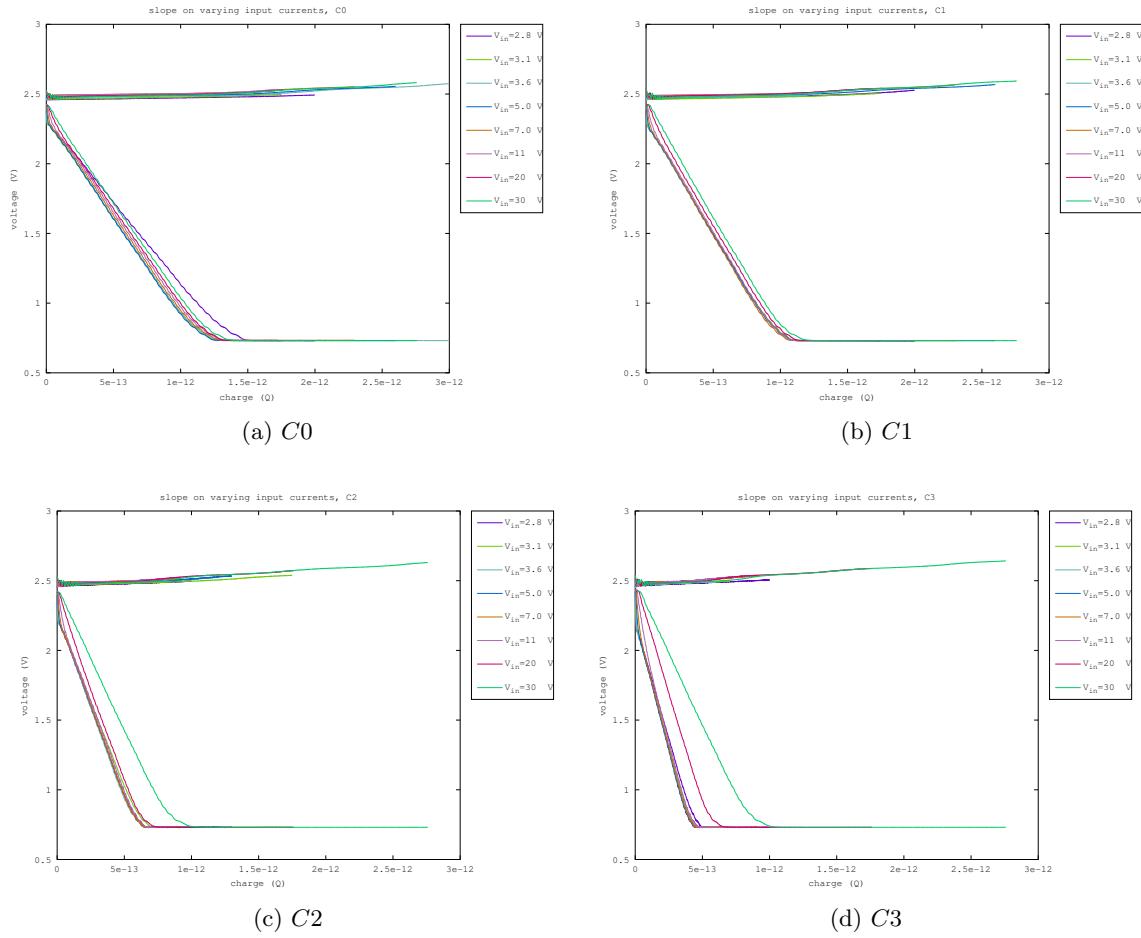


Figure 9: This plot is showing charge versus voltage

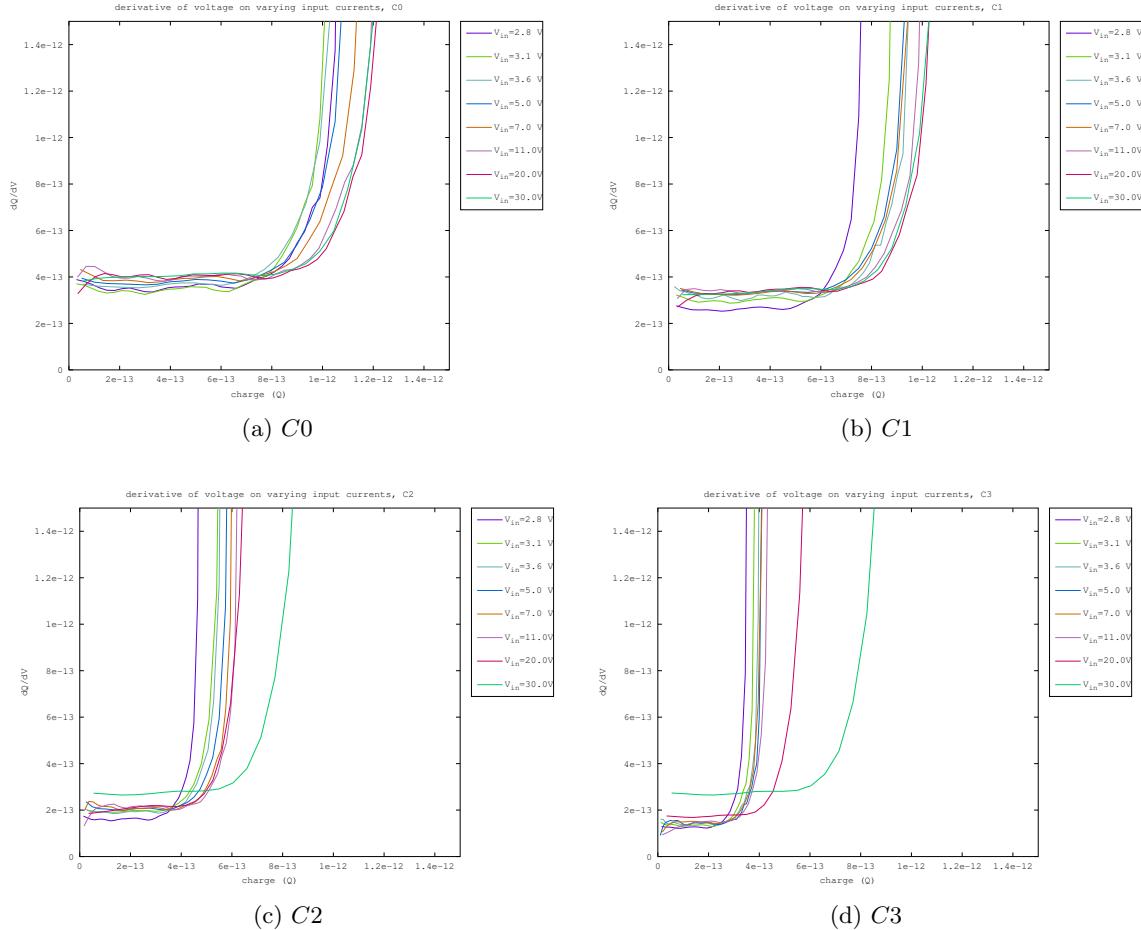


Figure 10: The plot shows  $dv/dt$  against time. The plot is in log scale, which allows for an easy read on the maximum slope and the time needed to discharge the integrator capacitance.

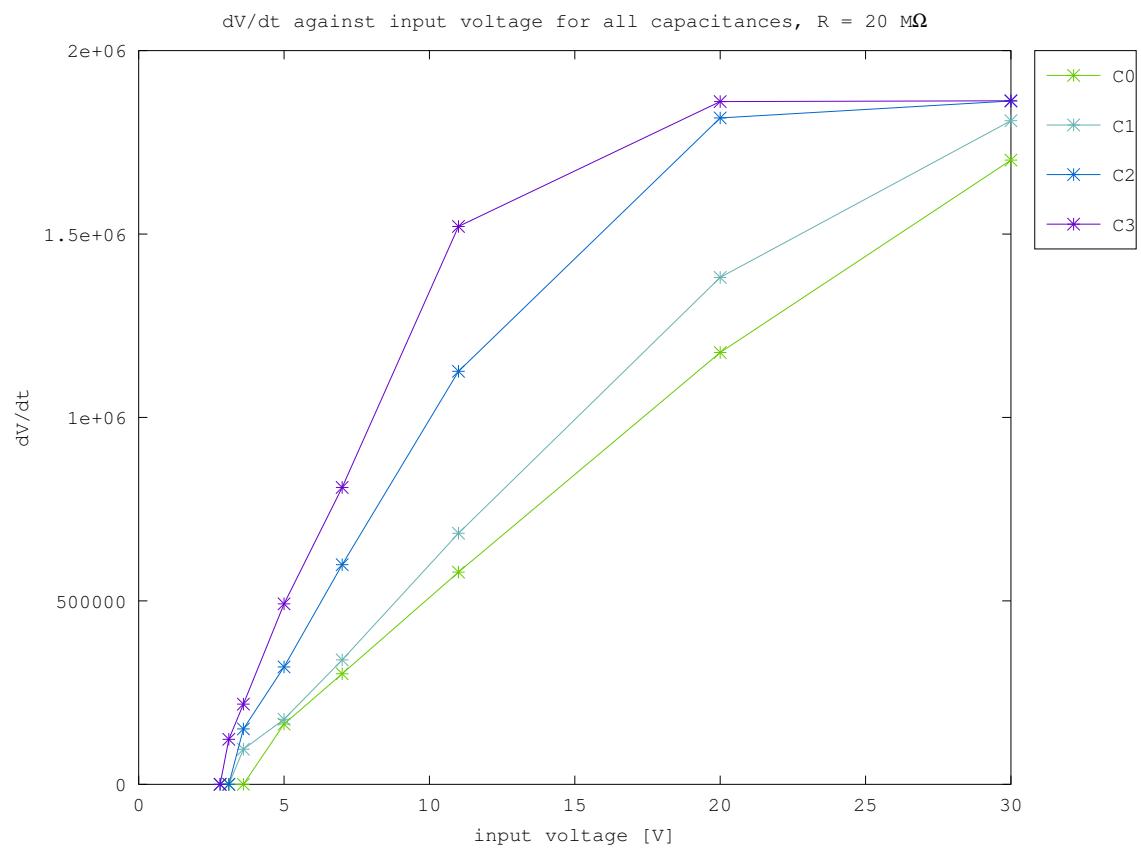


Figure 11:  $dV/dt$  against input voltage for all four capacitances. The x indicate the measurements.

### 5.4.2 High current behavior

In this section the  $20 M\Omega$  input resistor is replaced with a  $4 M\Omega$  resistor. The main goal is to observe the ROIC for very large currents.

Figure 12 shows the same plot as fig. 8, but this time with larger currents. Where a minimum slope could be observed at fig. 8, it is more prevalent here. This also shows more information about the behavior of VBO. For small voltages the VBO does not increase, but as the voltages get larger, one can observe that the voltages of VBO start rising when the OUT is done with discharging. It is also interesting to note that VBO seems to be not affected by the minimum slope at OUT. This gives rise to the hypothesis that the OUT is limited by the source follower.

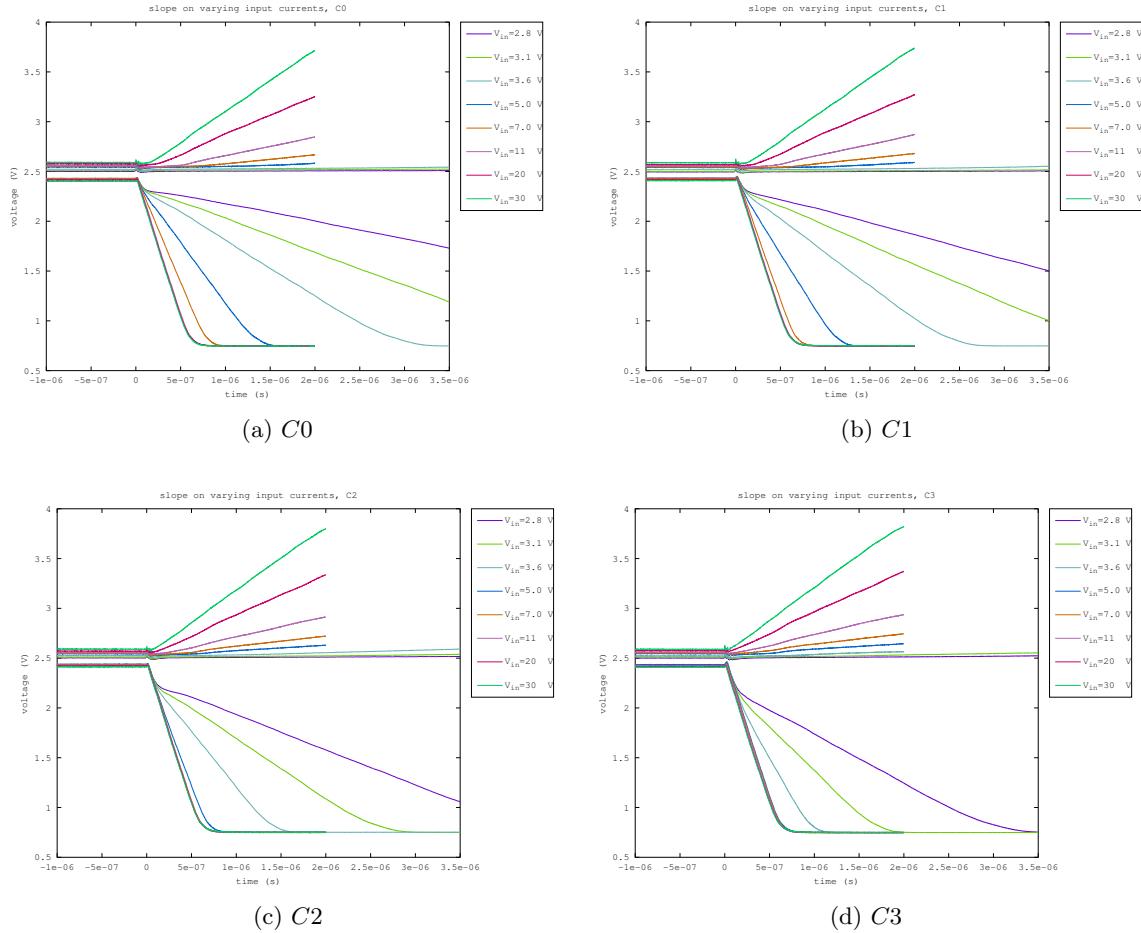


Figure 12: Expected versus measured charge up times for different input voltages. The input voltage is connected to the input through a resistor of  $4 M\Omega$

Figure 13 shows a similar plot as in fig. 9 but with higher currents. In fig. 9 one could observe that all currents fitted to the same line, but deviated at higher currents. This effect is also observed here, but in a stronger form. Which is to be expected.

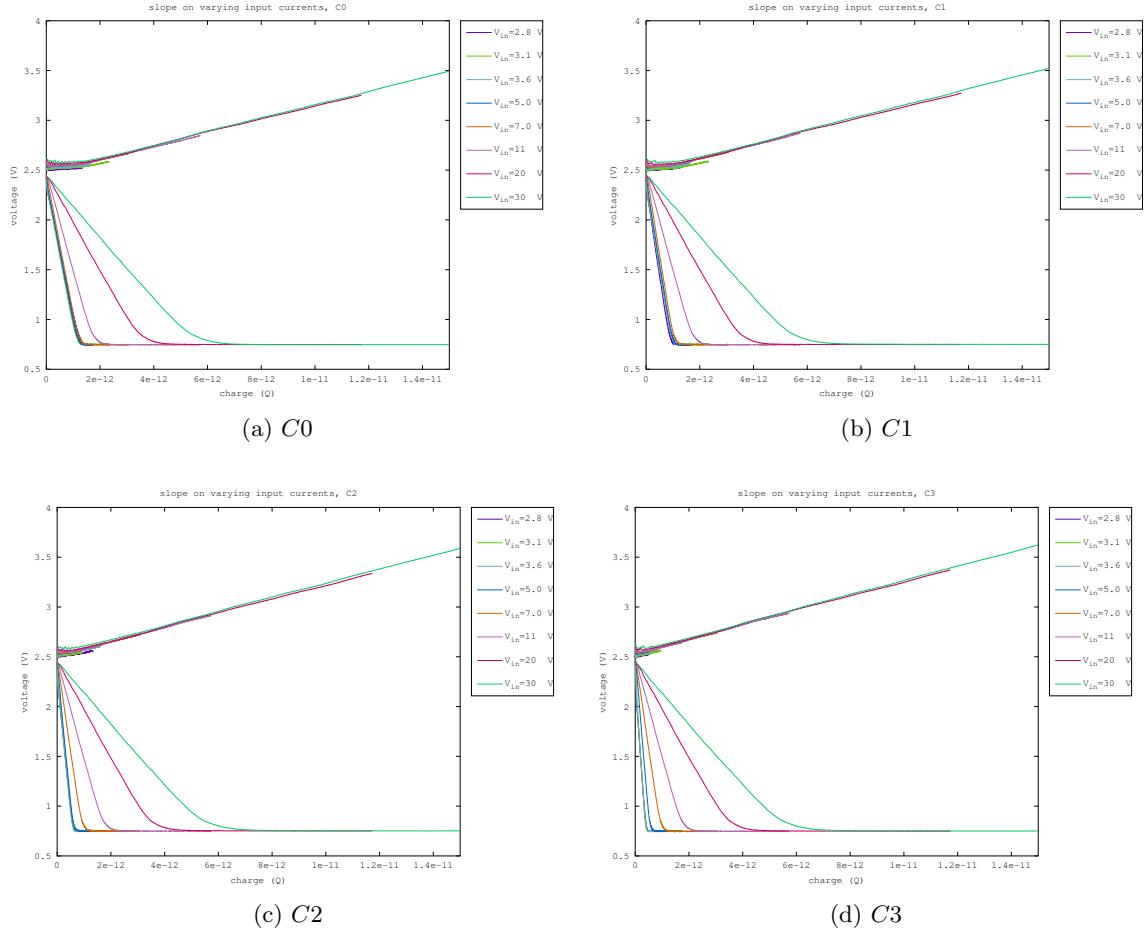


Figure 13: This plot is showing charge versus voltage

Figure 14 shows a plot of  $\delta V/\delta Q$  against charge. Note that the behavior for the low voltages differ across the different capacitances, but that the high voltages are not affected by a change in capacitance. This observation agrees with the hypothesis that the output is not limited by the input current, but by the speed of the source follower at the output.

Figure 15 shows the same plot as fig. 11, but with higher current. This plot clearly shows that all four capacitance configurations saturate at a  $\delta V\delta t \approx 3.1 V$ . This cannot be a limit applied to the input, because the capacitances are different. Therefore the output is limiting this, conform previous observations.

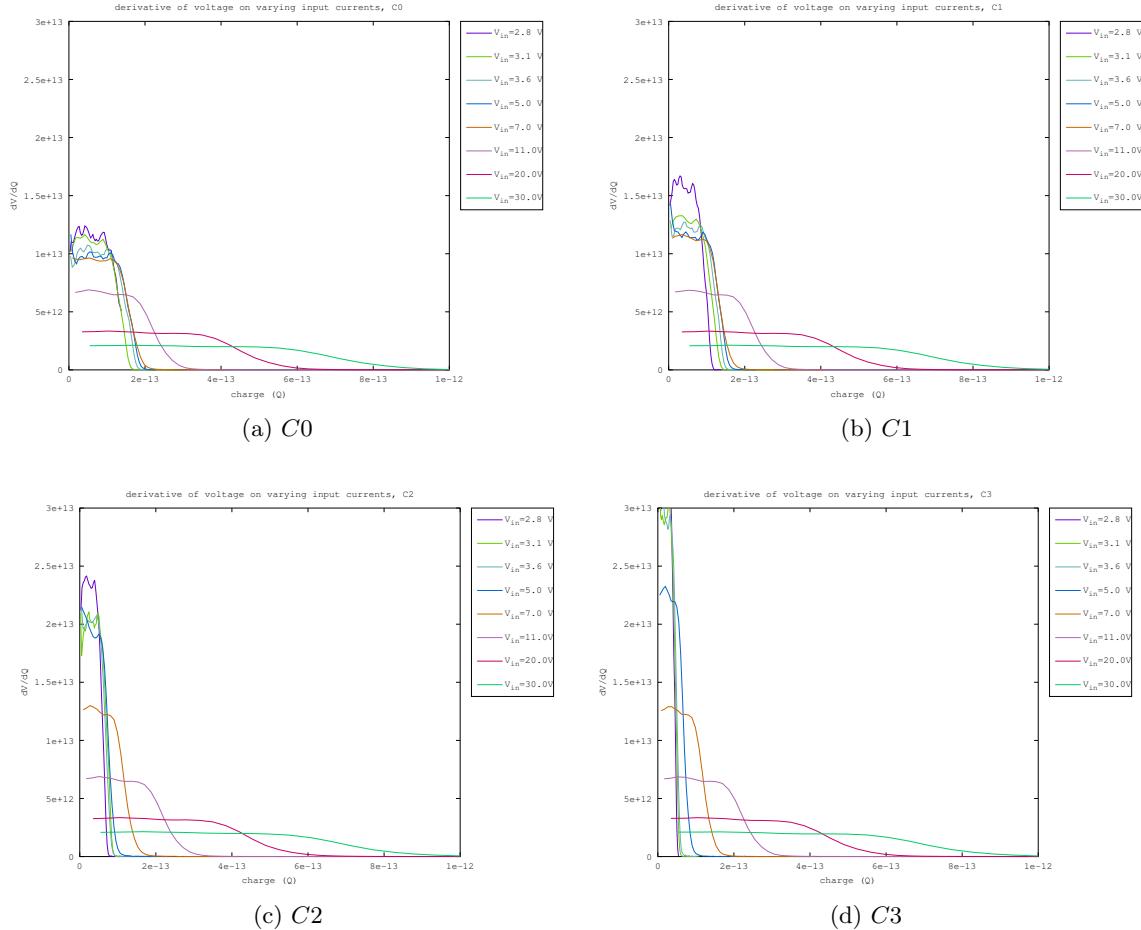


Figure 14: The plot shows  $dv/dt$  against time. The plot is in log scale, which allows for an easy read on the maximum slope and the time needed to discharge the integrator capacitance.

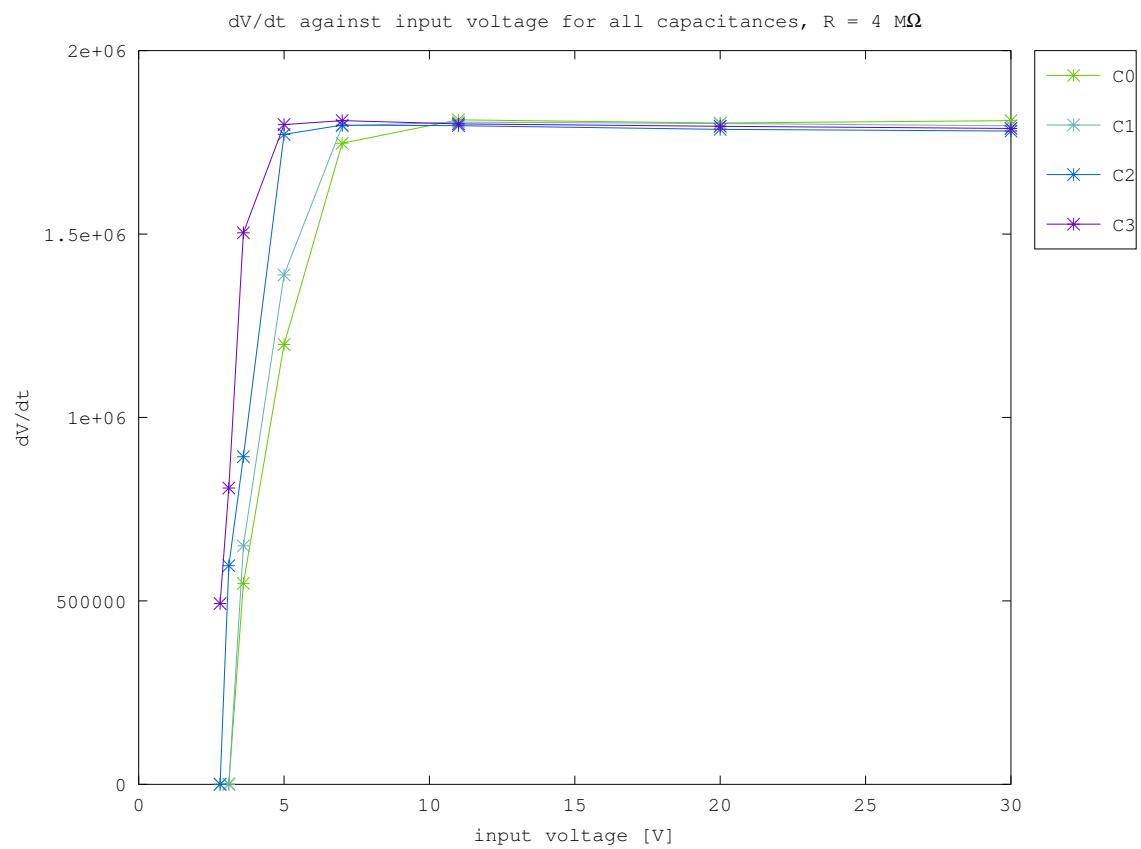


Figure 15:  $dV/dt$  against input voltage for all four capacitances. The x indicate the measurements.

### 5.4.3 VBO behavior

This section focusses on the output of the source follower that is directly connected to the output of the high voltage transistor connected to the input of the ROIC. The setup is identical to section 5.4.1, but the time scale is different to observe the slower behavior of VBO.

Figure 16 shows the time against voltage plot. This are a couple of important observations that can be made from these plots. First and foremost: the behavior of the VBO is almost not affected by the capacitance. There is a difference however, in that the VBO starts rising as the OUT reaches zero. This means that the VBO for  $450\text{ fF}$  is slightly delayed when compared to  $50\text{ fF}$ . It is also interesting to observe that VBO never increases above  $3.8\text{ V}$ . This behavior is most likely due to the functioning of the voltage limiter that will be investigated later on. Finally one can observe that for very low currents, VBO does not reach  $2.6\text{ V}$ . The reason for this is that the input reaches the voltage level of the power supply before the current limiter kicks in.

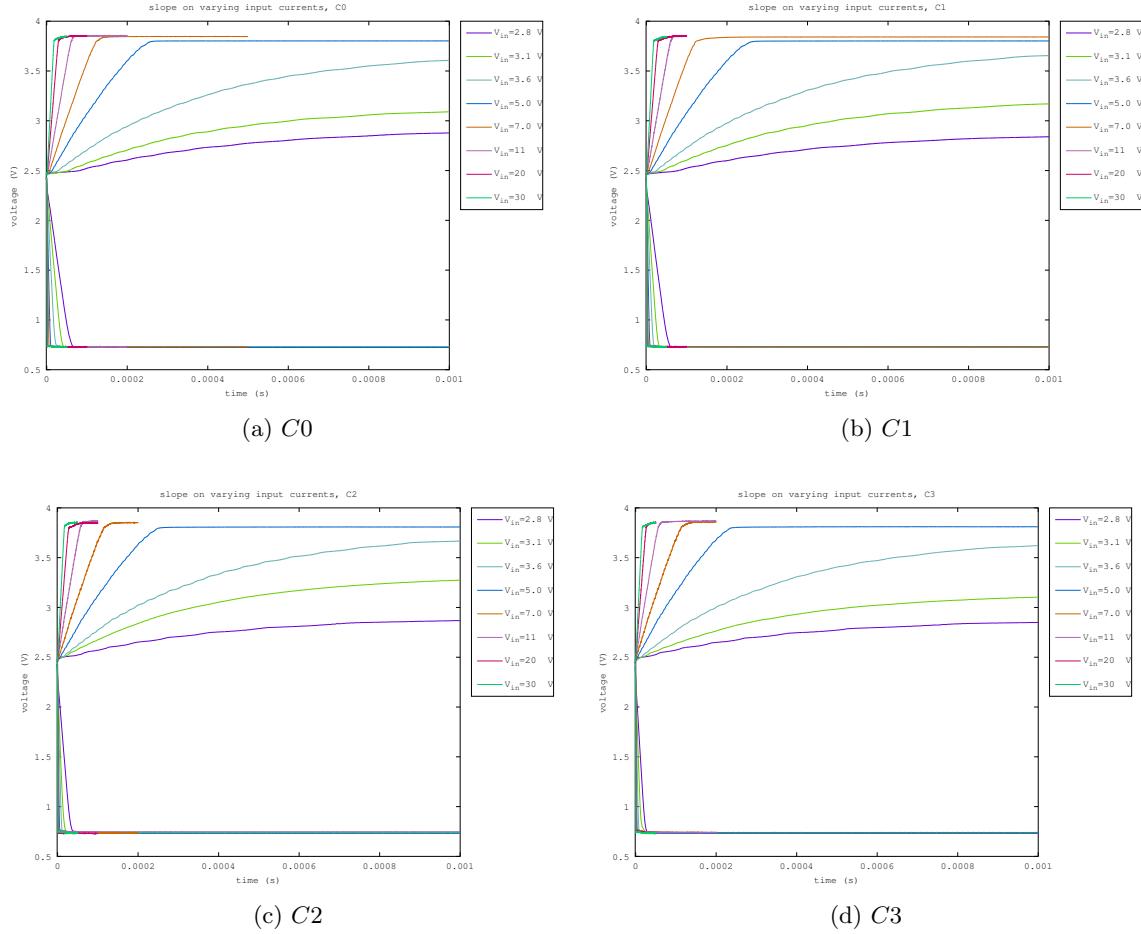


Figure 16: Expected versus measured charge up times for different input voltages. The input voltage is connected to the input through a resistor of  $20\text{ M}\Omega$

Figure 17 shows the plots of voltage against charge. One can observe that increasing the current causes the behavior to converge to a line with a linear slope that is constant with  $Q$ , and a saturation at  $3.8 V$ .

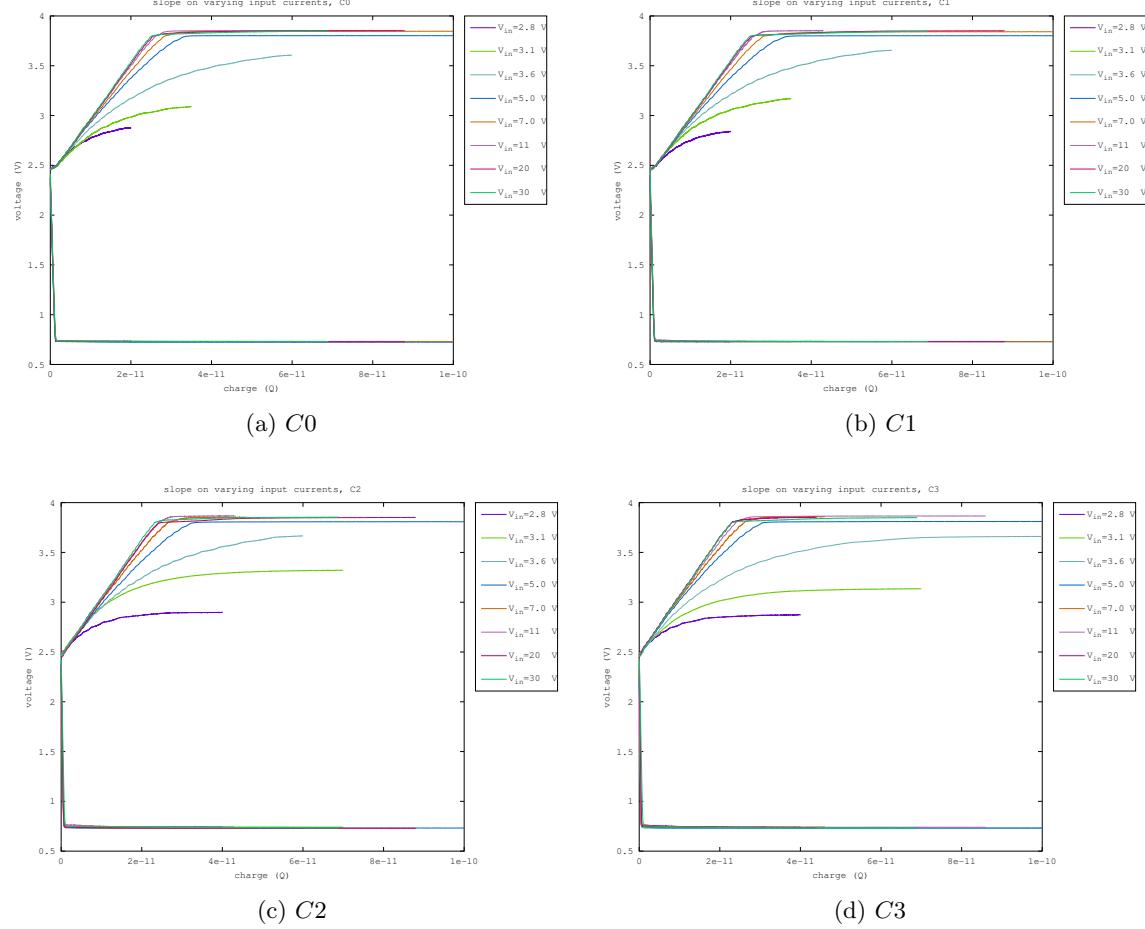


Figure 17: This plot is showing charge versus voltage

Figure 18 shows  $\delta V/\delta Q$  for the VBO. The main observation one can make from these plots is that the behavior of VBO is almost entirely unaffected by the integration capacitance.

Figure 19 shows the  $\delta V/\delta t$  against input voltage for VBO across all capacitances. For large voltages seem to behave in a normal linear fashion. The startup shows a scene that looks as if the  $C_0$  and  $C_1$  setup behave identical, and that the  $C_2$  and  $C_3$  setup behave identical. This might be due to the lack of measurement points, but is worth investigating further.

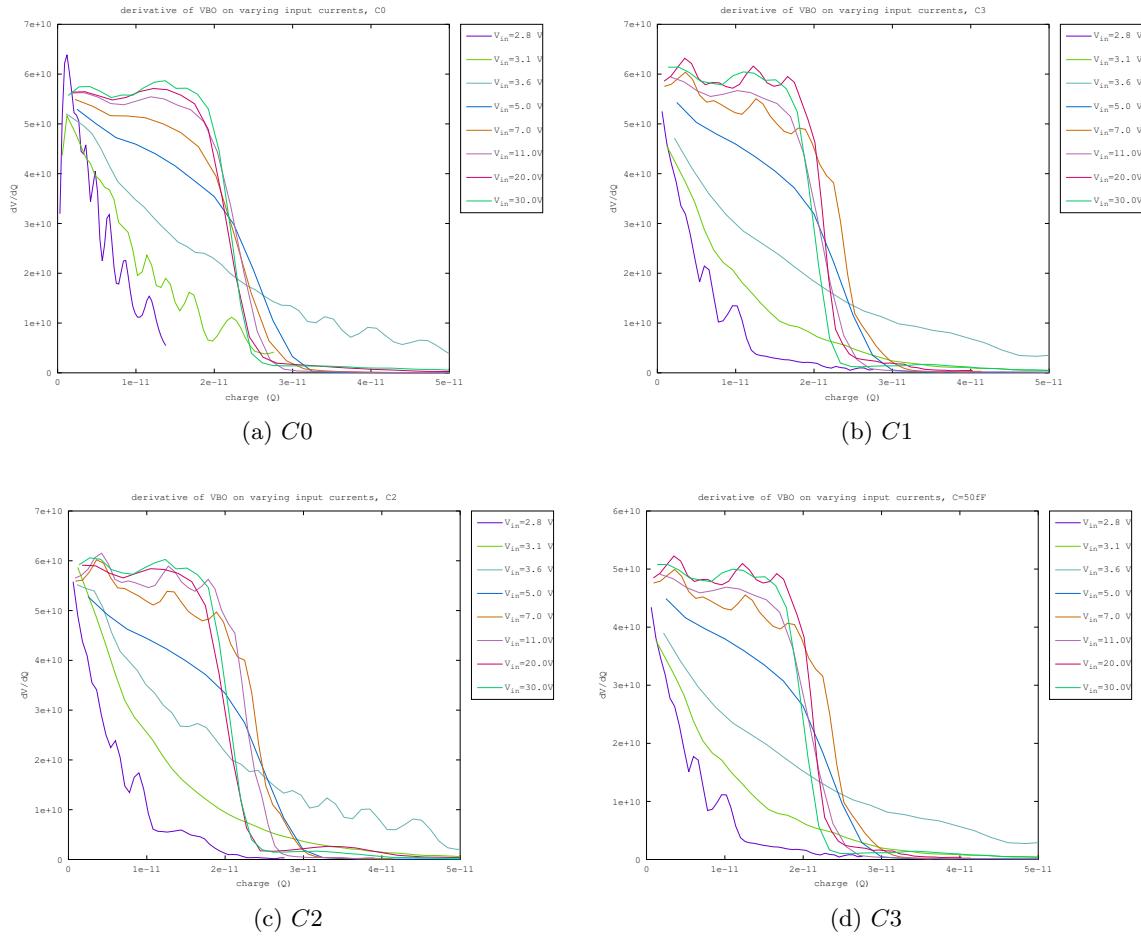


Figure 18: The plot shows  $dv/dt$  against time of the vbo.

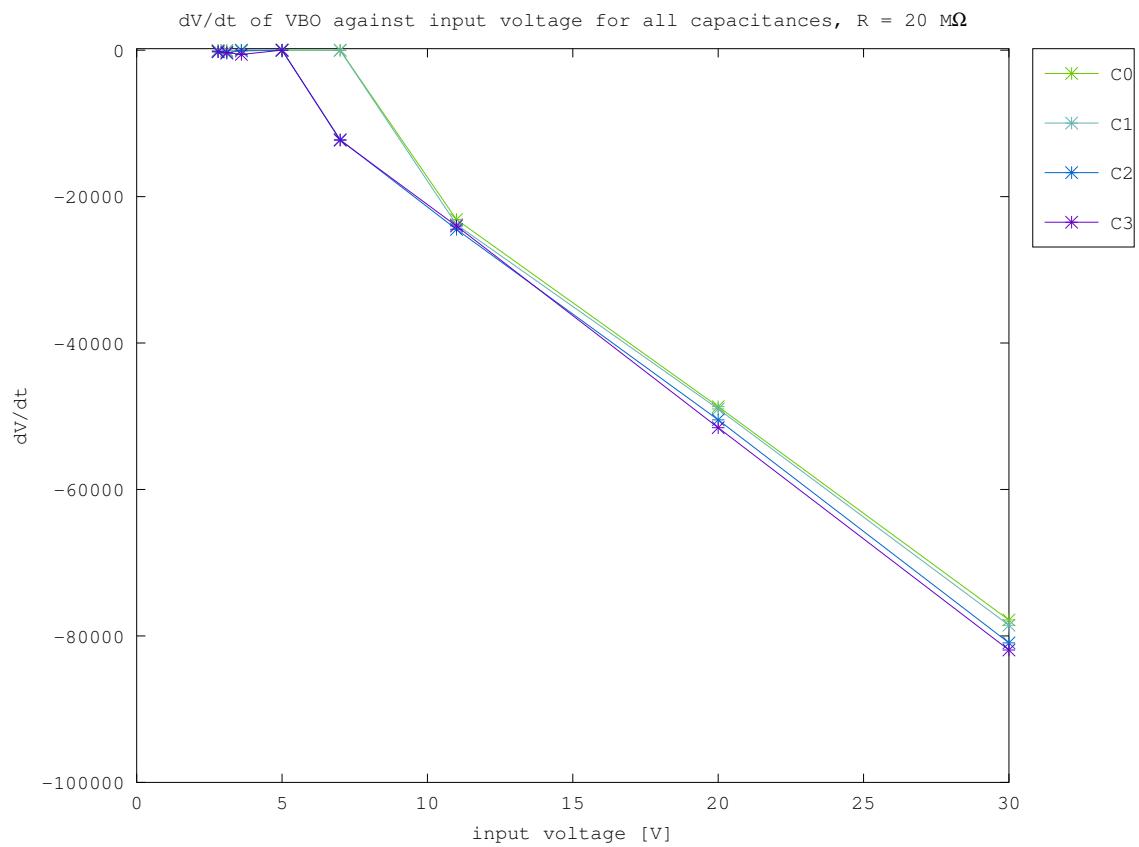


Figure 19:  $dV/dt$  of VBO against input voltage for all four capacitances. The x indicate the measurements.

## 5.5 Voltage limiter

In fig. 16 one can already observe the voltage limiter in action. The measurements in fig. 16 are taken with a  $V_g = 4.5 V$ , but it is worth investigating the behavior between  $V_g$  and the voltage limit posed by the voltage limiter. Figure 20 shows the measurement results of relationship between  $V_g$  and the voltage limit posed by the high voltage transistor at the input. The relationship appears to be linear between 3 and 3.8 V, but changes behavior at higher  $V_g$ . A possible explanation for this might be found in the reset transistor used to reset the integration capacitance. The body voltage of that pmos transistor is connected to the VDD of the circuit which is 3.3 V. Normally, this means that there is no current from source to the body, because the body is at the highest voltage, and the p-n junction between source and body will not conduct. This changes when the source voltage rises above the body voltage however, which can cause the p-n junction to draw current. This issue could explain the changed behavior of the voltage threshold at higher  $V_g$ . If this is the case, then a high  $V_g$  is very undesirable to operate the device, for it means that the device draws current even when saturated.

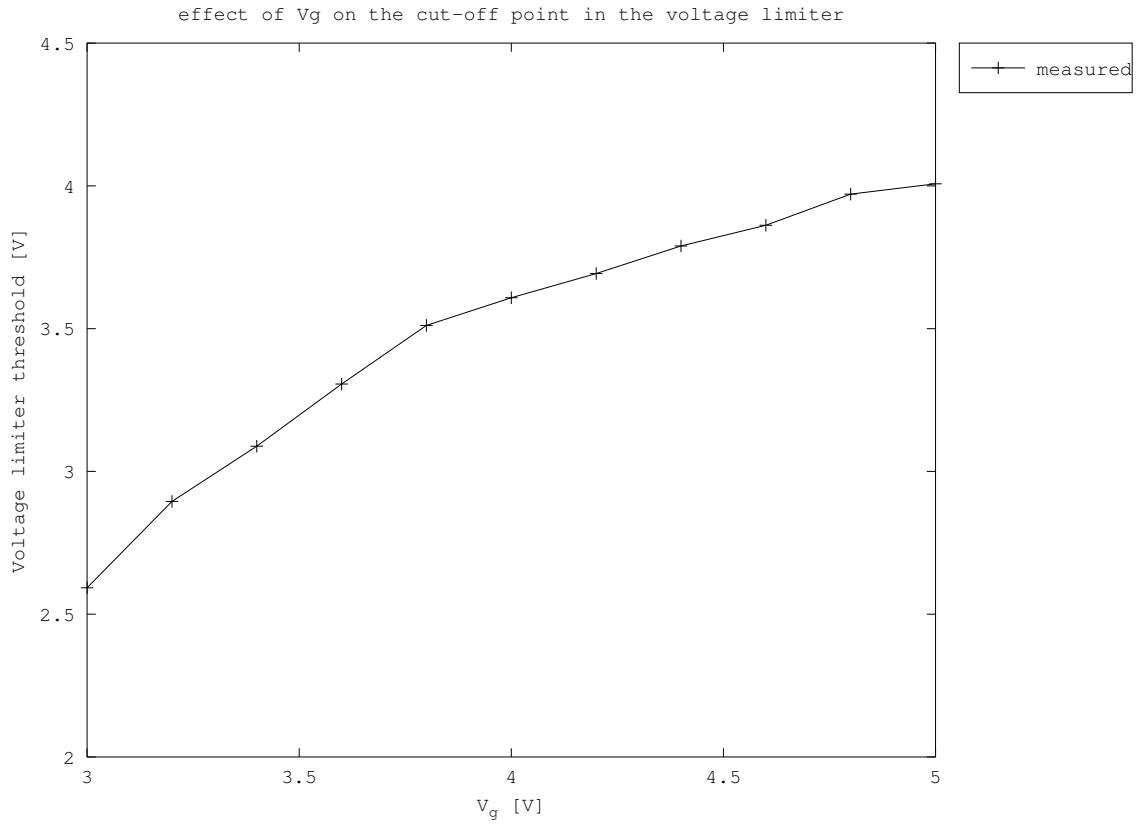


Figure 20: voltage limit as a function of  $V_g$

## 6 GaN sensors with ROIC

After the ROIC is characterized with constant controlled current sources, the next step is to attach it to the GaN sensors. The target range of operating voltages for the GaN sensors is 0 to -100 V. The primary interest lies in the I/V characteristics of the system. Because the same cations need to be performed all the time, it is worth to automate the setup one step further to save time.

### 6.1 Setup

In order to automate the measuring process further, the oscilloscope is connected to the laptop by cable, and directly controlled by `LabVIEW`. LabVIEW automatically acquires the required waveforms from the oscilloscope, and calculates the slope in real time. This action is repeated and used to accumulate data points for the  $I/V$  curve. When the program is finished, the processed data is stored. A bashscript collects all the data and calls `octave-cli` to put the results in a plot. There are two ways, that have been used to control the bias voltage of the GaN sensors. The first method is to use the arbitrary function generator (AFG) on the oscilloscope to generate a DC voltage between -2.5 and 2.5 V. A voltage amplifier with a gain of 10 is then used to achieve a range of -25 to 25 V that is directly controllable in `LabVIEW`. This allows `LabVIEW` to automatically sweep the bias voltage. However, the range of -25 to 25 V does not cover the target bias voltage range. Therefore, in order to increase the range further, a second method is used. This time the bias voltage is controlled manually with a voltage source. The oscilloscope measures both the input and output voltage. `LabVIEW` then calculates  $x$  and  $y$  coordinates repeatedly. This method provides the operator with full control over which part of the  $I/V$  curve is measured.

### 6.2 Calculation of current

The calculation of the current is done in `LabVIEW` in realtime, and to accommodate for that, the calculation of the slope is different. First a voltage threshold, and a time threshold is set. Then it is calculated when the slope crosses either of those thresholds. That point is used together with the starting point to calculate the slope. Again in order to calculate the input current, the measurement is corrected for source follower, and the slope divided by the capacitance.

### 6.3 External noise

One of the problems in the project was the susceptibility of the setup to noise. Throughout the project alterations were made to improve the SNR. The main improvements included rerouting of power cables, unplugging devices from the power grid, changing all long cables for shielded coax cables, and shielding the breadboard with metal plates. The measurements done in this section are therefore a lot less noisy than the measurements used for the characterization of the GaN sensors, and a lot less averaging is required for a stable output.

### 6.4 Automatic bias voltage sweep

Measurements in this section are acquired using the automatic bias voltage sweep. First the performance in forward bias is investigated. The result of these measurements are shown in fig. 21. The VBO channel is used for the measurements because of the large currents. There are several observations that can be made using this plot. First of all, there are several pins that appear to be

unaffected by the input voltage. This is not due to the GaN sensors, but because the ROIC channel broke after a certain point. This is most likely because the input was accidentally connected to a ground pin, which puts the high voltage directly to the input of the ROIC. A second observation is that the reset value of the VBO cannot be contained for large input voltages. This most likely means that the amount of current that is put into the ROIC is larger than the op amp in the ROIC can keep up with. Using an external current meter, the maximum amount of current the opamp can compete with is approximately  $15 \mu\text{A}$ . Finally it is interesting to observe that there is a substantial variance across the different devices. In order to test whether this variance is due to noise or due to variance across devices, a second set of measurements are made. This time only a single device is measured. The results are shown in fig. 22. These measurements show that the variance over different measurements is relatively low, which means that the observed variance in fig. 21 is mostly caused by variance across different devices.

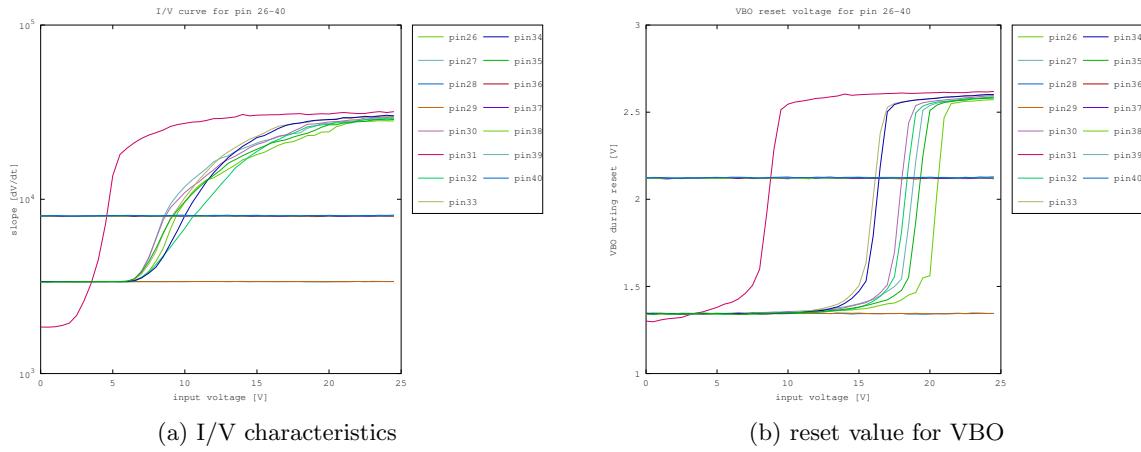


Figure 21: The slope and reset values for the VBO of pin26-40

Next up is the reverse bias performance. The I/V characteristics for several pins are shown in fig. 23. The jumps to negative current between 0 and  $2.4\text{ V}$  is due to the ground of the ROIC input being  $2.4\text{ V}$ . Therefore for lower voltages, the current flows into the opposite direction. The numbers are not representative for the actual current though, because the ROIC and measurement method are not designed for that direction of current. The main observation that can be made is that the voltage range available in the current setup is insufficient to observe the most interesting part of the  $I/V$  characteristics.

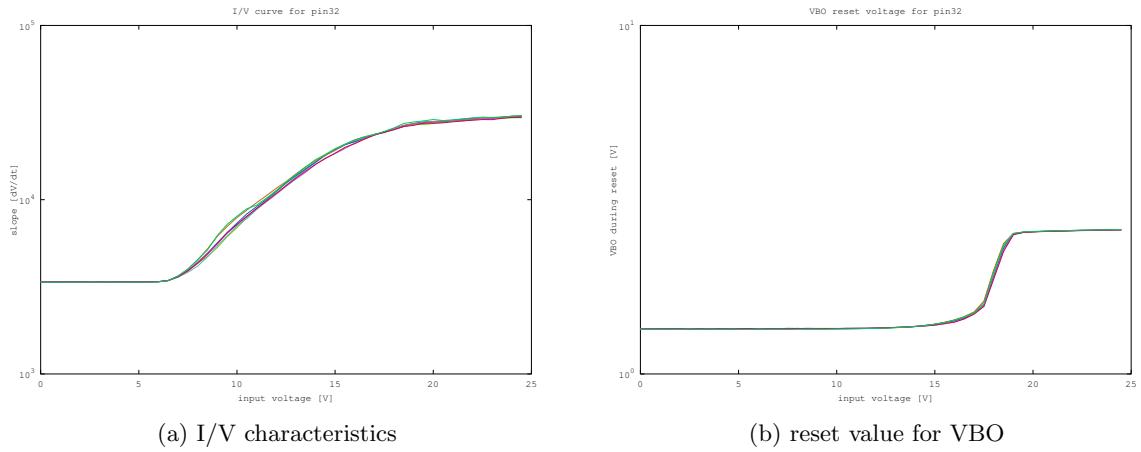


Figure 22: The slope and reset values for the VBO of pin32 repeated multiple times to test variance across measurements

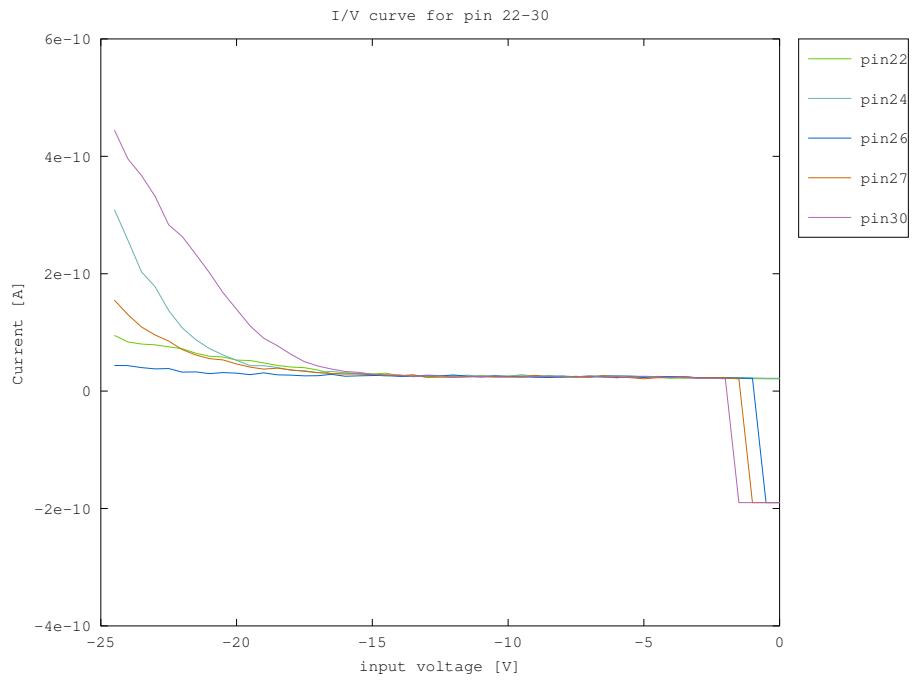


Figure 23: Voltage to current characteristics for several GaN sensors

## 6.5 Manually controlled bias voltage

To get to higher bias voltages, the bias voltages are manually controlled. This section will analyse measurement results based on individual sensors to determine both the GaN sensor and ROIC performance.

The  $I/V$  characteristics for pin 21 on the chip are shown in fig. 24. Note that the pin number indicates the GaN sensor on a chip that is connected. The results in this plot match with the expected behavior of GaN sensors based on previous measurements. There is a small exponential increase in current for low bias voltages. At a high bias voltage the device goes into breakdown with a steep exponential increase.

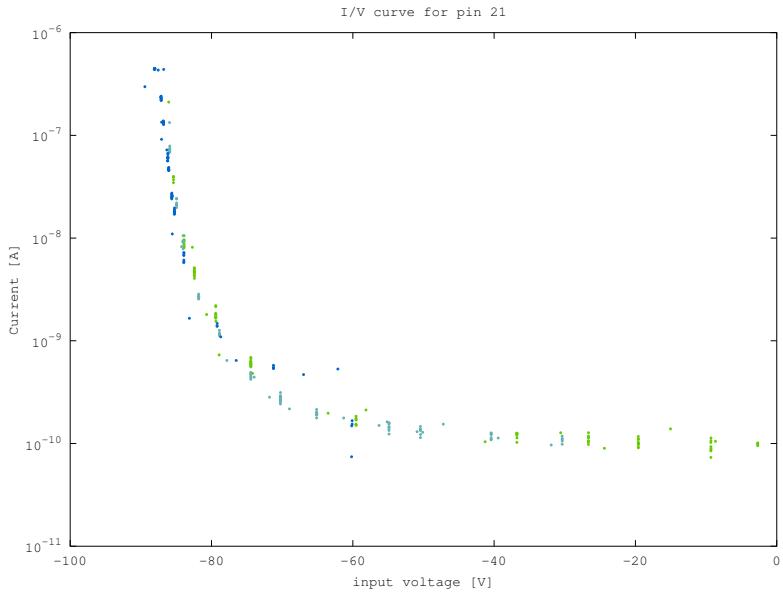


Figure 24: Voltage to current characteristics for a single GaN sensor

Figure 25 shows a different behavior, with no change in the exponential slope. The flat area for very high bias voltages is due to the limit of the source follower. The reason for this might be that the breakdown voltage lies at a higher bias voltage than what can be observed with the current setup.

Figure 26 shows the behavior of a different sensor. The behavior looks nothing like the previous observations which is most likely due to a defect in the sensor. The green OUT points can not rise to a higher value than approximately  $380\text{ nA}$ . This limit is caused by the maximum slope on the source follower. In order to extend the reach of the ROIC further, the VBO is used. As concluded in section 5.4.3, the VBO can handle higher voltages because of the higher capacitance. Combining VBO and OUT therefore allows for a large dynamic range.

Figure 27 and fig. 28 show plots for a sensor that is illuminated by a UV source. The wavelength and power of the UV source are unknown, so the measurements can only be used as an indication. One can see that the dark current has a steeper slope than the UV light. This means that a clear difference is observable for low bias voltages, but the UV loses significance when the dark current

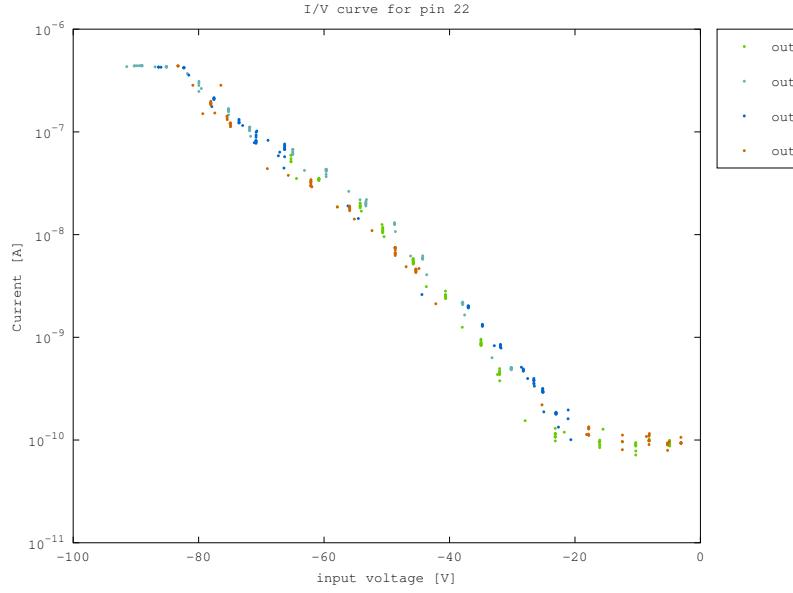


Figure 25: Voltage to current characteristics for a single GaN sensor

increases to higher levels.

Figure 29 shows a set of waveforms for varying bias voltages, where a UV source is either turned on or off. The plot illustrates that the difference between dark and UV illuminated is clearly observable. Again with the current setup there is no information available on the intensity of the illumination.

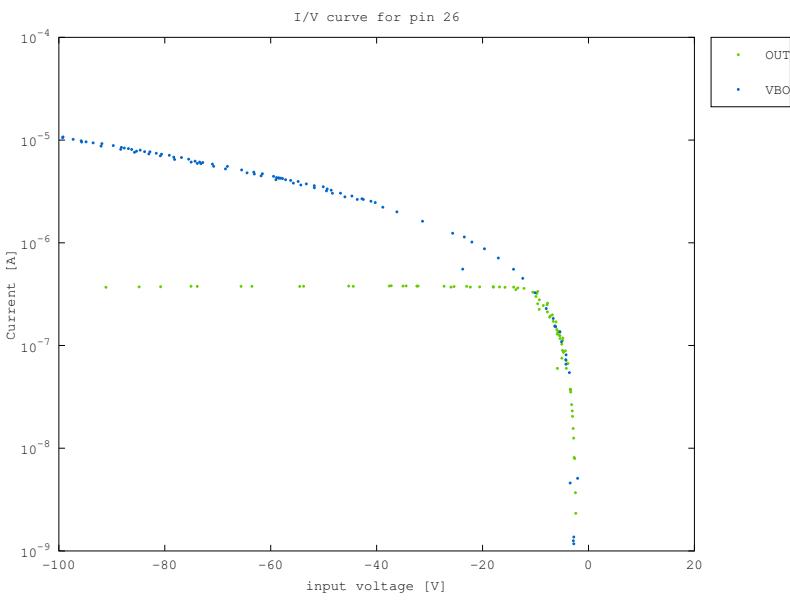


Figure 26: Voltage to current characteristics for a single GaN sensor

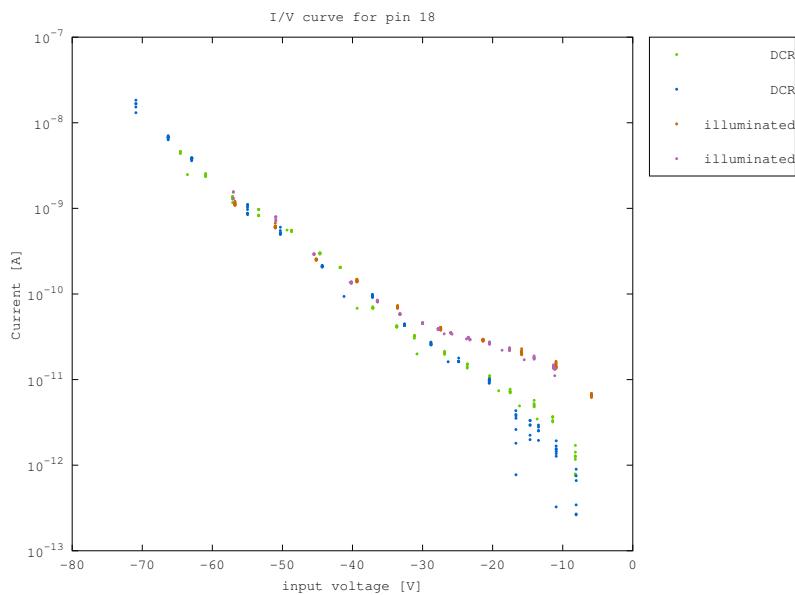


Figure 27: Voltage to current characteristics for a single GaN sensor

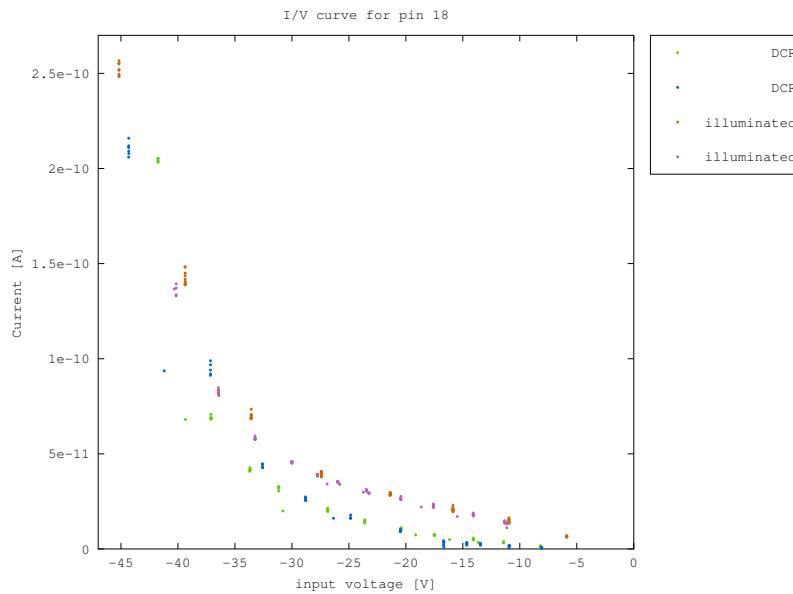


Figure 28: Voltage to current characteristics for a single GaN sensor

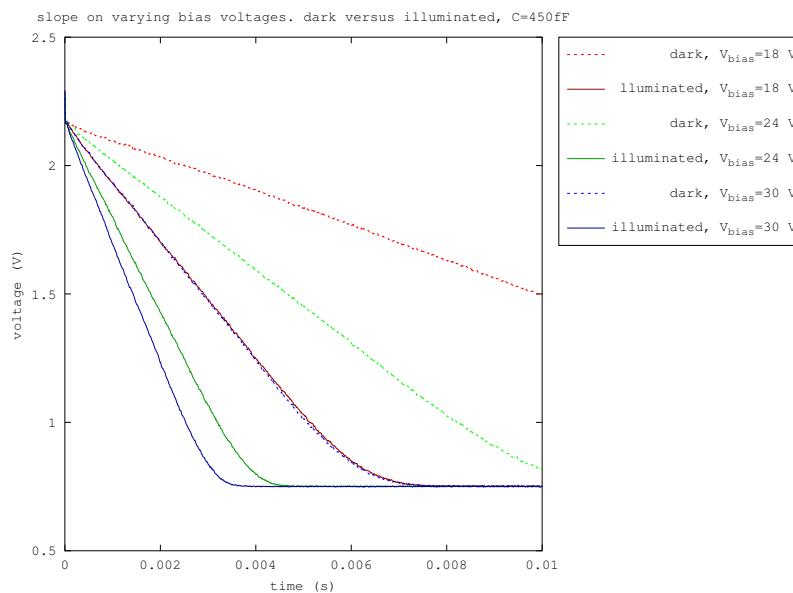


Figure 29: Waveform plots for UV illuminated and dark environments

## 6.6 Very high bias voltage

Besides the  $I/V$  measurements, a second observation was made. Specifically, the performance of the ROIC with the GaN sensors for very high bias voltages between 90 and 100 V. When the amount of current reaches a certain level, the ROIC is no longer able to maintain its reset values. This means that during reset, the op amp inside the RIOC is not able to keep up with current produced in the GaN sensor. This causes the input of the integrator to rise to the point that the voltage limiter kicks in. There are two things happening here. This means that the ROIC is no longer functioning. There is a second more problematic effect however. When this modus is kept for too long and/or at a voltage that is too high, the ROIC creates a spark. After that the ROIC is no longer useable. Because of this, three ROICs were damaged. A photo of the inside of the three packaged chips is shown in fig. 30. The burns on the chips are on different wires, but for all chips, the burned wire is the input of the channel that was used at that time. For all three cases, did the wirebond melt and disconnect. However, this is most likely a secondary effect. Especially because the entire chip stops functioning, which should not be the case if only the wirebond fails. Another observation is that the VBO output is pulled to ground, which means that the input is most likely shorted to ground.

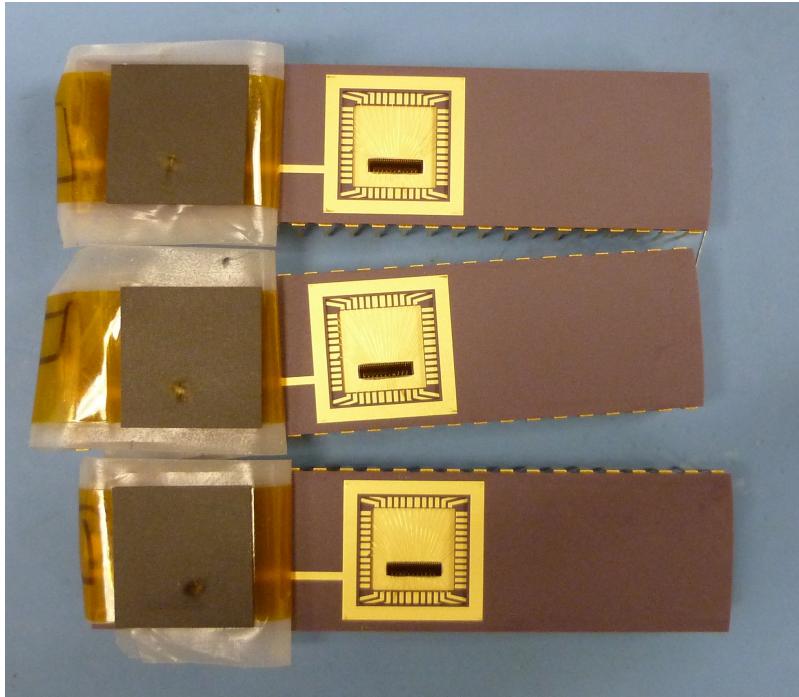


Figure 30: Inside of packaged ROIC chips after being exposed to too much power

This effect is currently the largest constraint to measuring the GaN sensors at high bias voltages, because the ROIC dies before the GaN sensors do.

## 7 Conclusions

The main goal of this project was to characterize the behavior of the readout circuit that was designed specifically to work with GaN photodiodes.

A setup was constructed that allowed for a quick and precise way of measuring the ROIC and GaN photodiodes using a digital oscilloscope connected to a computer. Programs were constructed to extract the input current from the measured waveforms.

The behavior of the source followers was characterized, to be able to compensate for its behavior in later stages. The performance of the integrator was characterized and the effective feedback capacitances were calculated in order to correctly address the relationship between the slope and input current. The performance of the voltage limiter was investigated, and the tunability of the voltage meter determined.

A limitation on the ROIC was found where a large input current and voltage result in the destruction of the ROIC, and an analysis was performed to the cause of this.

Various GaN photodiodes were measured and analyzed. Finally the performance of GaN photodiodes with a UV source was analyzed.

## 8 Recommendations and future work

Based on the observations and analysis performed, several recommendations can be made for future versions of the ROIC.

### **Stronger Op amp**

The op amp in the integrator should be able to draw more current. This is necessary to observe the GaN sensors above breakdown. Judging by the observations made with the GaN sensors, at least an order of magnitude is needed to observe all the way up to 100 V. Note that the pull down power of the op amp can be increased on the current chip by changing the bias voltage on the pull down network. However, the increased speed will not be enough to address the issue.

### **Separate channels**

In the current design a lot of elements are shared among different channels. The problem with this is that if one of these elements stops working, the entire chip is destroyed. There are a lot of unused pins on the input side of the chip that could be utilized to split up more elements on the chip.

### **Capacitance choices**

The observed capacitance options are 400 fF, 350 fF, 200 fF and 150 fF. It would be preferable to have a larger range of values to choose from, and most importantly, the lowest capacitance should be lower than it currently is. This increases the slope, and therefore allows for faster measurements and/or lower currents. The sample speed is currently limited to the range of 1 kHz.

### **Faster source follower pull down**

The fastest observable slope on the output of the integrator is limited by the pull down of the source follower. A stronger pull down would result in a wider range of observable input currents. The pull down in the current ROIC can already be increased by changing the bias voltage on the pull down network, but this will not be enough of an increase to address the problem entirely.

### **A circuitboard in a metal case**

In order to improve the SNR, it would be desireable to use a circuitboard housed in a metal case to minimize the length of the wires, and shield the circuit from outside interference.

### **Dedicated slope detection**

Currently an oscilloscope and computer are used to determine the slope. In order to scale up the technology, a dedicated solution must be found. One solution could be to use a sample and hold connected to an ADC. It is important however, that the signal controlling the sample and hold, is synchronized with the reset signal.

### **Array**

The next step is to construct an array of ROIC channels and connect them to an array of GaN sensors. A solution for this could be to connect a sample and hold to all the outputs on the ROIC, and using a multiplexer with an ADC to read out the values.

### **Other future work**

Additional characterization needs to be performed to determine how much power can be dissipated before damaging either the ROIC or the GaN sensors. This information can then be used to determine an appropriate frequency for the reset signal, and an appropriate setting for the voltage limiter.

The ROIC is only tested on one GaN sensor design. It should be used to observe different GaN sensor designs as well.

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