Summer Internship (July-September 2016)
Characterization and testing of CMOS Readout circuit for GaN photodiodes

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2 Introduction

2.1 Motivation

UV sensors have numerous applications including oberservation during assembly and the oberservation of outer space. One of the challenges of UV sensors is to deal with sensitivity to visible light, which is the main product of solar irradiation. Gallium Nitride (GaN) has intrinsic solar blindness, which makes it a prime candidate for UV sensors. The material can also still be used in solid state devices. There is currently no alternative to this combination of solarblindness and solid state. This research project focusses on the nontrivial task of designing and characterizing a suitable readout circuit for a GaN sensor. The project builds on the work of Padmanabhan et al. ???, who designed a first version of a Readout Integrated Circuit (ROIC). The main goal of this project is to characterize the ROIC, evaluate it's performance when coupled with GaN sensors, and propose improvements for future ROICs.

2.2 Gallium Nitride UV Sensors

3 Readout design

The ROIC used in this project is designed and manufactured by Padmanabhan et al. ???. The design features three main components. A voltage limiter, an integrator, and two source followers. A schematic of the circuit is shown in fig. 1.

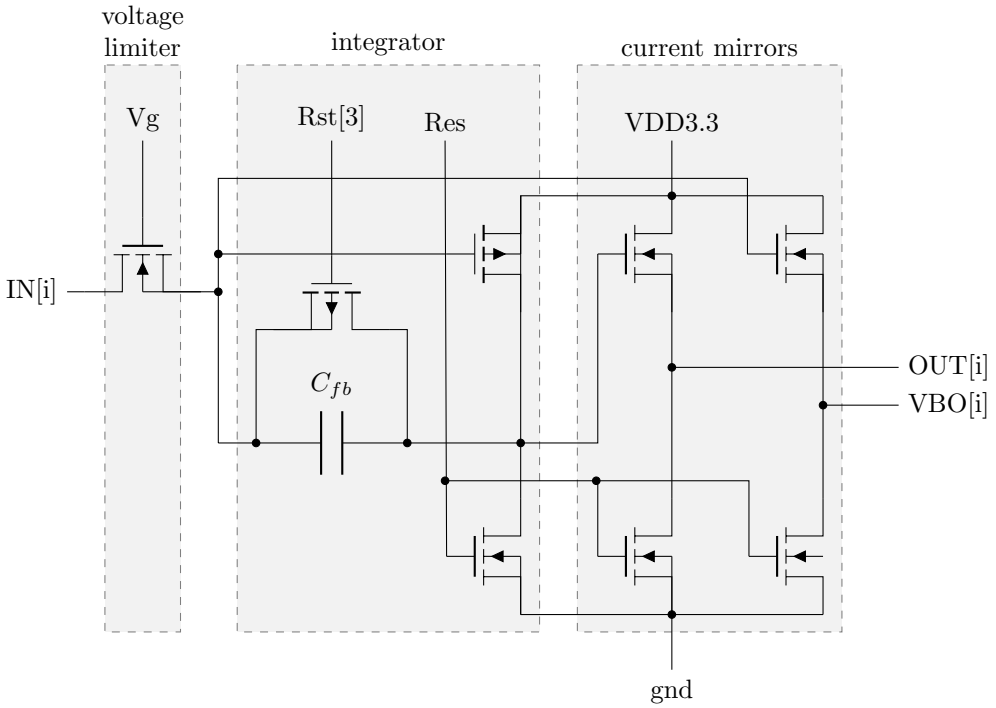


Figure 1: Schematic of ROIC channel

The voltage limiter limits the maximum voltage in the ROIC to protect both the ROIC and the GaN sensors from too much power dissipation. The integrator translates the accumulative amount of charge that has entered the device into an output voltage. The source followers allow for an external readout without affecting the behavior of the ROIC. Section 3.1-3.3 describe the different components in more detail.

3.1 Voltage limiter

The voltage limiter consists of a single transistor with a gate voltage V_g that can be controlled externally. The limiting effect uses the property of cutoff when $V_{GS} \leq V_t$. This means that $V_S \leq V_G - V_T$. A $V_T \approx 0.7$ and a $V_G = 4.5\,V$ for example, would yield a maximum $V_S \approx 3.8\,V$. The performance of the voltage limiter in practise will be investigated in ???.

3.2 Integrator

The integrator transforms the accumulated amount of charge at the input into a change in output voltage. The change in output voltage can be calculated using eq. (1). A schematic of the circuit is shown in eq. (1)

$$\Delta V_{out} = \frac{-1}{C} \int_0^T I\,dt = \frac{-q}{C} \tag{1}$$

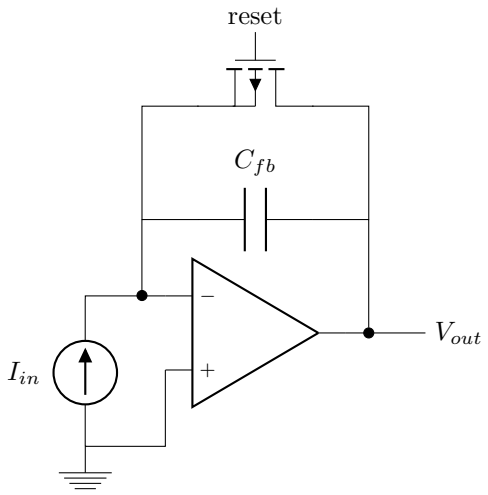


Figure 2: schematic of integrator

The input of the integrator is connected to the ouput of the voltage limiter. The reset switch is controlled externally and used to reset the integration capacitance C_{fb}. Note that the relationship between change in voltage and input current is negative. This means that the output voltage drops with a positive input current. The behavior of the integrator is further investigated in ???

3.3 Source follower

The source followers protect the circuit from external influences. There is one source follower connected to the inoput and one to the output of the integrator to be able to oberserve both the in and output on an unintrusive manner. A schematic overview of a the source followers is shown in fig. 3. Note that the relationship between V_{in} and V_{out} is non-linear. Also note that the speed at which the source follower can change slope is limited by the bias current for both the pull up and pull down. It is therefore possible that the input rises or falls at a faster speed than the source follower can keep up with. The behavior of the source followers is further investigated in ???

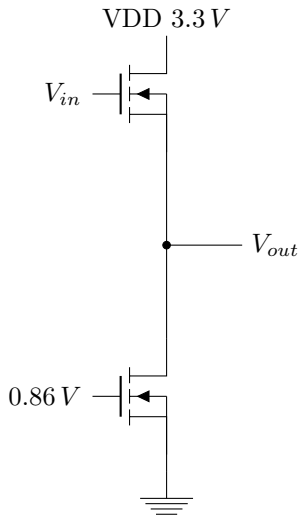


Figure 3: Schematic of source follower

4 Steady state ROIC characterization

The first part of the characterization process is the behavior in steady state. In particular the period where the reset is on. This state has no time component in it, and therefore can be observed with a relatively simple setup.

4.1 Setup

The first version of the setup consists of a breadboard with the ROIC, several voltage sources, and an oscilloscope. The layout of the breadboard is shown in fig. 4. All pins on the ROIC that are non listed are floating.

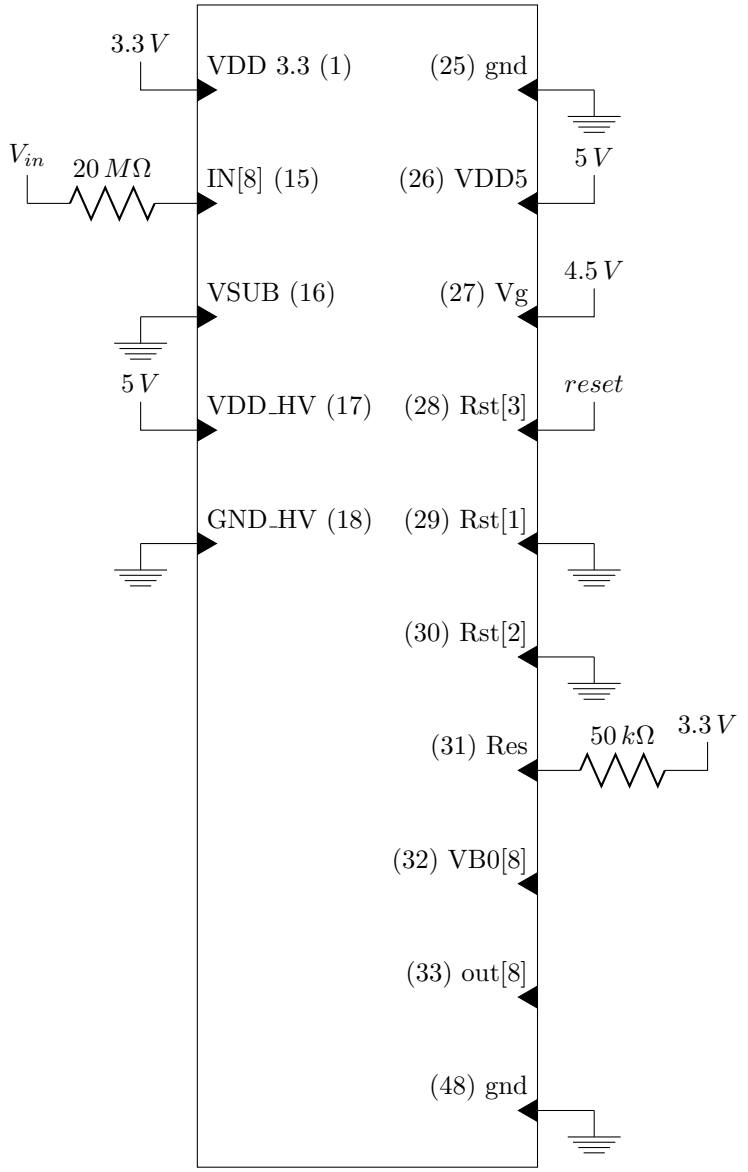


Figure 4: Schematic of breadbord

4.2 Behavior during reset

Because of the PMOS reset transistor, the circuit is in reset mode when reset=0 V. The results of measuring in this state are shown in fig. 5. The measured values match with the simulation results performed by Padmanabhan et al. ???. Note the input voltage of 2.4 V. This is an important value, for it is used to determine the input current, when a voltage source and resistor are used for input. Also note that the output voltage of VBO is 1.4 V, while the input is 2.4 V. This already shows

that the source followers don't match the input 1:1, and this will be further investigated in ???

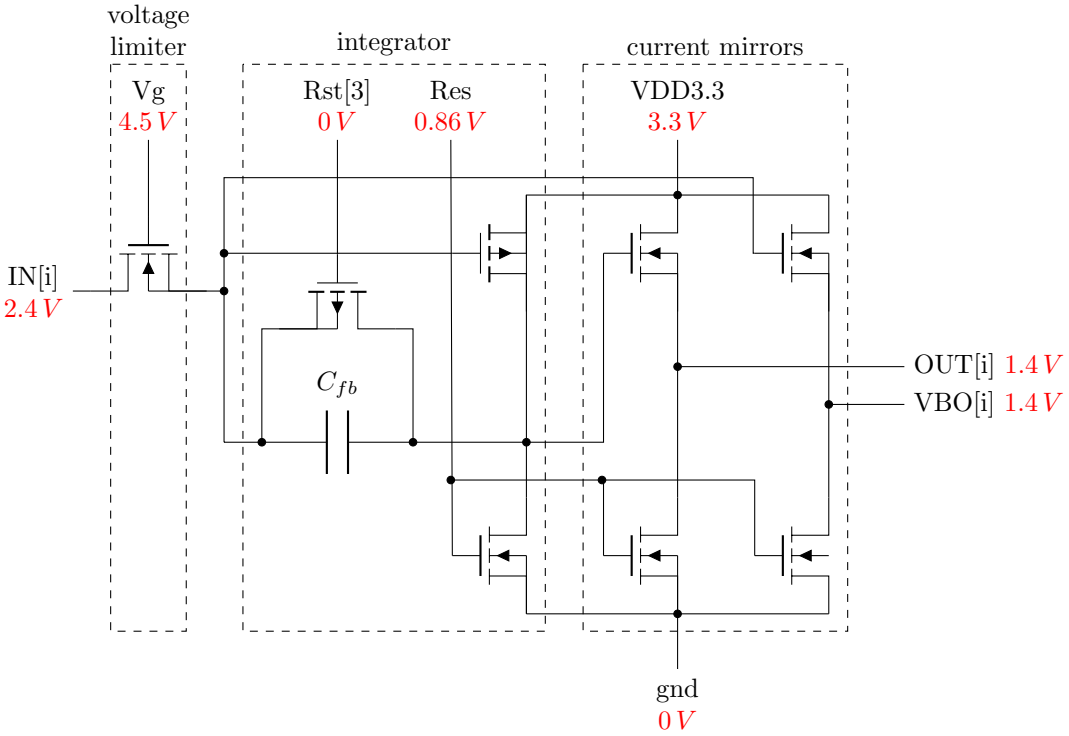


Figure 5: Schematic of ROIC channel template

5 Dynamic ROIC characterization

The next step is to look at the dynamic behaviour of the ROIC under varying input currents. The aim of this section is to characterize the dynamic behavior of the three different components of the ROIC seperately: The source followers, integrator and voltage limiter respecively. In order to measure this, a more sophisticated setup is required.

5.1 Setup

The desired measurements require a lot of samples and in order to observe a slope, waveforms. Also the device needs to be reset in order to oberserve the dynamic behavior of the integrator. In order to address all those issues, the function generator in the oscilloscope is used to create a periodic pulse for the reset. The trigger function of the oscilloscope is used to observe the period around the rising edge of the reset. The averaging function on the oscilloscope is used to reduce the effect of noise. The input voltage is manually controlled through a voltage source. The observed waveforms are stored to a usb and transported to a computere. On the computer, these waveforms are further processed in `octave-cli` (octave command line interface), which generates plots that are directly inserted into pdf. A bashscript is used to automate all processes on the computer.

This setup provides a convenient method of processing a lot of data, without an insurmountable amount of manual labor.

5.2 Source followers

The design of the source follower is described in section 3.3. In order to characterize the behavior of the source follower, a voltage source is directly connected to the input of the ROIC. This forces the output of the voltage limiter to the same value as the source follower, as long as the voltage limiter is not cut-off. The input of the source follower connected to the VBO output, is directly connected to this output, and is therefore fully controllable. The output of this source follower can be directly be observed. This means that the characteristics of the source follower can be measured directly. Note that the source follower connected to the output of the integrator is identical, which means that only one needs to be characterized. Figure 6 shows both the measured data and a fitted line with the formula $vbo = 0.827 v_{in} - 0.624$. In order to avoid pile-up it will be assumed that this formula characterizes the performance of both source followers for $1 < V_{in} < 4\,V$.

5.3 Integrator

The measurements of the behavior of the integrator are devided into three sections. Section 5.3.1 will focus on the output of the ROIC for low currents. Section 5.3.2 will do the same, but this time for currents that are a lot higher. Finally section 5.3.3 will look at the behavior of VBO, and investigate the viability of using the input follower as a secondary readout. Note that all plots are not what is directly observed at the output. All results have compensation for the behavior of the source followers.

5.3.1 Standard behavior

This test aims to address the basic relationship between input current and output voltage. Figure 7 shows the setup used for this test. Channel 8 was used, so the end of the 20 $M\Omega$ resistor is connected

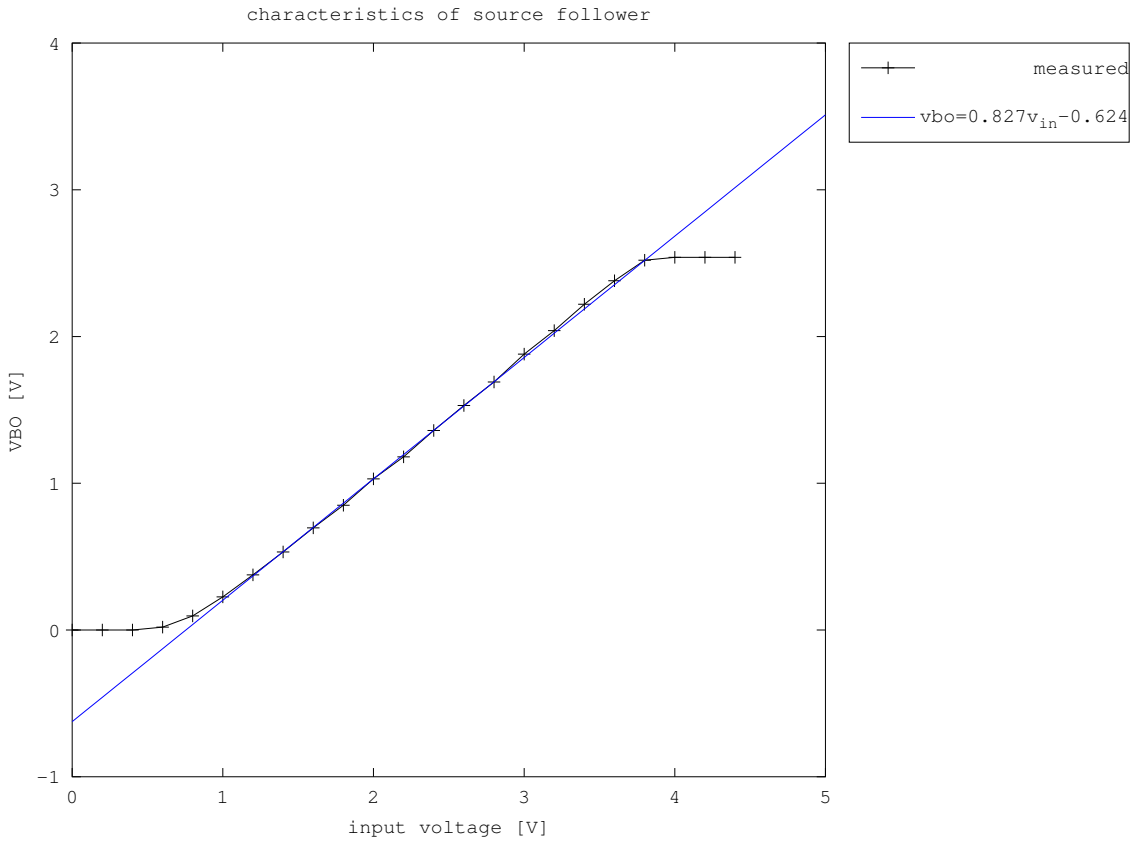


Figure 6: plot of the input voltage against VBO. This plot shows the characteristics of the voltage follower

to IN[8], and probes are connected to OUT[8] and VBO[8].

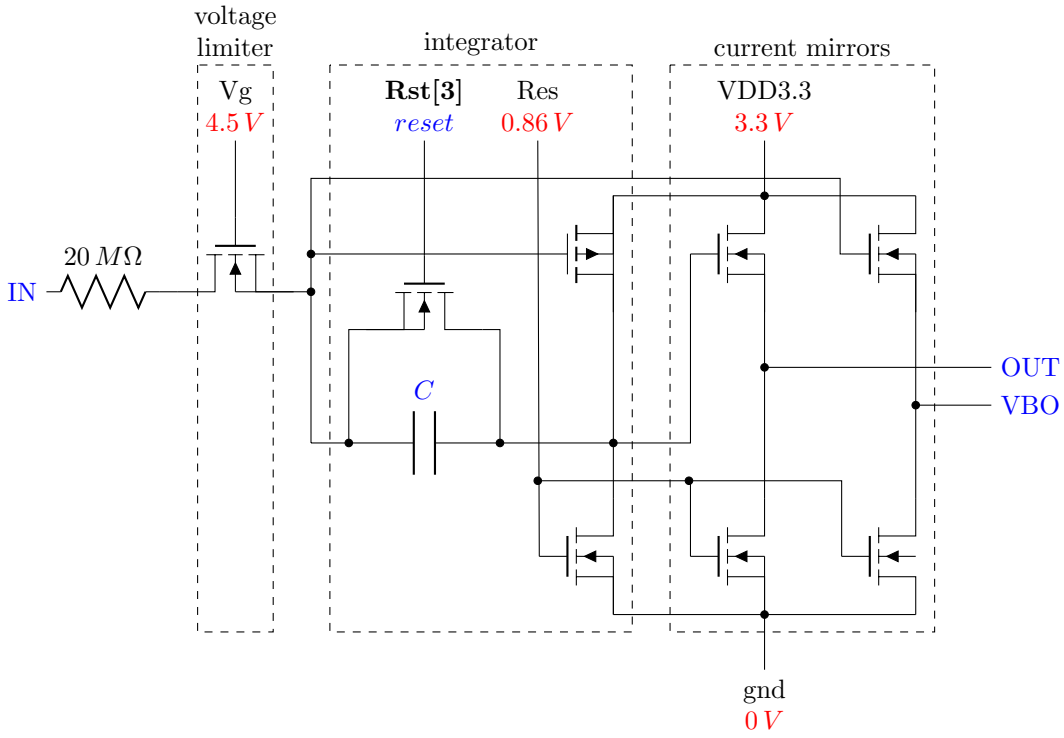
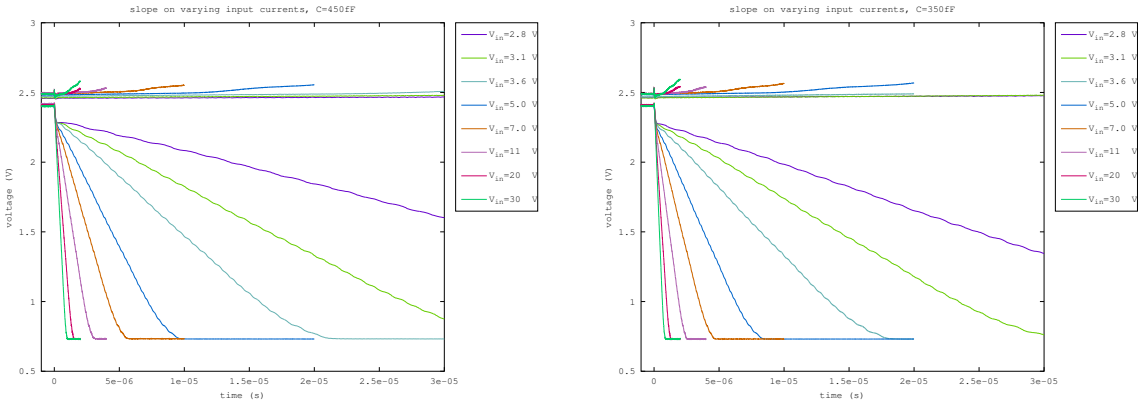


Figure 7: Schematic of ROIC channel template

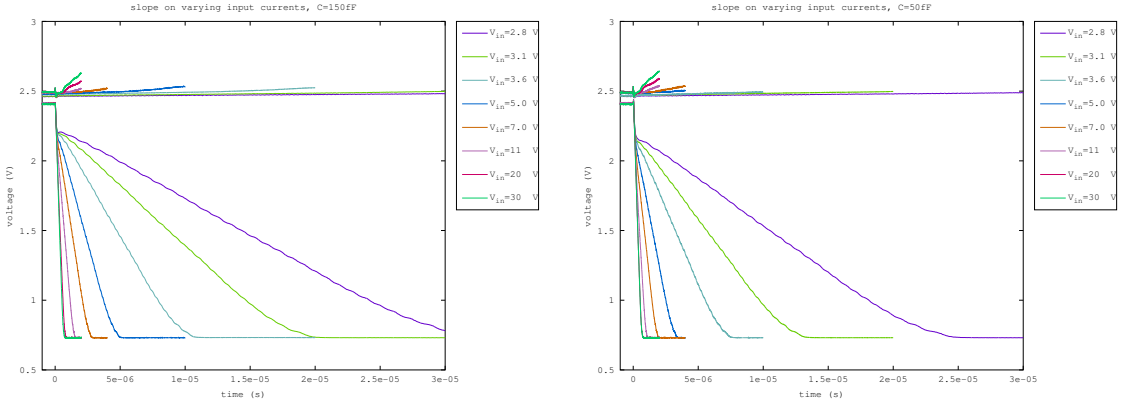
Figure 8 shows the time versus voltage plot of both the VBO and OUT for a constant input voltage. The rising and falling slopes are the VBO and OUT respecively. The timescale of this plot does not allow for much inside in VBO, but it does show some interesting results for the behavior of OUT. When the reset switches, the input node immediately loses some charge. Note that the oscilloscope matches the rising edge of the reset signal to time is $0\,s$, so this drop is at $0\,s$. When the reset is switched, a capacitance is removed almost instantly. It is interesting to observe that the slope immediately after the rising edge of the reset signal is constant for all input voltages. This means that the observed slope is not limited by the reset transistor, but by the source follower that tries to keep up. This observed slope is therefore the maximum rate at which the output node can be pulled down in the current set-up. Also note that the slope gets steeper when the integrator capacitance decreases. This matches the expected behavior of $\Delta V = \frac{-q}{C}$.

Figure 9 shows the same plot as fig. 8, but now the x axis is scaled with input current. This shows for fig. 8a and 8b that the relationship between output voltage and charge is equal across different input voltages. For fig. 8c and 8d however, one can see that the higher voltages lose this property. Another intersting observation is that when one looks closely at the plot, one can observe a small oscillation with a period that is constant with charge. Also the period is constant across different voltages. A hypothesis explaining this behavior has yet to be found.

Figure 10 shows the $\delta Q/\delta V$ against charge plots. Note that $\delta Q/\delta V$ is the capacitance. One can observe that while the capacitance is charging, the full value of the capacitancec can be observed, and when the capacitance is comopletely decharged, it behaves as if it is not there. One can use



(a) $C = 450\,fF$ (b) $C = 350\,fF$

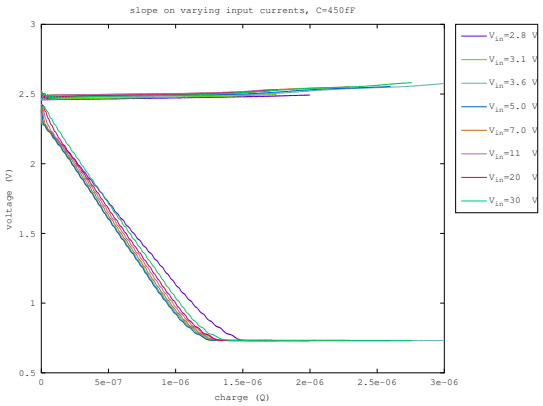


(c) $C = 150\,fF$ (d) $C = 50\,fF$

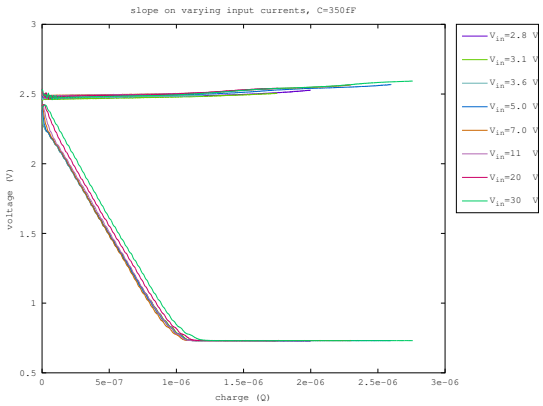
Figure 8: Expected versus measured charge up times for different input voltages. The input voltage is connected to the input through a resistor of $20\,M\Omega$

these plots to estimate the integration capacitance. The capitance for fig. 9a, 9b, 9c and 9d are approxiately $450\,fF$, $350\,fF$, $220\,fF$ and $180\,fF$ respectively.

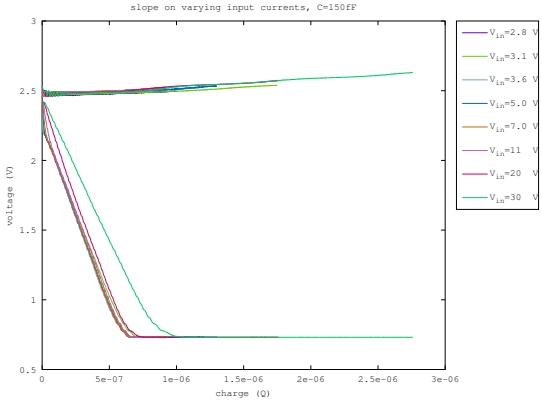
Figure 11 shows $\delta V/\delta t$ against input voltage for all capacitances. One can observe that all four have different slopes at first, but there appears to be a trend that they all converge to a value of $\delta V/\delta t \approx 3.2 \cdot 10^6$.



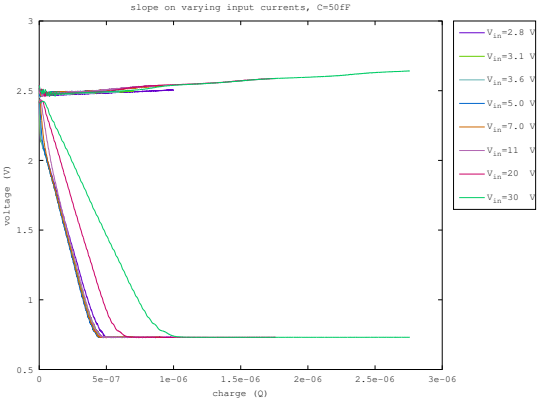
(a) $C = 450\,fF$



(b) $C = 350\,fF$

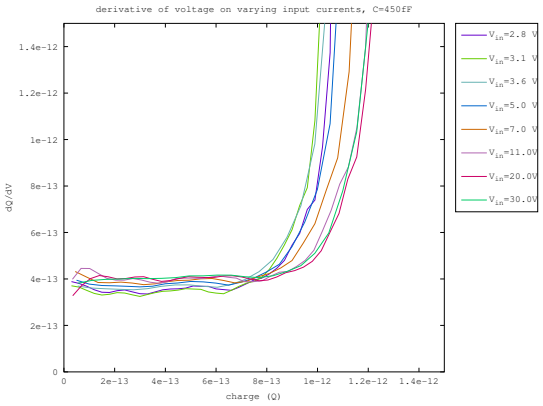


(c) $C = 150\,fF$

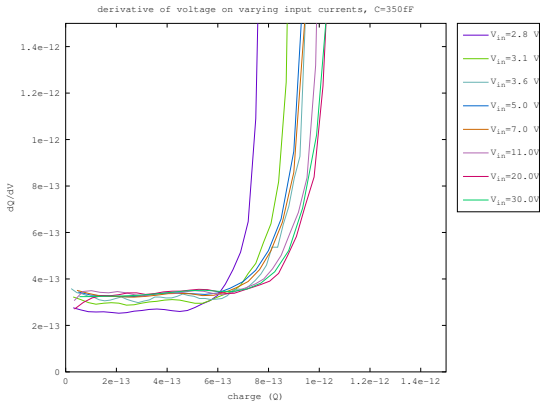


(d) $C = 50\,fF$

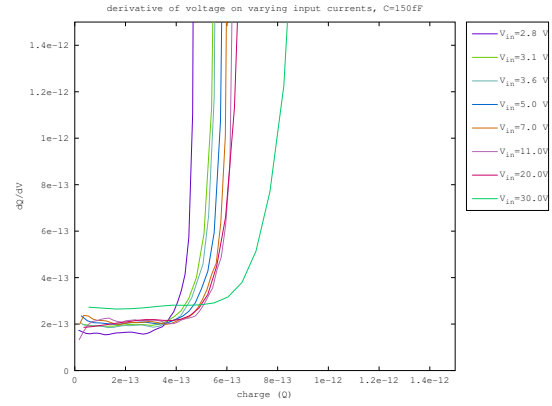
Figure 9: This plot is showing charge versus voltage



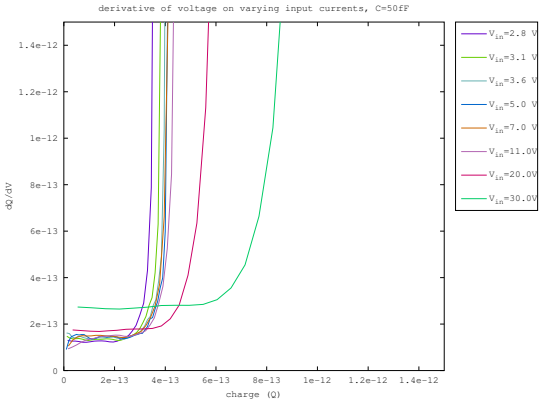
(a) $C = 450\,fF$



(b) $C = 350\,fF$



(c) $C = 150\,fF$



(d) $C = 50\,fF$

Figure 10: The plot shows dv/dt against time. The plot is in log scale, which allows for an easy read on the maximum slope and the time needed to discharge the integrator capacitance.

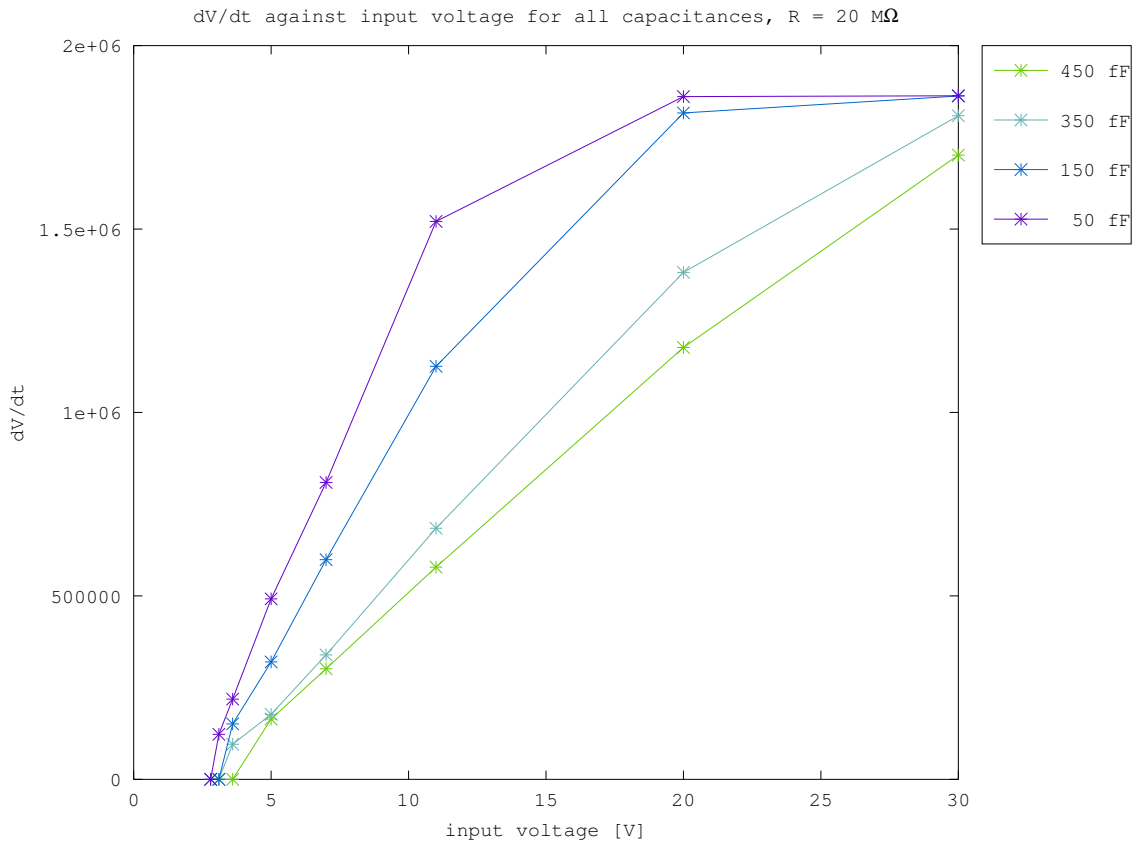
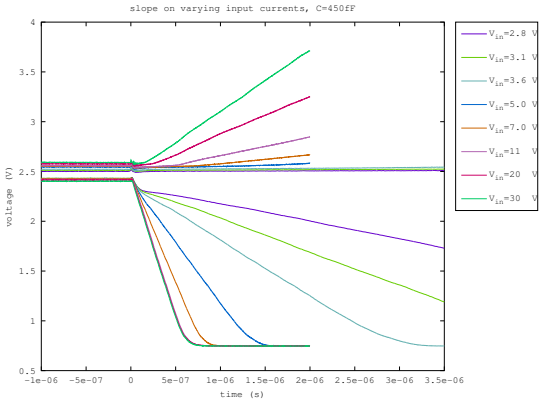


Figure 11: dV/dt against input voltage for all four capacitances. The x indicate the measurements.

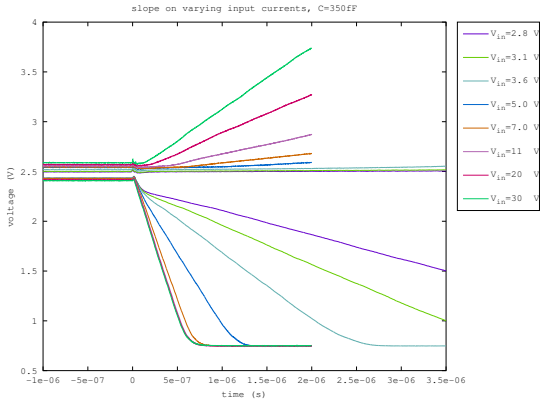
5.3.2 High current behavior

In this section the $20\,M\Omega$ input resistor is replaecd with a $4\,M\Omega$ resistor. The main goal is to observe the ROIC for very large currents.

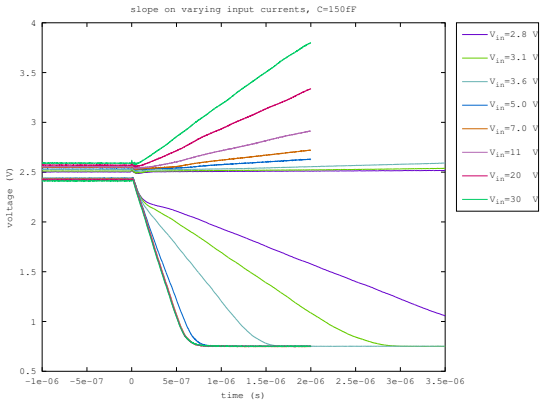
Figure 12 shows the same plot as fig. 8, but this time with larger currents. Where a minimum slope could be observed at fig. 8, it is more prevalent here. This also shows more information about the behavior of VBO. For small voltages the VBO does not increase, but as the voltages get larger, one can observe that the voltages of VBO start rising when the OUT is done with decharging. It is also interesting to note that VBO seems to be not affected by the minimum slope at OUT. This gives rise to the hypothesis that the OUT is limited by the source follower.



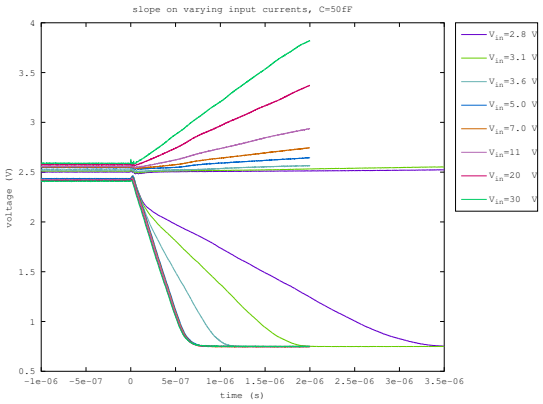
(a) $C = 450\,fF$



(b) $C = 350\,fF$



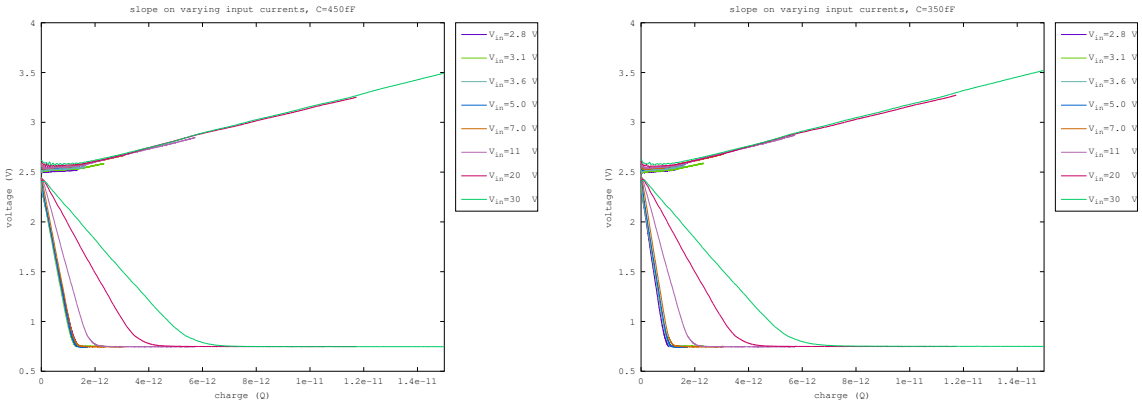
(c) $C = 150\,fF$



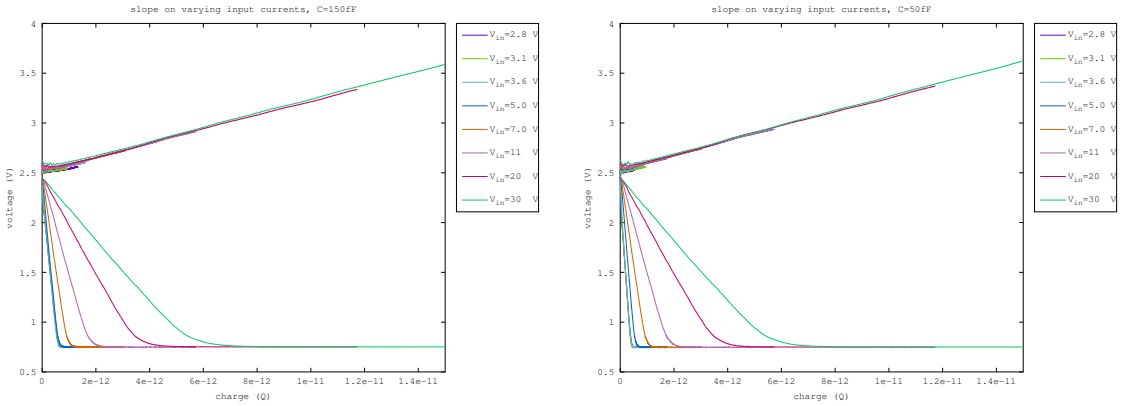
(d) $C = 50\,fF$

Figure 12: Expected versus measured charge up times for different input voltages. The input voltage is connected to the input through a resistor of $4\,M\Omega$

Figure 13 shows a similar plot as in fig. 9 but with higher currents. In fig. 9 one could observe that all currents fitted to the same line, but deviated at higher currents. This effect is also observed here, but in a stronger form. Which is to be expected.



(a) $C = 450\,fF$ (b) $C = 350\,fF$

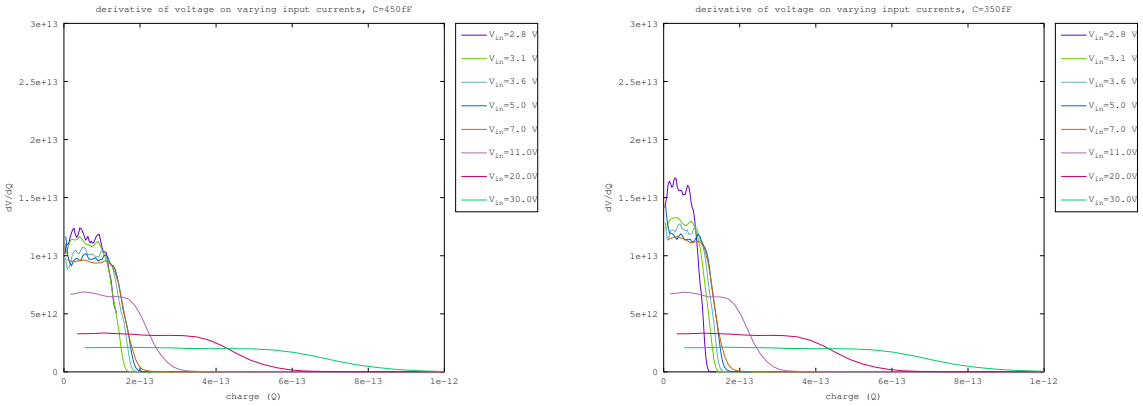


(c) $C = 150\,fF$ (d) $C = 50\,fF$

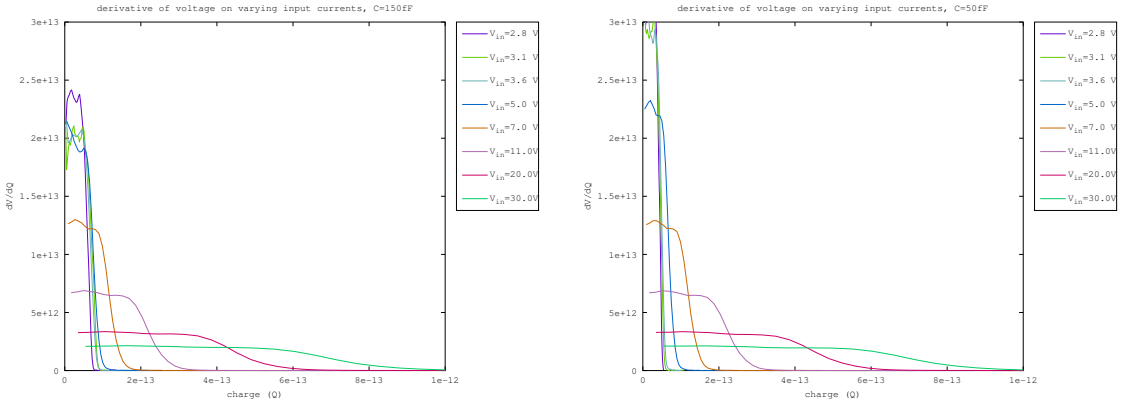
Figure 13: This plot is showing charge versus voltage

Figure 14 shows a plot of $\delta V/\delta Q$ against charge. Note that the behavior for the low voltages differ across the different capacitances, but that the high voltages are not affected by a change in capacitance. This observation agrees with the hypothesis that the output is not limited by the input current, but by the speed of the source follower at the output.

Figure 15 shows the same plot as fig. 11, but with higher current. This plot clearly shows that all four capacitance configurations saturate at a $\delta V \delta t \approx 3.1\,V$. This cannot be a limit applied to the input, because the capacitances are different. Therefore the output is limiting this, conform previous observations.



(a) $C = 450\,fF$ (b) $C = 350\,fF$



(c) $C = 150\,fF$ (d) $C = 50\,fF$

Figure 14: The plot shows dv/dt against time. The plot is in log scale, which allows for an easy read on the maximum slope and the time needed to discharge the integrator capacitance.

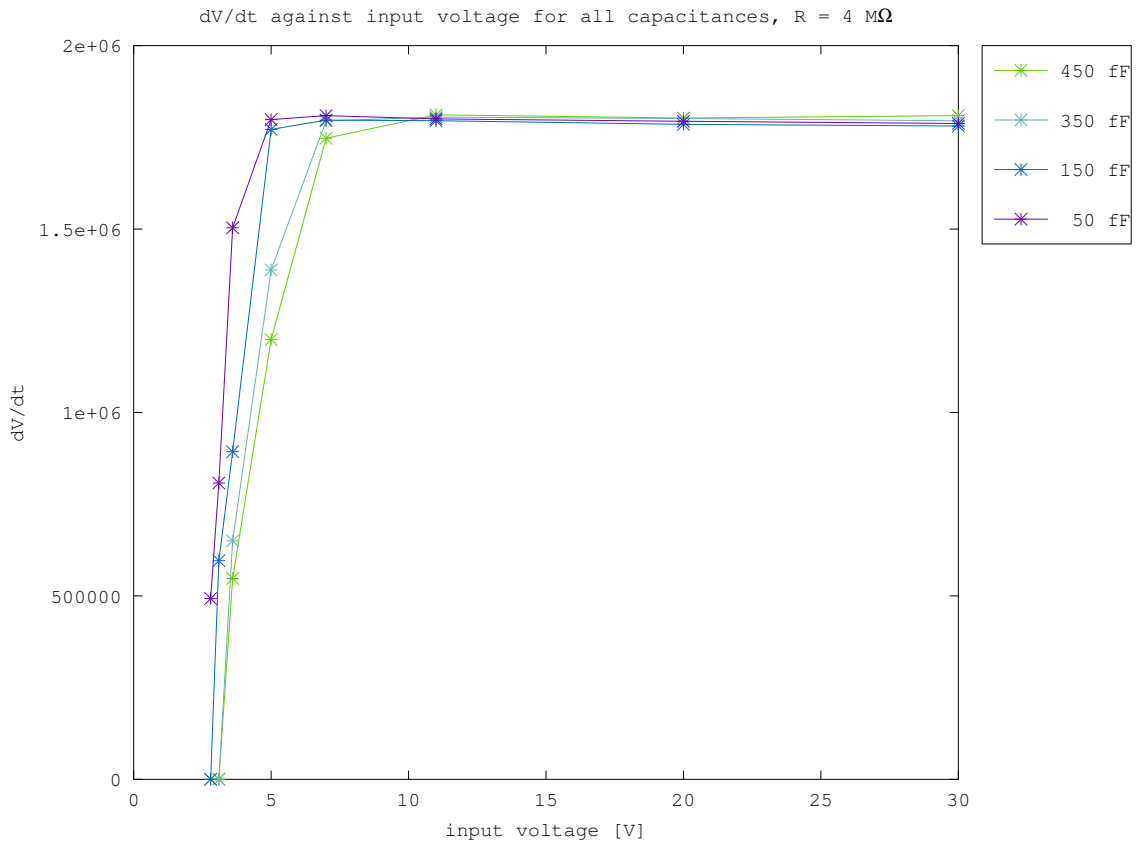
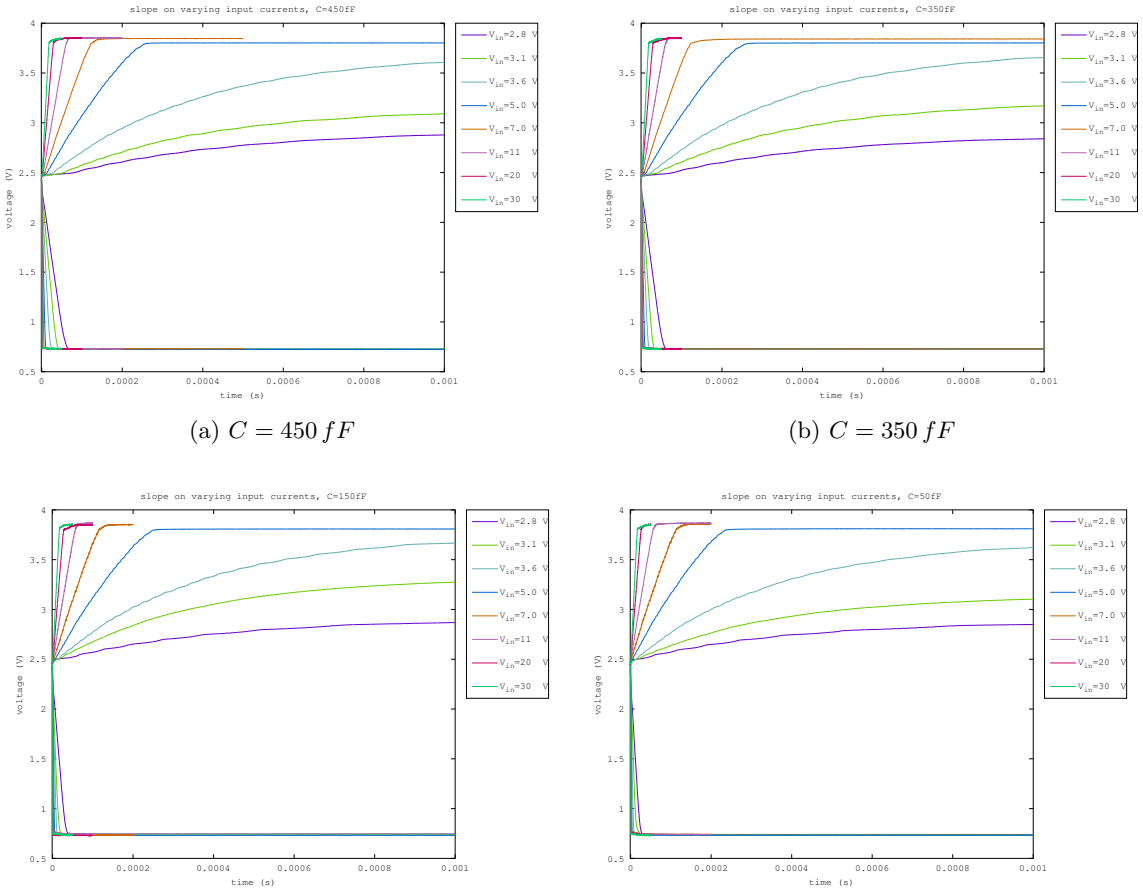


Figure 15: dV/dt against input voltage for all four capacitances. The x indicate the measurements.

5.3.3 VBO behavior

This section focusses on the output of the source follower that is directly connected to the output of the high voltage transistor connected to the input of the ROIC. The setup is identical to section 5.3.1, but the time scale is different to oberve the slower behavior of VBO.

Figure 16 shows the time against voltage plot. This are a couple of important observations that can be made from these plots. First and foremost: the behavior of the VBO is almost not affected by the capacitance. There is a difference however, in that the VBO starts rising as the OUT reaches zero. This means that the VBO for $450\,fF$ is slightly delayed when compared to $50\,fF$. It is also intersting to observe that VBO never increases above $3.8\,V$. This behavior is most likely due to the functioning of the voltage limiter that will be ivestigated later on. Finally one can observe that for very low currents, VBO does not reach $2.6\,V$. The reason for this is that the input reaches the voltage level of the power supply before the current limiter kicks in.



(a) $C = 450\,fF$

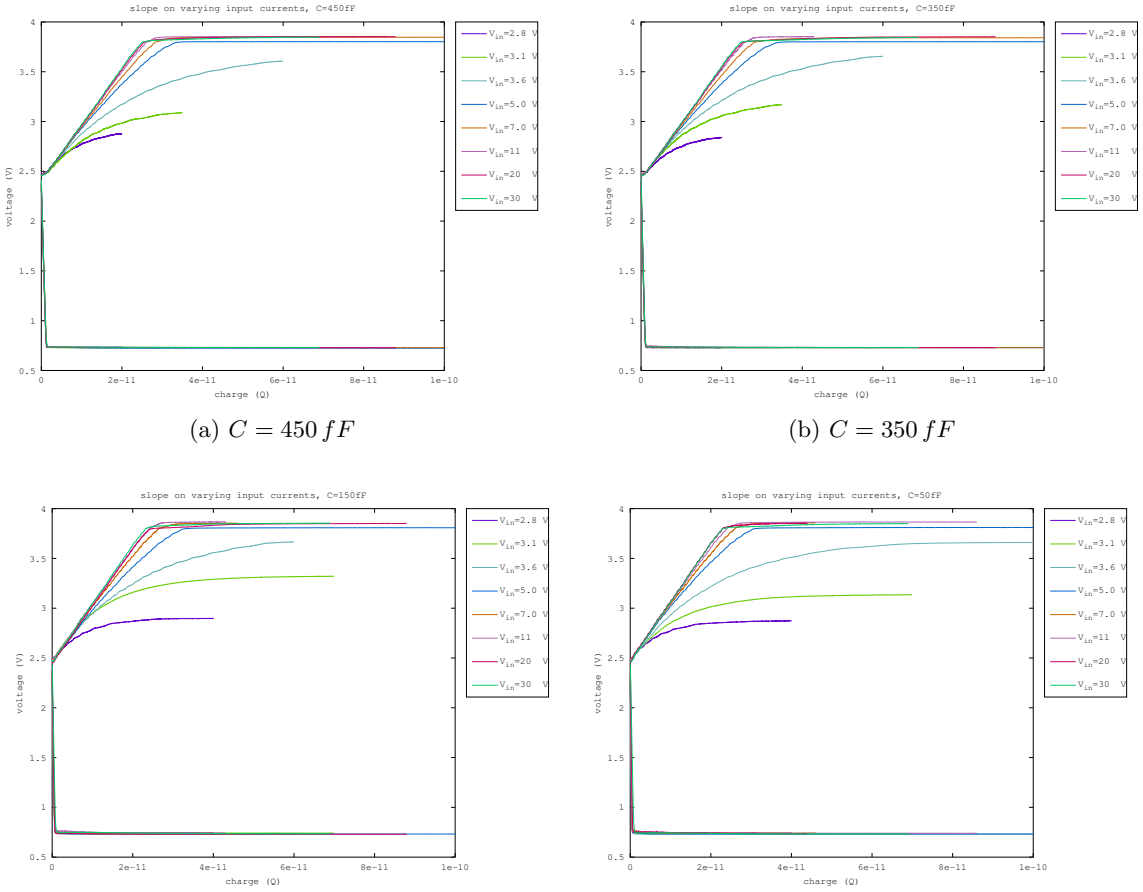
(b) $C = 350\,fF$

(c) $C = 150\,fF$

(d) $C = 50\,fF$

Figure 16: Expected versus measured charge up times for different input voltages. The input voltage is connected to the input through a resistor of $20\,M\Omega$

Figure 17 shows the plots of voltage against charge. One can observe that increasing the current causes the behavior to converge to a line with a linear slope that is constant with Q, and a saturation at $3.8\,V$.



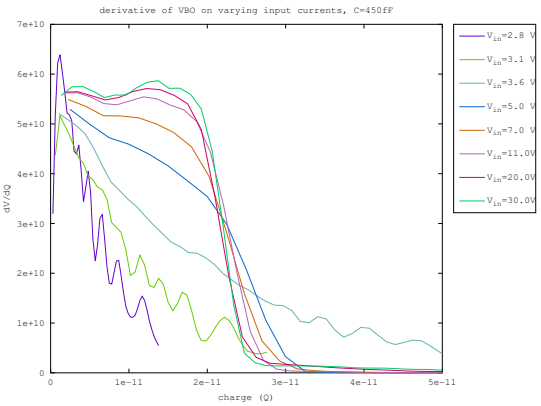
(a) $C = 450\,fF$ (b) $C = 350\,fF$

(c) $C = 150\,fF$ (d) $C = 50\,fF$

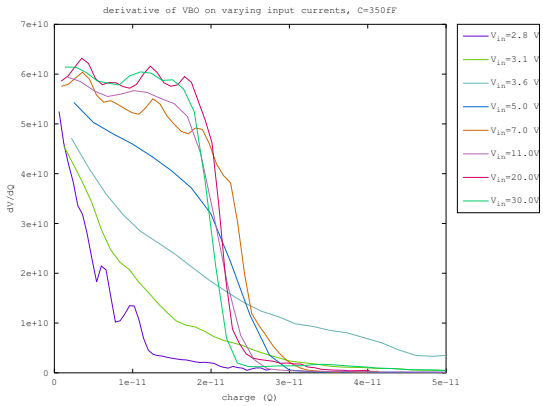
Figure 17: This plot is showing charge versus voltage

Figure 18 shows $\delta V/\delta Q$ for the VBO. The main observation one can make fromthese plots is that the behavior of VBO is almost entirely unaffected by the integration capacitance.

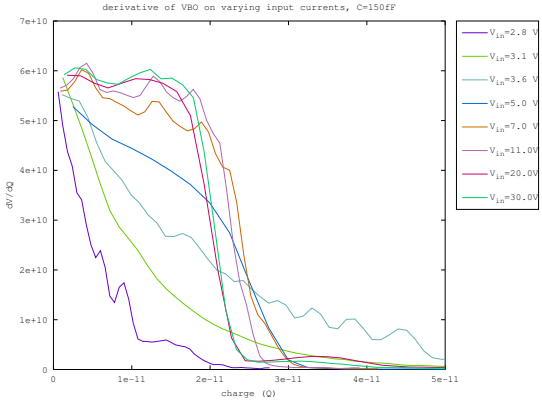
Figure 19 shows the $\delta V/\delta t$ against input voltage for VBO across all capacitances. For large voltages seem to behave in a normal linear fashion. The startup shows a scene that looks as if the $450\,fF$ and $350\,fF$ setup behave identical, and that the $150\,fF$ and $50\,fF$ setup behave identical. This might be due to the lack of measurement points, but is worth investigating further.



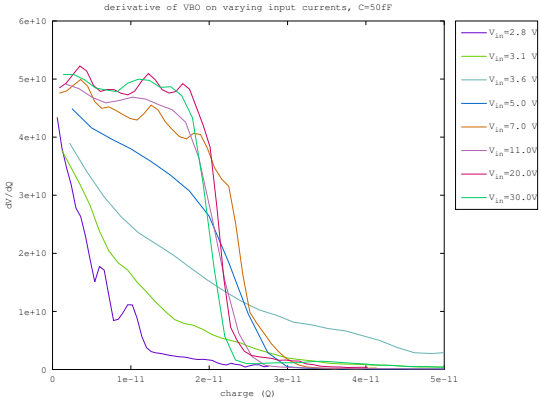
(a) $C = 450\,fF$



(b) $C = 350\,fF$



(c) $C = 150\,fF$



(d) $C = 50\,fF$

Figure 18: The plot shows dv/dt against time of the vbo.

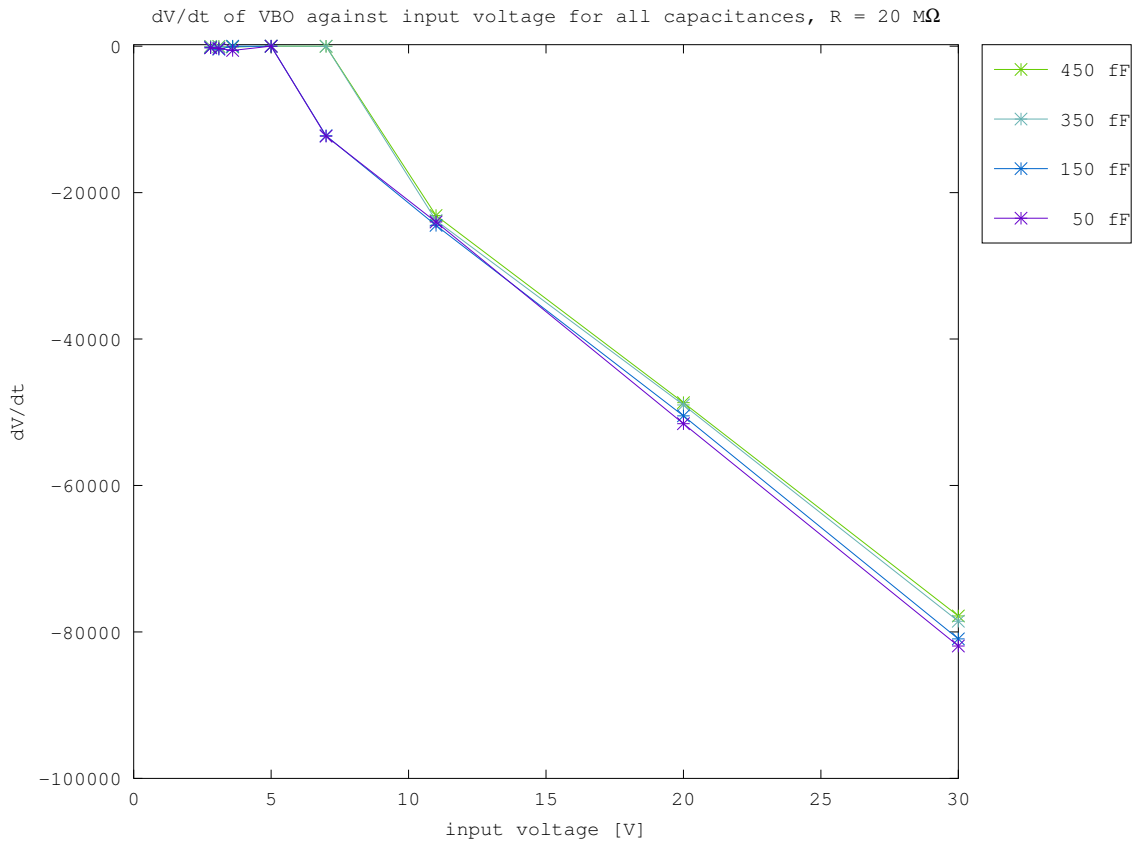


Figure 19: dV/dt of VBO against input voltage for all four capacitances. The x indicate the measurements.

5.4 Voltage limiter

In fig. 16 one can already observe the voltage limiter in action. The measurements in fig. 16 are taken with a $V_g = 4.5\,V$, but it is worth investigating the bevahior between V_g and the voltage limit posed by the voltage limiter. Figure 20 shows the measurement rsults of relationship between V_g and the voltage limit posed by the high voltage transistor at the input. The relationship appears the be linear between 3 and $3.8\,V$, but changes behavior at higher V_g. A possible explanation for this might be found in the reset transistor used to reset the integration capacitance. The body voltage of that pmos transistor is connected to the VDD of the circuit which is $3.3\,V$. Normally, this means that there is no current from source to the body, because the body is at the highest voltage, and the p-n junction between source and body will not conduct. This changes when the source voltage rises above the body voltage however, which can cause the p-n junction to draw current. This issue could explain the changed behavior of the voltage threshold at higher V_g. If this is the case, then a high V_g is very undesireable to operate the device, for it means that the device draws current even when saturated.

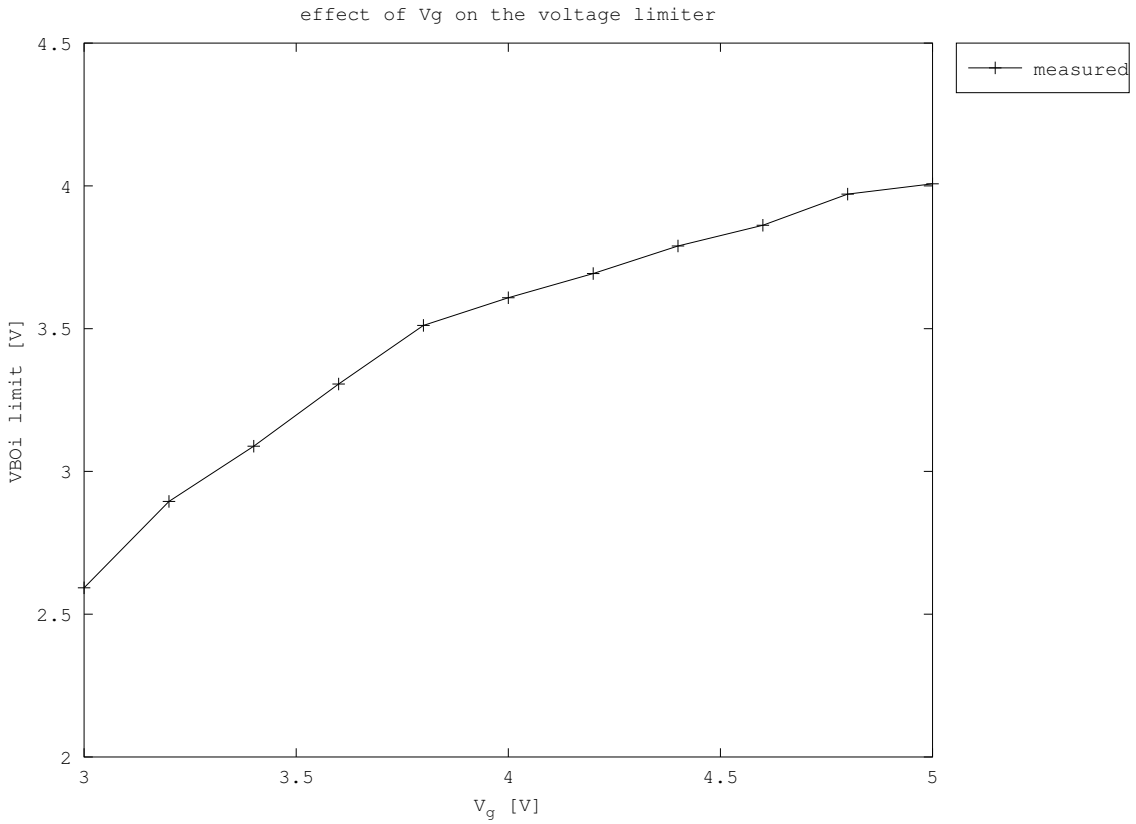


Figure 20: voltage limit as a function of Vg

6 GaN sensors with ROIC

After the ROIC is characterized with constant controlled current sources, the next step is to attach it to the GaN sensors. The target range of operating voltages for the GaN sensors is 0 to -100 V. The primary interest lies in the I/V characteristics of the system. Because the same cations need to be performed all the time, it is worth to automate the setup one step further to save time.

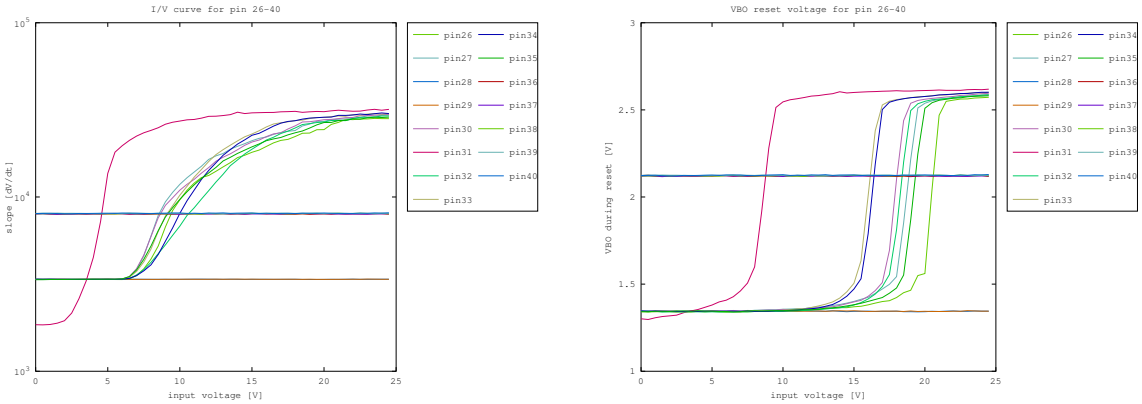
6.1 Setup

In order to automate the measuring process further, the oscilloscope is connected to the laptop by cable, and directly controlled by `labVIEW`. `LabVIEW` automatically acquires the required waveforms from the oscilloscope, and calculates the slope in real time. This action is repeated and used to accumulate data points for the I/V curve. When the program is finished, the processed data is stored. A bashscript collects all the data and calls `octave-cli` to put the results in a plot. There are two ways, that have been used to controll the bias voltage of the GaN sensors. The first method is to use the arbitrary function generator (AFG) on the oscilloscope to generate a DC voltage between -2.5 and $2.5\,V$. A voltage amplifier with a gain of 10 is then used to achieve a range of -25 to $25\,V$ that is directly controllable in `labVIEW`. This allows `labVIEW` to automatically sweep the bias voltage. However, the range of -25 to $25\,V$ does not cover the target bias voltage range. Therefore, in order to increase the range further, a second method is used. This time the bias voltage is controlled manually with a voltage source. The oscilloscope measures both the input and output voltage. `LabVIEW` then calculates x and y coördinates repeatedly. This method provides the operator with full control over which part of the I/V curve is measured.

6.2 Automatic bias voltage sweep

Measurements in this section are acquired using the automatic bias voltage sweep. First the performance in forward bias is investigated. The result of these measurements are shown in fig. 21. The VBO channel is used for the measurements because of the large currents. There are several oberservations that be made using this plot. First of all, there are several pins that appear to be unaffected by the input voltage. This is not due to the GaN sensors, but because the ROIC channel broke after a certain point. This is most likely because the input was accidently connected to a ground pin, which puts the high voltage directly to the input of the ROIC. A second observation is that the reset value of the VBO cannot be contained for large input voltages. This most likely means that the amount of current that is put into the ROIC is larger than the op amp in the ROIC can keep up with. Using an external current meter, the maximum amount of current the opamp can compete with is approximately $15\,\mu A$. Finally it is interesting to observe that there is a substantial variance across the different devices. In order to test whether this variance is due to noise or due to variance across devices, a second set of measurements are made. This time only a single device is measured. The results are shown in fig. 22. These measurements show that the variance over different measurements is relatively low, which means that the observed variance in fig. 21 is mostly caused by variance across different devices.

Next, the reverse bias performance. The I/V characteristics for several pins are shown in fig. 23. The jumps to negative current between 0 and $2.4\,V$ is due to the ground of the ROIC input being $2.4\,V$. Therefore for lower voltages, the current flows into the opposite direction. The numbers are not representative for the actual current though, because the ROIC and measurement method are not designed for that direction of current. The main observation that can be made is that the



(a) I/V characteristics

(b) reset value for VBO

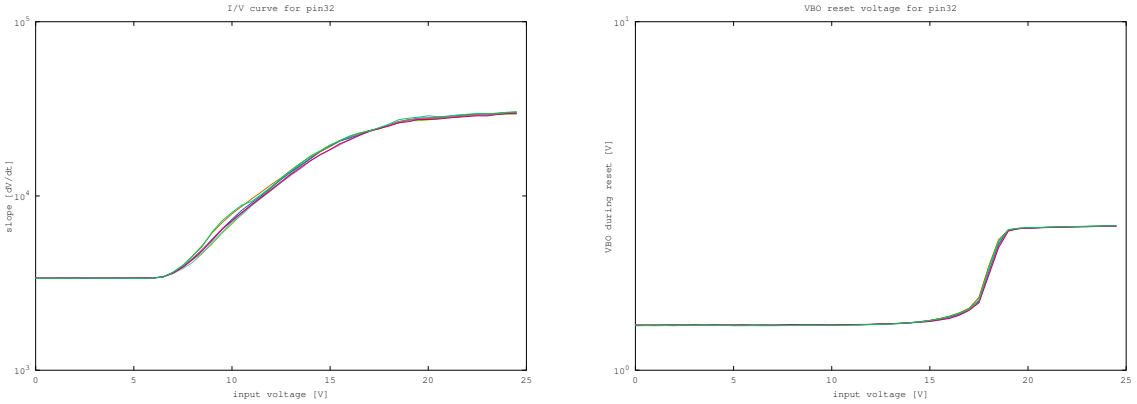
Figure 21: The slope and reset values for the VBO of pin26-40

voltage range available in the current setup is insufficient to observe the most interesting part of the I/V characteristics.

6.3 Manually controlled bias voltage

To get to higher bias voltages, the bias voltages are manually controlled. This section will analyse measurement results based on individual sensors to determine both the GaN sensor and ROIc performance.

The I/V characteristics for pin 21 on the chip are shown in fig. 25. Note that the pin number indicates the GaN sensor on a chip that is connected. The results in this plot match with the expected behavior of GaN sensors based on previous measurements. There is a small expontial increase in current for low bias voltages. At a high bias voltage the device goes into breakdown with a steep exponential increase.



(a) I/V characteristics

(b) reset value for VBO

Figure 22: The slope and reset values for the VBO of pin32 repeated multiple times to test variance across measurements

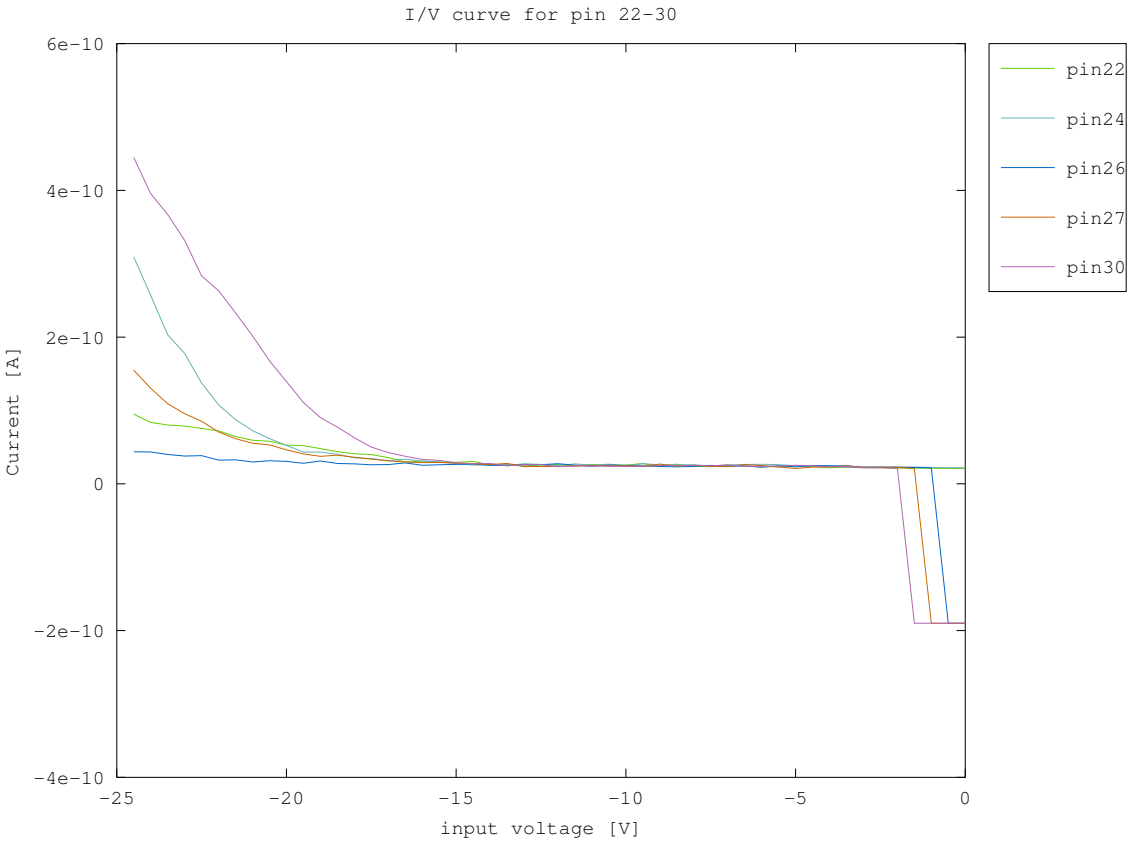


Figure 23: Voltage to current characteristics for several GaN sensors

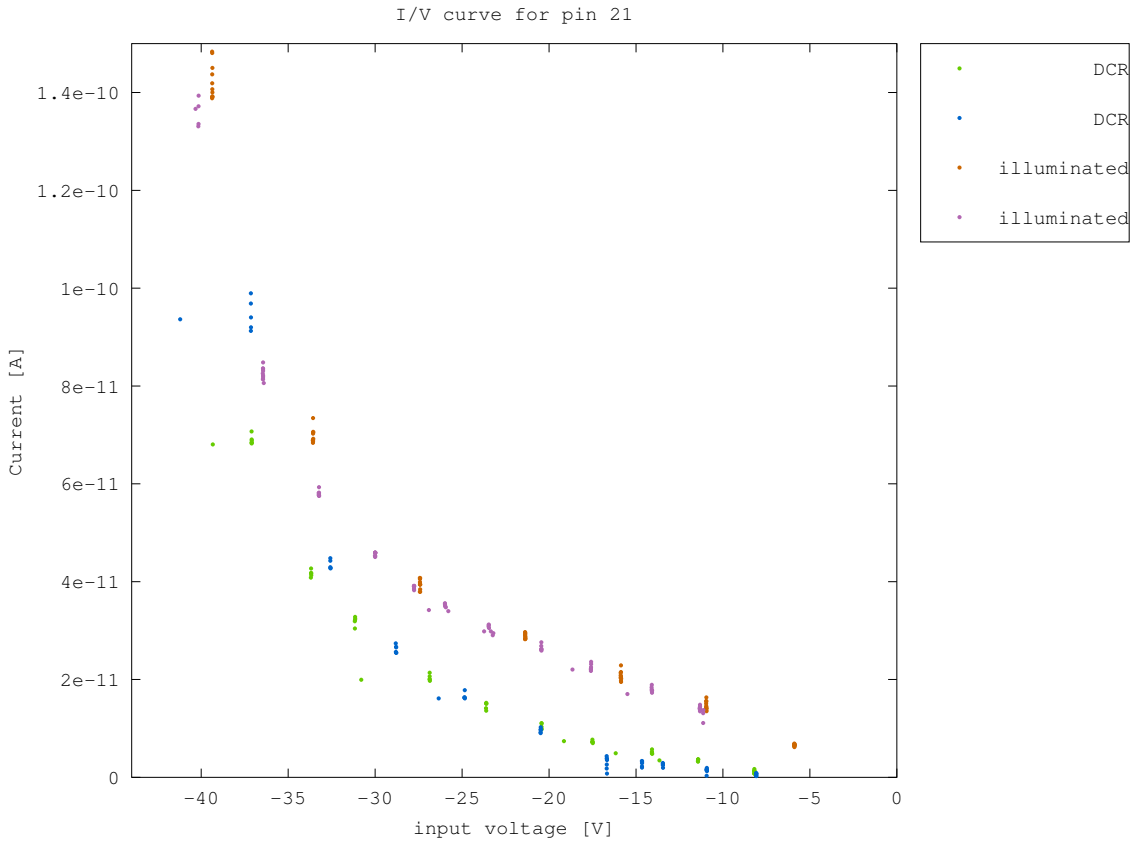


Figure 24: Voltage to current characteristics for a single GaN sensor

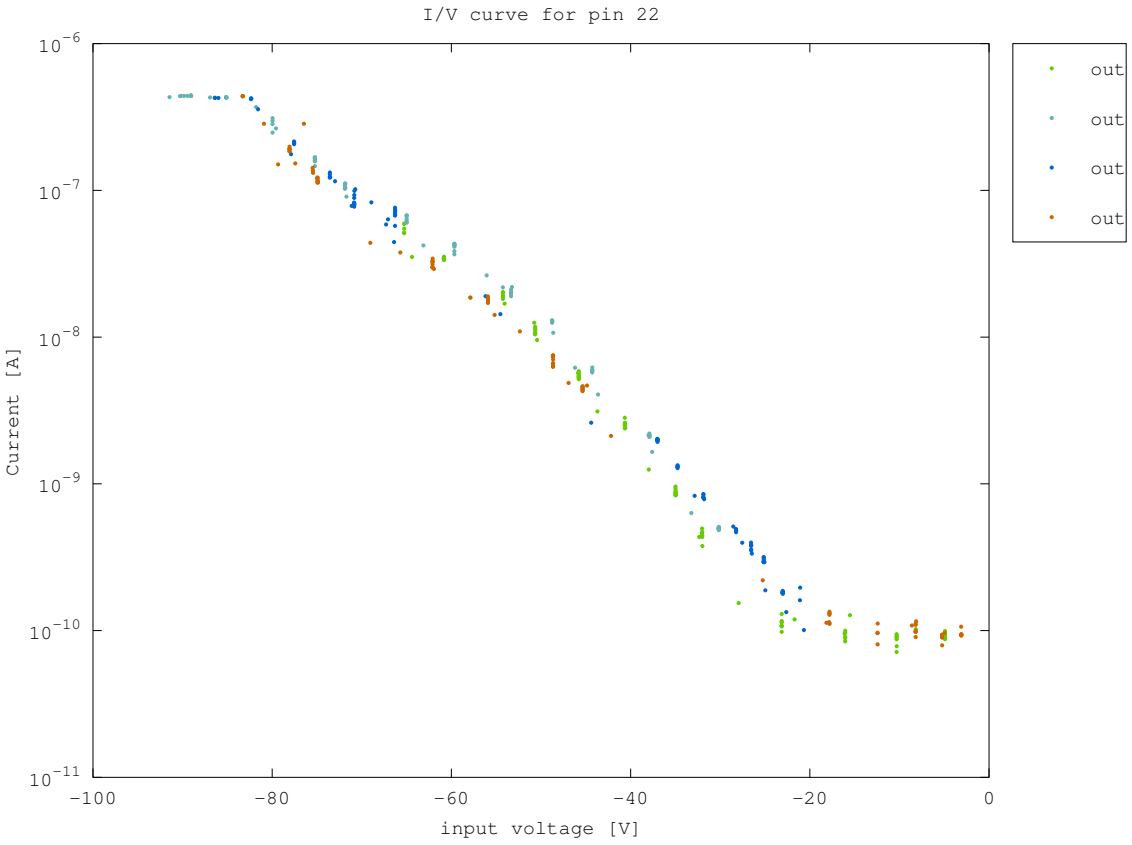


Figure 25: Voltage to current characteristics for a single GaN sensor

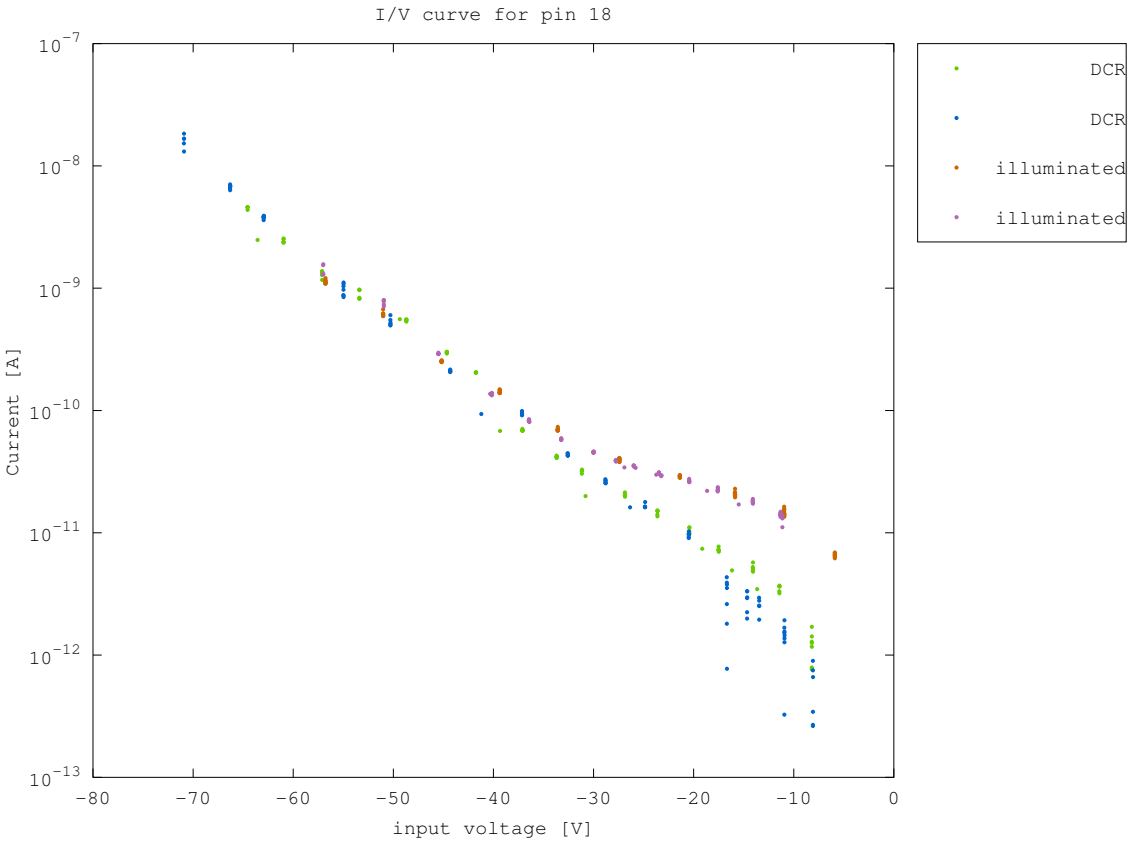


Figure 26: Voltage to current characteristics for a single GaN sensor

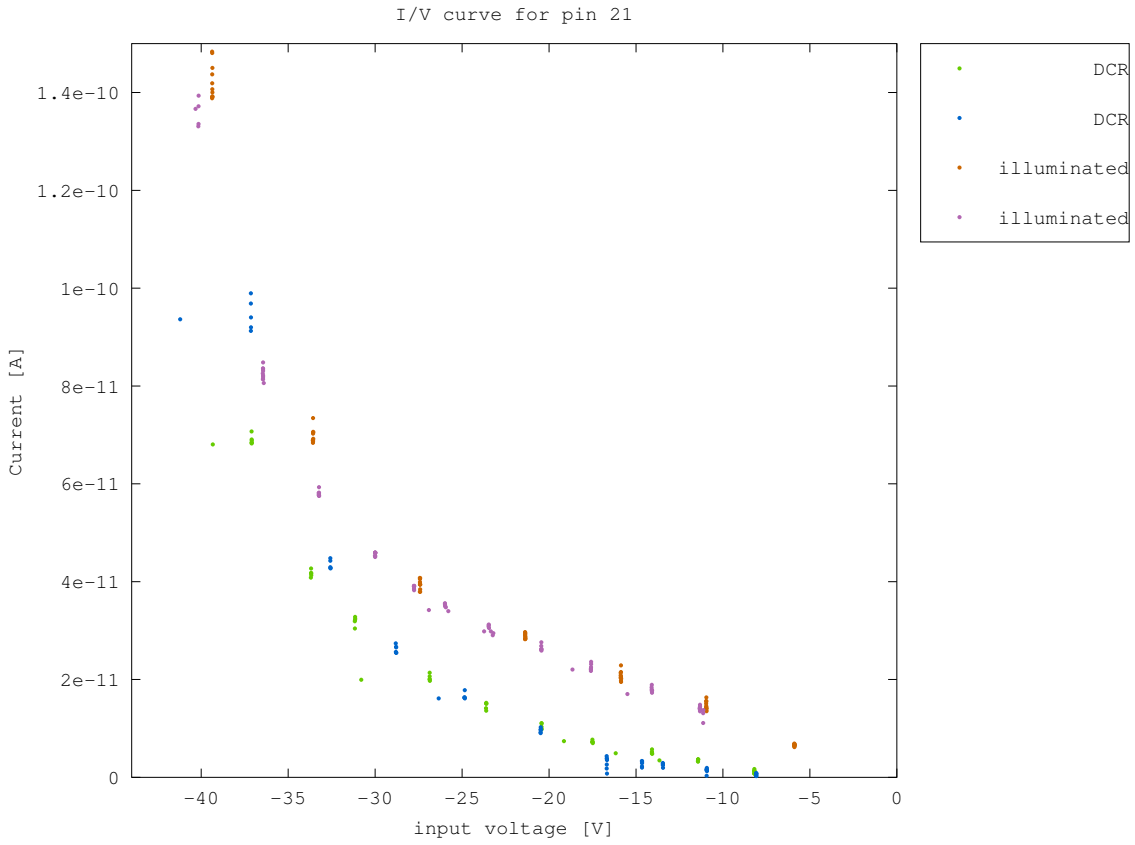


Figure 27: Voltage to current characteristics for a single GaN sensor

6.4 Very high bias voltage

7 Conclusions and Future work