

Preethi's ROIC analysis

Kees Kroep 4246373

August 26, 2016

1 setup

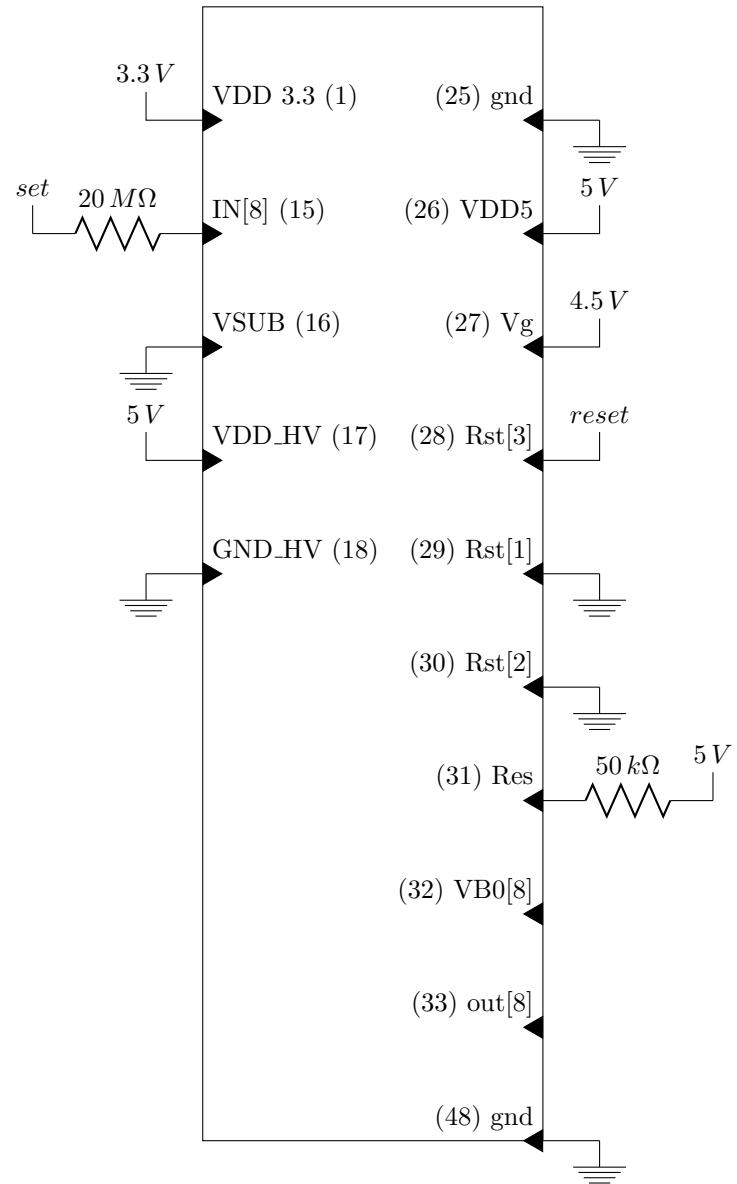


Figure 1: Schematic of breadboard

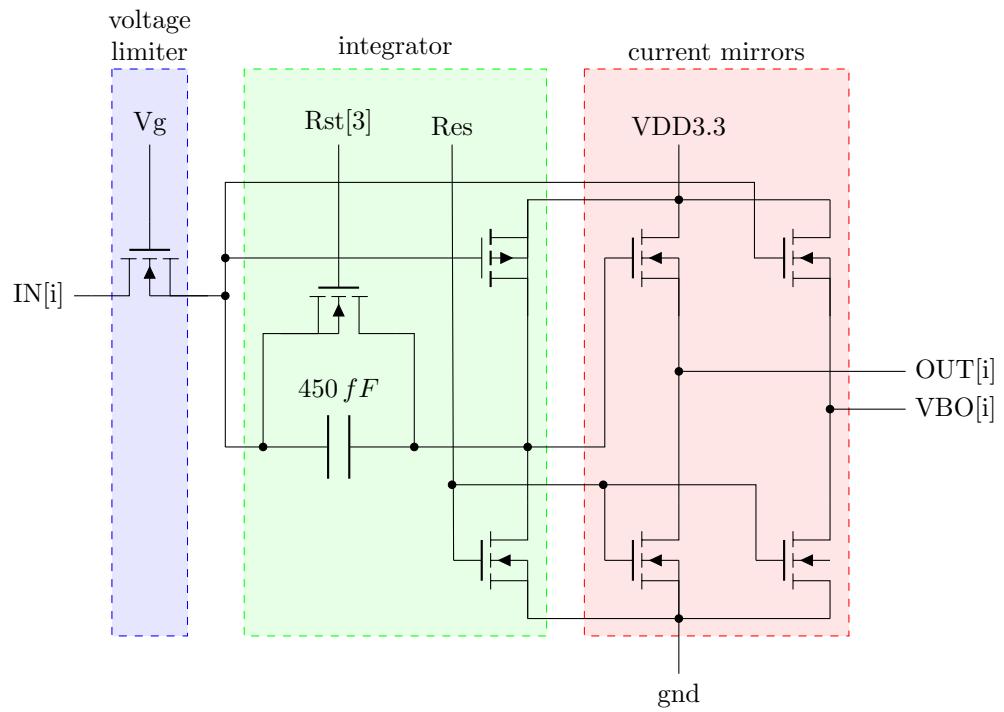


Figure 2: Schematic of ROIC channel

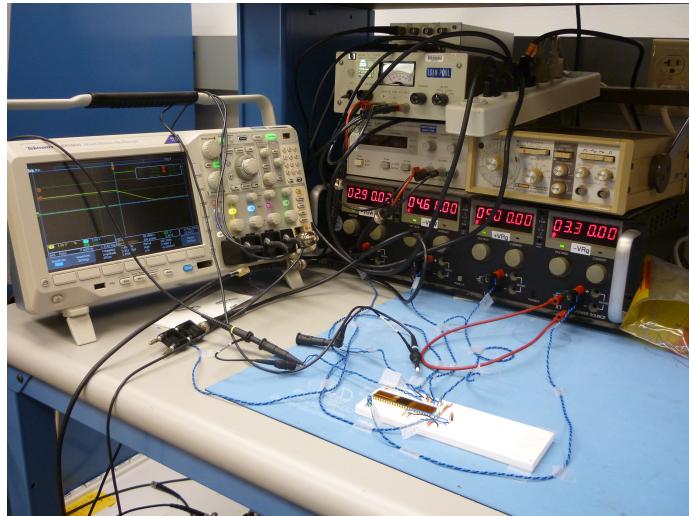


Figure 3: setup overview

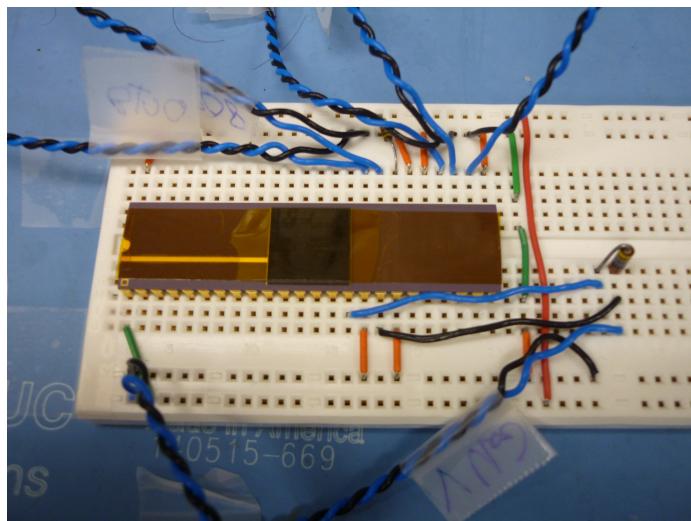


Figure 4: close-up

2 Characterization for high impedance voltage source

This section aims to characterize the behavior of the ROIC while exposed to a voltage source with a high resistance in the order of several $M\Omega$. A focus is put onto the performance in reset state, the relationship between input current and output voltage, and the current limiting properties of the input transistor.

2.1 Reset

This measurement addresses the behavior of the circuit in reset mode. Figure 5 shows the measured values during reset mode. Note that the input voltage is 2.4 V, which is important when calculating the input current.

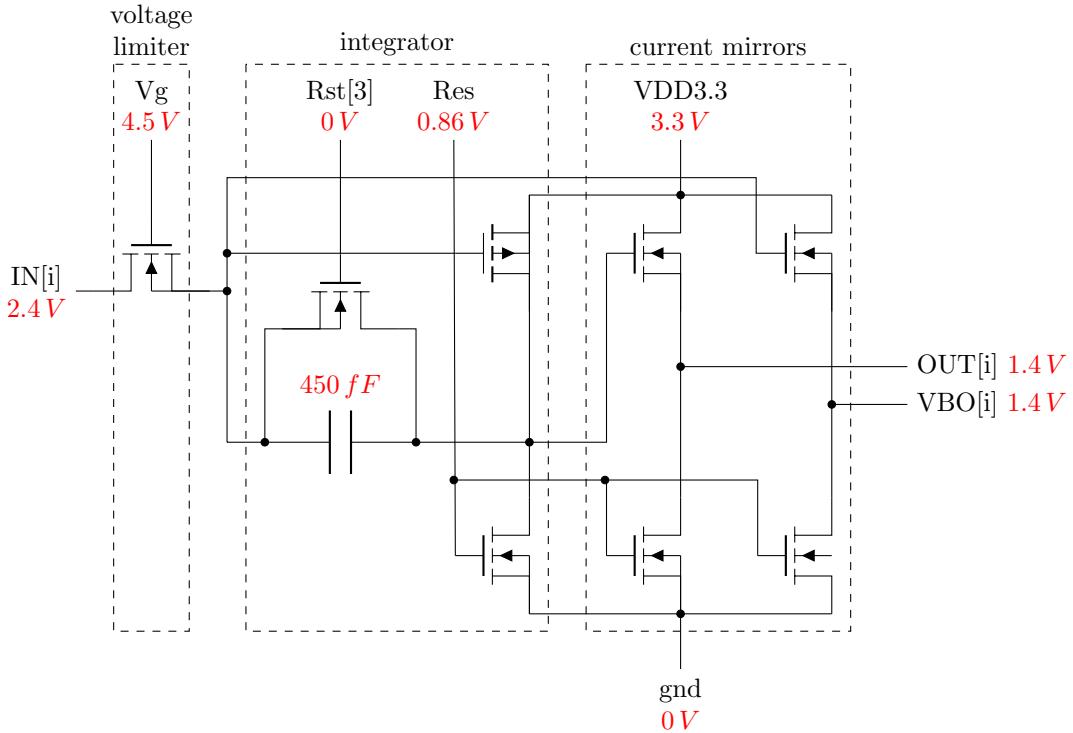


Figure 5: Schematic of ROIC channel template

2.2 Standard performance

This test aims to address the basic relationship between input current and output voltage. Figure 6 shows the setup used for this test. Channel 8 was used, so the end of the $20 M\Omega$ resistor is connected to IN[8], and probes are connected to OUT[8] and VBO[8].

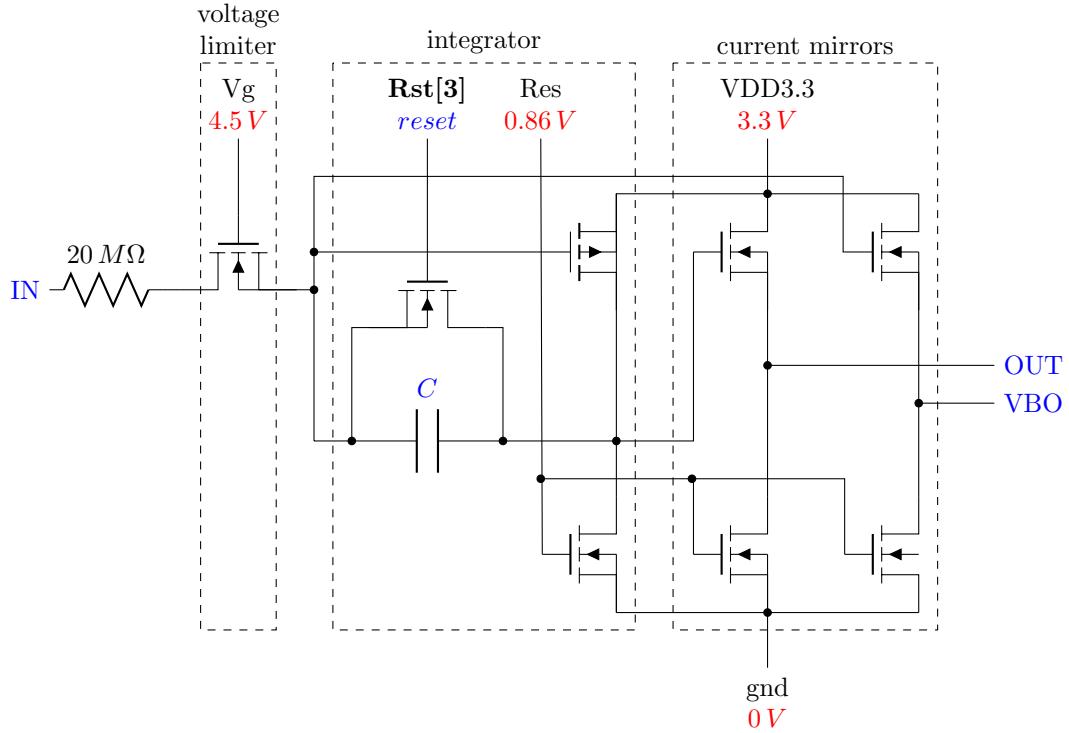


Figure 6: Schematic of ROIC channel template

Figure 7 shows the time versus voltage plot of both the VBO and OUT for a constant input voltage. The rising and falling slopes are the VBO and OUT respectively. The timescale of this plot does not allow for much inside in VBO, but it does show some interesting results for the behavior of OUT. When the reset switches, the input node immediately loses some charge. Note that the oscilloscope matches the rising edge of the rset signal to time is 0 s, so this drop is at 0 s. It is interesting to observe that the slope is constant for all input voltages. The slopes is much slower than the time necessary for the reset transistor to switch, so the observed slope is not limited by the reset transistor, but by the source follower that tries to keep up. This observed slope is therefore the maximum rate at which the output node can be pulled down in the current set-up. Iso note that the slope gets steeper when the integrator capacitance decreases. This is to be expected. However also note that the maximum slopes across the different capacitances are all identical.

Figure 8 shows a

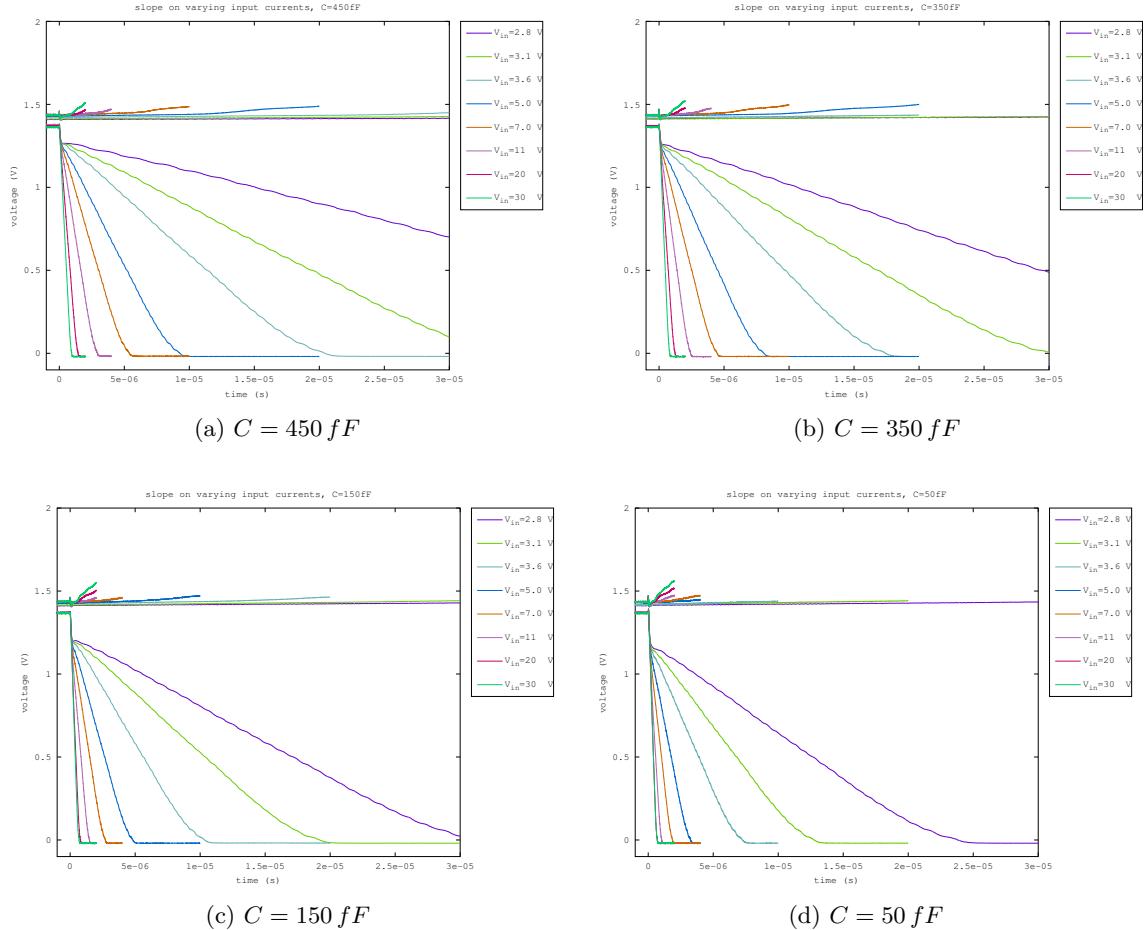


Figure 7: Expected versus measured charge up times for different input voltages. The input voltage is connected to the input through a resistor of $20 \text{ M}\Omega$

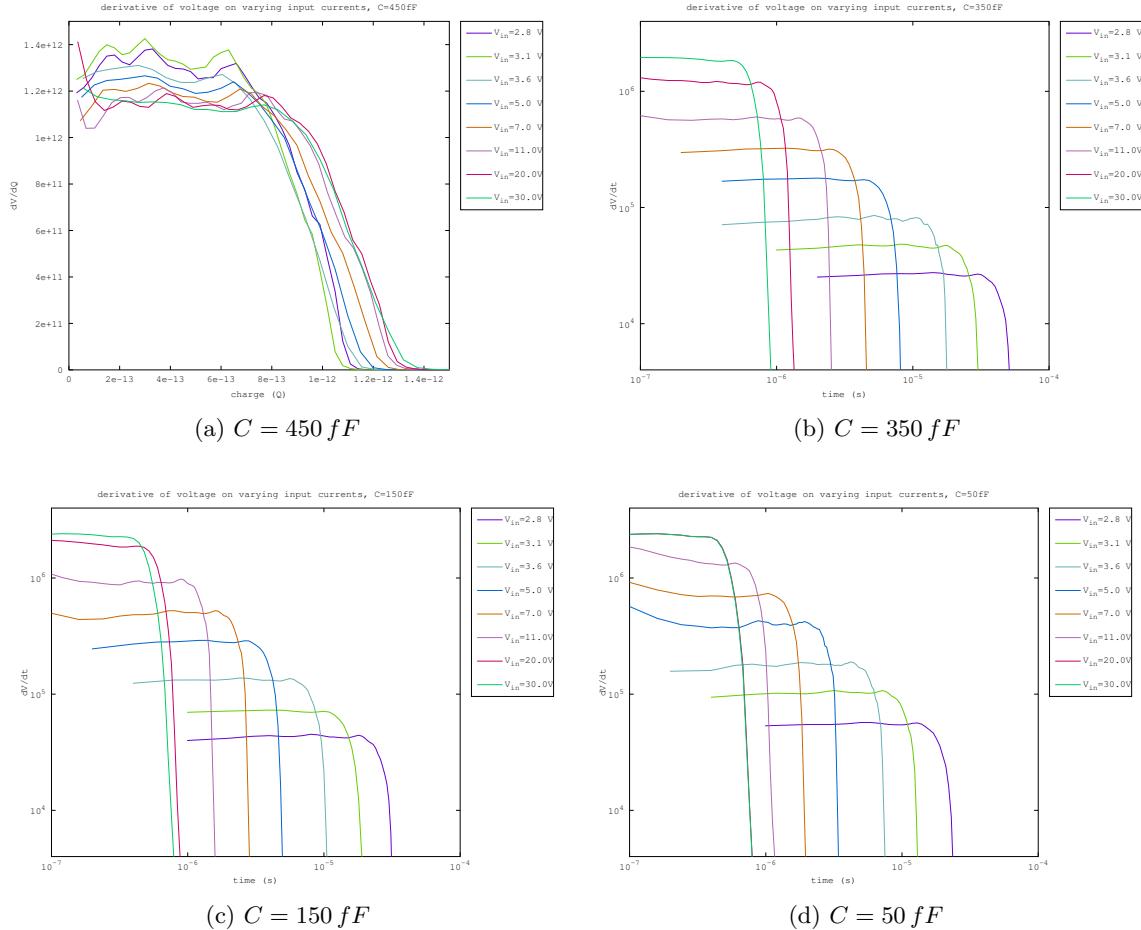


Figure 8: The plot shows $\frac{dv}{dt}$ against time. The plot is in log scale, which allows for an easy read on the maximum slope and the time needed to discharge the integrator capacitance.

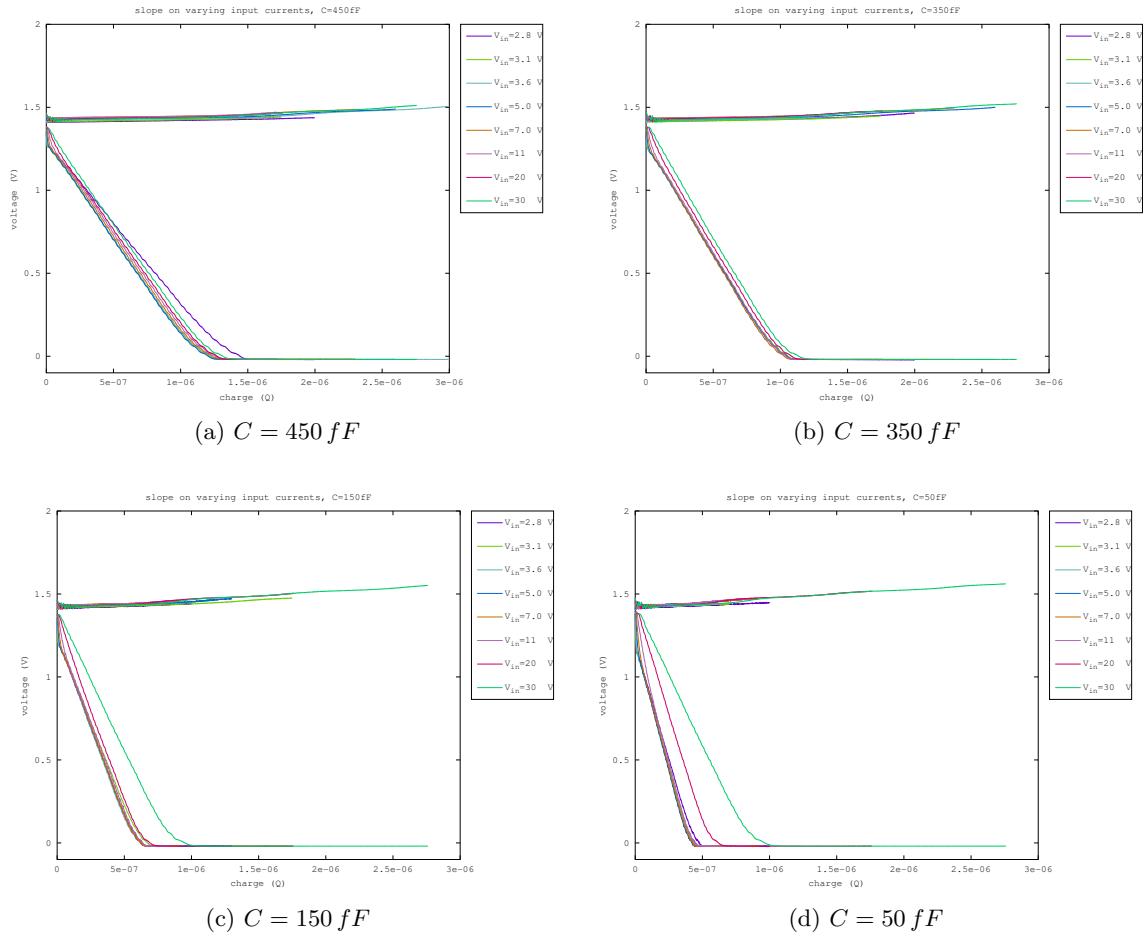


Figure 9: This plot is showing charge versus voltage

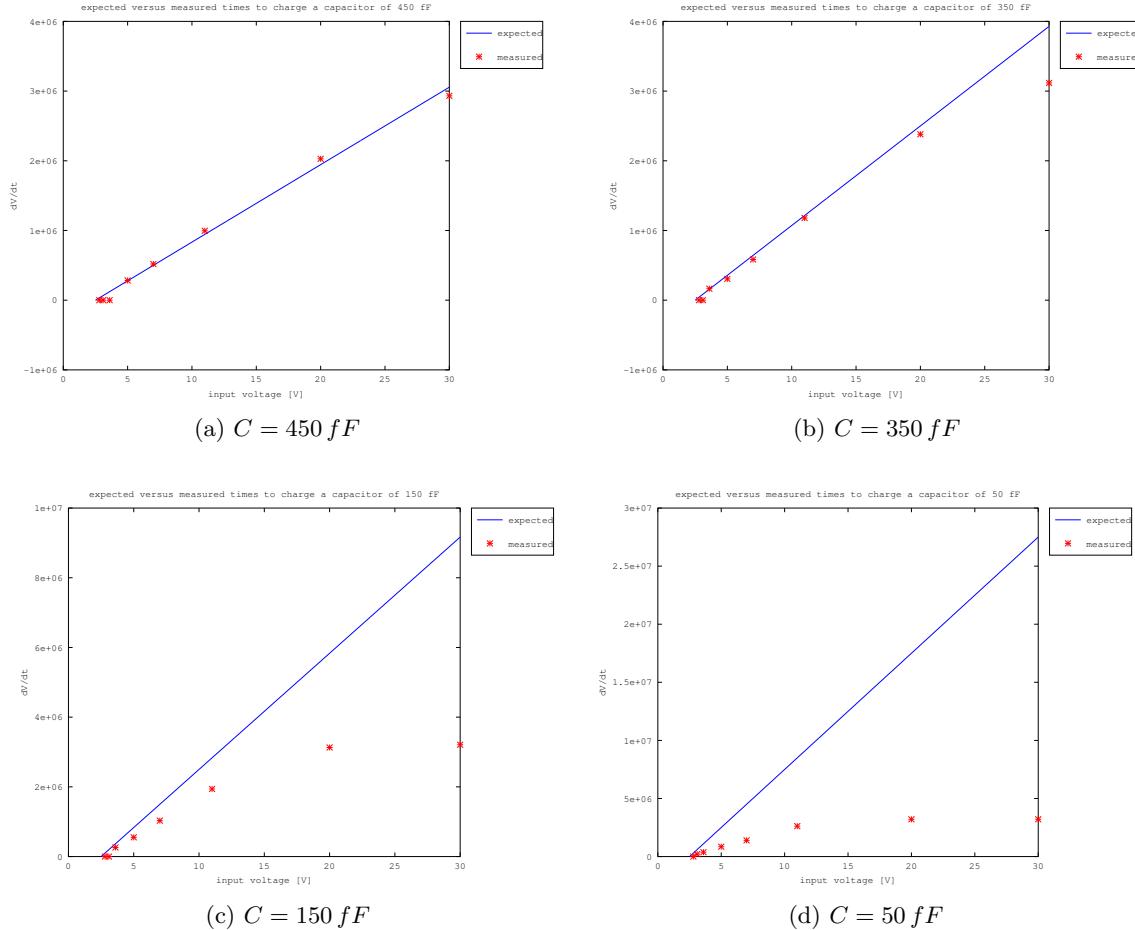


Figure 10: Expected versus measured charge up times for different input voltages. The input voltage is connected to the input through a resistor of $20 \text{ M}\Omega$.

2.3 large current focussed

In this section the $20 M\Omega$ input resistor is replaced with a $4 M\Omega$ resistor.

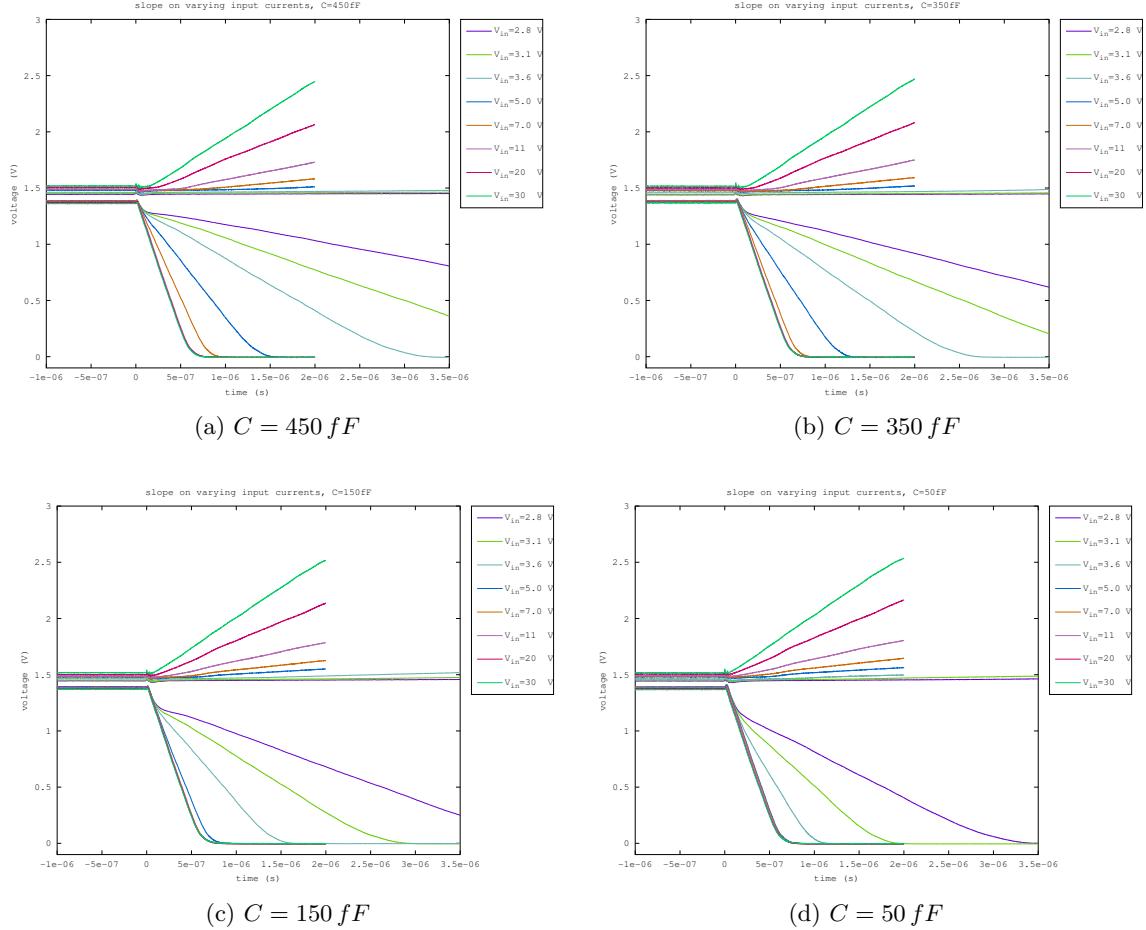


Figure 11: Expected versus measured charge up times for different input voltages. The input voltage is connected to the input through a resistor of $4 M\Omega$

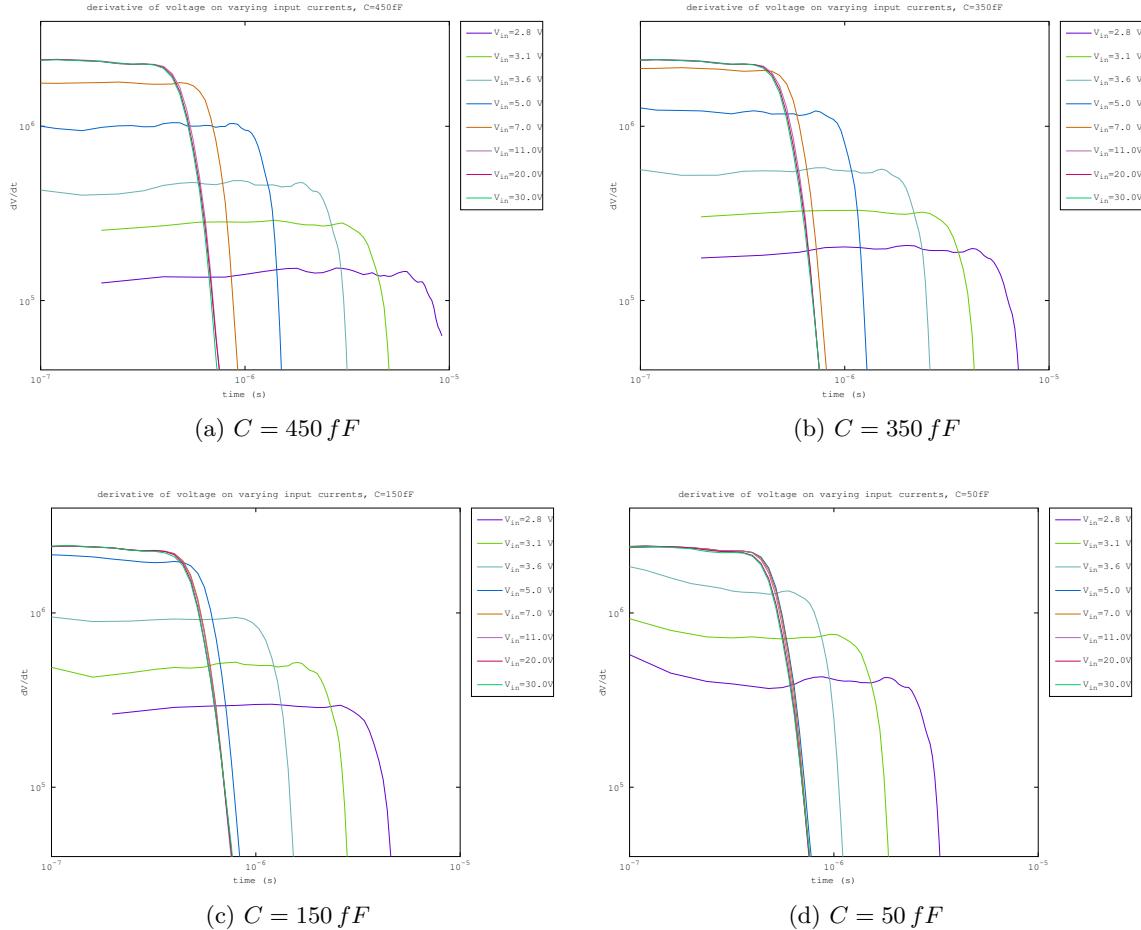


Figure 12: The plot shows dv/dt against time. The plot is in log scale, which allows for an easy read on the maximum slope and the time needed to discharge the integrator capacitance.

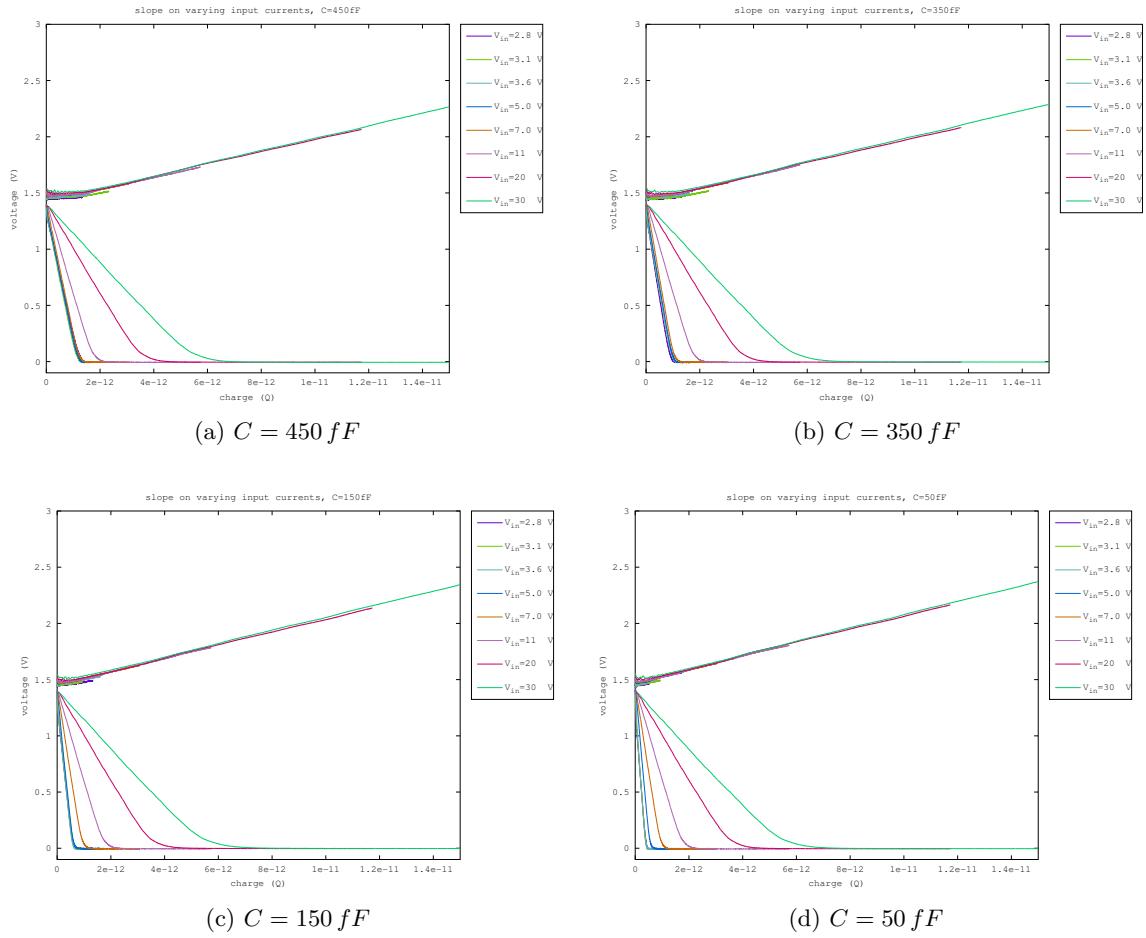


Figure 13: This plot is showing charge versus voltage

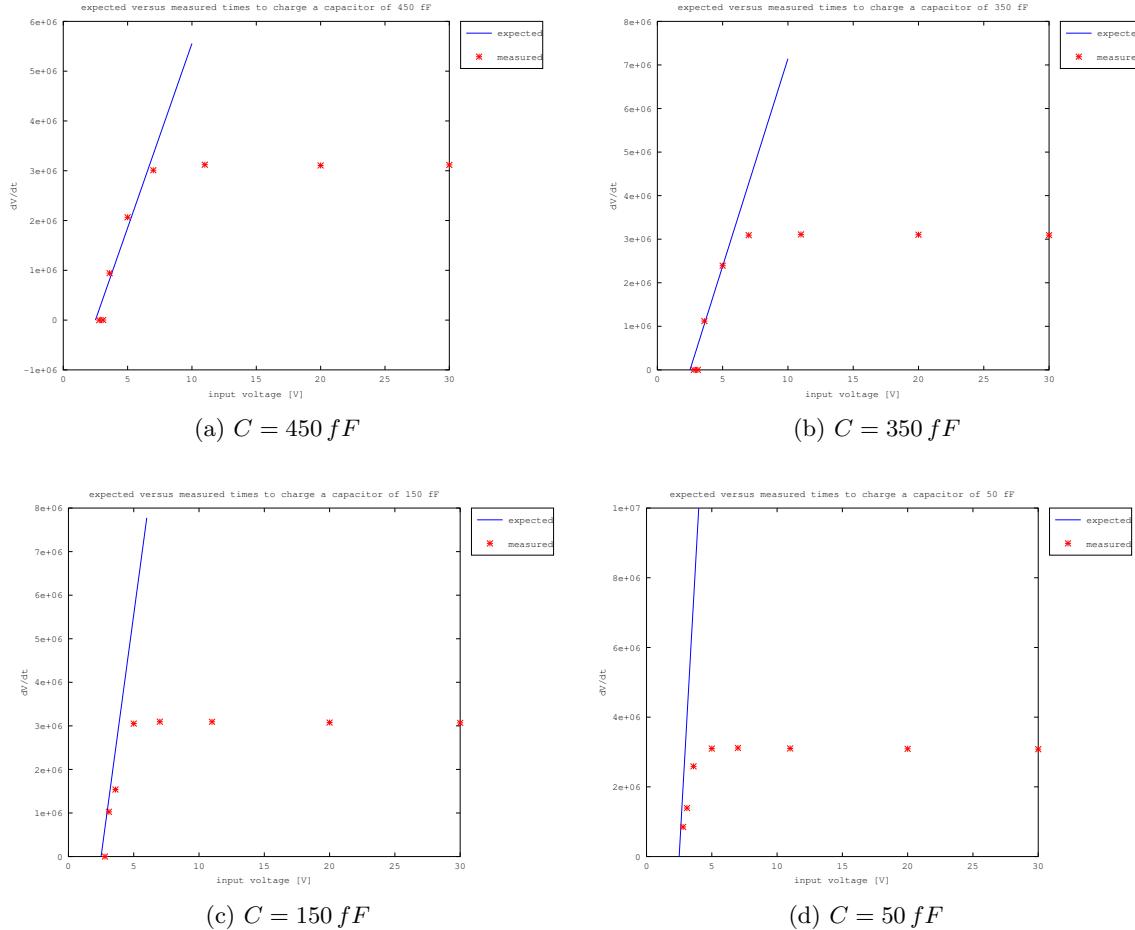


Figure 14: Expected versus measured charge up times for different input voltages. The input voltage is connected to the input through a resistor of $4 \text{ M}\Omega$.

2.4 vbo focussed

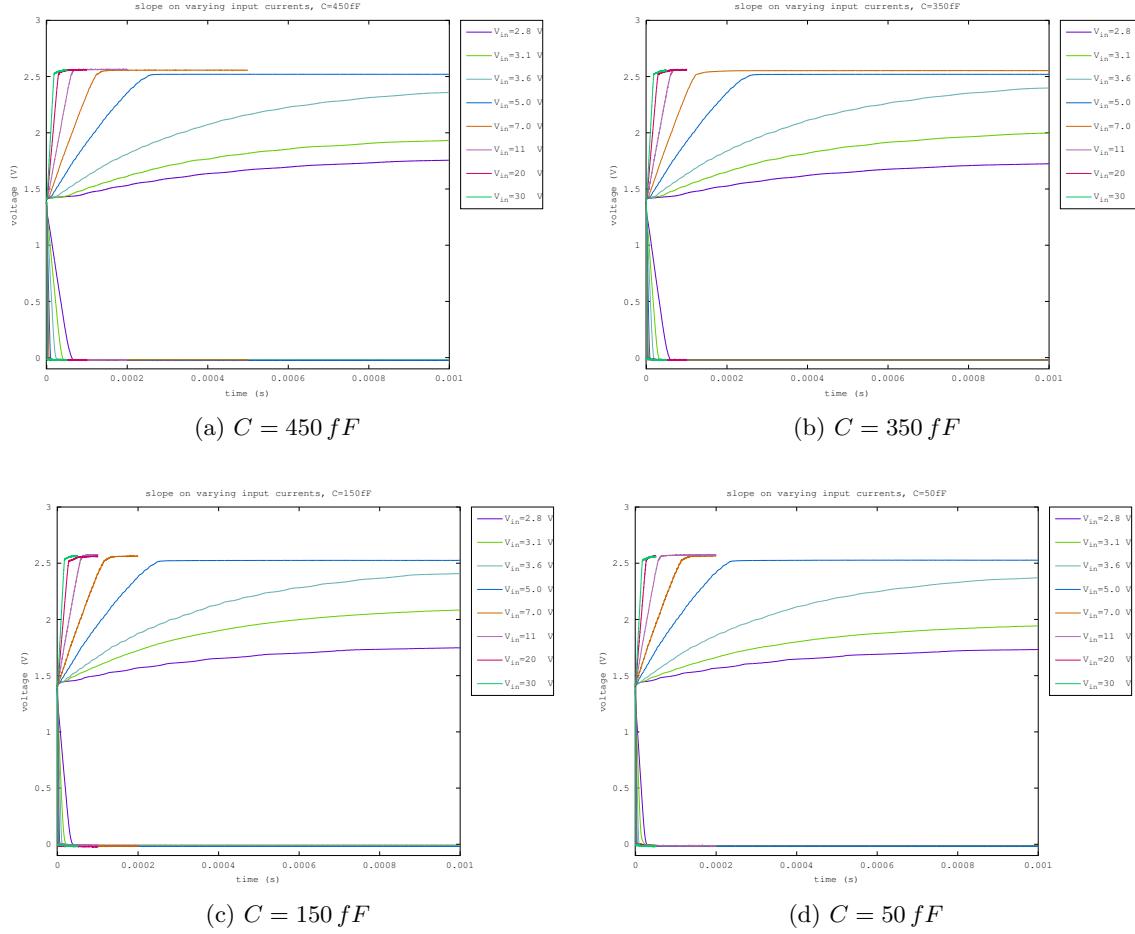


Figure 15: Expected versus measured charge up times for different input voltages. The input voltage is connected to the input through a resistor of $20 \text{ M}\Omega$

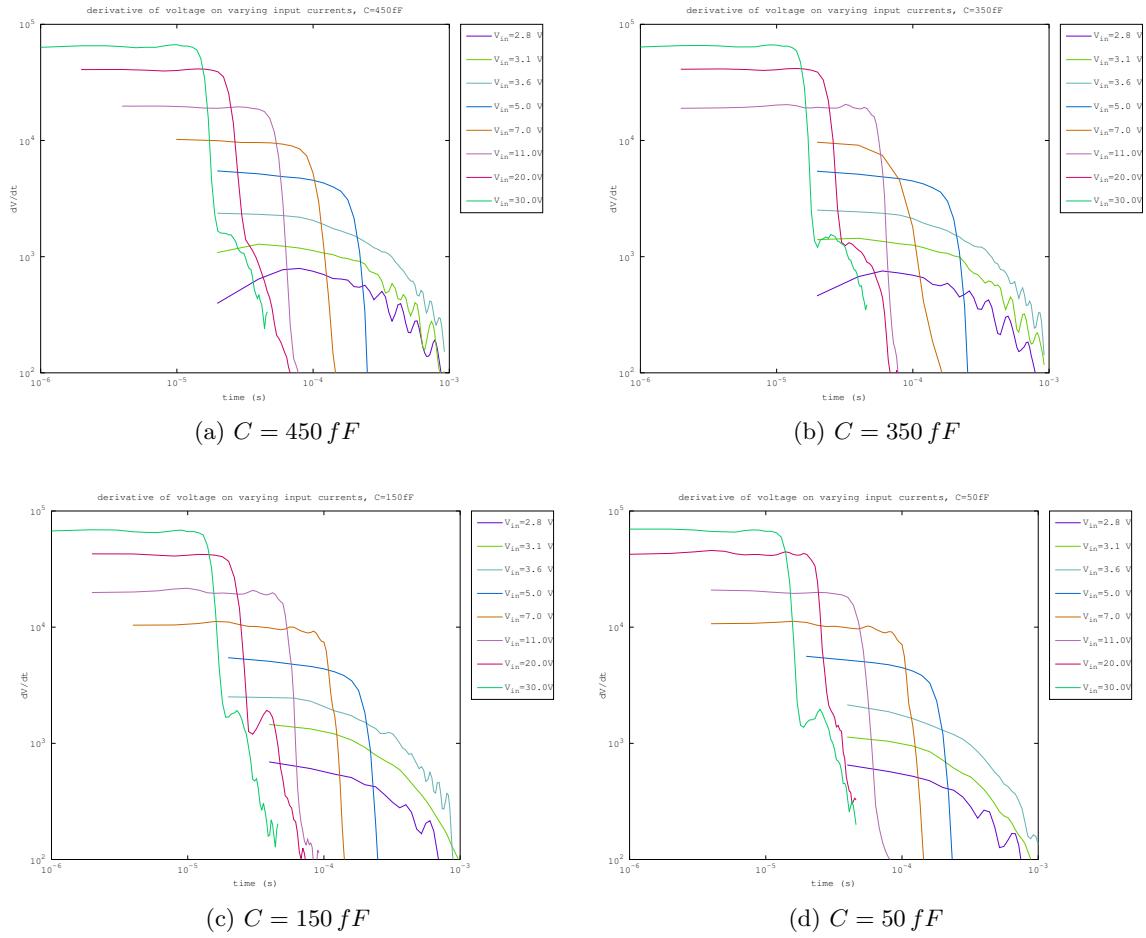


Figure 16: The plot shows dv/dt against time of the vbo.

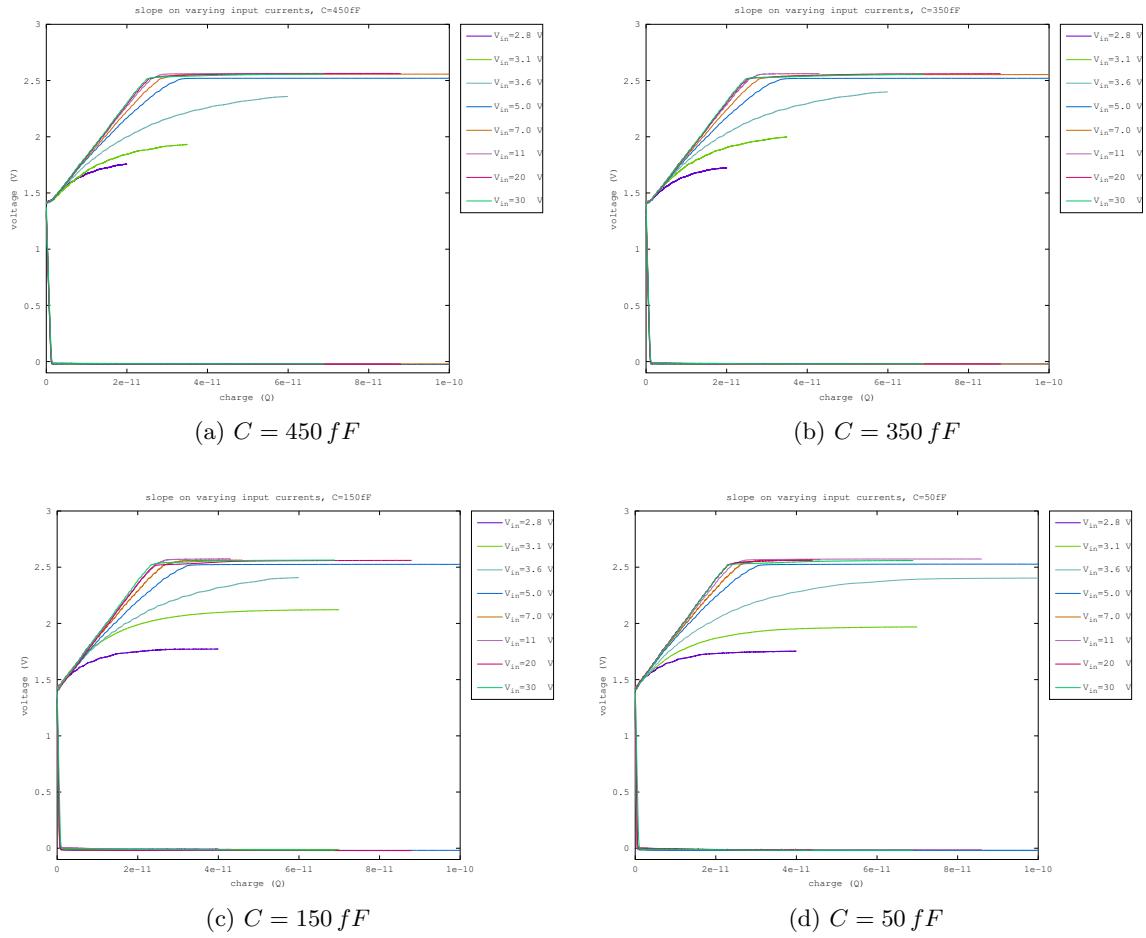


Figure 17: This plot is showing charge versus voltage

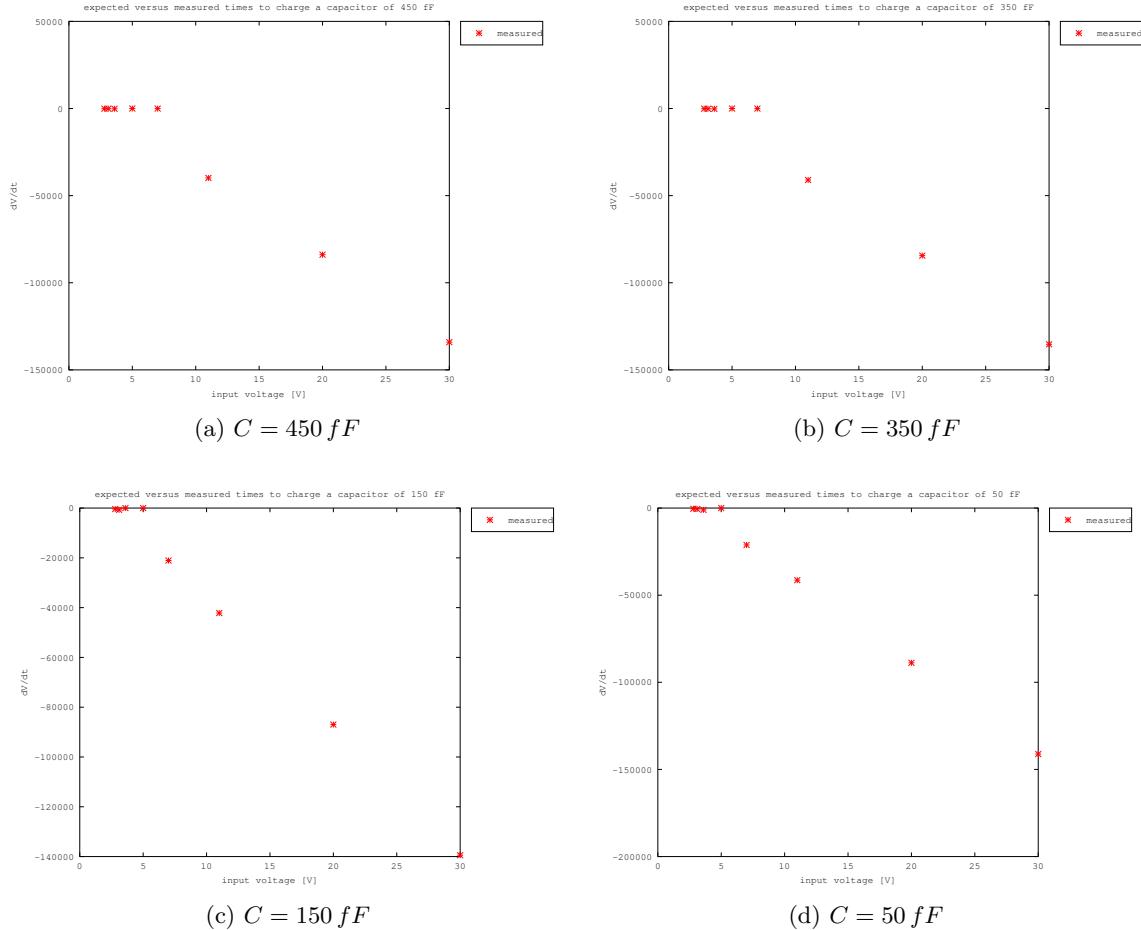


Figure 18: charge times of vbo for different input voltages. The input voltage is connected to the input through a resistor of $20 \text{ M}\Omega$.

