Project Midterm Report

EECS 495: Advanced Low Power Digital and Mixed Signal Circuit Design

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Objective: To design an efficient Integrated Switched Capacitor DC-DC Voltage Regulator.

Procedure:

Around 1.2V DC supply to SCVR (Switched Capacitor Voltage Regulator), so this input voltage line will work as a rail and there should be less number of rails going to the SCVR to get significant energy benefits.

Conventional inductor based switched converters suffer from scalability limitations in size and power. So recently switched capacitor DC-DC converters have emerged with increased current carrying capability. High-density metal-insulator-metal (MIM) capacitors are used.

Different configurations like 1:1, 2:1, 3:2, 5:4 (the numbers in ratio as integers are used as integers) and so on are used and find the highest efficiencies amongst the configurations.

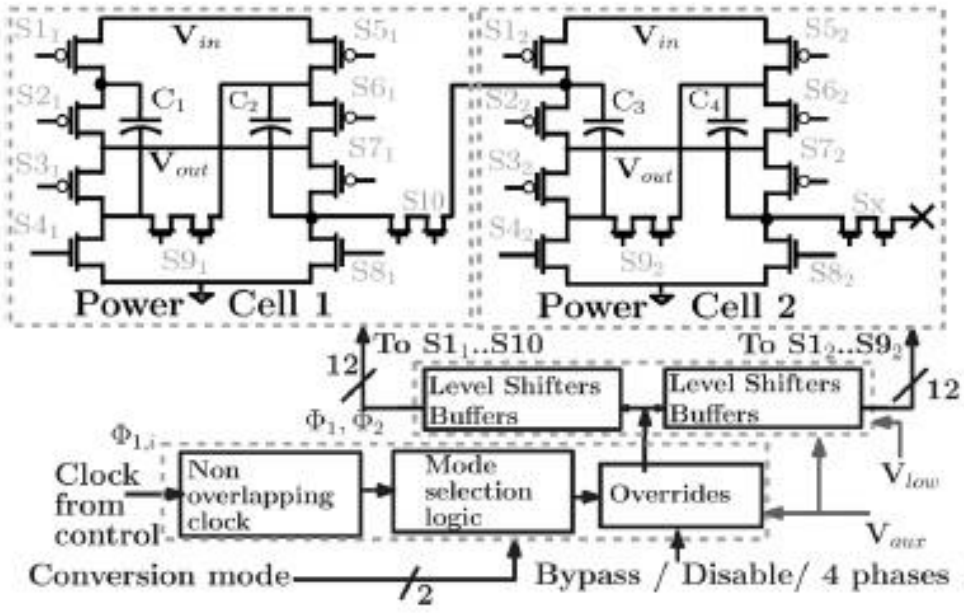

Fig. 3. Power stage module.

There are various functions of this block through which efficient conversion can take place. The schematic for level shifter can be used as shown in circuit below.

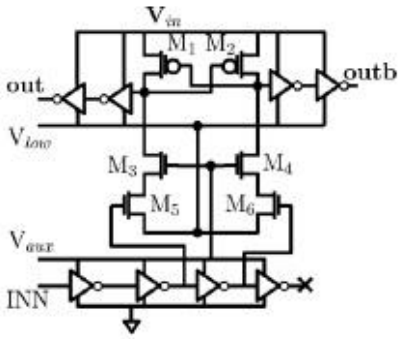

Fig. 6. Schematic of the level shifter.

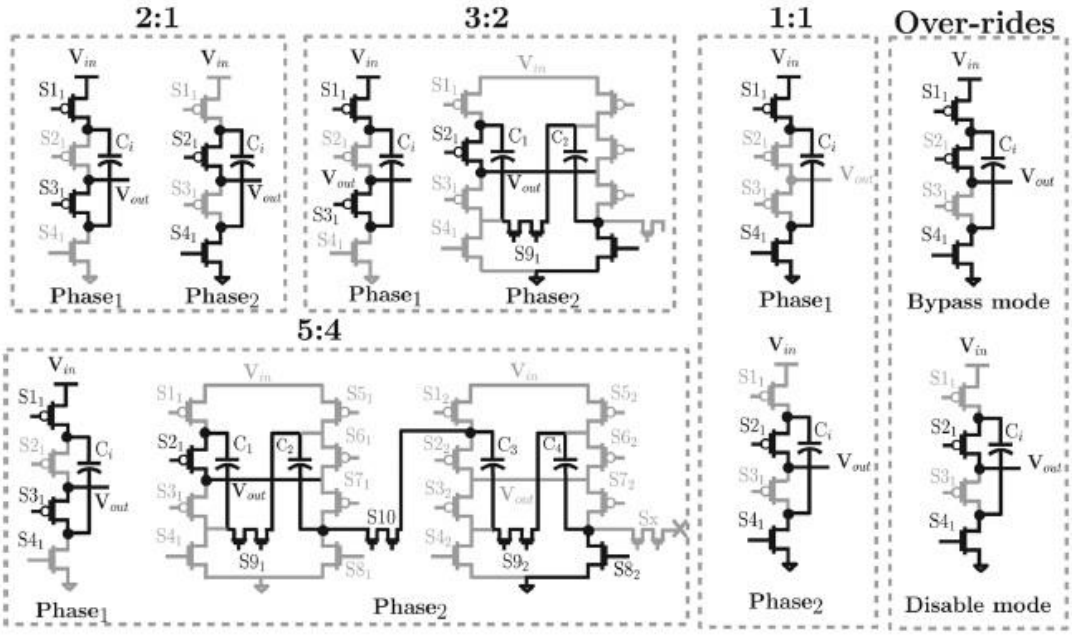

Fig. 5. Multiple transformation ratios.

The intrinsic Equivalent Series Resistance (ESR) combined with interconnected resistances to and from MIM are dominant and has significant impact on capacitance, ESR and frequency response of the capacitor. The width of capacitor was determined by routing template adopted for top metal. Fly capacitor terminals are routed to the transistors through the localized grids. The current flow and heating is assumed for the worst case.

Goal:

To test of configurations for many SCVR topologies and find the most efficient one. Design the circuits in software, get layout and try implementing. Obtain the outputs ranging from 0.4-0.8V with max. efficiency.

Future Steps:

Finalize the way inputs and outputs propagate through system, which software to use to design the circuit and layouts and schematic. Also, clear the doubts if any more question pops up. So, the basic design will be as shown as in figure 5.

Different Topologies from other Paper:

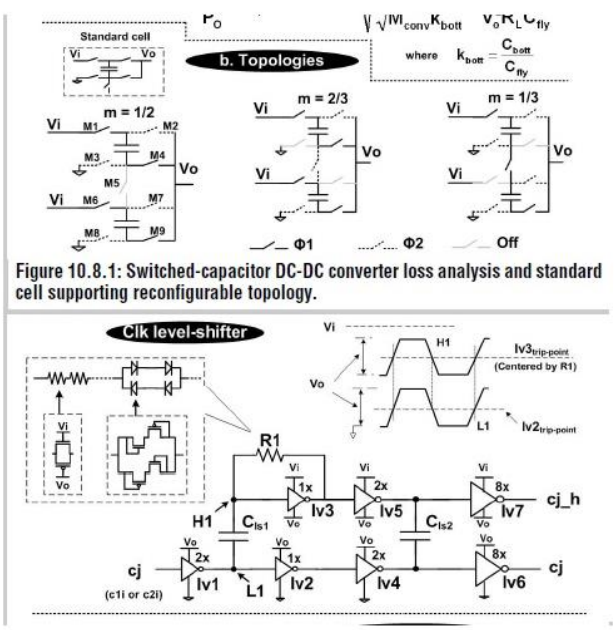

Figure 10.8.1: Switched-capacitor DC-DC converter loss analysis and standard cell supporting reconfigurable topology.

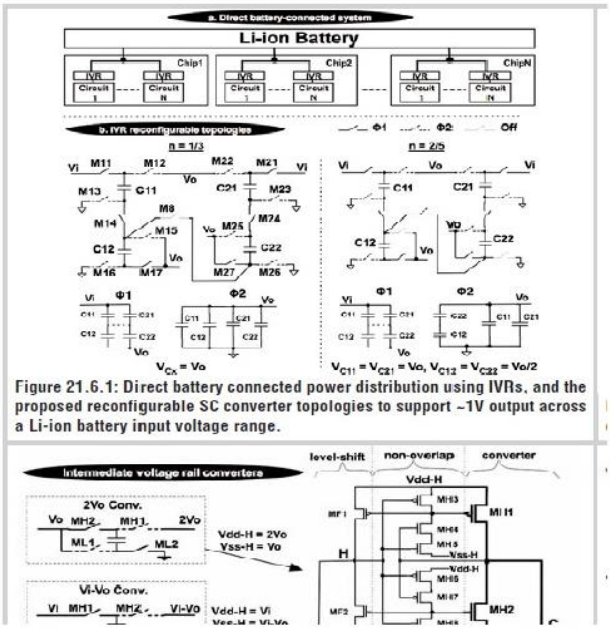

Figure 21.6.1: Direct battery connected power distribution using IVRs, and the proposed reconfigurable SC converter topologies to support ~1V output across a Li-ion battery input voltage range.

These circuits show various topologies found in various literatures and thus, the circuit design discussed in the beginning is the main circuit which will lay base for this project's model.

Literature referred:

1. (Base for Project): Fully-Integrated Distributed Switched Capacitor DC-DC Converter With High Density MIM Capacitor in 22 nm Tri-Gate CMOS. IEEE JOURNAL OF SOLID-STATE CIRCUITS, VOL. 49, NO. 4, APRIL 2014

2. Fully Integrated Reconfigurable Switched-Capacitor DC-DC Converter Delivering 0.55W/mm2 at 81% Efficiency. ISSCC 2010 / February 9, 2010

3. A Sub-ns Response Fully Integrated Battery-Connected Switched-Capacitor Voltage Regulator Delivering 0.19W/mm2 at 73% Efficiency. ISSCC 2013 / February 20, 2013

4. 3.7µW 0.8V VCO-Integrator-Based High-Efficiency Capacitor-Free Low-Dropout Voltage Regulator.

5. On-Chip Hybrid Regulator Topology for Portable SoCs with Near-Threshold Operation.