A 0.45–1 V Fully-Integrated Distributed Switched Capacitor DC-DC Converter With High Density MIM Capacitor in 22 nm Tri-Gate CMOS

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***Abstract*—A fully integrated switched capacitor voltage regulator (SCVR) with on-die high density MIM capacitor, distributed across a 14 KB register file (RF) load is demonstrated in 22 nm tri-gate CMOS. The multi-conversion-ratio SCVR provides a wide output voltage range of 0.45–1 V from a fixed input voltage of 1.225 V. It achieves 63–84% conversion efficiency and supports a maximum load current density of 0.88 A/mm^2. The area overhead of the dedicated SCVR on the load is 3.6%. Measured data is presented on various performance indices in detail. Subsequent learning on tradeoffs between various factors like capacitance characteristics, conversion efficiency and current density are delineated and, correlated with theoretical estimates. Performance of RF array shows comparable results when powered with the SCVR and the external rail. The all-digital, modular design allows efficient spatial distribution across the load and hence robust power delivery. The extremely fast response times in the order of few nanoseconds is targeted to benefit agile power management. This work evinces voltage regulator technology as a standard homogenous CMOS component, which can proliferate DVFS domains for maximum energy and area benefits.**

***Index Terms*—CMOS digital power supply, distributed voltage regulators, integrated voltage regulators, many voltage domains, switched capacitor voltage regulator.**

I. Introduction

RECENT advances in mobile electronics show explosive growth in the demand for compute power, data storage and, the number of RF and analog interfaces mandated by increasingly context-aware and perceptual user experience. These factors combined with the compact form factor demands and, extreme sensitivity to cost and energy are driving innovations in mixed-signal SoCs at an unprecedented rate. Power delivery in mixed-signal systems-on-chips (SOC) is inherently challenging due to many voltage domains. With today's processors adopting modular execution architectures, voltage domains are proliferating to reduce active and stand-by power by exploiting unique workloads and $\mathrm{V_{min}}$s across functional blocks, e.g., [1]. With the possibility of low-foot-print CMOS voltage regulators (VR) that are truly akin to other functional blocks, an arbitrary number and placement of these VRs in the die become a reality. This enables dedicated VRs at any granularity allowing system-level cost and energy optimizations. They can also be spatially distributed across the load ensuring true proximity to the switching event; therefore, voltage sources are fast and robust with tighter noise margins at the same time.

One of the gaps experienced in power delivery is the incompatibility of the lithium ion battery voltage (3.6 V per cell) and the maximum voltage that the die can withstand in the advanced CMOS technology nodes. The limiting factor may be the break-down voltage of the back-end dielectrics or transistor gates. This imposes a natural contention between (a) the number of voltage rails needed for DVFS and, (b) a single stage voltage step-down for reduced conversion losses.

Efficient integrated voltage regulators (IVR) at the point of load, supplied by a minimum number of incoming rails from a PMIC is examined here and turns out to have significant energy benefits. Fig. 1(a) shows the average power consumption of a block under alternate power delivery scenarios namely, a shared rail and a dedicated rail. In the former case, power is plotted as a function of β, which is defined as the percentage of the idle time of the block that the shared rail is at $\mathrm{V_{min}}$. In the latter, it is plotted as a function of the conversion efficiency of the dedicated VR. For a realistic case of activity factor $\alpha = 0.1, \mathrm{V_{min}} = 0.55$ V and $\beta = 0.1$ ($\beta = 1$ for a dedicated rail), a VR with 80% can yield 37% energy savings as highlighted, indicating the power savings potential when blocks have non-homogeneous functionality or workloads like in an SoC. Fig. 1(b) presents the power consumption of a near threshold voltage (NTV) core at a given performance under various power delivery scenarios. The minimum power consumption corresponds to a dedicated external rail; however this option becomes prohibitive with increased number of rails. Down-conversion of voltage using IVRs has a conversion loss penalty, which may be circumvented where possible,[1] with input volt-

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[1]When bumps and noise requirements do not mandate down-conversion of supply voltage.

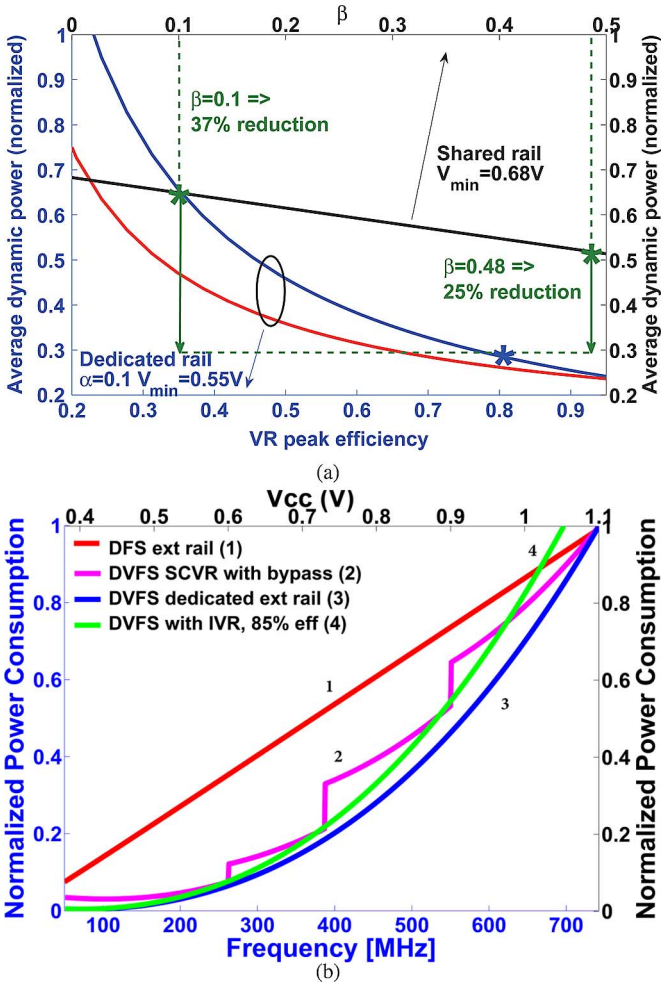


Fig. 1. Power benefit from many voltage domains via fully integrated voltage regulators. (a) Average power consumption at typical usages. Black: Shared rail, $\alpha \triangleq$ residency in high frequency modes (HFM) where $V_{cc} = V_{max}$; $\beta \triangleq$ % of idle time the shared rail allows $V_{cc} = V_{min}$ else V_{max}; Red: Dedicated rail with $V_{in} \approx V_{max}$ and VR is bypassed in HFM; Blue: Dedicated rail with $V_{in} \gg V_{max}$ with no VR bypass option, (b) DVFS benefits using data from NTV core, Courtesy—Sriram Vangal, Intel.

ages around Vmax as shown by the bypass mode in SCVR. It can be seen that it approaches the best case in the critical operating ranges that experience high residencies typically. Multiple domains thus enabled will fragment the existing resources namely, the metal grids and decoupling capacitors into dedicated blocks. However, fewer unique input voltage rails keeps power delivery to the die tractable and will allow die-package interconnections to be retained as a big pool. These do not scale with the transistor gate length, e.g., C4 bump pitch has followed a sub-Moore scaling trend per ITRS, scaling 0.67x in 6 years as opposed to 0.7x every 2 years.

Therefore, fast and efficient on-die voltage regulators that can be fully integrated with minimal area and process complexity overheads are essential for dynamic voltage and frequency scaling (DVFS) in multi-voltage designs. These capabilities combined with a wide output voltage (V_{out}) range can maximize energy efficiency. There are several past publications on fully integrated voltage regulator solutions [2], [3]. With the domain area and power getting smaller in fine grained voltage domains, conventional inductor based switched converters

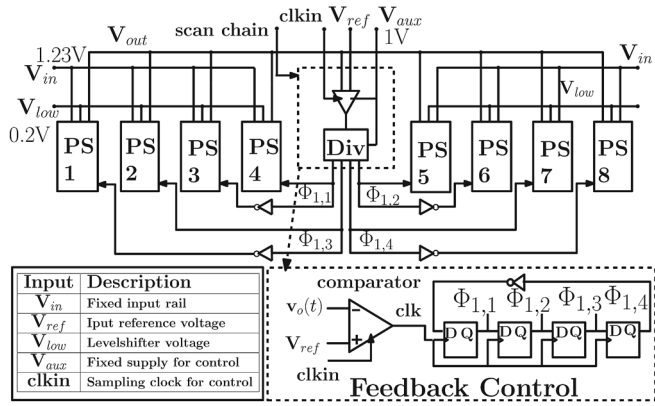


Fig. 2. SCVR architecture.

suffer from scalability limitations in size and power [4], [5]. Recently, switched capacitor DC-DC converters have emerged with increased current capability and consequent regulation mechanisms over its traditional application as a charge pump [10]–[16]. Recognizing that a 1 A/mm^2 load would incur 50% additional silicon area when using a 2 A/mm^2-capable dedicated IVR, the IVR current densities should far exceed what is observed in the PMIC VRs. An area overhead metric is proposed, in addition to the current density in the context of fine grained voltage domains, defined as the silicon footprint of the VR as a percentage of load area.

In this paper, we present a fully integrated switched capacitor voltage regulator (SCVR) with high density metal-insulator-metal (MIM) capacitors implemented in 22 nm tri-gate CMOS [6]. The SCVR is distributed across a 14 KB register file (RF) array with V_{out} range spanning V_{min}. The chip design features: (a) a high density on-die MIM capacitor, residing between M8 and M9 above the load, used as fly and decoupling capacitors; (b) down-conversion capability from a fixed 1.225 high voltage input using thin gate 22 nm tri-gate transistors; (c) a wide V_{out} range of 0.45–1.05 V with four peak-efficiency voltages at conversion ratios of 2:1, 3:2 and 5:4 and 1:1; (d) all-digital feedback control for area-efficient integration (e) an 8-way interleaving for output voltage ripple cancellation; (f) fast start up and response times of a few ns; and (g) minimal droop at load transients.

II. SCVR Architecture and Components

A modular power stage architecture is used that handles high voltage input as shown in Fig. 2. Eight identical power stage modules are used, one for each interleaved phase for ripple cancellation. Uniformly phase shifted clocks are generated for each of the interleaved phase in the central feedback control, that regulates the output voltage using frequency modulation. Two separate rails are externally provided—one for level shifting purposes and the other for control circuits.

A power stage module consists of two basic power cells, each is a 10 switch, 2 capacitor series-parallel topology as shown in Fig. 3, for daisy chaining of four capacitors that allow output resolutions of 1/n, where $n \leq 5$. This topology has the best capacitance utilization with regards to the capacitors contribution to the output resistance [8].

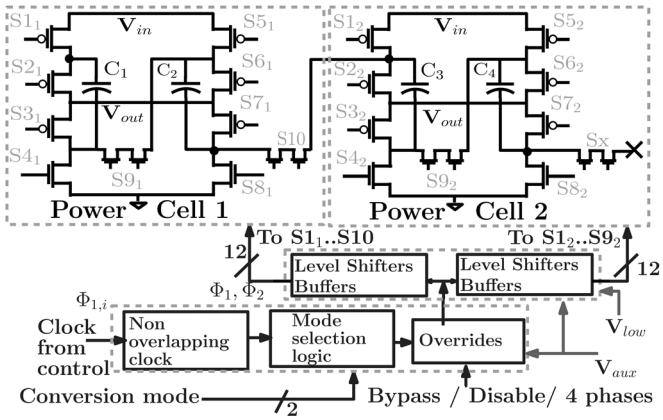


Fig. 3. Power stage module.

Four voltage step-down modes are used in this topology, namely, a 1:1 which is an inherent "switched LDO", 5:4, 3:2, and 2:1 to generate ideal V_{out} at 1.225, 0.98, 0.8, and 0.612 V, respectively. The 1:1 mode may be replaced by a digital LDO with marginal control overhead for lower dropout voltage; however this mode was instrumental in characterizing various loss mechanisms at 1 V and full load. These modes realize evenly spaced high efficiency regions covering the output voltage range of interest, with efficiency linearly dropping in the intermittent regions. This is because all fine regulation strategies in a switched capacitor converter like frequency, switch resistance, capacitance or duty cycle modulates the equivalent output resistance R_{out} as shown by an averaged model in Fig. 4. This model for a representative example of a 2:1 circuit illustrates the fundamentally lossy nature of regulation in Fig. 4(b). Reconfiguring conversion ratio m:n where m and n are integers provides a lossless coarse regulation mechanism that is taken advantage for large voltage ranges of operation [9].

The non-overlap clock generator (Fig. 3) inserts a fixed dead time to avoid shoot-through currents in the power stage. The mode select block generates the gate drive signals for each of the 10 switches of the two power cells, based on the conversion mode select bits and the over rides. The gate drive signals to the MOSFETs that connect to the Vin rail namely S_1, S_2, S_5 and S_6 are level shifted to V_{low} to limit transistor voltages below the rated 1.05 V, and further buffered appropriately. The switches S_9 and S_{10} are cascoded. The schematic of the level shifter used is shown in Fig. 6.

Over-rides for a bypass/power gate mode and an SCVR disable mode are included for independent characterization of the RF arrays. Fig. 5 shows the transistor states during the two phases of a switching cycle in various modes. A 4 phase mode is also enabled for lighter operating conditions which include low currents and voltages farther away from the ideal levels mentioned in any conversion mode. An external voltage rail V_{aux} of 1 V powers all the control circuits for ease of power break down and characterization. This also powers the buffers that drive lower switches (e.g., S_3, S_4, S_7 and S_8) in the power stage.

A clocked comparator based lower-bound hysteresis control is used to realize frequency modulation for the feedback as shown by Fig. 7 [9]. Frequency modulation offers the full range of regulation required by the wide operating ranges in output voltages and current conditions and also results in all loss mechanisms namely the capacitor charge-discharge losses and, the transistor conduction and switching losses to scale with load. Besides the fact that clocked comparator based approach incurs minimal power overhead (100 μW at 2 GHz), it also eliminates the need for start-up and other assist circuits that is otherwise required when implemented using an analog comparator. The clocked comparator design is derived from a latch based sense amplifier as shown in Fig. 7(b). A clock divider generates the uniformly phase-shifted 50% dutycyle clocks $\Phi_{1,i}$ at $\leq$250 MHz for each power stage (Fig. 8) resulting in 8-way interleaving. The frequency f_{ripple} of clkin f_{clkin} is assumed to be $\gg$ the expected ripple frequency for simplicity of illustration.

III. Distributed SCVR Design Across Register File Array

The top half of the die image (Fig. 9) is the active experiment area with probe pads for the membrane probe interface occupying the bottom half. This is done to avoid artificially and overly constraining the use of MIM because of the probe pad being at a tighter pitch compared with C4 bumps. The register file (RF) array is implemented as four quadrants of 3.5 KB modules, with the MIM capacitors for SCVR placed on the top (Fig. 9). High density MIM capacitor resides between M8 and top metal (M9) as shown in Fig. 10(a) [6], [7]. Eight power stage modules are placed in the central strip across the RF for symmetrical location with respect to the MIM capacitors, and RF arrays being custom blocks with a modular design, allowed this degree of intrusion. This alleviates metal resource demand for low-resistance routing between the capacitor terminals and the switches which would otherwise dominate in the case of contiguous load blocks where the VR circuits will have to be placed along the periphery. The feedback control block is placed in the middle and the clocks, $\Phi_{1,i}$ are routed to each module. The fly capacitors add up to a total capacitance of 1.6 nF. A nominal 100 pF MIM is used explicitly at the output node for decoupling, to take advantage of the intrinsic capacitance of the RF arrays and its default nature of scattered switching events. The area utilization is summarized in Fig. 10(b).

All metal layers on the SCVR power stage strip in the middle are heavily used, and the congestion is exacerbated by multiple auxiliary rails for VR housekeeping and high voltage rules associated with the input voltage and independent test/debug of the dual-Vcc RF. Output voltage of the SCVR is heavily gridded on all layers from M8 and below. This allows better quality MIM templates and also saves the need for ESD clamps and package decoupling in the real scenario. However, for our experiment, these are sparingly routed to the pads for test and debug.

A. Capacitor Layout and Routing—Design Considerations

The bottom plate parasitics are negligible in these MIM capacitors as they are placed on the top metal layers. The top plate parasitics of the top electrode to the top metal tracks are estimated to be less than 1%. However, the intrinsic ESR combined with interconnect resistances (to and fro M9) are dominant and the layout has significant impact on the capacitance, ESR and the frequency response of the capacitor. Quality factor

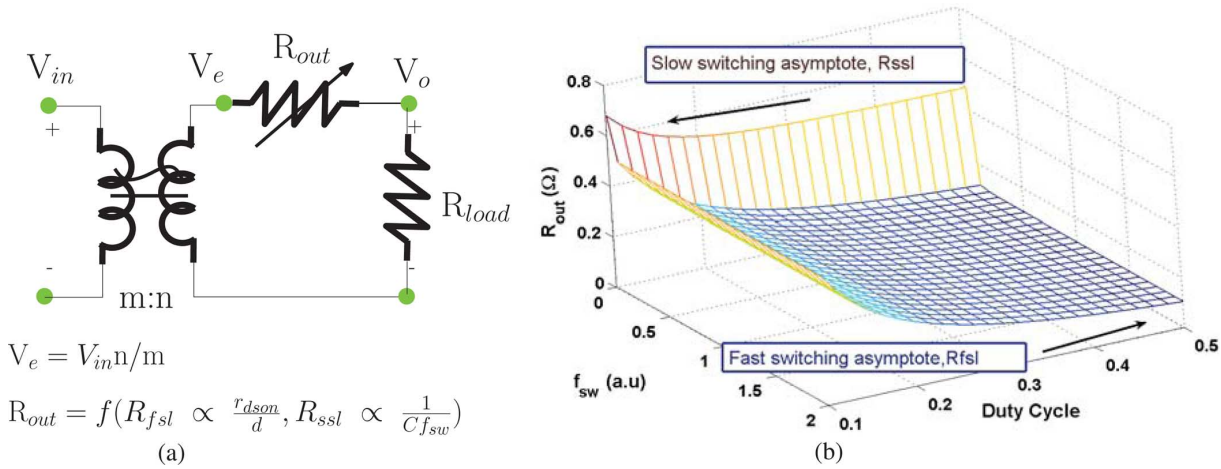


Fig. 4. Regulation in a switched capacitor converter. (a) Averaged model, (b) Exact solution of R_{out} as a function of f_{sw}, the switching frequency; d, the duty cycle between charge and discharge phases; for a given r_{dson}, the ratio-specific effective resistance from transistors, and C, the ratio-specific effective capacitance.

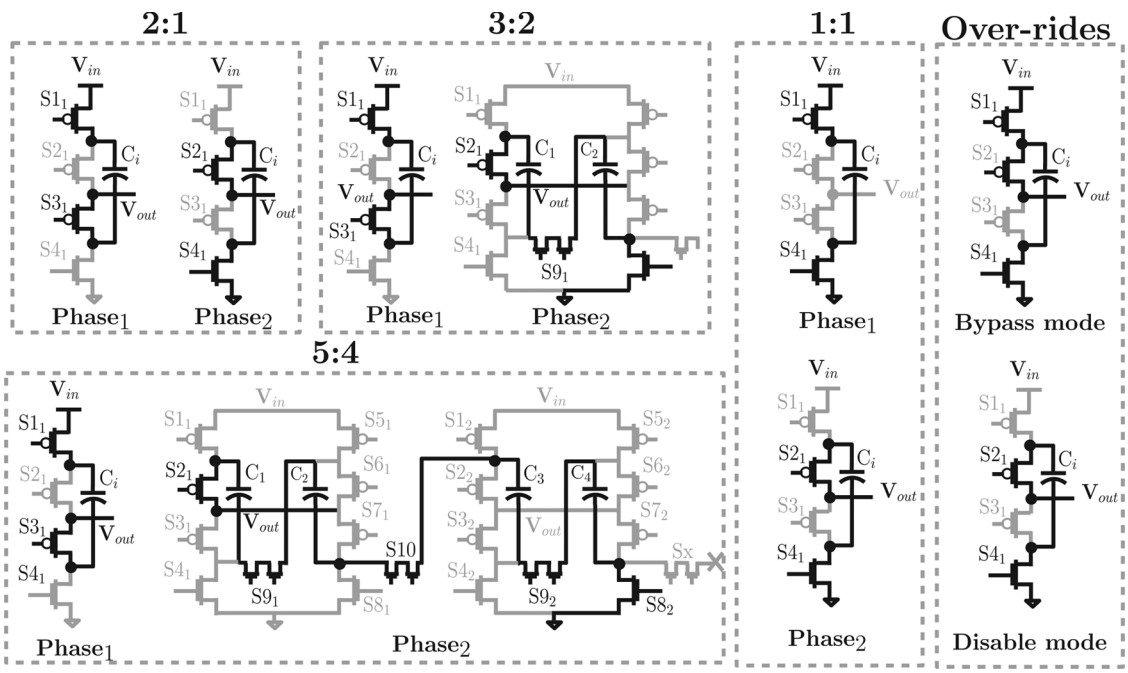


Fig. 5. Multiple transformation ratios.

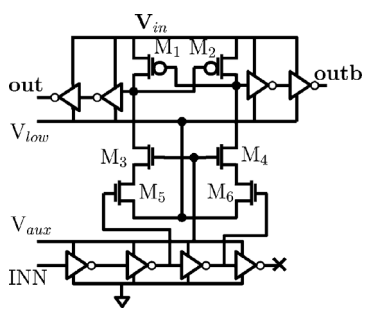


Fig. 6. Schematic of the level shifter.

of the capacitor was not a comprehensive metric for our purposes. We instead used R_{out} as our cost function, which was minimized. Two factors that still limited the optimal switching frequencies with MIM to be around 200 MHz were the excessive ESR, which in turn warranted for much larger transistor widths to maintain target current density, and the capacitance roll offs with frequency.

As a result, the MIM layout template of choice has the plate contacts placed as close to each other, to reduce intrinsic ESR. The width of a capacitor unit was determined by a routing template adopted for top metal, allowing two traces to be used for the capacitor terminals while reserving three for power and signal, resulting in 40% utilization on the top metal. Fly capacitor terminals are routed to the transistors through localized grids which resulted in increased local metal utilization on M8 in the central region between MIM contacts, which constitutes about 50% of MIM template area.

All the power MOSFETs are identical in size because of the reconfigurability required. The current flow through various switches and capacitors across all conversion modes were considered and the routing was designed based on electomigration and self heating guidelines for the worst case. The 1:1 mode

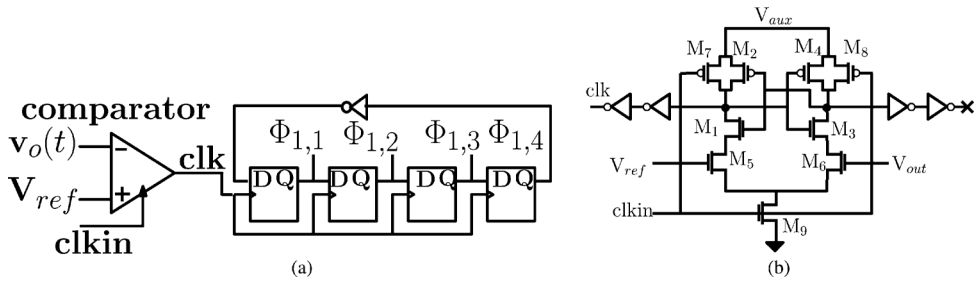


Fig. 7. Frequency modulation using lower bound hysteretic (LBH) control. (a) Lower bound hysteretic control. (b) Schematic of the clocked comparator.

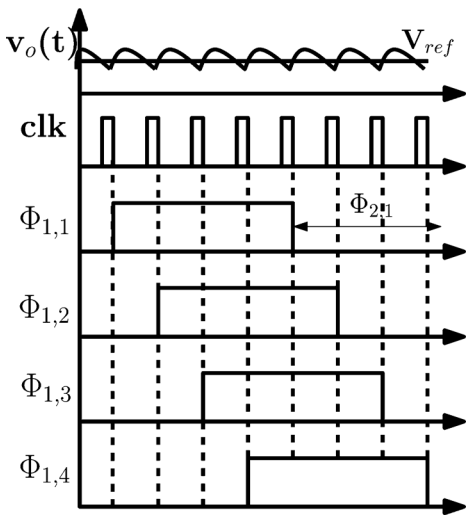


Fig. 8. Timing diagram for LBH control. Assume $f_{\mathrm{clkin}} \gg f_{\mathrm{ripple}}$ for illustration.

dominated all the corresponding switches and their routes, and 5:4 dominated the remaining. All the intermediate nodes in the power stage are gridded, however it is to be noted that for the highest current density experiments shown presented here, this resistance also starts to dominate and contributes to the increase in load line resistance at high currents.

IV. Performance Indices of the SCVR

The measurement set-up is shown in Fig. 11. The 2 GHz sampling clock for the comparator and clock for the RF are externally provided through high-frequency pads. All the external voltage rails are supplied through low-frequency pads. A total of 30 pads were used for characterizing both SCVR and RF. A common scan chain shared by the two was used for all the configure bits. Several muxes were used for observability due to the limited number of pads available. All the digital inputs are held constant during an experiment including the conversion ratio, as limited by the inability to modify select bits without affecting the others because of a simple scan chain design. The $\mathrm{V_{in}}, \mathrm{V_{low}}, \mathrm{V_{aux}}$ are held at fixed 1.225 V, 0.2 V, and 1.05 V DC, respectively, for all measurements discussed further.

A. Regulation and Transient Response—Measurements

Reference tracking capability of the SCVR in 1:1 mode is shown by the $\mathrm{V_{out}}$ in Fig. 12. The stimulus is a periodic step change in $\mathrm{V_{ref}}$ between 1.05 V and 0.65 V at a load resistance of 99 Ω. The seeming high frequency noise common to both the $\mathrm{V_{out}}$ and $\mathrm{V_{ref}}$ shown is measurement and/or signal processing artifacts. The color graded persistence plot substantiates this through the sample count shown and only the lighter regions correspond to the actual ripple at switching frequency. This is 43 mV peak to peak when captured at high sampling rate as shown by the inset in Fig. 12.

Fig. 13 corresponds to 1:1 mode with a load stimulus that is stepped from 15 mA (50%) to 30 mA (100%) of rated current in 20 μs as limited by the test equipment. A larger step from minimum load condition shown at 0.83 V in the inset shows no effect on the $\mathrm{V_{out}}$.

Start up transient is stimulated by a step in $\mathrm{V_{ref}}$ from 0 V in 2:1 mode with a load of 99 Ω. $\mathrm{V_{ref}}$ is supplied through a low frequency pad, hence slow ramp is observed in Fig. 14. The waveform indicates instantaneous start-up upon $\mathrm{V_{ref}}$ reaching a threshold of 0.2 V. The ringing observed limits further high speed measurements. This arise from the use of 25 kOhm probe tip to avoid the loading of the sense point that would otherwise result from a 50 Ohm termination.

B. Droop and Start-Up Transients—Simulations

Because of the practical difficulty in capturing fast response times discussed above, simulation results from the same circuit in 1:1 mode are shown in Fig. 15. Fig. 15(a) shows 3.6 ns start-up time to reach a full 0.95 V at rated load. Droop simulations with representative parasitic numbers for a power delivery network show negligible output droop in Fig. 15(b).

C. Ripple—Measurements and Implications

Output voltage regulation via frequency modulation is demonstrated in Fig. 16. Measured peak to peak ripple is shown in Fig. 16(a). The key limitation of using frequency modulation not augmented with other conductance modulation schemes is the increased ripple at the output during operating conditions that result in low switching frequencies. This also attributes to the impulsive input currents characteristic of slow switching mode where the capacitor voltages equilibrate in every cycle. However, for extremely low power levels such as this prototype this may still be adequate because the ripple is asymmetric about the $\mathrm{V_{ref}}$ as shown by Fig. 16(c). Any comparator offset, sampling delay and the delay introduced by various control blocks are the key factors contributing to the offset between the minimum $(\mathrm{V_{out}(t)})$ and $\mathrm{V_{ref}}$. This may be minimized through careful choice of sampling frequency relative to the highest ripple frequency and, delay-aware design and layout in general.

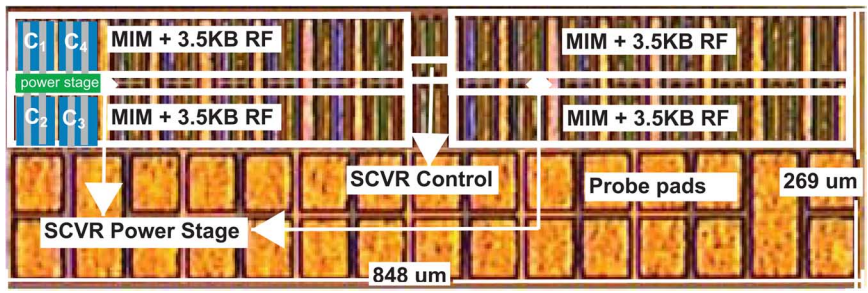
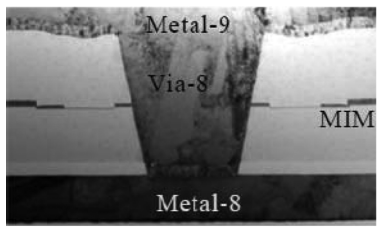


Fig. 9. Die image.



(a)

Technology	22nm Tri-gate CMOS
Passive Type	High Density MIM
MIM Area	99450 μm^2
Power Stage Area	3240 μm^2
Control Area	420 μm^2
Total Active Area	3660 μm^2
Total RF Area	101376 μm^2
Test Interface	Membrane probe

(b)

Fig. 10. MIM and silicon area usage. (a) High density MIM. (b) Area break up.

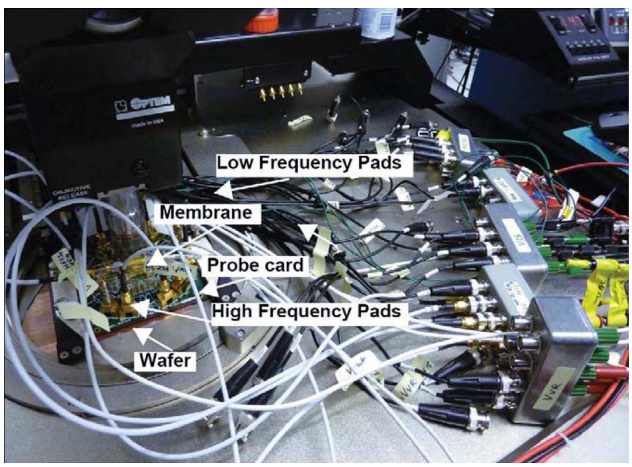


Fig. 11. Test setup.

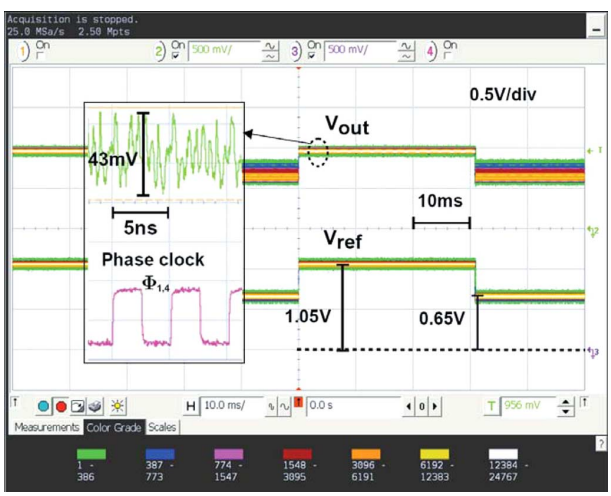


Fig. 12. Reference tracking.

Further, a correction on V_{ref} may be applied to compensate for the net offset.

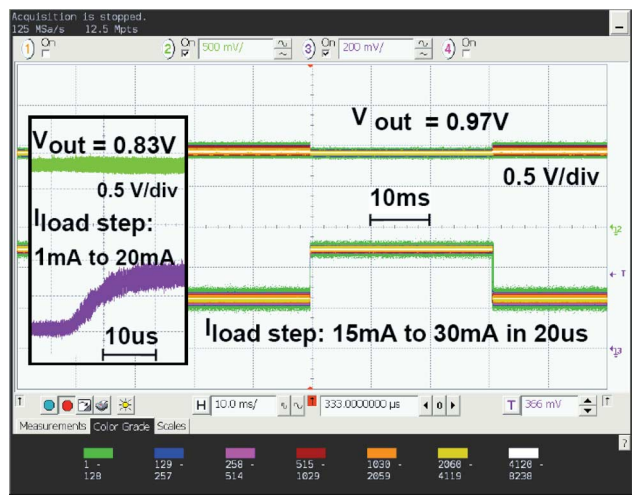


Fig. 13. Output voltage regulation with load steps.

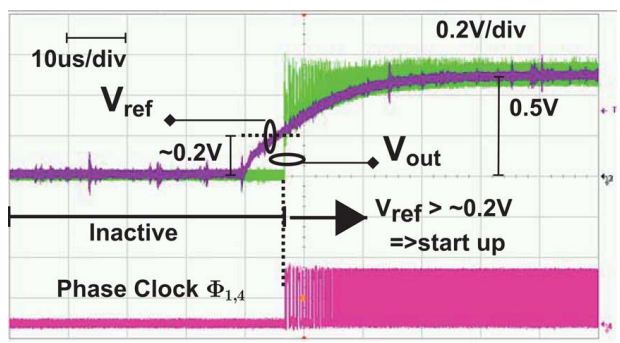
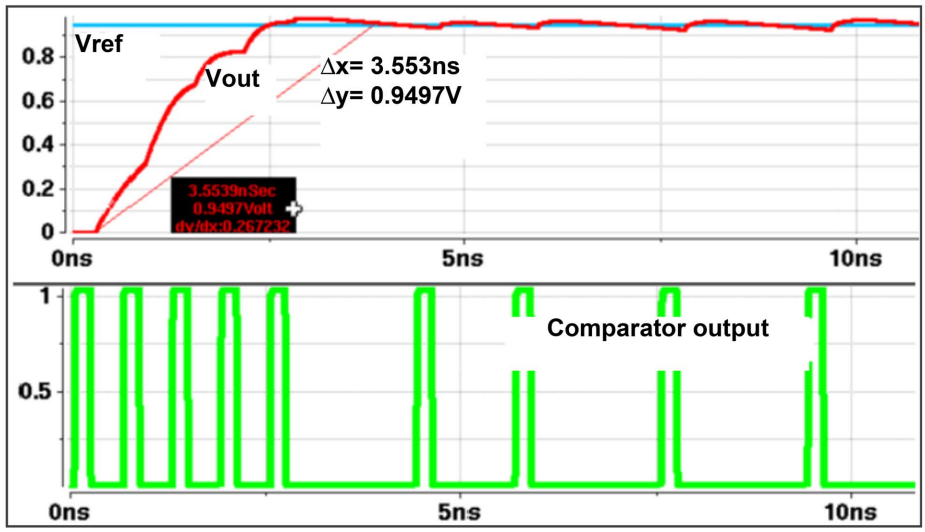
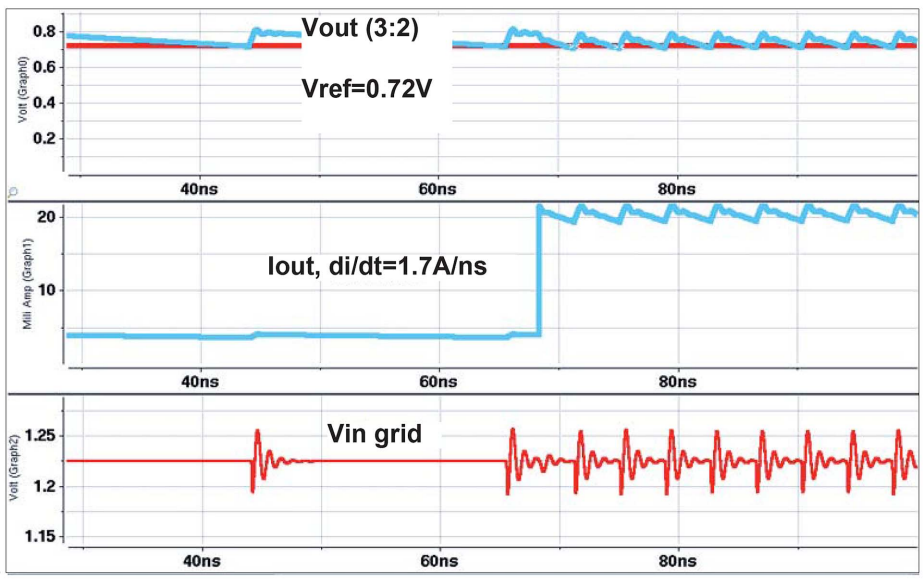


Fig. 14. Start-up measurements.

Lower bound hysteretic control bounds the minimum value of the V_{out} to V_{ref}-Δ (a function of the factors described earlier). The conversion ratio asserts an upper bound on the average value of the V_{out} to the respective V_{ideal}, thereby yielding unconditional stability. The implementation using clocked comparator requires a choice of the sampling frequency within



(a)



(b)

Fig. 15. Simulation results. (a) VR response time during start up. (b) Output voltage droop with an input power delivery network.

a specified range to avoid potential sub-harmonic oscillations [9], which otherwise would result in increased losses and $\max(\mathrm{V_{out}(t)})$. It can be seen that the allowed range is dependent on the maximum optimal switching frequency of the design and the control delays.

A power utilization factor (PUF) can be defined to quantify the effect of ripple on the overall power efficiency, which is characteristic of the load. For a resistive load, PUF is 1. For a logic load where $\mathrm{V_{min}}$ determines the useful throughput, PUF may be defined as $\mathrm{V_{min}^2/V_{rms}^2}$ thereby penalizing the ac component in the VR output voltage. This when multiplied with a classic VR conversion efficiency yields the net useful power efficiency.

D. Conversion Efficiency—Measurements

Overall conversion efficiencies higher than 63% are measured in the range of 0.45–1.05 V. A peak efficiency of 84.2% (82.7%) is attained at 1.1 V and 13 mW (25 mW) with external resistive load (Fig. 17(a)). The power drawn from all the voltage rails have been included in this calculation. V_{ref} and clkin are availed externally and the power required for generating these have not been estimated or included.

A dynamic high-activity load was emulated by reading all 14 KB RF bits simultaneously as shown by Fig. 17(b). Efficiency measured is 80.7% (78%) at 14.5 mW (30 mW). The difference of 3–4% in efficiency between the load types is primarily because of the noise induced by the load on $\mathrm{V_{out}}$ that is comprehended in the computation of the useful power for the RF. This includes the effect of the steady state PUF described earlier. This also signifies the dynamic effects of such loads and the consequent need for additional decoupling at the $\mathrm{V_{out}}$ in addition to the intrinsic capacitance. There is also degradation in the expected decoupling from fly capacitors, attributed to the relatively high equivalent series resistance (ESR) and interconnect resistances of the MIM. This data in 1:1 mode is also representative of the peak efficiency that can be achieved in other

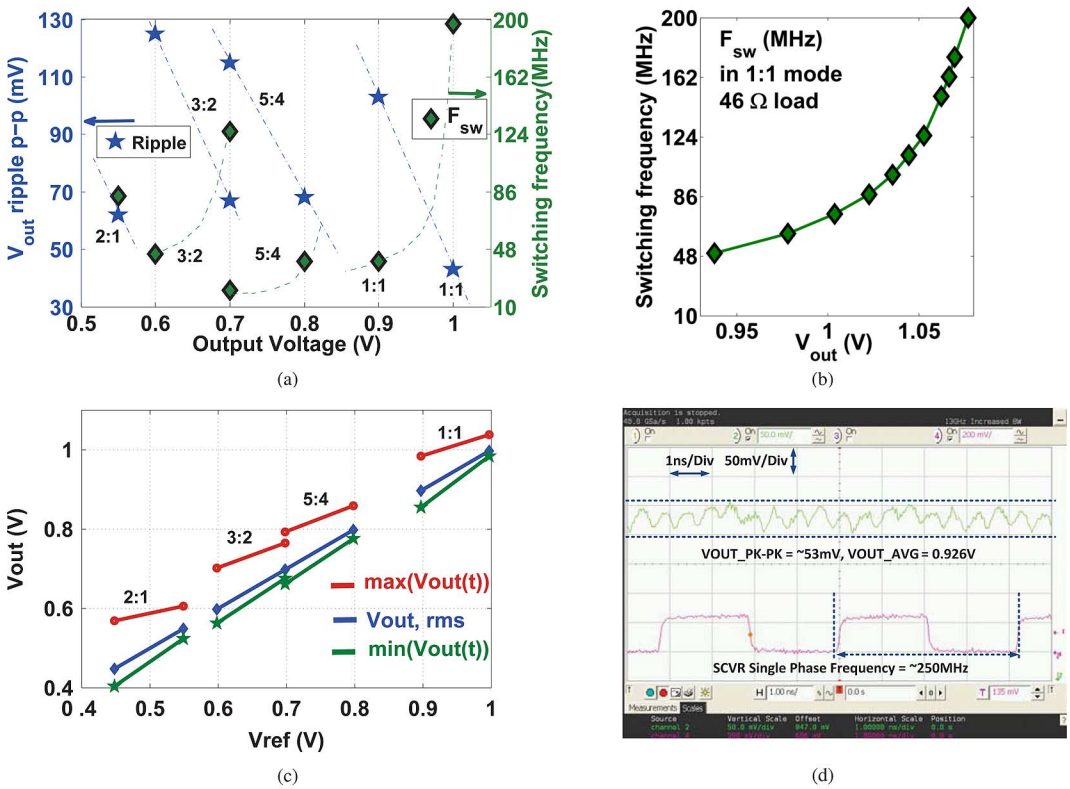


Fig. 16. Ripple characteristics across operating conditions. (a) Peak to peak ripple. (b) Switching frequency. (c) Minimum of $\mathrm{V_{out}}(t)$ (measured). (d) Output waveform.

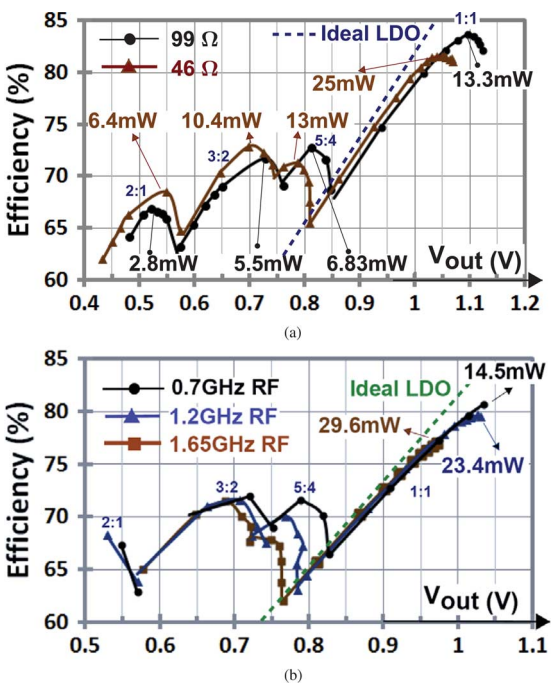


Fig. 17. Conversion efficiency across load types. (a) Constant resistive load. (b) High activity factor dynamic load.

modes with switch sizes optimal for the power levels. Efficiency is constant across 10% to 100% of the rated load as shown in Fig. 18.

E. Current Capability and Output Resistance—Measurements

The load line measurements from 1:1 and 2:1 modes are shown by Fig. 19. The maximum load current is divided by

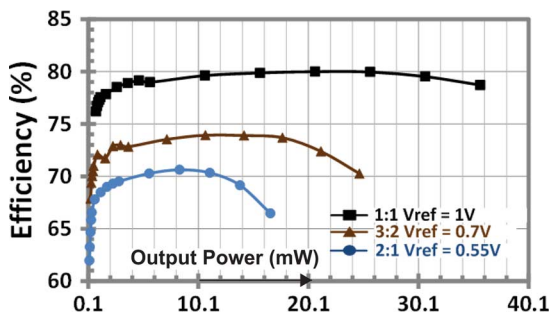


Fig. 18. Efficiency measurements as a function of load.

the total SCVR area of 103110 μm^2 that includes the MIM (Fig. 10(b)) to compute the current densities. The SCVR supports a maximum load current density of 0.4 A/mm^2 in 1:1 mode and 0.88 A/mm^2 in 2:1 mode. Theoretical estimates on $\mathrm{R_{out}}$ assuming ideal grids show that 2:1 is capable of 4 times the current capability of 1:1 mode, at same output voltage, switch size and switching frequency. $\mathrm{R_{out}}$ is derived from the model for the series parallel circuit as described in [8], as the root-mean-squares of the slow and fast switching limits (SSL and FSL). The corresponding numbers for 3:2 and 5:4 modes (Fig. 3) are 2x and 1.56x, respectively. The measured output resistance on 2:1 (Fig. 19) indicate that the interconnect resistance contributions limit its current capability to 2.85x of 1:1 at any given drop out voltage, $\Delta V_{\mathrm{dropout}} = V_{\mathrm{out}} - V_{\mathrm{ideal}}$. The level shifter design limits the input voltage to 1.4 V, thereby limiting the measurements for 2:1 from being carried out at $\mathrm{V_{out}}$ similar to 1:1. Further deviation observed at high load conditions in 2:1 is due to the degradation of the on-resistance of the PMOS S3 and S7 at low $\mathrm{V_{out}}$s.

TABLE I
COMPARISON WITH OTHER FULLY INTEGRATED SWITCHED CAPACITOR VOLTAGE REGULATORS

Reference	L. Chang VLSI 2010	Y. Ramadass ISSCC 2010	D. Somasekhar VLSI 2009	H. -P. Le ISSCC 2010	This work
Process	45nm SOI	45nm	32nm	32nm SOI	22nm trigate
Passives type	Deep trench	Gate Oxide SOI	Metal Finger	Gate Oxide	MIM
Maximum frequency	100MHz	30MHz	1GHz	225MHz	250MHz
Input Voltage	2V	1.8V	1-1.2V	2V	1.23V
Output	0.95V/2.7mA	0.8-1V/8mA	1.5V/5mA	0.4-1.1V/0.28A	0.45-1V, 88mA
Power Efficiency %	90	69	60	81	70@0.55V,84@1.1V
Response time	Unregulated	120-200ns	Unregulated	Unregulated	3-5ns†
Droop	-	250mV	-	-	$\ll$25mV†
Current density A/mm^2	2.3	0.050	1.12	0.73	0.88
Area Overhead	13%	6x	26%	41%	3.6%

† The fast transient numbers are derived from simulation results.

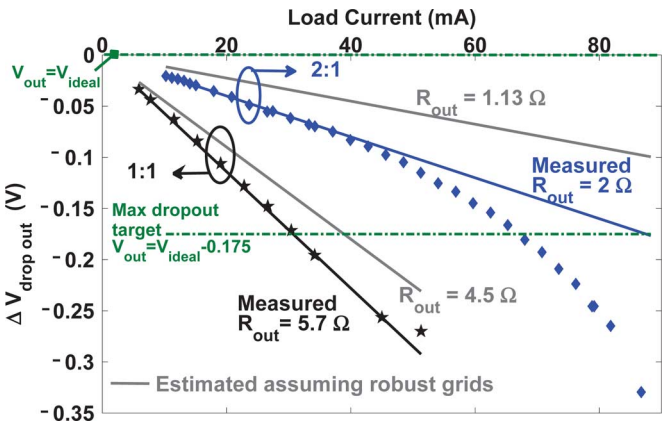


Fig. 19. Current capability measurements in 2:1 and 1:1 mode.

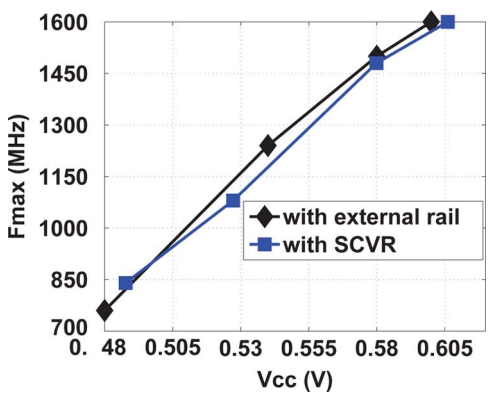


Fig. 20. F_{max} vs. Vcc measurements for register file array.

F. Impact on RF Array Performance—Measurements

The maximum operating frequencies of the RF array at different voltages when supplied by the SCVR are comparable to those when powered with an external rail (Fig. 20). A pre-programmed clock sequence was used to sweep the pulse width of the word line access (in other words, the read frequency) to find f_{max}. The tests have been performed on 1 Kbit RF bits across all four quadrants on the arrays closest and farthest from the center where the decoupling capacitor is located. The data shown corresponds to the closest array. The arrays farthest see slight deterioration in f_{max}, and reinforces the need for higher/distributed decoupling capacitance. This problem may be circumvented by enabling MOS capacitance in the white space in the load area for distributed and high quality decoupling.

V. SUMMARY AND CONCLUSION

The key metrics from the work have been compared with previously reported fully-integrated switched capacitor DC-DC converters using different capacitor technologies and are shown in Table I [11]–[14]. While there are several interesting works in this area, we have focused on solutions that are viable to supply few hundreds of mA as opposed to the traditional sub mA currents targeted in the past. A 1 A/mm^2 reference load would incur a 50% VR area overhead when using a 2 A/mm^2 VR. Thus, in addition to the traditional current density metric for VRs, area overhead metric becomes important in the context of fine grained voltage domains—defined as the silicon footprint of the VR as a percentage of load area. We have used the VR current density numbers reported in these works and projected their area overhead for a representative load of density 300 mA/mm^2 for comparison. The table reveals similar conversion efficiency and maximum load current density with significantly low die area overhead.

A fully integrated switched capacitor voltage regulator (SCVR) with on-die high density MIM capacitor, distributed across a 14 KB register file (RF) load is demonstrated in 22 nm tri-gate CMOS. The multi-conversion-ratio SCVR provides a wide output voltage range of 0.45–1V from a fixed input voltage of 1.225 V. It achieves 63–84% conversion efficiency and supports a maximum load current density of 0.88 A/mm^2. The area overhead of the dedicated SCVR on the load is 3.6%. Measured data is presented on various performance indices in detail. Subsequent learning on tradeoffs between various factors like capacitance characteristics, conversion efficiency and current density are discussed and correlated with theoretical estimates. Performance of RF array shows comparable results when powered with the SCVR and the external rail. The all-digital, modular design allows efficient spatial distribution across the load and robust power delivery. The extremely fast response times in the order of few nanoseconds is targeted to benefit agile power management. This work evinces voltage regulator technology as a standard homogenous CMOS component, which can proliferate DVFS domains for maximum energy and area benefits.

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REFERENCES

[1] J. Kulkarni *et al.*, "Dual-VCC 8T-bitcell SRAM array in 22 nm tri-gate CMOS for energy-efficient operation across wide dynamic voltage range," in *VLSI Circuits Symp.*, 2013.

[2] G. Patounakis *et al.*, "A fully integrated on-chip DCDC conversion and power management system," *IEEE J. Solid-State Circuits*, vol. 39, pp. 443–451, 2004.

[3] J. Wibben *et al.*, "A high-efficiency DCDC converter using 2 nH integrated inductors," *IEEE J. Solid-State Circuits*, vol. 43, pp. 844–854, Apr. 2008.

[4] S. Sanders *et al.*, "The road to fully integrated DCDC conversion via the switched-capacitor approach," *IEEE Trans. Power Electronics*, vol. 28, pp. 4146–4155, 2013.

[5] G. V. Pique and R. Karadi, "Potential benefits of integrated switching power converters: Inductive vs. switched-capacitor," in *IEEE Int. Workshop Power Supply on Chip*, Nov. 2012.

[6] C.-H. Jan *et al.*, "A 22 nm SoC platform technology featuring 3-D tri-gate and high-k/metal gate, optimized for ultra low power, high performance and high density SoC applications," in *IEDM Tech. Dig. 2012*, pp. 44–47.

[7] C. Auth *et al.*, "A 22 nm high performance and low power CMOS technology featuring fully-depleted tri-gate transistors, self-aligned contacts and high density MIM capacitors," in *VLSI Technology Symp.*, Jun. 2012, pp. 131–132.

[8] M. D. Seeman and S. R. Sanders, "Analysis and optimization of switched capacitor DC-DC converters," *IEEE Trans. Power Electronics*, vol. 23, pp. 841–851, 2008.

[9] R. Jain and S. Sanders, "A 200 mA switched capacitor voltage regulator on 32 nm CMOS and regulation schemes to enable DVFS," in *European Conf. Power Electronics*, 2011, pp. 1–10.

[10] T. Van Breussegem and M. Steyaert, "Monolithic capacitive DC-DC converter with single boundary multiphase control and voltage domain stacking in 90 nm CMOS," *IEEE J. Solid-State Circuits*, vol. 46, no. 7, pp. 1715–1727, 2011.

[11] L. Chang *et al.*, "A fully-integrated switched-capacitor 2:1 voltage converter with regulation capability and 90% efficiency at 2.3 A/mm^2," in *VLSI Circuits Symp.*, 2010, pp. 55–56.

[12] Y. Ramadass *et al.*, "A fully-integrated switched-capacitor step-down DC-DC converter with digital capacitance modulation in 45 nm," *IEEE J. Solid-State Circuits*, vol. 45, no. 12, pp. 2557–2565, Dec. 2010.

[13] D. Somasekhar *et al.*, "Multi-phase 1 GHz voltage doubler charge-pump in 32 nm logic process," *IEEE J. Solid-State Circuits*, vol. 45, no. 4, pp. 751–758, 2010.

[14] H.-P. Le *et al.*, "Design techniques for fully integrated switched-capacitor DC-DC converters," *IEEE J. Solid-State Circuits*, vol. 46, pp. 2120–2131, 2011.

[15] D. El-Damak *et al.*, "A 93% efficiency reconfigurable switched-capacitor DC-DC converter using on-chip ferroelectric capacitors," in *IEEE ISSCC Dig. Tech. Papers*, 2013, pp. 374–375.

[16] G. V. Piqué *et al.*, "A 41-phase switched-capacitor power converter with 3.8 mV output ripple and 81% efficiency in baseline 90 nm CMOS," in *IEEE ISSCC Dig. Tech. Papers*, 2012, pp. 98–101.

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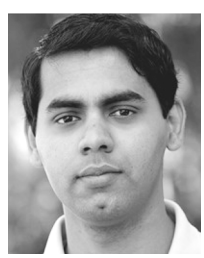

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