Reliability and Safety Analysis

Year: 2022 Semester: Fall Team: 05 Project: Metaporter

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Assignment Evaluation:

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| --- | --- | --- | --- | --- |
| **Item** | **Score (0-5)** | **Weight** | **Points** | **Notes** |
| **Assignment-Specific Items** | | | | |
| **Reliability Analysis** |  | x2 |  |  |
| **MTTF Tables** |  | x3 |  |  |
| **FMECA Analysis** |  | x2 |  |  |
| **Schematic of Functional Blocks (Appendix A)** |  | x2 |  |  |
| **FMECA Worksheet (Appendix B)** |  | x3 |  |  |
| **Writing-Specific Items** | | | | |
| **Spelling and Grammar** |  | x2 |  |  |
| **Formatting and Citations** |  | x1 |  |  |
| **Figures and Graphs** |  | x2 |  |  |
| **Technical Writing Style** |  | x3 |  |  |
| **Total Score** |  | | |  |

5: Excellent 4: Good 3: Acceptable 2: Poor 1: Very Poor 0: Not attempted

Comments:

1. Reliability Analysis

The selected components of concern in this analysis are NCP1117ST33T3G LDO regulator, BNO-085 9-axis IMU, and STM32F091RCT6 microcontroller. The primary reason for such a concern is due to the high junction temperature these components exhibits during operation, as NCP1117ST33T3G is a power converter and both BNO-085 and STM32F091RCT6 is a highly complicated IC with very dense CMOS transistors.

In our use case, NCP1117ST33T3G LDO is mostly responsible for down converting the source 5V to 3.3V that would supply the rest of the PCB. The heat dissipation is around 0.153Watts as our nominal operating current reaches 90mA with 1.7V of voltage dropout. Such a high heat dissipation over a dense area could not be underestimated and therefore preliminary reliability analysis must be conducted for our design.

BNO-085 and STM32F091RCT6 on the other hand, both utilizes 32bit Cortex M0 that contributes to a higher failure rate due to the die complexity. In addition, both chips have a rather complex package form which also adds to failure rate.

Our analysis model is based off the Military Handbook MIL-HDBK-217f [1], shorthand for “the handbook”, it was determined that several key factor that contributes to the overall failure rate is:

* C1, die complexity failure, dictated by the numbers of transistors and transistor layout chosen.
* C2, package failure, dictated by the packaged method and its formfactor.
* πT, temperature factor, in which higher junction temperature of a device in concern would result in a higher failure rate.
* πE, environment factor, as the project is meant to be a mobile handheld device, its factor will be 4, a ground mobile device.
* πQ, quality factor, which depends on the set of standards each component is designed for. As all components chosen is only for commercial purposes, its factor will be 10 across all parts.
* πL, learning factor, as new immature parts induce additional failure rate as opposed to a matured device.

The handbook’s estimation of λp,failure rate in million hours, is seen as a linear relationship contributed by each of the aforementioned factor, and the model is as follows:

λp = (C1 πT + C2 πE) πQ πL

Figure 1, estimation model of λp

And the mean time to failure (MTTF), in terms of years, is given by:

MTTF = 106 / (24 \* 365 \* λp)

Figure 2, equation for MTTF

The tables shown below provide values of each factor for each perspective device in concern:

Table 1. NCP1117ST33T3G[2] LDO Parameter Analysis

|  |  |  |  |
| --- | --- | --- | --- |
| Parameter name | Description | Value | Comments |
| C1 | Die complexity failure | 0.01 | Based on the handbook [1] for device with 1~100 GaAs bipolar transistors |
| πT | Temperature factor | 5.60 | Assume specified maximum junction temperature of Tj = 150°C |
| C2 | Package failure | 0.0013 | 4 Pin Surface Mount Device |
| πE | Environment factor | 4.00 | Ground, Mobile |
| πQ | Quality factor | 10.00 | Commercial components |
| πL | Learning factor | 1.00 | Has been more than two years in production |
| λp | Failure per million hrs | 0.108 | λp = (C1 πT + C2 πE) πQ πL |
| MTTF | Mean Time to Failure | 1056.99 | Average of Approx. 1057 yrs for a device failure |

Table 2. BNO-085[3] IMU Parameter Analysis

|  |  |  |  |
| --- | --- | --- | --- |
| Parameter name | Description | Value | Comments |
| C1 | Die complexity failure | 0.56 | Based on the handbook [1] for System in a Package (SiP) that contains a 32-bit CMOS microcontroller  (ARM Cortex M0+) |
| πT | Temperature factor | 1.10 | Assume specified maximum junction temperature of Tj = 85°C |
| C2 | Package failure | 0.01 | QFN 28-Pin Hermetic Package |
| πE | Environment factor | 4.00 | Ground, Mobile |
| πQ | Quality factor | 10.00 | Commercial components |
| πL | Learning factor | 1.00 | Has been more than two years in production |
| λp | Failure per million hrs | 6.56 | λp = (C1 πT + C2 πE) πQ πL |
| MTTF | Mean Time to Failure | 17.402 | Average of Approx. 17.40 yrs for a device failure |

Table 3. STM32F091RCT6[3] Microcontroller Parameter Analysis

|  |  |  |  |
| --- | --- | --- | --- |
| Parameter name | Description | Value | Comments |
| C1 | Die complexity failure | 0.56 | Based on the handbook [1] for a 32-bit CMOS microcontroller  (ARM Cortex M0) |
| πT | Temperature factor | 2.10 | Assume specified maximum junction temperature of Tj = 125°C |
| C2 | Package failure | 0.025 | LQFP 64-Pin Hermetic Package |
| πE | Environment factor | 4.00 | Ground, Mobile |
| πQ | Quality factor | 10.00 | Commercial components |
| πL | Learning factor | 1.00 | Has been more than two years in production |
| λp | Failure per million hrs | 12.76 | λp = (C1 πT + C2 πE) πQ πL |
| MTTF | Mean Time to Failure | 8.946 | Average of Approx. 8.95 yrs for a device failure |

1.1 Reliability Summary

As seen above, the LDO are the most reliable part as it has MTTF of 1057 years, the primary reason being the simplicity of the die construction. Whereas BNO-085 and STM32F091RCT6, while similar in die complexity, has a vastly different MTTF of 17.402 and 8.946 years respectively. All due to the extra complexity in package formfactor and higher thermal junction STM32F091RCT6 exhibits.

Nonetheless, all three parts of are overall very reliable, as πT, the temperature factor uses the maximum thermal junction provided by the manufacturer rather than the realistic thermal envelope. In our mechanical design, the PCB will be open vented to ensure adequate amount of heat transfer.

1. Failure Mode, Effects, and Criticality Analysis (FMECA)

The schematics of team Metaporter will be divided into three subsections with an emphasis on electrical design. These subsystems are the power supply, microcontrollers, and the peripheral device.

* 1. Levels of Criticality

The canonical method of ranking criticality is used to differentiate the severity of each failure modes.

“High” failure mode indicates a catastrophic failure in which the board could be permanently damaged and may present harm to the user. Further assessment is required before our board can be used again. Such an failure has a very low failure rate, speculative of 10-9 or less, as appropriate measurements were considered during the design of the board development.

“Medium” failure mode could be any failures that won’t harm the user but may impose potential damage to the system. Such a damage could be mitigated by various provision. The intended failure rate is a magnitude higher than the high failure mode, but still well within a reasonable range of 10-7

“Low” failure mode is reserved for failures that are insignificant to the intended core functionality of the device but requires methods to mitigate the effect. While still very unlikely, it is intended to have a failure rate of 10-6.

3.0 Sources Cited:

[1] “Military Handbook,” Jan 1990. [Online]. Available: <https://purdue.brightspace.com/d2l/le/dropbox/599839/632179/DownloadAttachment?fid=21219302> [Accessed 11/6/2022].

[2] Onsemi, “NCV1117- A Low-Dropout Positive Fixed and Adjustable Voltage Regulators” Aug 2021. [Online]. Available: <https://www.onsemi.com/pdf/datasheet/ncp1117-d.pdf> [Accessed 11/6/2022]

[3] Hillcrestlabs, “BNO080/85/86 Data Sheet” Jan 2021. [Online]. Available: <https://www.ceva-dsp.com/wp-content/uploads/2019/10/BNO080_085-Datasheet.pdf> [Accessed 11/6/2022]

[4] ST Microelectronics, “Mainstream Arm Cortex-M0 Access line MCU with 256Kbytes of Flash memory, 48Mhz CPU, CAN and CEC functions” Nov 2022. [Online]. Available: <https://www.st.com/en/microcontrollers-microprocessors/stm32f091rc.html> [Accessed 11/6/2022]

Appendix A: Schematic Functional Blocks

Subsystem A: Power circuitry

Diagram, schematic

Description automatically generated

Figure 3: Power circuit during operational mode

A picture containing text

Description automatically generated Diagram, schematic

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Figure 4: Power source during normal mode Figure 5: Power source during debugging mode

Subsystem B: Microcontroller

Timeline

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Figure 6: Microcontroller Decoupling Capacitor Layout

Calendar

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Figure 7: Microcontroller Boot Pin configuration

Subsystem C: Peripheral Device

Calendar

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Figure 8: Keypad Connector Figure 9: SPI Display Connector

A picture containing diagram

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Figure 10: UART Connector Figure 11: I2C IMU Connector

Diagram, schematic

Description automatically generated

Figure 12: Alternative On-board IMU LayoutAppendix B: FMECA Worksheet

Subsystem A: Power Supply

|  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- |
| **Failure No.** | **Failure Mode** | **Possible Causes** | **Failure Effects** | **Method of Detection** | **Criticality** | **Remarks** |
| A1 | Reverse Current towards to source power | Diode shorts or failure, along with debug power and normal power conflict | Would trigger over-surge protection on the Nano that hard resets the system | Observation | High | May damage debugging USB port as well |
| A2 | Inconsistent 3.3V voltage | Capacitor failure or LDO degradation | Board may experience erratic boot up behavior | Inspection by measuring 3.3V vias | Medium | May damage peripheral components |
| A3 | 5V voltage saturating 3.3V power rail | LDO failure or short circuit | Board will not work and could fry the microcontroller | Inspection by measuring 3.3V vias | High | May damage peripheral components |
| A4 | Excessive Current (>150mA) from the source power | Diode shorts or failure | Microcontroller’s VDDIO will be destroyed and thus making the board unusable | Observation  (Signs of smoke…) | High | Most likely would fry up diode first which would make an open circuit |
| A5 | Source voltage below 5V | Jetson Nano degradation or ST-LINK degradation | Board may or may not boot with erroneous behaviors | Inspection by measuring 5V input pin | Low | May behave completely normal as LDO only exerts 1.3V of dropout voltage |

Subsystem B: Microcontroller

|  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- |
| **Failure No.** | **Failure Mode** | **Possible Causes** | **Failure Effects** | **Method of Detection** | **Criticality** | **Remarks** |
| B1 | ESD current surge | Inappropriate handling of the device | Could destroy certain functionalities of the MCU | Observation | High | May deem VDDIO completely unusable |
| B2 | Floating Boot Pin | Corrosion of boot pin wire or R4 failure | Board may experience occasional shutdown | Inspection by measuring the boot pin to ground | High | Could be concealed and hard to detect |
| B3 | Decoupling cap failure | LDO failure or short circuit | Board will experience random dips or spikes in voltage | Inspection by measuring the 3.3V power rail | High |  |
| B4 | No data could be transmitted from MCU | GPIO failure, pin corrosion, software | MCU is not working as intended | Observation | Low | MCU currently has a couple reserved pins in case of such an event |

Subsystem C: Peripheral Devices

|  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- |
| **Failure No.** | **Failure Mode** | **Possible Causes** | **Failure Effects** | **Method of Detection** | **Criticality** | **Remarks** |
| C1 | Unsecure contact | Loose connection between the header pins and the peripheral device | May deem some peripherals unusable | Observation | Low |  |
| C2 | Polarized connection | Inverted connections of the intended peripherals | May deem some peripherals unusable | Observation | Low | Silkscreens and designs such as segregating the ground, power pins are implemented to prevent any serious incident |
| C3 | ESD shock | ESD resistor failure or improper handling of the device | Current spike propagates to the microcontroller | Inspection by measuring between the data vias | Medium | Very unlikely as additional impedance + ESD resistor are employed. |
| C4 | No data could be read | Pin corrosion, GPIO failure, software | Device might not work as intended | Inspection by measuring between the data vias | Low | Extra reserved pins are provided to mitigate such an impact. |
| C5 | IMU unresponsive | SCL/SDA line failure, IMU chip malfunction | IMU device no longer works | erratic behavior exhibits by the IMU measurement | Medium |  |