Fmax Summary report for lab3
Mon Sep 19 11:19:22 2022
Quartus Prime Version 20.1.1 Build 720 11/11/2020 Patches 1.02i SJ Lite Edition

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; Legal Notice ;

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; Slow 1100mV 85C Model Fmax Summary   ;
+-----------+-----------------+--------------+------+
; Fmax   ; Restricted Fmax ; Clock Name   ; Note ;
+-----------+-----------------+--------------+------+
; 75.15 MHz ; 75.15 MHz   ; actual_clock ;   ;
+-----------+-----------------+--------------+------+
This panel reports FMAX for every clock in the design, regardless of the user-specified clock periods. FMAX is only computed for paths where the source and destination registers or ports are driven by the same clock. Paths of different clocks, including generated clocks, are ignored. For paths between a clock and its inversion, FMAX is computed as if the rising and falling edges are scaled along with FMAX, such that the duty cycle (in terms of a percentage) is maintained. Altera recommends that you always use clock constraints and other slack reports for sign-off analysis.