

PROJECT – 2A

EEE 234

Project 2A

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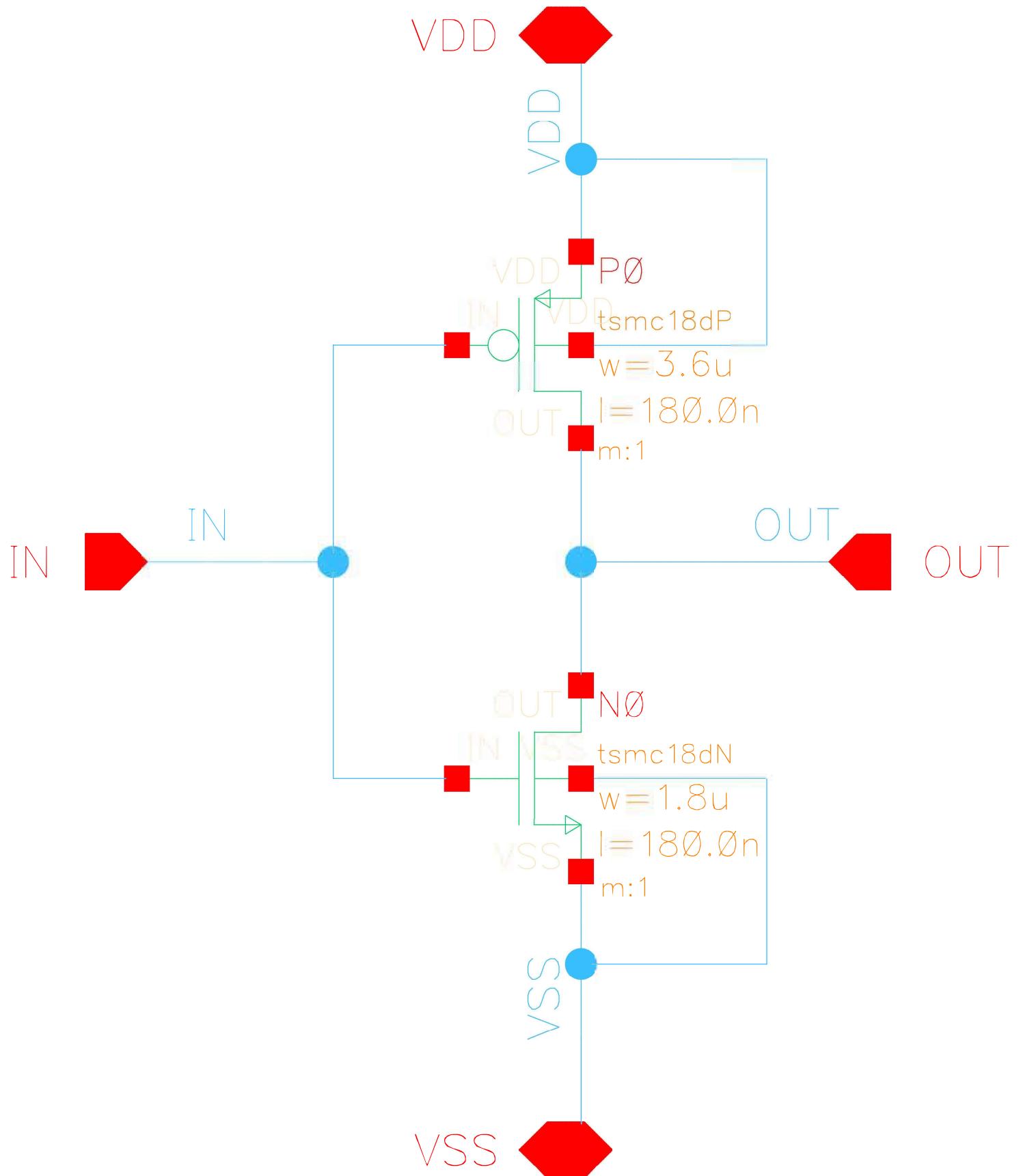
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Inverter

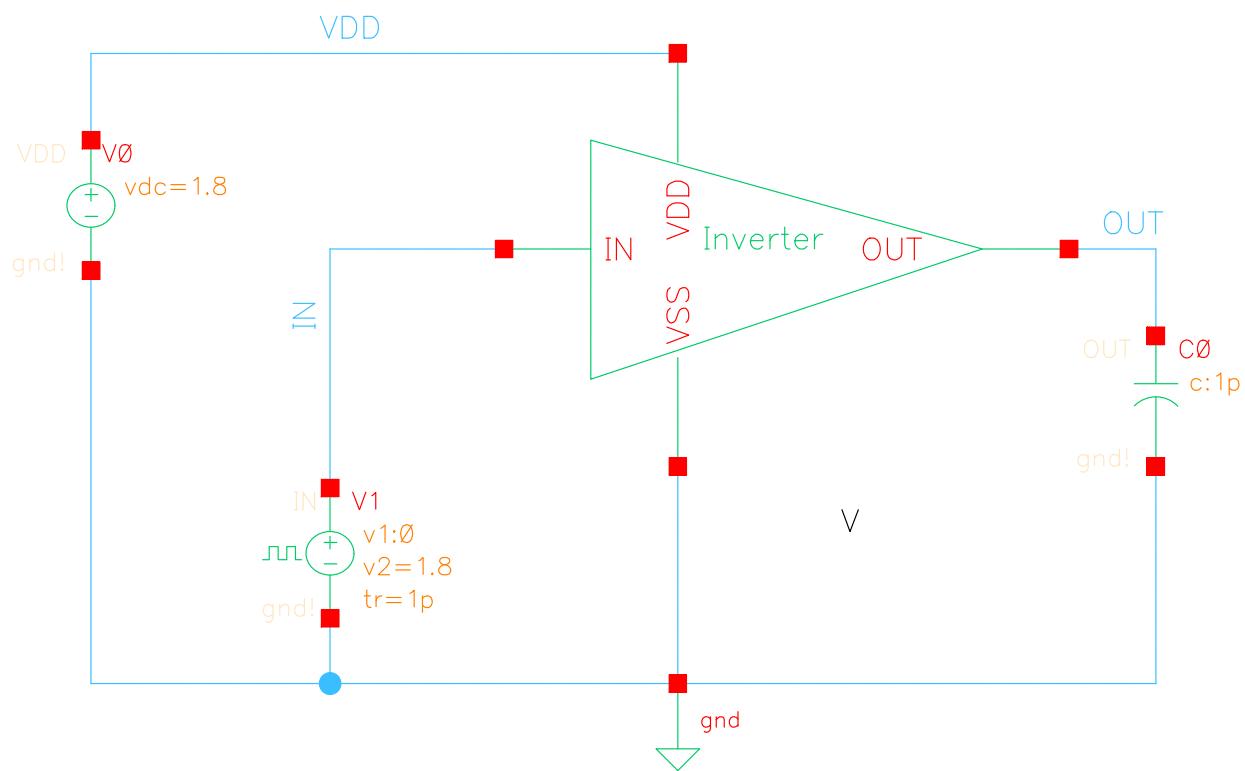
$(W/L)_n = 1.8/0.18$

$(W/L)_p = 3.6/0.18$

Schematic (Inverter)



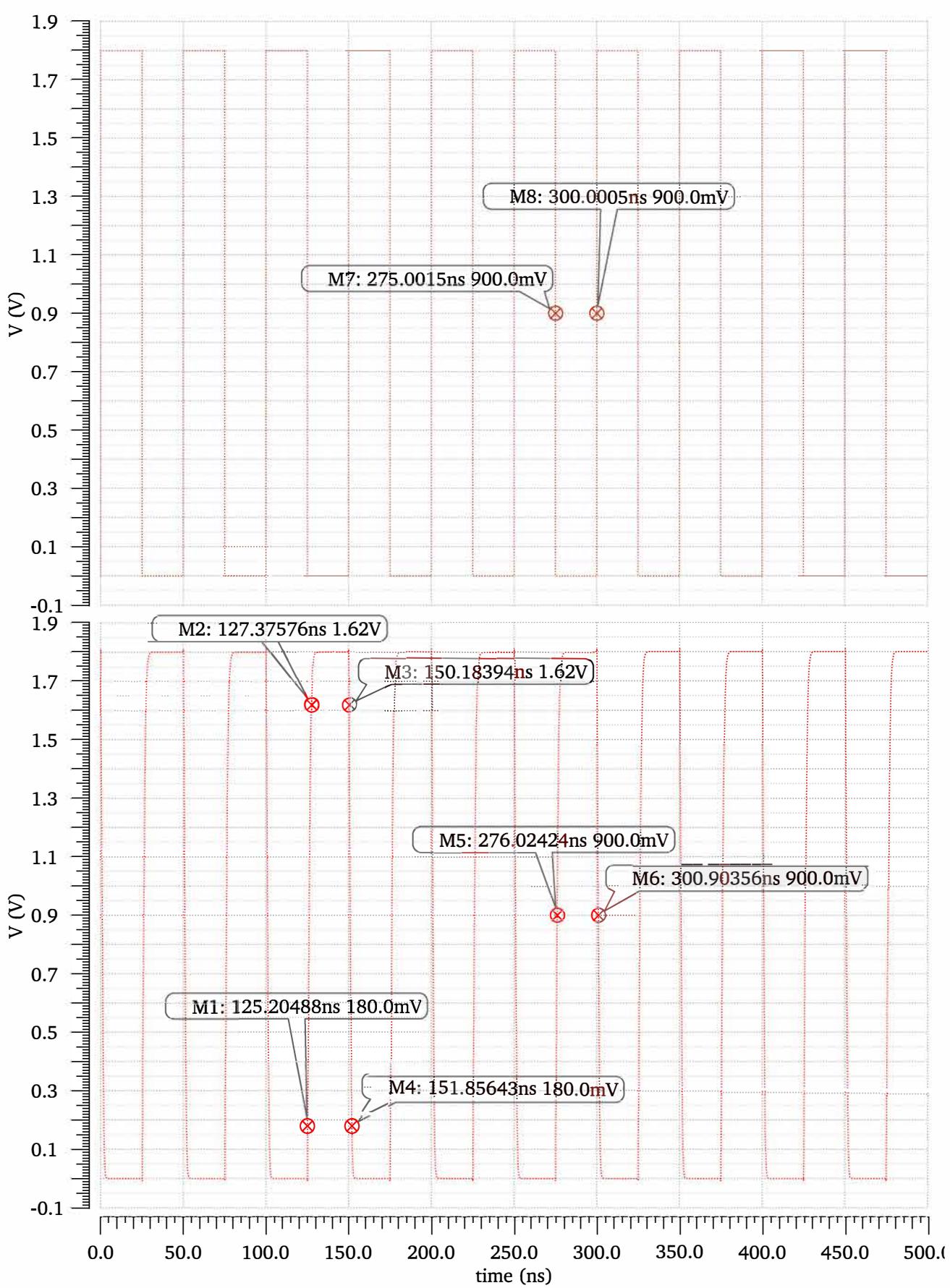
Testbench (Inverter)

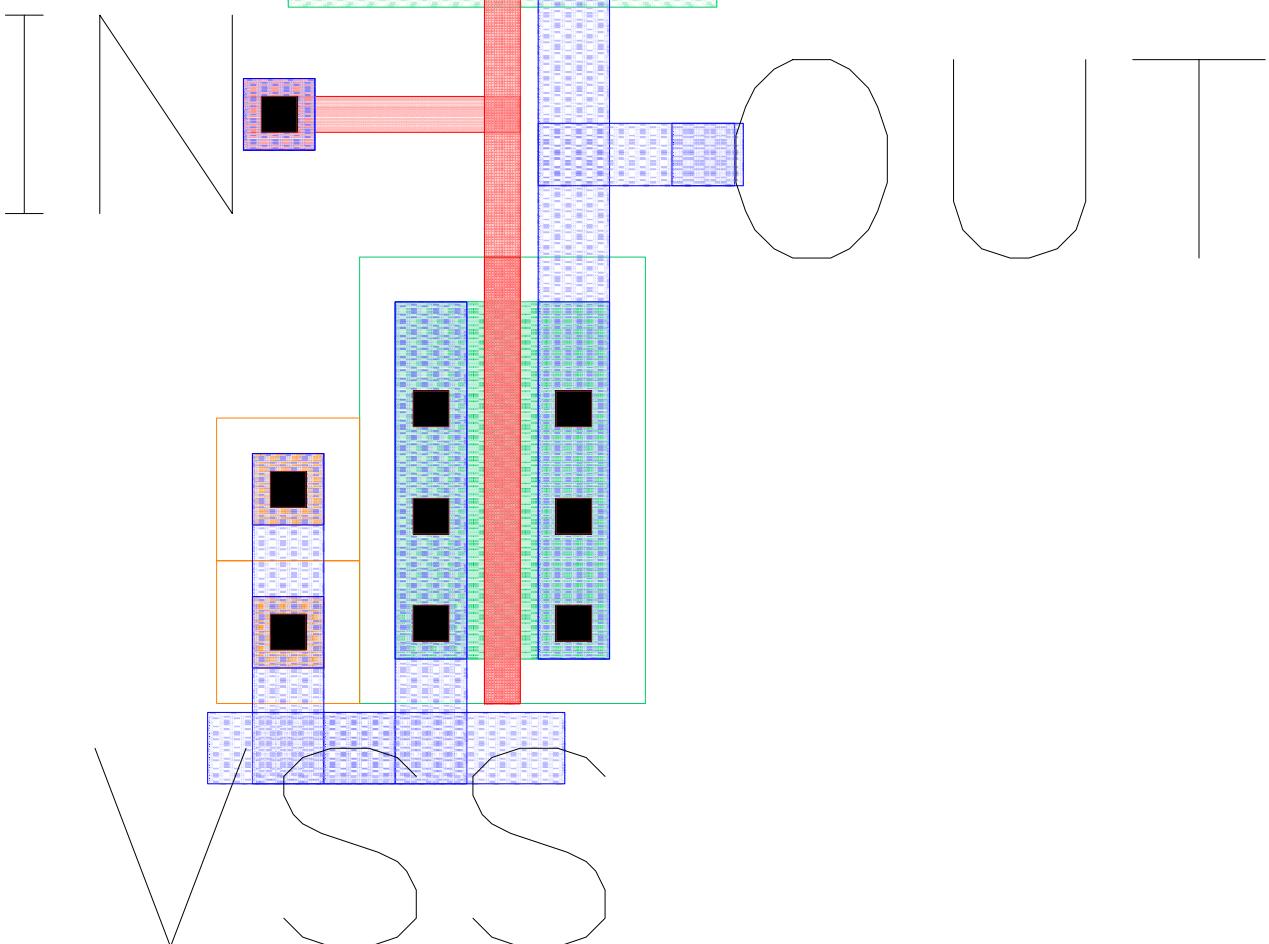
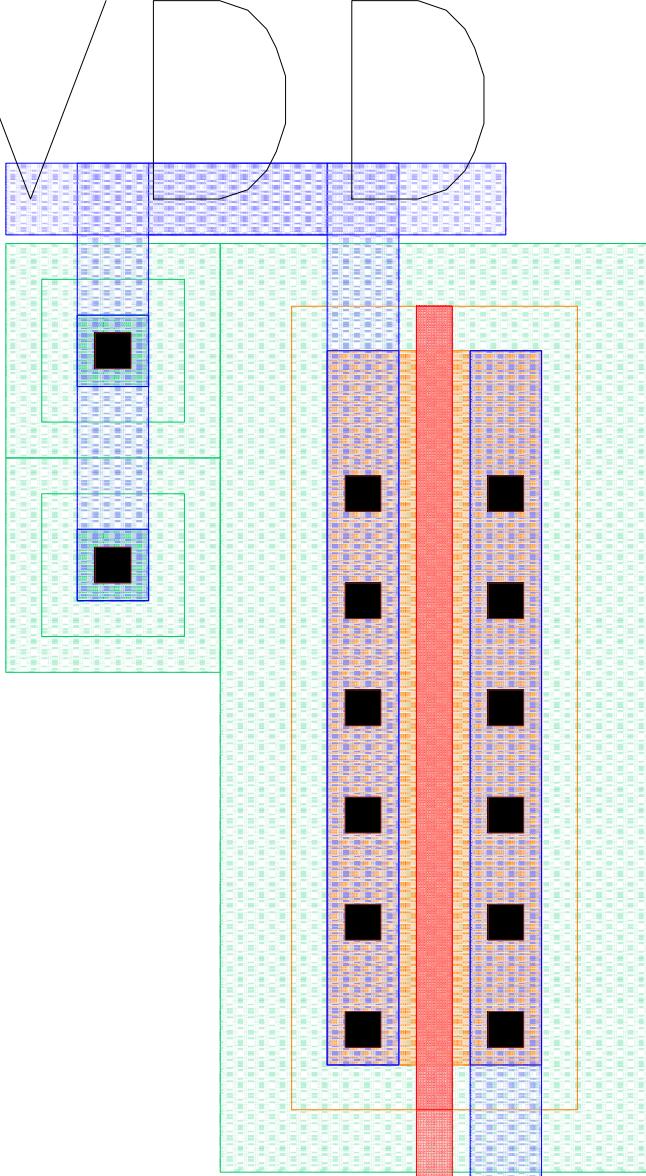


Transient Response**Inverter Waveform**

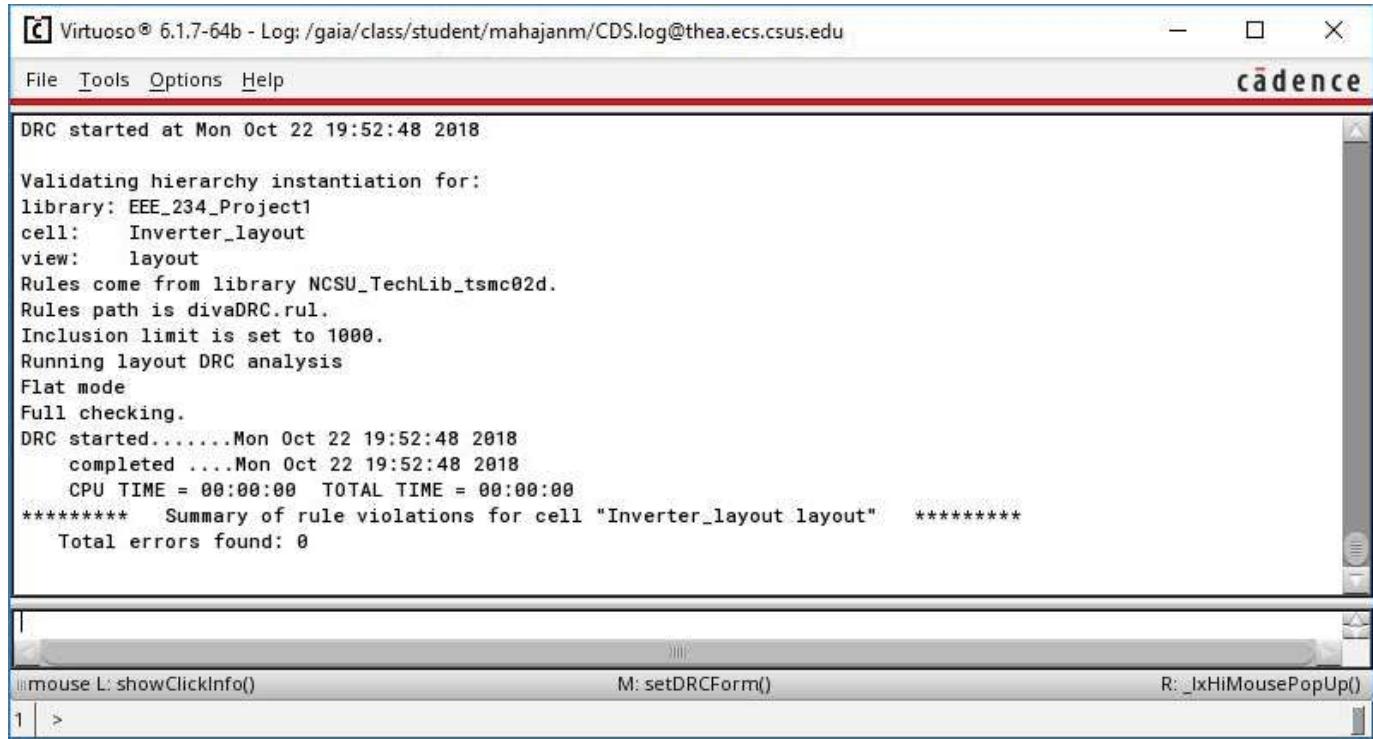
Sun Oct 7 20:43:09 2018

| Name | Vis |
|------|-----|
| /IN | |





DRC (Inverter)



Virtuoso® 6.1.7-64b - Log: /gaia/class/student/mahajanm/CDS.log@thea.ecs.csus.edu

File Tools Options Help

cadence

```
DRC started at Mon Oct 22 19:52:48 2018

Validating hierarchy instantiation for:
library: EEE_234_Project1
cell: Inverter_layout
view: layout
Rules come from library NCSU_TechLib_tsmc02d.
Rules path is divaDRC.rul.
Inclusion limit is set to 1000.
Running layout DRC analysis
Flat mode
Full checking.

DRC started.....Mon Oct 22 19:52:48 2018
completed ....Mon Oct 22 19:52:48 2018
CPU TIME = 00:00:00 TOTAL TIME = 00:00:00
***** Summary of rule violations for cell "Inverter_layout layout" *****
Total errors found: 0
```

mouse L: showClickInfo() M: setDRCForm() R: _lxHiMousePopUp()

1 | >

LVS (INVERTER) :

Running simulation in directory: "/gaia/class/student/mahajanm/EEE_234_Project1/LVS".

Begin netlist: Oct 22 19:46:59 2018

```
view name list = ("auLvs" "extracted" "schematic")
stop name list = ("auLvs")
library name = "EEE_234_Project1"
cell name = "Inverter_layout"
view name = "extracted"
globals lib = "basic"
```

Running Artist Flat Netlisting ...

End netlist: Oct 22 19:46:59 2018

Begin netlist: Oct 22 19:46:59 2018

```
view name list = ("auLvs" "schematic")
stop name list = ("auLvs")
library name = "EEE_234_Project1"
cell name = "Inverter"
view name = "schematic"
globals lib = "basic"
```

Running Artist Flat Netlisting ...

End netlist: Oct 22 19:46:59 2018

Moving original netlist to extNetlist

Removing parasitic components from netlist

```
presistors removed: 0
pcapacitors removed: 0
pinductors removed: 0
pdiodes removed: 0
trans lines removed: 0
4 nodes merged into 4 nodes
```

Running netlist comparison program: LVS

Begin comparison: Oct 22 19:46:59 2018

@(#)CDS: LVS version 6.1.7-64b 09/27/2016 19:41 (sjfhw305) \$

The net-lists match.

layout schematic

instances

| | | |
|-------------|---|---|
| un-matched | 0 | 0 |
| rewired | 0 | 0 |
| size errors | 0 | 0 |
| pruned | 0 | 0 |
| active | 2 | 2 |
| total | 2 | 2 |

nets

| | | |
|------------|---|---|
| un-matched | 0 | 0 |
| merged | 0 | 0 |
| pruned | 0 | 0 |
| active | 4 | 4 |
| total | 4 | 4 |

terminals

| | | |
|----------------|---|---|
| un-matched | 0 | 0 |
| matched but | | |
| different type | 1 | 1 |
| total | 4 | 4 |

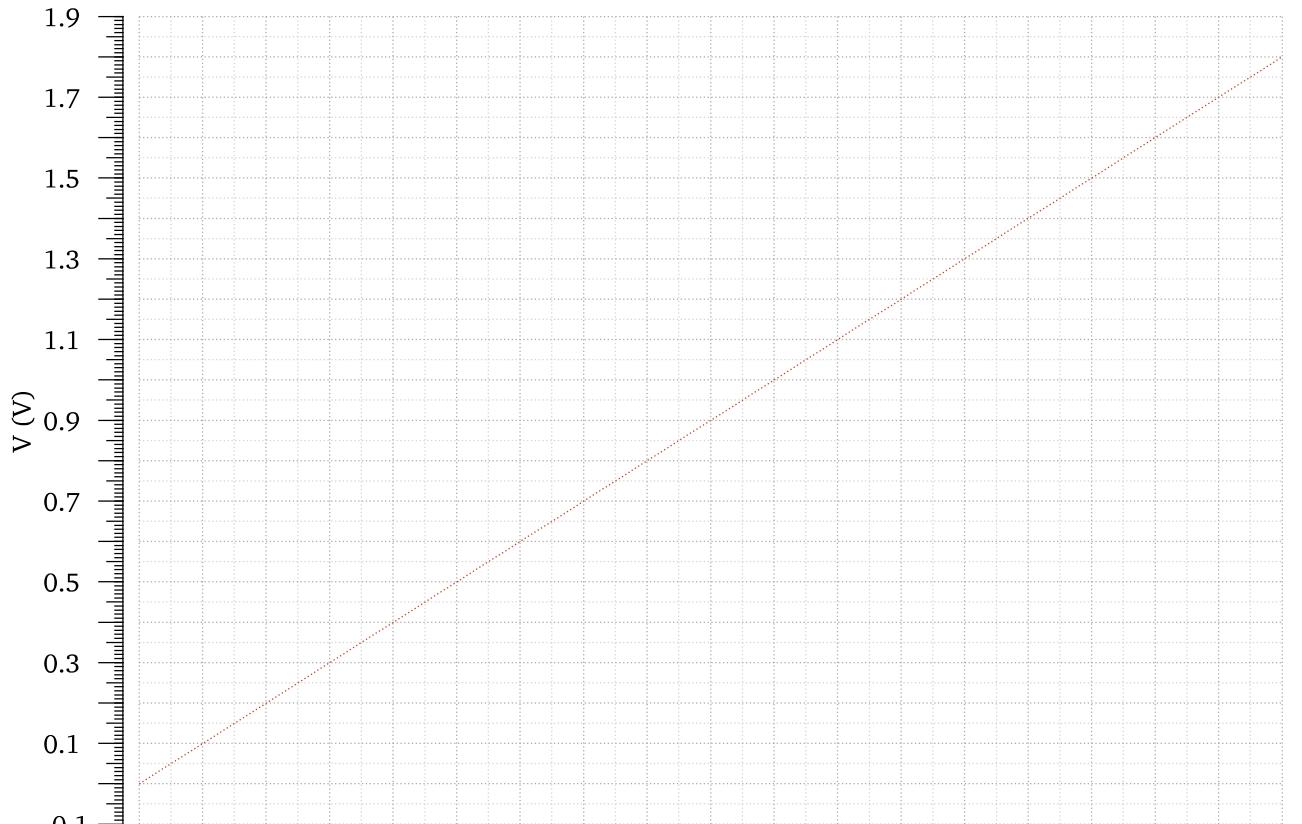
End comparison: Oct 22 19:46:59 2018

Comparison program completed successfully.

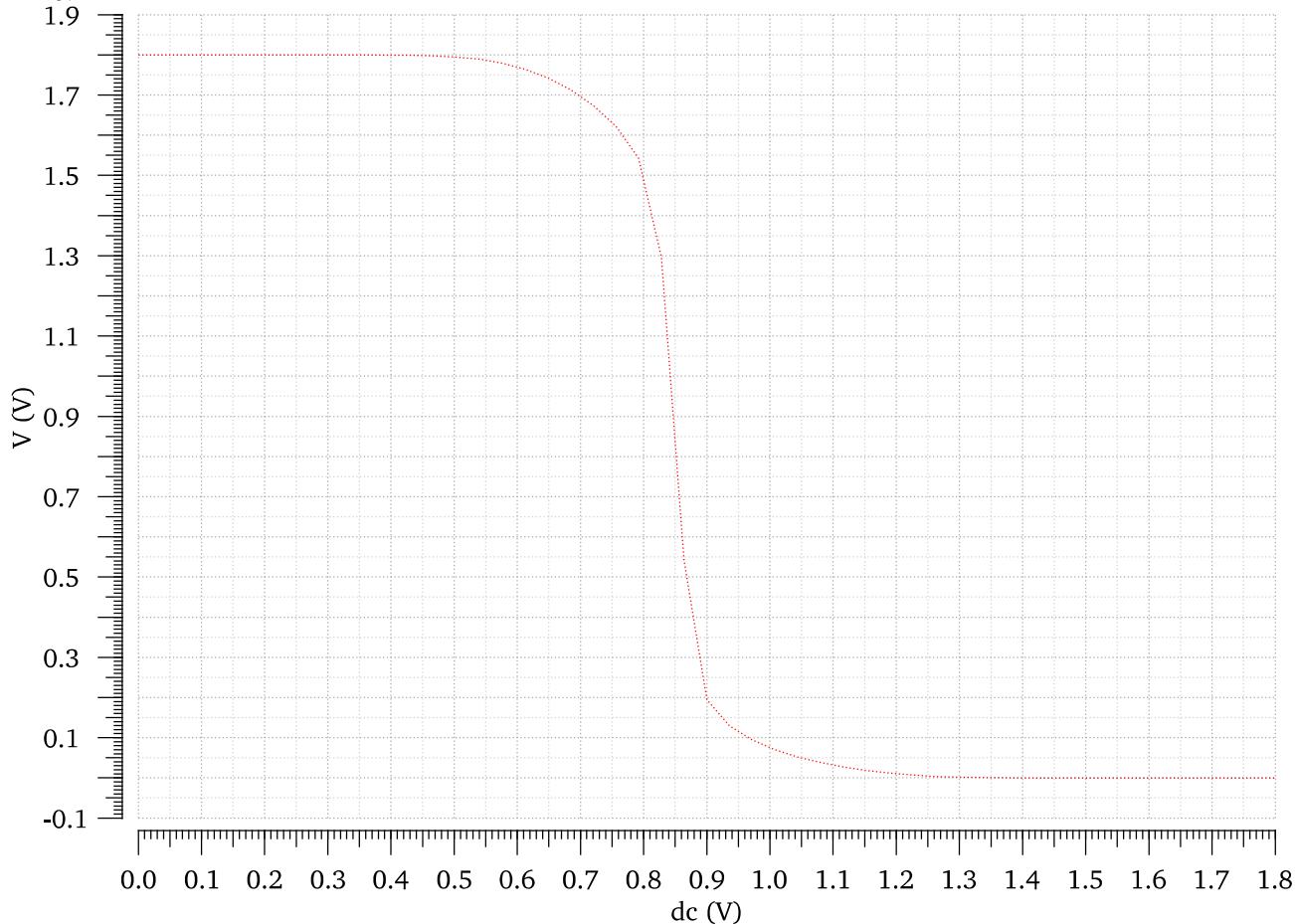
DC Response**Inverter DC Waveform****Thu Oct 25 15:53:09 2018**

Name Vis

■ /IN



■ /OUT

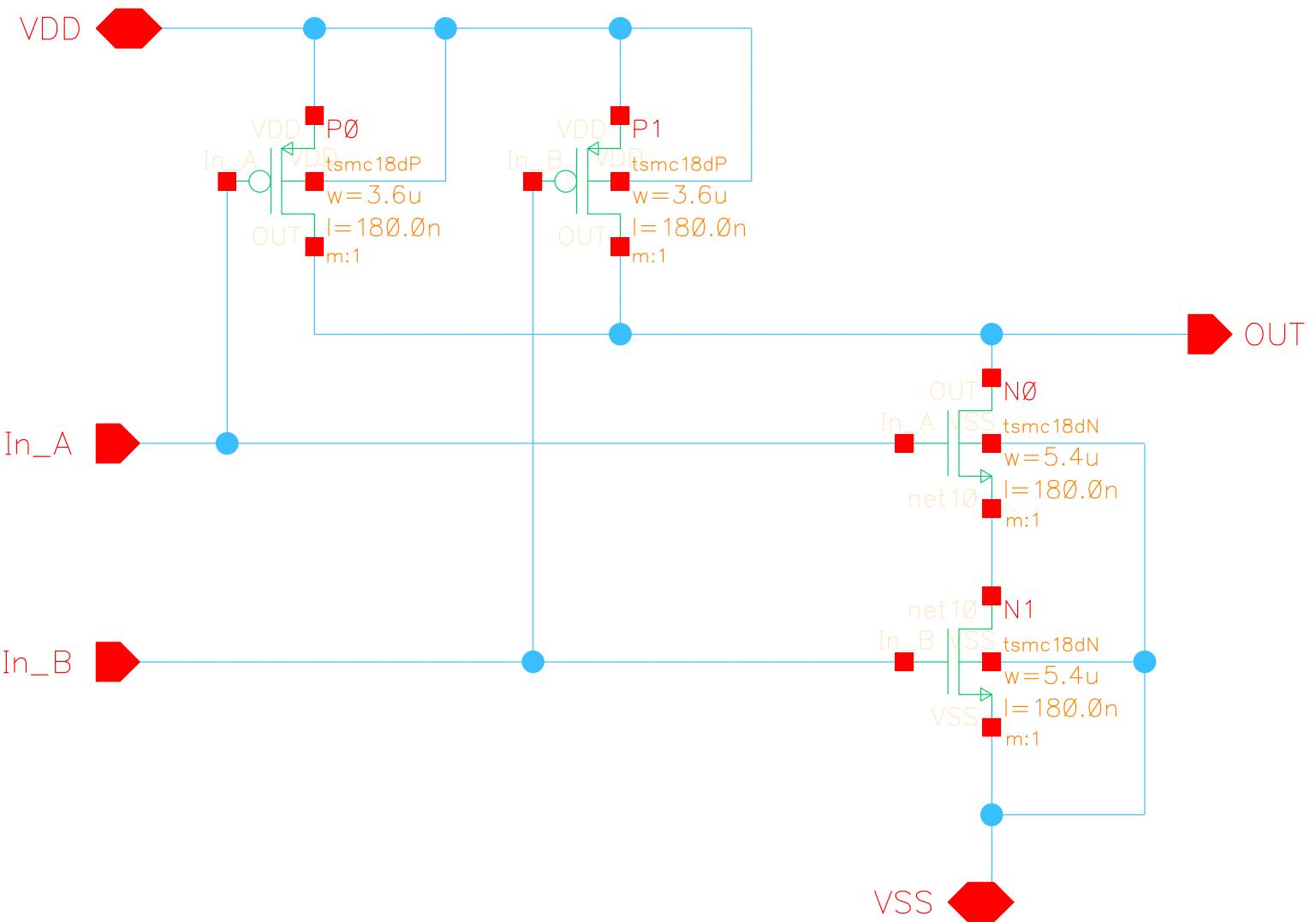


2-input NAND gate

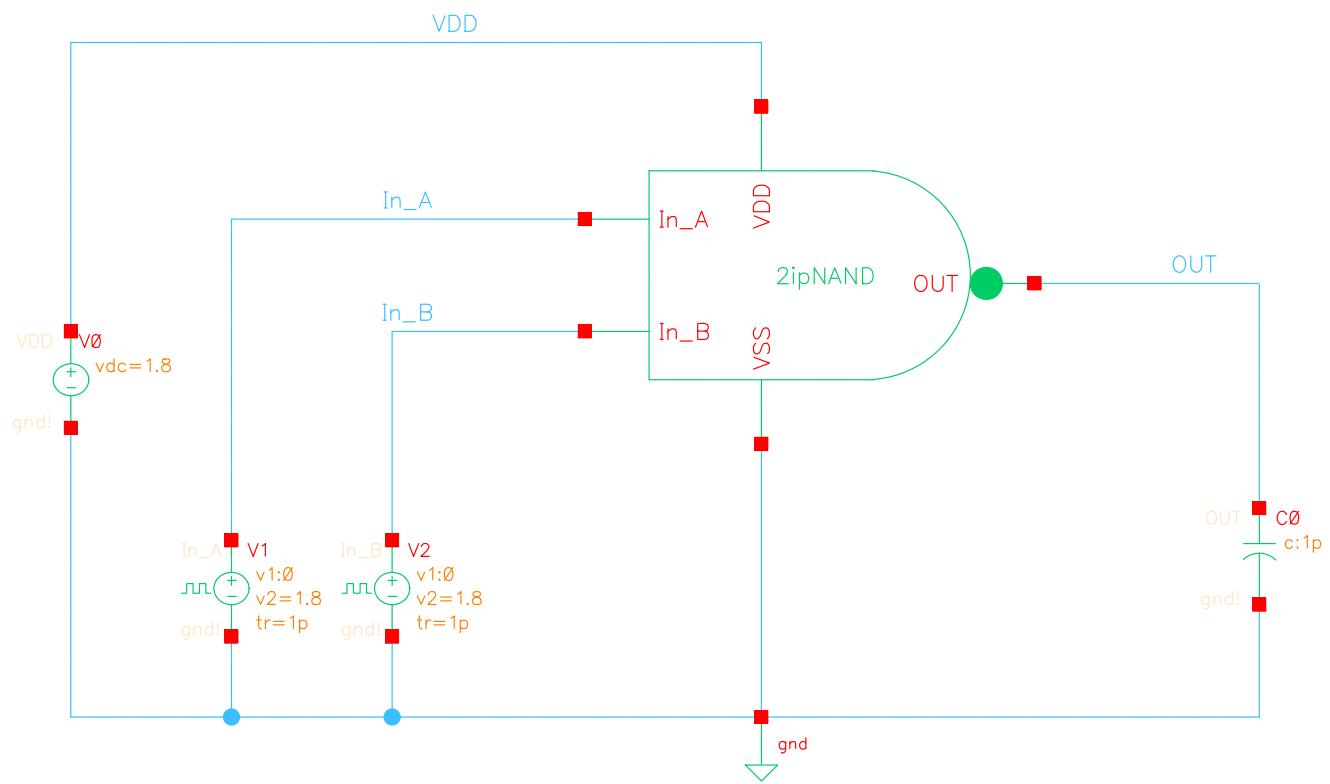
(W/L)_n = 5.4/0.18

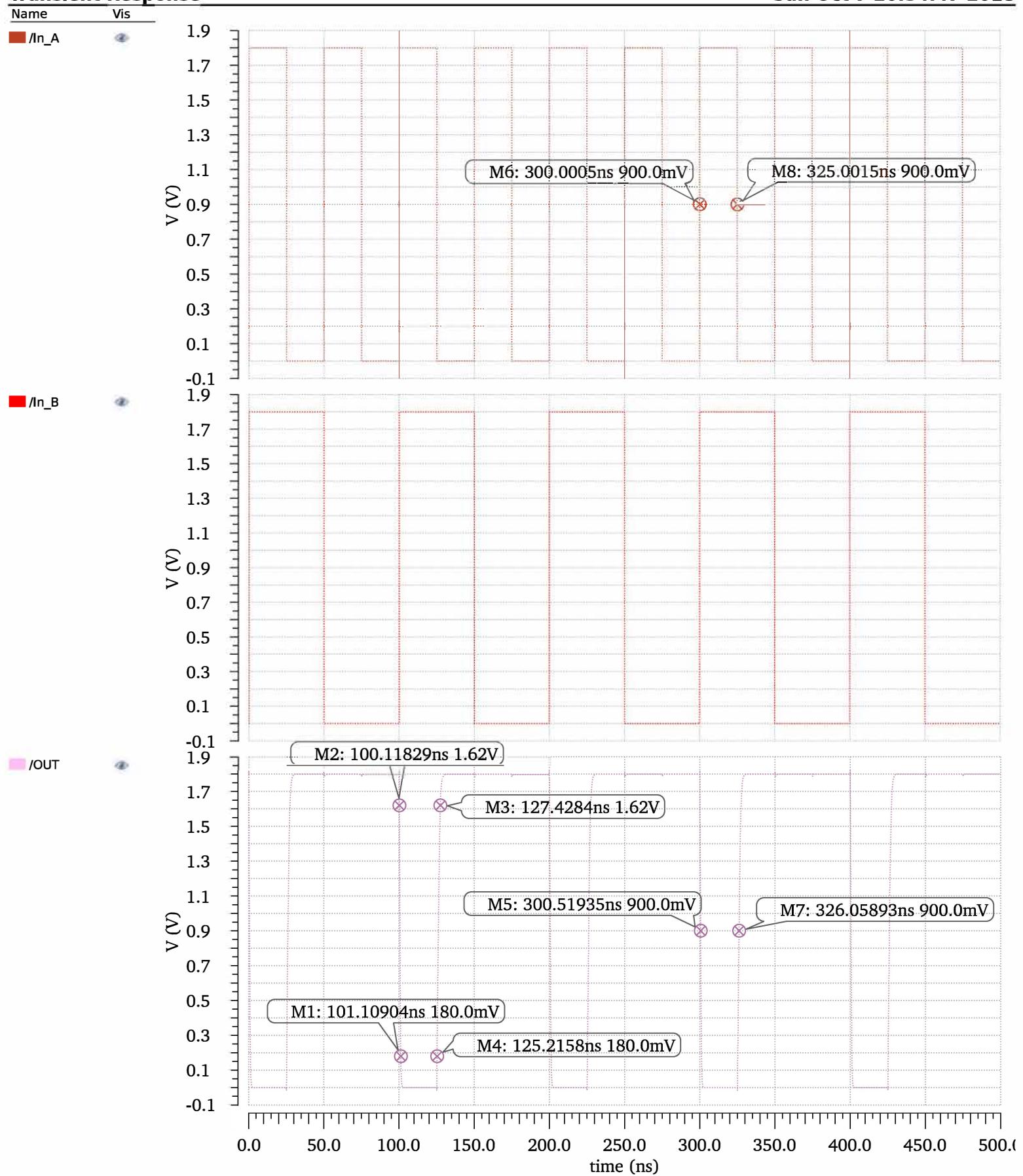
(W/L)_p = 3.6/0.18

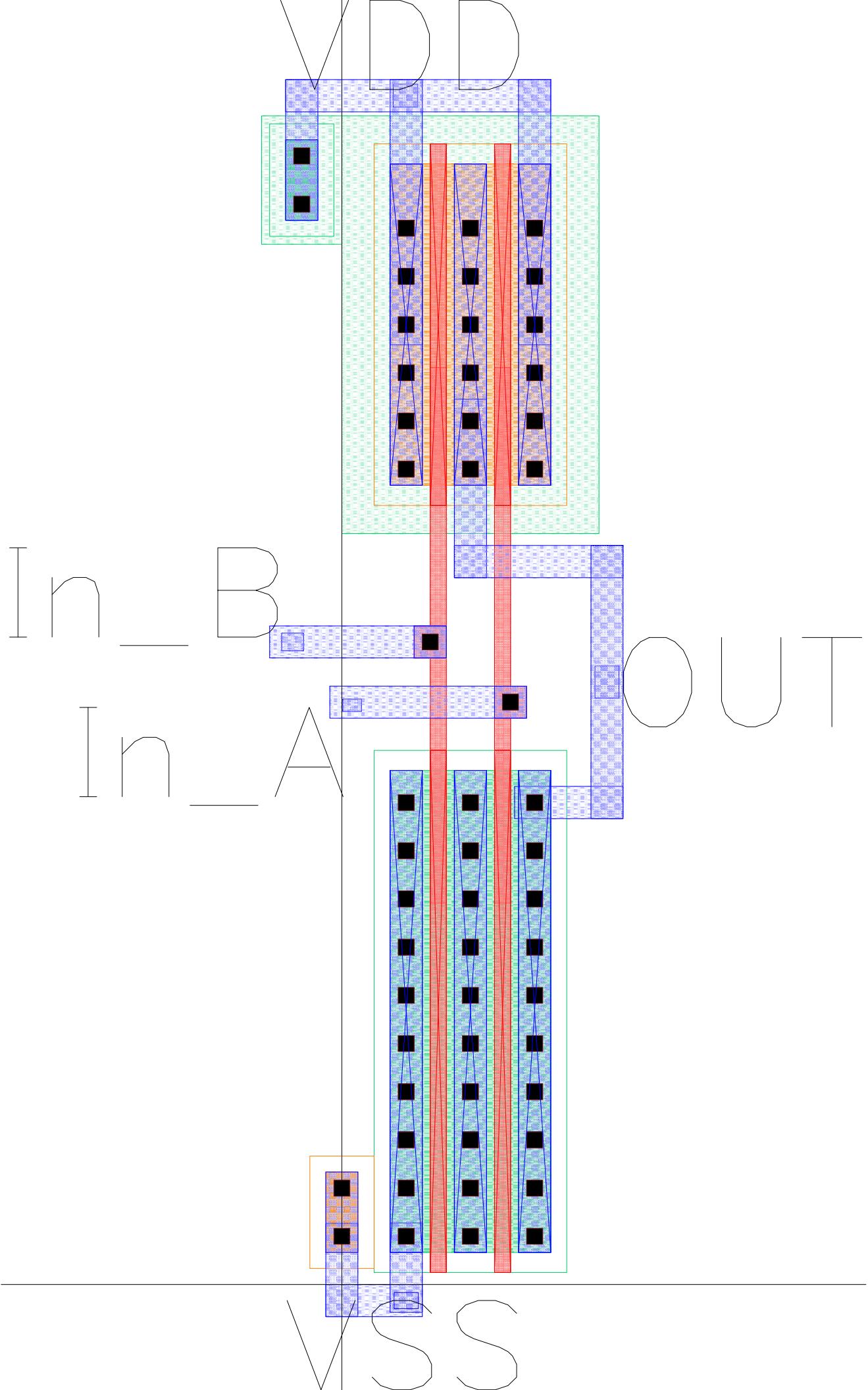
Schematic (2-input NAND gate)



Tesbench (2-input NAND gate)



Transient Response**2 Input NAND Waveform****Sun Oct 7 20:34:47 2018**



DRC (2-input NAND gate)

Virtuoso® 6.1.7-64b - Log: /gaia/class/student/mahajanm/CDS.log.1@thea.ecs.csus.edu

File Tools Options Help

DRC started at Wed Oct 24 18:26:52 2018

Validating hierarchy instantiation for:
library: EEE_234_Project1
cell: NAND2_Layout
view: layout
Rules come from library NCSU_TechLib_tsmc02d.
Rules path is divaDRC.rul.
Inclusion limit is set to 1000.
Running layout DRC analysis
Flat mode
Full checking.
DRC started.....Wed Oct 24 18:26:52 2018
completedWed Oct 24 18:26:52 2018
CPU TIME = 00:00:00 TOTAL TIME = 00:00:00
***** Summary of rule violations for cell "NAND2_Layout layout" *****
Total errors found: 0

mouse L: showClickInfo()
M: setDRCForm()
R: _IxHiMousePopUp()

```
@(#)$CDS: LVS version 6.1.7-64b 09/27/2016 19:41 (sjfhw305) $
```

Command line: /software/cadence/install/IC617/tools.lnx86/dfl/bin/64bit/LVS -dir
/gaia/class/student/mahajanm/EEE_234_Project1/LVS -l -s -t
/gaia/class/student/mahajanm/EEE_234_Project1/LVS/layout
/gaia/class/student/mahajanm/EEE_234_Project1/LVS/schematic

Like matching is enabled.

Net swapping is enabled.

Using terminal names as correspondence points.

Net-list summary for /gaia/class/student/mahajanm/EEE_234_Project1/LVS/layout/netlist

| count | |
|-------|-----------|
| 7 | nets |
| 5 | terminals |
| 3 | pmos |
| 3 | nmos |

Net-list summary for /gaia/class/student/mahajanm/EEE_234_Project1/LVS/schematic/netlist

| count | |
|-------|-----------|
| 7 | nets |
| 5 | terminals |
| 3 | pmos |
| 3 | nmos |

Terminal correspondence points

| | | |
|----|----|-----|
| N5 | N4 | IN1 |
| N4 | N5 | IN2 |
| N3 | N3 | OUT |
| N6 | N2 | VDD |

N2 N1 VSS

Devices in the netlist but not in the rules:

pmos nmox

The net-lists match.

layout schematic

instances

| | | |
|-------------|---|---|
| un-matched | 0 | 0 |
| rewired | 0 | 0 |
| size errors | 0 | 0 |
| pruned | 0 | 0 |
| active | 6 | 6 |
| total | 6 | 6 |

nets

| | | |
|------------|---|---|
| un-matched | 0 | 0 |
| merged | 0 | 0 |
| pruned | 0 | 0 |
| active | 7 | 7 |
| total | 7 | 7 |

terminals

| | | |
|-------------------------------|---|---|
| un-matched | 0 | 0 |
| matched but different type | 0 | 0 |
| total | 5 | 5 |

Probe files from /gaia/class/student/mahajanm/EEE_234_Project1/LVS/schematic

devbad.out:

netbad.out:

mergenet.out:

termbad.out:

prunenet.out:

prunedev.out:

audit.out:

Probe files from /gaia/class/student/mahajanm/EEE_234_Project1/LVS/layout

devbad.out:

netbad.out:

mergenet.out:

termbad.out:

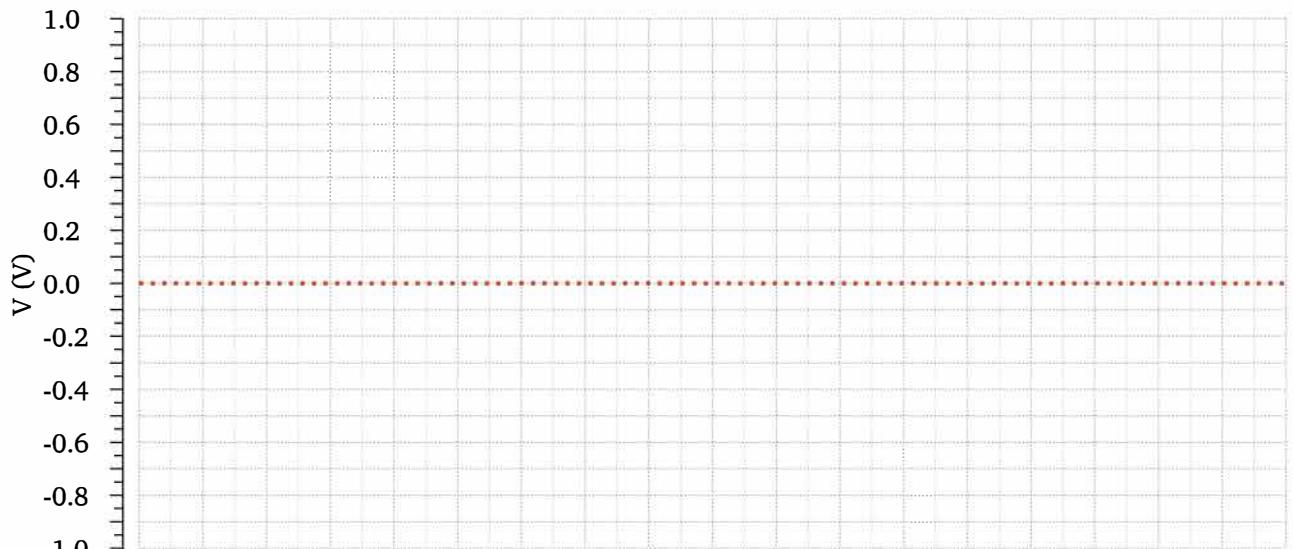
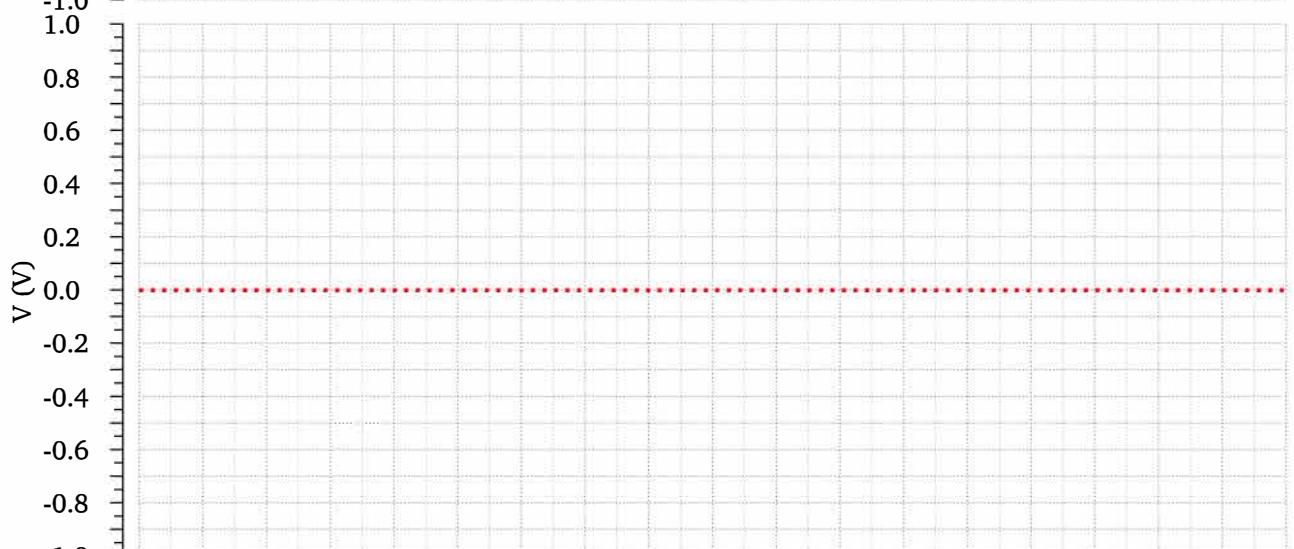
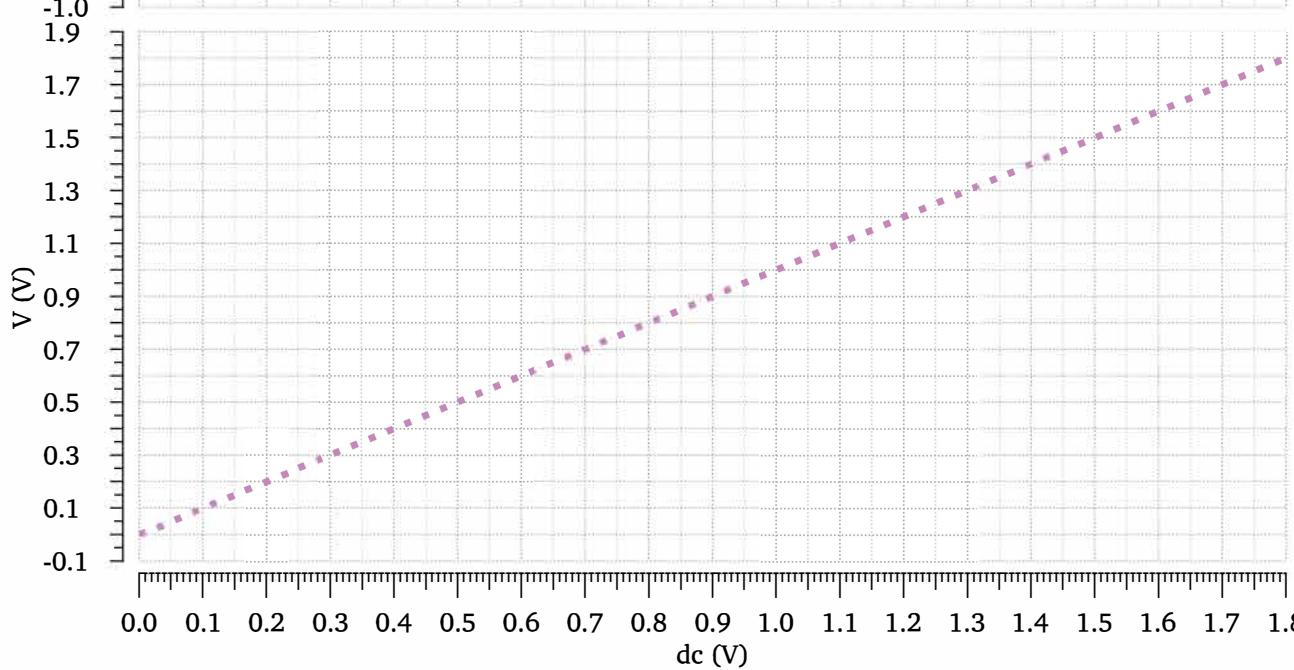
prunenet.out:

prunedev.out:

audit.out:

DC Response**2 Input NAND DC Waveform****Wed Oct 24 18:41:04 2018**

| Name | Vis |
|------|-----|
|------|-----|

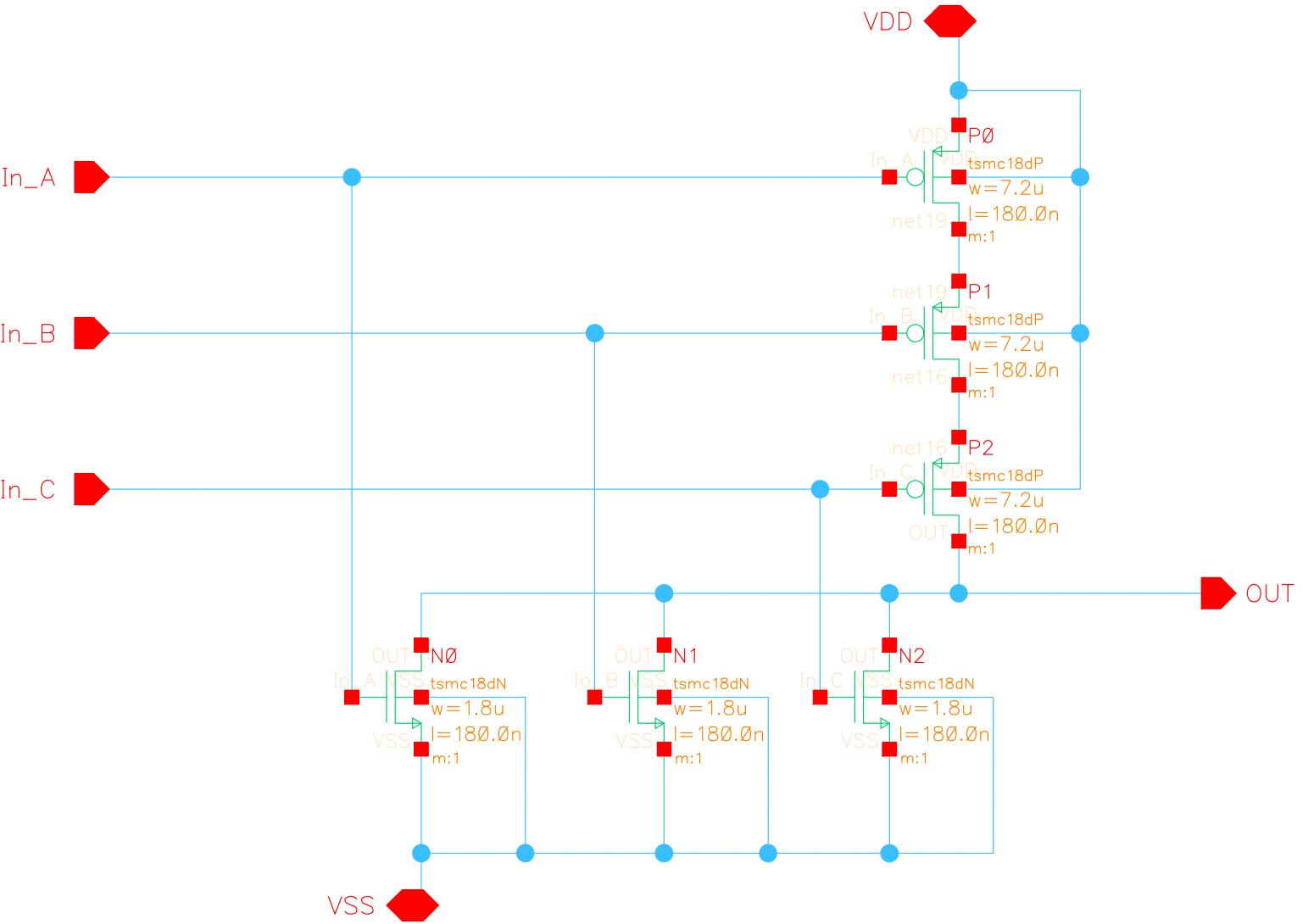
■ /In_A■ /In_B■ /OUT

3-input NOR gate

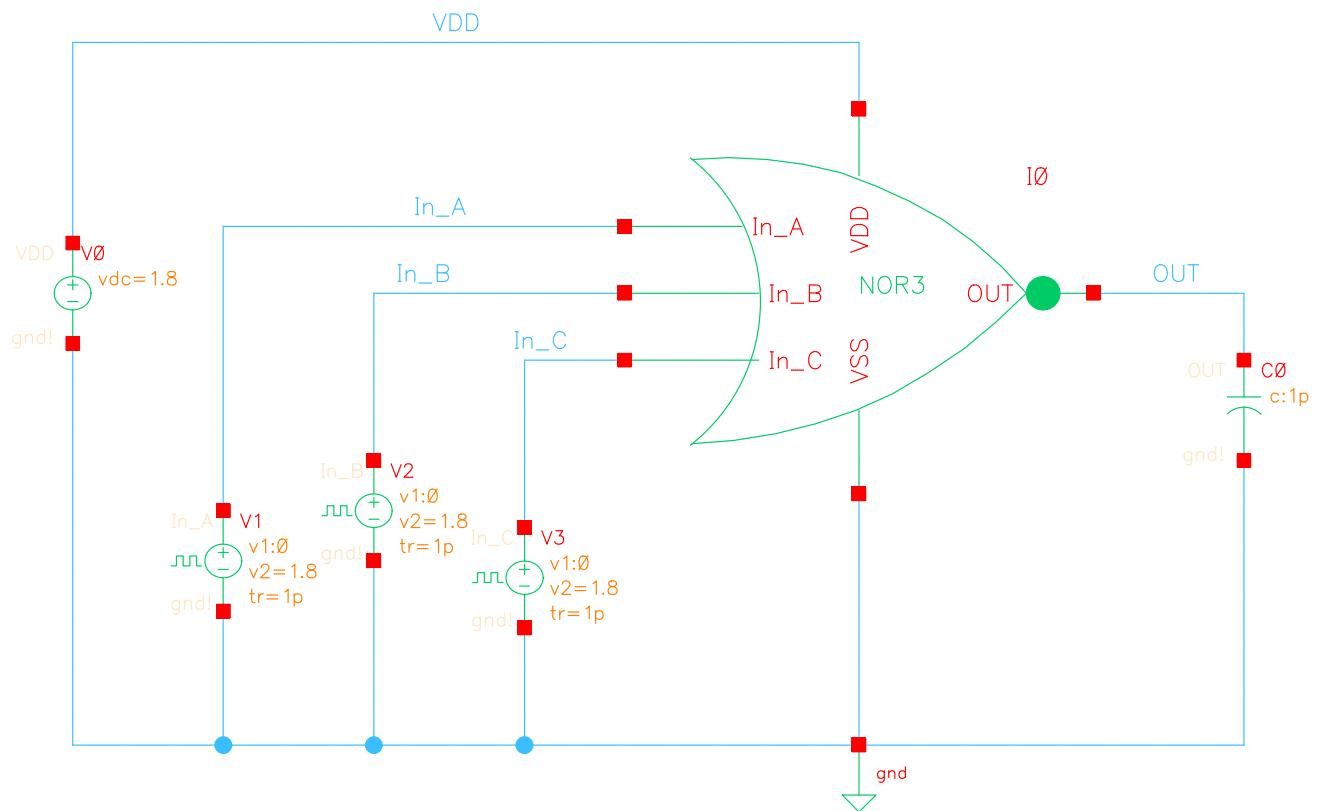
(W/L)_n = 1.8/0.18

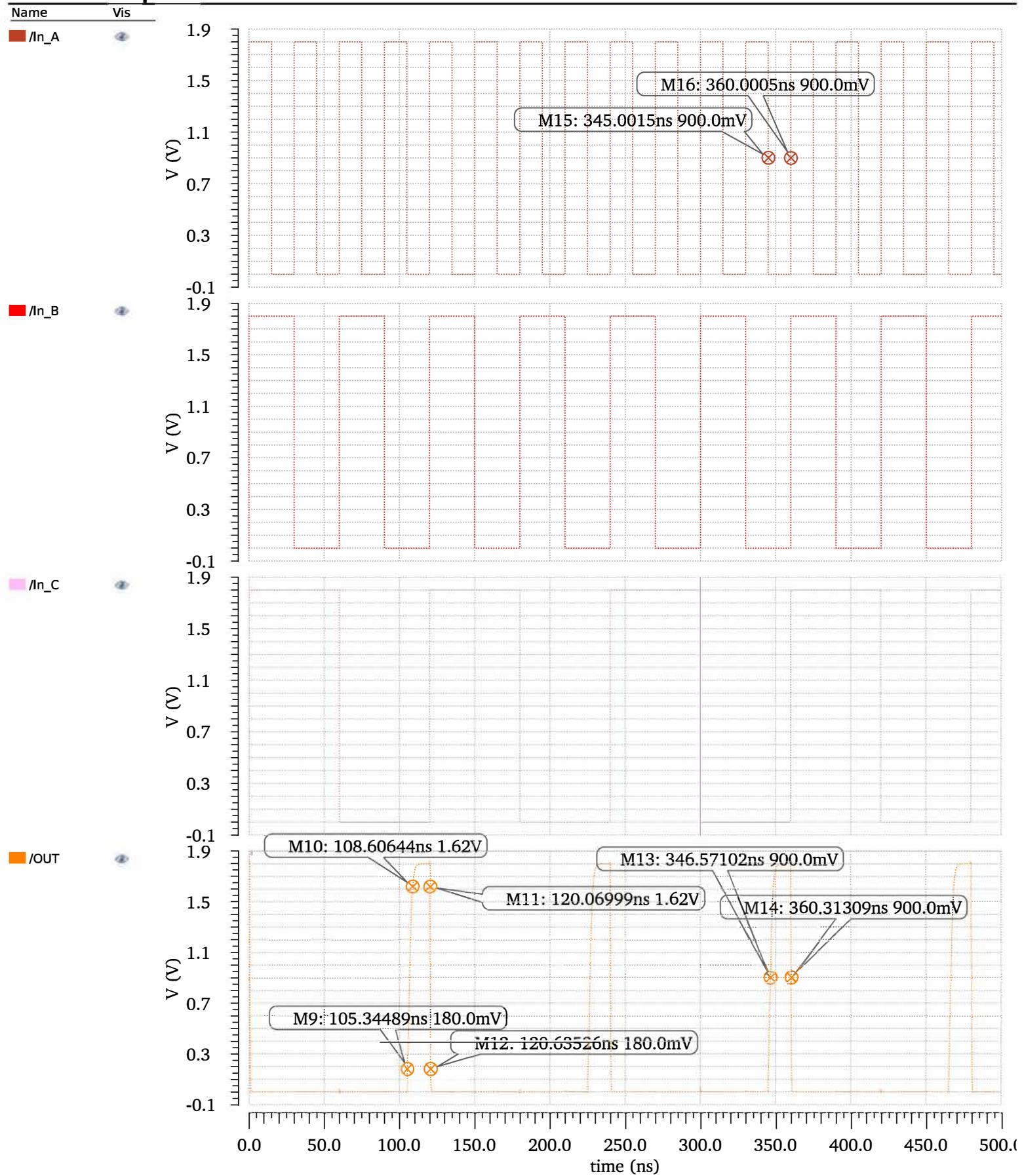
(W/L)_p = 7.2/0.18

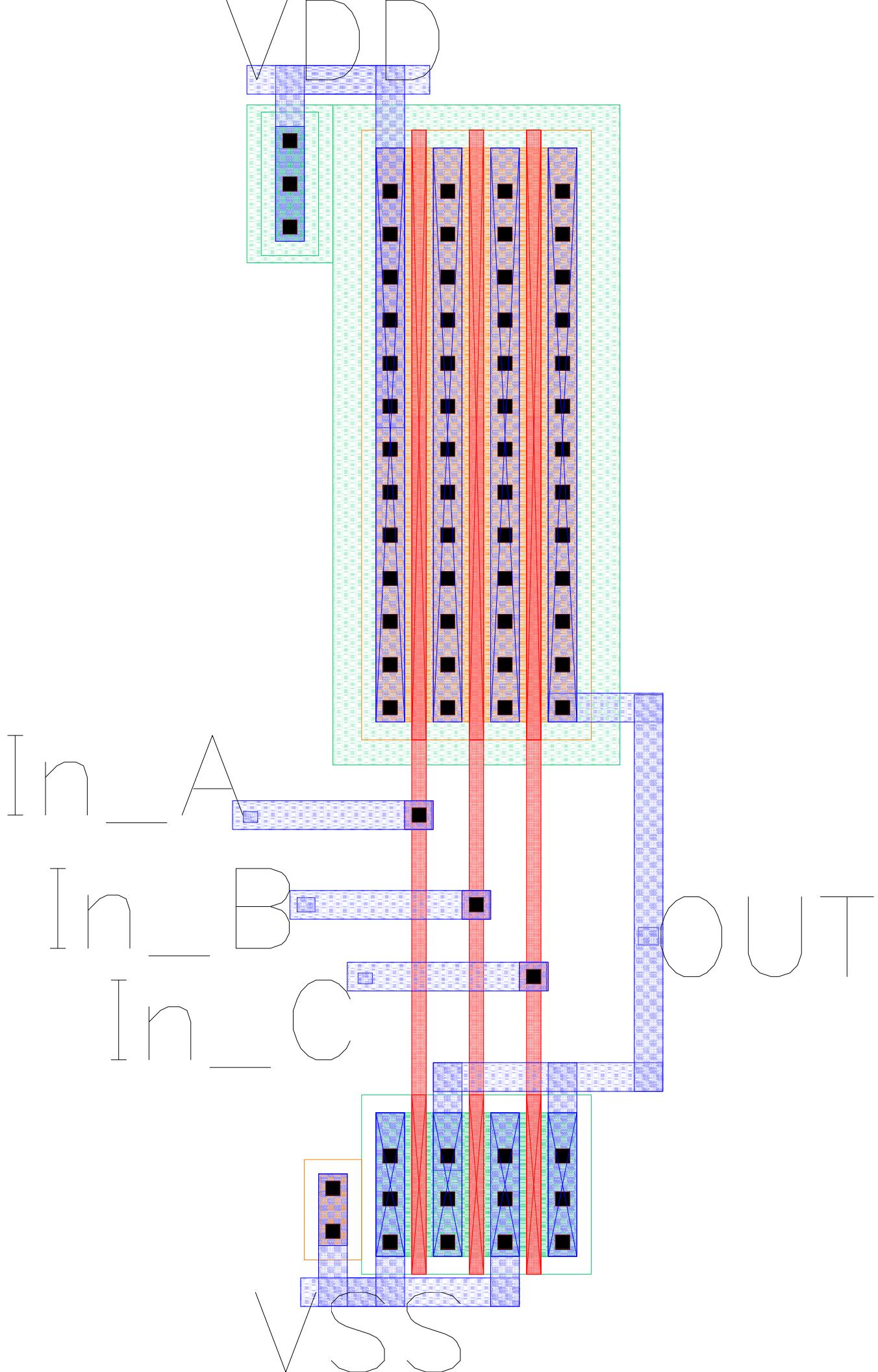
Schematic (3-input NOR gate)



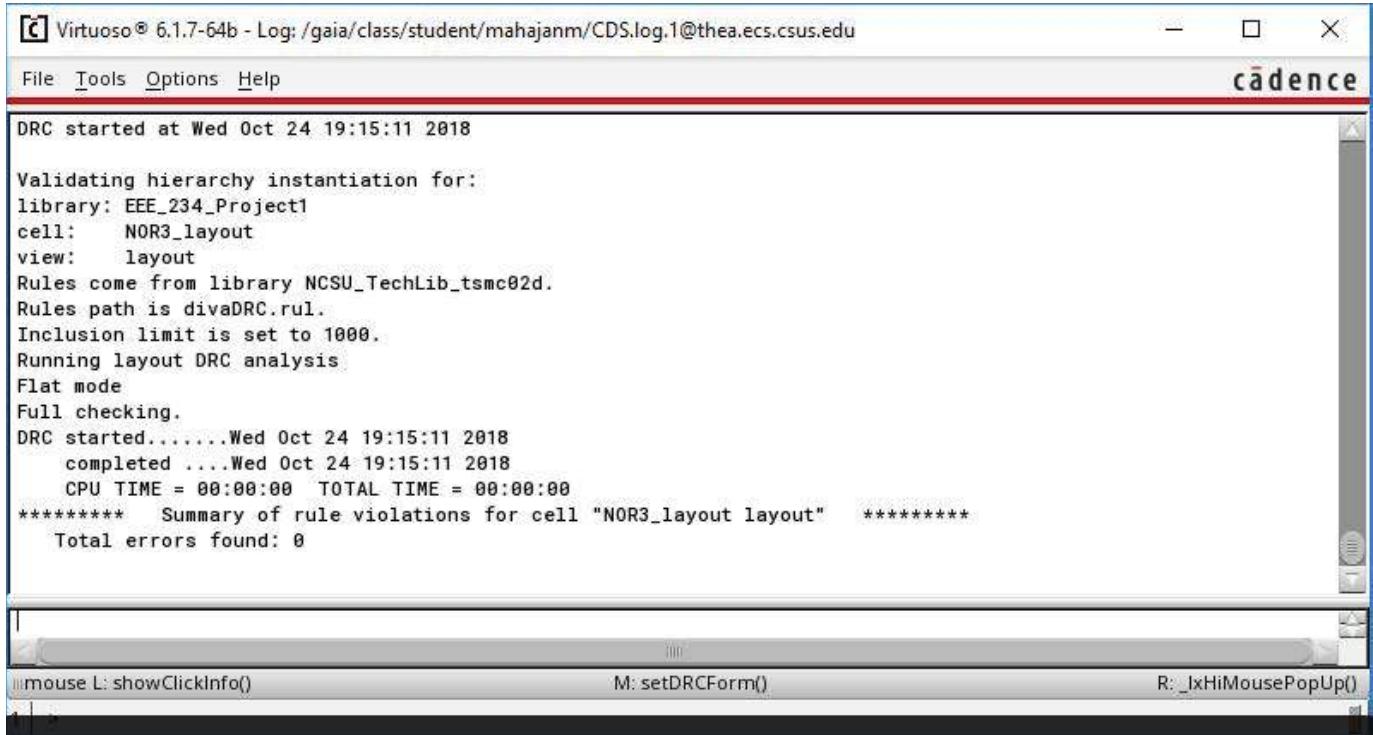
Testbench (3-input NOR gate)



Transient Response**3 Input NOR Waveform****Sun Oct 7 20:24:44 2018**



DRC (3-input NOR gate)



The screenshot shows a terminal window titled "Virtuoso® 6.1.7-64b - Log: /gaia/class/student/mahajanm/CDS.log.1@thea.ecs.csus.edu". The window displays the output of a DRC analysis for a 3-input NOR gate. The log message indicates that the DRC started at Wednesday, October 24, 19:15:11, 2018. It details the validation process, mentioning the library (EEE_234_Project1), cell (NOR3_layout), and view (layout). It also notes the rule source (NCSU_TechLib_tsmc02d) and rule path (divaDRC.rul). The inclusion limit is set to 1000. The analysis is performed in flat mode with full checking. The DRC completed successfully in 00:00:00 CPU time and 00:00:00 total time, reporting 0 total errors. The bottom of the window shows three menu items: mouse L: showClickInfo(), M: setDRCForm(), and R: _IxHiMousePopUp().

```
Virtuoso® 6.1.7-64b - Log: /gaia/class/student/mahajanm/CDS.log.1@thea.ecs.csus.edu
File Tools Options Help
cadence

DRC started at Wed Oct 24 19:15:11 2018

Validating hierarchy instantiation for:
library: EEE_234_Project1
cell:   NOR3_layout
view:   layout
Rules come from library NCSU_TechLib_tsmc02d.
Rules path is divaDRC.rul.
Inclusion limit is set to 1000.
Running layout DRC analysis
Flat mode
Full checking.
DRC started.....Wed Oct 24 19:15:11 2018
completed ....Wed Oct 24 19:15:11 2018
CPU TIME = 00:00:00  TOTAL TIME = 00:00:00
***** Summary of rule violations for cell "NOR3_layout layout" *****
Total errors found: 0

mouse L: showClickInfo()
M: setDRCForm()
R: _IxHiMousePopUp()
```

LVS (3inputNOR) :

Running simulation in directory: "/gaia/class/student/mahajanm/EEE_234_Project1/LVS".

Begin netlist: Oct 24 19:16:53 2018

```
view name list = ("auLvs" "extracted" "schematic")
stop name list = ("auLvs")
library name = "EEE_234_Project1"
cell name = "NOR3_layout"
view name = "extracted"
globals lib = "basic"
```

Running Artist Flat Netlisting ...

End netlist: Oct 24 19:16:53 2018

Begin netlist: Oct 24 19:16:53 2018

```
view name list = ("auLvs" "schematic")
stop name list = ("auLvs")
library name = "EEE_234_Project1"
cell name = "NOR3"
view name = "schematic"
globals lib = "basic"
```

Running Artist Flat Netlisting ...

End netlist: Oct 24 19:16:54 2018

Moving original netlist to extNetlist

Removing parasitic components from netlist

presistors removed: 0

pcapacitors removed: 0

pinductors removed: 0

pdiodes removed: 0

trans lines removed: 0

8 nodes merged into 8 nodes

Running netlist comparison program: LVS

Begin comparison: Oct 24 19:16:54 2018

@(#)CDS: LVS version 6.1.7-64b 09/27/2016 19:41 (sjfhw305) \$

The net-lists match.

layout schematic

instances

| | | |
|-------------|---|---|
| un-matched | 0 | 0 |
| rewired | 0 | 0 |
| size errors | 0 | 0 |
| pruned | 0 | 0 |
| active | 6 | 6 |
| total | 6 | 6 |

nets

| | | |
|------------|---|---|
| un-matched | 0 | 0 |
| merged | 0 | 0 |
| pruned | 0 | 0 |
| active | 8 | 8 |
| total | 8 | 8 |

terminals

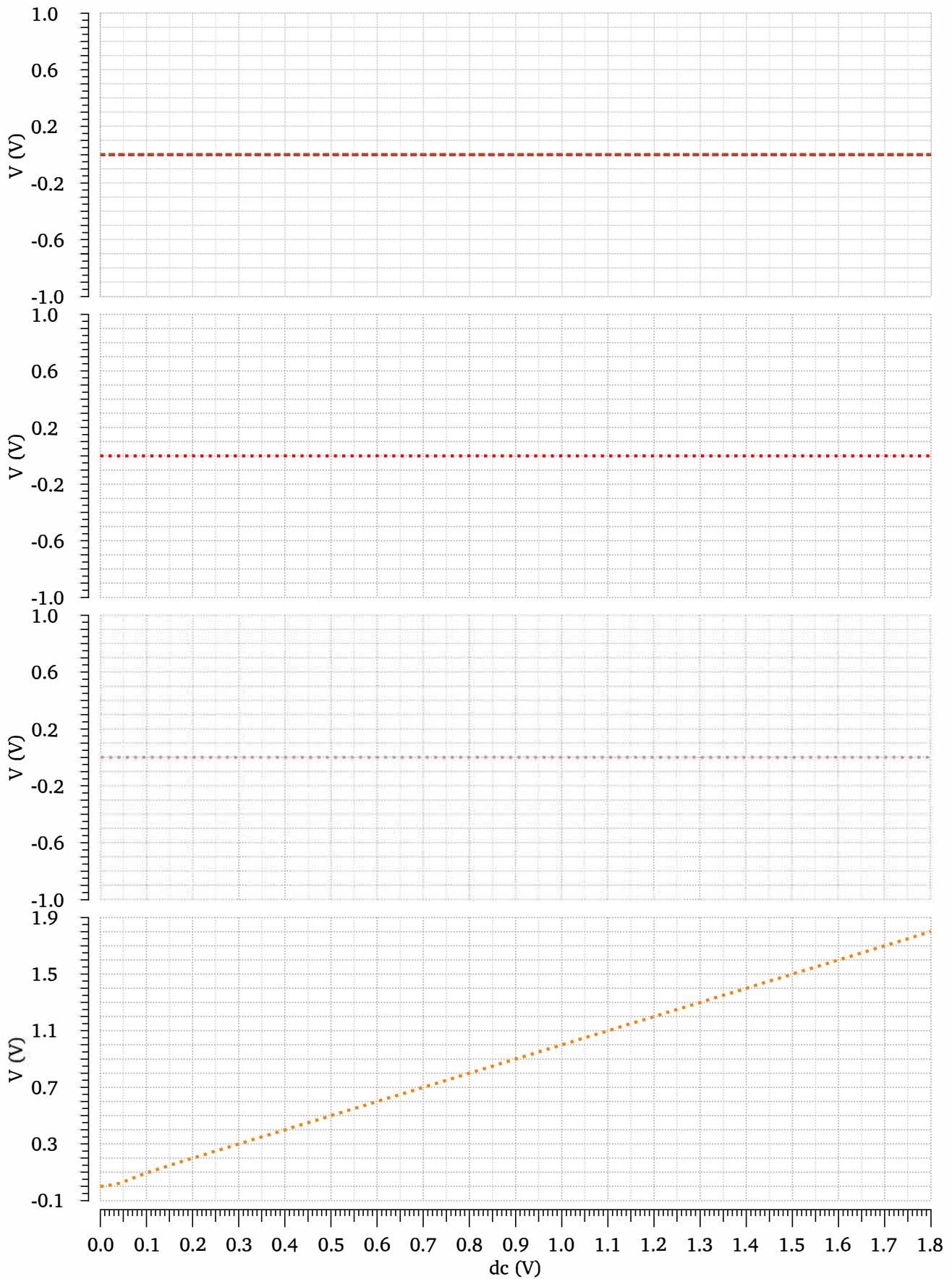
| | | |
|----------------|---|---|
| un-matched | 0 | 0 |
| matched but | | |
| different type | 0 | 0 |
| total | 6 | 6 |

End comparison: Oct 24 19:16:54 2018

Comparison program completed successfully.

DC Response**3 Input NOR DC Waveform****Wed Oct 24 19:19:34 2018**

| Name | Vis |
|-------|-----|
| /In_A | • |

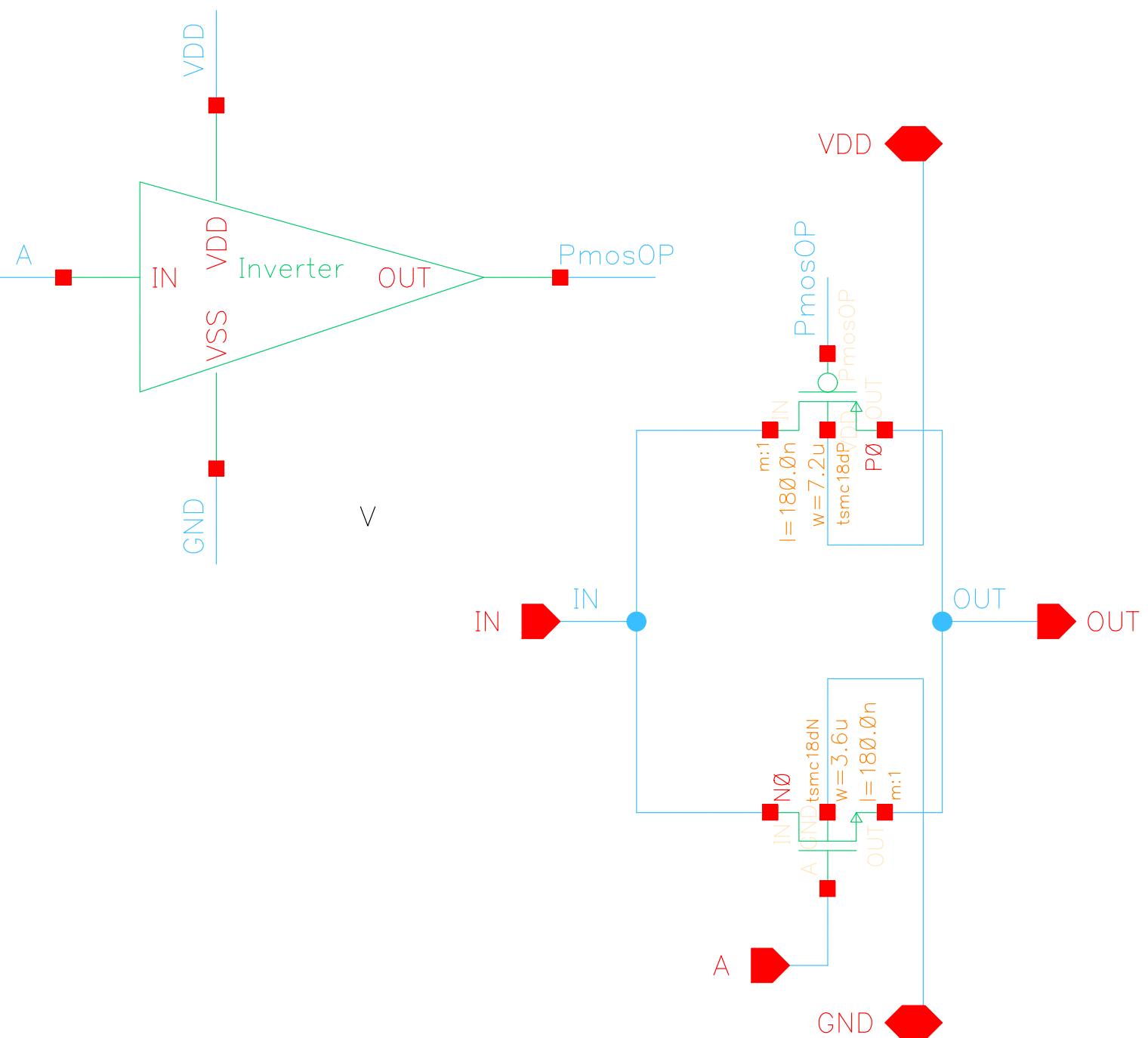


Transmission Gate

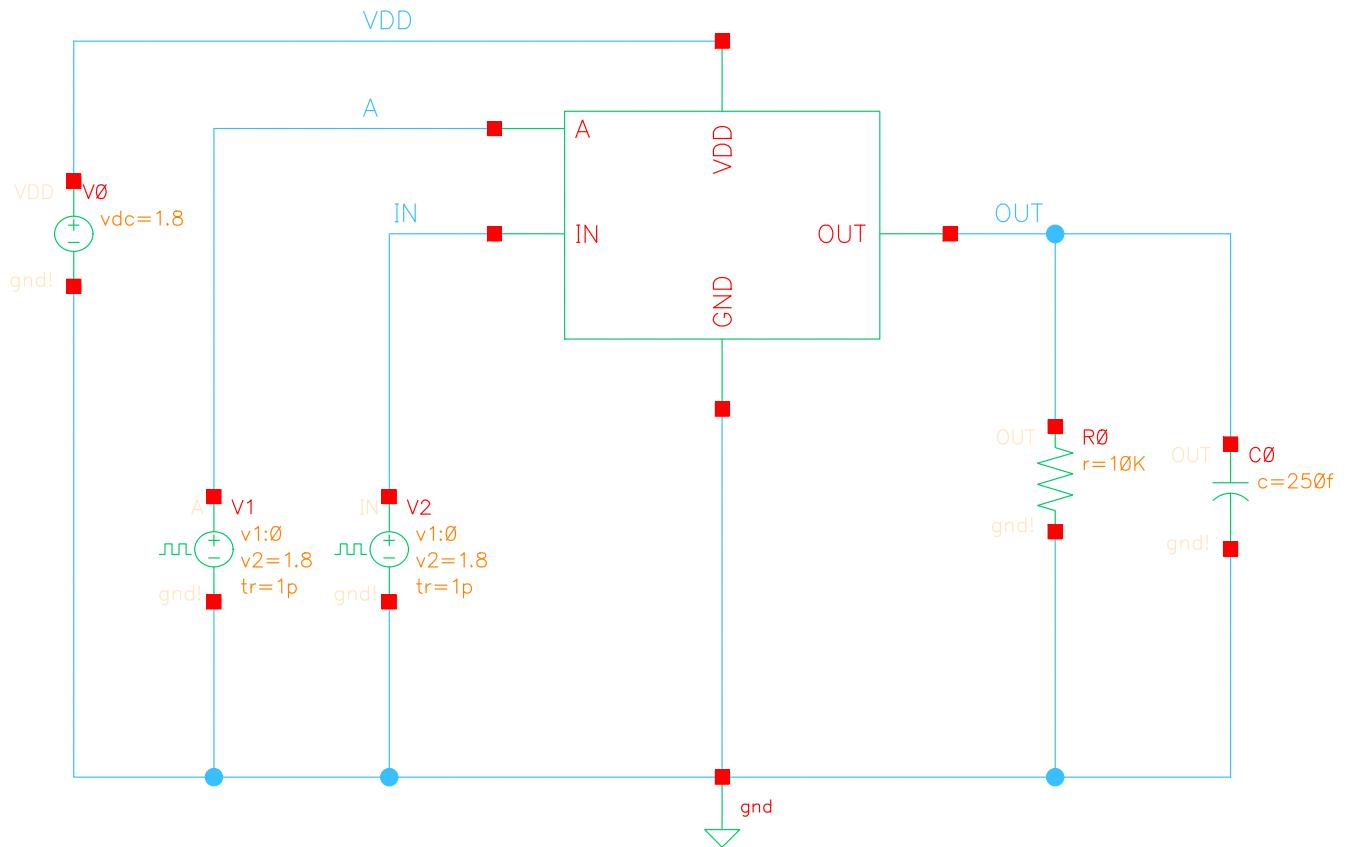
$$(W/L)_n = 1.8/0.18$$

$$(W/L)_p = 3.6/0.18$$

Schematic (Transmission Gate)

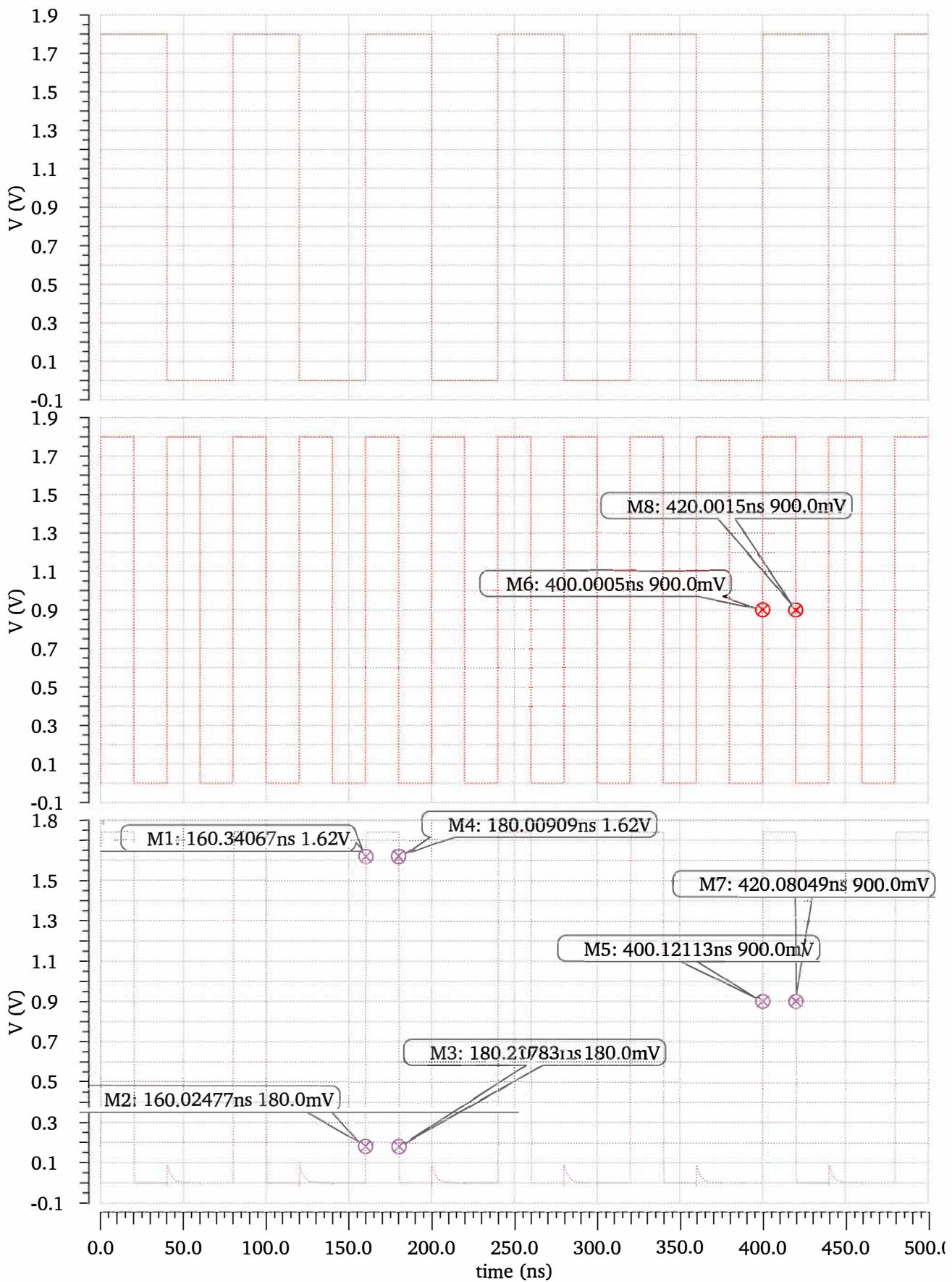


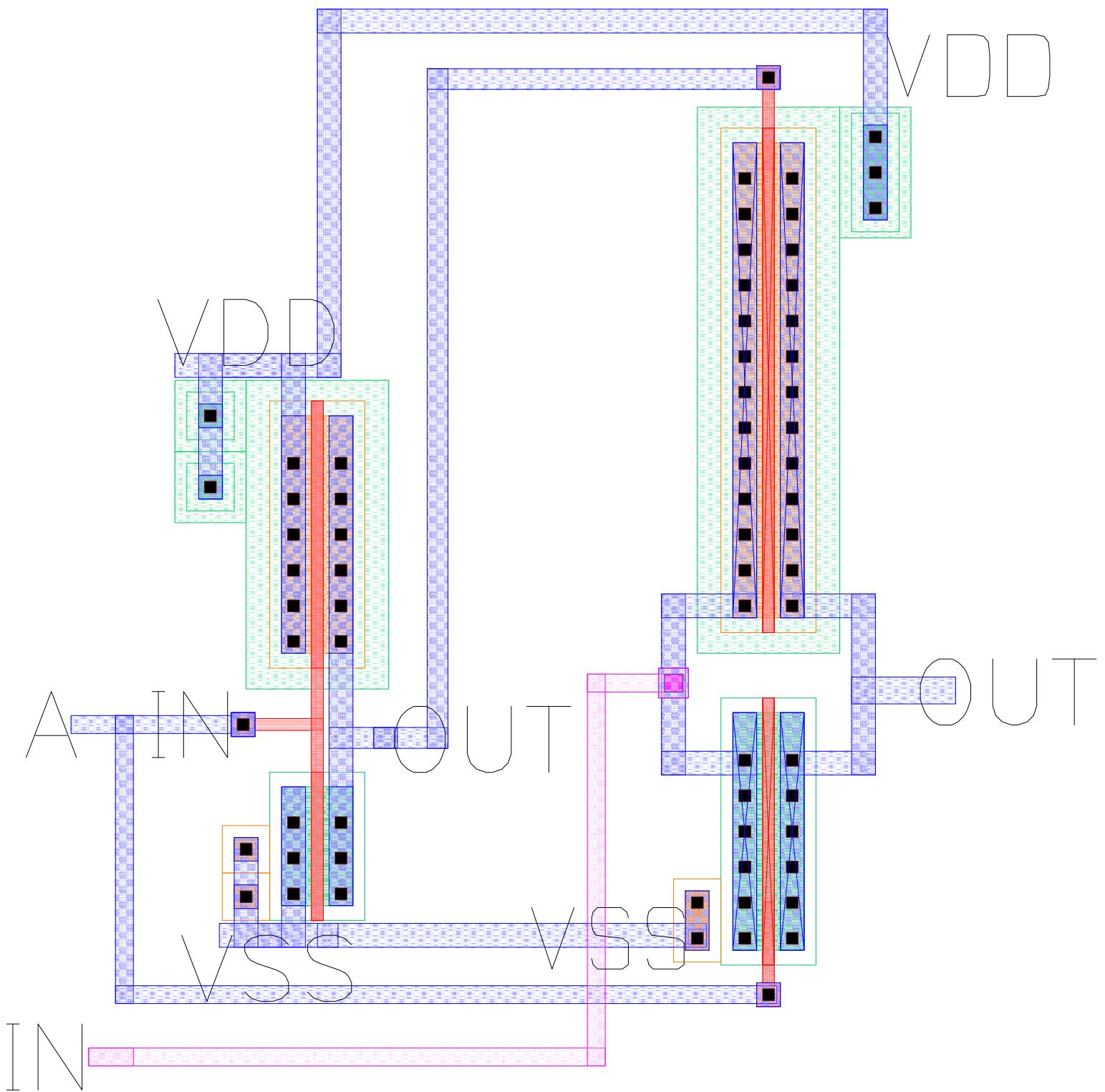
Test bench (Transmission Gate)



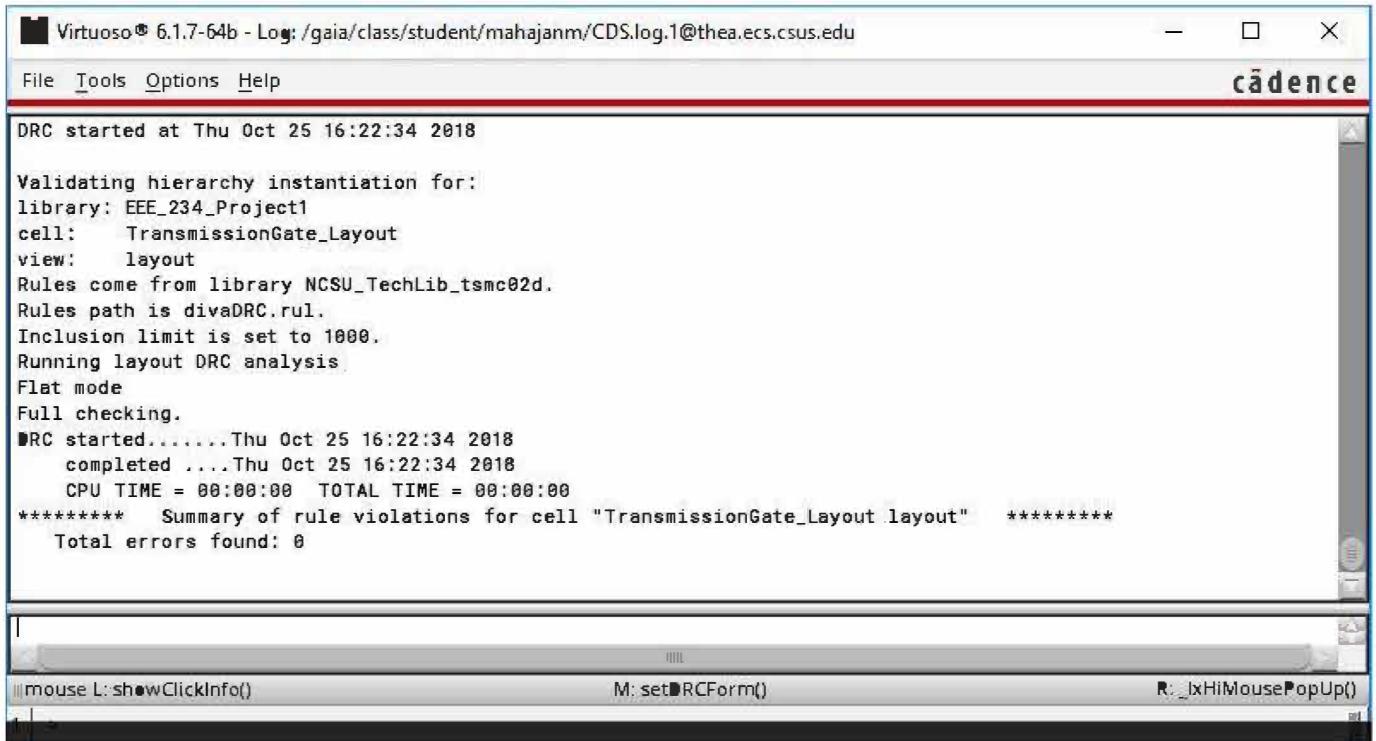
Transient Response**Transmission Gate Waveform****Sun Oct 7 20:11:20 2018**

| Name | Vis |
|--------|-----|
| ■ /A | ● |
| ■ /IN | ● |
| ■ /OUT | ● |





DRC (Transmission Gate)



Virtuoso® 6.1.7-64b - Log: /gaia/class/student/mahajanm/CDS.log.1@thea.ecs.csus.edu

File Tools Options Help

cadence

```
DRC started at Thu Oct 25 16:22:34 2018

Validating hierarchy instantiation for:
library: EEE_234_Project1
cell: TransmissionGate_Layout
view: layout
Rules come from library NCSU_TechLib_tsmc02d.
Rules path is divaDRC.rul.
Inclusion limit is set to 1000.
Running layout DRC analysis
Flat mode
Full checking.
DRC started.....Thu Oct 25 16:22:34 2018
completed ....Thu Oct 25 16:22:34 2018
CPU TIME = 00:00:00 TOTAL TIME = 00:00:00
***** Summary of rule violations for cell "TransmissionGate_Layout layout" *****
Total errors found: 0
```

mouse L:showClickInfo() M: setDRCForm() R: _lxHiMousePopUp()

LVS(Transmission Gate) :

Running simulation in directory: "/gaia/class/student/mahajanm/EEE_234_Project1/LVS".

Begin netlist: Oct 25 17:04:40 2018

```
view name list = ("auLvs" "extracted" "schematic")
stop name list = ("auLvs")
library name = "EEE_234_Project1"
cell name = "TransmissionGate_Layout"
view name = "extracted"
globals lib = "basic"
```

Running Artist Flat Netlisting ...

End netlist: Oct 25 17:04:40 2018

Begin netlist: Oct 25 17:04:40 2018

```
view name list = ("auLvs" "schematic")
stop name list = ("auLvs")
library name = "EEE_234_Project1"
cell name = "TransmissionGate"
view name = "schematic"
globals lib = "basic"
```

Running Artist Flat Netlisting ...

End netlist: Oct 25 17:04:40 2018

Moving original netlist to extNetlist

Removing parasitic components from netlist

```
presistors removed: 0
pcapacitors removed: 0
pinductors removed: 0
pdiodes removed: 0
trans lines removed: 0
6 nodes merged into 6 nodes
```

Running netlist comparison program: LVS

Begin comparison: Oct 25 17:04:40 2018

@(#) \$CDS: LVS version 6.1.7-64b 09/27/2016 19:41 (sjfhw305) \$

The net-lists match.

layout schematic

instances

| | | |
|-------------|---|---|
| un-matched | 0 | 0 |
| rewired | 0 | 0 |
| size errors | 0 | 0 |
| pruned | 0 | 0 |
| active | 4 | 4 |
| total | 4 | 4 |

nets

| | | |
|------------|---|---|
| un-matched | 0 | 0 |
| merged | 0 | 0 |
| pruned | 0 | 0 |
| active | 6 | 6 |
| total | 6 | 6 |

terminals

| | | |
|----------------|---|---|
| un-matched | 0 | 0 |
| matched but | | |
| different type | 2 | 2 |
| total | 5 | 5 |

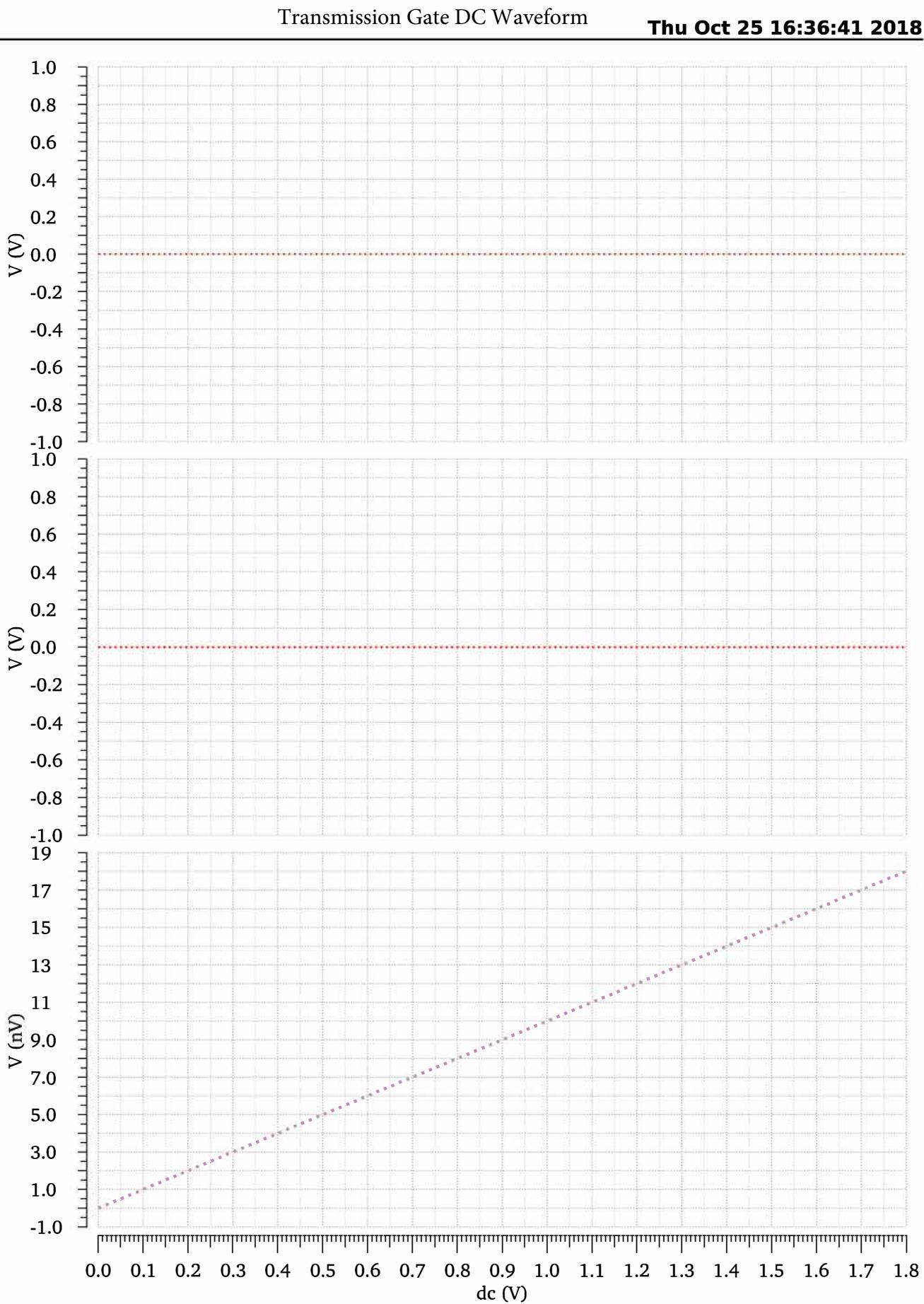
End comparison: Oct 25 17:04:40 2018

Comparison program completed successfully.

DC Response

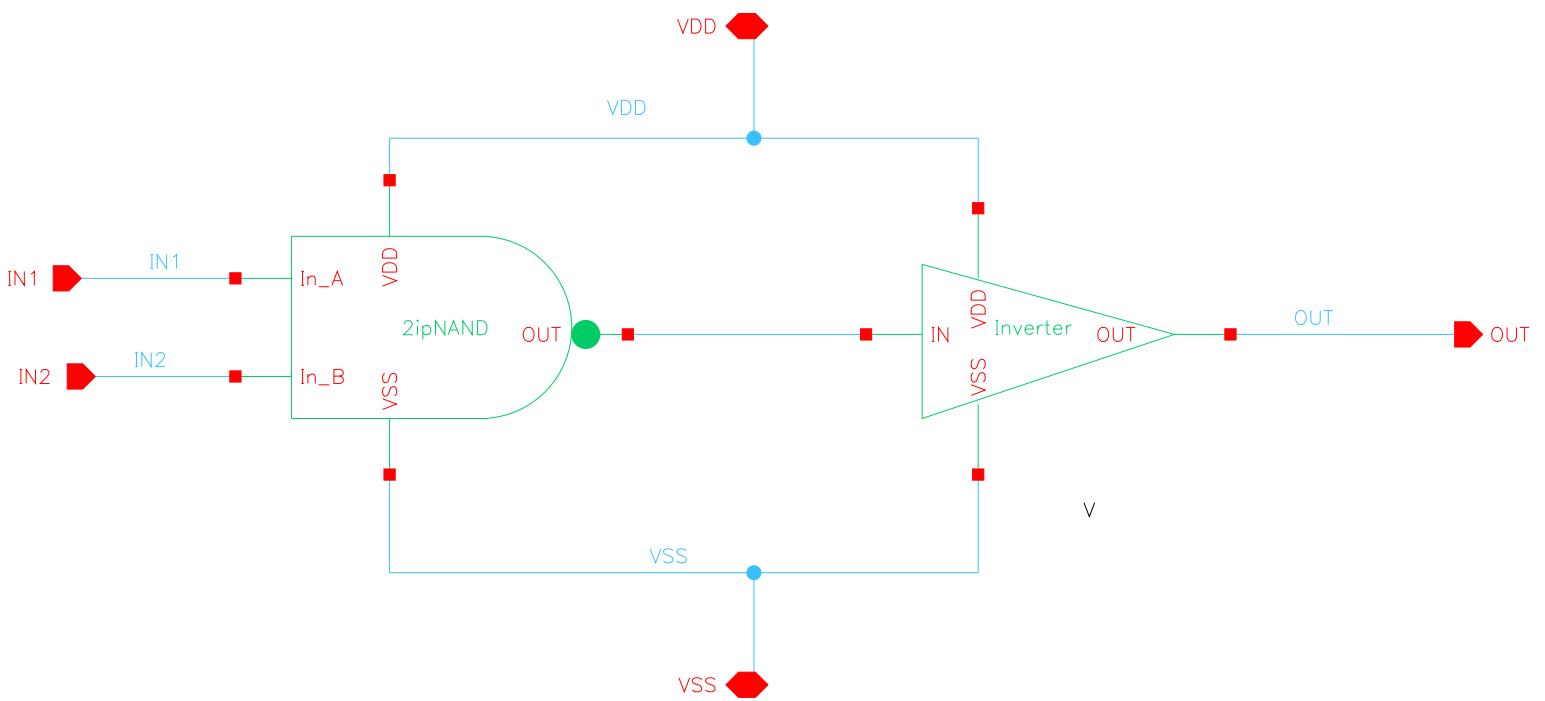
Name Vis

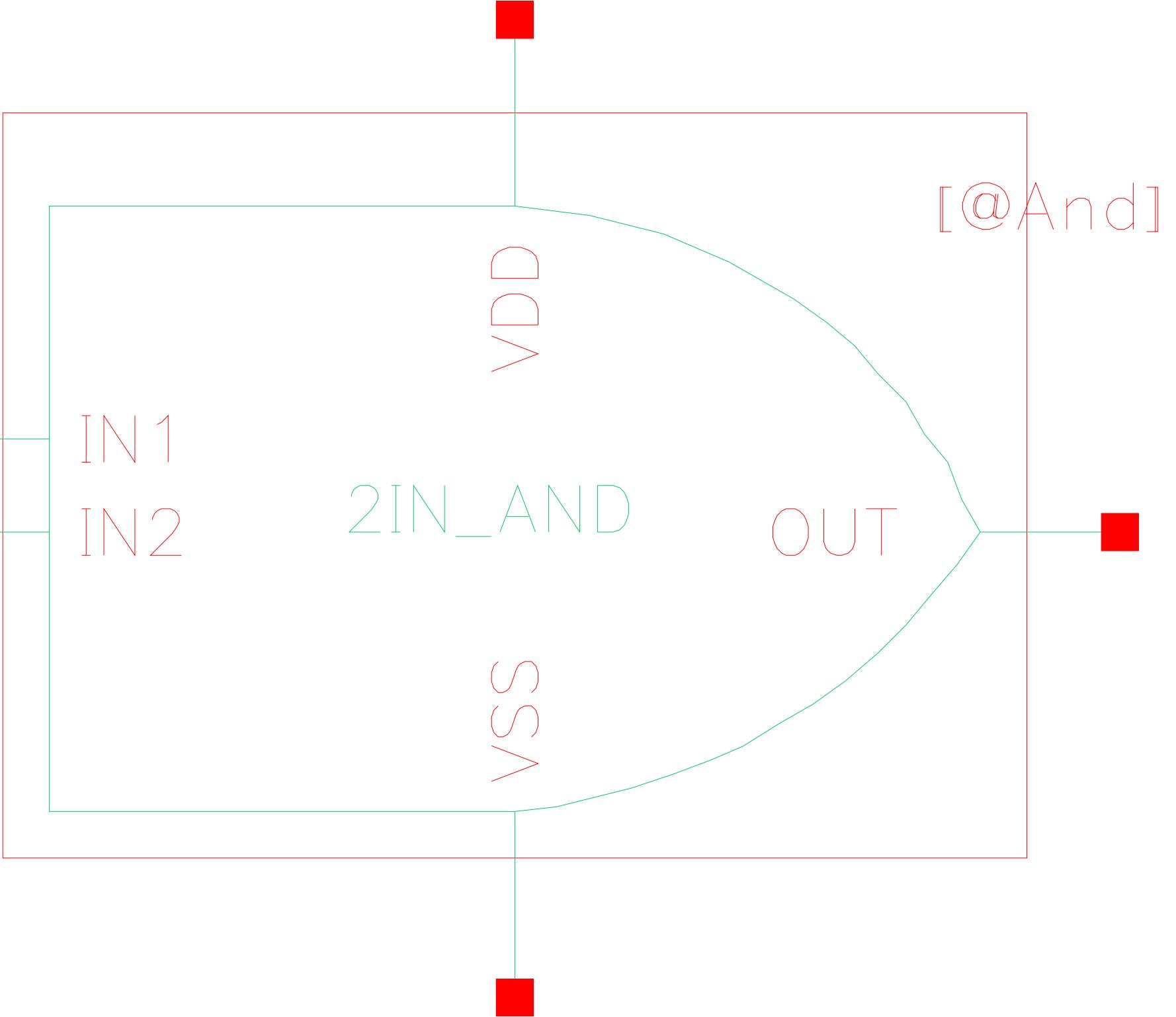
■ /A

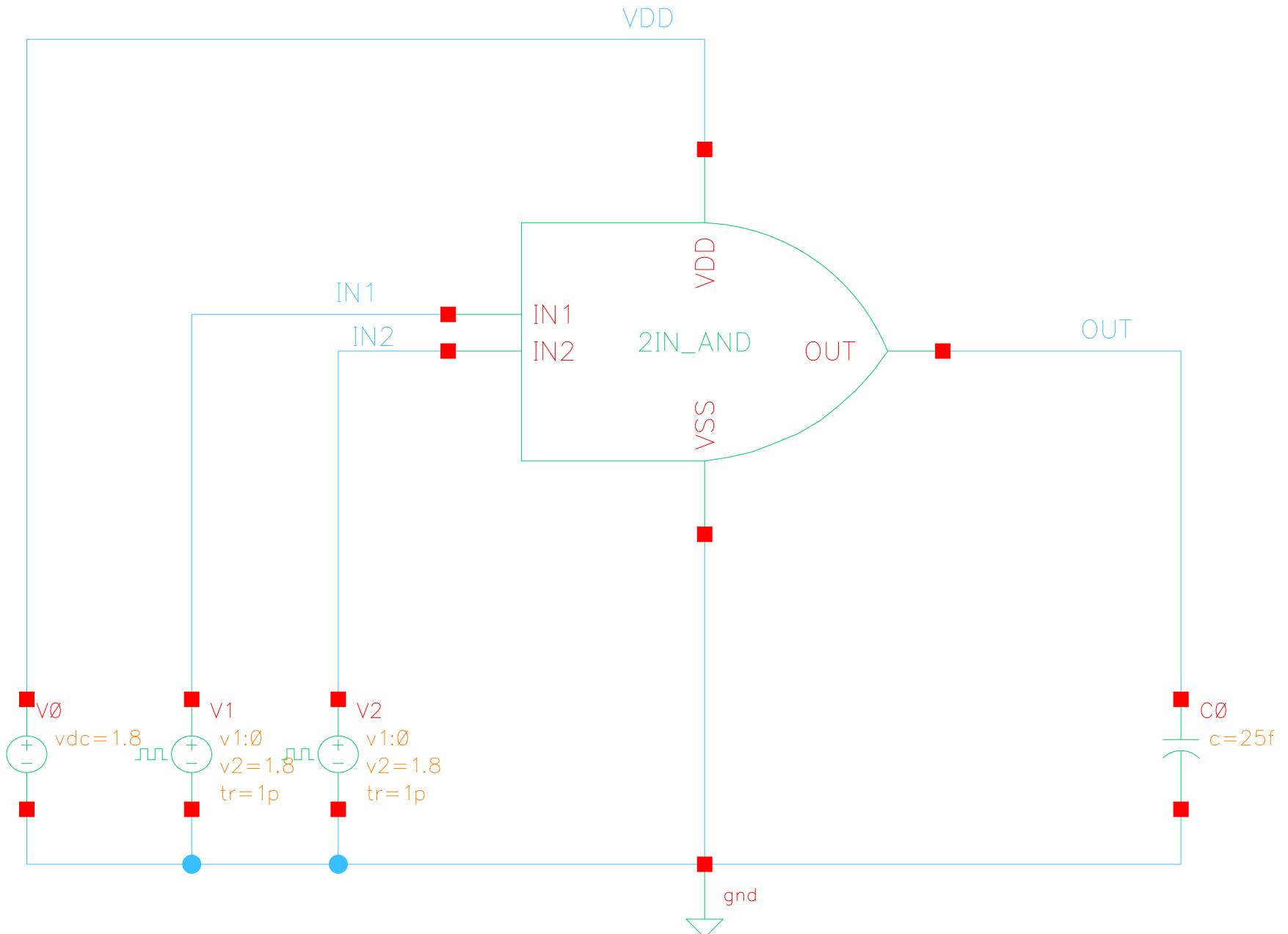


2 Input AND gate

2 Input AND gate schematic



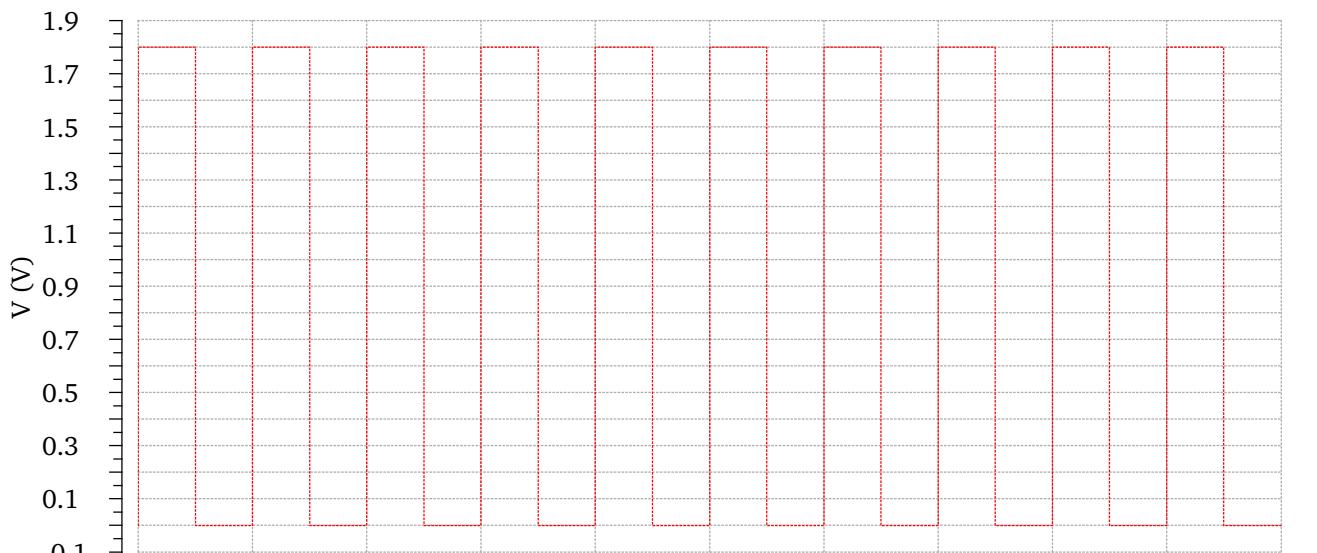




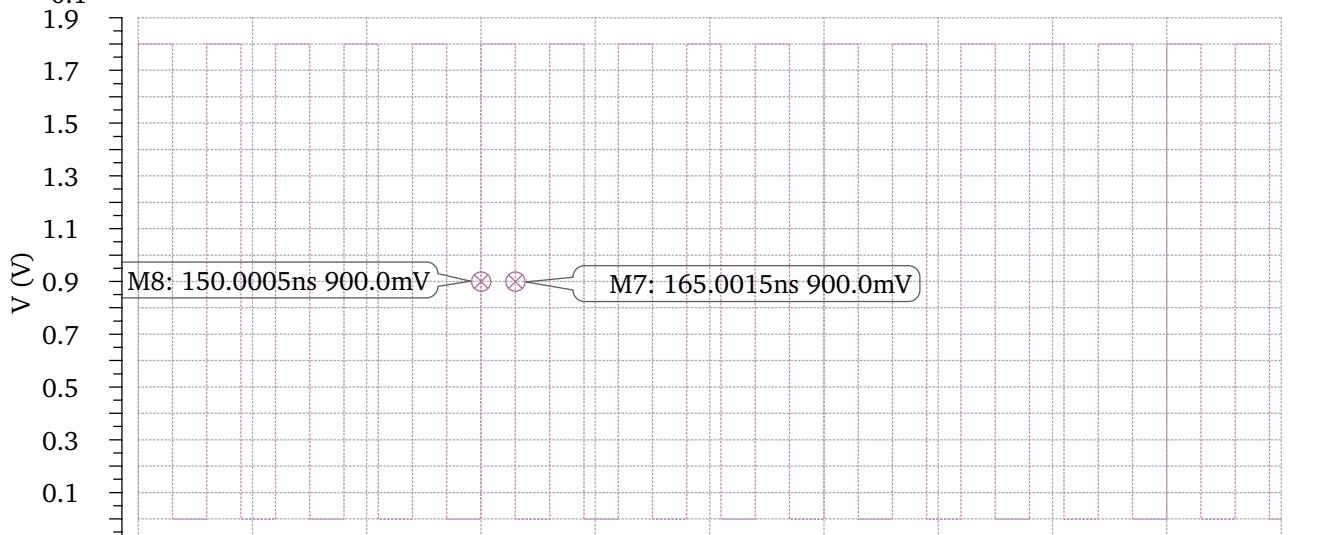
Transient Response**2 input AND Waveform****Fri Nov 30 22:32:02 2018**

Name Vis

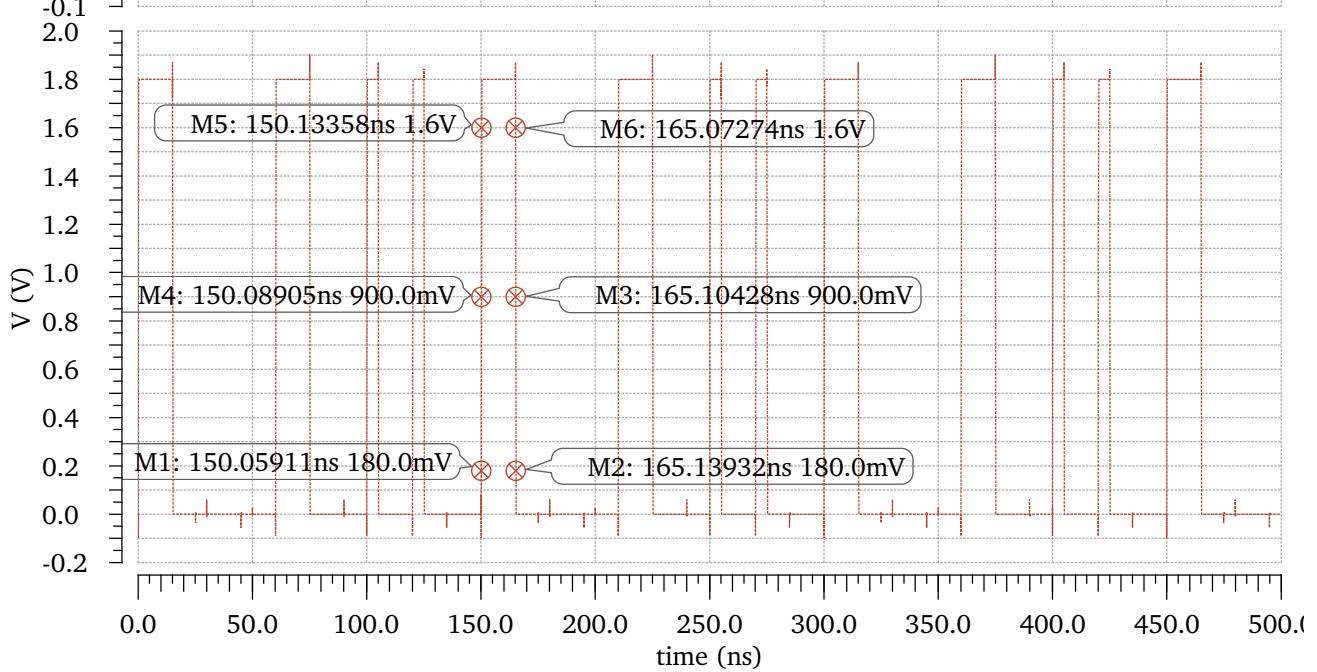
■ /IN2

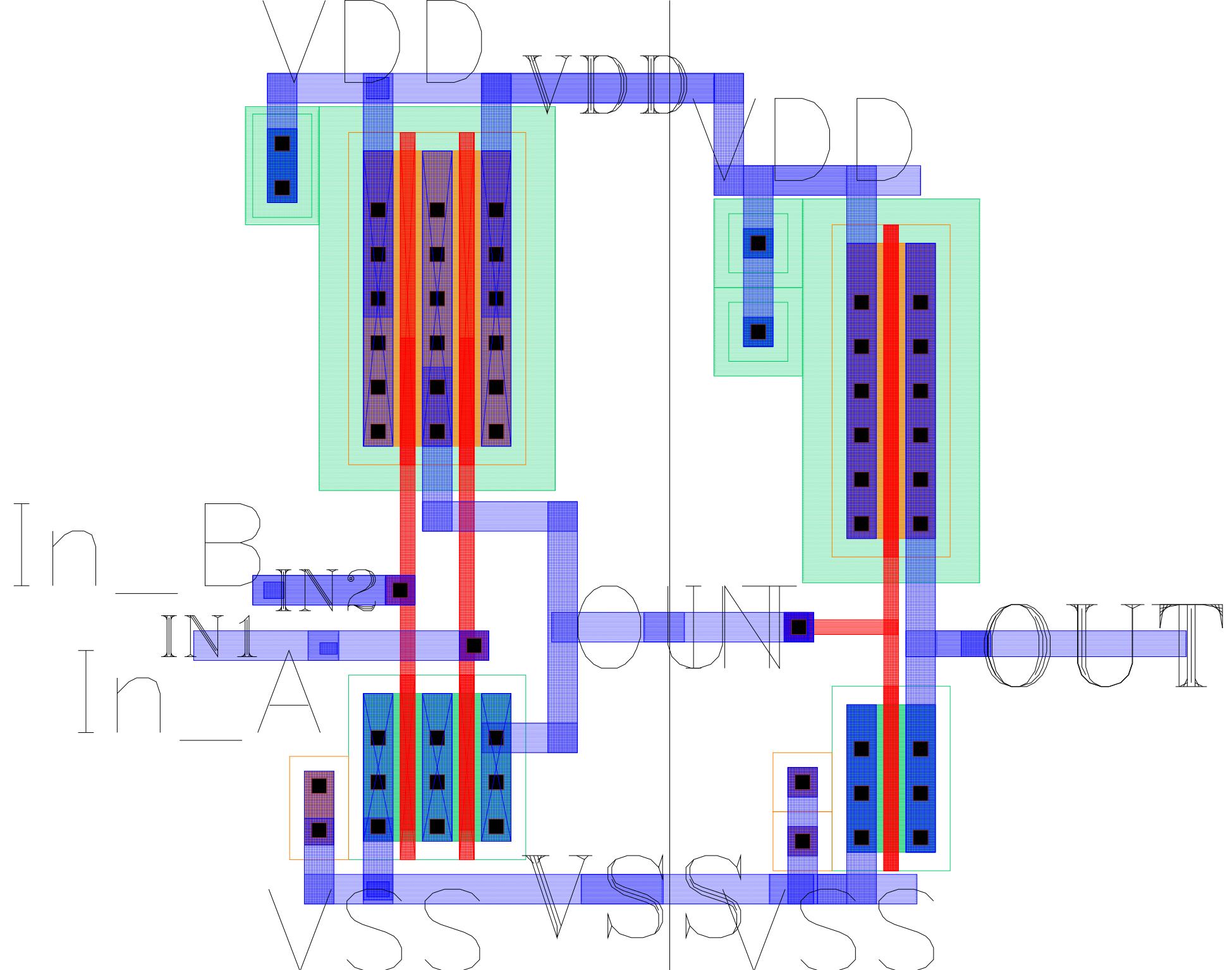


■ /IN1



■ /OUT





File Tools Options Help

cadence

CPU TIME = 00:00:00 TOTAL TIME = 00:00:00

***** Summary of rule violations for cell "2IN_AND_Layout layout" *****

Total errors found: 0

mouse L: showClickInfo()

M: setDRCForm()

R: _IxHiMousePopUp()

1 >

2 Input AND gate

@(#) \$CDS: LVS version 6.1.7-64b 09/27/2016 19:41 (sjfhw305) \$

Command line: /software/cadence/install/IC617/tools.lnx86/dfII/bin/64bit/LVS -dir
/gaia/class/student/kumars/EEE_234_share/LVS -l -s -t /gaia/class/student/kumars/EEE_234_share/LVS/layout
/gaia/class/student/kumars/EEE_234_share/LVS/schematic

Like matching is enabled.

Net swapping is enabled.

Using terminal names as correspondence points.

Net-list summary for /gaia/class/student/kumars/EEE_234_share/LVS/layout/netlist

count

| | |
|---|-----------|
| 7 | nets |
| 5 | terminals |
| 3 | pmos |
| 3 | nmos |

Net-list summary for /gaia/class/student/kumars/EEE_234_share/LVS/schematic/netlist

count

| | |
|---|-----------|
| 7 | nets |
| 5 | terminals |
| 3 | pmos |
| 3 | nmos |

Terminal correspondence points

| | | |
|----|----|-----|
| N5 | N1 | IN1 |
| N4 | N5 | IN2 |
| N3 | N2 | OUT |
| N6 | N3 | VDD |
| N2 | N0 | VSS |

Devices in the netlist but not in the rules:

pmos nmos

The net-lists match.

| | layout | schematic |
|-------------|-----------|-----------|
| | instances | |
| un-matched | 0 | 0 |
| rewired | 0 | 0 |
| size errors | 0 | 0 |
| pruned | 0 | 0 |
| active | 6 | 6 |
| total | 6 | 6 |

| | nets | |
|------------|------|---|
| un-matched | 0 | 0 |
| merged | 0 | 0 |
| pruned | 0 | 0 |
| active | 7 | 7 |
| total | 7 | 7 |

terminals

2 Input AND gate

| | | |
|-------------------------------|---|---|
| un-matched | 0 | 0 |
| matched but different type | 0 | 0 |
| total | 5 | 5 |

Probe files from /gaia/class/student/kumars/EEE_234_share/LVS/schematic

devbad.out:

netbad.out:

mergenet.out:

termbad.out:

prunenet.out:

prunedev.out:

audit.out:

Probe files from /gaia/class/student/kumars/EEE_234_share/LVS/layout

devbad.out:

netbad.out:

mergenet.out:

termbad.out:

prunenet.out:

prunedev.out:

audit.out:

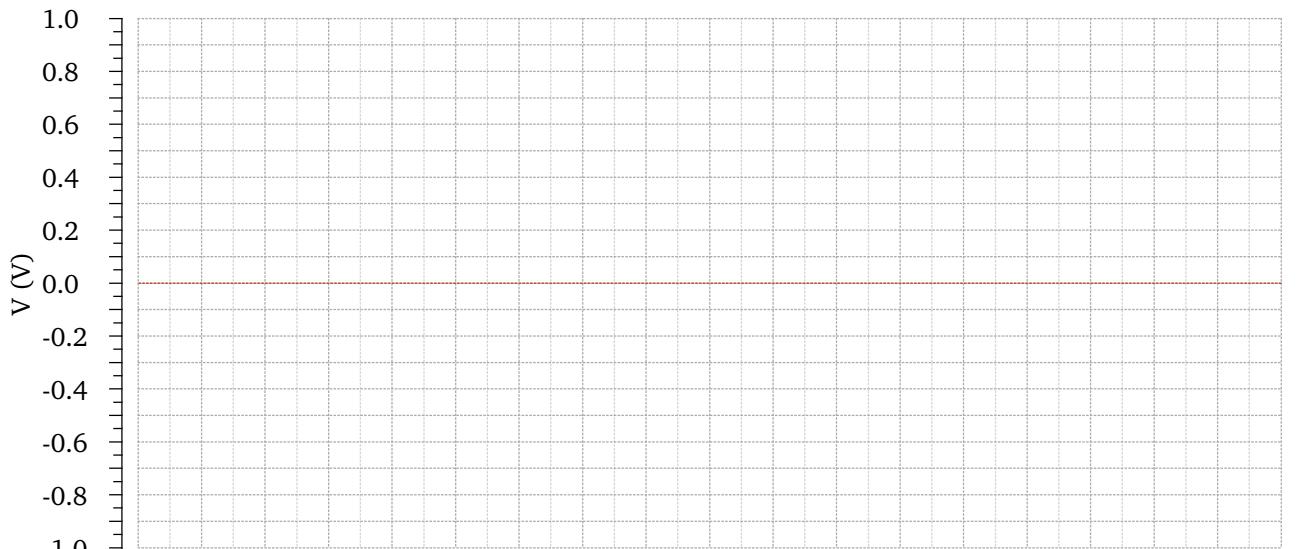
2 Input AND gate

Sat Dec 1 14:24:10 2018

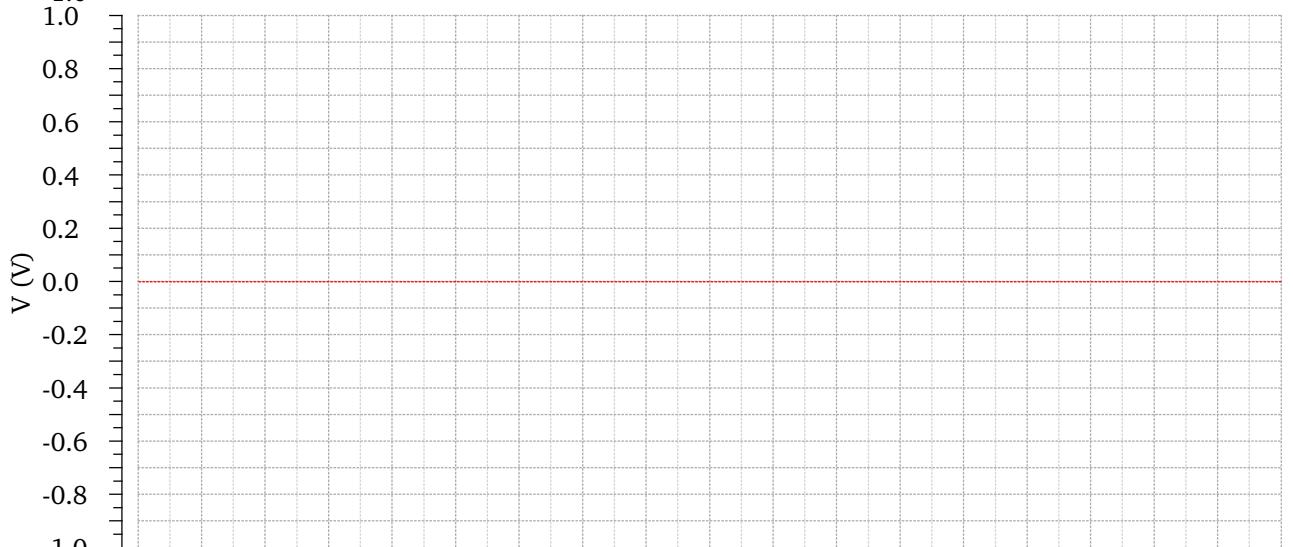
DC Response

Name Vis

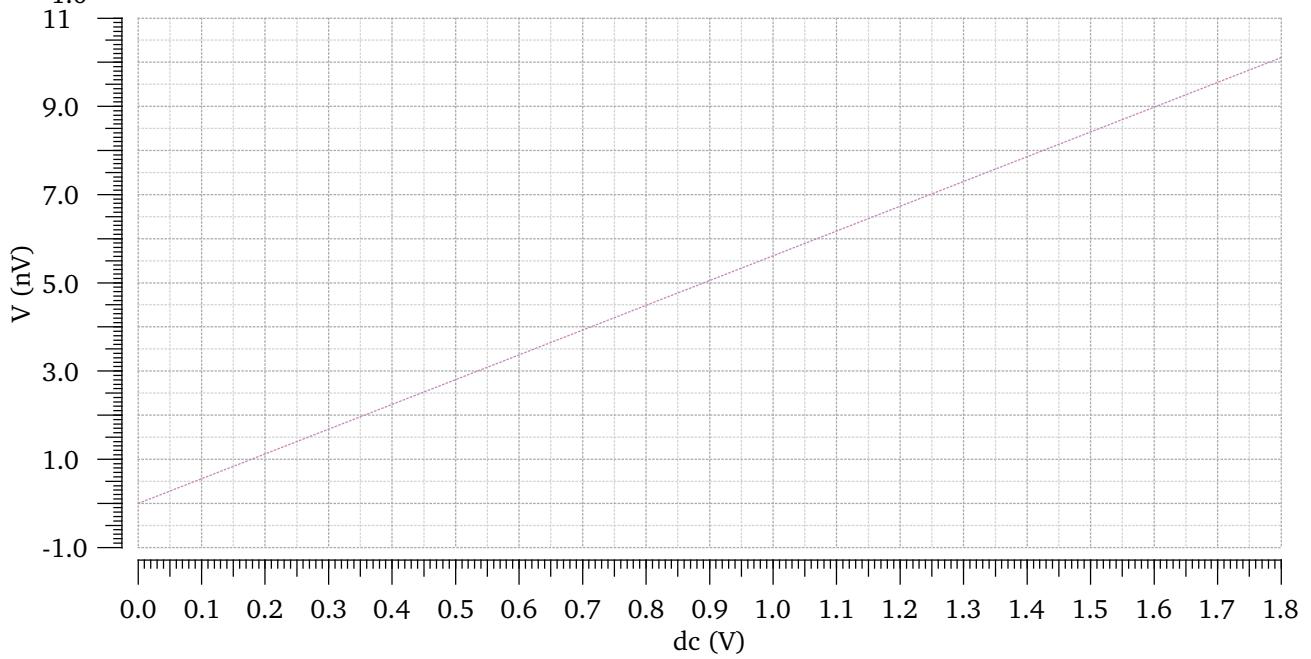
■ /IN1



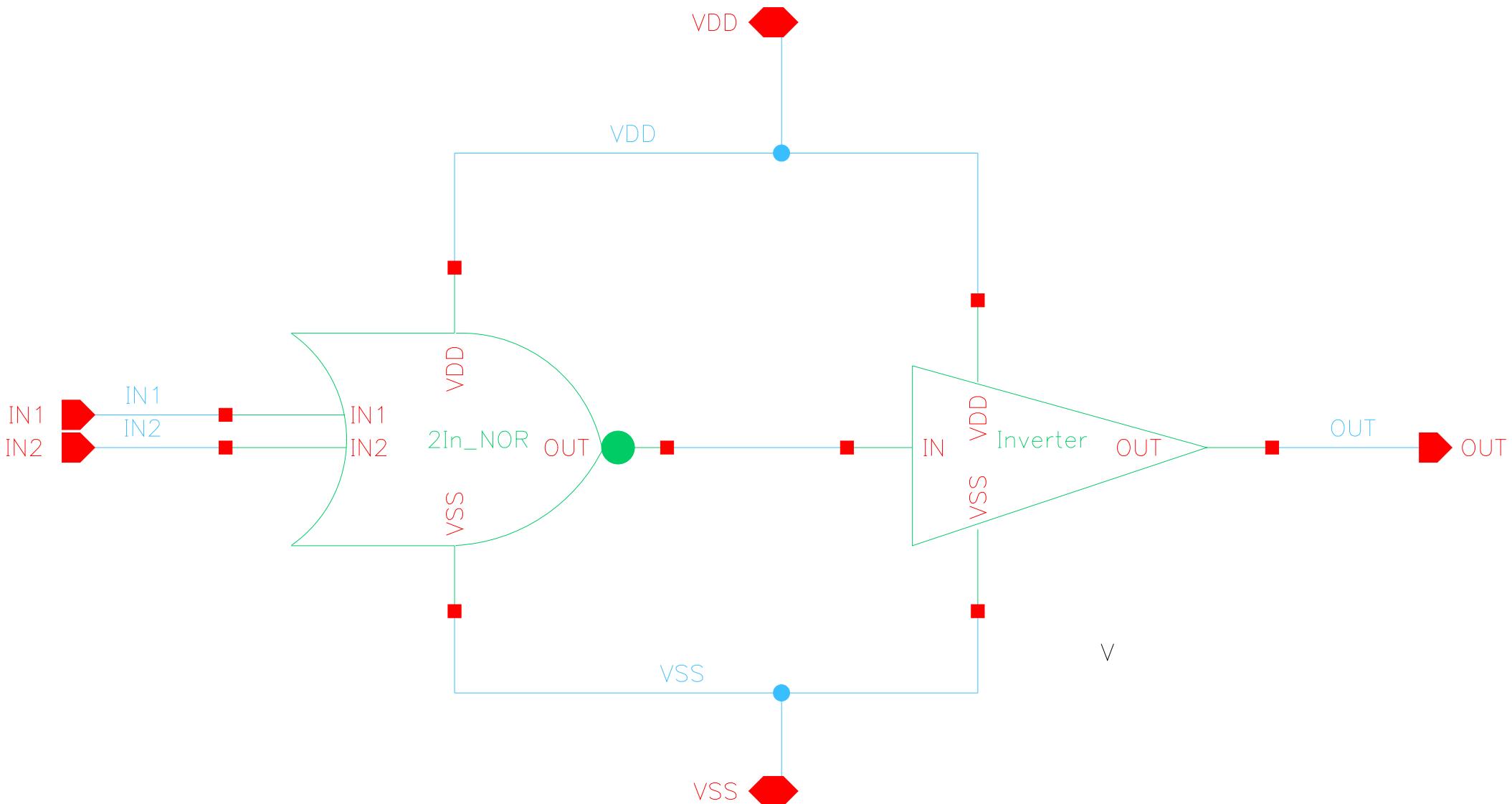
■ /IN2



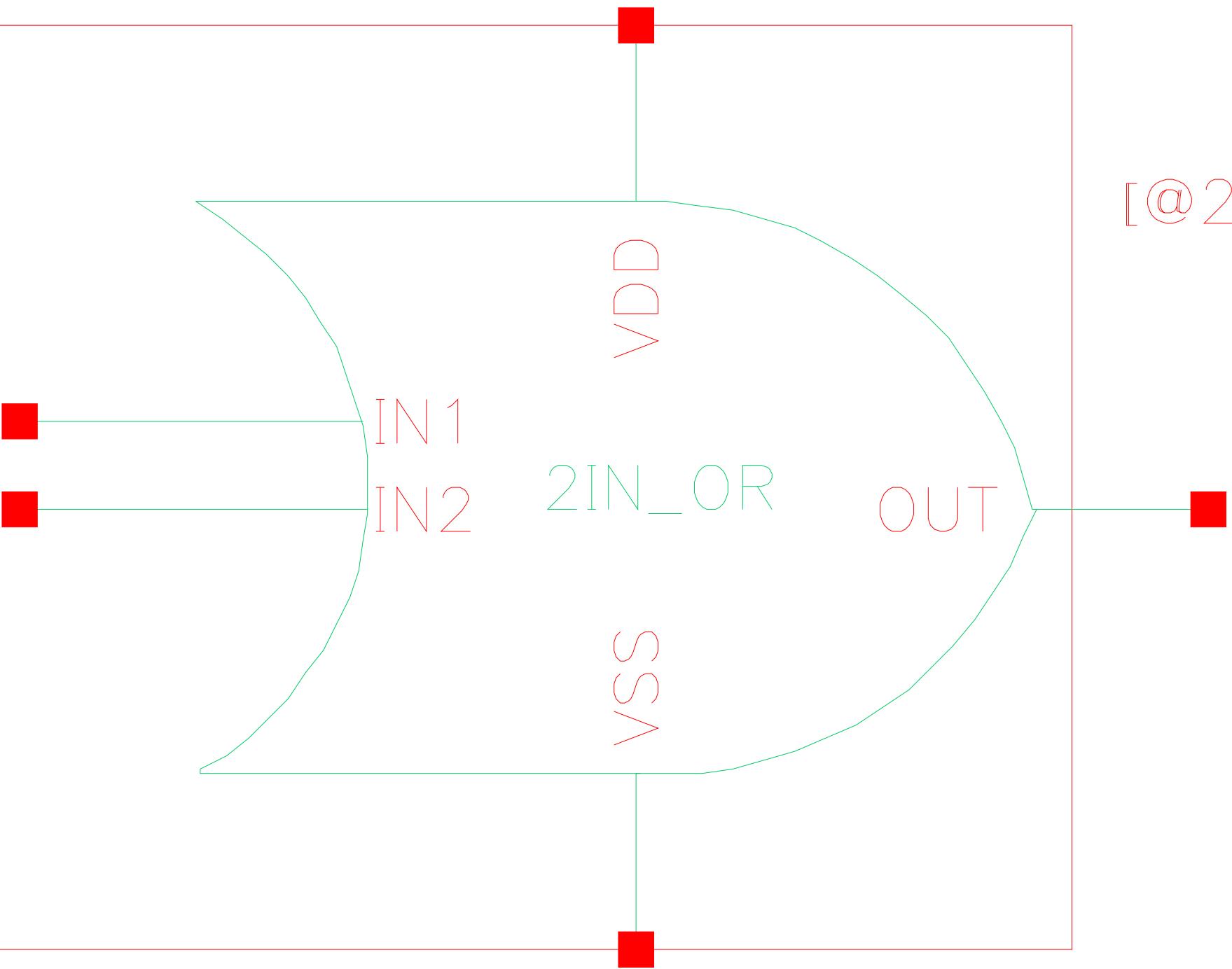
■ /OUT

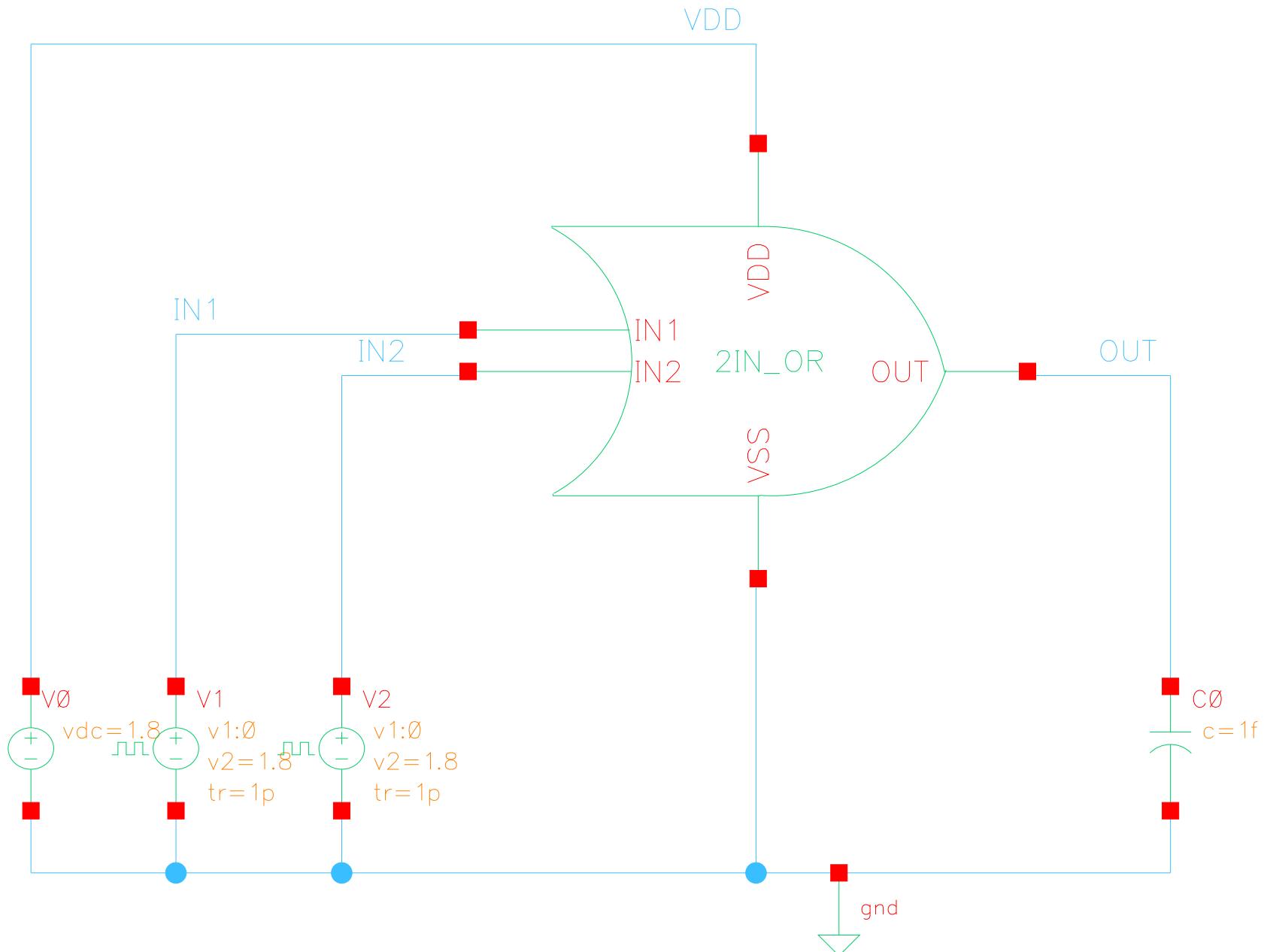


2 Input OR gate



[@20R]

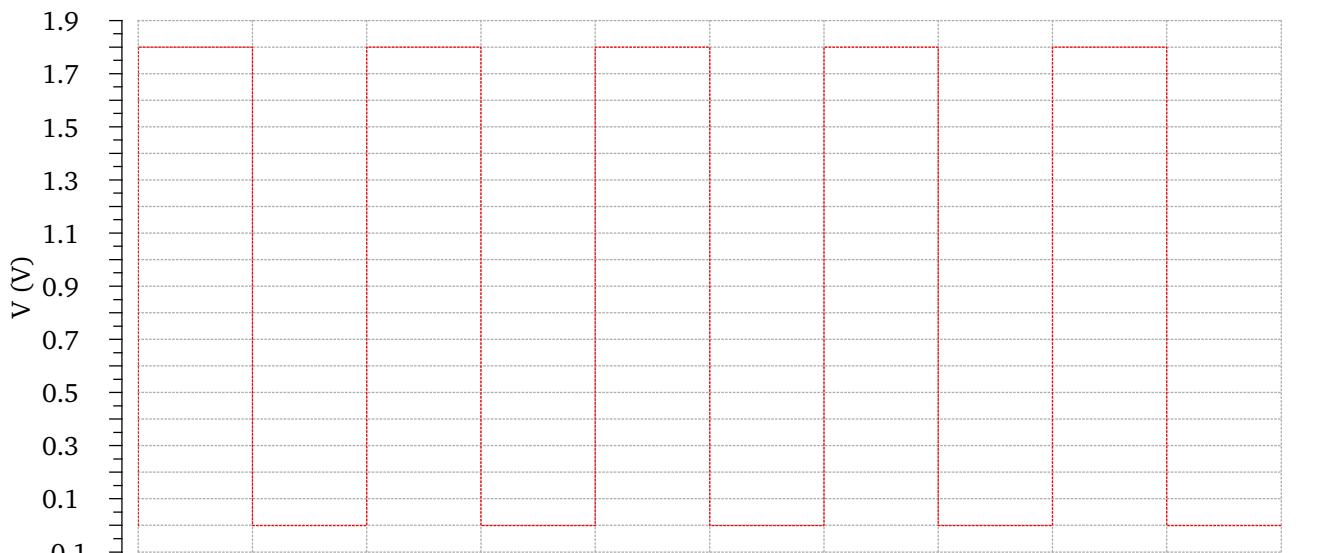




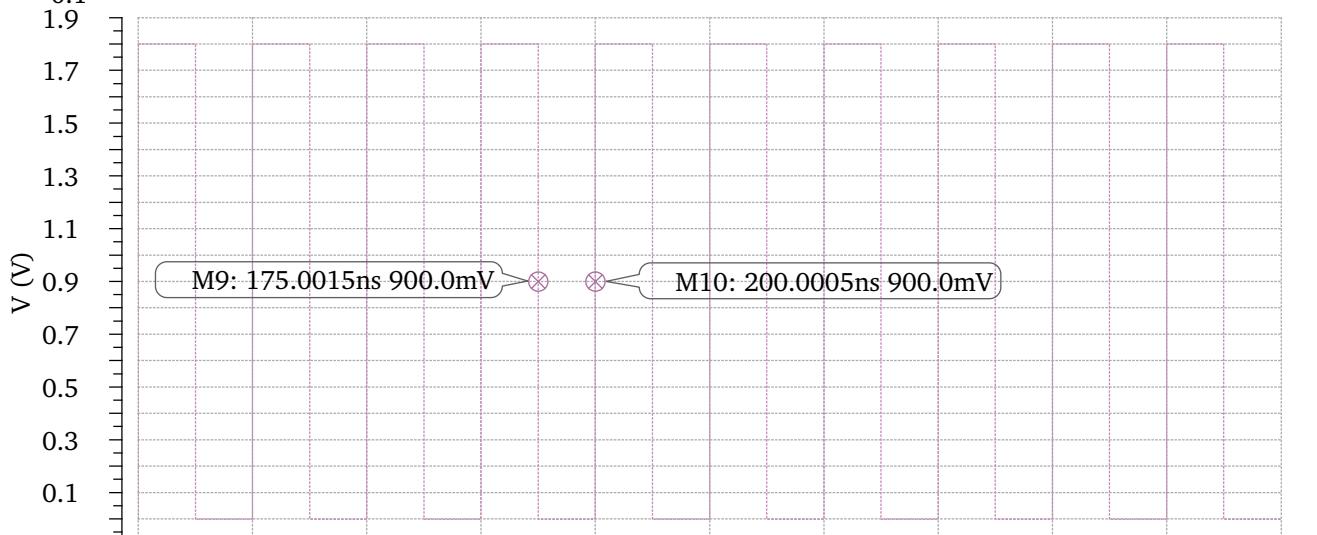
Transient Response**2 Input OR gate****Sat Dec 1 00:53:21 2018**

Name Vis

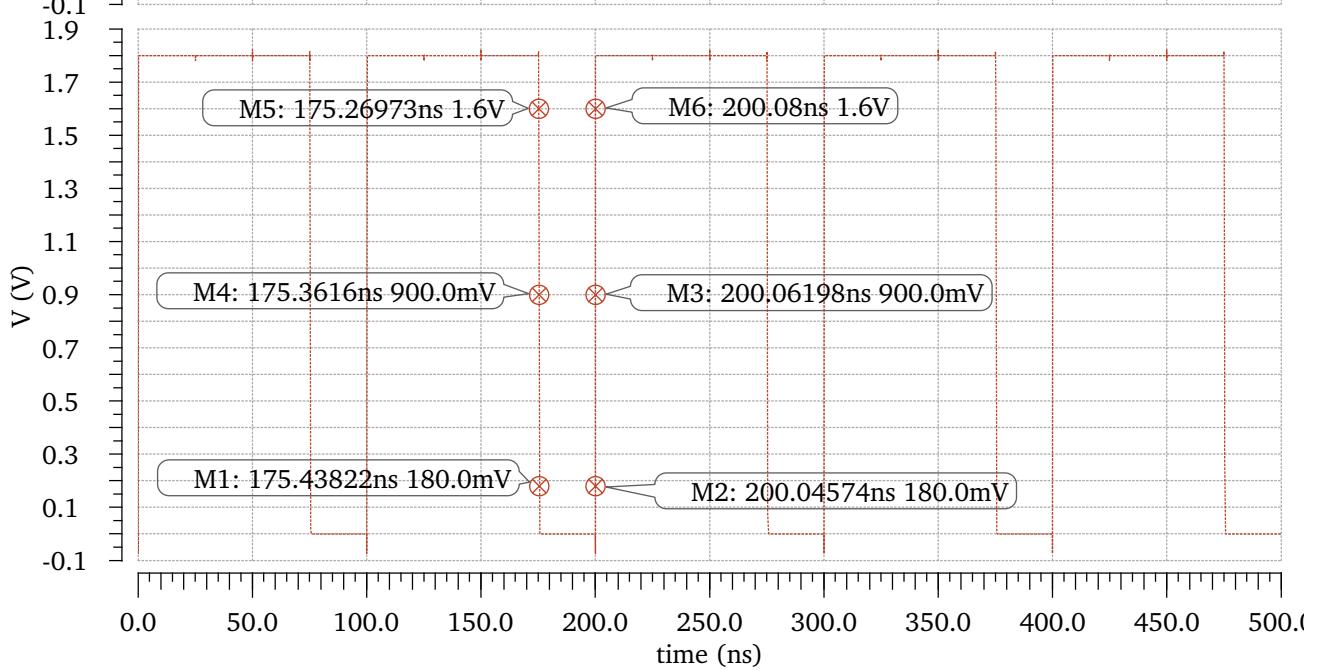
■ /IN2

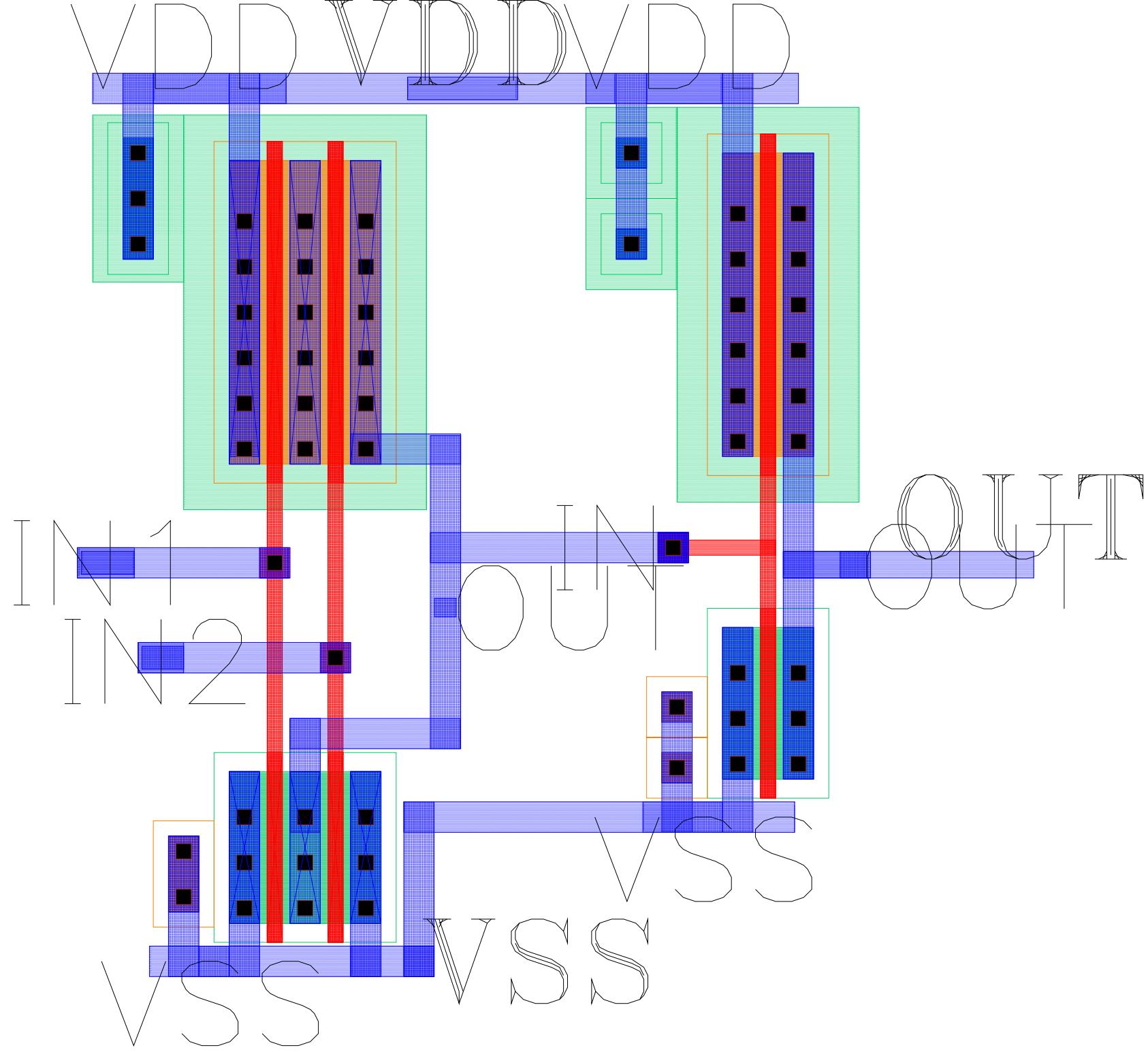


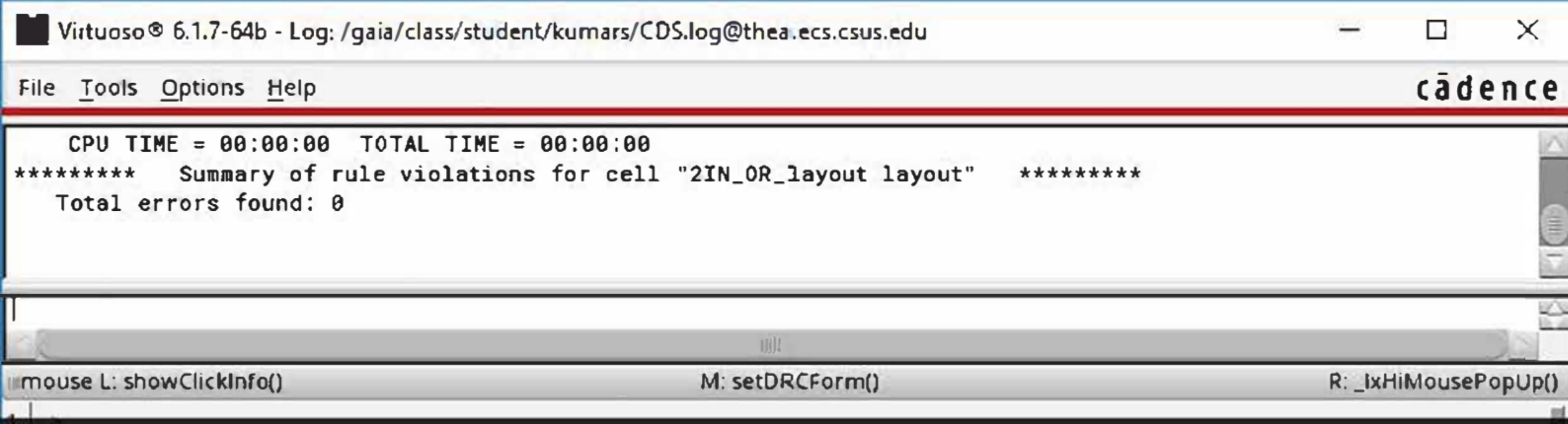
■ /IN1



■ /OUT







2 Input OR gate

@(#) \$CDS: LVS version 6.1.7-64b 09/27/2016 19:41 (sjfhw305) \$

Command line: /software/cadence/install/IC617/tools.lnx86/dfII/bin/64bit/LVS -dir
/gaia/class/student/kumars/EEE_234_share/LVS -l -s -t /gaia/class/student/kumars/EEE_234_share/LVS/layout
/gaia/class/student/kumars/EEE_234_share/LVS/schematic

Like matching is enabled.

Net swapping is enabled.

Using terminal names as correspondence points.

Net-list summary for /gaia/class/student/kumars/EEE_234_share/LVS/layout/netlist

count

| | |
|---|-----------|
| 7 | nets |
| 5 | terminals |
| 3 | pmos |
| 3 | nmos |

Net-list summary for /gaia/class/student/kumars/EEE_234_share/LVS/schematic/netlist

count

| | |
|---|-----------|
| 7 | nets |
| 5 | terminals |
| 3 | pmos |
| 3 | nmos |

Terminal correspondence points

| | | |
|----|----|-----|
| N5 | N1 | IN1 |
| N4 | N5 | IN2 |
| N3 | N2 | OUT |
| N6 | N3 | VDD |
| N2 | N0 | VSS |

Devices in the netlist but not in the rules:

pmos nmos

The net-lists match.

| | layout | schematic |
|-------------|-----------|-----------|
| | instances | |
| un-matched | 0 | 0 |
| rewired | 0 | 0 |
| size errors | 0 | 0 |
| pruned | 0 | 0 |
| active | 6 | 6 |
| total | 6 | 6 |

| | nets | |
|------------|------|---|
| un-matched | 0 | 0 |
| merged | 0 | 0 |
| pruned | 0 | 0 |
| active | 7 | 7 |
| total | 7 | 7 |

terminals

2 Input OR gate

| | | |
|-------------------------------|---|---|
| un-matched | 0 | 0 |
| matched but different type | 0 | 0 |
| total | 5 | 5 |

Probe files from /gaia/class/student/kumars/EEE_234_share/LVS/schematic

devbad.out:

netbad.out:

mergenet.out:

termbad.out:

prunenet.out:

prunedev.out:

audit.out:

Probe files from /gaia/class/student/kumars/EEE_234_share/LVS/layout

devbad.out:

netbad.out:

mergenet.out:

termbad.out:

prunenet.out:

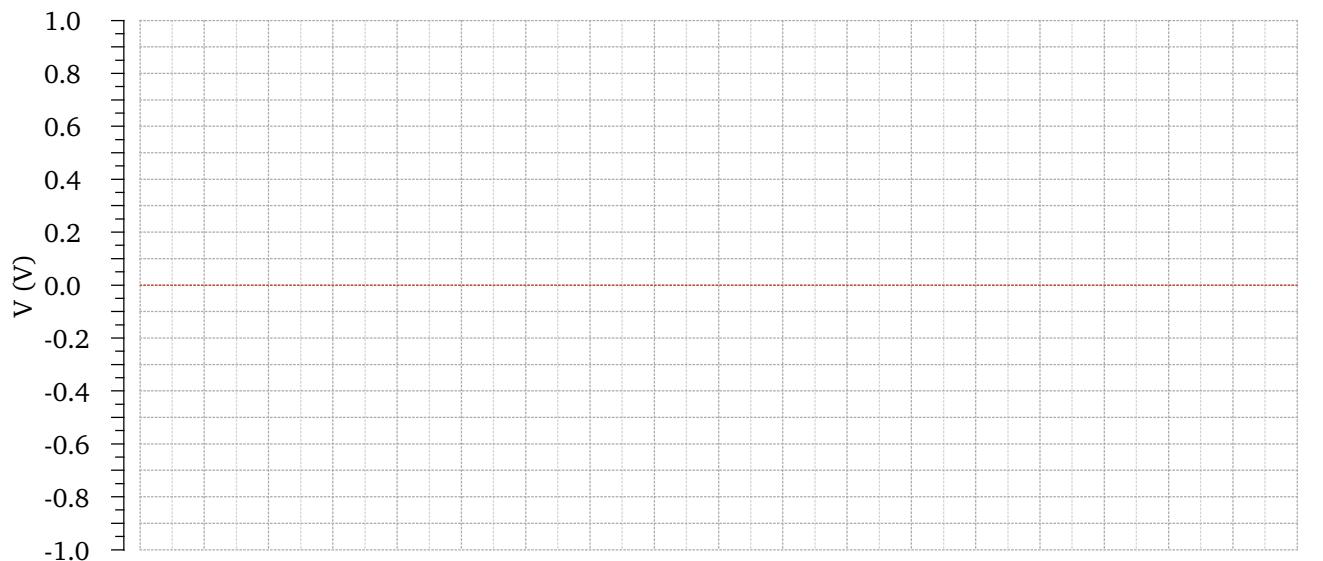
prunedev.out:

audit.out:

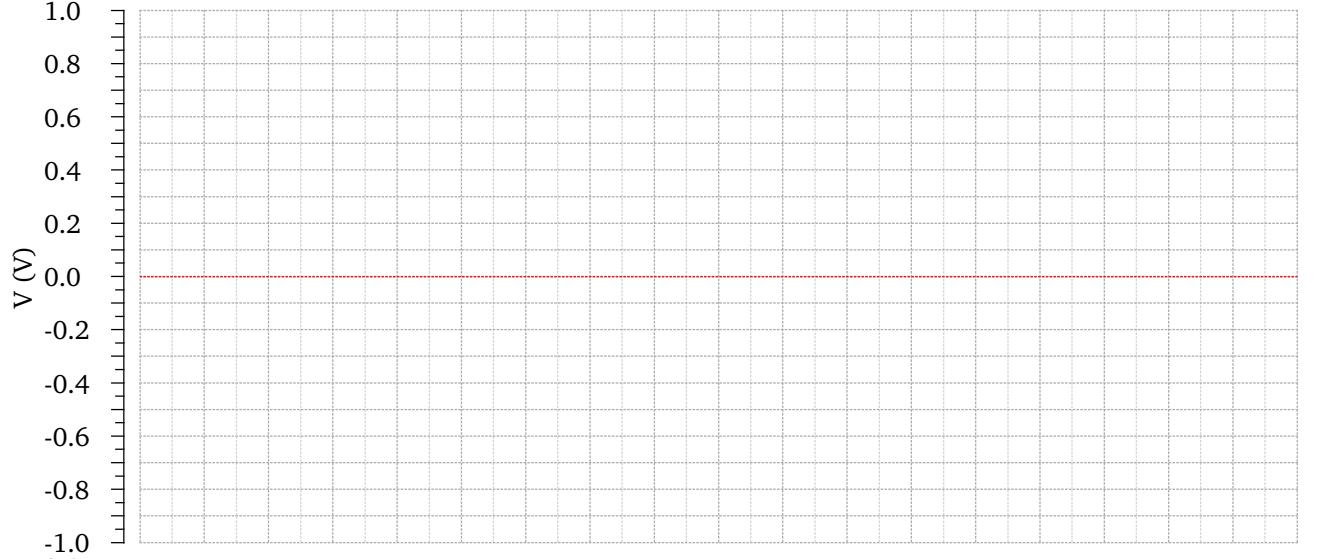
2 Input OR gate**Sat Dec 1 14:28:35 2018****DC Response**

Name Vis

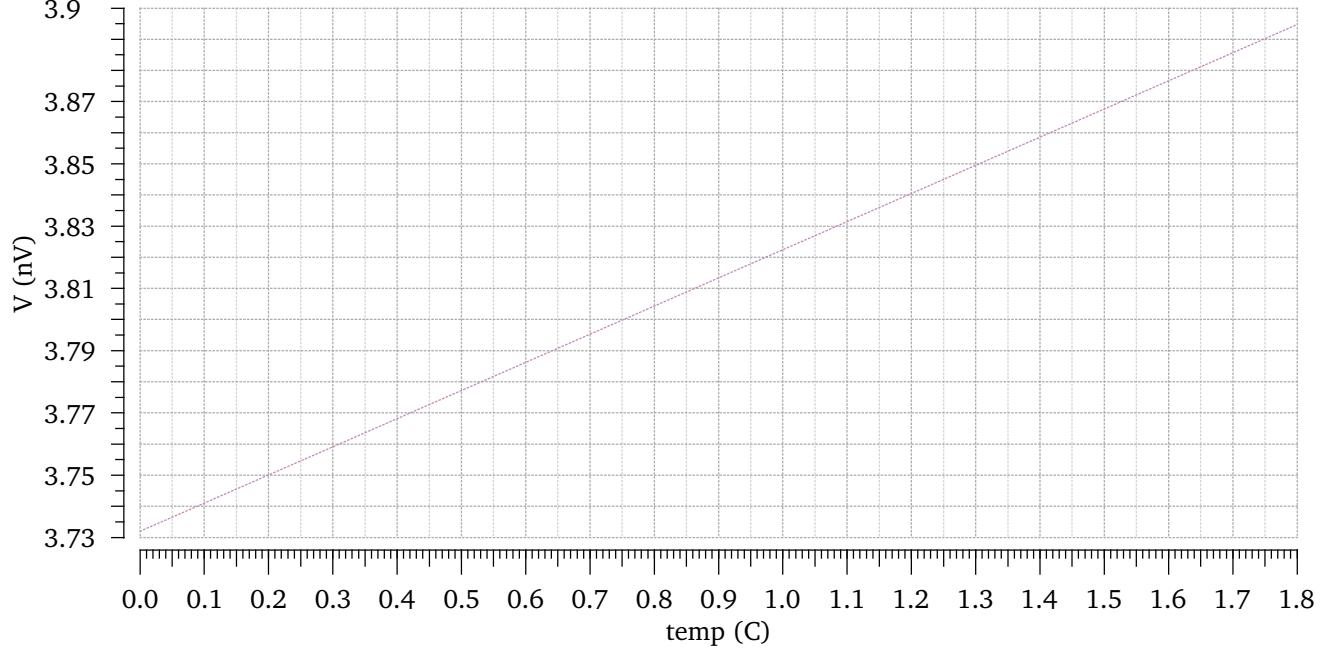
■ /IN1



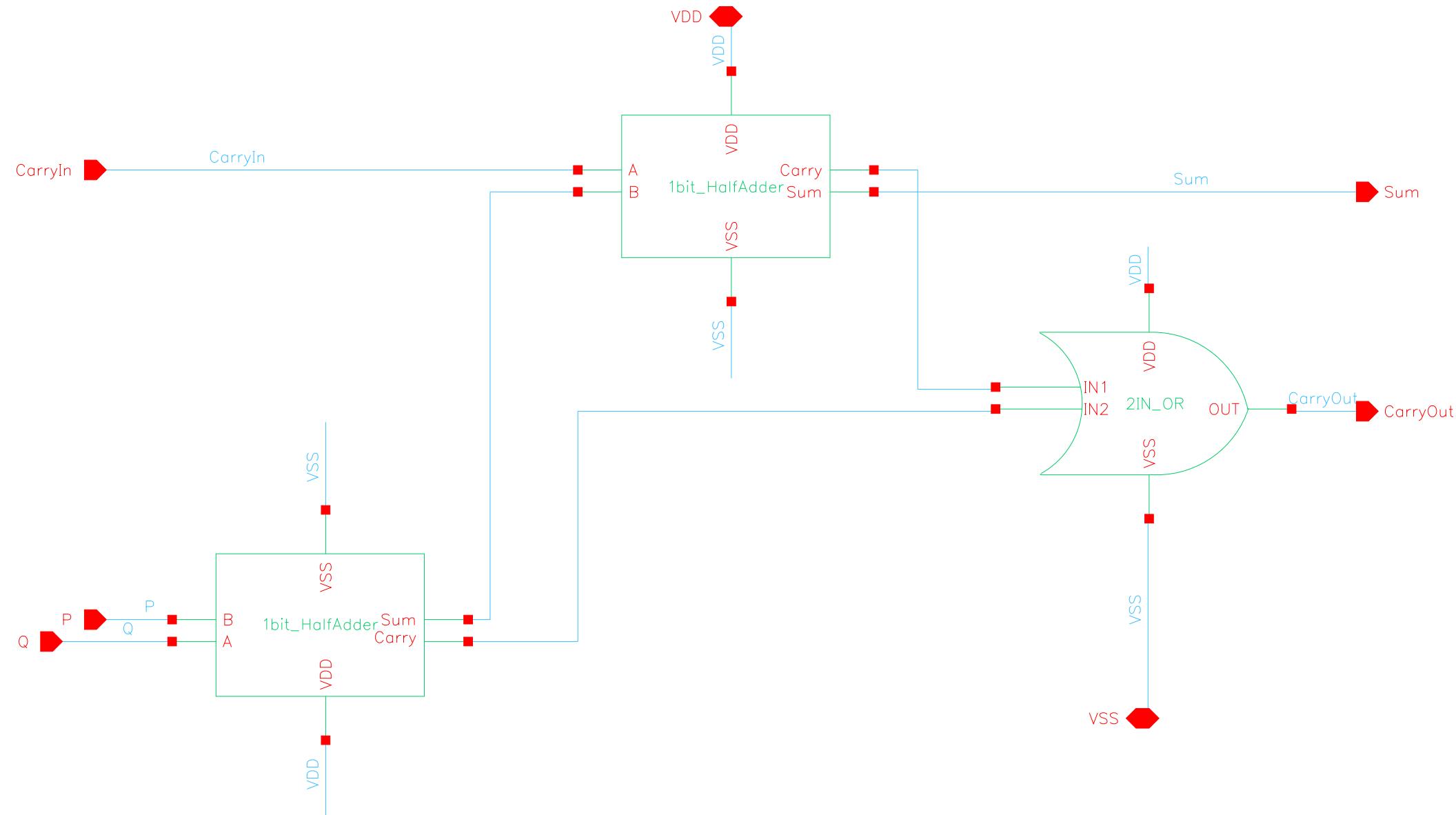
■ /IN2

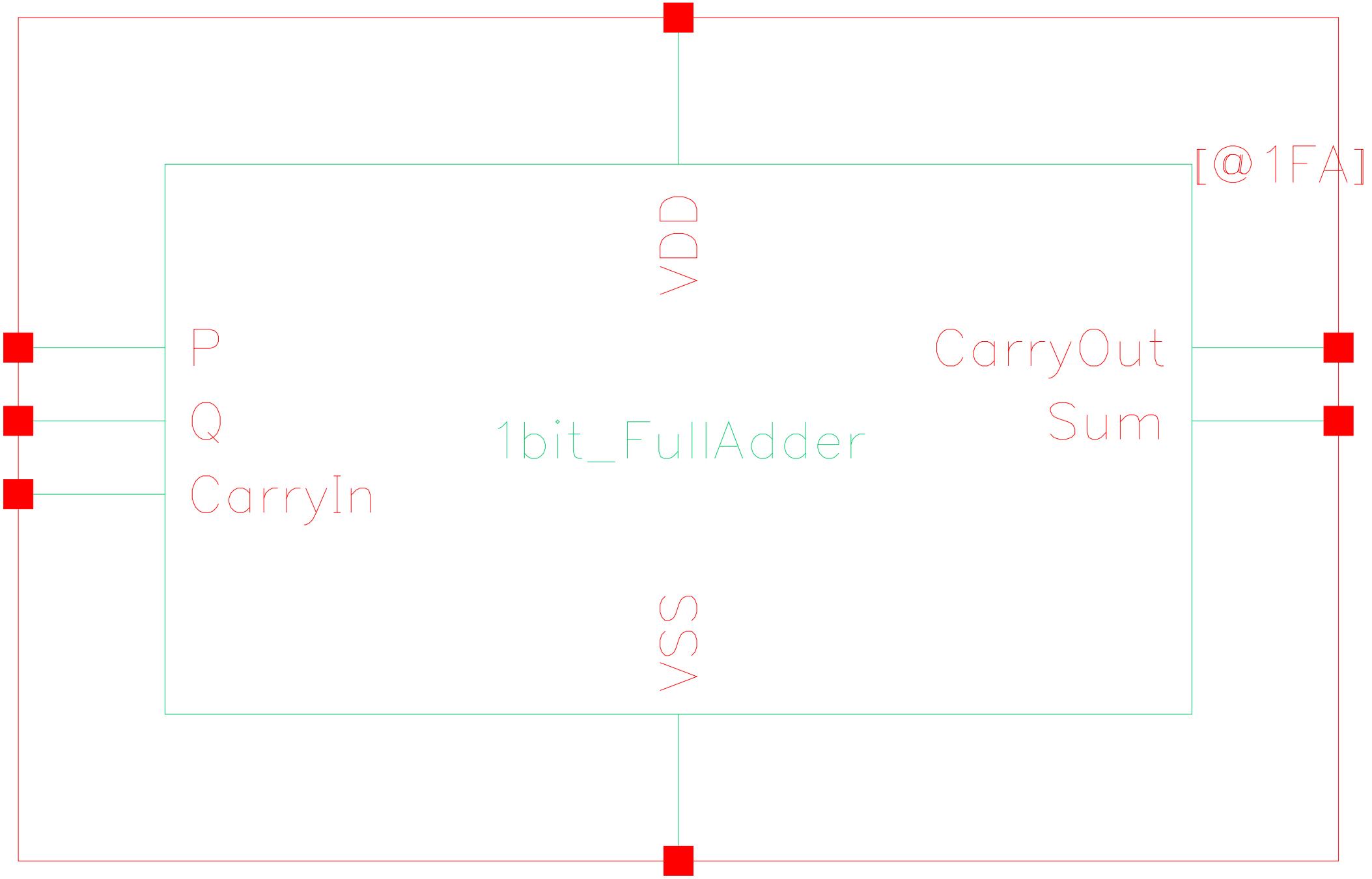


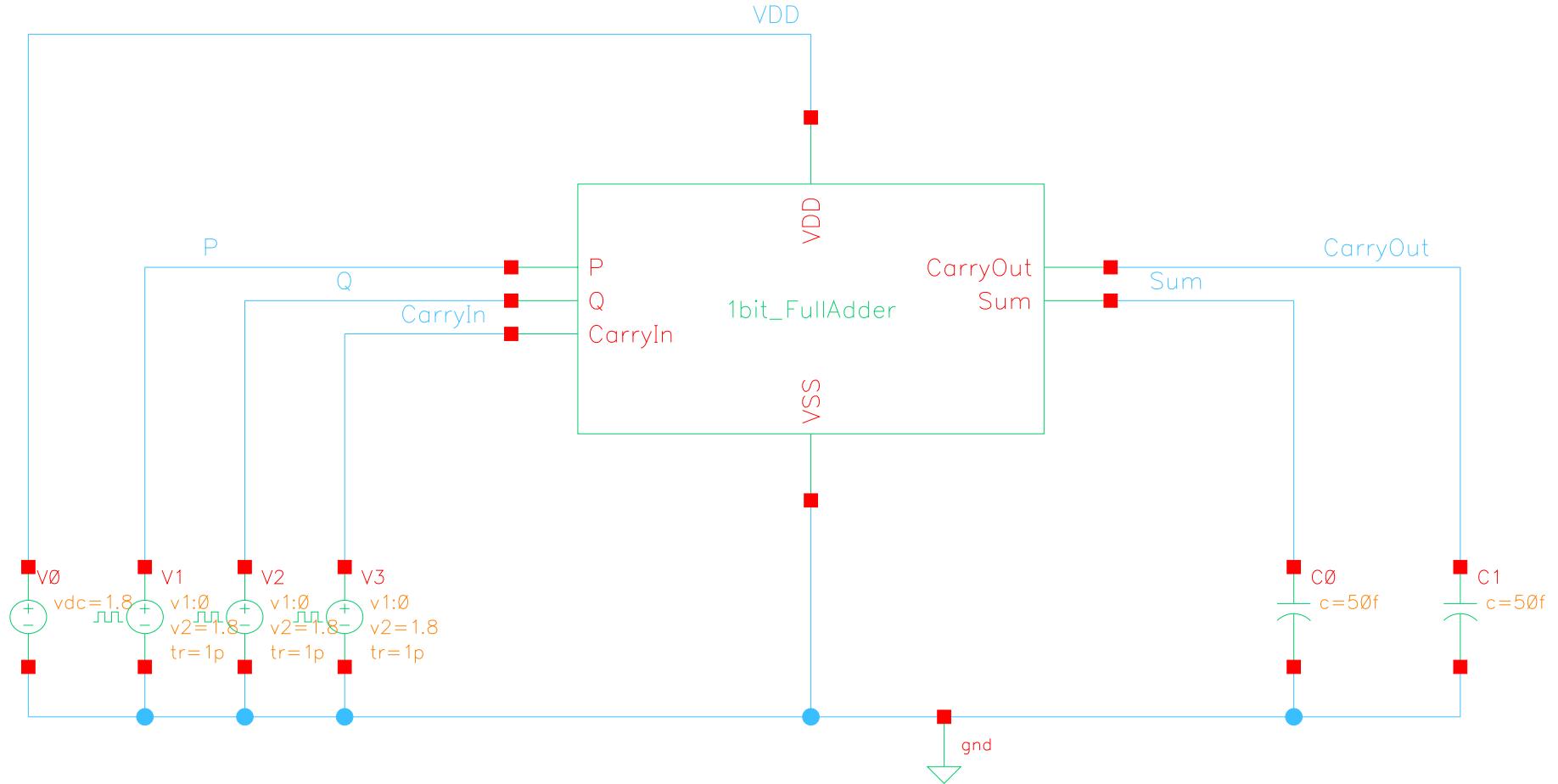
■ /OUT

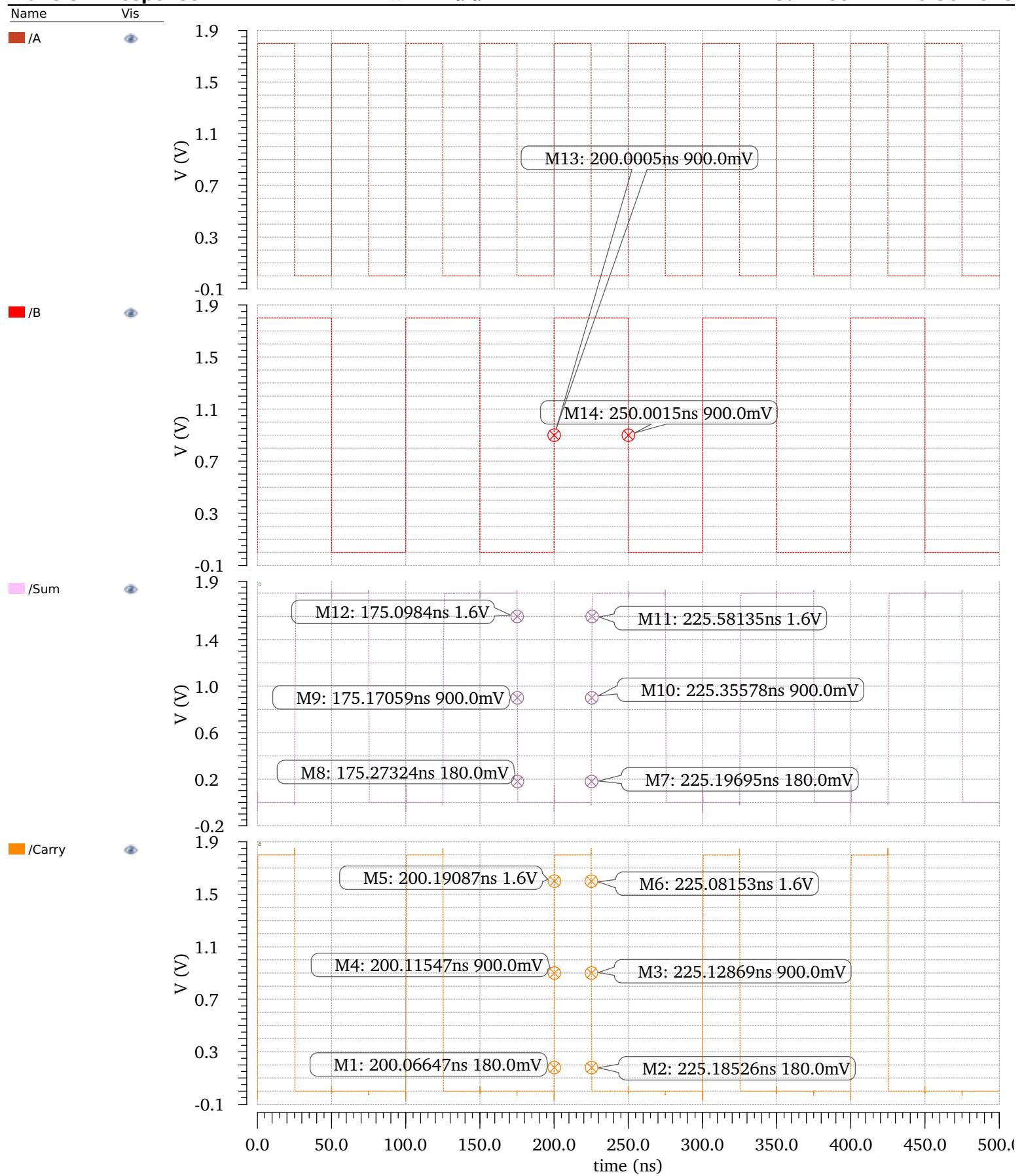


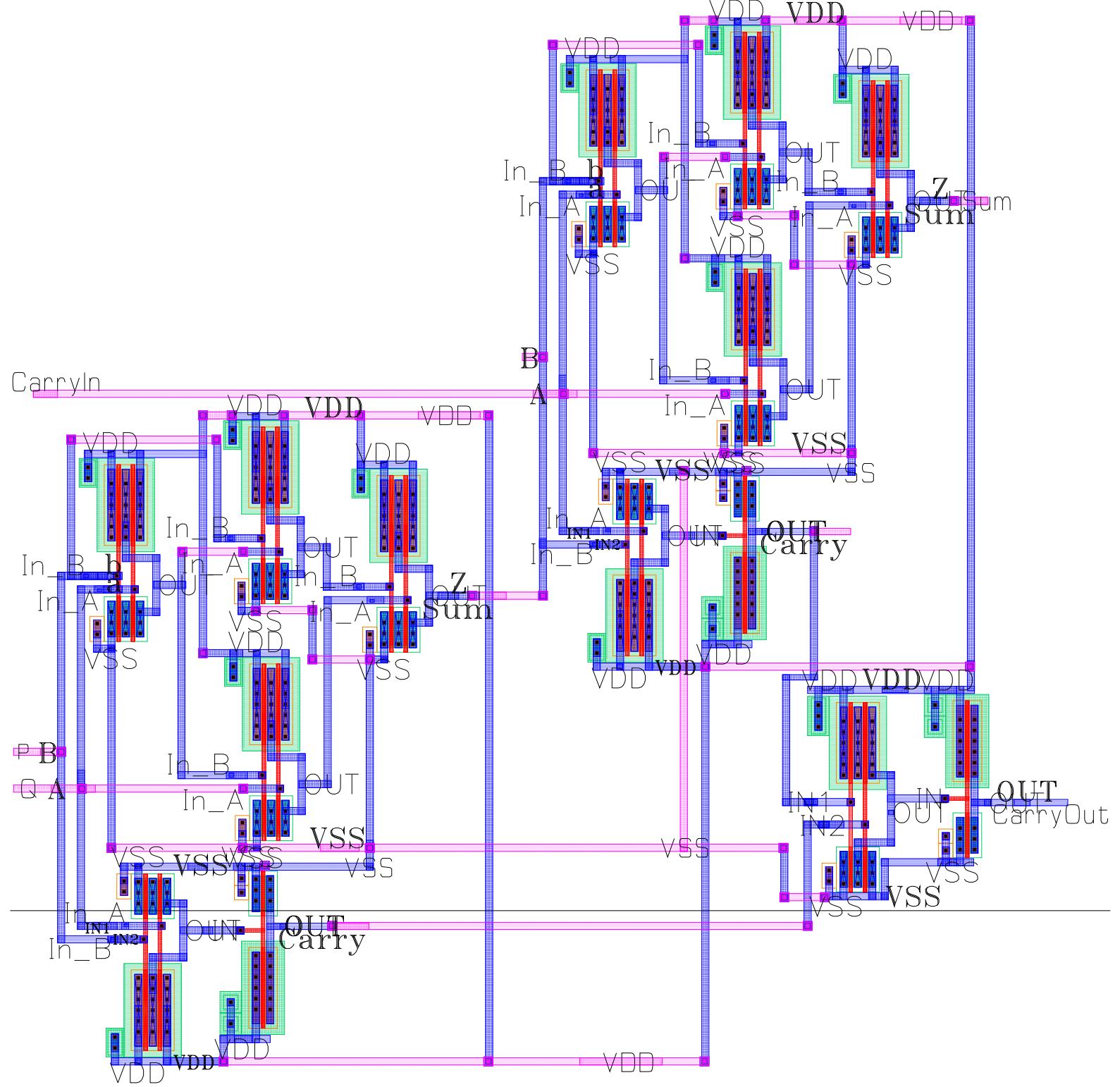
1 Bit Half Adder







Transient Response**1 Bit Half Adder****Sat Dec 1 12:10:36 2018**



File Tools Options Help

cadence

CPU TIME = 00:00:00 TOTAL TIME = 00:00:00

***** Summary of rule violations for cell "1bit_HalfAdder_layout layout" *****

Total errors found: 0

...mouse L: showClickInfo()

M: setDRCForm()

R: _IxHiMousePopUp()

1 >

1 Bit Half Adder

@(#) \$CDS: LVS version 6.1.7-64b 09/27/2016 19:41 (sjfhw305) \$

Command line: /software/cadence/install/IC617/tools.lnx86/dfII/bin/64bit/LVS -dir
/gaia/class/student/kumars/EEE_234_share/LVS -l -s -t /gaia/class/student/kumars/EEE_234_share/LVS/layout
/gaia/class/student/kumars/EEE_234_share/LVS/schematic

Link matching is enabled.

Net swapping is enabled.

Using terminal names as correspondence points.

Net-list summary for /gaia/class/student/kumars/EEE_234_share/LVS/layout/netlist

| count | |
|-------|-----------|
| 15 | nets |
| 6 | terminals |
| 11 | pmos |
| 11 | nmos |

Net-list summary for /gaia/class/student/kumars/EEE_234_share/LVS/schematic/netlist

| count | |
|-------|-----------|
| 15 | nets |
| 6 | terminals |
| 11 | pmos |
| 11 | nmos |

Terminal correspondence points

| | | |
|-----|----|-------|
| N11 | N5 | A |
| N10 | N3 | B |
| N14 | N4 | Carry |
| N12 | N1 | Sum |
| N13 | N2 | VDD |
| N9 | N0 | VSS |

Devices in the netlist but not in the rules:

pmos nmos

The net-lists match.

| | layout | schematic |
|-------------|-----------|-----------|
| | instances | |
| un-matched | 0 | 0 |
| rewired | 0 | 0 |
| size errors | 0 | 0 |
| pruned | 0 | 0 |
| active | 22 | 22 |
| total | 22 | 22 |

| | nets | |
|------------|------|----|
| un-matched | 0 | 0 |
| merged | 0 | 0 |
| pruned | 0 | 0 |
| active | 15 | 15 |
| total | 15 | 15 |

1 Bit Half Adder

terminals

| | | |
|----------------|---|---|
| un-matched | 0 | 0 |
| matched but | | |
| different type | 0 | 0 |
| total | 6 | 6 |

Probe files from /gaia/class/student/kumars/EEE_234_share/LVS/schematic

devbad.out:

netbad.out:

mergenet.out:

termbad.out:

prunenet.out:

prunedev.out:

audit.out:

Probe files from /gaia/class/student/kumars/EEE_234_share/LVS/layout

devbad.out:

netbad.out:

mergenet.out:

termbad.out:

prunenet.out:

prunedev.out:

audit.out:

DC Response

Name Vis

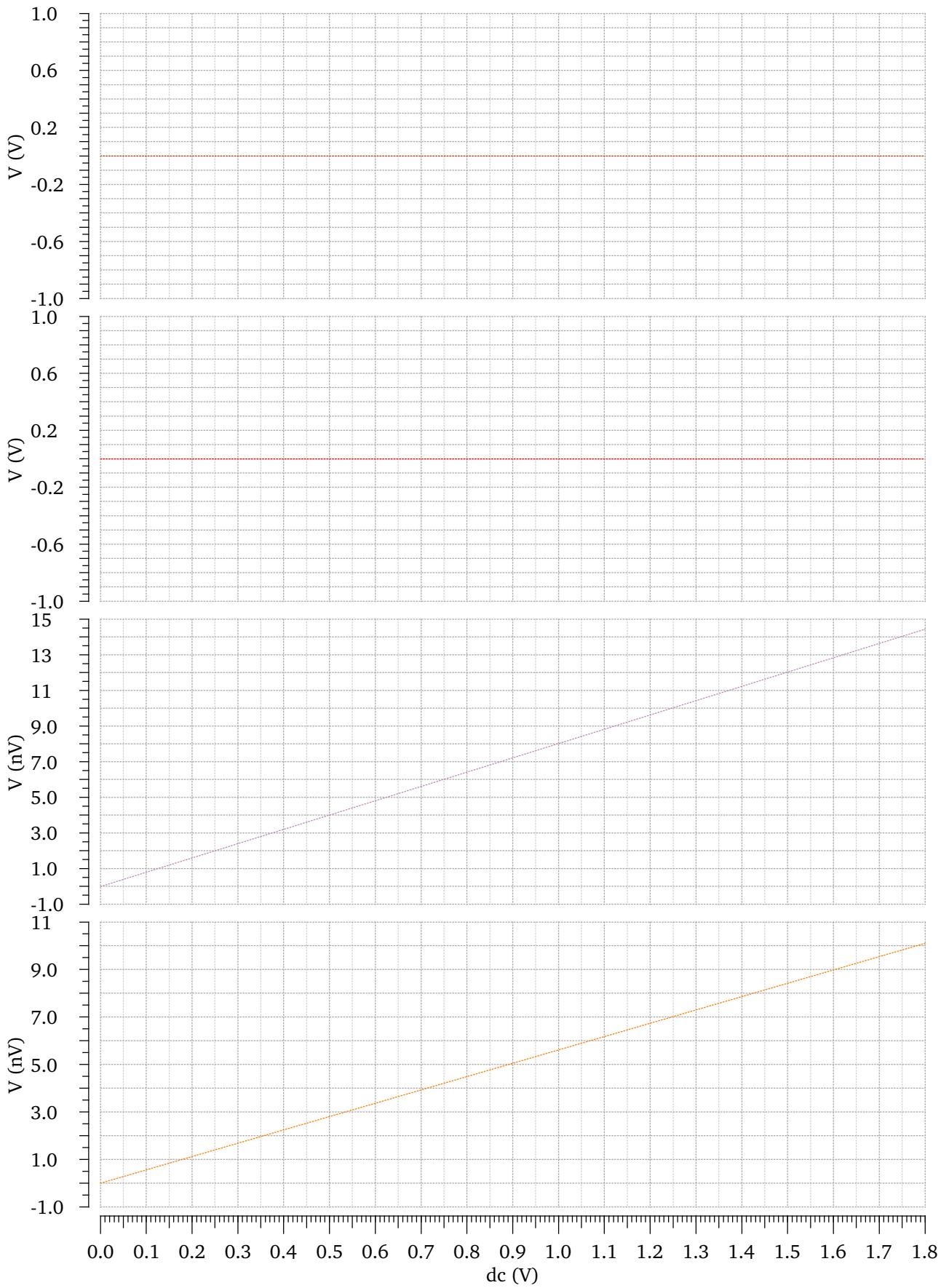
■ /A

1 Bit Half Adder**Sat Dec 1 14:26:57 2018**

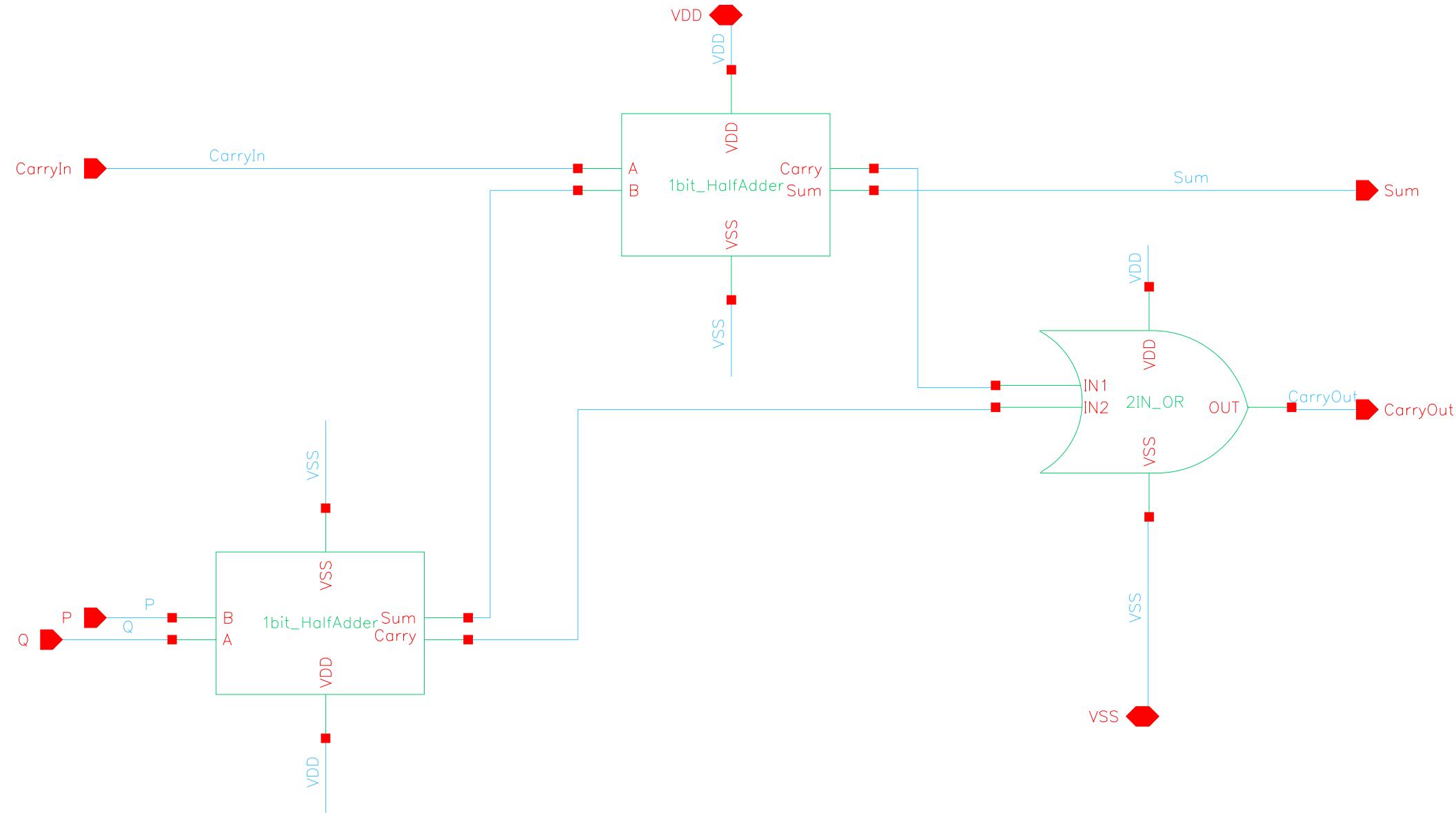
■ /B

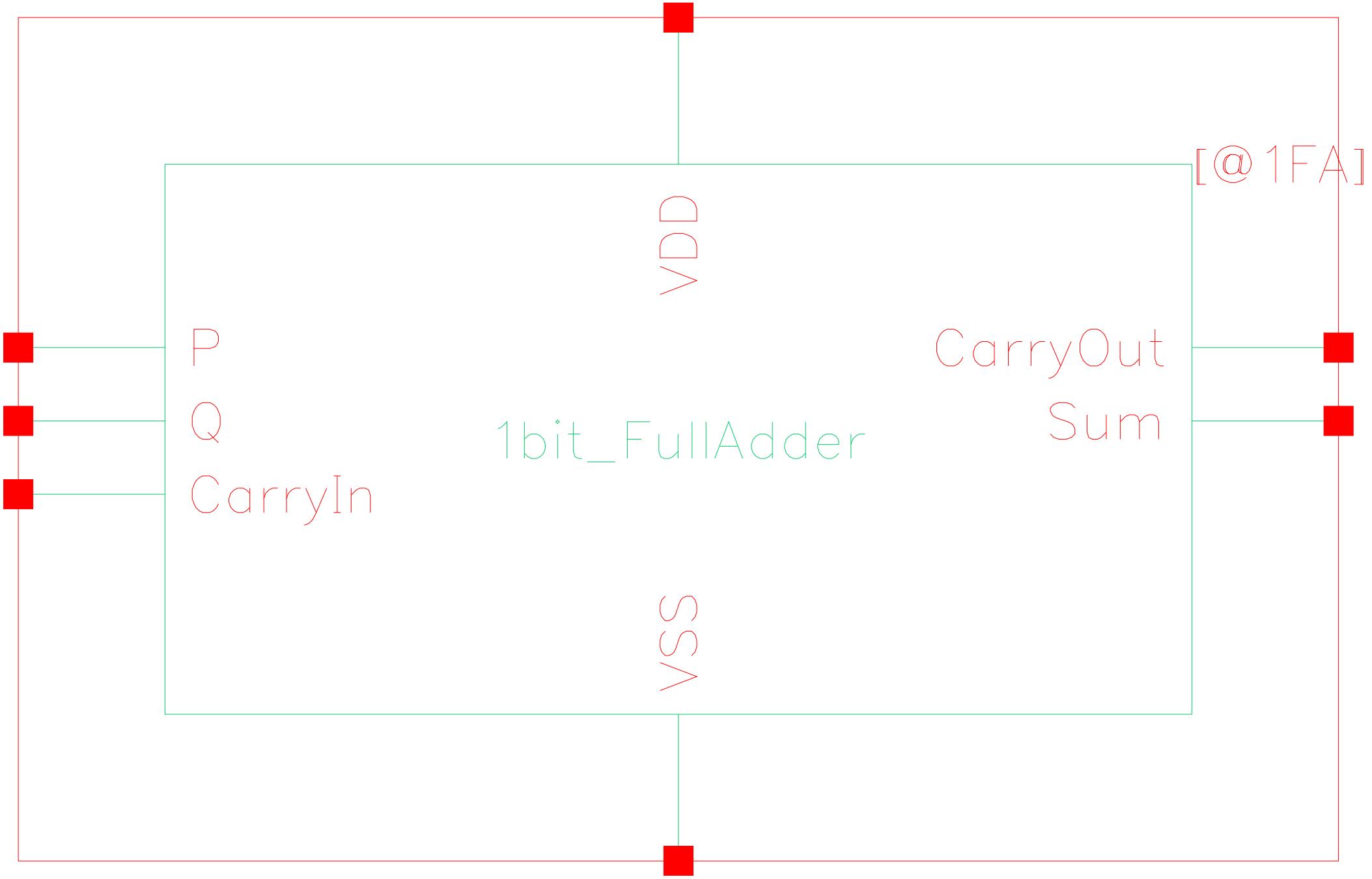
■ /Sum

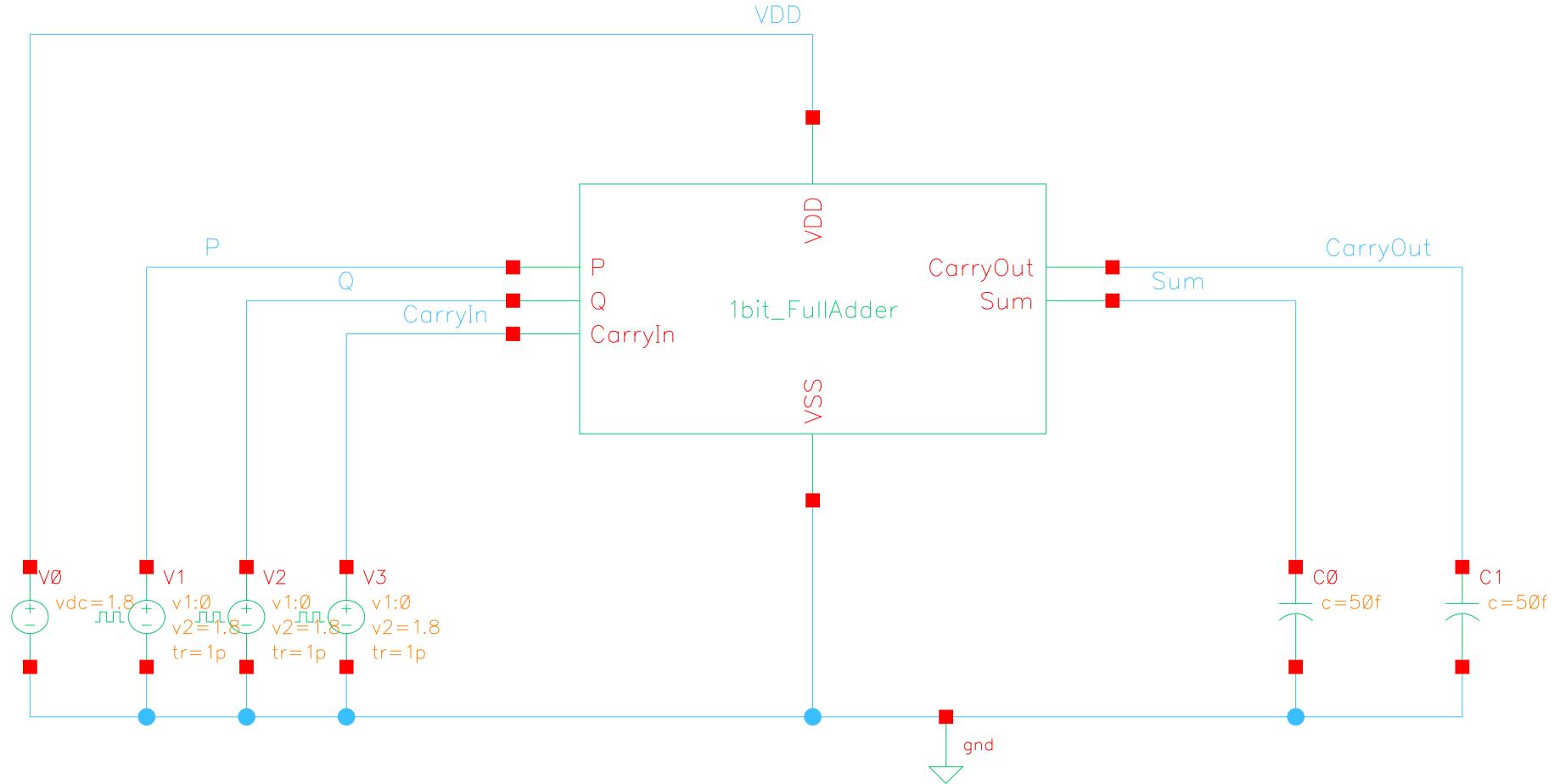
■ /Carry

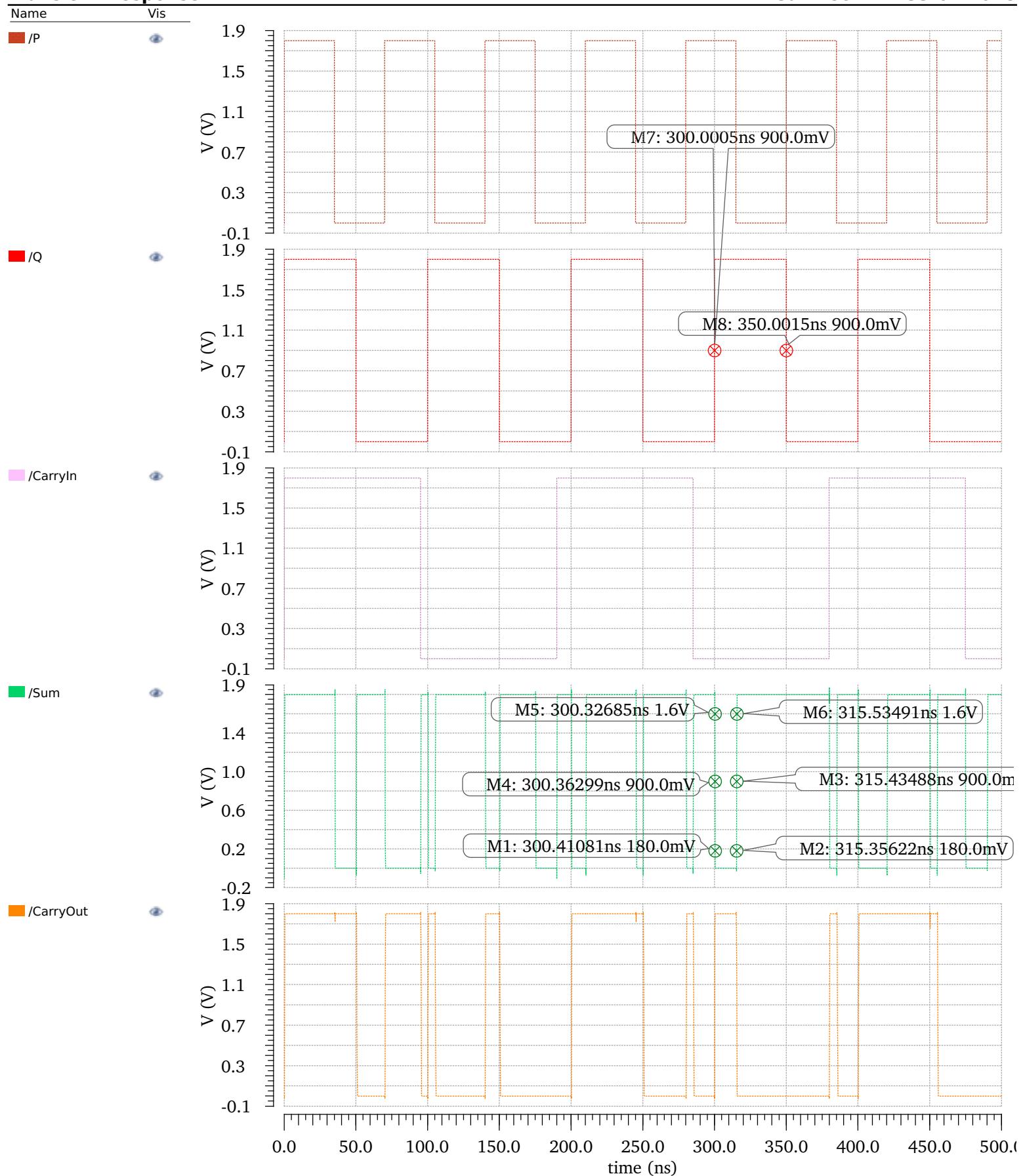


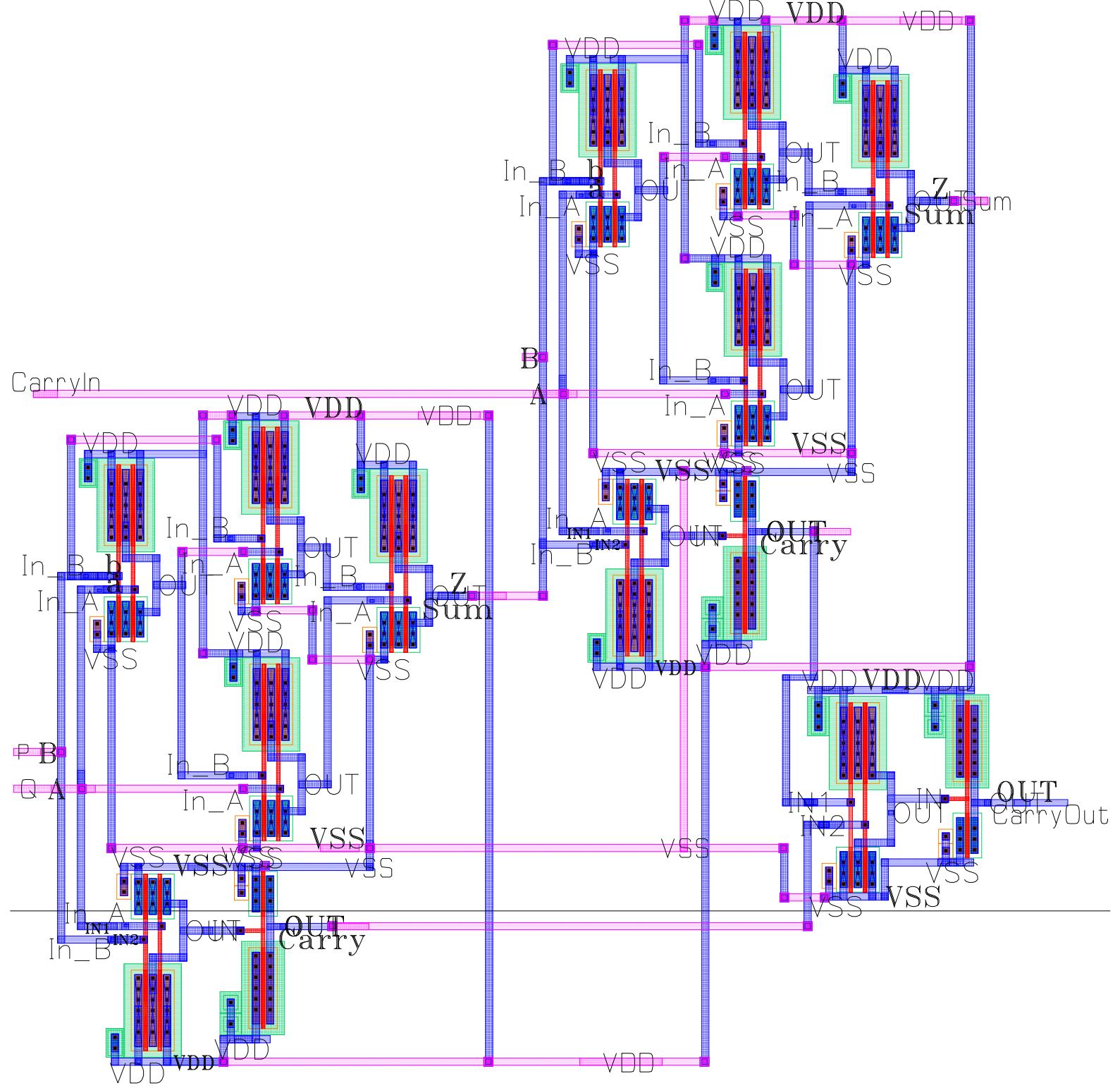
1 Bit Full Adder







Transient Response**1 Bit Full Adder****Sat Dec 1 12:33:02 2018**



File Tools Options Help

cādence

CPU TIME = 00:00:00 TOTAL TIME = 00:00:00

***** Summary of rule violations for cell "1bit_FullAdder_Layout layout" *****

Total errors found: 0

... mouse L: showClickInfo()

M: setDRCForm()

R: _IxHiMousePopUp()

1 Bit Full Adder

@(#) \$CDS: LVS version 6.1.7-64b 09/27/2016 19:41 (sjfhw305) \$

Command line: /software/cadence/install/IC617/tools.lnx86/dfII/bin/64bit/LVS -dir
/gaia/class/student/kumars/EEE_234_share/LVS -l -s -t /gaia/class/student/kumars/EEE_234_share/LVS/layout
/gaia/class/student/kumars/EEE_234_share/LVS/schematic

Like matching is enabled.

Net swapping is enabled.

Using terminal names as correspondence points.

Net-list summary for /gaia/class/student/kumars/EEE_234_share/LVS/layout/netlist

| count | |
|-------|-----------|
| 30 | nets |
| 7 | terminals |
| 25 | pmos |
| 25 | nmos |

Net-list summary for /gaia/class/student/kumars/EEE_234_share/LVS/schematic/netlist

| count | |
|-------|-----------|
| 30 | nets |
| 7 | terminals |
| 25 | pmos |
| 25 | nmos |

Terminal correspondence points

| | | |
|-----|----|----------|
| N28 | N8 | CarryIn |
| N27 | N2 | CarryOut |
| N25 | N4 | P |
| N24 | N1 | Q |
| N26 | N7 | Sum |
| N29 | N3 | VDD |
| N23 | N9 | VSS |

Devices in the netlist but not in the rules:

pmos nmos

The net-lists match.

| | layout | schematic |
|-------------|-----------|-----------|
| | instances | |
| un-matched | 0 | 0 |
| rewired | 0 | 0 |
| size errors | 0 | 0 |
| pruned | 0 | 0 |
| active | 50 | 50 |
| total | 50 | 50 |

| | nets | |
|------------|------|----|
| un-matched | 0 | 0 |
| merged | 0 | 0 |
| pruned | 0 | 0 |
| active | 30 | 30 |
| total | 30 | 30 |

1 Bit Full Adder

terminals

| | | |
|----------------|---|---|
| un-matched | 0 | 0 |
| matched but | | |
| different type | 0 | 0 |
| total | 7 | 7 |

Probe files from /gaia/class/student/kumars/EEE_234_share/LVS/schematic

devbad.out:

netbad.out:

mergenet.out:

termbad.out:

prunenet.out:

prunedev.out:

audit.out:

Probe files from /gaia/class/student/kumars/EEE_234_share/LVS/layout

devbad.out:

netbad.out:

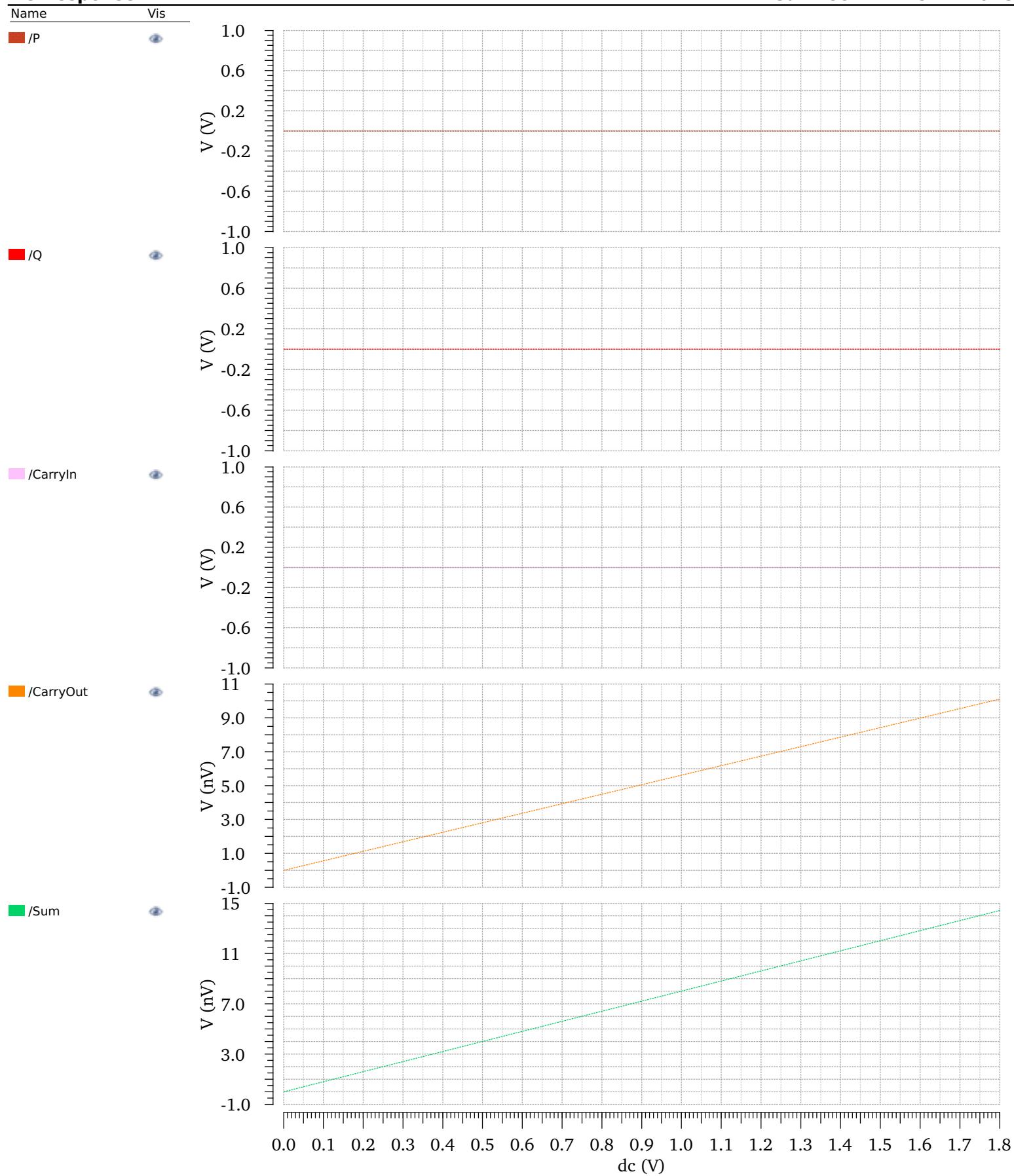
mergenet.out:

termbad.out:

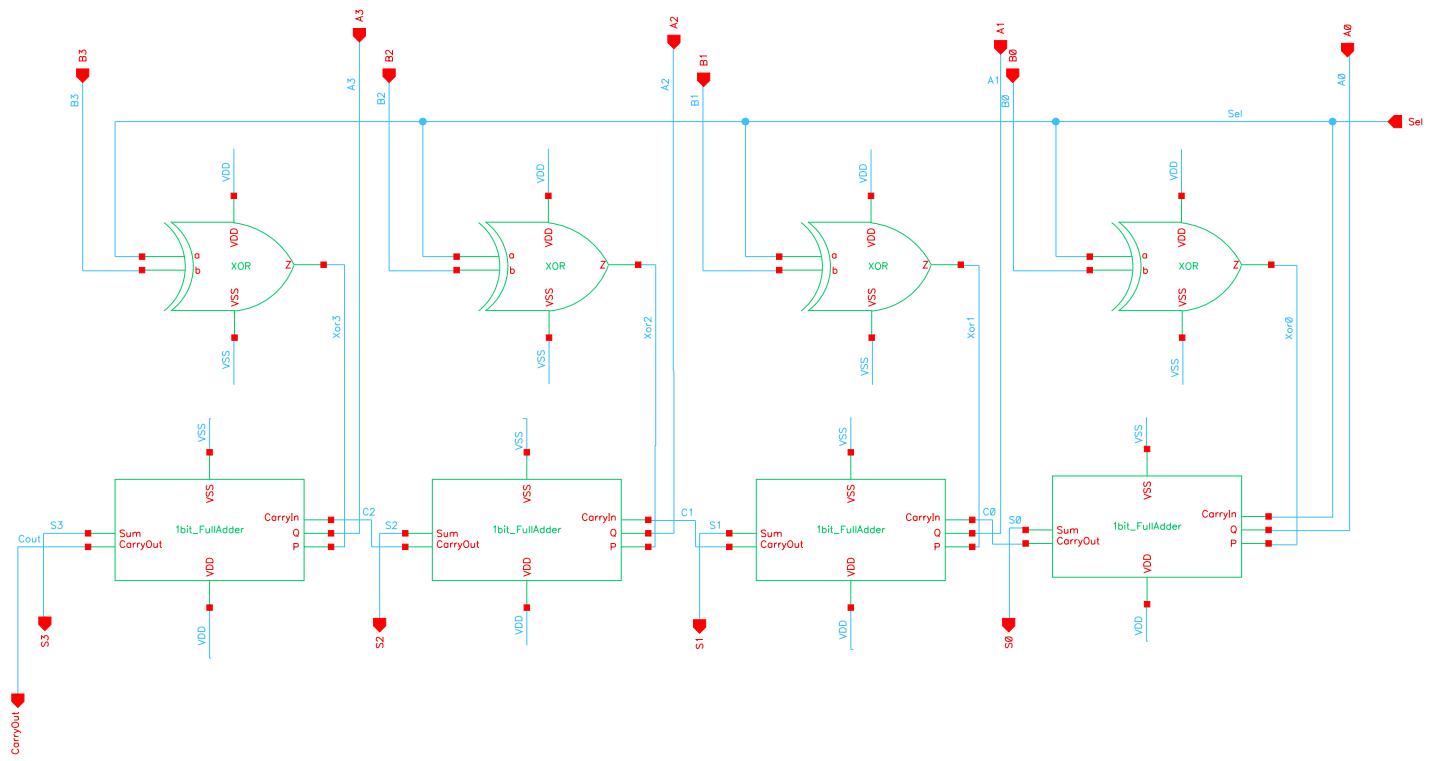
prunenet.out:

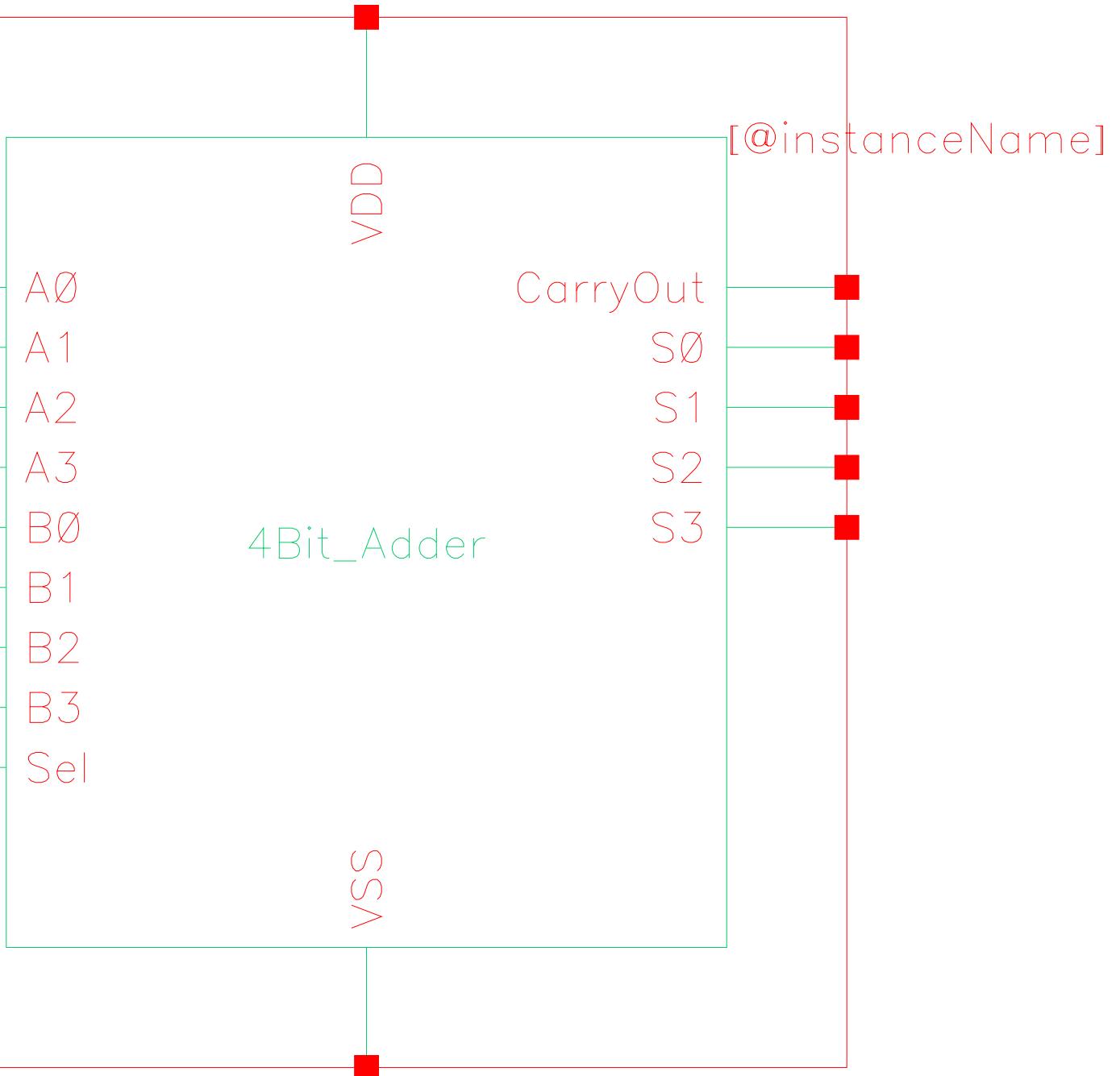
prunedev.out:

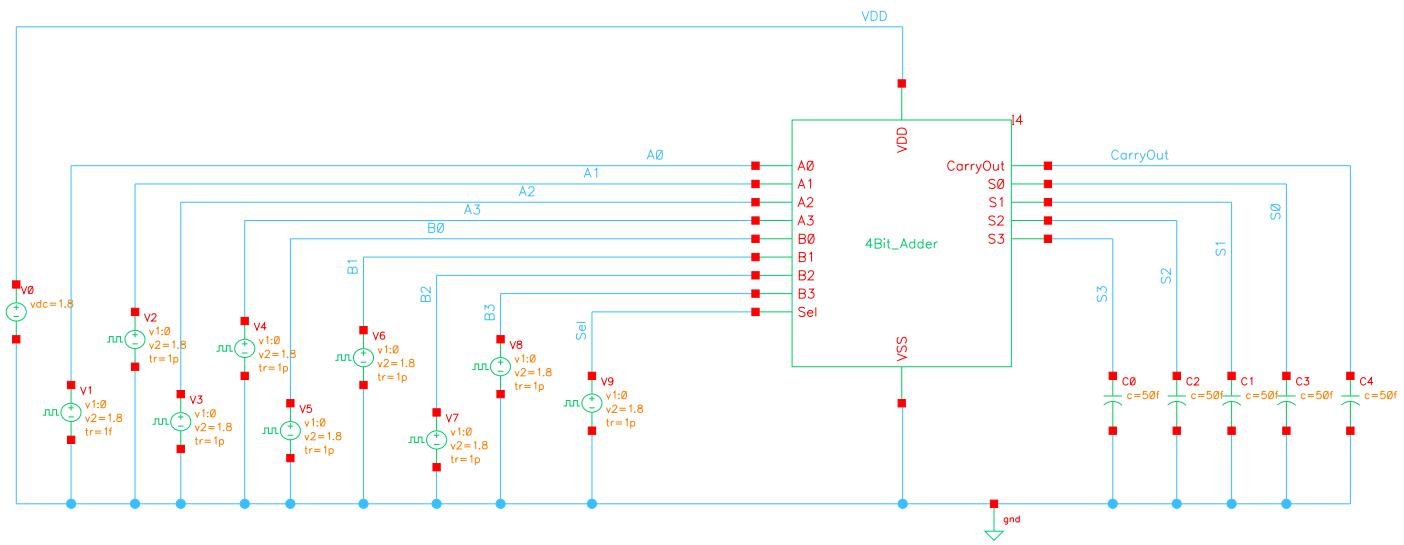
audit.out:

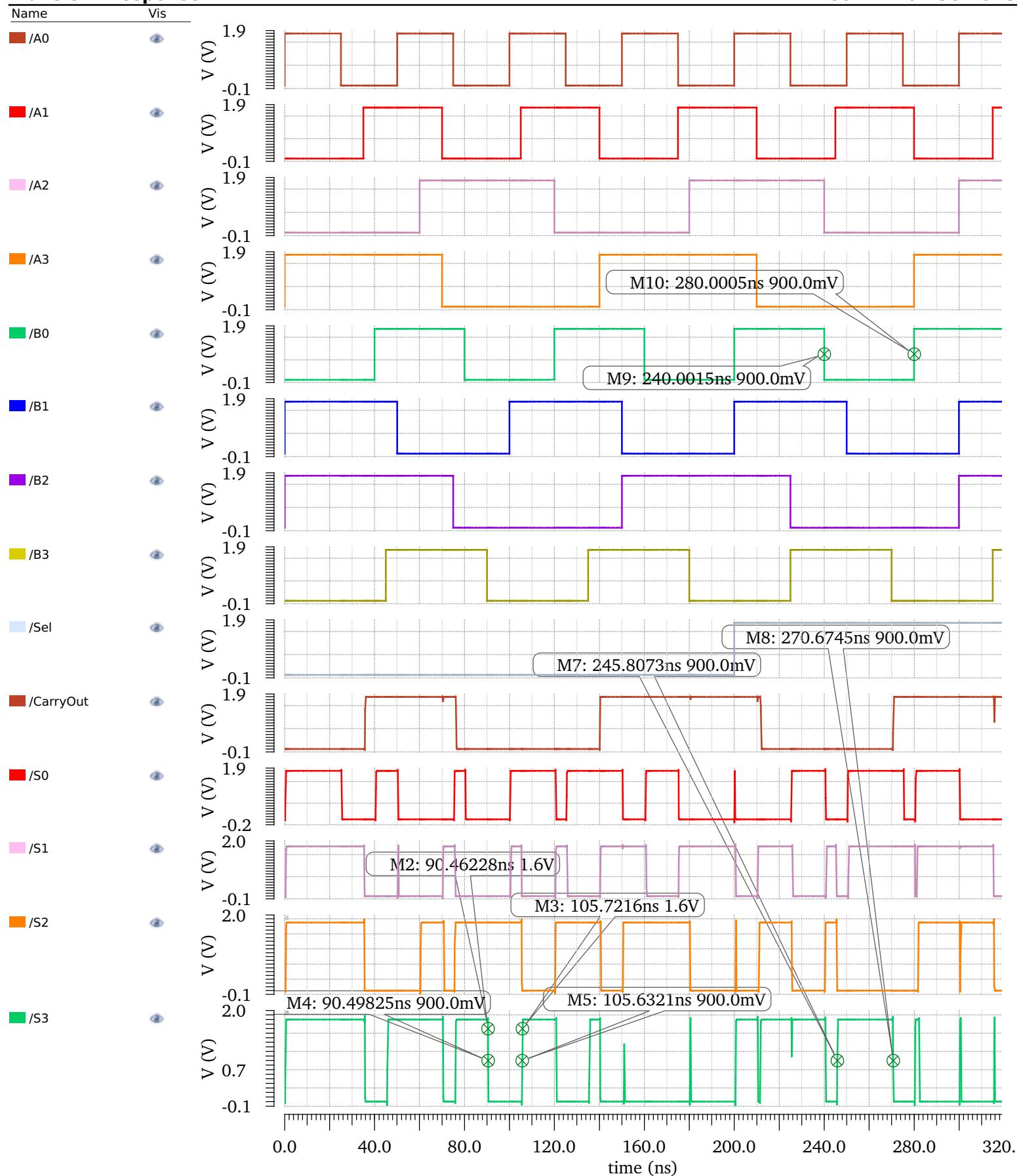
DC Response**1 Bit Full Adder****Sat Dec 1 14:25:41 2018**

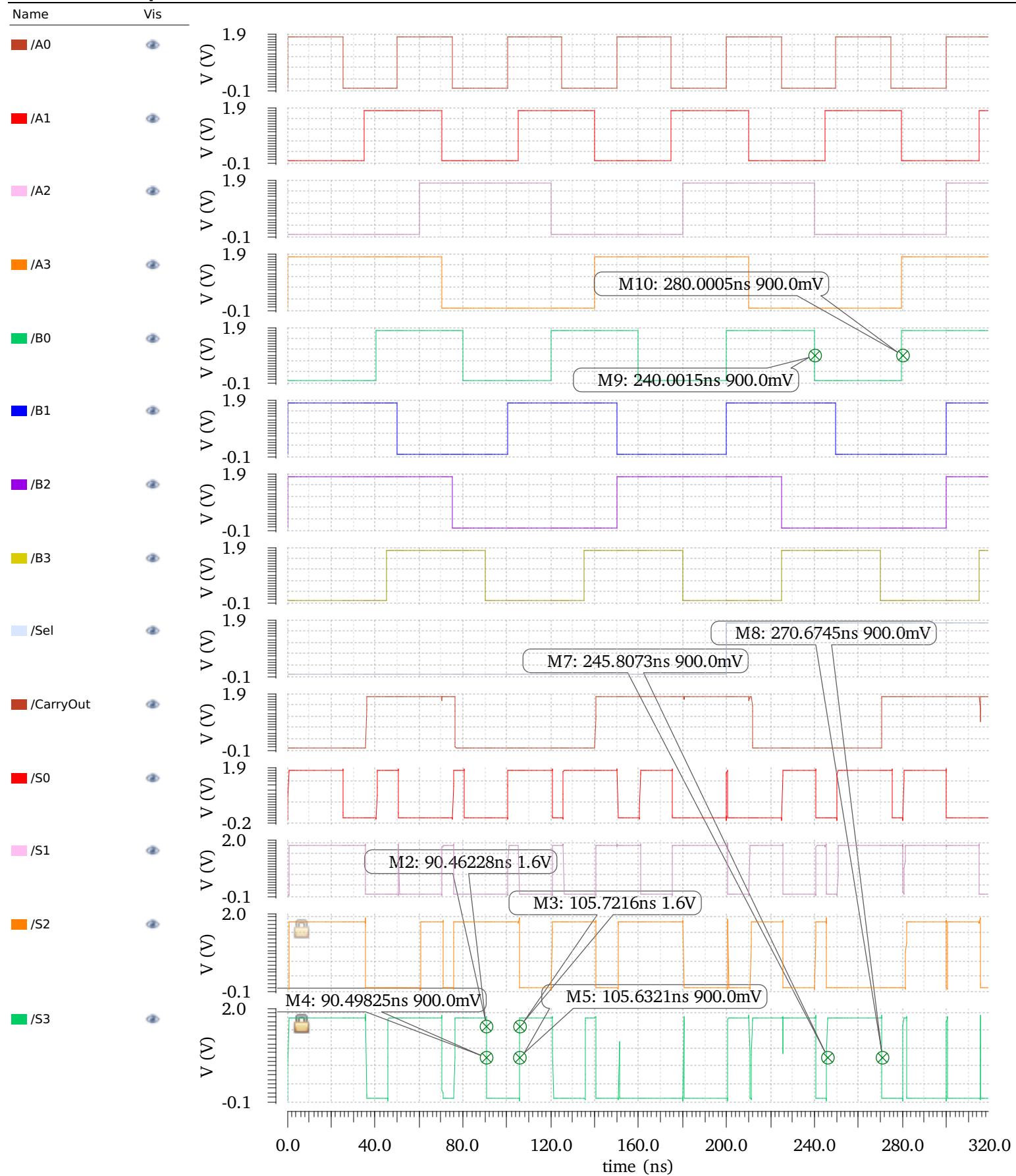
4 Bit Adder

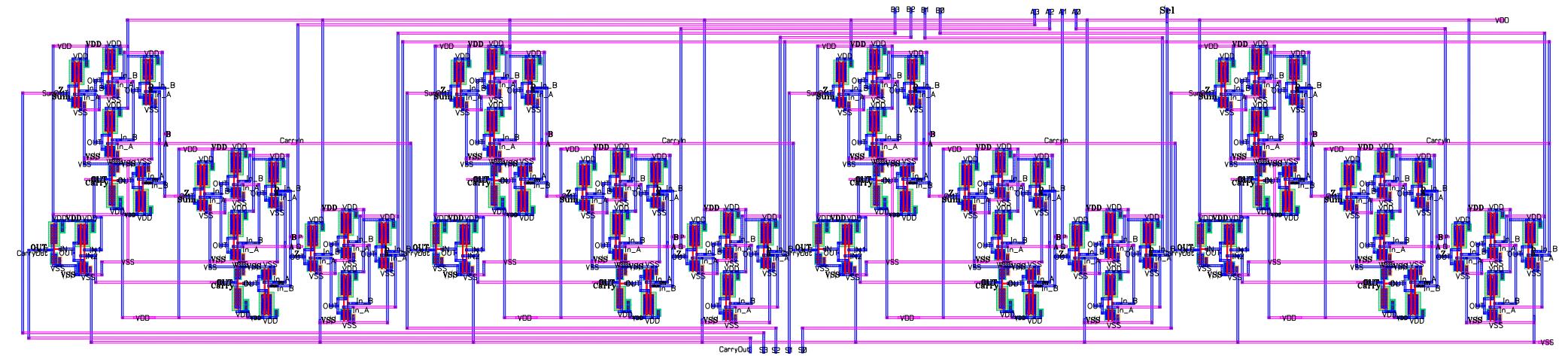






Transient Response**4 Bit Adder Waveform****Fri Dec 7 22:04:38 2018**

Transient Response**4 Bit- Adder Waveform****Fri Dec 7 22:04:38 2018**



File Tools Options Help

cadence

DRC started..... Sun Dec 2 17:55:51 2018

completed Sun Dec 2 17:55:52 2018

CPU TIME = 00:00:00 TOTAL TIME = 00:00:01

***** Summary of rule violations for cell "4Bit_Adder_layout layout" *****

Total errors found: 0

mouse L:showClickInfo()

M: setDRCForm()

R: _IxHiMousePopUp()

```
@(#)$CDS: LVS version 6.1.7-64b 09/27/2016 19:41 (sjfhw305) $
```

```
Command line: /software/cadence/install/IC617/tools.lnx86/dfII/bin/64bit/LVS -dir  
/gaia/class/student/mahajanm/EEE_234_Project1/LVS -l -s -t  
/gaia/class/student/mahajanm/EEE_234_Project1/LVS/layout  
/gaia/class/student/mahajanm/EEE_234_Project1/LVS/schematic
```

Like matching is enabled.

Net swapping is enabled.

Using terminal names as correspondence points.

Compiling Diva LVS rules...

```
Net-list summary for /gaia/class/student/mahajanm/EEE_234_Project1/LVS/layout/netlist
```

```
count  
143      nets  
16       terminals  
132      pmos  
132      nmos
```

```
Net-list summary for /gaia/class/student/mahajanm/EEE_234_Project1/LVS/schematic/netlist
```

```
count  
143      nets  
16       terminals  
132      pmos  
132      nmos
```

Terminal correspondence points

```
N133  N0   A0  
N132  N22  A1  
N131  N6   A2  
N130  N7   A3  
N141  N8   B0  
N140  N10  B1
```

| | | |
|------|-----|----------|
| N139 | N12 | B2 |
| N137 | N14 | B3 |
| N136 | N15 | CarryOut |
| N129 | N19 | S0 |
| N128 | N17 | S1 |
| N127 | N11 | S2 |
| N142 | N18 | S3 |
| N135 | N1 | Sel |
| N138 | N21 | VDD |
| N134 | N9 | VSS |

Devices in the rules but not in the netlist:

```
cap nfet pfet nmos4 pmos4
```

The net-lists match.

| | layout | schematic |
|-------------|-----------|-----------|
| | instances | |
| un-matched | 0 | 0 |
| rewired | 0 | 0 |
| size errors | 0 | 0 |
| pruned | 0 | 0 |
| active | 264 | 264 |
| total | 264 | 264 |

| | nets | |
|------------|------|-----|
| un-matched | 0 | 0 |
| merged | 0 | 0 |
| pruned | 0 | 0 |
| active | 143 | 143 |
| total | 143 | 143 |

terminals

| | | |
|----------------|----|----|
| un-matched | 0 | 0 |
| matched but | | |
| different type | 0 | 0 |
| total | 16 | 16 |

Probe files from /gaia/class/student/mahajanm/EEE_234_Project1/LVS/schematic

devbad.out:

netbad.out:

mergenet.out:

termbad.out:

prunenet.out:

prunedev.out:

audit.out:

Probe files from /gaia/class/student/mahajanm/EEE_234_Project1/LVS/layout

devbad.out:

netbad.out:

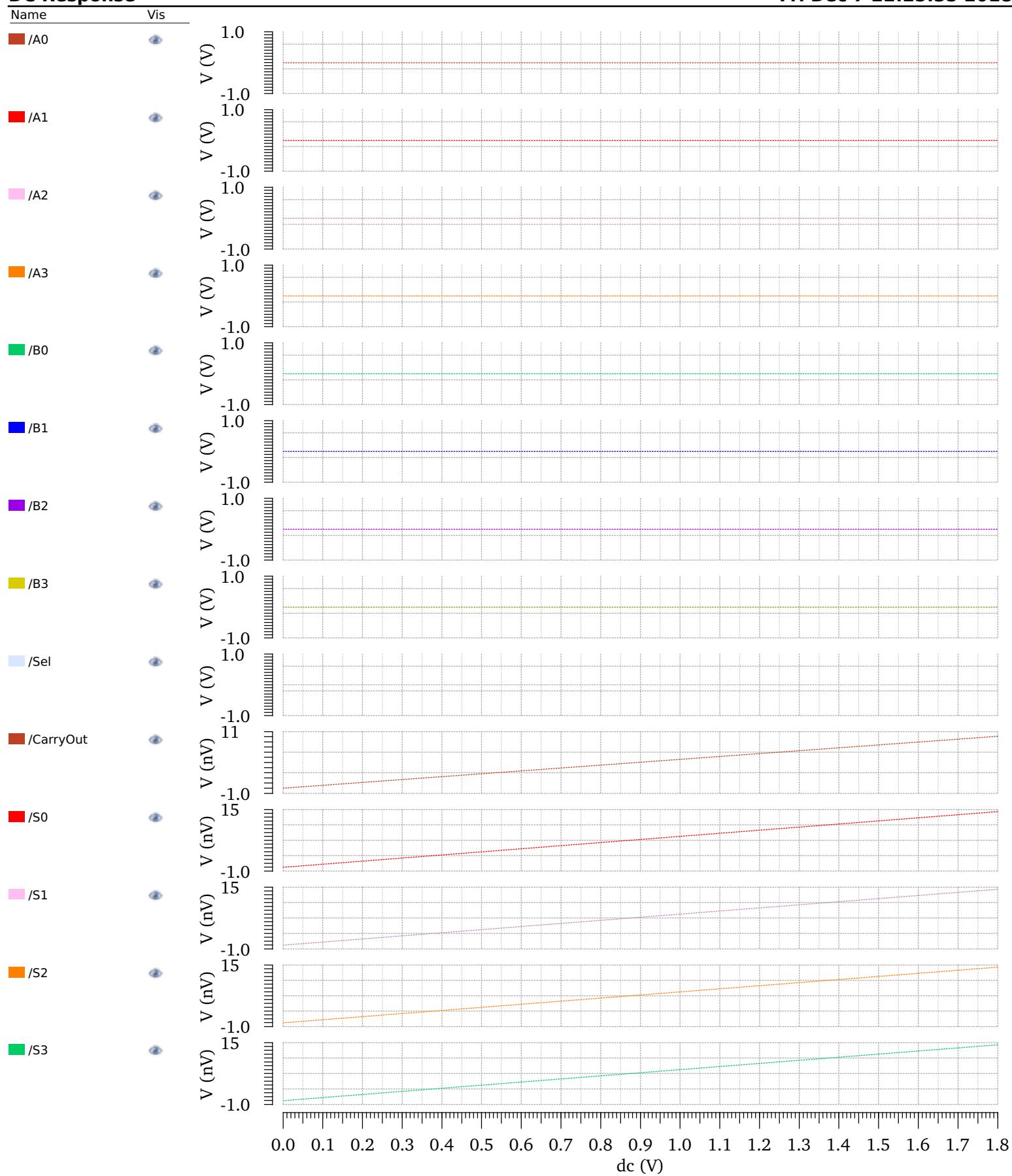
mergenet.out:

termbad.out:

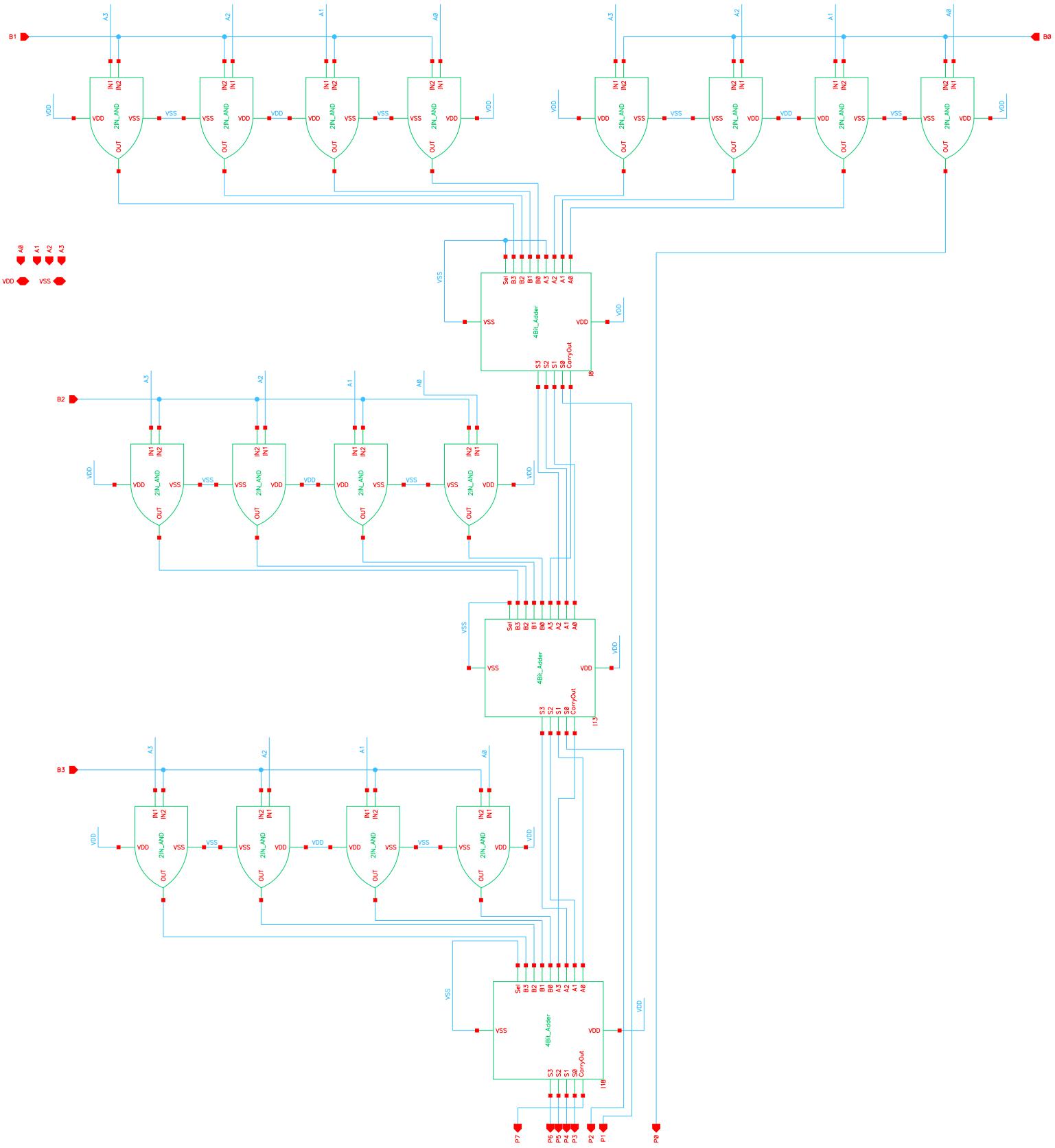
prunenet.out:

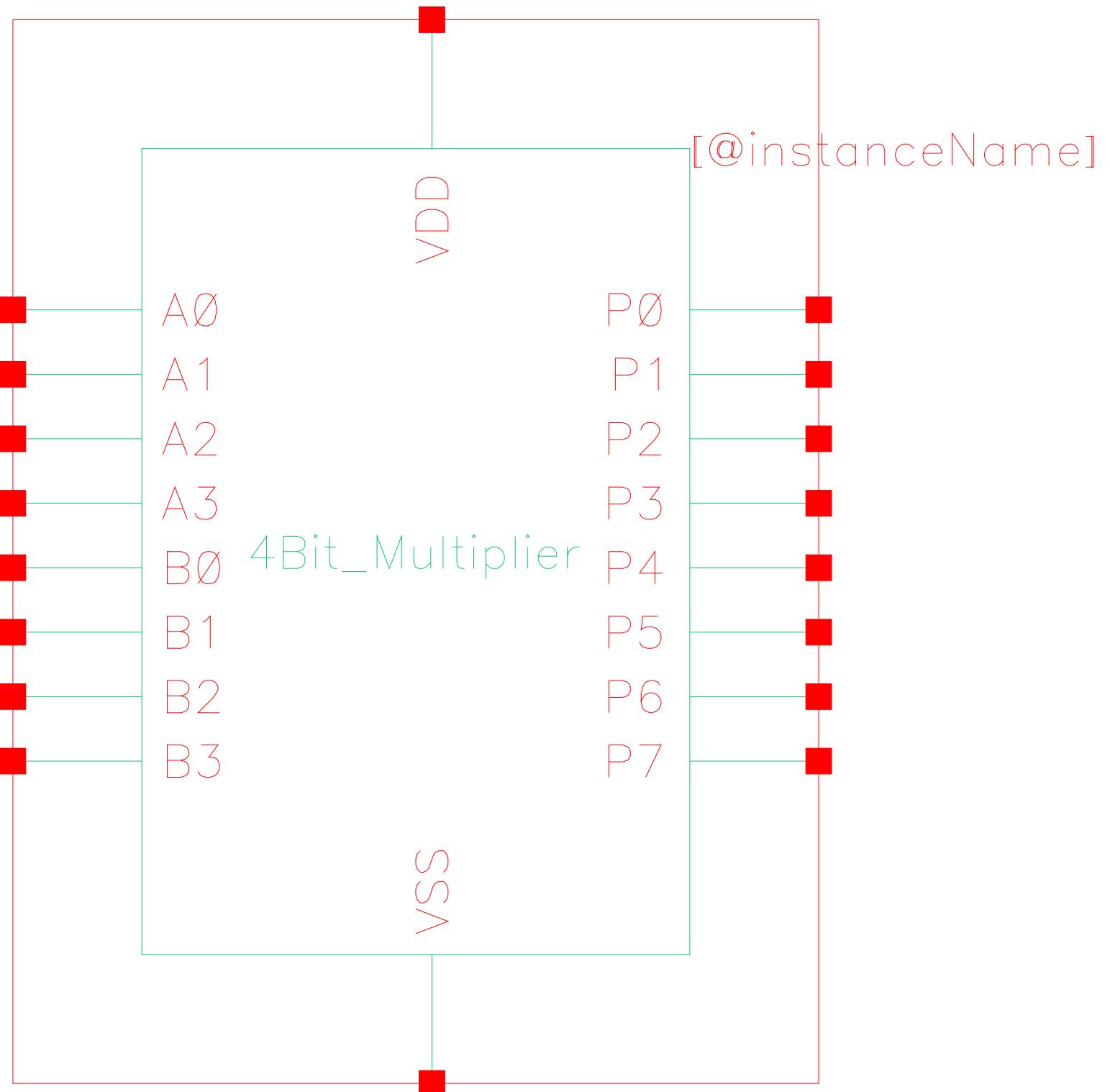
prunedev.out:

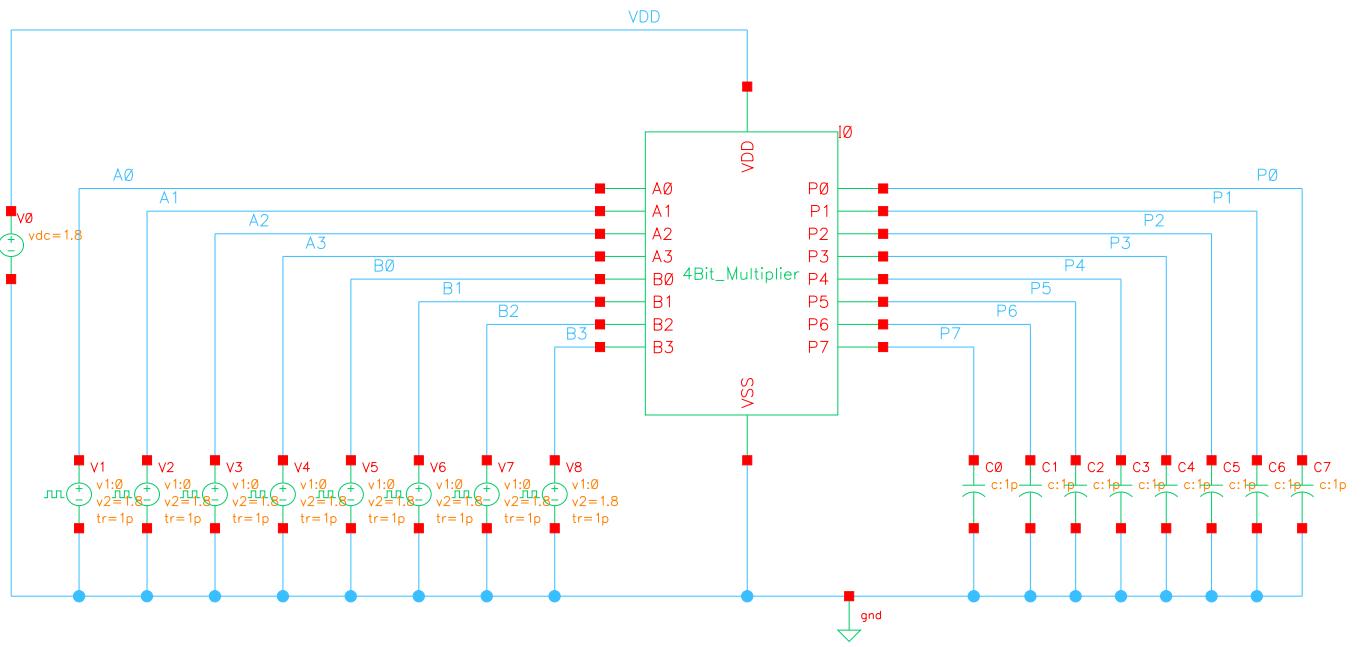
audit.out:

DC Response**4 Bit Adder DC Waveform****Fri Dec 7 22:25:35 2018**

Multiplier

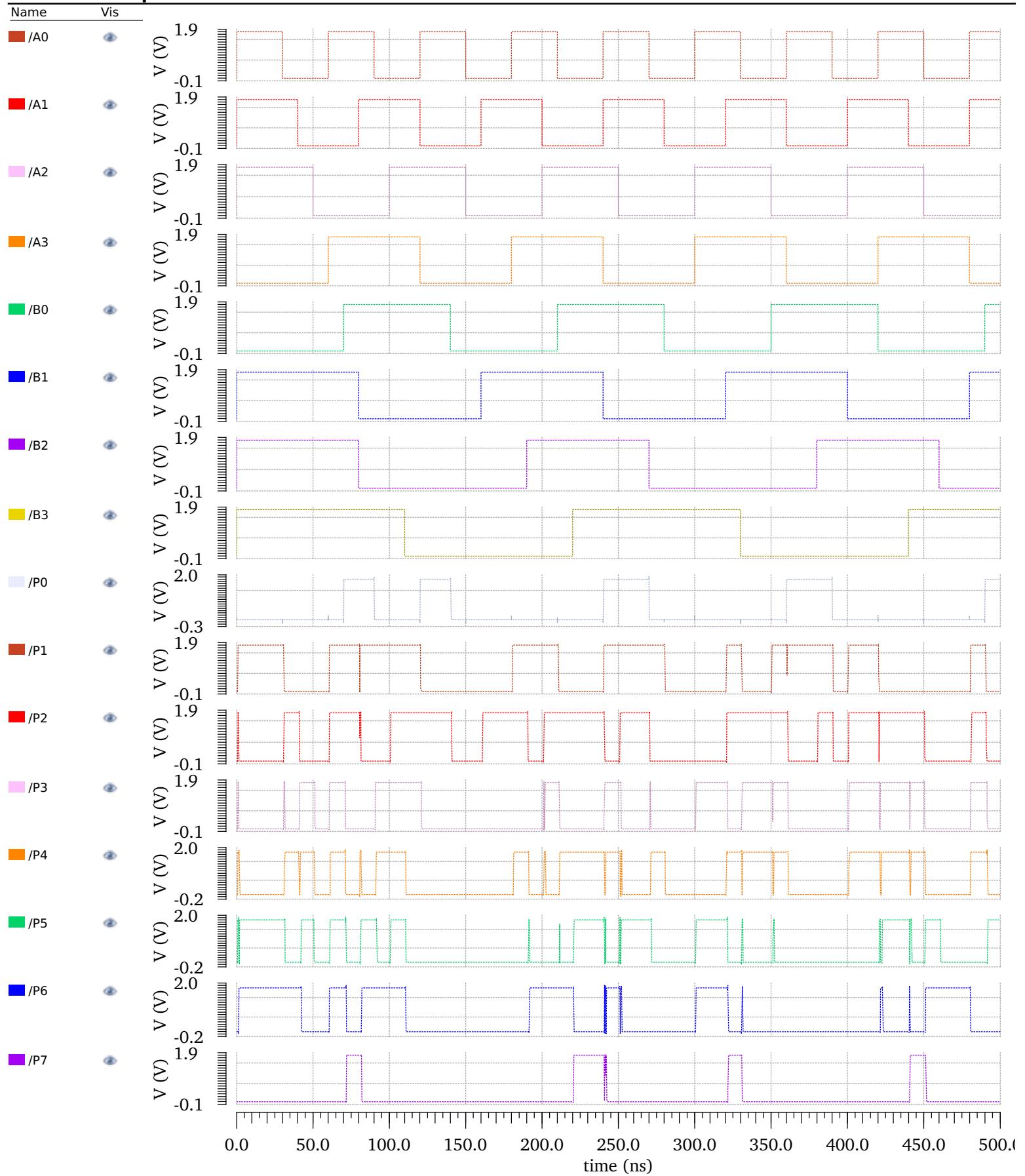


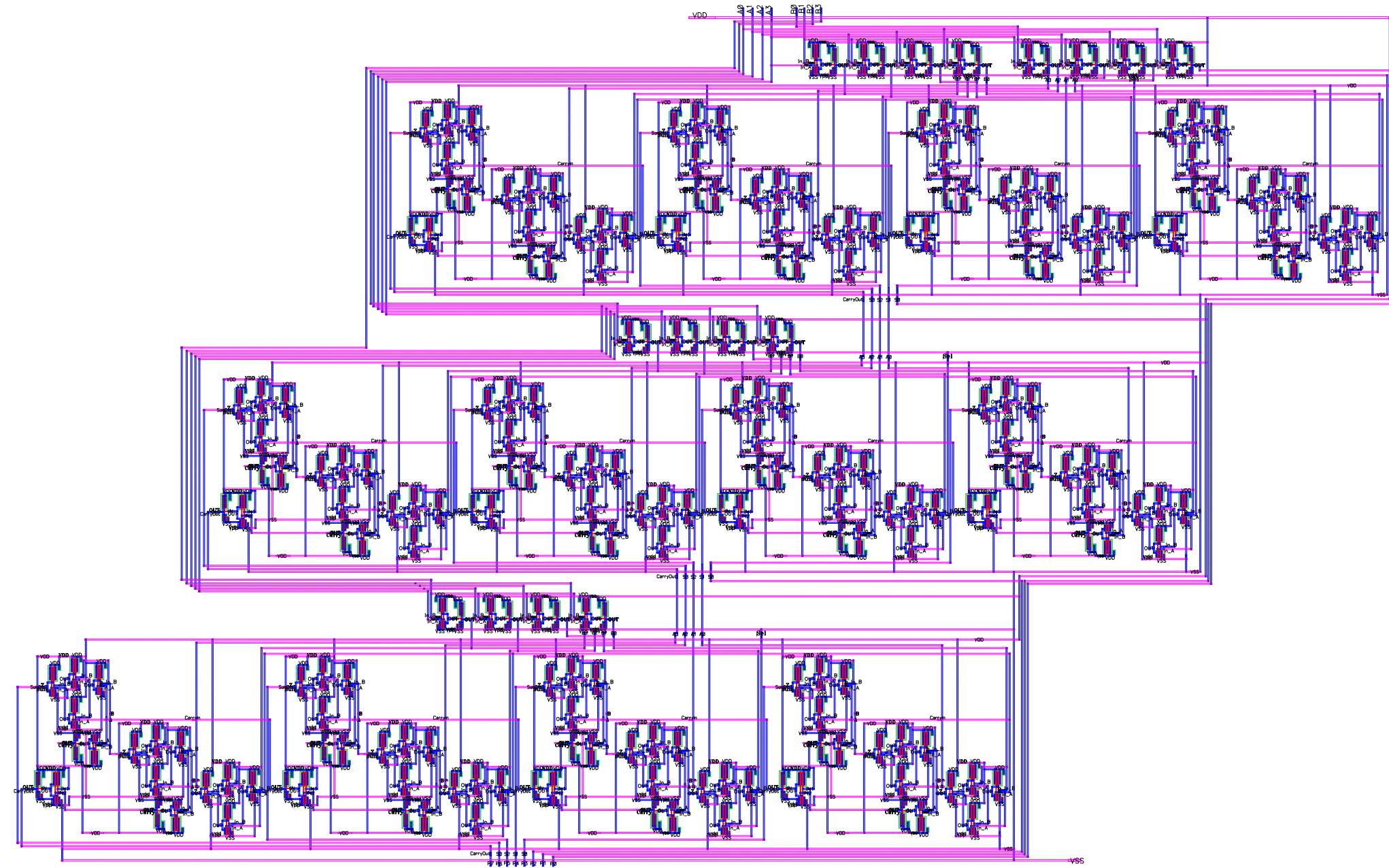




Transient Response**4 Bit Multiplier Waveform**

Thu Dec 6 00:32:34 2018





File Tools Options Help

cadence

```
DRC started..... Sun Dec 2 16:43:56 2018
completed .... Sun Dec 2 16:43:57 2018
CPU TIME = 00:00:00  TOTAL TIME = 00:00:01
***** Summary of rule violations for cell "4Bit_Multiplier_Layout layout" *****
Total errors found: 0
```

mouse L:showClickInfo()

M: setDRCForm()

R: _IxHiMousePopUp()

```
@(#)$CDS: LVS version 6.1.7-64b 09/27/2016 19:41 (sjfhw305) $
```

```
Command line: /software/cadence/install/IC617/tools.lnx86/dfl/bin/64bit/LVS -dir  
/gaia/class/student/mahajanm/EEE_234_Project1/LVS -l -s -t  
/gaia/class/student/mahajanm/EEE_234_Project1/LVS/layout  
/gaia/class/student/mahajanm/EEE_234_Project1/LVS/schematic
```

Like matching is enabled.

Net swapping is enabled.

Using terminal names as correspondence points.

Compiling Diva LVS rules...

```
Net-list summary for /gaia/class/student/mahajanm/EEE_234_Project1/LVS/layout/netlist
```

| count | |
|-------|-----------|
| 454 | nets |
| 18 | terminals |
| 444 | pmos |
| 444 | nmos |

```
Net-list summary for /gaia/class/student/mahajanm/EEE_234_Project1/LVS/schematic/netlist
```

| count | |
|-------|-----------|
| 454 | nets |
| 18 | terminals |
| 444 | pmos |
| 444 | nmos |

Terminal correspondence points

| | | |
|------|-----|----|
| N439 | N17 | A0 |
| N438 | N18 | A1 |
| N437 | N19 | A2 |
| N436 | N20 | A3 |
| N453 | N15 | B0 |
| N452 | N33 | B1 |

| | | |
|------|-----|-----|
| N451 | N36 | B2 |
| N449 | N32 | B3 |
| N448 | N35 | P0 |
| N447 | N39 | P1 |
| N446 | N10 | P2 |
| N445 | N13 | P3 |
| N444 | N38 | P4 |
| N443 | N37 | P5 |
| N442 | N34 | P6 |
| N441 | N40 | P7 |
| N450 | N25 | VDD |
| N440 | N1 | VSS |

Devices in the rules but not in the netlist:

```
cap nfet pfet nmos4 pmos4
```

The net-lists match.

| | | |
|------------------|-----|-----|
| layout schematic | | |
| instances | | |
| un-matched | 0 | 0 |
| rewired | 0 | 0 |
| size errors | 0 | 0 |
| pruned | 0 | 0 |
| active | 888 | 888 |
| total | 888 | 888 |

| | | |
|------------|-----|-----|
| nets | | |
| un-matched | 0 | 0 |
| merged | 0 | 0 |
| pruned | 0 | 0 |
| active | 454 | 454 |

total 454 454

terminals

un-matched 0 0

matched but

different type 0 0

total 18 18

Probe files from /gaia/class/student/mahajanm/EEE_234_Project1/LVS/schematic

devbad.out:

netbad.out:

mergenet.out:

termbad.out:

prunenet.out:

prunedev.out:

audit.out:

Probe files from /gaia/class/student/mahajanm/EEE_234_Project1/LVS/layout

devbad.out:

netbad.out:

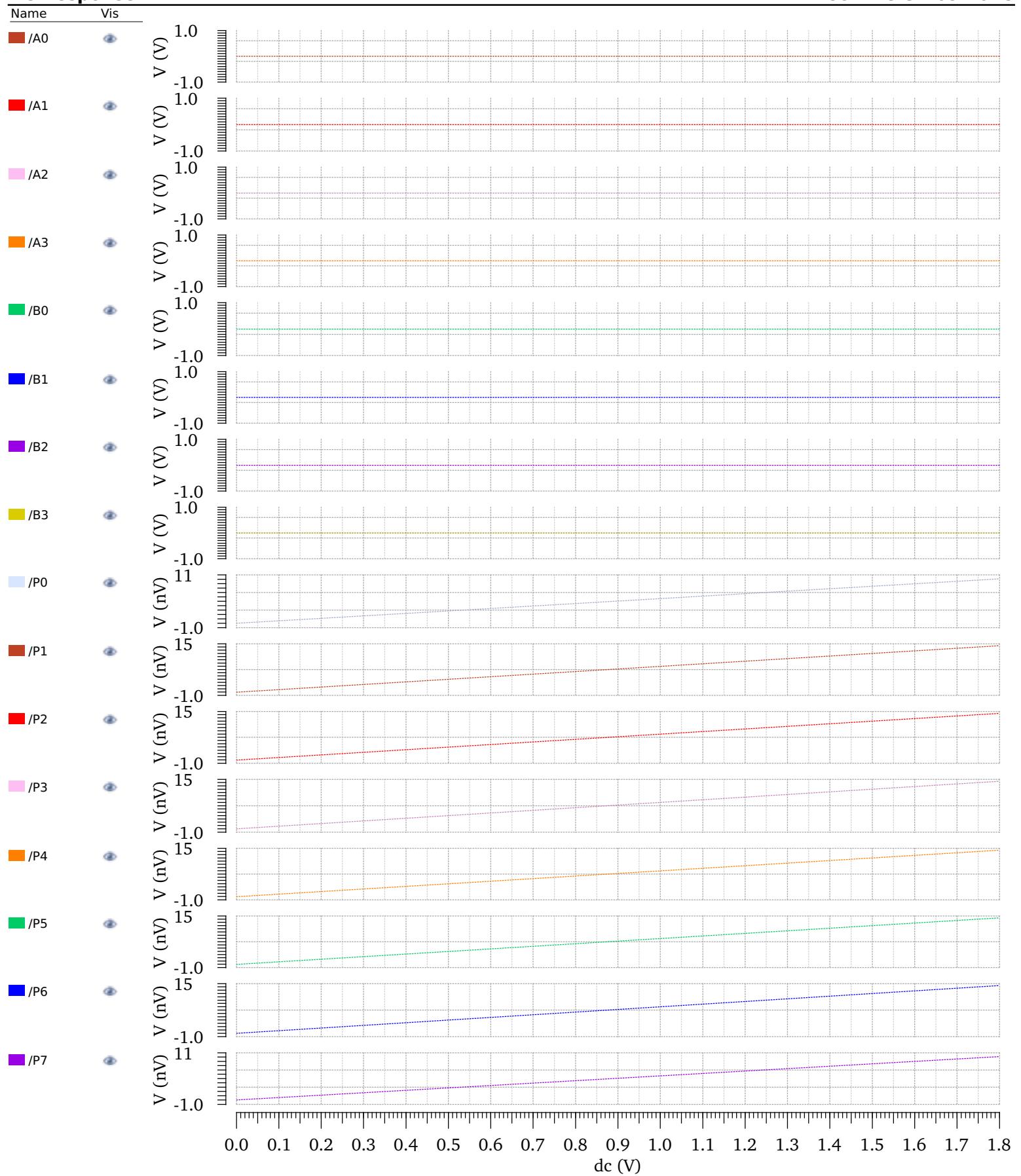
mergenet.out:

termbad.out:

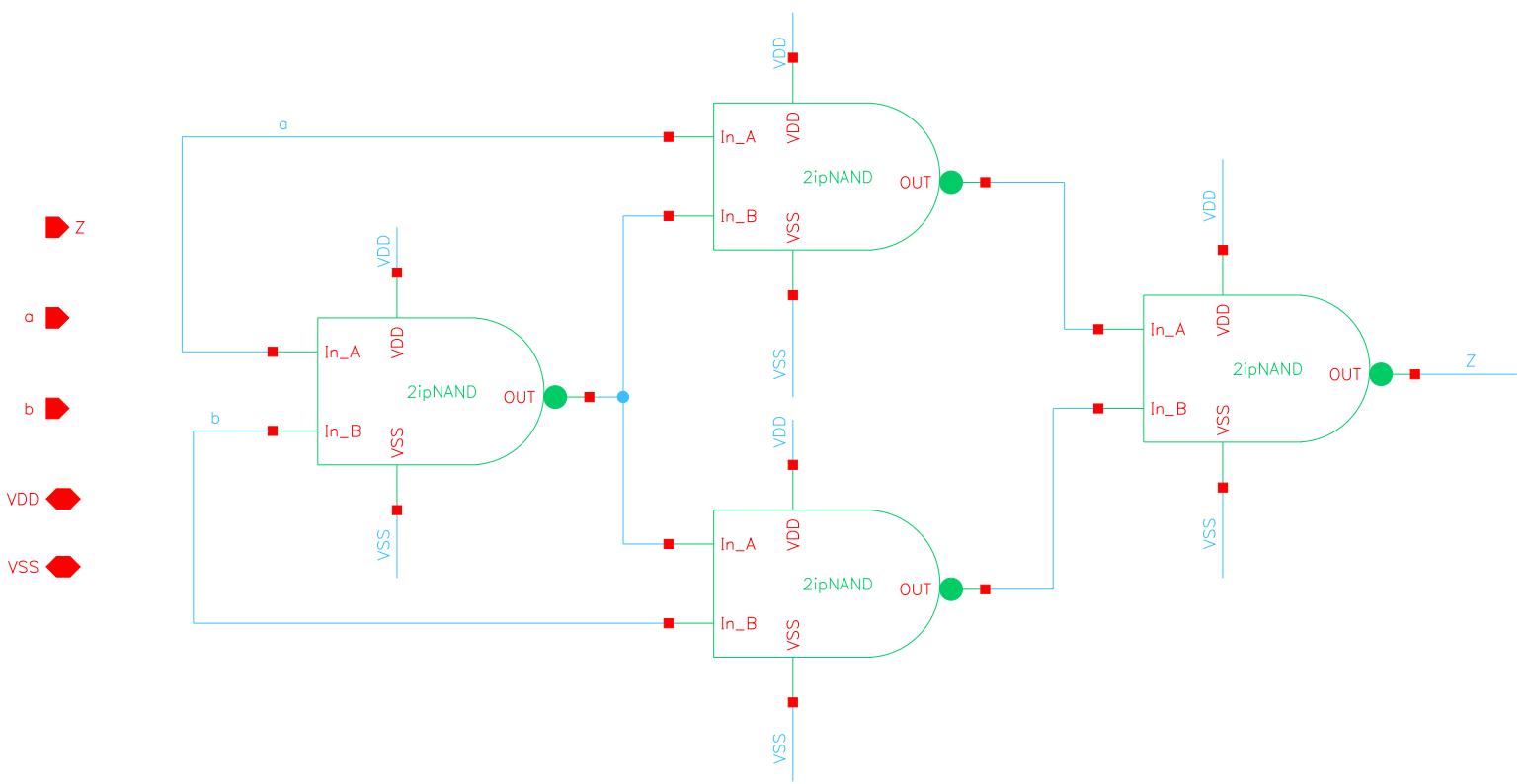
prunenet.out:

prunedev.out:

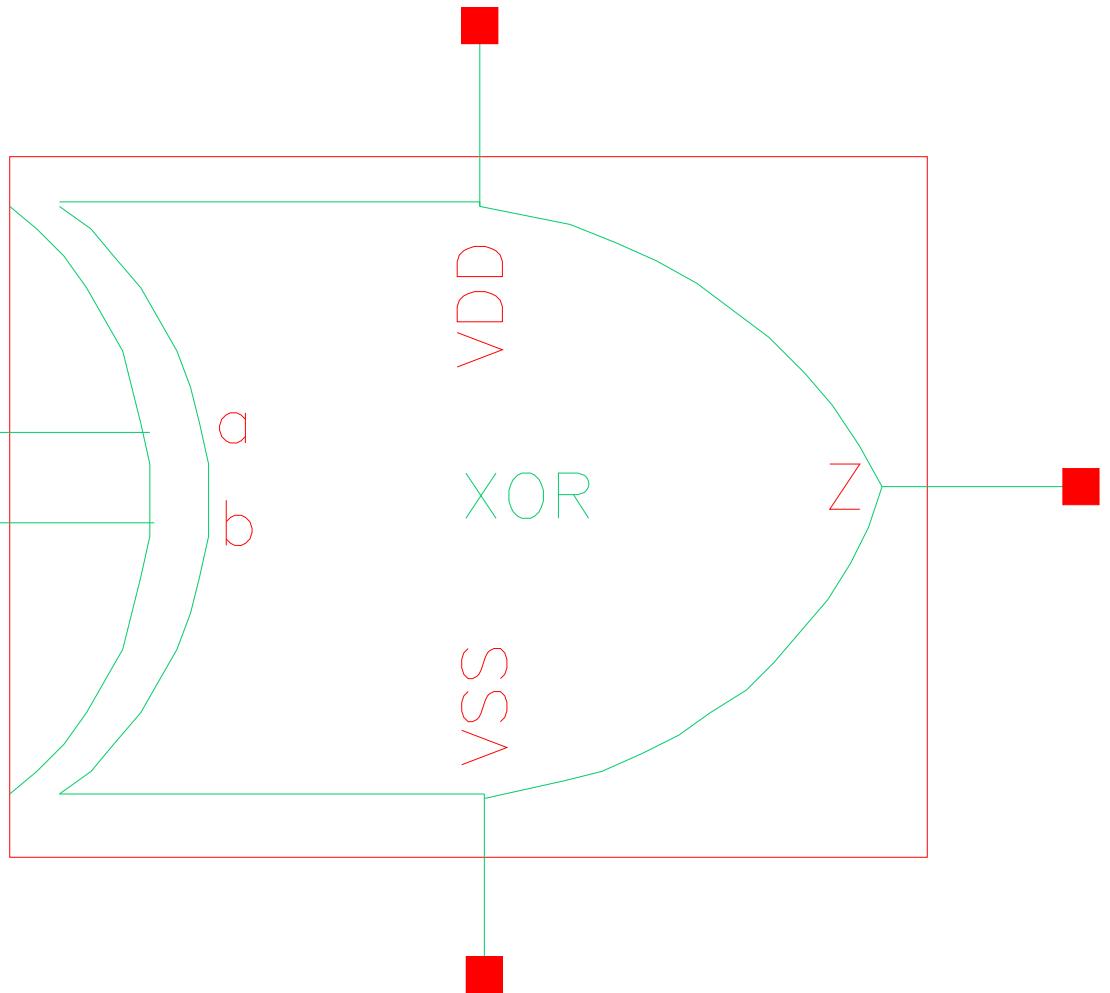
audit.out:

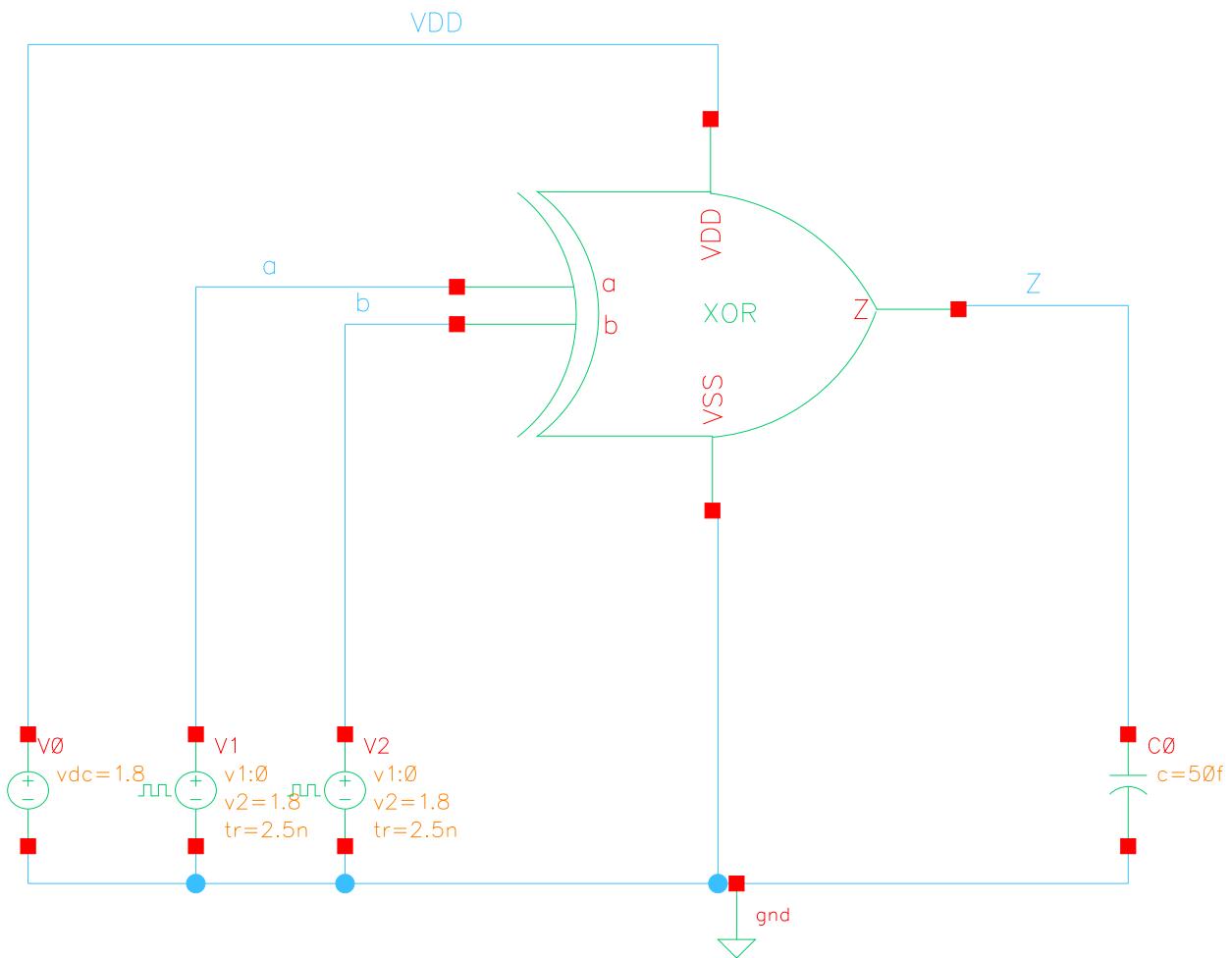
DC Response**4 bit Multiplier DC Waveform****Fri Dec 7 18:31:09 2018**

XOR



[@XOR]

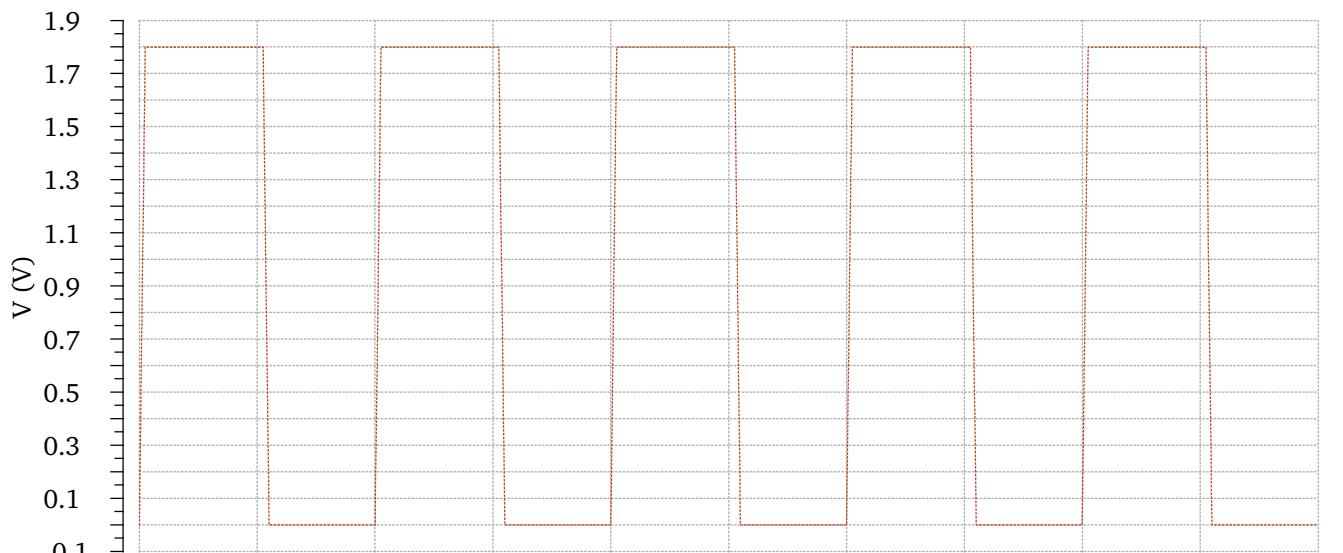




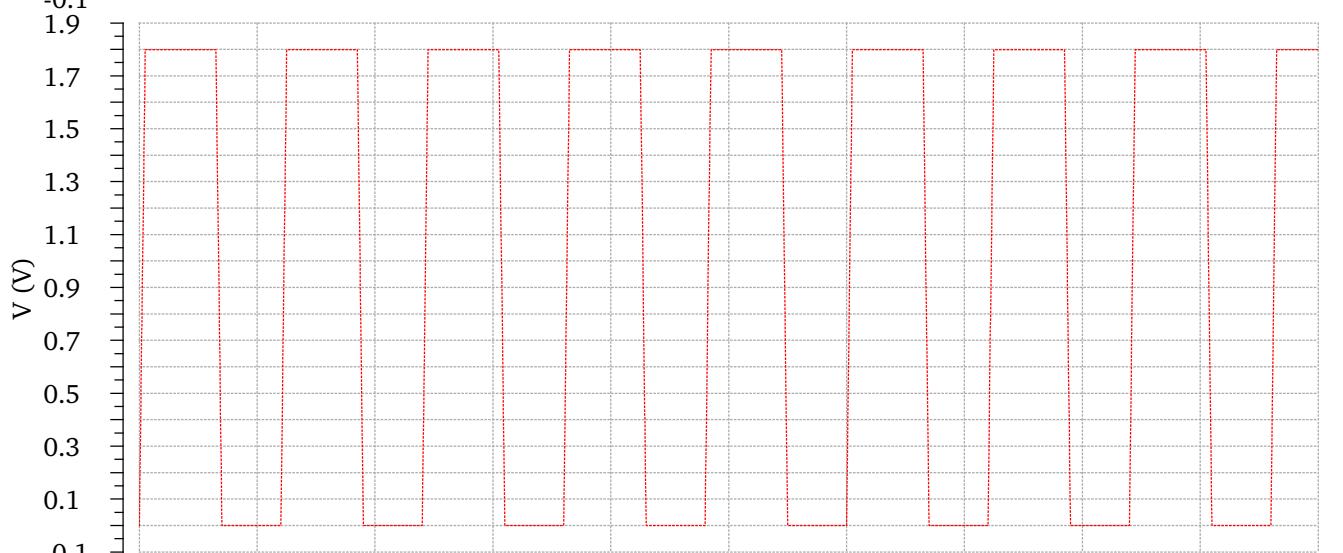
Transient Response**Fri Dec 7 23:24:51 2018**

Name Vis

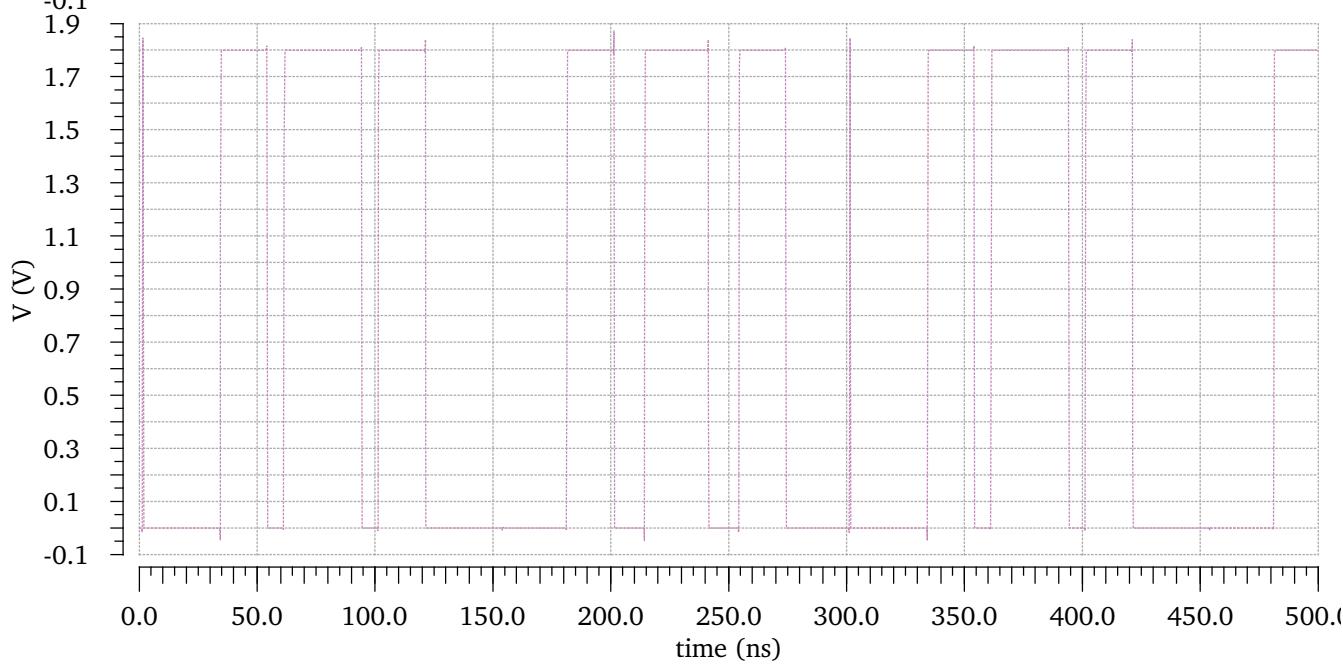
■ /a

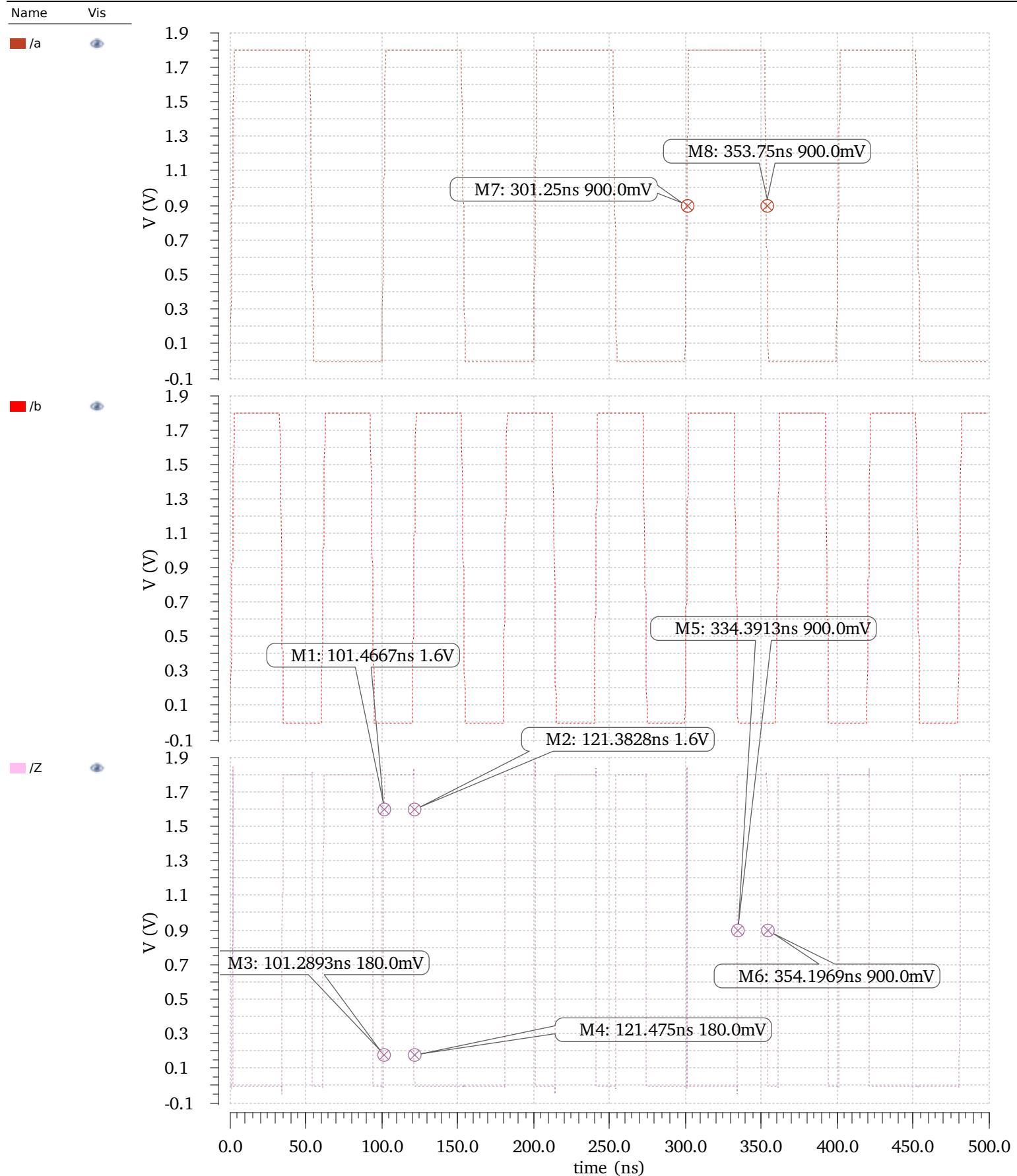


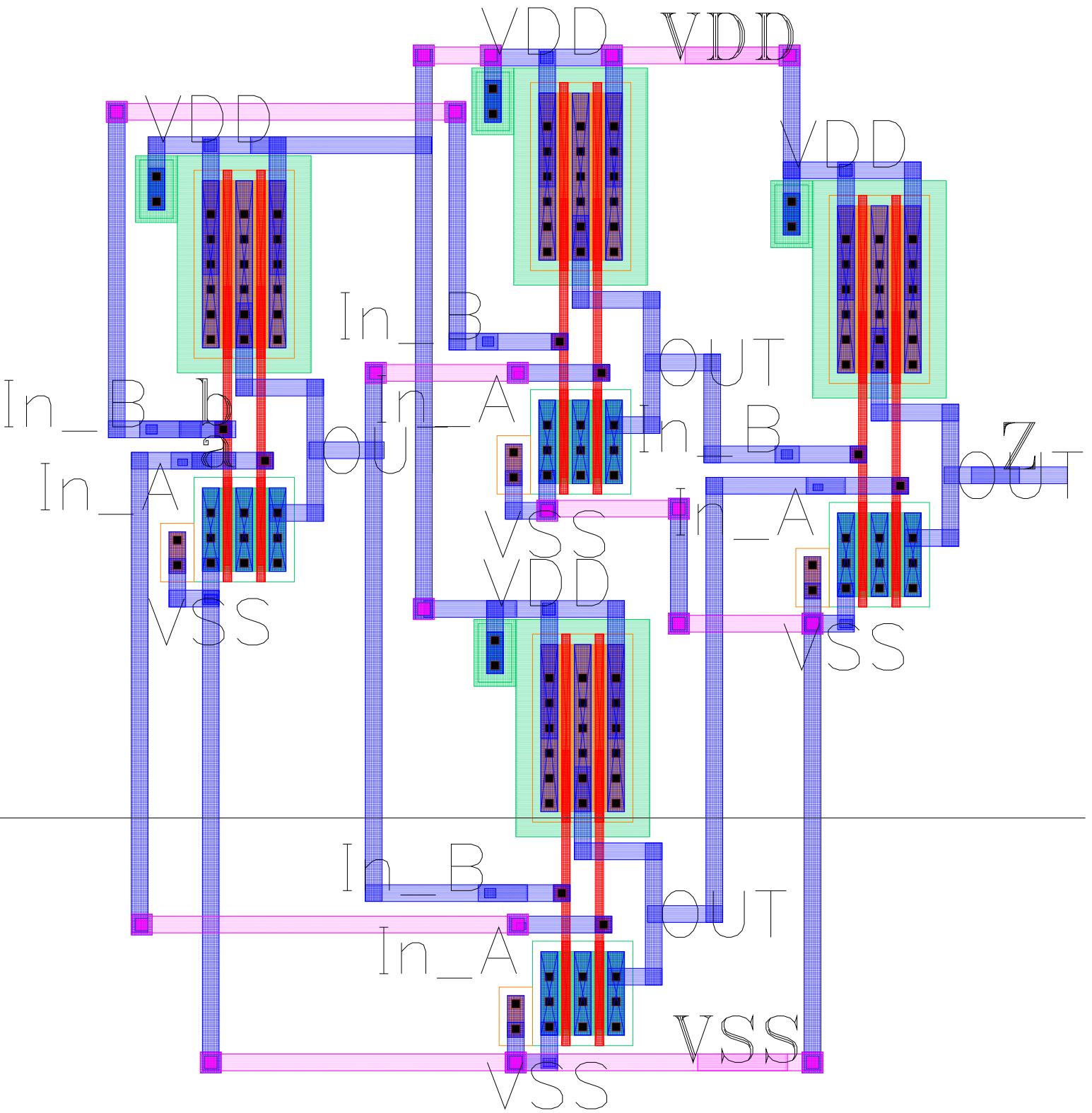
■ /b



■ /z



Transient Response**Fri Dec 7 23:24:51 2018**



File Tools Options Help

DRC started.....Fri Dec 7 23:29:30 2018

completedFri Dec 7 23:29:30 2018

CPU TIME = 00:00:00 TOTAL TIME = 00:00:00

***** Summary of rule violations for cell "XOR_Layout layout" *****

Total errors found: 0

mouse L: showClickInfo()

M: setDRCForm()

R: _IxHiMousePopUp()

```
@(#)$CDS: LVS version 6.1.7-64b 09/27/2016 19:41 (sjfhw305) $
```

Command line: /software/cadence/install/IC617/tools.lnx86/dfl/bin/64bit/LVS -dir
/gaia/class/student/mahajanm/EEE_234_Project1/LVS -l -s -t
/gaia/class/student/mahajanm/EEE_234_Project1/LVS/layout
/gaia/class/student/mahajanm/EEE_234_Project1/LVS/schematic

Like matching is enabled.

Net swapping is enabled.

Using terminal names as correspondence points.

Net-list summary for /gaia/class/student/mahajanm/EEE_234_Project1/LVS/layout/netlist

```
count  
12      nets  
5       terminals  
8       pmos  
8       nmos
```

Net-list summary for /gaia/class/student/mahajanm/EEE_234_Project1/LVS/schematic/netlist

```
count  
12      nets  
5       terminals  
8       pmos  
8       nmos
```

Terminal correspondence points

```
N11    N7    VDD  
N7     N2    VSS  
N10    N5    Z  
N9     N3    a
```

N8 N1 b

Devices in the netlist but not in the rules:

pmos nmox

The net-lists match.

layout schematic

instances

| | | |
|-------------|----|----|
| un-matched | 0 | 0 |
| rewired | 0 | 0 |
| size errors | 0 | 0 |
| pruned | 0 | 0 |
| active | 16 | 16 |
| total | 16 | 16 |

nets

| | | |
|------------|----|----|
| un-matched | 0 | 0 |
| merged | 0 | 0 |
| pruned | 0 | 0 |
| active | 12 | 12 |
| total | 12 | 12 |

terminals

| | | |
|----------------|---|---|
| un-matched | 0 | 0 |
| matched but | | |
| different type | 0 | 0 |
| total | 5 | 5 |

Probe files from /gaia/class/student/mahajanm/EEE_234_Project1/LVS/schematic

devbad.out:

netbad.out:

mergenet.out:

termbad.out:

prunenet.out:

prunedev.out:

audit.out:

Probe files from /gaia/class/student/mahajanm/EEE_234_Project1/LVS/layout

devbad.out:

netbad.out:

mergenet.out:

termbad.out:

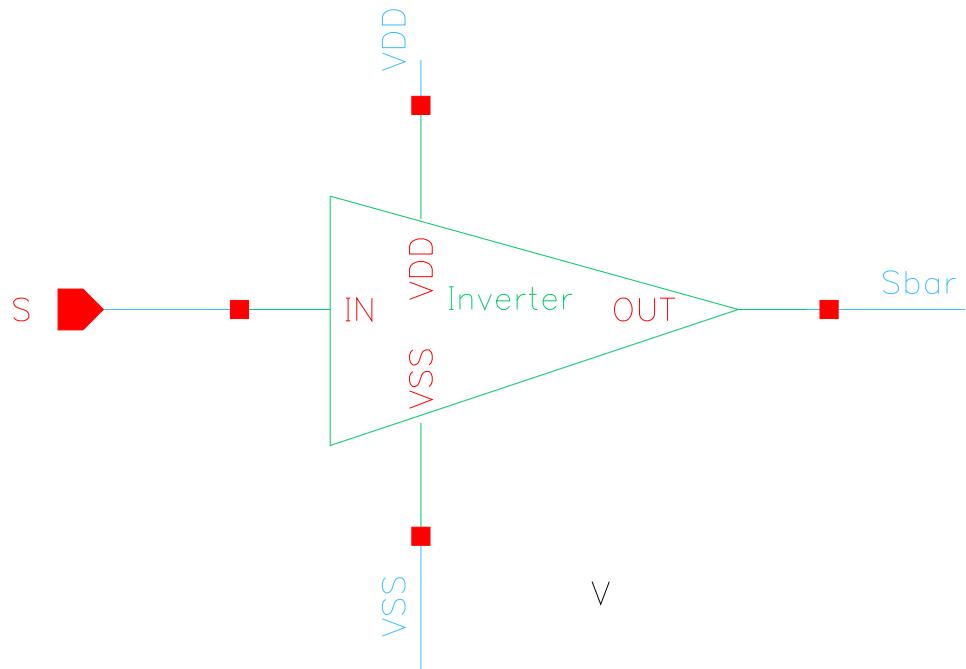
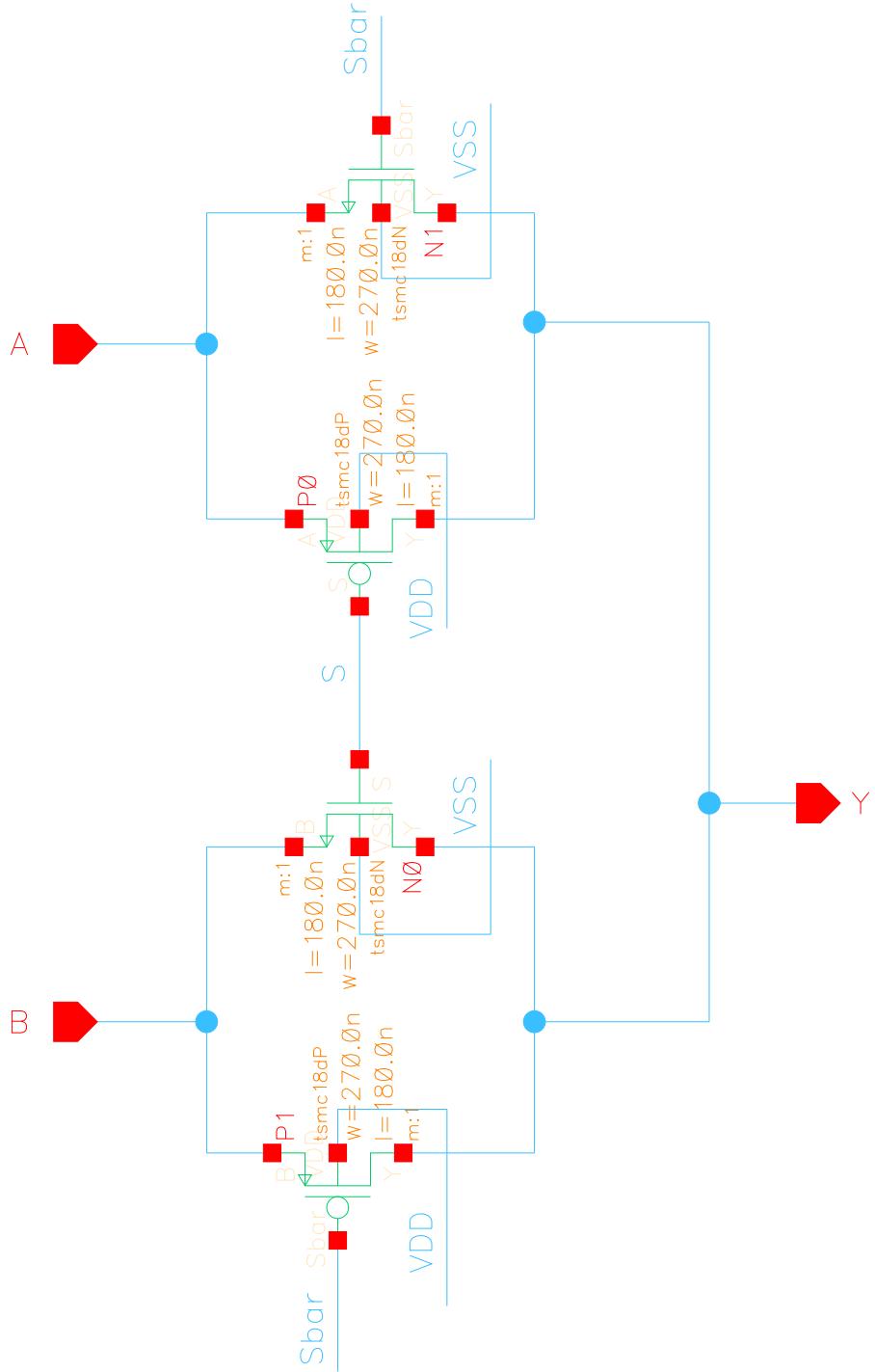
prunenet.out:

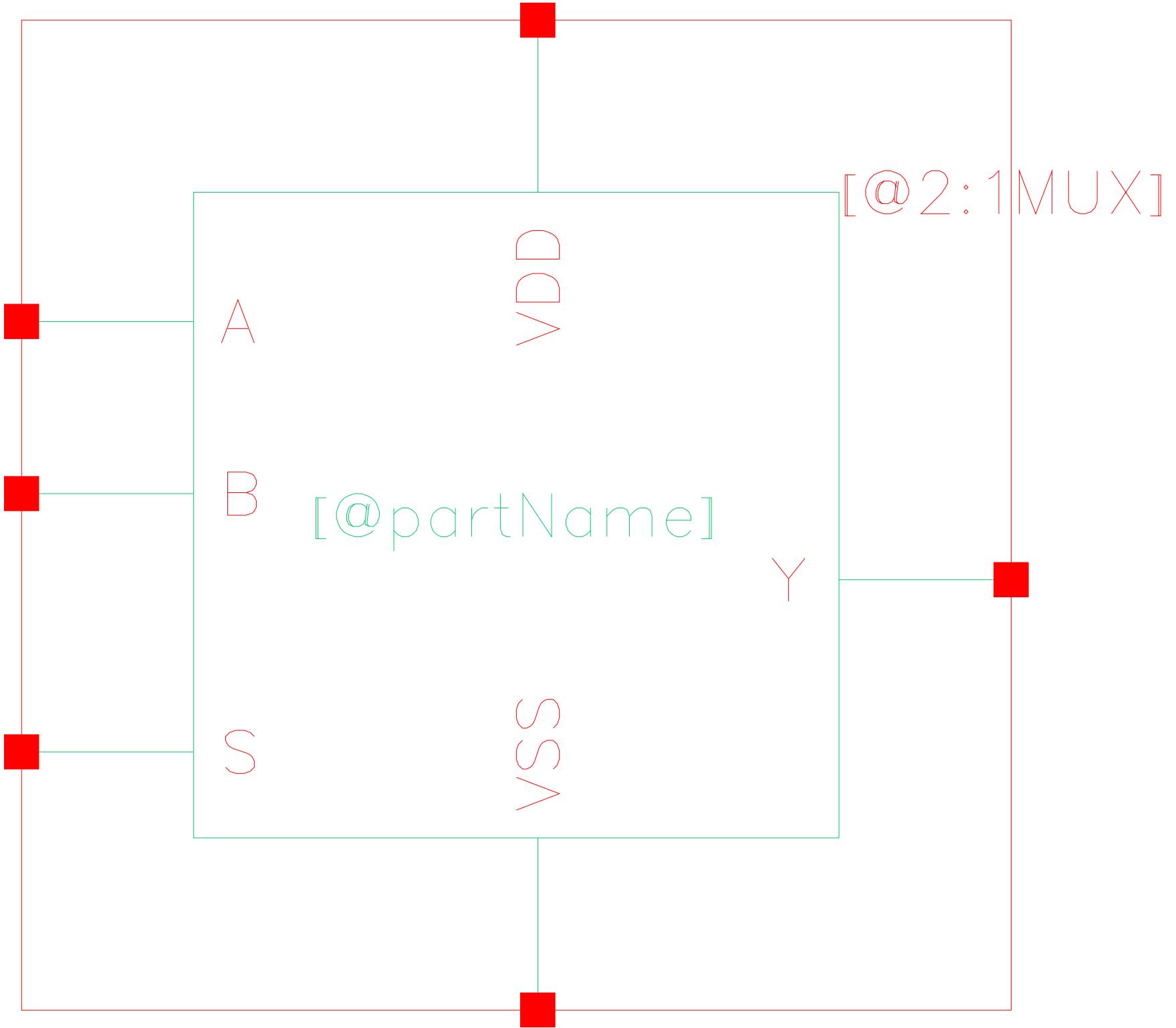
prunedev.out:

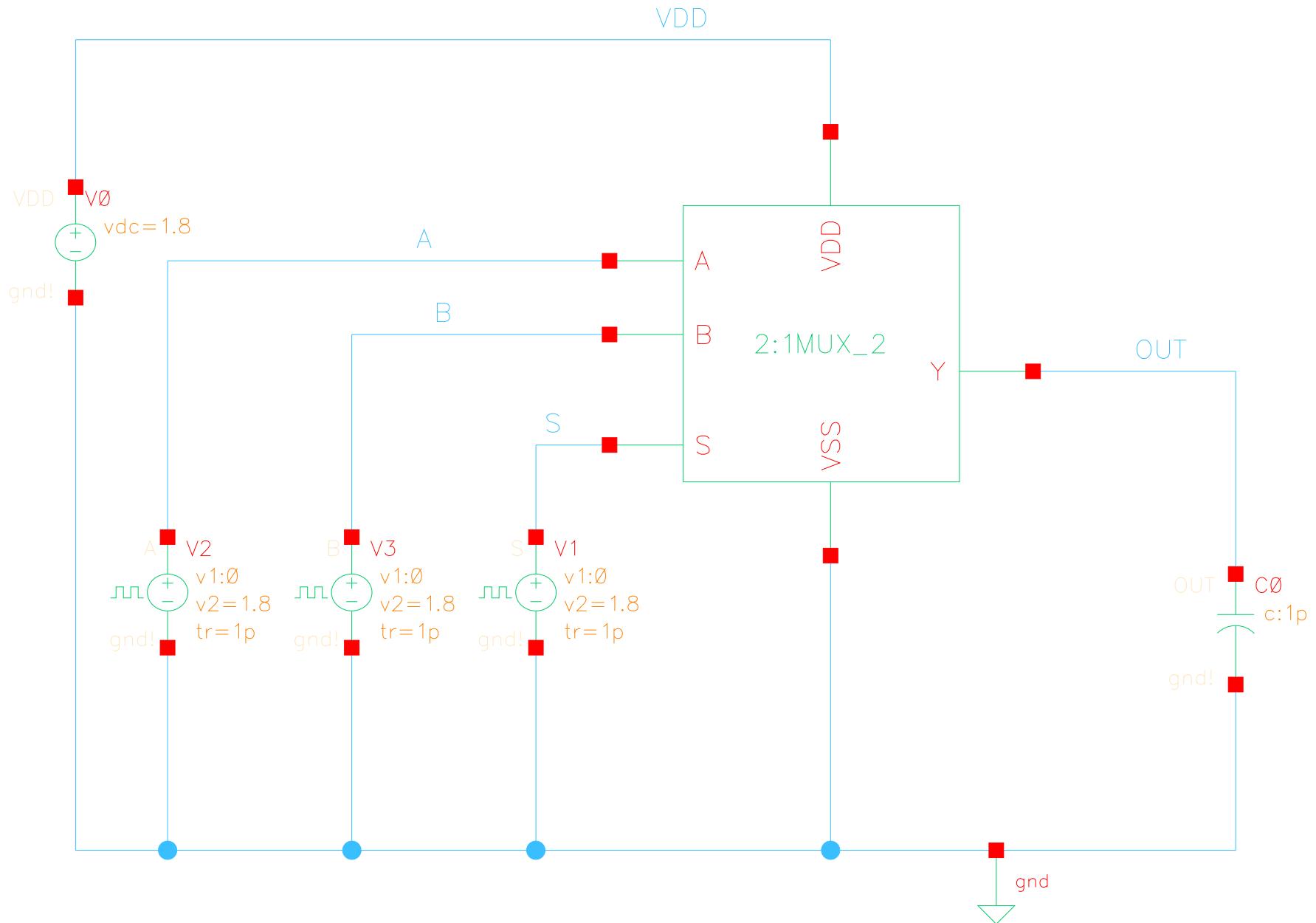
audit.out:

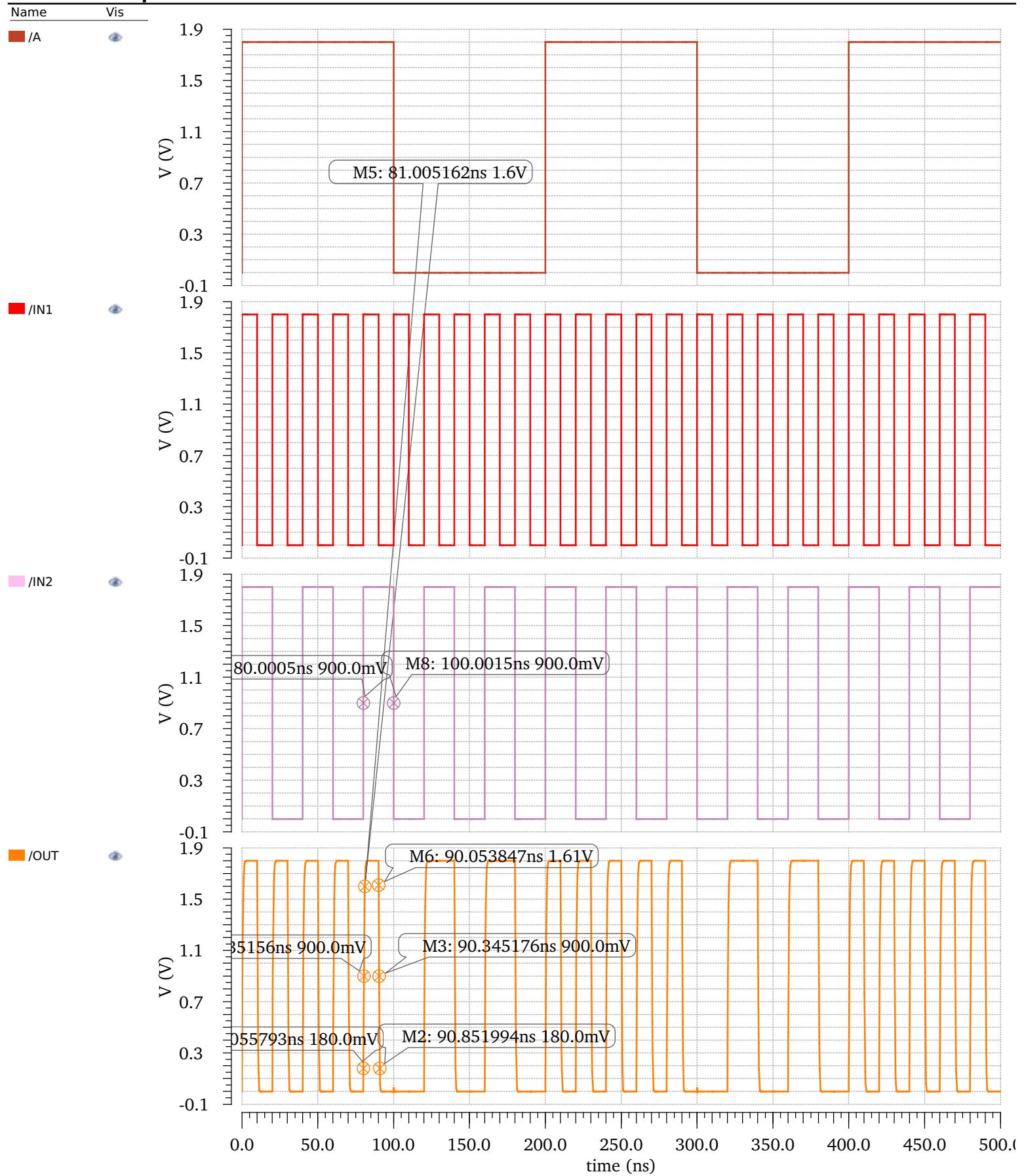
2:1 MUX

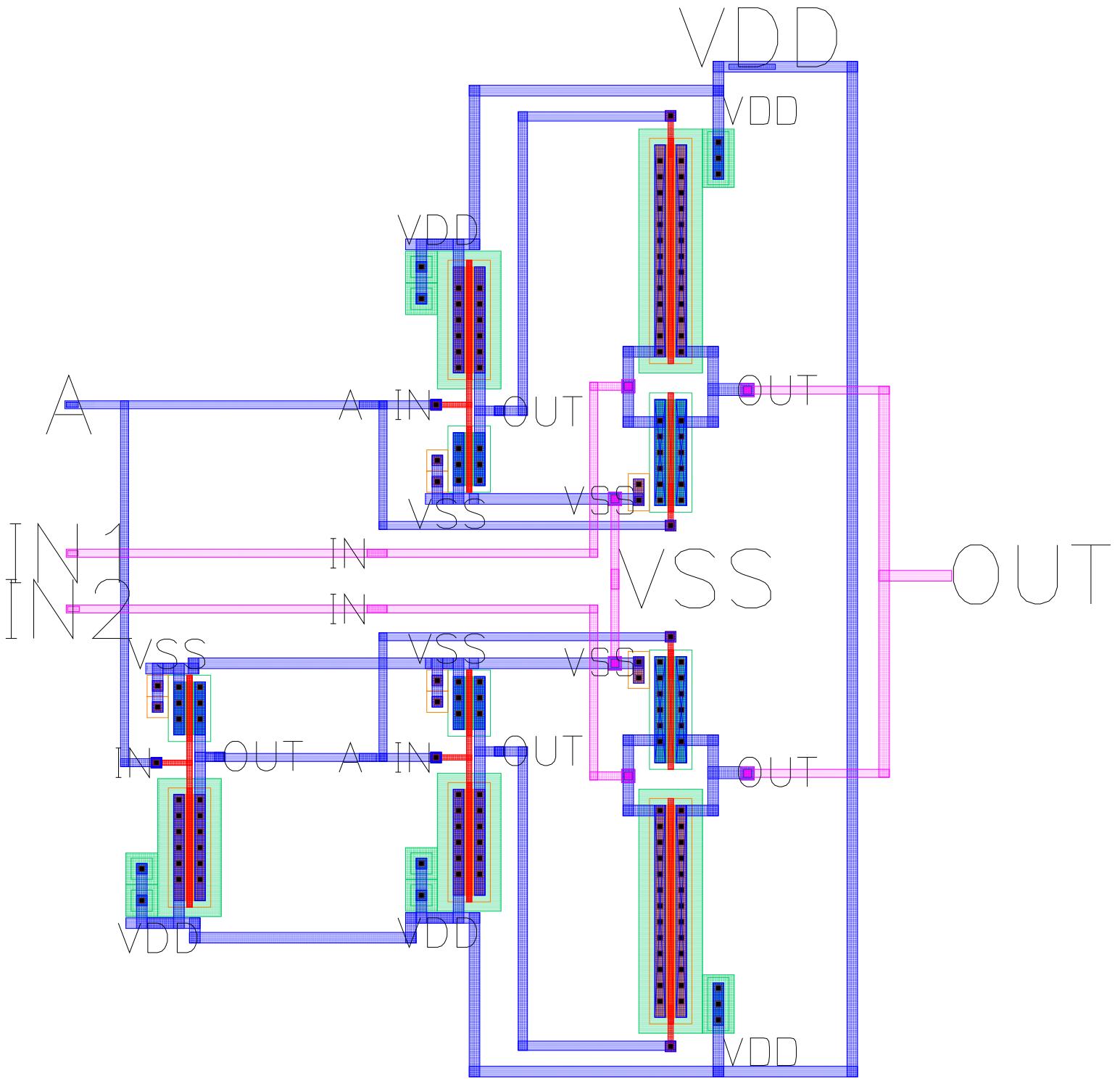
VDD
VSS







Transient Response**2:1 MUX Waveform****Fri Dec 7 18:33:58 2018**



File Tools Options Help

DRC started at Sun Oct 28 13:22:33 2018

Validating hierarchy instantiation for:

library: EEE_234_Project1

cell: 2:1MUX_Layout

view: layout

Rules come from library NCSU_TechLib_tsmc02d.

Rules path is divaDRC.rul.

Inclusion limit is set to 1000.

Running layout DRC analysis

Flat mode

Full checking.

DRC started.....Sun Oct 28 13:22:33 2018

completedSun Oct 28 13:22:33 2018

CPU TIME = 00:00:00 TOTAL TIME = 00:00:00

***** Summary of rule violations for cell "2:1MUX_Layout layout" *****

Total errors found: 0

mouse L: showClickInfo()

M: setDRCForm()

R: _lxHiMousePopUp()

LVS (2:1MUX) :

Running simulation in directory: "/gaia/class/student/mahajanm/EEE_234_Project1/LVS".

Begin netlist: Oct 27 19:27:42 2018

```
view name list = ("auLvs" "extracted" "schematic")
stop name list = ("auLvs")
library name    = "EEE_234_Project1"
cell name       = "2:1MUX_Layout"
view name       = "extracted"
globals lib     = "basic"
```

Running Artist Flat Netlisting ...

End netlist: Oct 27 19:27:43 2018

Begin netlist: Oct 27 19:27:43 2018

```
view name list = ("auLvs" "schematic")
stop name list = ("auLvs")
library name    = "EEE_234_Project1"
cell name       = "2:1MUX"
view name       = "schematic"
globals lib     = "basic"
```

Running Artist Flat Netlisting ...

End netlist: Oct 27 19:27:44 2018

Moving original netlist to extNetlist

Removing parasitic components from netlist

```
presistors removed: 0
pcapacitors removed: 0
pinductors removed: 0
pdiodes removed: 0
trans lines removed: 0
20 nodes merged into 20 nodes
```

Running netlist comparison program: LVS

Begin comparison: Oct 27 19:27:44 2018

@(#) \$CDS: LVS version 6.1.7-64b 09/27/2016 19:41 (sjfhw305) \$

The net-lists match.

layout schematic

instances

| | | |
|-------------|----|----|
| un-matched | 0 | 0 |
| rewired | 0 | 0 |
| size errors | 0 | 0 |
| pruned | 0 | 0 |
| active | 10 | 10 |
| total | 10 | 10 |

nets

| | | |
|------------|---|---|
| un-matched | 0 | 0 |
| merged | 0 | 0 |
| pruned | 0 | 0 |
| active | 0 | 0 |
| total | 9 | 9 |

terminals

| | | |
|----------------|---|---|
| un-matched | 0 | 0 |
| matched but | | |
| different type | 0 | 0 |
| total | 6 | 6 |

End comparison: Oct 27 19:27:45 2018

Comparison program completed successfully.

@(#)\$CDS: LVS version 6.1.7-64b 09/27/2016 19:41 (sjfhw305) \$

Command line: /software/cadence/install/IC617/tools.lnx86/dfII/bin/64bit/LVS -dir
/gaia/class/student/mahajanm/EEE_234_Project1/LVS -l -s -t
/gaia/class/student/mahajanm/EEE_234_Project1/LVS/layout
/gaia/class/student/mahajanm/EEE_234_Project1/LVS/schematic

Like matching is enabled.

Net swapping is enabled.

Using terminal names as correspondence points.

Net-list summary for /gaia/class/student/mahajanm/EEE_234_Project1/LVS/layout/netlist

| count | |
|-------|-----------|
| 6 | nets |
| 5 | terminals |
| 2 | pmos |
| 2 | nmos |

Net-list summary for /gaia/class/student/mahajanm/EEE_234_Project1/LVS/schematic/netlist

| count | |
|-------|-----------|
| 6 | nets |
| 5 | terminals |
| 2 | pmos |
| 2 | nmos |

Terminal correspondence points

| | | |
|----|----|------|
| N4 | N1 | In_A |
| N3 | N4 | In_B |
| N2 | N3 | OUT |
| N5 | N2 | VDD |
| N1 | N0 | VSS |

Probe files from /gaia/class/student/mahajanm/EEE_234_Project1/LVS/schematic

devbad.out:

netbad.out:

mergenet.out:

termbad.out:

prunenet.out:

prunedev.out:

audit.out:

Probe files from /gaia/class/student/mahajanm/EEE_234_Project1/LVS/layout

devbad.out:

netbad.out:

mergenet.out:

termbad.out:

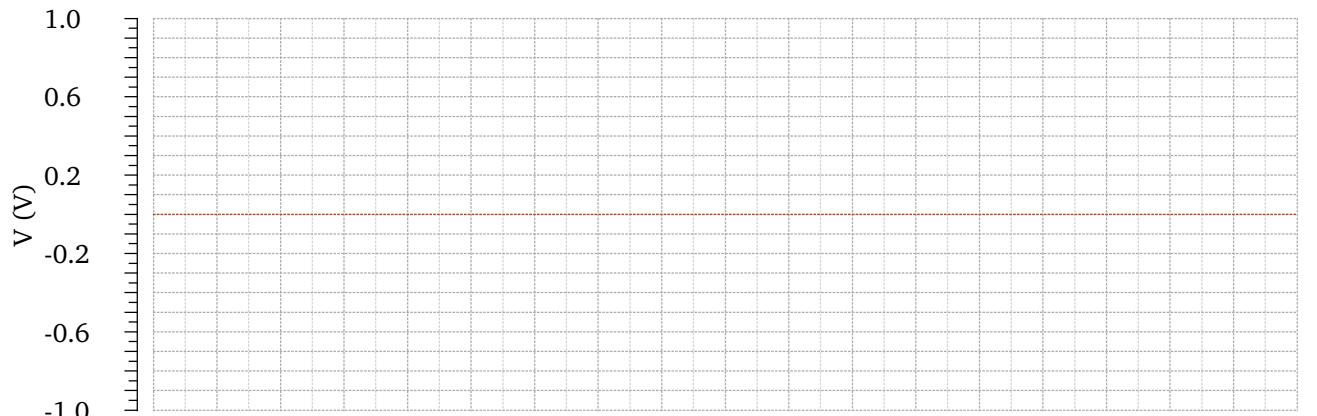
prunenet.out:

prunedev.out:

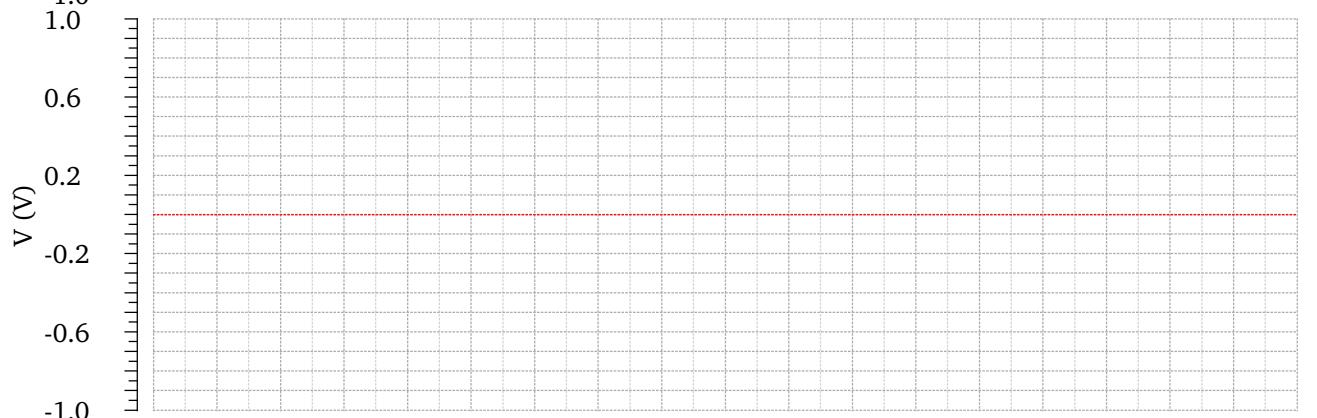
audit.out:

DC Response**2:1 MUX DC Waveform****Fri Dec 7 18:38:09 2018**

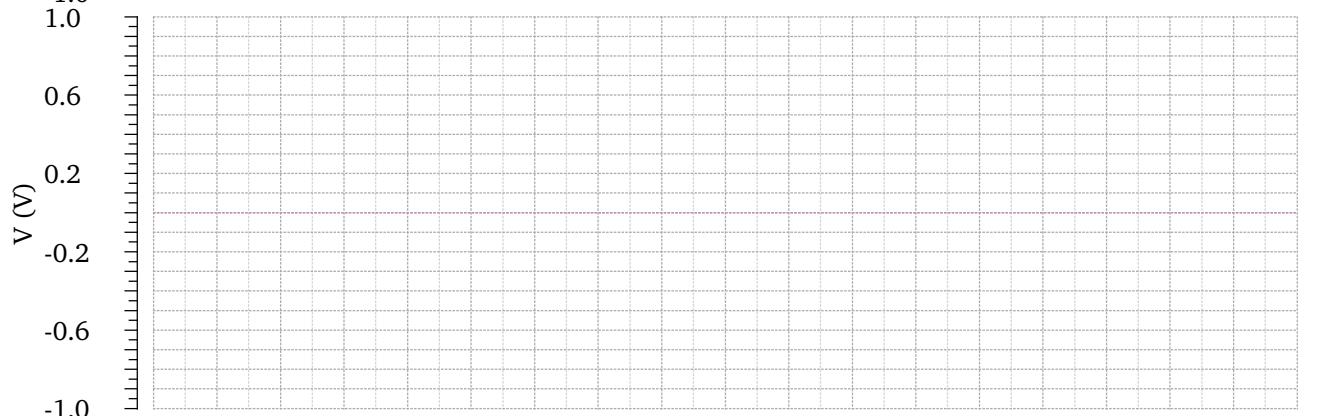
| Name | Vis |
|------|-----|
| ■ /A | ● |



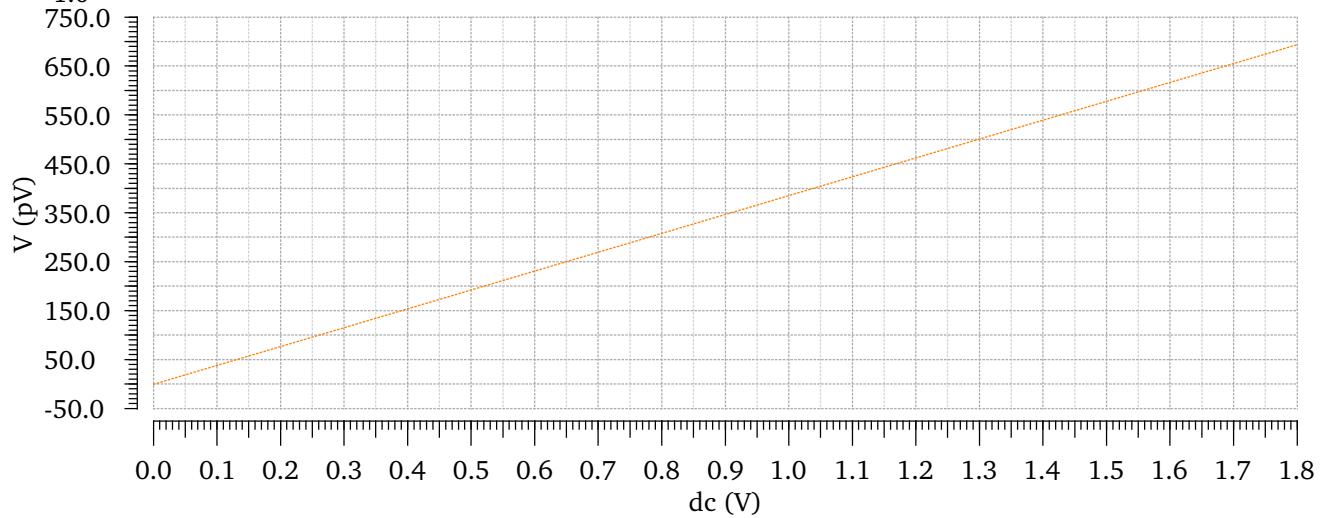
| | |
|--------|---|
| ■ /IN1 | ● |
|--------|---|



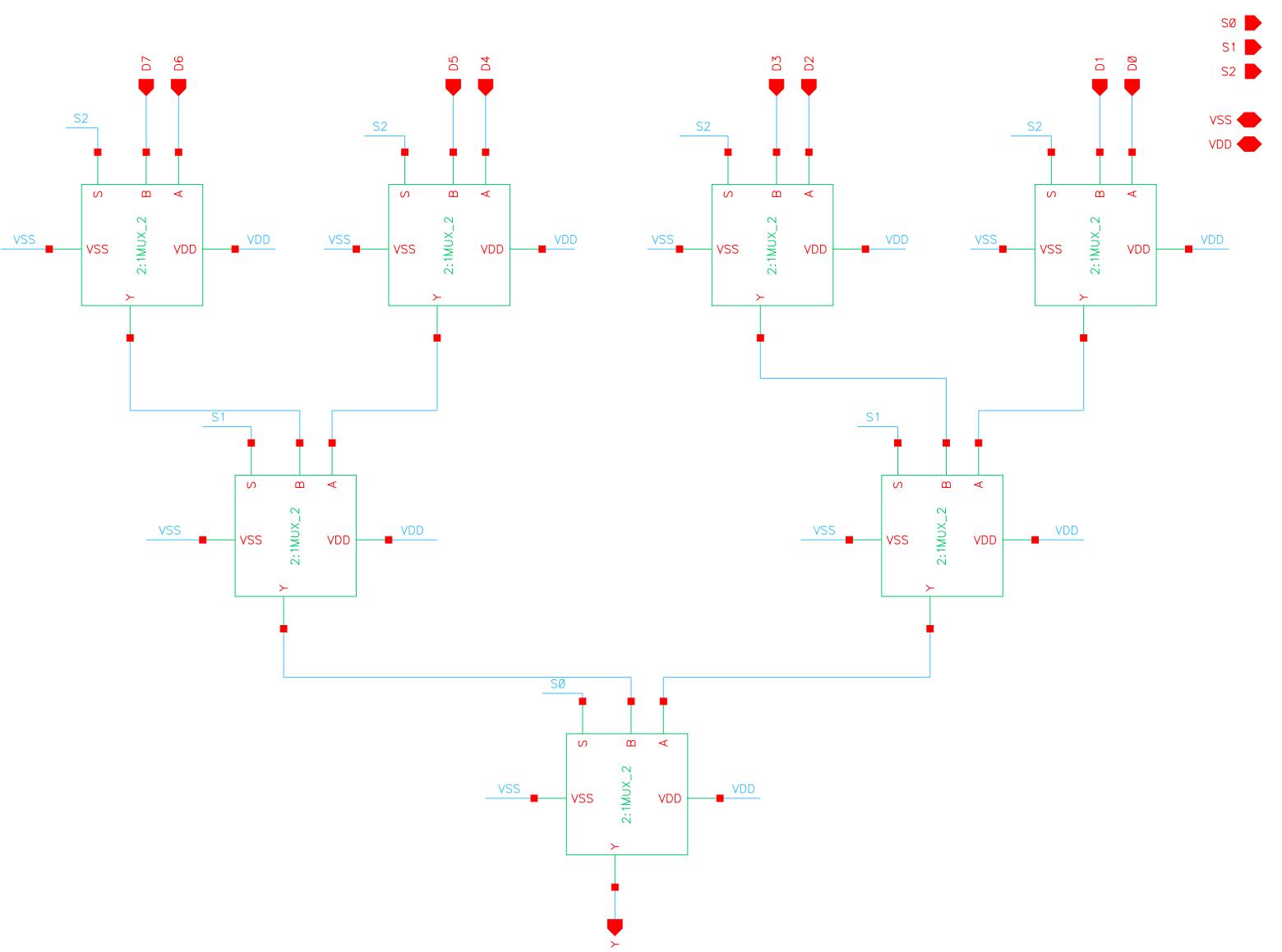
| | |
|--------|---|
| ■ /IN2 | ● |
|--------|---|

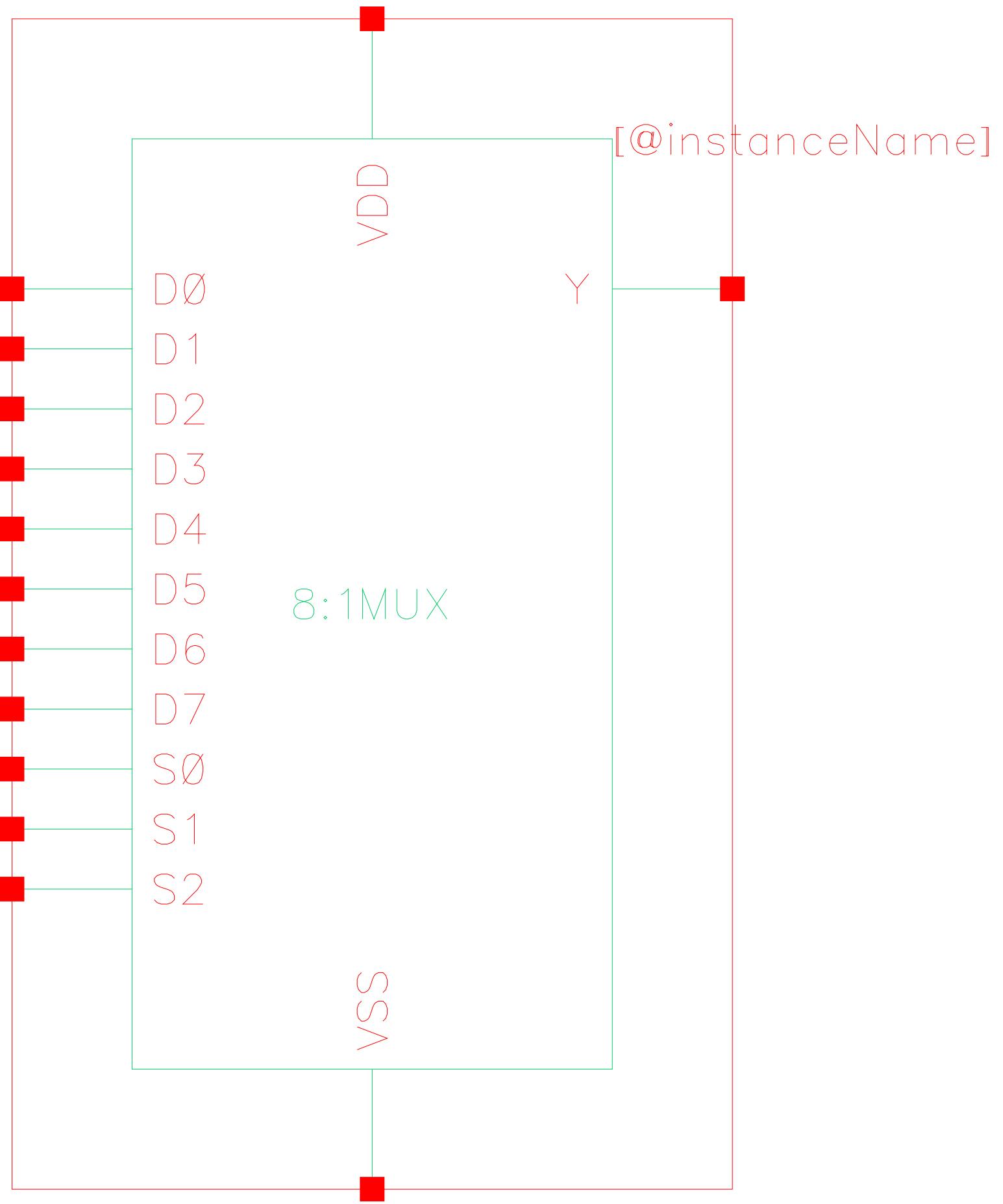


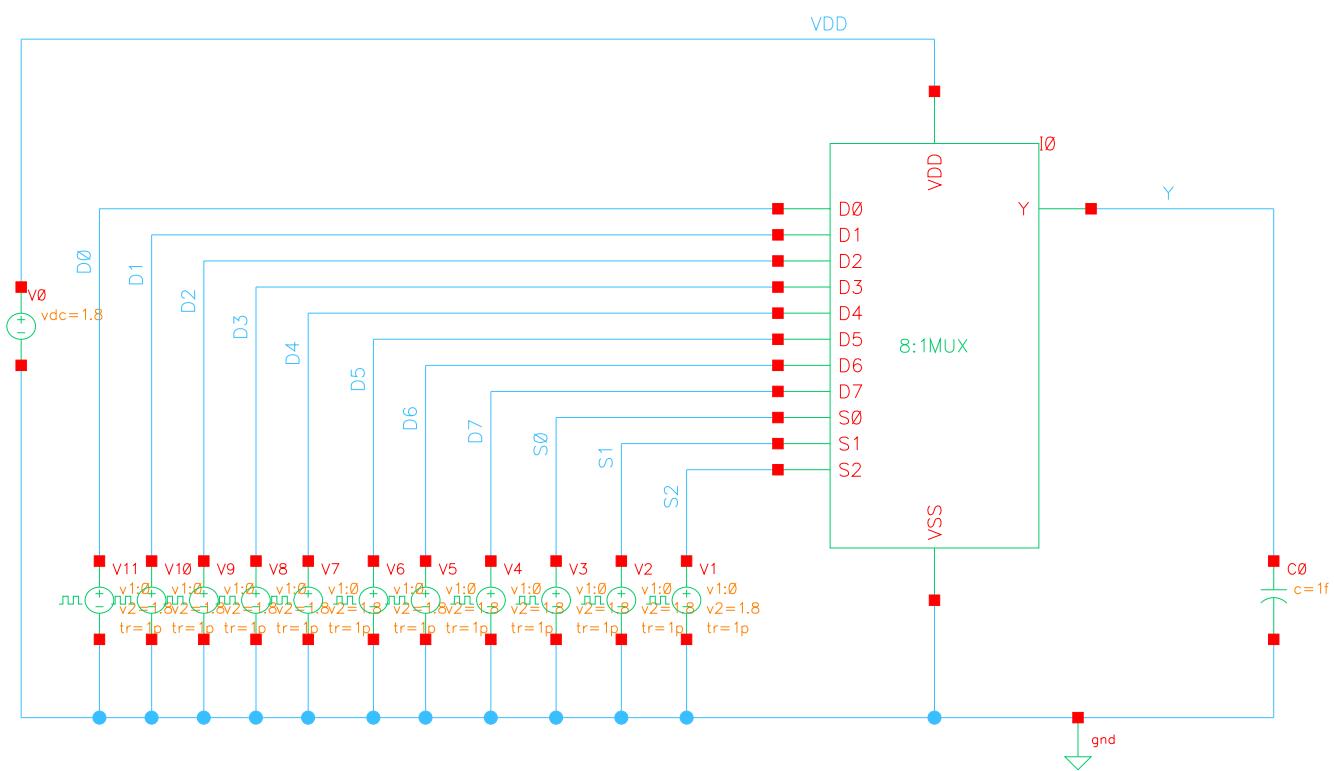
| | |
|--------|---|
| ■ /OUT | ● |
|--------|---|

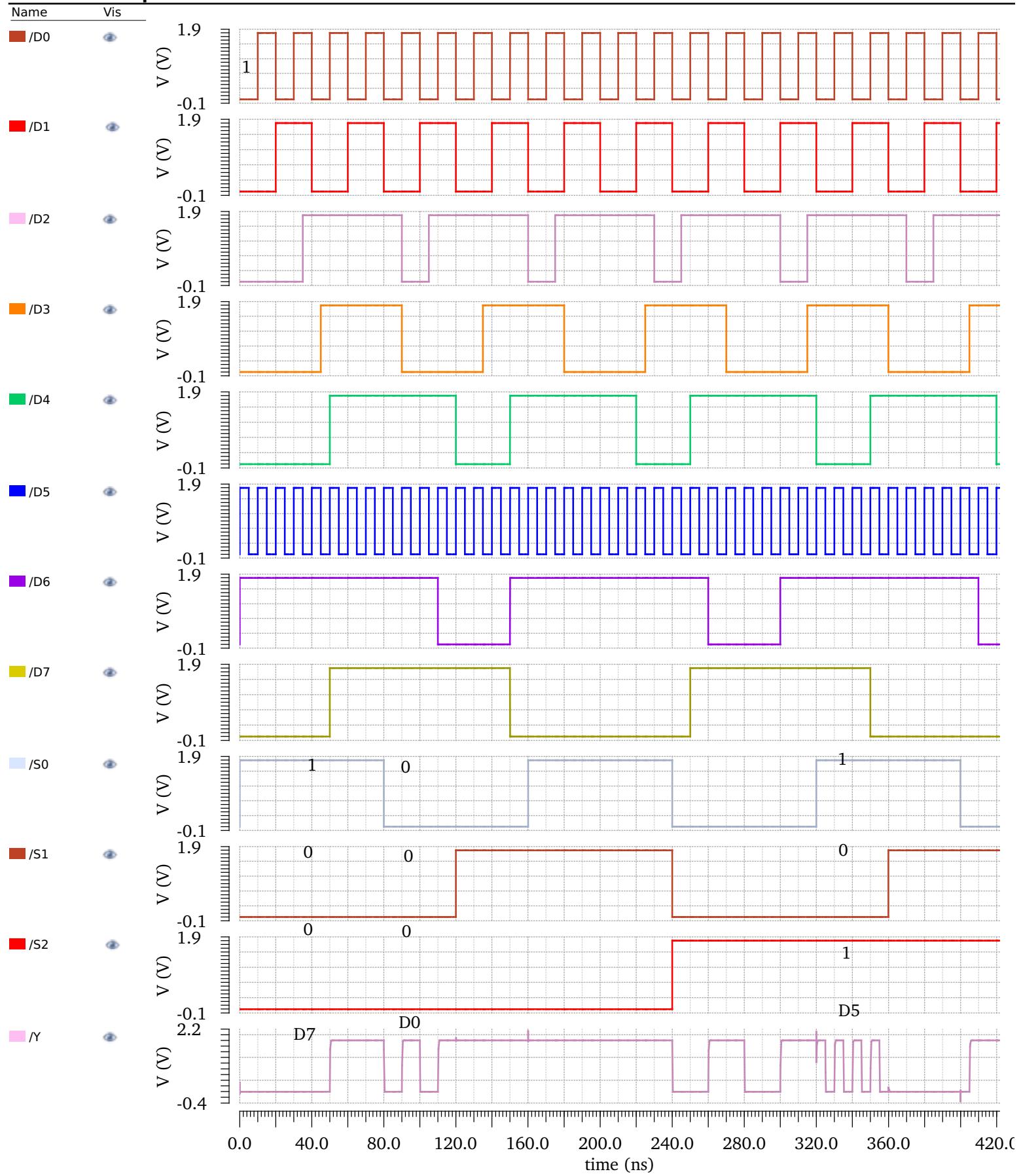


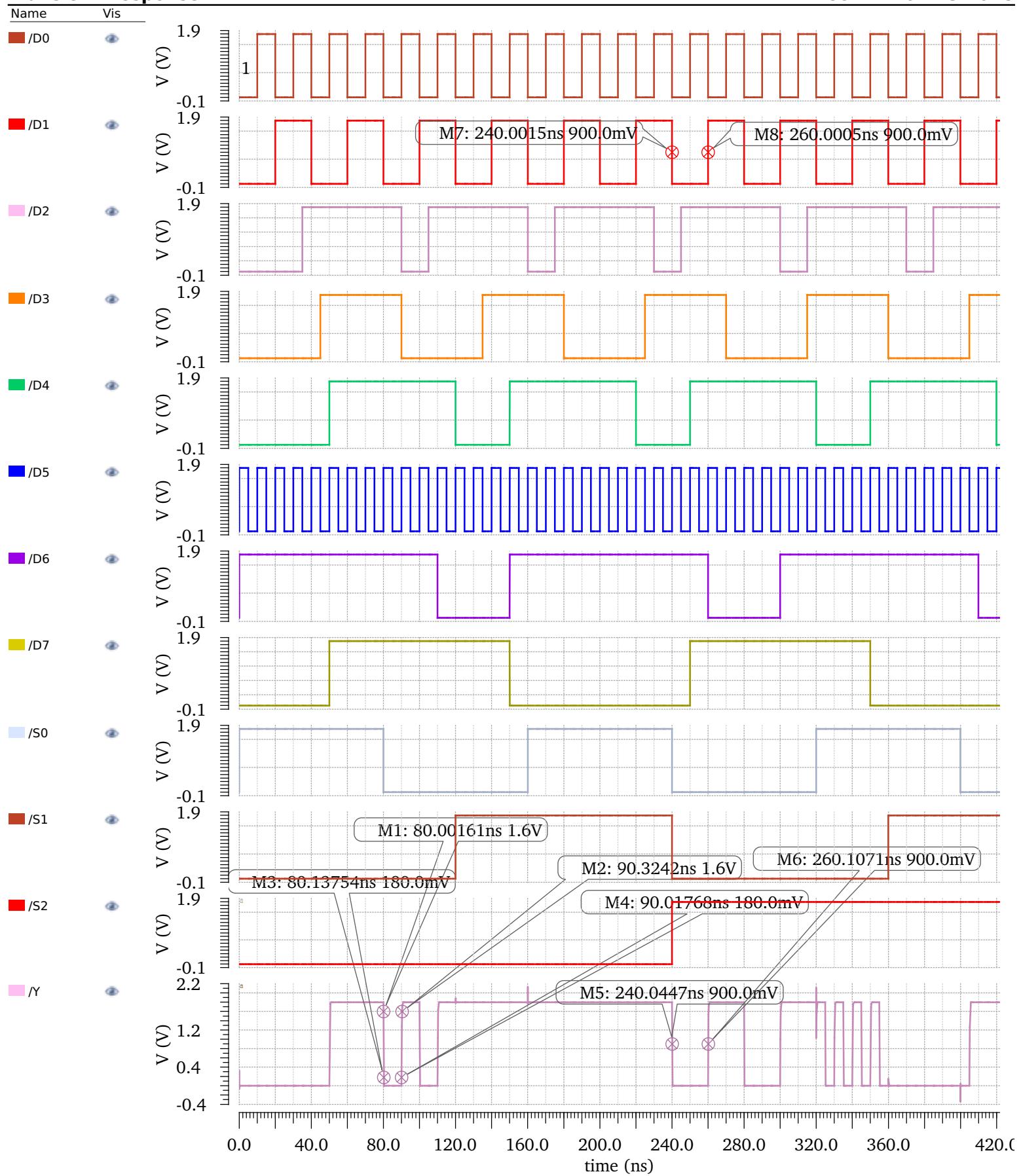
8:1 MUX

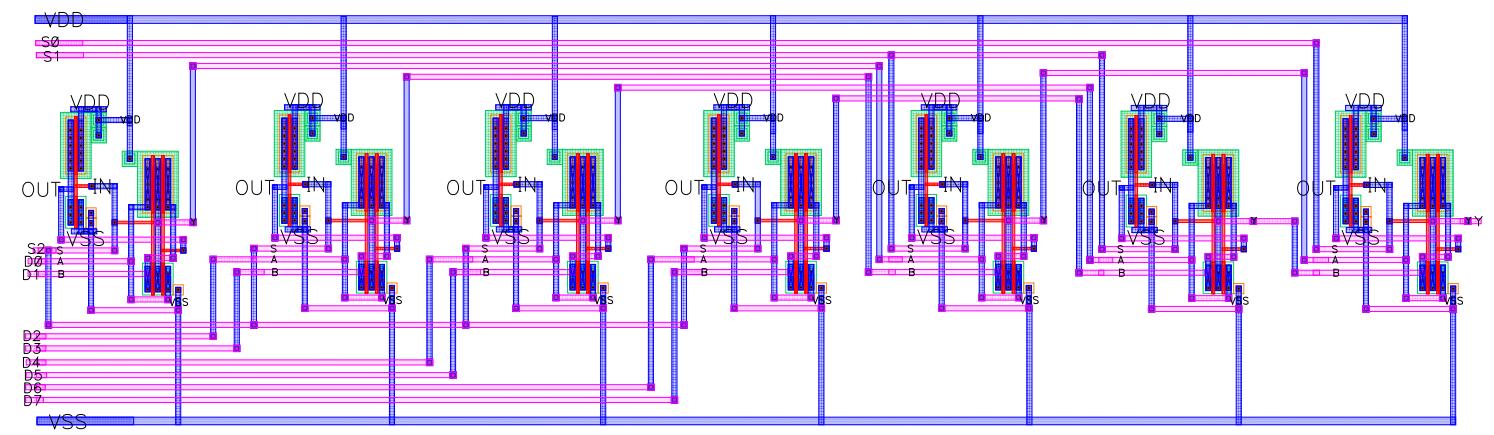






Transient Response**8:1 MUX Waveform****Fri Dec 7 21:07:43 2018**

Transient Response**8:1 MUX Waveform****Fri Dec 7 21:07:43 2018**



File Tools Options Help

cadence

```
DRC started.....Fri Dec 7 22:27:14 2018
completed ....Fri Dec 7 22:27:14 2018
CPU TIME = 00:00:00  TOTAL TIME = 00:00:00
***** Summary of rule violations for cell "8:1MUX_Layout layout" *****
Total errors found: 0
```

mouse L:showClickInfo()

M: setDRCForm()

R: _IxHiMousePopUp()

1 >

@(#)\$CDS: LVS version 6.1.7-64b 09/27/2016 19:41 (sjfhw305) \$

Command line: /software/cadence/install/IC617/tools.lnx86/dfl/bin/64bit/LVS -dir
/gaia/class/student/mahajanm/EEE_234_Project1/LVS -l -s -t
/gaia/class/student/mahajanm/EEE_234_Project1/LVS/layout
/gaia/class/student/mahajanm/EEE_234_Project1/LVS/schematic

Like matching is enabled.

Net swapping is enabled.

Using terminal names as correspondence points.

Compiling Diva LVS rules...

Net-list summary for /gaia/class/student/mahajanm/EEE_234_Project1/LVS/layout/netlist

count

| | |
|----|-----------|
| 27 | nets |
| 14 | terminals |
| 21 | pmos |
| 21 | nmos |

Net-list summary for /gaia/class/student/mahajanm/EEE_234_Project1/LVS/schematic/netlist

count

| | |
|----|-----------|
| 27 | nets |
| 14 | terminals |
| 21 | pmos |
| 21 | nmos |

Terminal correspondence points

| | | |
|-----|-----|----|
| N25 | N7 | D0 |
| N24 | N4 | D1 |
| N23 | N1 | D2 |
| N22 | N5 | D3 |
| N21 | N18 | D4 |
| N20 | N8 | D5 |

| | | |
|-----|-----|-----|
| N19 | N3 | D6 |
| N18 | N19 | D7 |
| N15 | N10 | S0 |
| N14 | N13 | S1 |
| N13 | N14 | S2 |
| N26 | N2 | VDD |
| N16 | N15 | VSS |
| N17 | N0 | Y |

Devices in the rules but not in the netlist:

```
cap nfet pfet nmos4 pmos4
```

The net-lists match.

layout schematic

instances

| | | |
|-------------|----|----|
| un-matched | 0 | 0 |
| rewired | 0 | 0 |
| size errors | 0 | 0 |
| pruned | 0 | 0 |
| active | 42 | 42 |
| total | 42 | 42 |

nets

| | | |
|------------|----|----|
| un-matched | 0 | 0 |
| merged | 0 | 0 |
| pruned | 0 | 0 |
| active | 27 | 27 |
| total | 27 | 27 |

terminals

| | | |
|------------|---|---|
| un-matched | 0 | 0 |
|------------|---|---|

| | | |
|----------------|----|----|
| matched but | | |
| different type | 0 | 0 |
| total | 14 | 14 |

Probe files from /gaia/class/student/mahajanm/EEE_234_Project1/LVS/schematic

devbad.out:

netbad.out:

mergenet.out:

termbad.out:

prunenet.out:

prunedev.out:

audit.out:

Probe files from /gaia/class/student/mahajanm/EEE_234_Project1/LVS/layout

devbad.out:

netbad.out:

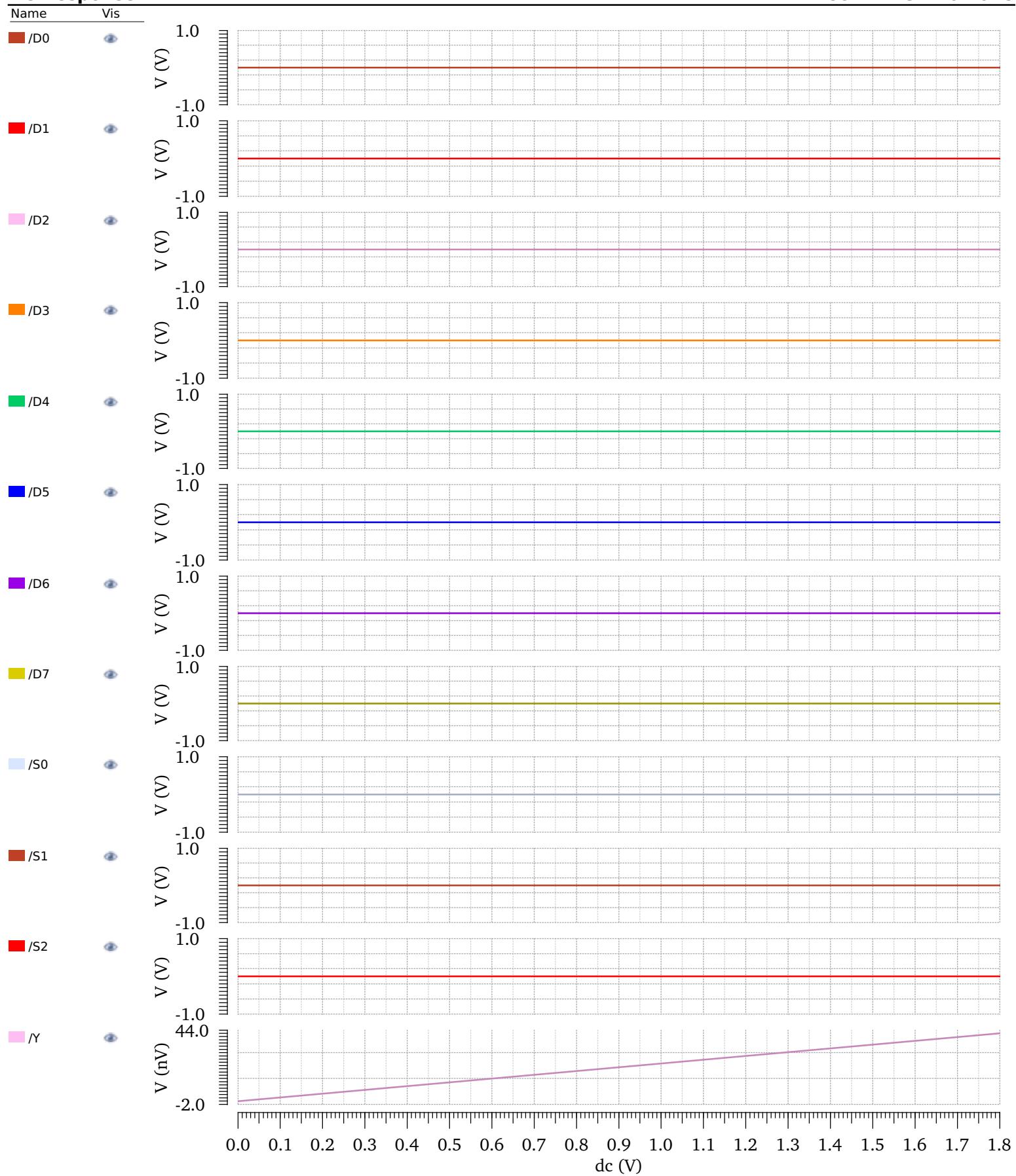
mergenet.out:

termbad.out:

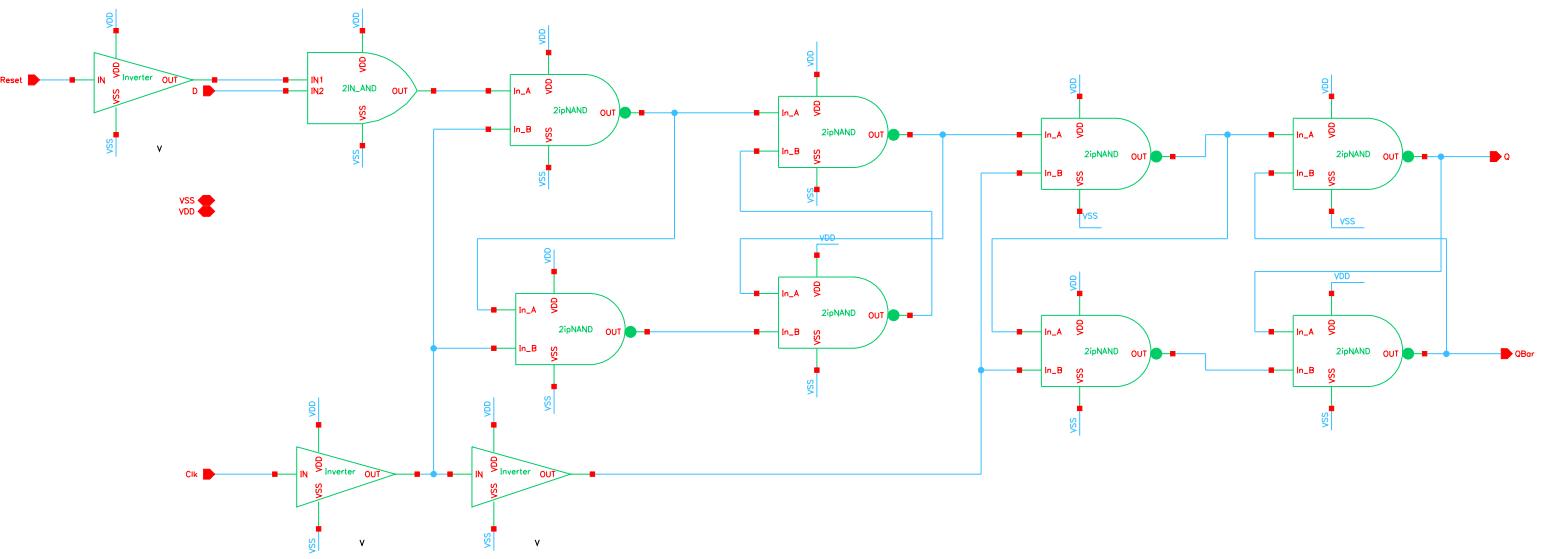
prunenet.out:

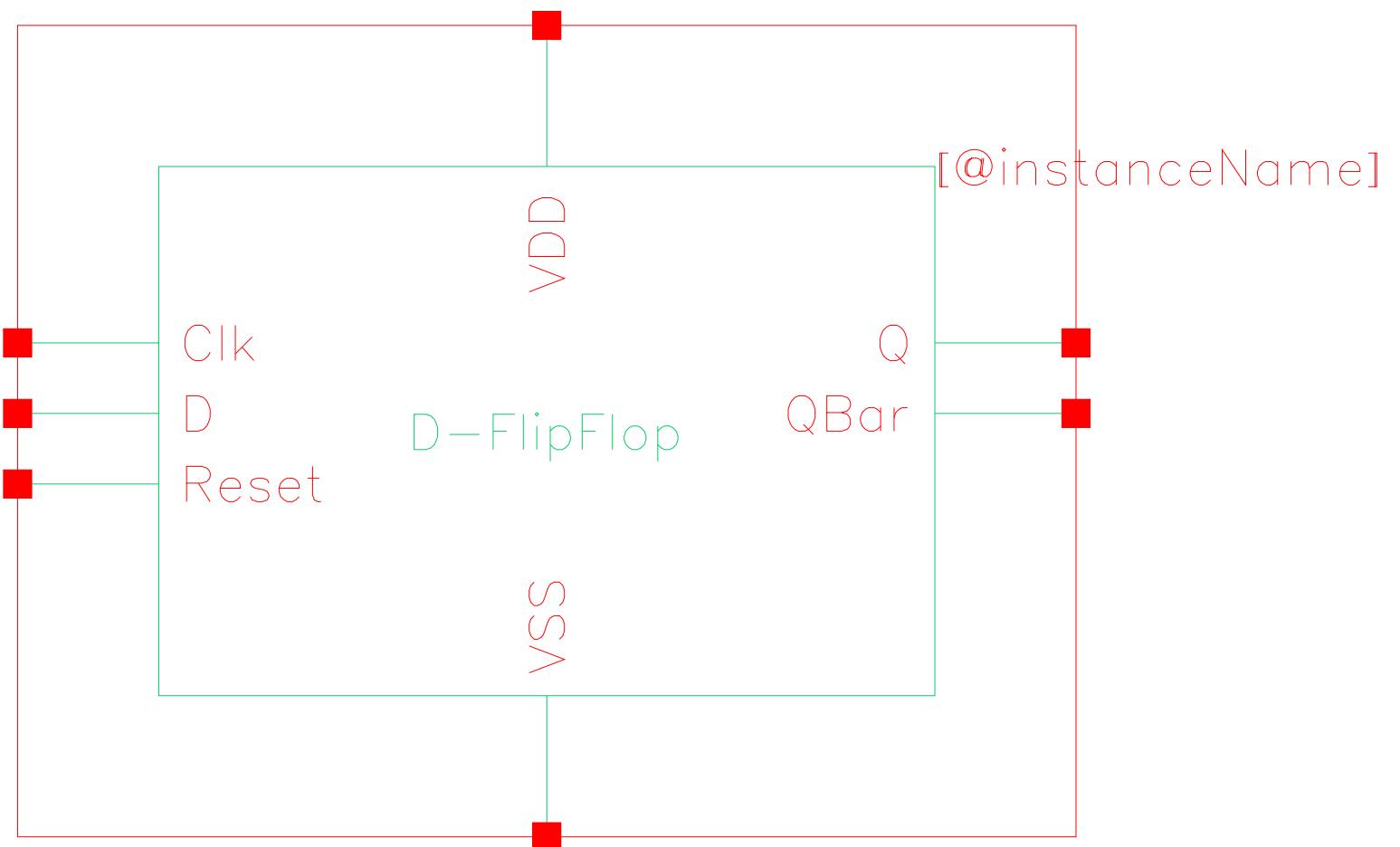
prunedev.out:

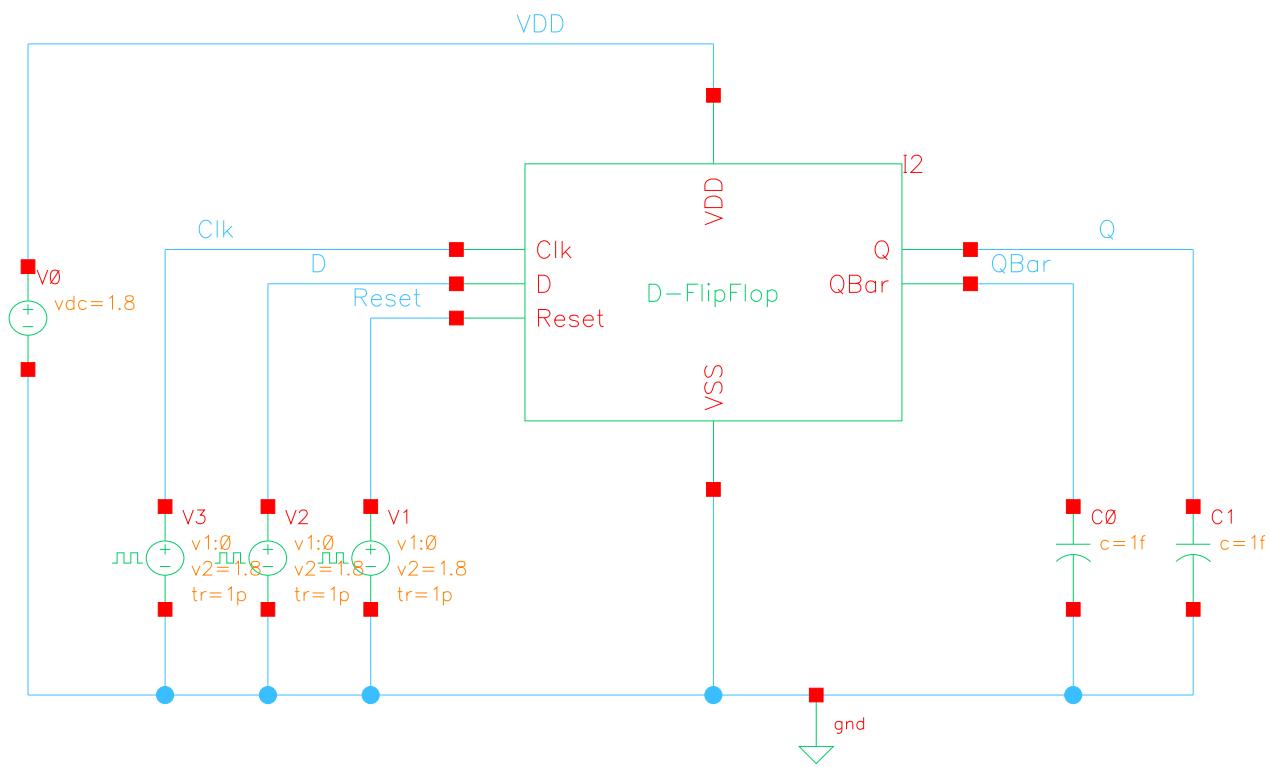
audit.out:

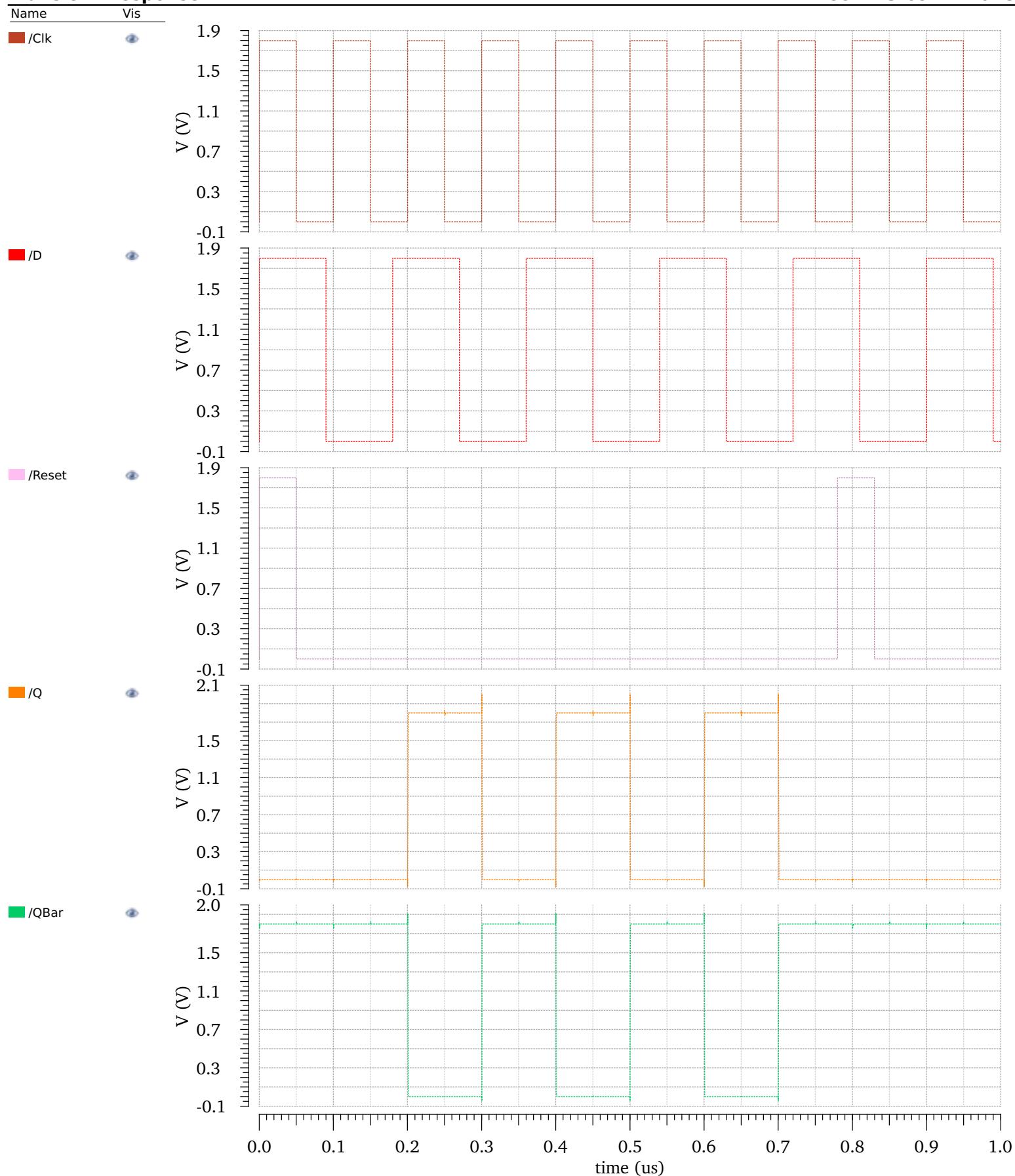
DC Response**8:1 MUX DC Waveform****Fri Dec 7 21:37:46 2018**

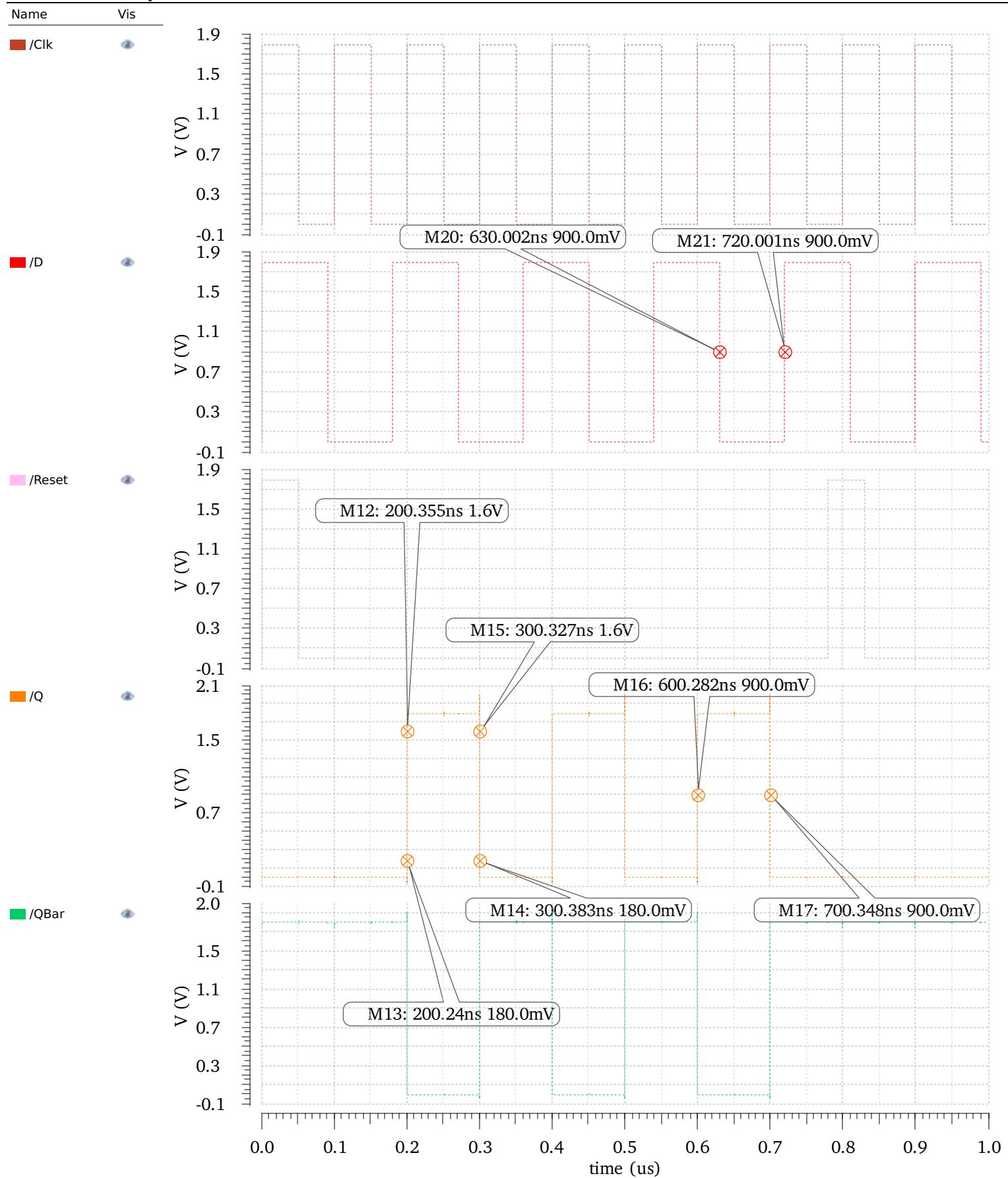
D Flip Flop

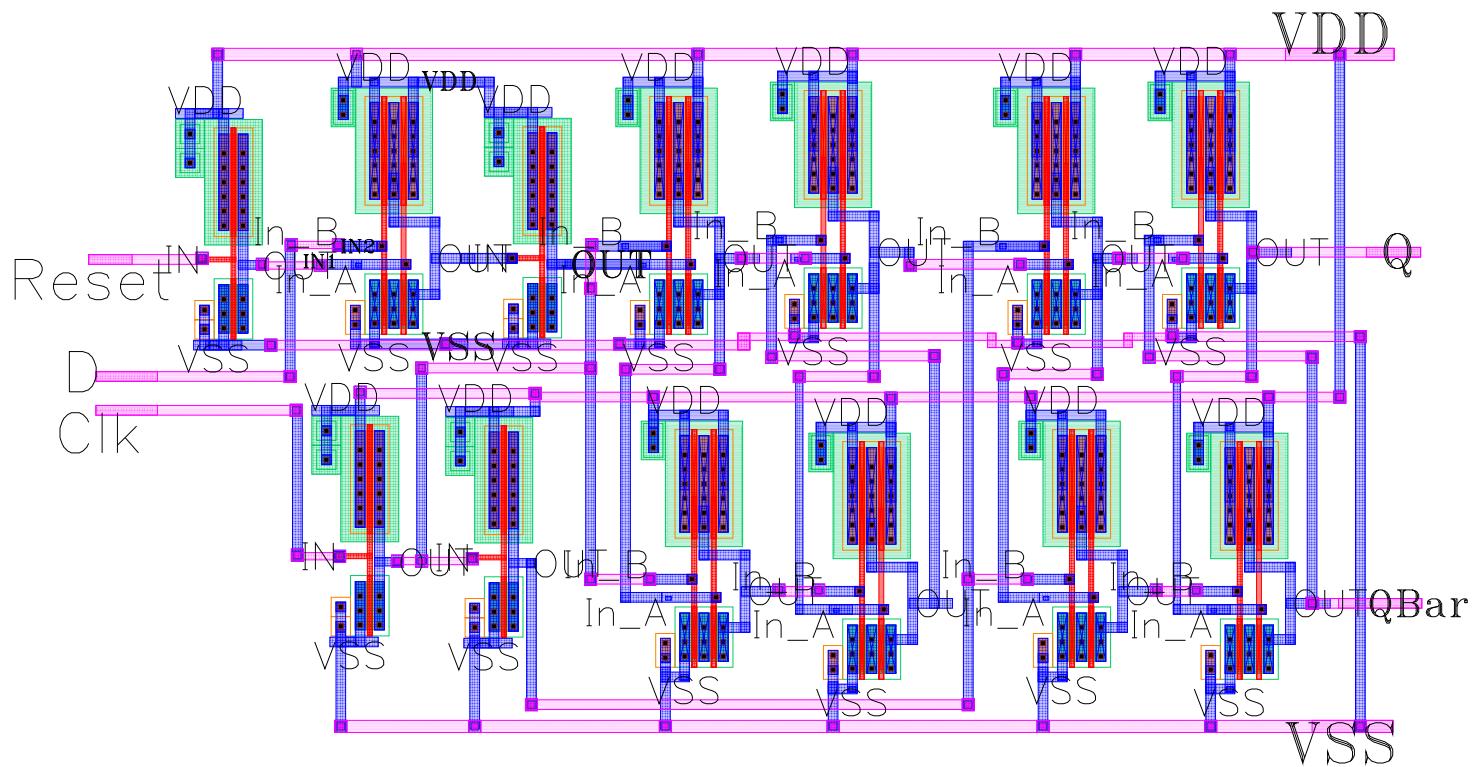






Transient Response**Fri Dec 7 23:09:24 2018**

Transient Response**Fri Dec 7 23:09:24 2018**



@(#)\$CDS: LVS version 6.1.7-64b 09/27/2016 19:41 (sjfhw305) \$

Command line: /software/cadence/install/IC617/tools.lnx86/dfl/bin/64bit/LVS -dir
/gaia/class/student/mahajanm/EEE_234_Project1/LVS -l -s -t
/gaia/class/student/mahajanm/EEE_234_Project1/LVS/layout
/gaia/class/student/mahajanm/EEE_234_Project1/LVS/schematic

Like matching is enabled.

Net swapping is enabled.

Using terminal names as correspondence points.

Net-list summary for /gaia/class/student/mahajanm/EEE_234_Project1/LVS/layout/netlist

| count | |
|-------|-----------|
| 27 | nets |
| 7 | terminals |
| 22 | pmos |
| 22 | nmos |

Net-list summary for /gaia/class/student/mahajanm/EEE_234_Project1/LVS/schematic/netlist

| count | |
|-------|-----------|
| 27 | nets |
| 7 | terminals |
| 22 | pmos |
| 22 | nmos |

Terminal correspondence points

| | | |
|-----|-----|-------|
| N24 | N4 | Clk |
| N23 | N14 | D |
| N22 | N2 | Q |
| N21 | N15 | QBar |
| N26 | N16 | Reset |
| N25 | N11 | VDD |
| N20 | N12 | VSS |

Devices in the netlist but not in the rules:

pmos nmos

The net-lists match.

layout schematic

instances

| | | |
|-------------|----|----|
| un-matched | 0 | 0 |
| rewired | 0 | 0 |
| size errors | 0 | 0 |
| pruned | 0 | 0 |
| active | 44 | 44 |
| total | 44 | 44 |

nets

| | | |
|------------|----|----|
| un-matched | 0 | 0 |
| merged | 0 | 0 |
| pruned | 0 | 0 |
| active | 27 | 27 |
| total | 27 | 27 |

terminals

| | | |
|-------------------------------|---|---|
| un-matched | 0 | 0 |
| matched but different type | 0 | 0 |
| total | 7 | 7 |

Probe files from /gaia/class/student/mahajanm/EEE_234_Project1/LVS/schematic

devbad.out:

netbad.out:

mergenet.out:

termbad.out:

prunenet.out:

prunedev.out:

audit.out:

Probe files from /gaia/class/student/mahajanm/EEE_234_Project1/LVS/layout

devbad.out:

netbad.out:

mergenet.out:

termbad.out:

prunenet.out:

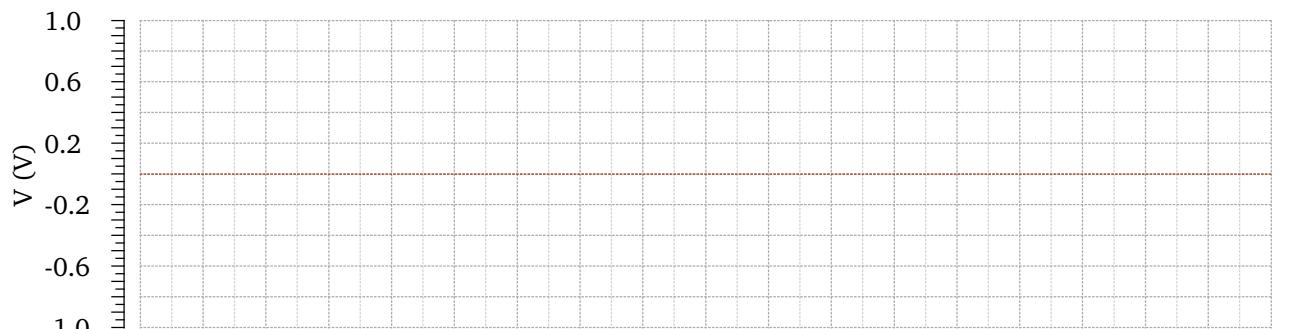
prunedev.out:

audit.out:

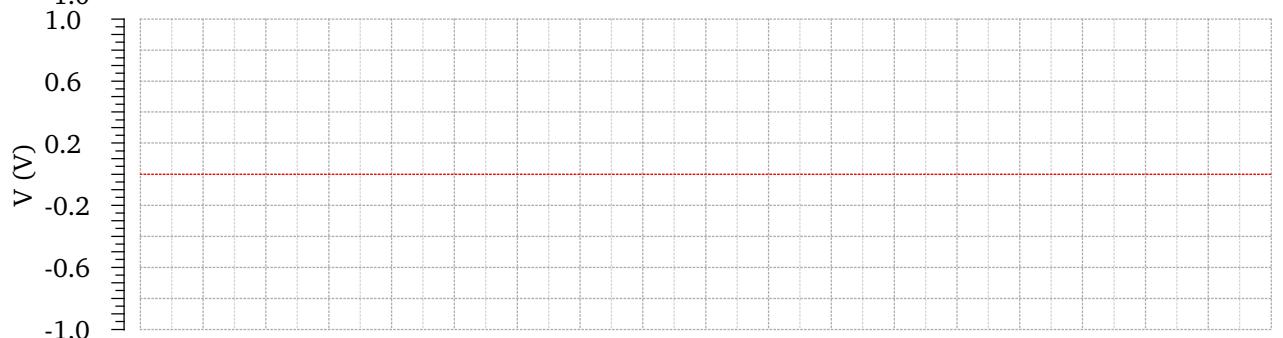
DC Response**Fri Dec 7 23:17:25 2018**

Name Vis

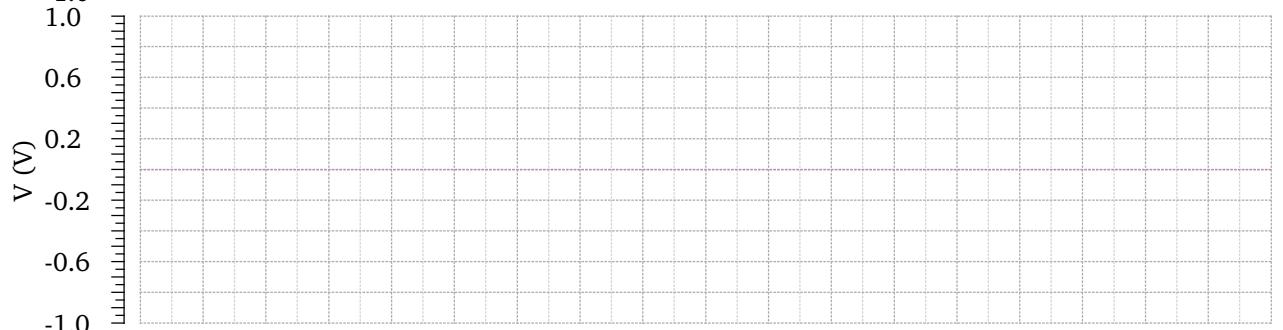
■ /Clk



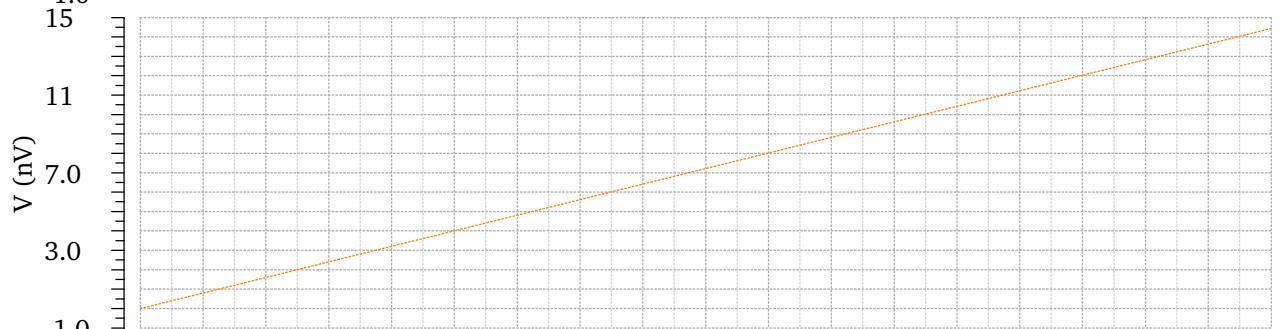
■ /D



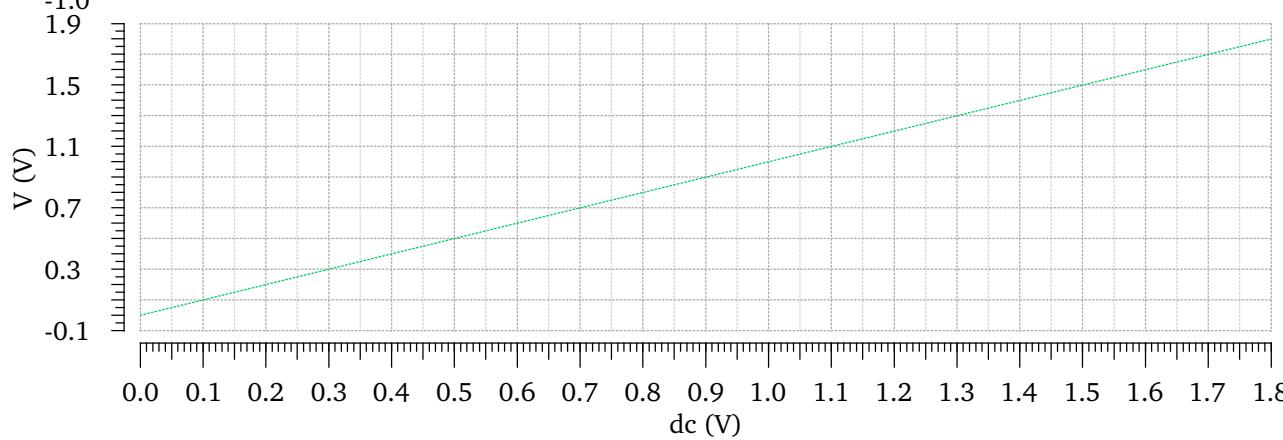
■ /Reset



■ /Q

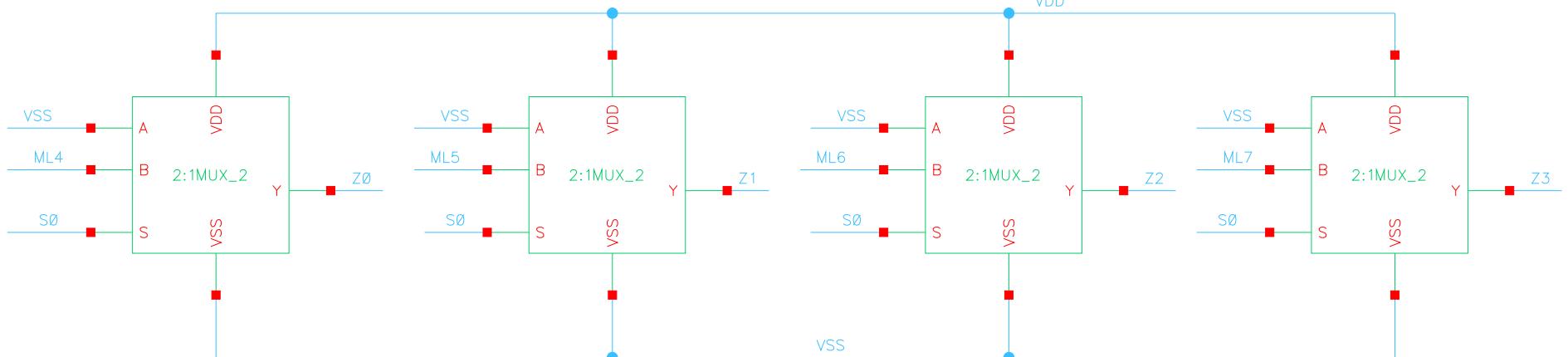
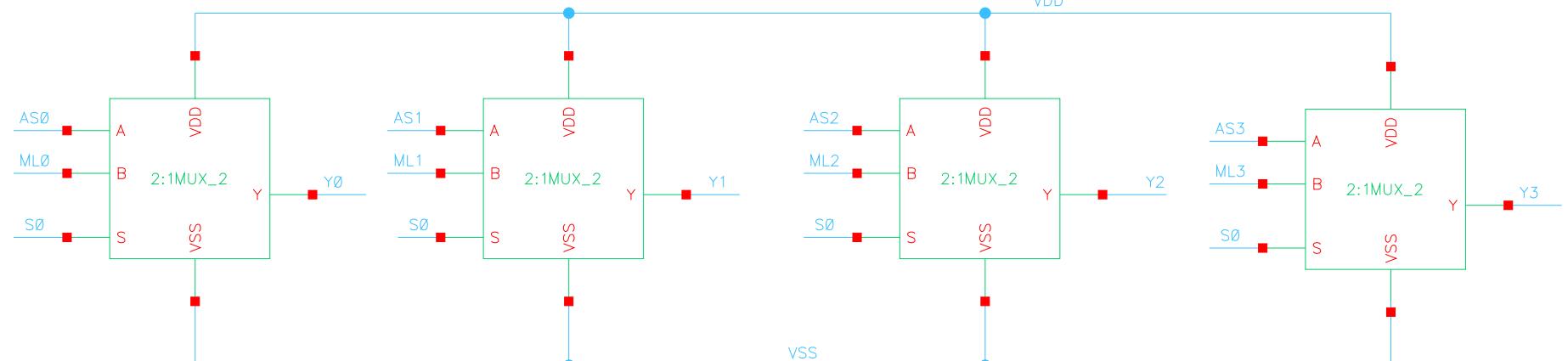
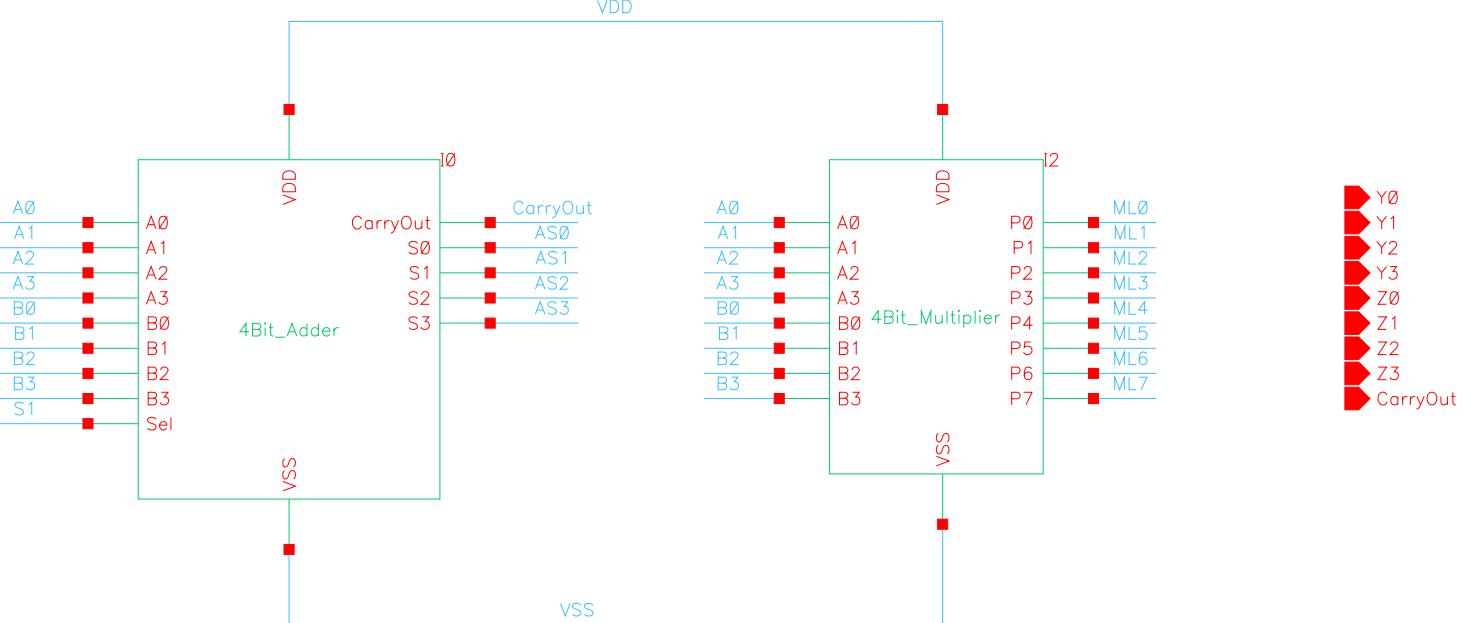


■ /QBar

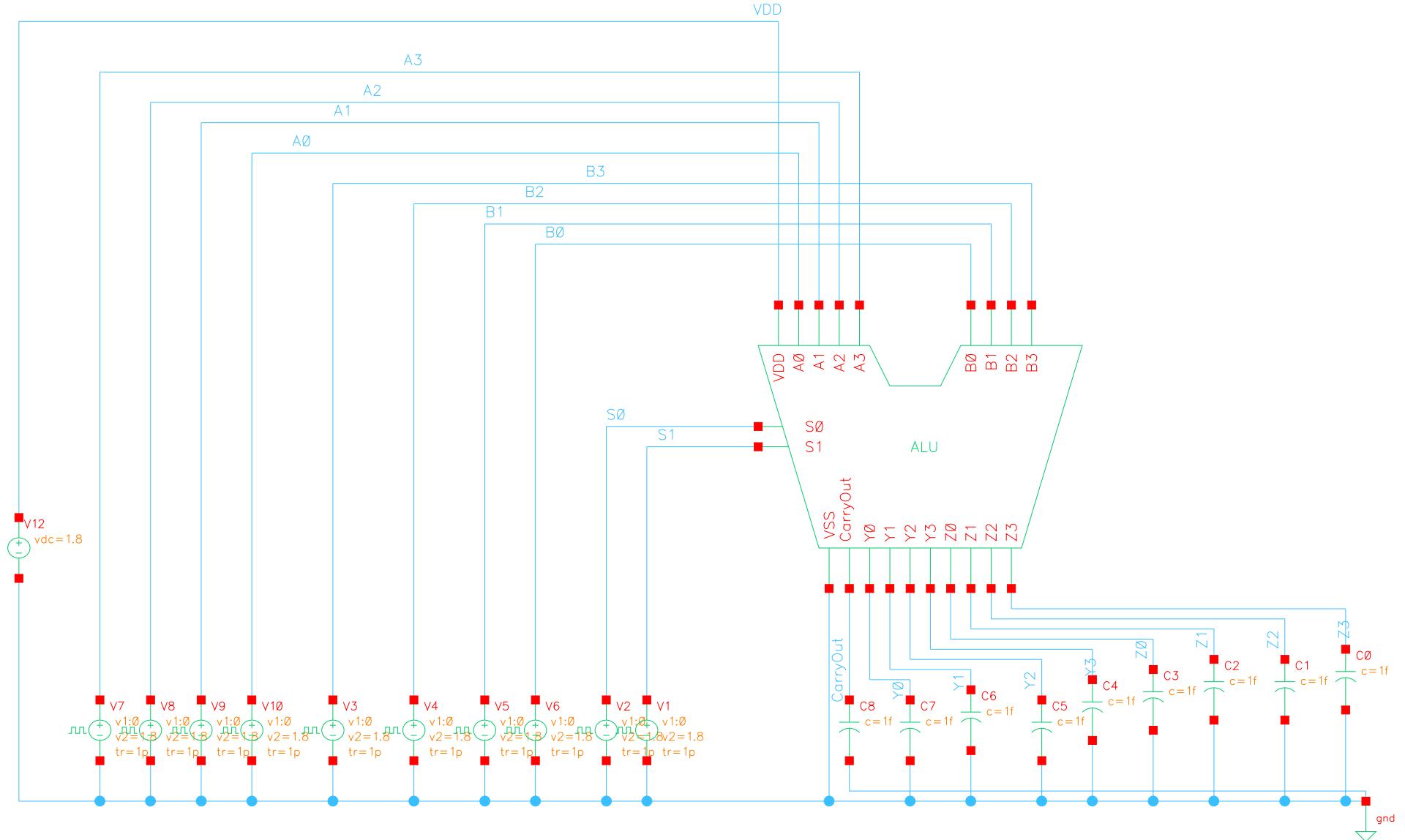


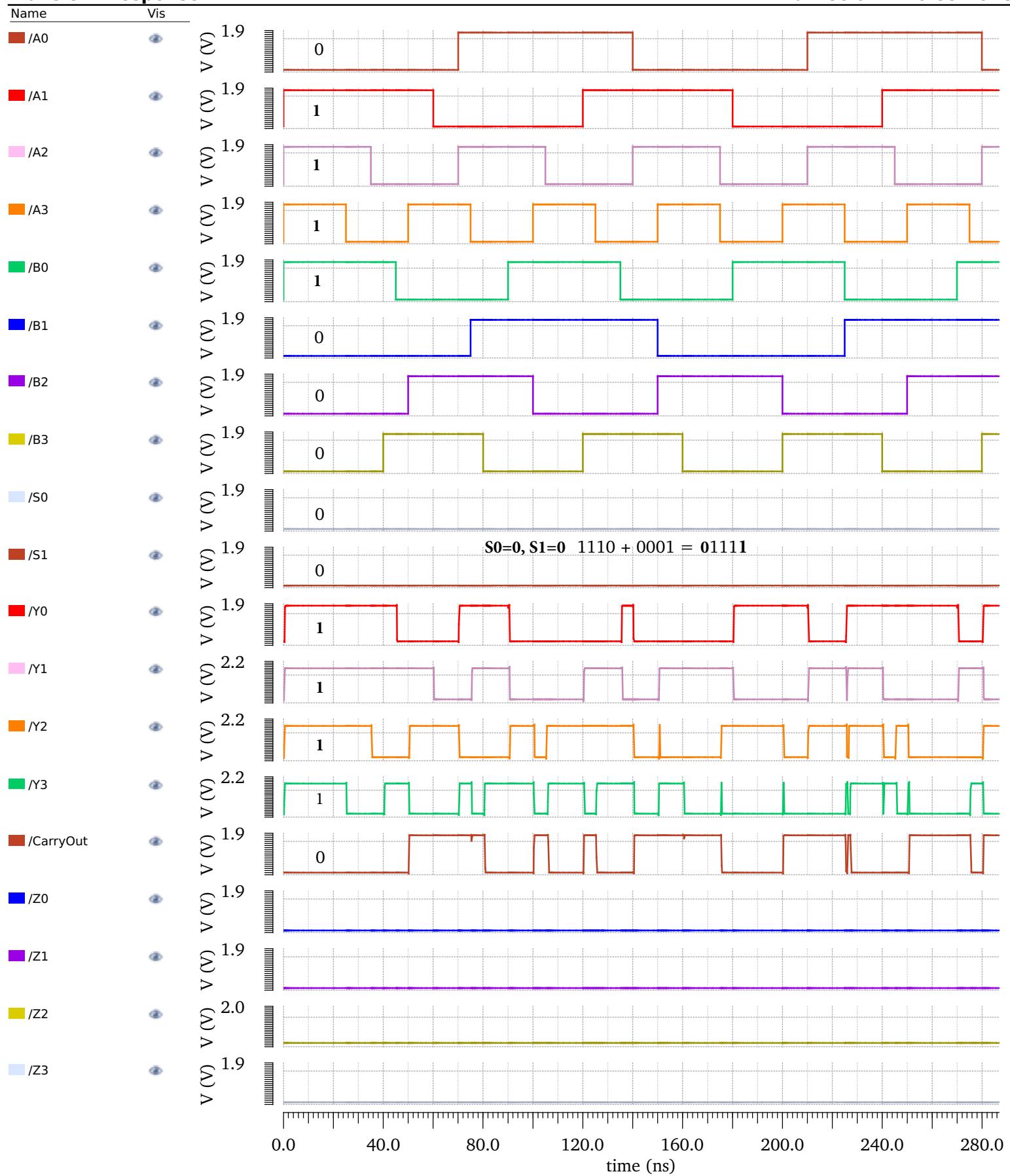
ALU

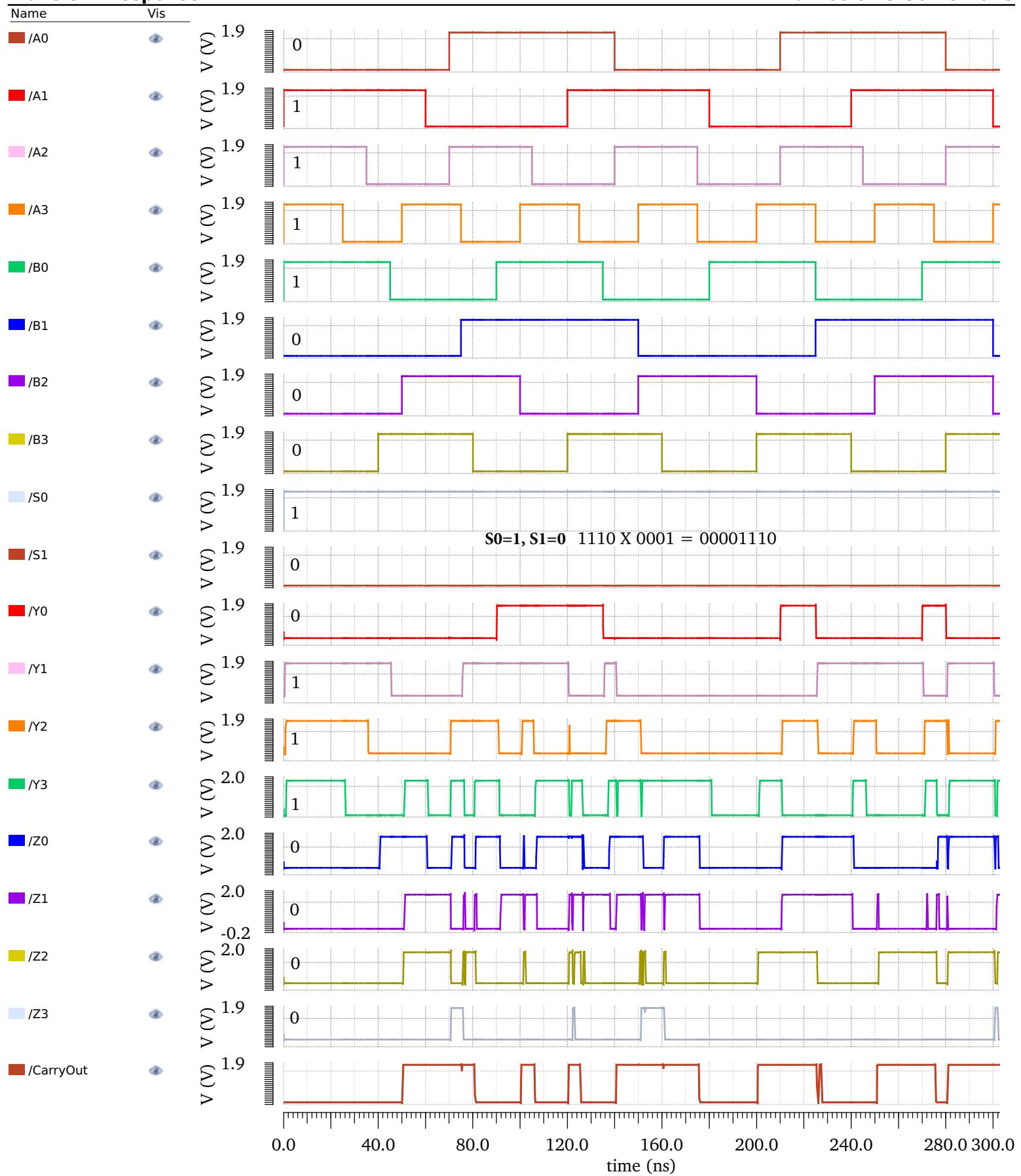
A_0
 A_1
 A_2
 A_3
 B_0
 B_1
 B_2
 B_3
 S_0
 S_1

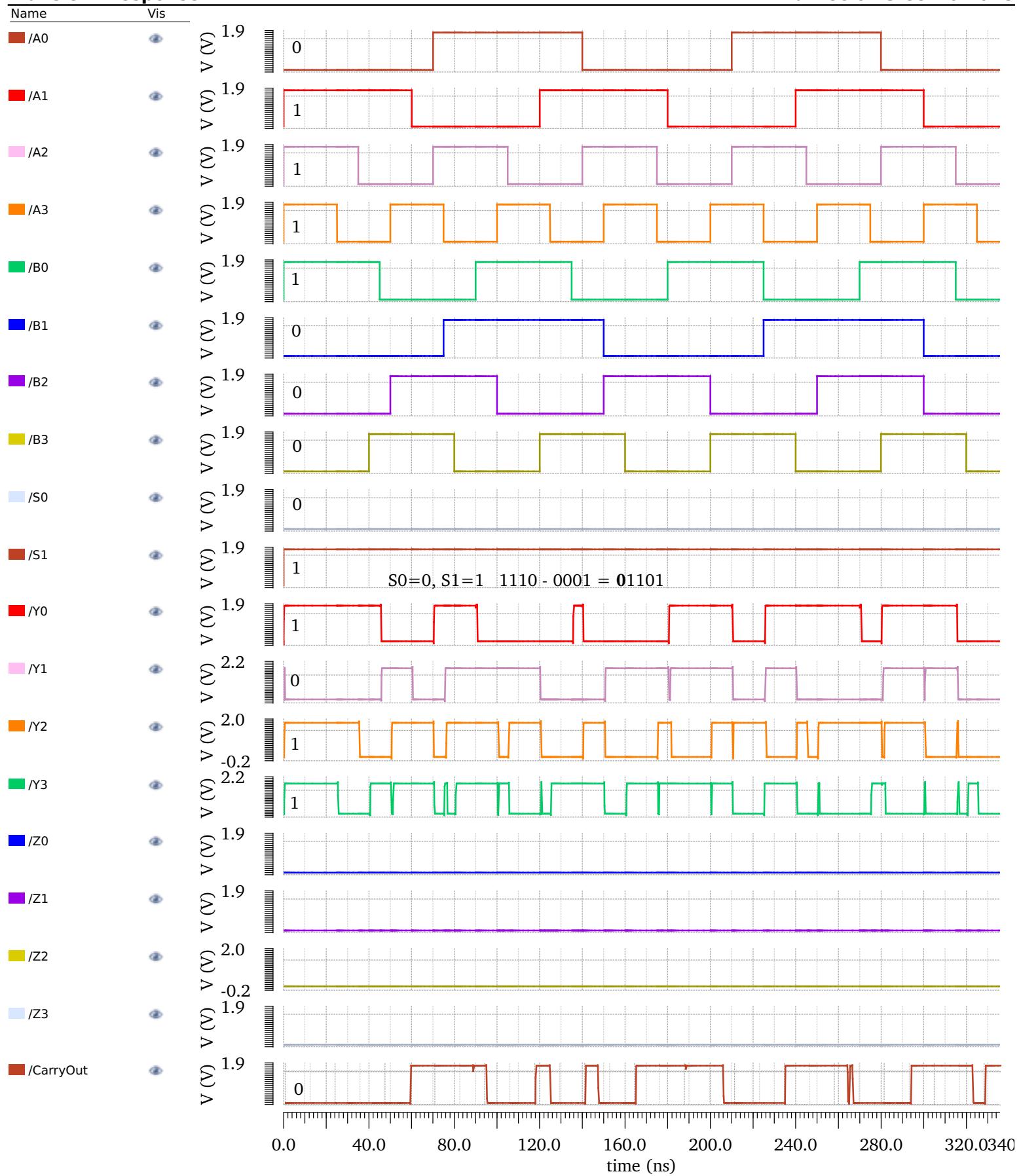


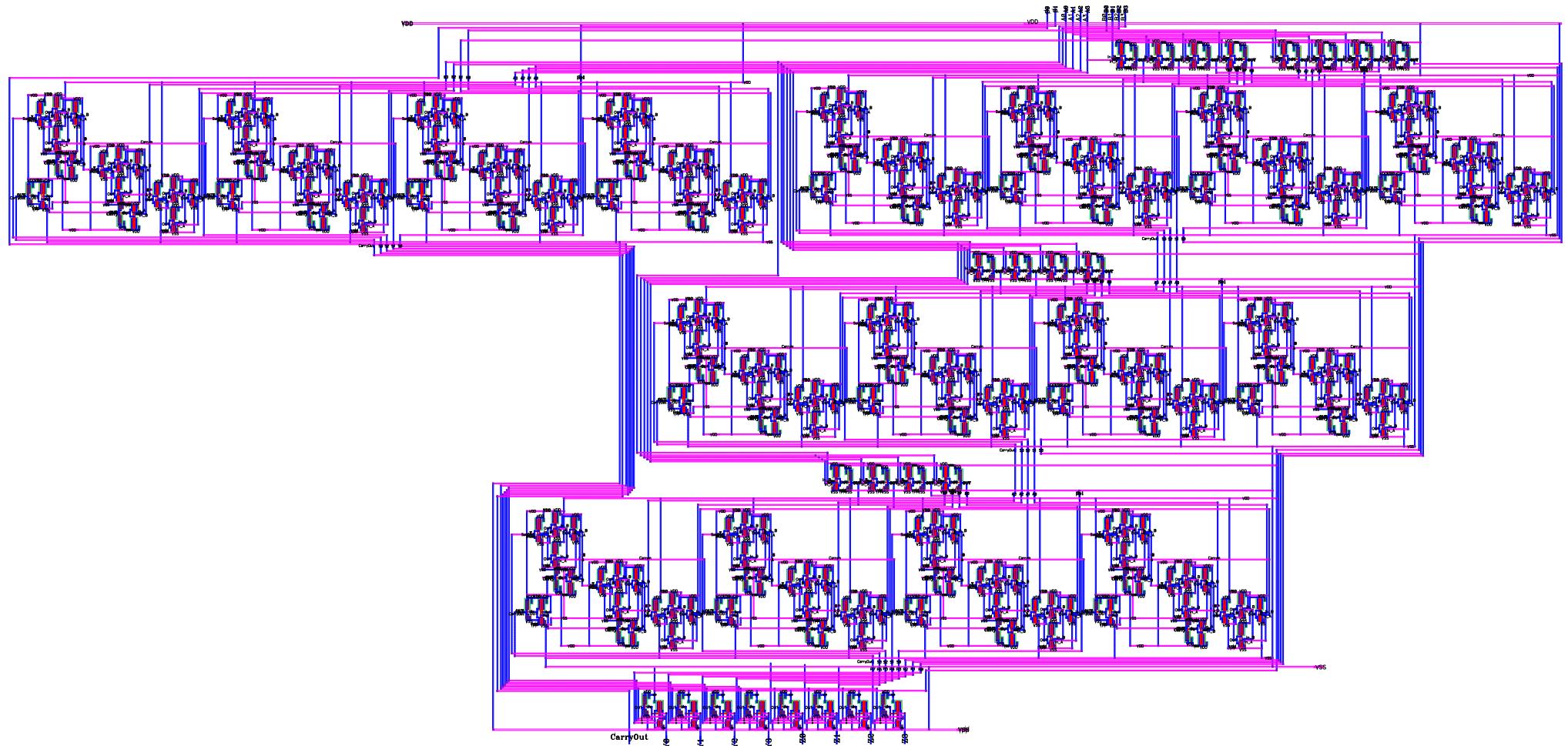
Y_0
 Y_1
 Y_2
 Y_3
 Z_0
 Z_1
 Z_2
 Z_3
 $CarryOut$



Transient Response**Thu Dec 6 22:26:59 2018**

Transient Response**Thu Dec 6 23:30:15 2018**

Transient Response**Thu Dec 6 23:59:26 2018**



Calculation

Rise Time and Fall Time Calculation

Rise Time= (at 90% Output) - (at 10% Output)

Fall Time = (at (10% Output) - (at 90% Output)

Propagation Delay

Propagation Delay(rising t_{pdr})= 50% of Output time - 50% of Input time

Propagation Delay(falling t_{pdf})= 50% of Output time - 50% of Input time

Average Propagation Delay = $(t_{pdr}+t_{pdf})/2$

| Gate | tr | tf | tpdr | tpdf | Average(Tpdr+tpdf)/2 |
|---------------------------|---------|--------|--------|---------|----------------------|
| Inverter | 2.17ns | 1.67ns | 1.02ns | 0.9ns | 0.96ns |
| NAND | 2.20ns | 0.99ns | 1.05ns | 0.519ns | 0.788ns |
| AND | 0.7ns | 0.6ns | 0.89ns | 1.025ns | 0.95ns |
| NOR | 3.26ns | 0.57ns | 1.56ns | 0.31ns | 0.936ns |
| OR | 0.457ns | 0.17ns | 0.36ns | 0.06ns | 0.21s |
| XOR | 2.17ns | 1.67ns | 0.9ns | 1.02ns | 0.96ns |
| TM Gate | 0.32ns | 0.2ns | 0.12ns | 0.079ns | 0.095ns |
| 1 Bit Half Adder | 24ns | 1.05ns | 0.15ns | 0.24ns | 0.19ns |
| 1 Bit Full Adder | 18ns | 0.09ns | 0.36ns | 0.34ns | 0.35ns |
| 4 Bit Fuller Adder | 0.1ns | 1.05ns | 1.42ns | 1.00ns | 2.71ns |
| Multiplier | 0.17ns | 0.36ns | 0.36ns | 0.93ns | 0.645ns |
| D Flip-Flop | 1.29ns | 1.02ns | 2.65ns | 1.26ns | 1.95 |
| 2:1 MUX | 0.59ns | 0.43ns | 1.02ns | 0.59ns | 0.805ns |
| 8:1 MUX | 0.12ns | 0.25ns | 0.04ns | 0.107ns | 0.03ns |
| ALU | 0.1ns | 0.54ns | 0.3ns | 0.667ns | 0.48ns |

CONCLUSION:

Thus the layout of the ALU is designed using the basic gates and the Post Simulation results are obtained.