

Low-Power Spiking Neural Network with Clock-gating technique

S1290033

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Content

- Research Introduction
- Network
- Clock gating
- Logical synthesis of clock-gated design
- Research progress
 - Done
 - Doing
 - Todo
- Schedule

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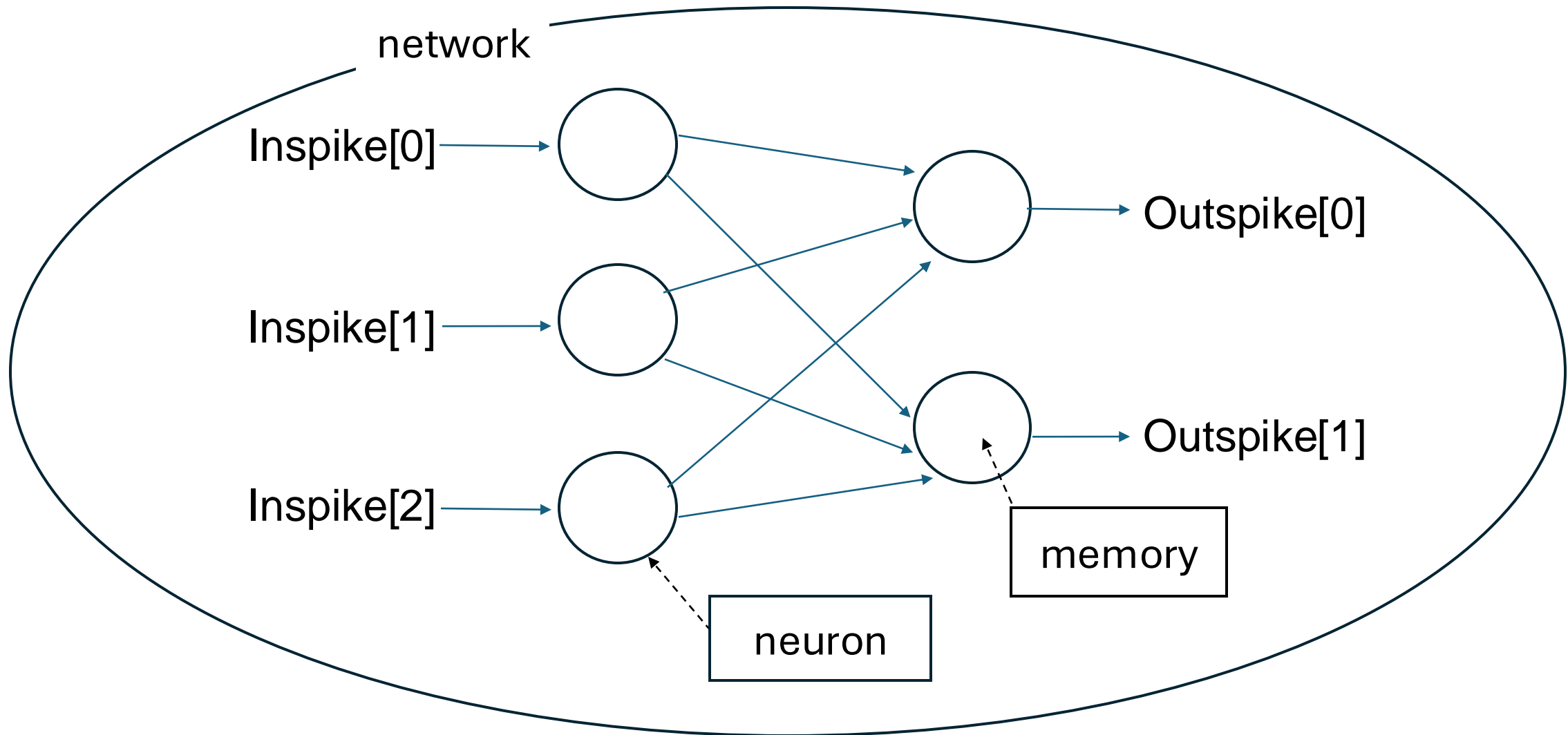
Research introduction

- My research is about clock gating in LIF neuron.
- My goal is to reduce power consumption.

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Network (1)



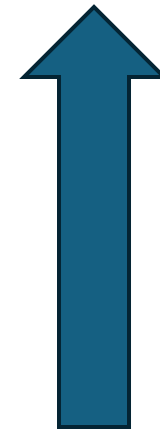
Network (2)

network.v

neuron.v

memory.v

Upper



Lower

Content

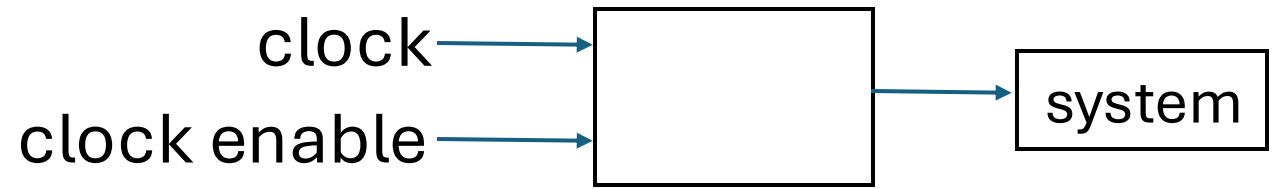
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Clock gating

Conventional system



Clock-gated system




- Can save dynamic power by turning off clock enable signal.
- No computation is done while clock enable signal is off.

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Logical synthesis of clock-gated network

- Change compared with previous synthesis

Clock gating cell: AND2_X1  CGLPPRX2

- Power

Dynamic power: 979.7480 μ W

Static power: 4.0211e04 nW

Total power: 1.0200e03 μ W

- Area

Combinational cell area: 682.2900

Noncombinational cell area: 1411.6620

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Research Progress | Done

- Coding in verilog hdl
- RTL simulation
- Synthesis
- Post-synthesis simulation
- Power estimation
- Application of clock gating
- Logical synthesis

Research Progress | Doing

- Creation of tutorial on clock gating
- PyTorch

Research Progress | Todo

- Physical synthesis
- SNN Torch

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- **Schedule**

Schedule

Task	Deadline
Creation of tutorial	13 August 2024
PyTorch	
Physical synthesis	
SNNTorch	

Thank you for your attention!