The University of Aizu

Research Progress Seminar

Spiking Neural Network with 3-D IC-based Stacking Memory

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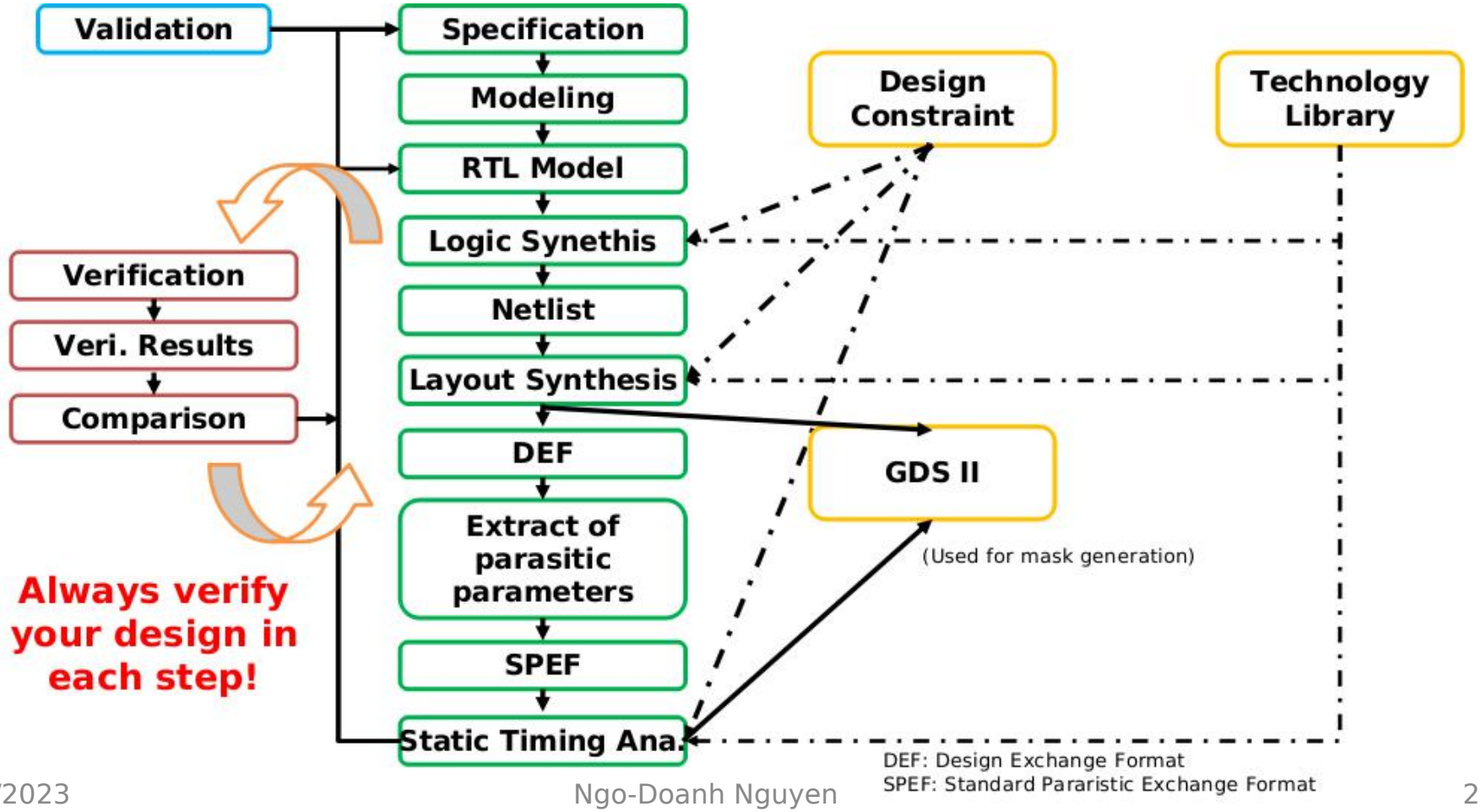
2023-02-17

Previous RPS (1)

- Introduce to hardware implementation flow

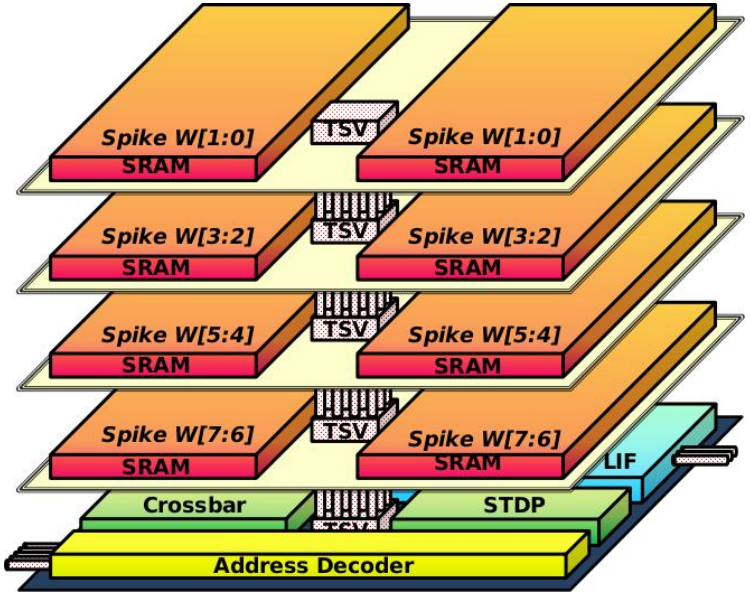


Previous RPS (2)

- Simulation tools (ModelSim, Iverilog + GTKwave,...)
  - Simulate RTL behavior
- Cadence Genus
  - RTL synthesis => Netlist (gate logic)
  - Approximate extract area, power, timing results
- Cadence Innovus
  - Layout synthesis => GDS (Graphic Data Stream)
  - Increase the accuracy of area, power, timing results

Progress (1)

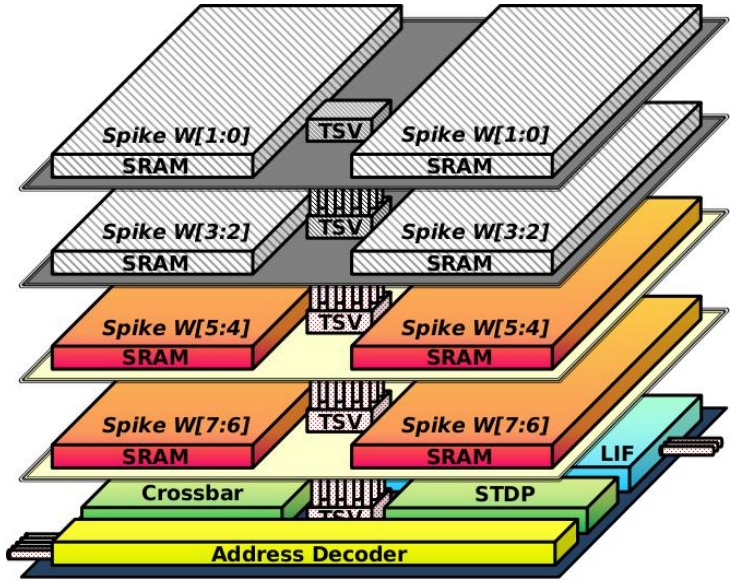
- Design: 3-D Synaptic Computing Core
  - SNPC core
  - 4x2-bit memory layers (8-bit synaptic weights)



SNPC Hardware Architecture

Progress (2)

- Extract SNPC power consumption with Cadance & Synopsis tools
  - All 4 memory layeres (8-bit)
  - 3 bottom memory layers (6-bit)
  - 2 bottom memory layers (4-bit)



SNPC without power supply for 2 upper mem. layer

Results (1)

- Power Estimation with PrimeTime Synopsys

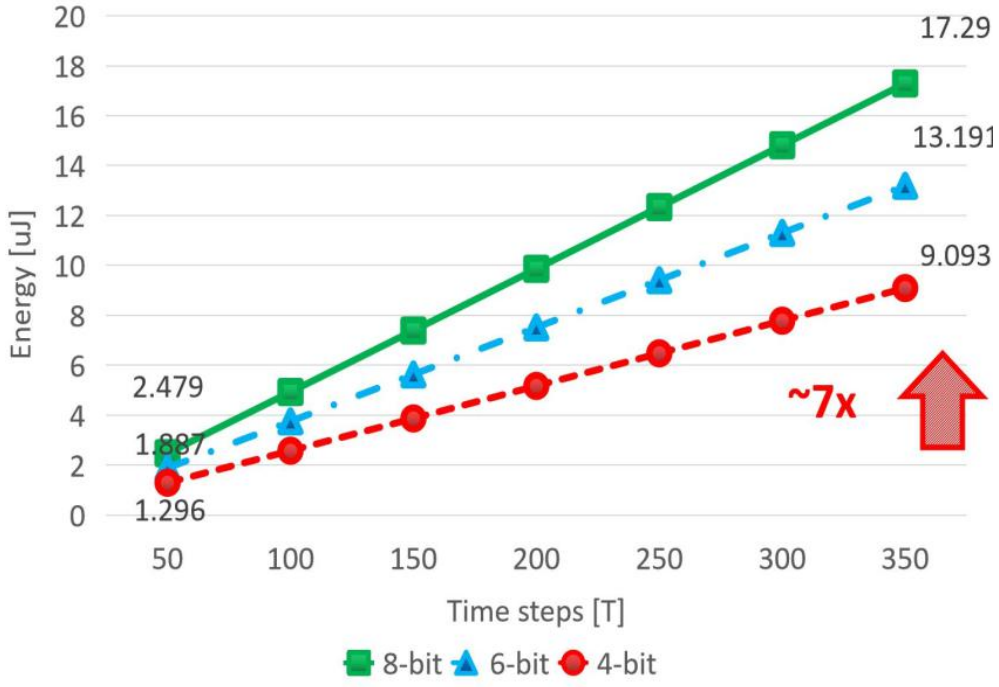
```
Power-specific unit information :
    Voltage Units = 1 V
    Capacitance Units = 1 pf
    Time Units = 1 ns
    Dynamic Power Units = 1 W
    Leakage Power Units = 1 W


                                        Int      Switch   Leak      Total
Hierarchy                               Power    Power    Power     Power    %
------------------------------------------------------------------------------
SNPC                                      3.003 7.86e-02 1.36e-04     3.082 100.0
  LIF_GEN[7].LIF0 (LIF_neuron_WEIGHT_WIDTH8_OUTPUT_REG0_37)
                                        9.73e-03 5.55e-03 3.97e-06  1.53e-02   0.5
  LIF_GEN[0].LIF0 (LIF_neuron_WEIGHT_WIDTH8_OUTPUT_REG0)
                                        1.16e-02 4.87e-03 3.92e-06  1.65e-02   0.5
  XBAR0 (xbar_LAYER_INDX0_WEIGHT_WIDTH8_SPK_ARRAY_WIDTH256_NEURAL_ARRAY_WIDTH10_ST
                                          2.896 2.66e-02 9.59e-05     2.922  94.8
  LIF_GEN[3].LIF0 (LIF_neuron_WEIGHT_WIDTH8_OUTPUT_REG0_41)
                                        1.06e-02 5.61e-03 3.95e-06  1.62e-02   0.5
  LIF_GEN[6].LIF0 (LIF_neuron_WEIGHT_WIDTH8_OUTPUT_REG0_38)
                                        9.62e-03 5.28e-03 3.94e-06  1.49e-02   0.5
                                          LIF_GEN[2].LIF0 (LIF_neuron_WEIGHT_WIDTH8_
                                        1.11e-02 4.85e-03 3.93e-06  1.59e-02   0.5
  LIF_GEN[1].LIF0 (LIF_neuron_WEIGHT_WIDTH8_OUTPUT_REG0_43)
                                        1.07e-02 5.56e-03 3.93e-06  1.62e-02   0.5
  LIF_GEN[9].LIF0 (LIF_neuron_WEIGHT_WIDTH8_OUTPUT_REG0_35)
                                        1.01e-02 4.29e-03 3.85e-06  1.44e-02   0.5
  LIF_GEN[5].LIF0 (LIF_neuron_WEIGHT_WIDTH8_OUTPUT_REG0_39)
                                        1.07e-02 5.49e-03 3.92e-06  1.62e-02   0.5
  LIF_GEN[8].LIF0 (LIF_neuron_WEIGHT_WIDTH8_OUTPUT_REG0_36)
                                        1.14e-02 4.85e-03 3.92e-06  1.63e-02   0.5
  CNTL0 (SNPC_cntrl)                    2.05e-03 3.06e-05 5.47e-07  2.08e-03   0.1
  LIF_GEN[4].LIF0 (LIF_neuron_WEIGHT_WIDTH8_OUTPUT_REG0_40)
                                        1.02e-02 5.66e-03 3.94e-06  1.58e-02   0.5
1
```

Power at 350 TS

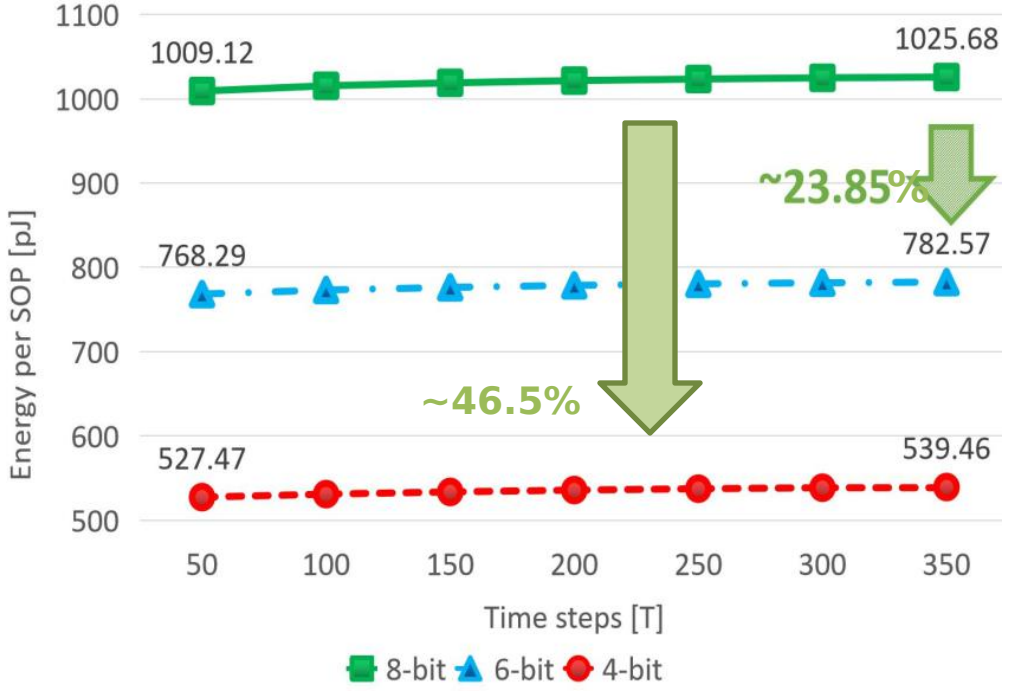
```
Power-specific unit information :
    Voltage Units = 1 V
    Capacitance Units = 1 pf
    Time Units = 1 ns
    Dynamic Power Units = 1 W
    Leakage Power Units = 1 W


                                        Int      Switch   Leak      Total
Hierarchy                               Power    Power    Power     Power    %
------------------------------------------------------------------------------
SNPC                                      2.988 7.27e-02 1.36e-04     3.061 100.0
  LIF_GEN[7].LIF0 (LIF_neuron_WEIGHT_WIDTH8_OUTPUT_REG0_37)
                                        8.97e-03 4.65e-03 3.97e-06  1.36e-02   0.4
  LIF_GEN[0].LIF0 (LIF_neuron_WEIGHT_WIDTH8_OUTPUT_REG0)
                                        9.38e-03 4.83e-03 3.95e-06  1.42e-02   0.5
  XBAR0 (xbar_LAYER_INDX0_WEIGHT_WIDTH8_SPK_ARRAY_WIDTH256_NEURAL_ARRAY_WIDTH10_ST
                                          2.896 2.64e-02 9.59e-05     2.922  95.5
  LIF_GEN[3].LIF0 (LIF_neuron_WEIGHT_WIDTH8_OUTPUT_REG0_41)
                                        8.82e-03 4.68e-03 3.97e-06  1.35e-02   0.4
  LIF_GEN[6].LIF0 (LIF_neuron_WEIGHT_WIDTH8_OUTPUT_REG0_38)
                                        9.20e-03 4.63e-03 3.97e-06  1.38e-02   0.5
  LIF_GEN[2].LIF0 (LIF_neuron_WEIGHT_WIDTH8_OUTPUT_REG0_42)
                                        8.56e-03 4.61e-03 3.95e-06  1.32e-02   0.4
  LIF_GEN[1].LIF0 (LIF_neuron_WEIGHT_WIDTH8_OUTPUT_REG0_43)
                                        8.88e-03 4.78e-03 3.97e-06  1.37e-02   0.4
  LIF_GEN[9].LIF0 (LIF_neuron_WEIGHT_WIDTH8_OUTPUT_REG0_35)
                                        1.00e-02 4.27e-03 3.85e-06  1.43e-02   0.5
  LIF_GEN[5].LIF0 (LIF_neuron_WEIGHT_WIDTH8_OUTPUT_REG0_39)
                                        8.95e-03 4.56e-03 3.95e-06  1.35e-02   0.4
  LIF_GEN[8].LIF0 (LIF_neuron_WEIGHT_WIDTH8_OUTPUT_REG0_36)
                                        8.81e-03 4.67e-03 3.95e-06  1.35e-02   0.4
  CNTL0 (SNPC_cntrl)                    2.05e-03 3.03e-05 5.47e-07  2.08e-03   0.1
  LIF_GEN[4].LIF0 (LIF_neuron_WEIGHT_WIDTH8_OUTPUT_REG0_40)
                                        8.97e-03 4.62e-03 3.97e-06  1.36e-02   0.4
1
```

Power at 50 TS

Results (2)



Energy Per Time Step



Energy Per SOP

Schedule

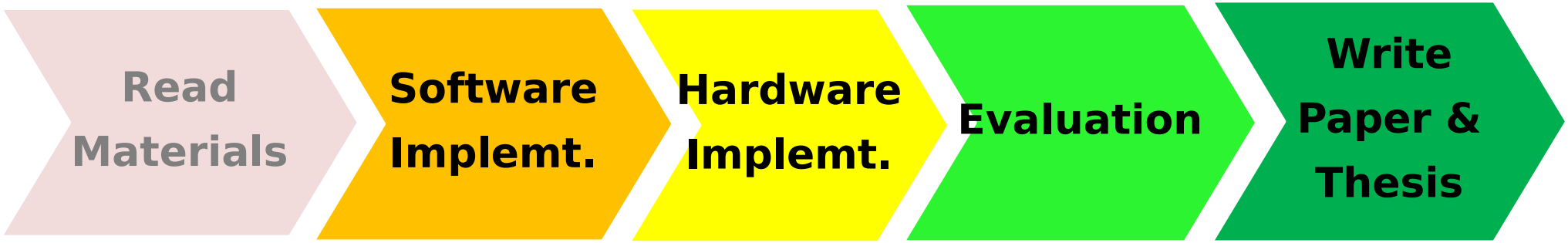
- Master's Course Schedule

1/23 - 5/23

- Build SW model as a golden reference for HW

12/23 - 3/24

- Evaluation power consumption & accuracy



10/22 - 1/23

- Get familiar with SNN

5/23 - 12/23

- Build HW model
- Optimize HW model

3/24 - 9/24

- Submit papers
- Complete thesis

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Thank you

for your attention.