LIF Neuron

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Content

- Research Introduction
- Overall system/architecture
- Research progress
  - Done
  - Doing
  - Todo
- Schedule

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Research introduction

- The theme of my research hasn't decided yet.
- It will be "LIF neuron" or "clock gating".
- I have been implementing LIF neuron.

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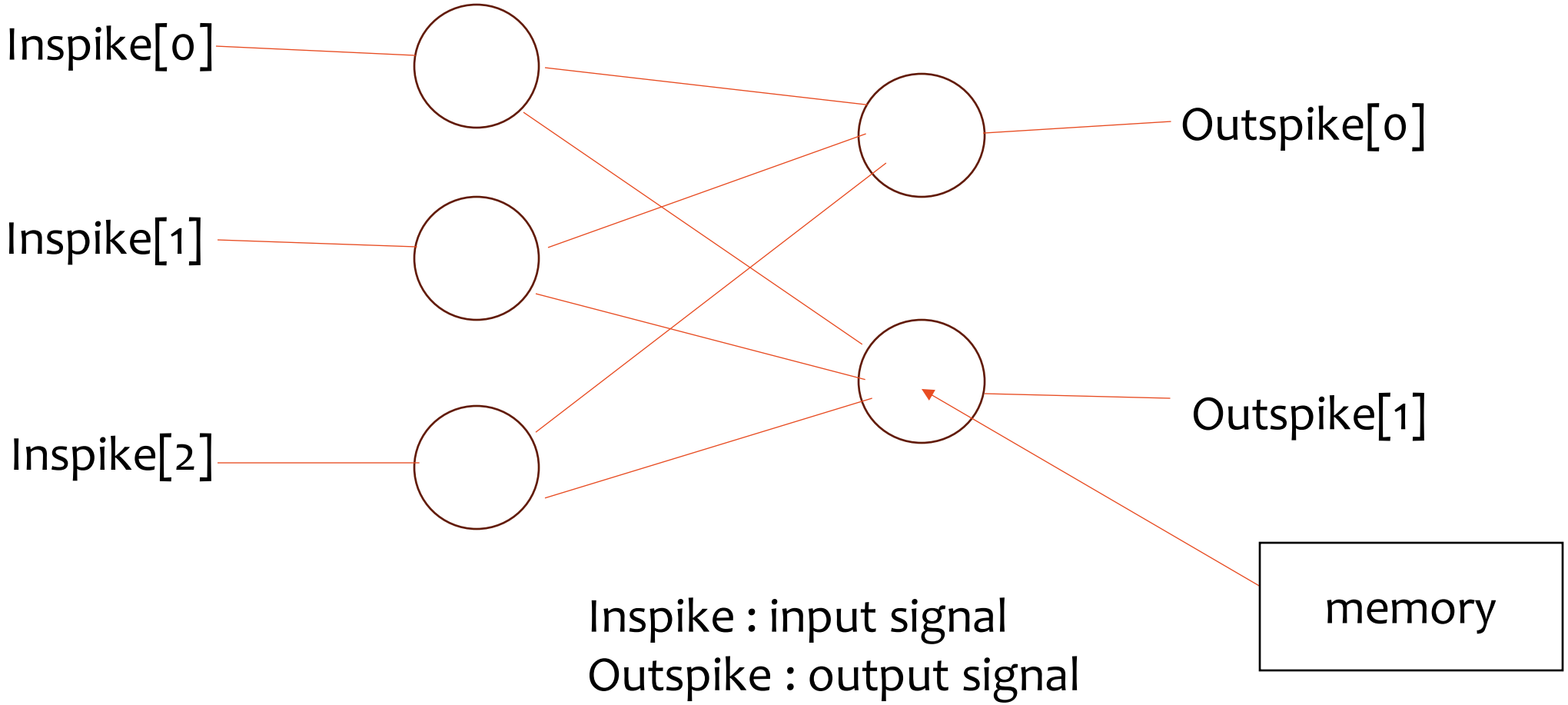
Overall system (1)



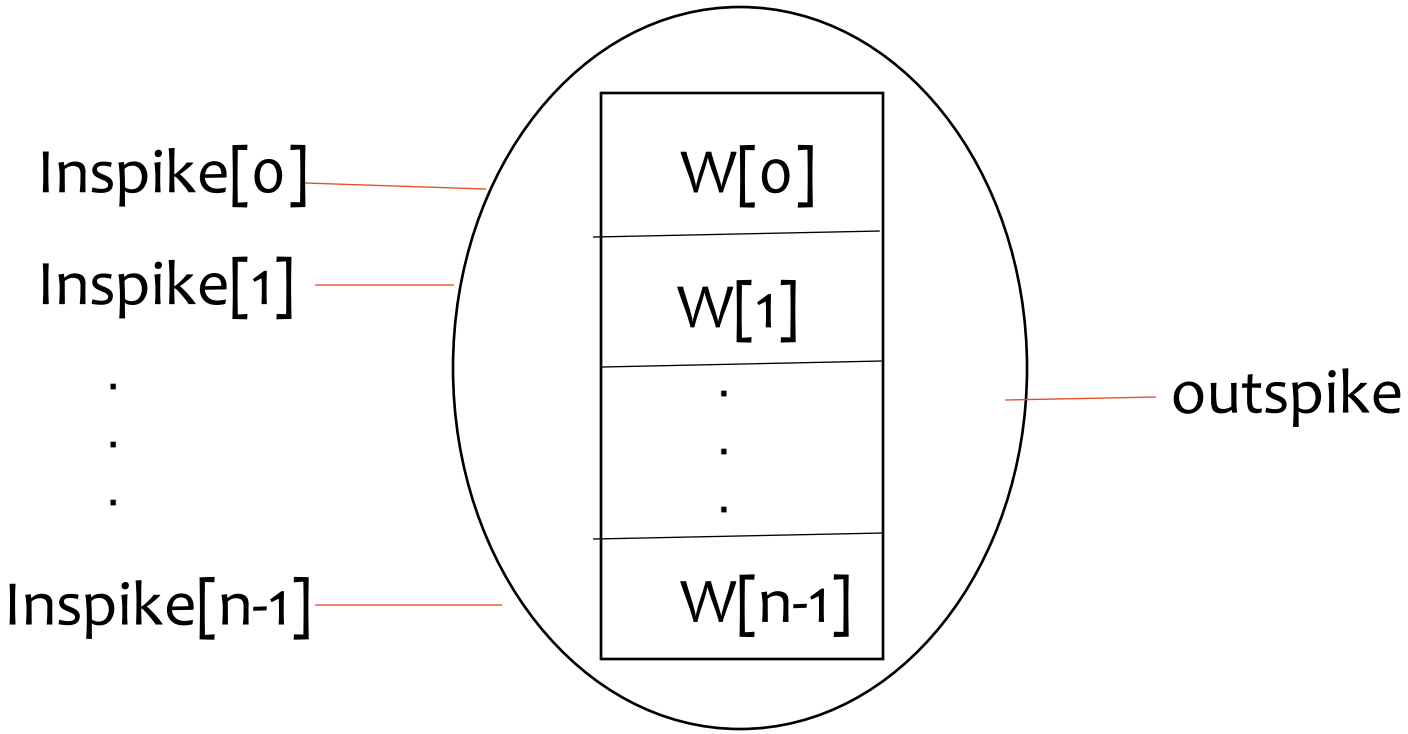
Inspike : input signal
Outspike : output signal

Overall system (2)

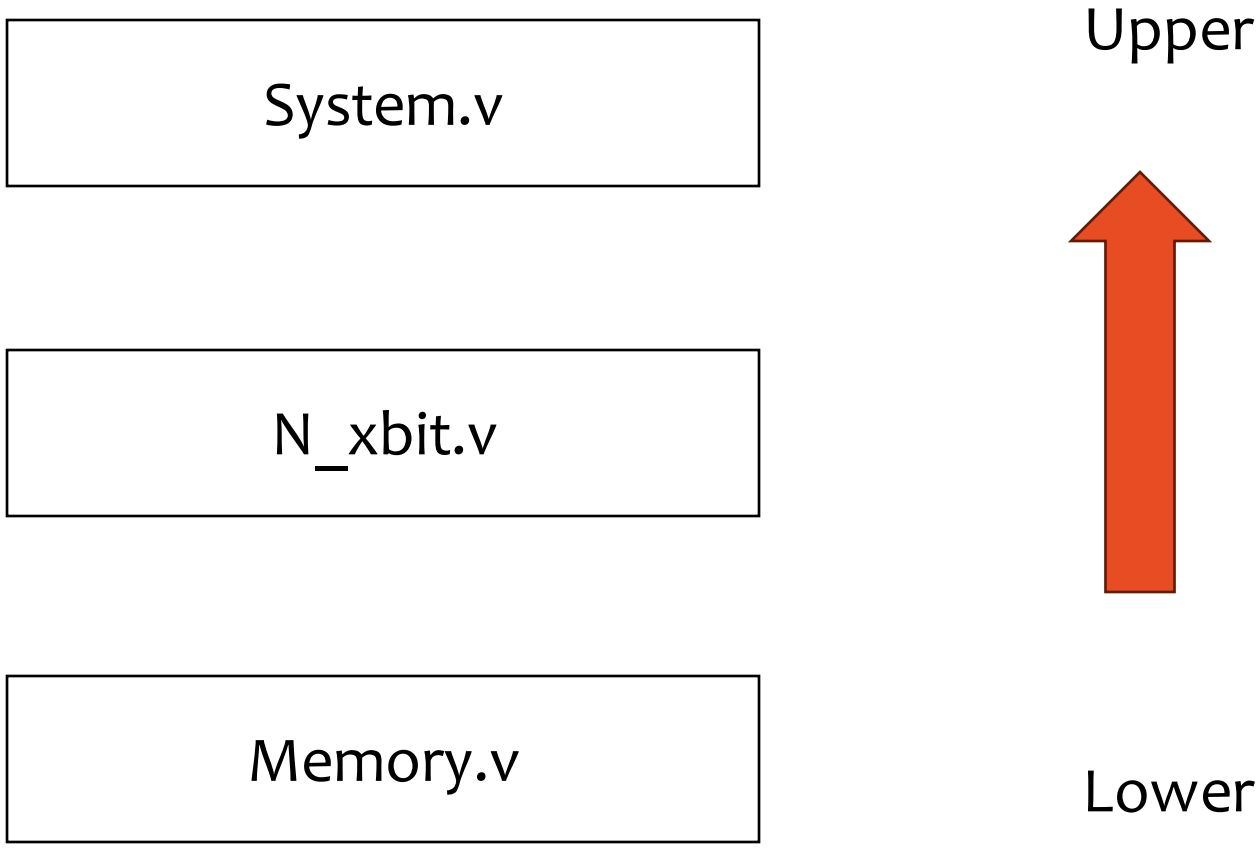
```
V = 0;
for (i = 0 ; i < n ; i++)
    V = V + inspike[i] * w[i] ;

if (V >=  Vth)
    outspike = 1 ;
else
    outspike = 0;
```

n : the width of inspike
Vth : threshold voltage
w : weight



Overall system (3)



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Research Progress | Completed

- Coding in verilog hdl
- RTL simulation
- Synthesis

Research Progress | On-going

- Post-synthesis simulation
- Clock gating

Research Progress | Todo

- Post-synthesis simulation with timing
- Power estimation

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Schedule

Task	Deadline
Clock gating	29 May 2025

Thank you for your attention!