Low-Power Spiking Neural Network with Clock-gating technique

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1. Summary of the Research

Background

Spiking Neural Network (SNN) is a brain-inspired model. It mimics the spiking nature of biological neurons and can reproduce neuron spiking patterns. To design it, reducing power consumption is important aspect.

My Research Goal

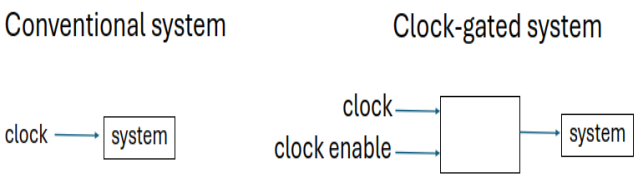
I will reduce power consumption using clock gating find a solution to reduce power consumption further.

2. Approach/Methodology

2.1 Definition of clock gating

Clock gating is a technique for reducing dynamic power. In clock-gated system, there are a clock enable signal and a clock gating cell. If clock enable signal is off, no computation is done.

2.2 Overview system



2.3 Main steps

① Coding
② Simulation
③ Synthesis
④ Post-synthesis simulation
⑤ Power Consumption

3. Current Results and Status

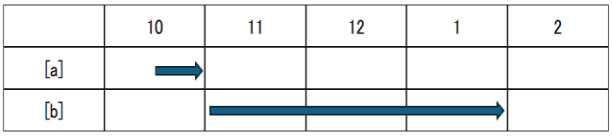
I did experiment on clock gating with 3 × 2 network. From no on, I apply clock gating to MNIST dataset with FPGA.

3.1 Experiments results

Dynamic power reduced by 30%. Static power was almost unchanged. In total, power consumption decreased by 25%.

	Dynamic Power	Static Power	Total Power
Conventional System	2.08e-04 W	4.28e-05 W	2.51e-04 W
Clock-gated System	1.46e-04 W	4.29e-05 W	1.89e-04 W

4. Remaining Tasks and Schedule



[a] FPGA Demonstaration of SNN
[b] Writing thesis

References

[1] Prithwineel Paul, Petr Sosik, Lucie Ciencialova, "A survey on learning models of spiking neural membrane systems and spiking neural networks" (2024)

[3] Nandita Srinivasana, Navamitha.S.Prakasha, Shalakha.Da, Sivaranjani.Da, Swetha Sri Lakshmi.Ga, B.Bala Tripura Sundari, "Power Reduction by Clock Gating Technique" (2015)