Low-Power Spiking Neural Network with Clock-gating technique

S1290033

Rui Shiota

Content

- Research Introduction
- FPGA Demonstration of SNN
- Simulation of RTL code for SNN
- Research progress
  - Done
  - Todo
- Schedule

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Research introduction

- My research is about clock gating in LIF neuron.
- My goal is to reduce power consumption.
- Systems can have a great effect on low power consumption.

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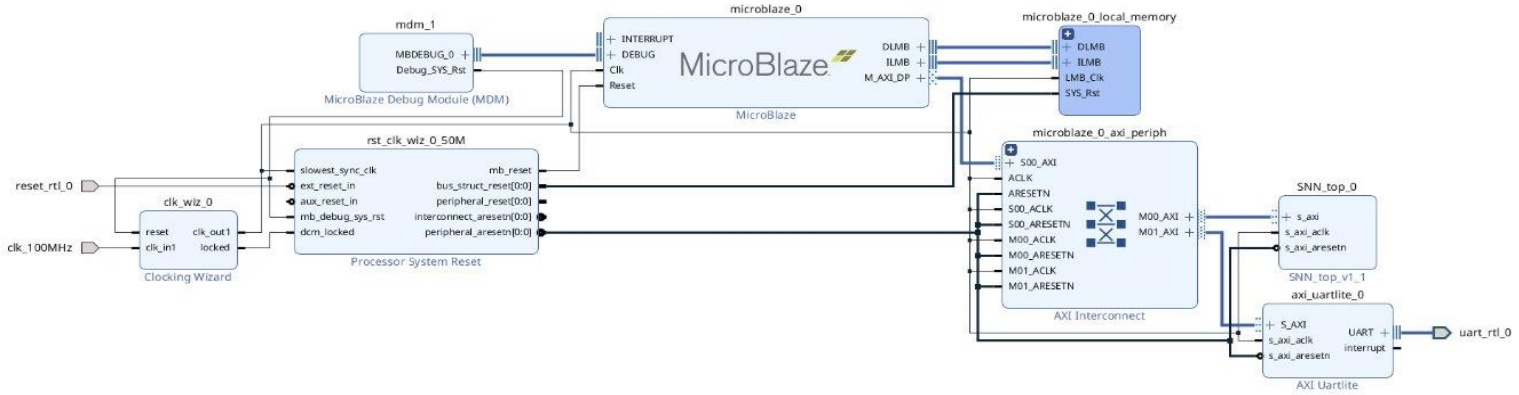
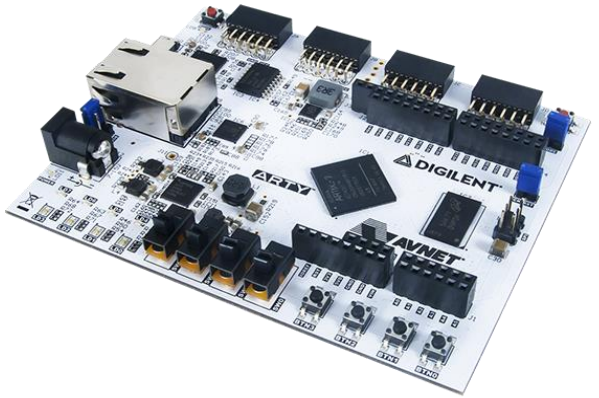
FPGA Demonstration of SNN (1)





Arty A7

- Baud Rate: 115200
- Clock Frequency: 50MHz
- Instruction Cache: 32kB
- Data Cache: 32kB
- System RAM: 128kB
- SNN IP Address: (`0x44Aa0_0000` - `0x44a0_FFFF`)
- UART Address: (`0x4060_0000` - `0x4060_FFFF`)
- Local Memory Address: (`0x0000_0000` - `0x0001_FFFF`)

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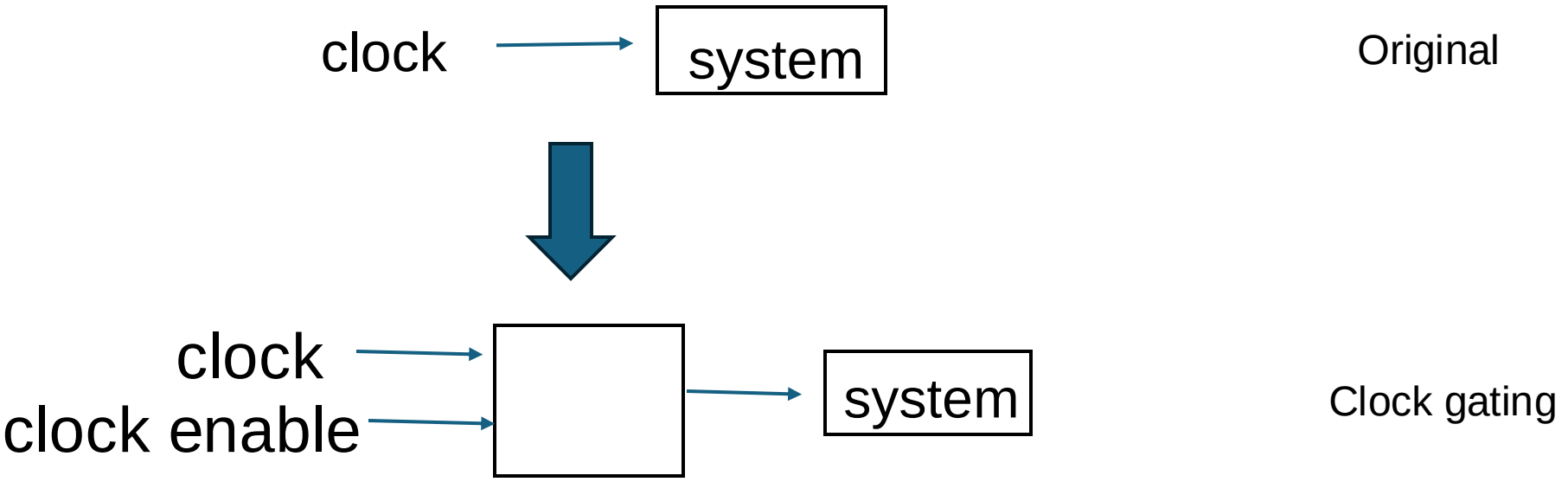
Simulation of RTL code for SNN (1)

1. Follow tutorial (simulation)
2. Apply clock gating technique
3. Estimate power consumption
4. Compare result of power consumption between original and clock-gated SNN

Simulation of RTL code for SNN (2)

Clock gating: technique to reduce dynamic power



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Research Progress | Done

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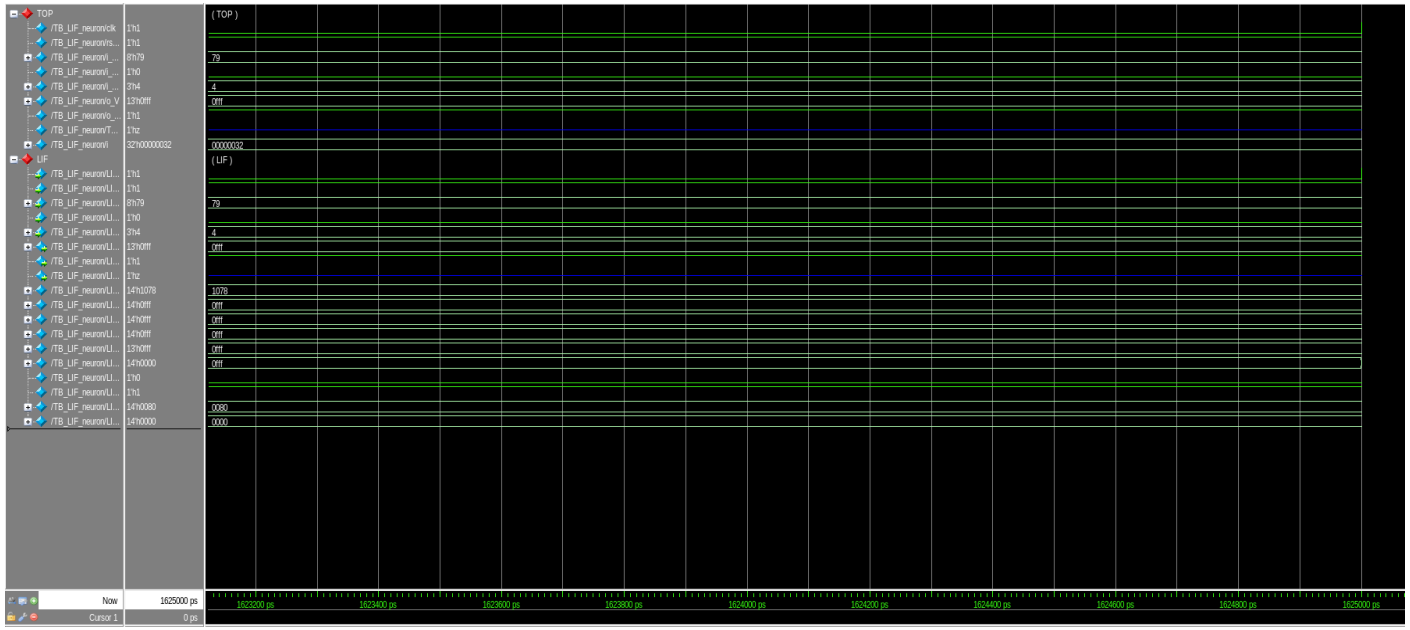
- Simulation of RTL code for SNN



Research Progress | Todo

- Application of clock gating to RTL code for SNN

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Schedule

Task	Deadline
Meeting	November 17

Thank you for your attention!