

Designing Low-Power Spiking Neural Network

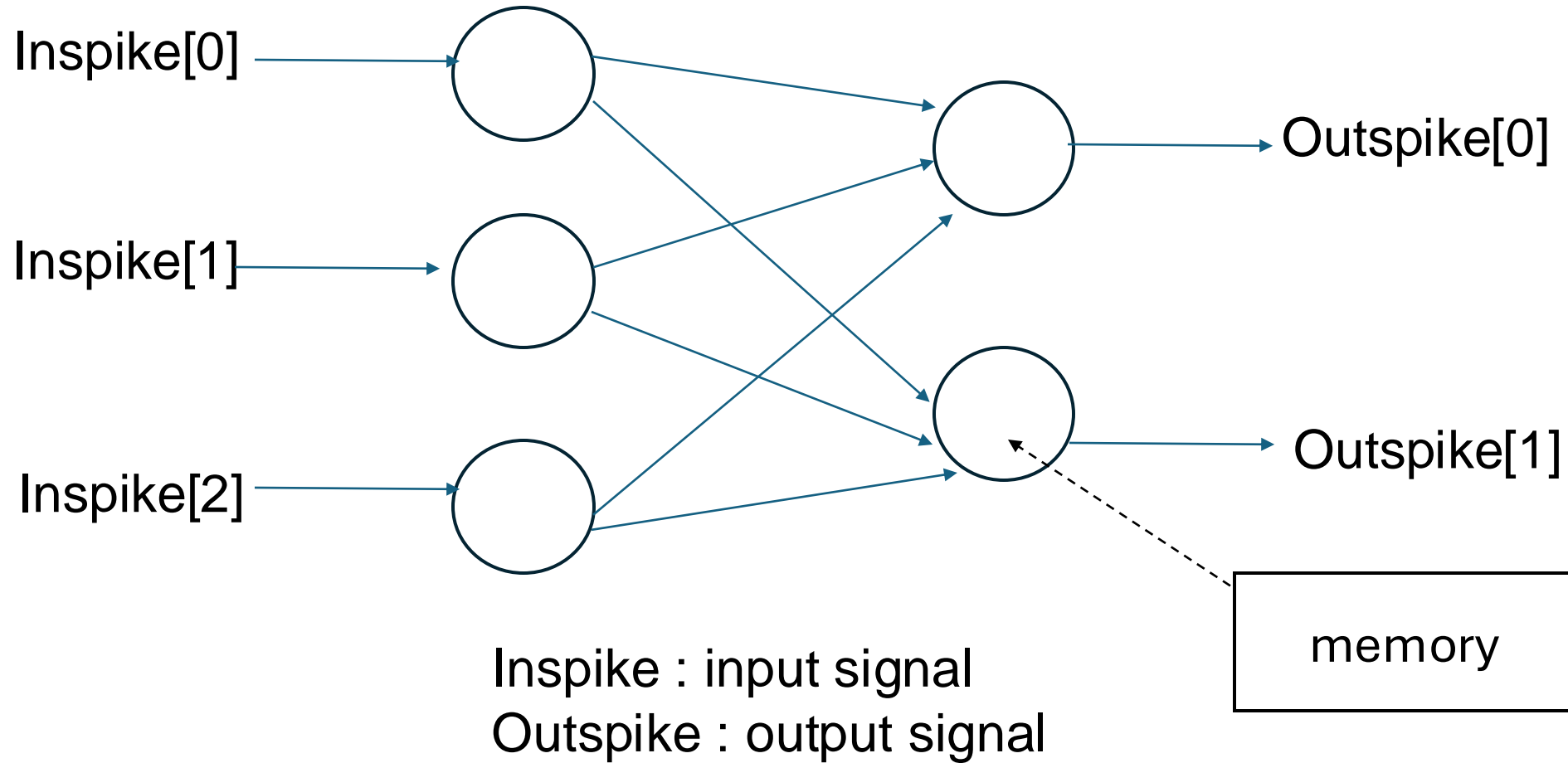
S1290033

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Content

- LIF neuron
- Clock gaitng
- Master's research

LIF neuron (1)



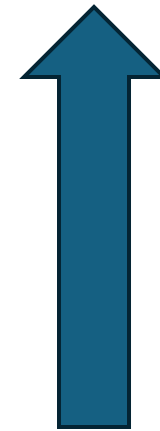
LIF neuron (2)

system.v

n_xbit.v

memory.v

Upper



Lower

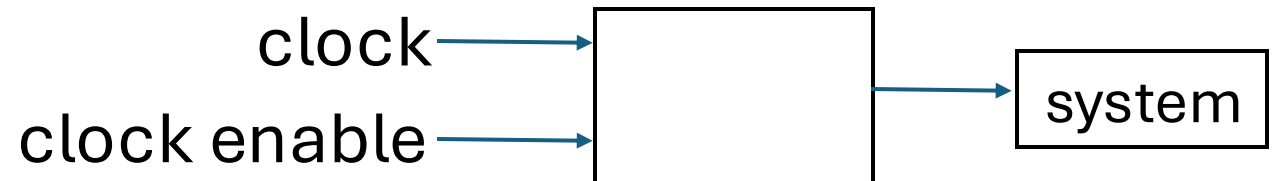
Clock gating (1)

- Clock gating: technique for reducing dynamic power

Conventional system



Clock-gated system



Clock gating (2)

The result of power consumption of n_xbit

	Dynamic Power	Static Power	Total Power
Conventional n_xbit	4.71e-05 W	1.01e-05 W	6.48e-05 W
Clock-gated n_xbit	3.98e-05 W	1.01e-05 W	5.00e-05 W

- Dynamic Power: 15% ↓
- Static power: Unchanged
- Total power: 30 % ↓

Clock gating (3)

The result of power consumption of System

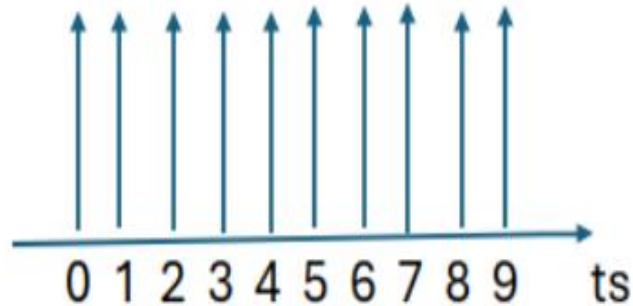
	Dynamic Power	Static Power	Total Power
Conventional System	2.07e-04 W	4.14e-05 W	2.49e-04 W
Clock-gated System	1.42e-04 W	4.01e-05 W	1.84e-04 W

- Dynamic Power: 30% ↓
- Static Power: 3% ↓
- Total Power: 26% ↓

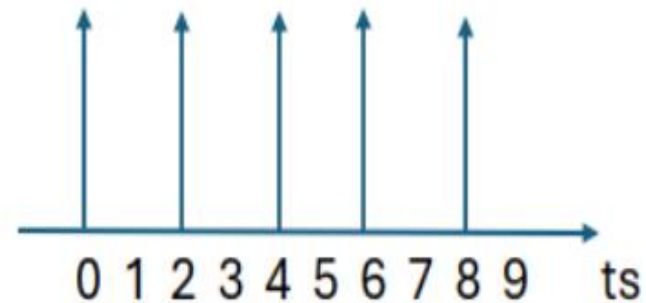
Master's research

- Focus on rate coding to apply clock gating
- Rate coding: method to represent information by the frequency of spikes

Value = $10/10 = 1$



Value = $5/10 = 0.5$



Thank you for your attention!