Low-Power Spiking Neural Network with Clock-gating technique

S1290033

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Content

- Research Introduction
- FPGA Demonstration of SNN
- Research progress
  - Done
  - Doing
  - Todo
- Schedule

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Research introduction

- My research is about clock gating in LIF neuron.
- My goal is to reduce power consumption.

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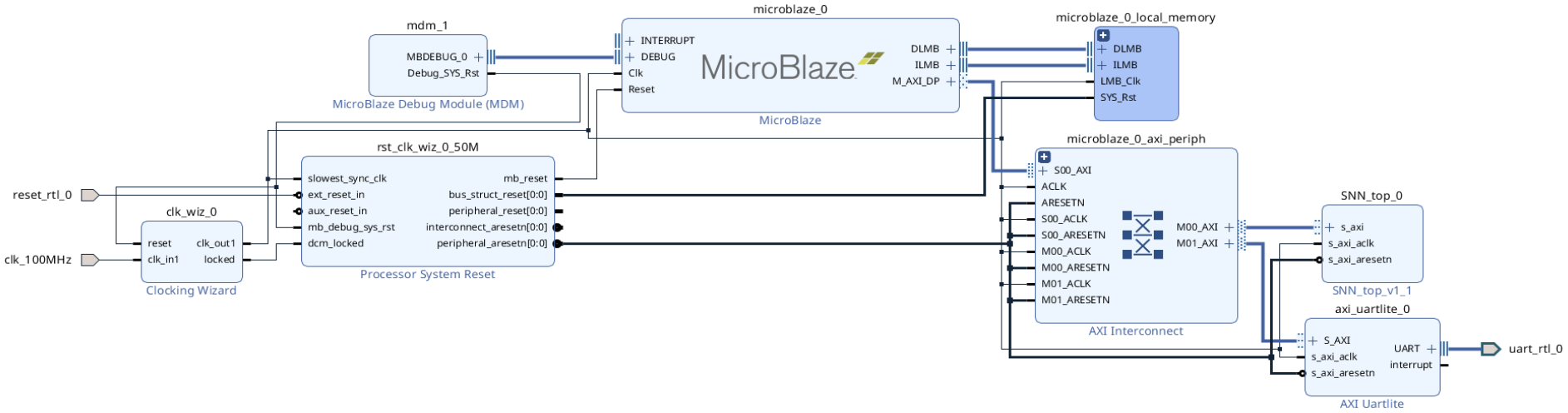
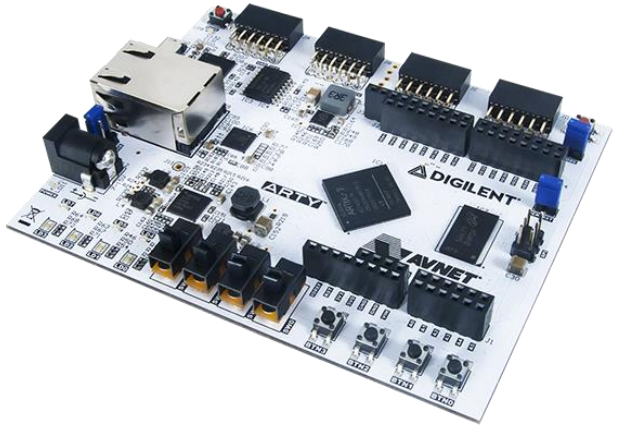
FPGA Demonstration of SNN (1)





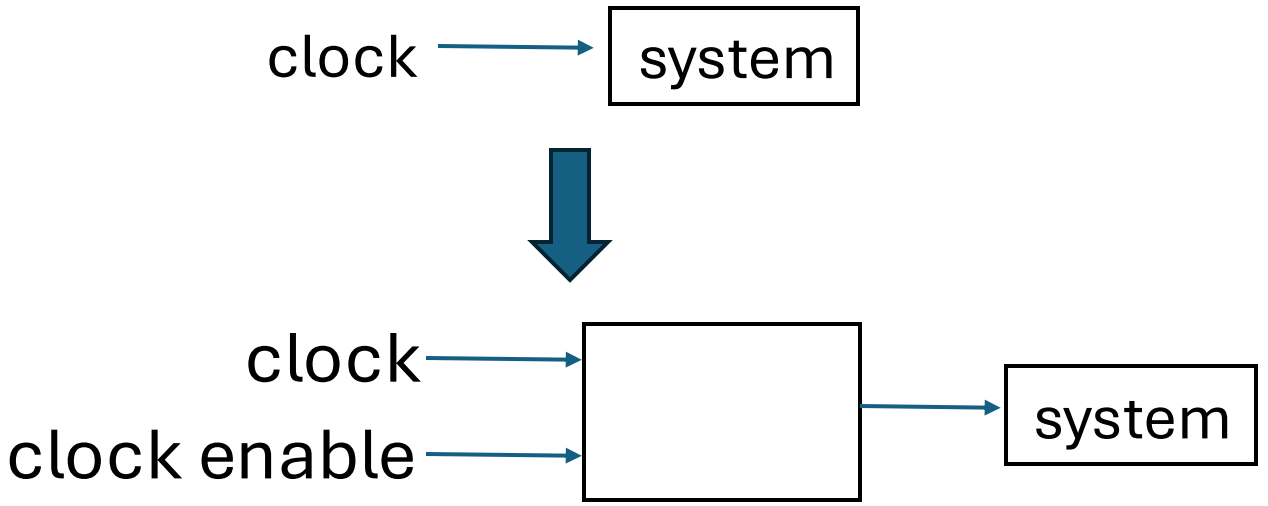
FPGA Demonstration of SNN (2)

Plan

- Study of MNIST dataset
- Development of the program with verilog HDL (Application of MNIST dataset and clock gating)

FPGA Demonstration of SNN (3)

- MNIST database: a large database of handwritten digits
- Clock gating: a technique for reducing dynamic power



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Research Progress | Done

- Tutorial of FPGA Demonstration

Research Progress | Doing

- Preparation of RPR and RPS

Research Progress | Todo

- Study of MNIST
- Development of the program

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Schedule

Task	Deadline
RPR	November 6
RPS	November 8

Thank you for your attention!