Low-Power Spiking Neural Network with Clock-gating technique

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Content

- Abstract
- Agenda
- Introduction
- Objectives
- Clock Gating Overview
- Methodology
- Research Progress
    - Done
    - Doing
    - Todo
- Schedule

Abstract

- Design SNNs with and without clock gating
- Estimate power consumtion
- Compare results

Agenda

- How much power consumption can be reduced

- How to do to apply clock gating

- When to apply clock gating

Introduction (1)

Power consumption of AI

- Uses a lot of electricity
- Dameges environment
- Generates CO_2

Spiking Neural Networks (SNNs)

- Brain-inspired model
- Mimics biological neurons
- Communicates and computes using spikes

Introduction (2)

Importance of energy efficiency

- Can become a factor of 100 to 1,000 more energy -efficient

Possible to put much more
AI into chips

High power consumption in SNN hardware implementations

- Works more efficiently than non-neuromorphic systems
- However, affects the environment

Objectives

①Reduce power consumption maintaining accuracy

- Become enegy-efficint
- Prevent from using electricity wastefully

②Reduce further by sacrificing accuracy

- Suppress of generation of CO_2
- Work with ultra-low-power

Clock Gating Overview (1)

- Clock gating: technique for reducing dynamic power

SNN
- conduct a large amount of computation
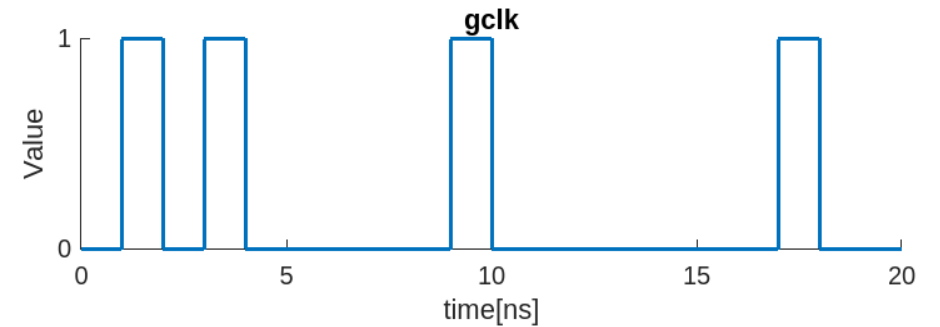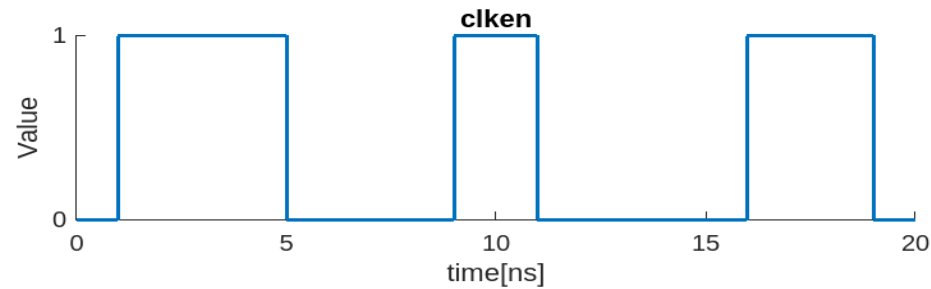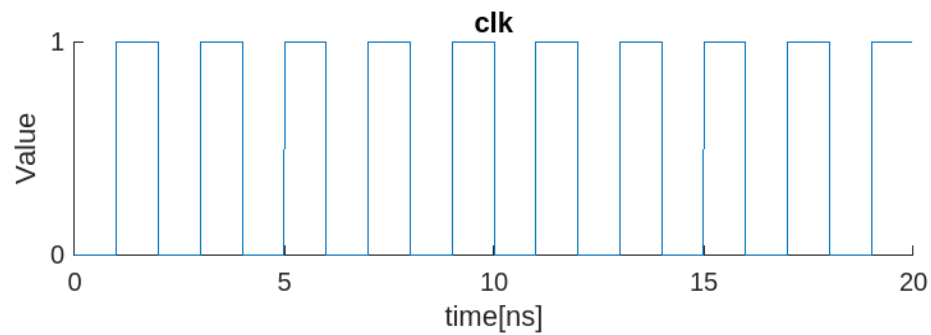- need large-scale computational resources

Application of clock gating

Reduce
- Operational expenses
- Battery life
- Environmental effect

Clock Gating Overview (2)

$$gclk = clk \land clken$$

Methodology (1)

1) Preparation codes of conventional circuit
2) Simulation
3) Synthesis
4) Post-synthesis simulation
5) Power estimation
6) Do the same tasks with clock-gated circuit

Methodology (2)

How

- Introduce clock enable signal as input
- add cell to calculate gated clock signal

Strategy

- Decide on standard to apply clock gating depending on the number of rising spikes

Modification of code for SNN

1. Follow tutorial (finished)
2. Apply clock gating technique
3. Estimate power consumption
4. Compare result of power consumption between original and clock-gated SNN

Research Progress | Done

- Simulation of RTL code for SNN
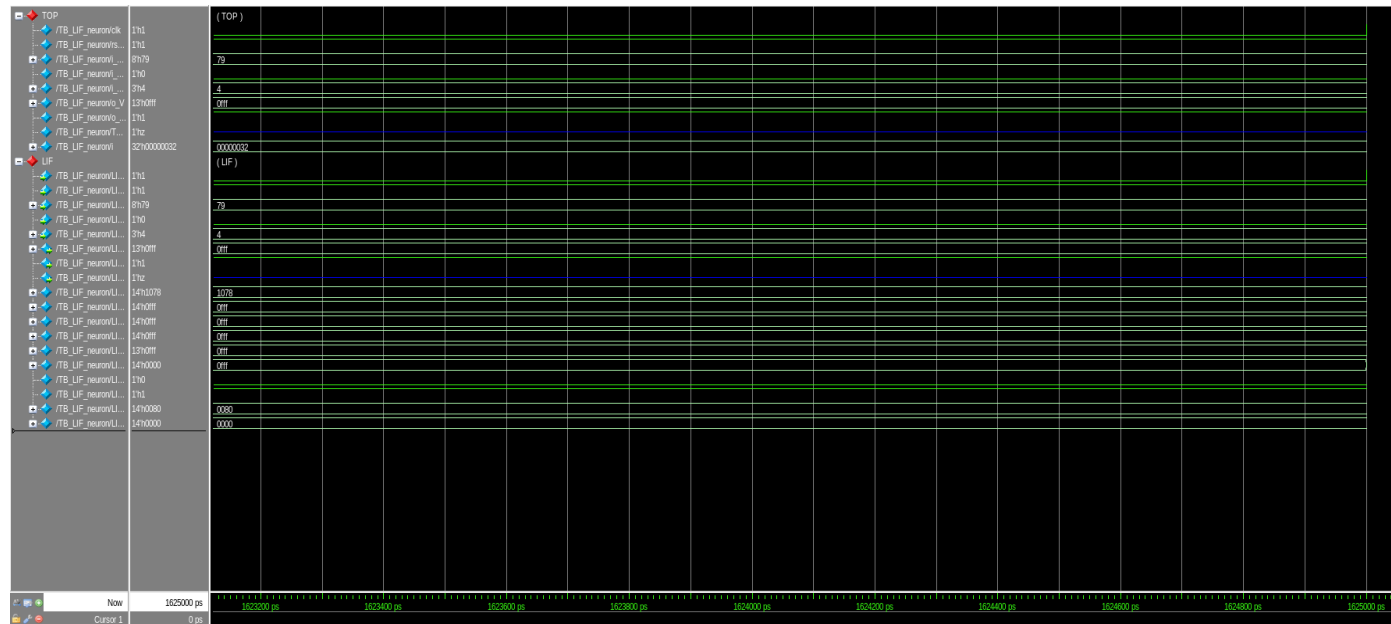
Research Progress | Doing

- Application of clock gating to RTL code for SNN
- Graduation thesis
- Revise of slide

Research Progress | Todo

- Estimate power consumption
- Compare results

Schedule

Task	Deadline
Meeting	December 9
Graduation thesis	January

Thank you for your attention!