Designing Low-Power Spiking Neural Network

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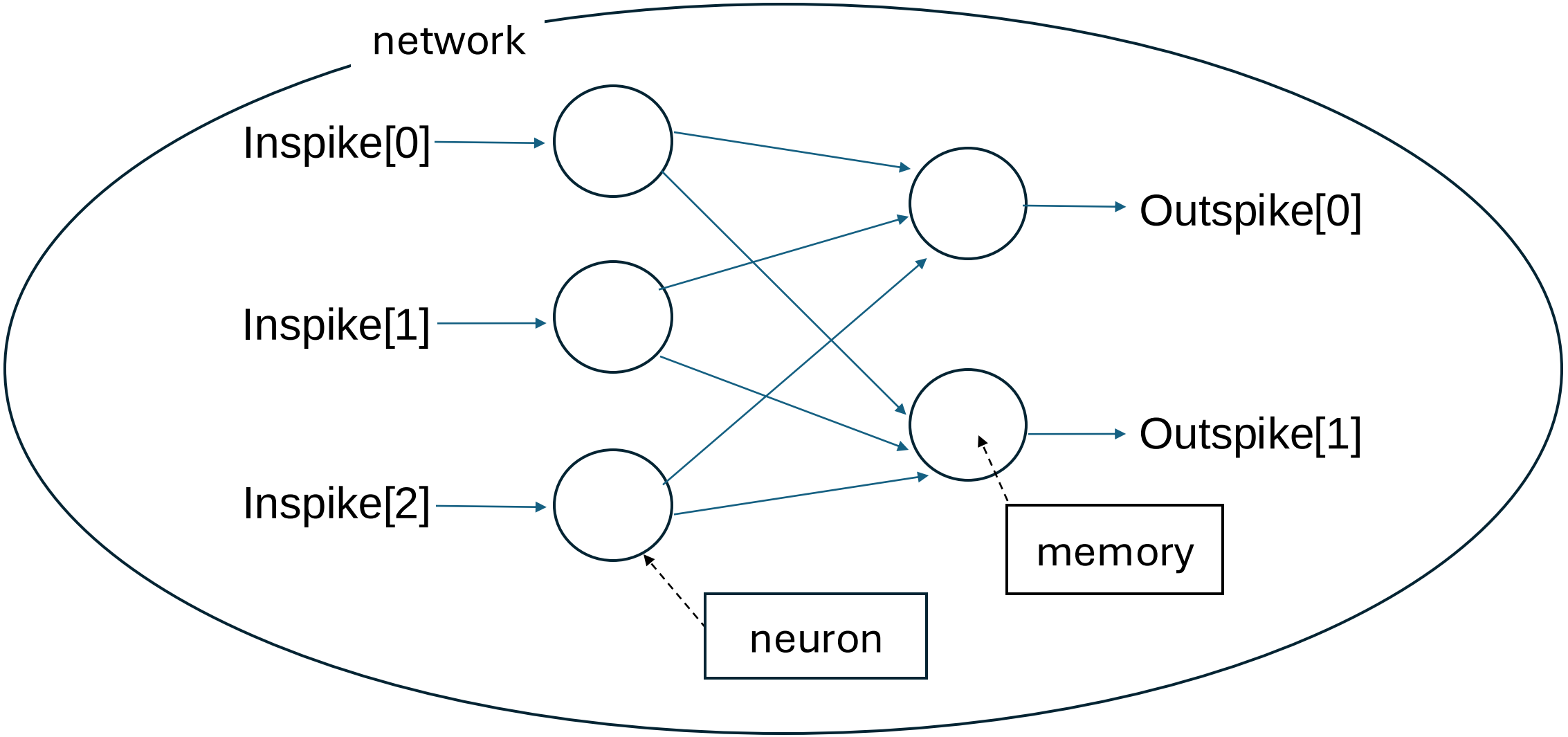
- Background / Related works
- Design of neural network
- Clock gating
- Master's research

Background / Related works

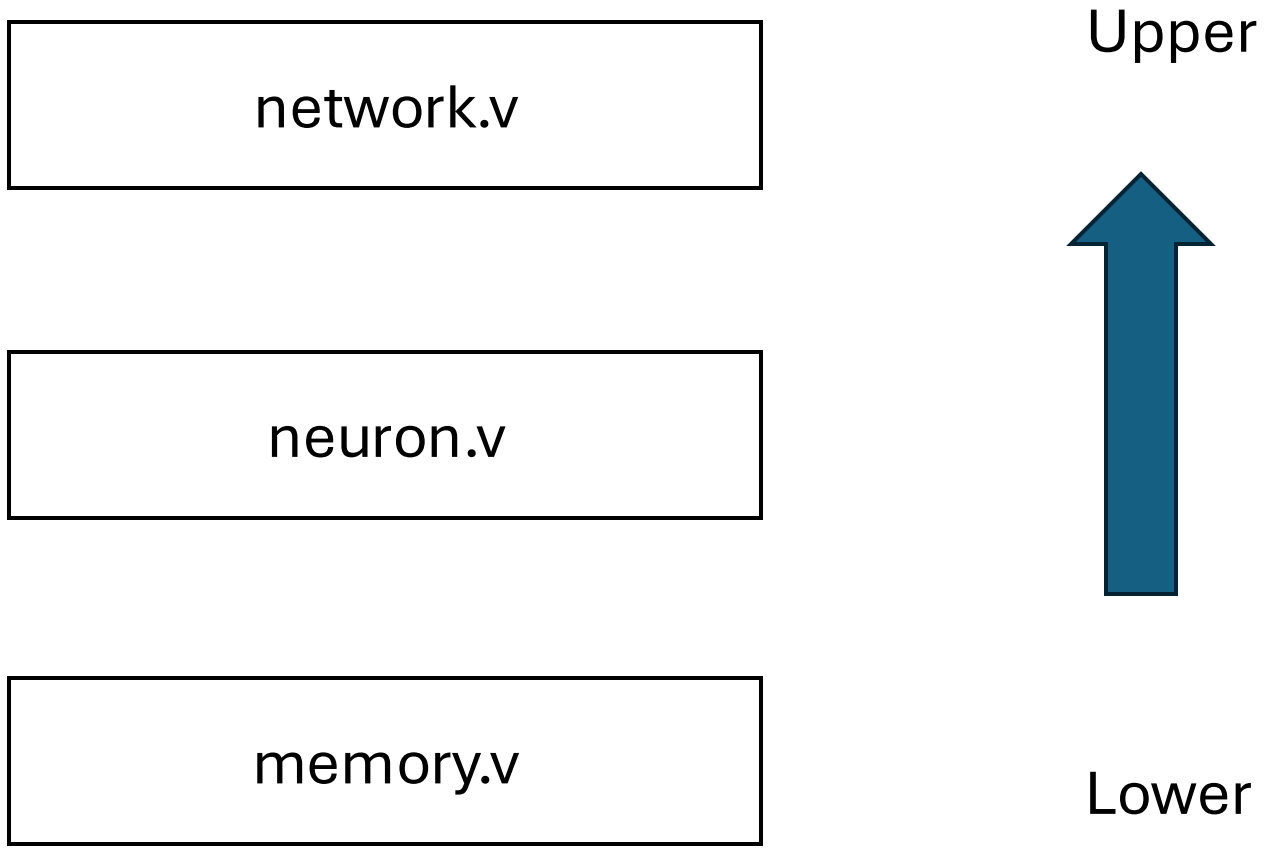
- Spiking Neural Network: brain-inspired model of neural communication and computation

- Clock gating: technique for reducing consumption

Design of neural network (1)

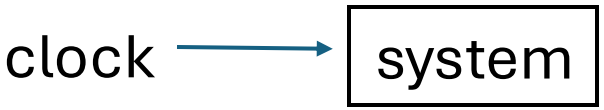


Design of neural network (2)

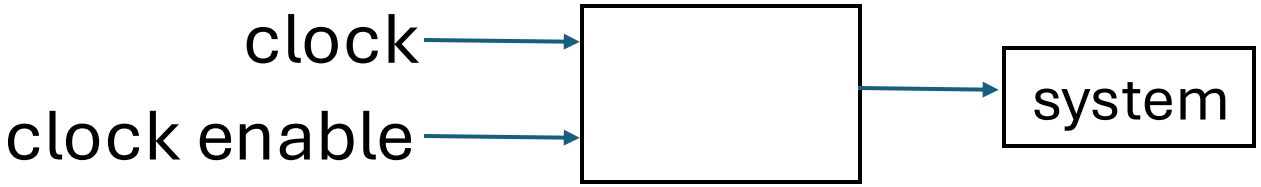


Clock gating (1)

Conventional system



Clock-gated system



- Can save dynamic power by turning off clock enable signal.
- No computation is done while clock enable signal is off.

Clock gating (2)

The result of power consumption of neuron

	Dynamic Power	Static Power	Total Power
Conventional neuron	5.30e-05 W	1.04e-05 W	6.34e-05 W
Clock-gated neuron	3.91e-05 W	1.04e-05 W	4.96-05 W

- Dynamic Power: 26% ⬇
- Static power: Unchanged
- Total power: 22 % ⬇

Clock gating (3)

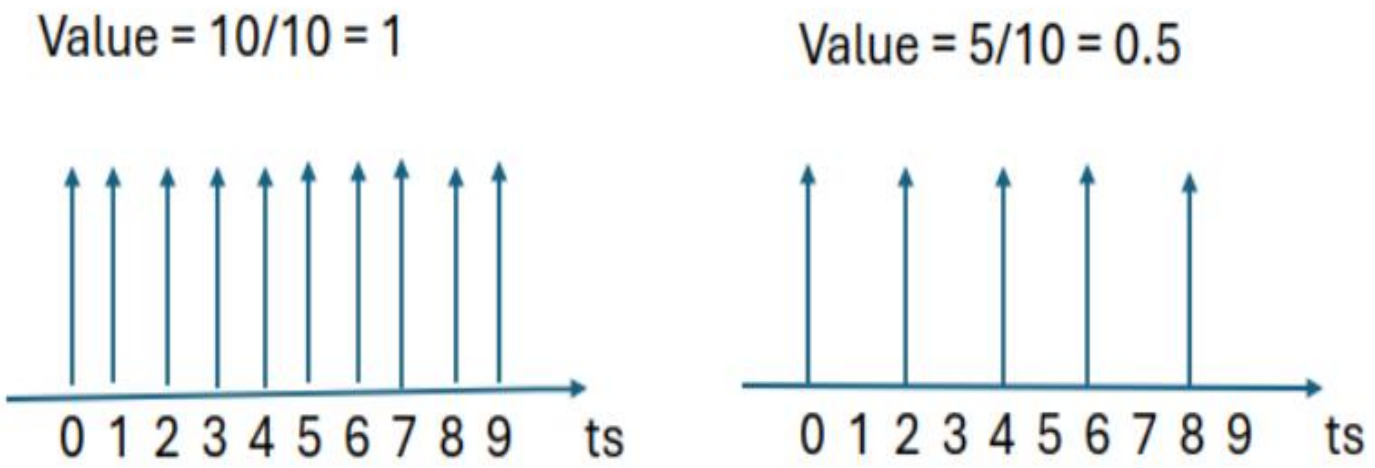
The result of power consumption of network

	Dynamic Power	Static Power	Total Power
Conventional network	2.08e-04 W	4.28e-05 W	2.51e-04 W
Clock-gated network	1.46e-04 W	4.29e-05 W	1.89e-04 W

- Dynamic Power: 30% ⬇
- Static Power: Almost unchanged
- Total Power:25% ⬇

Master's research (1)

- Focus on rate coding to apply clock gating
- Rate coding: method to represent information by the frequency of spikes



Master's research (2)

- Goal: to find a way to reduce the power consumption further

Year	M1			M2		
Month	4~7	8~11	12~3	4~7	8~11	12~3
Coding in Verilog HDL	→		→			
Simulation	→		→			
Synthesis		→		→		
Post-synthesis simulation		→		→		
Power estimation		→		→		
Consideration			→			
Writing a thesis					→	

Thank you for your attention!