Low-Power Spiking Neural Network with Clock-gating technique

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- Research Introduction
- Neuron model with clock gating
- Neuron model
- Clock gating
- Research progress
  - Done
  - Doing
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Research introduction

- My research is about clock gating in LIF neuron.
- My goal is to reduce power consumption.

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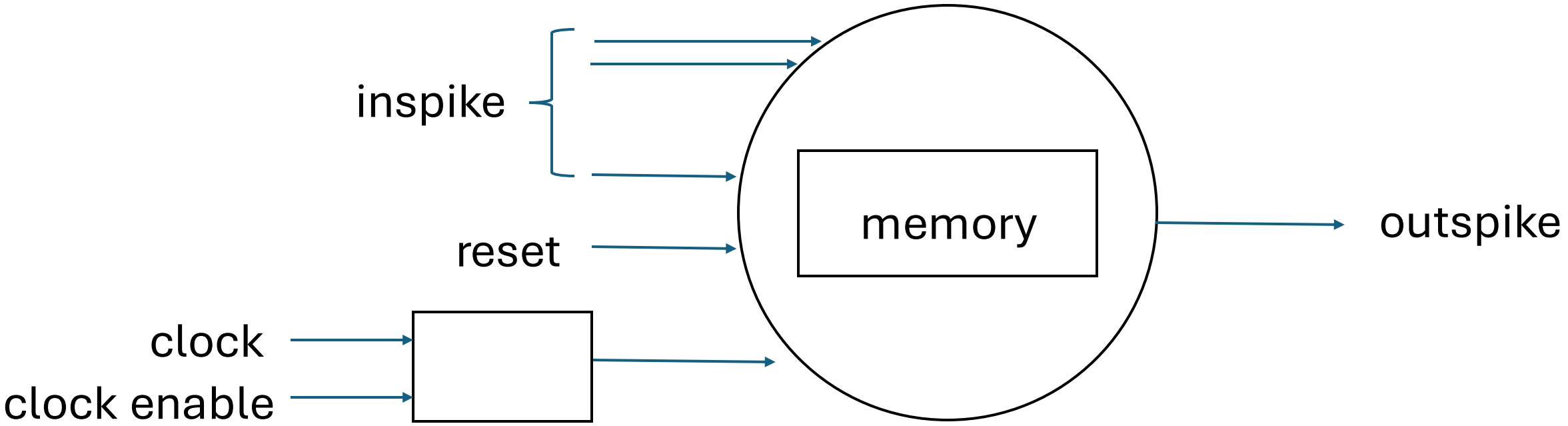
Neuron model with clock gating



Inspike : input signal
Outspike : output signal

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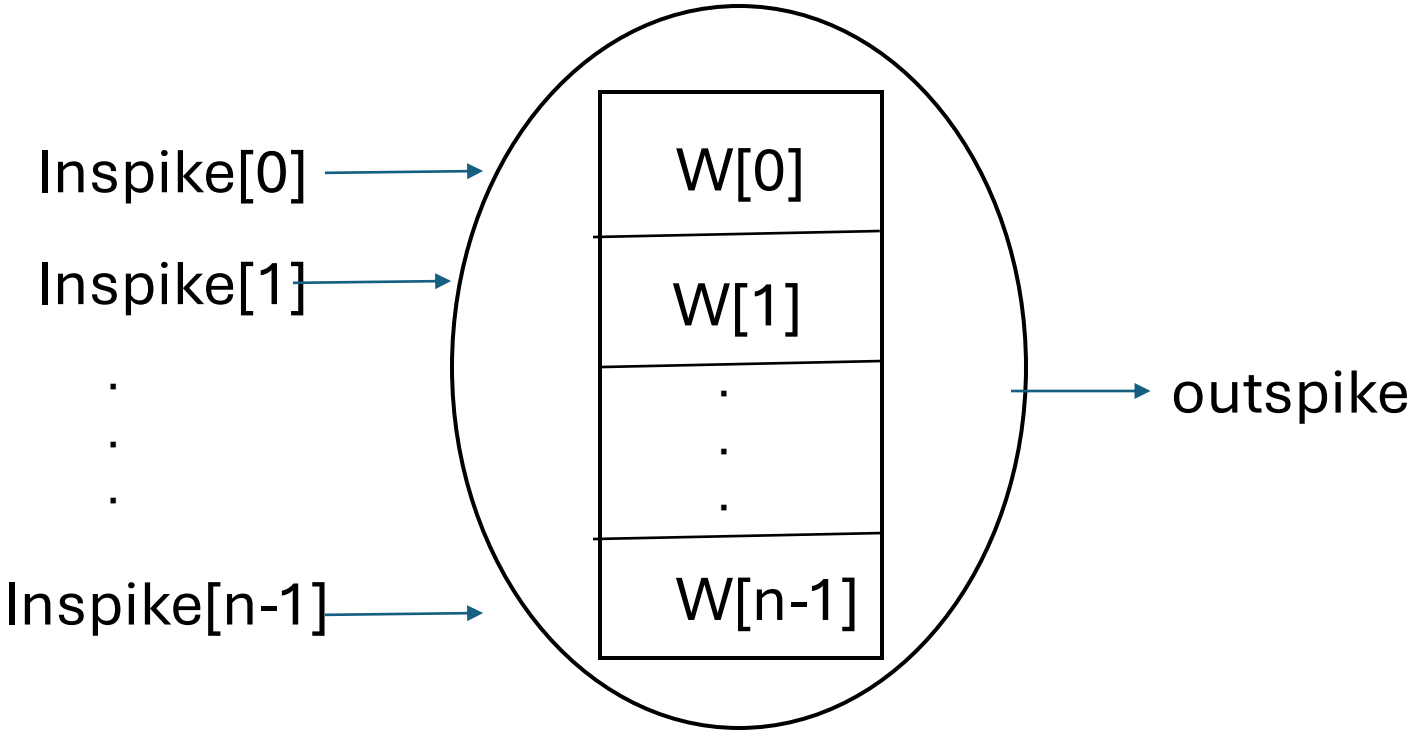
Neuron model

```
V = 0;
for (i = 0 ; i < n ; i++)
    V = V + inspike[i] * w[i] ;

if (V >=  Vth)
    outspike = 1 ;
else
    outspike = 0;
```

n : the width of inspike
Vth : threshold voltage
w : weight



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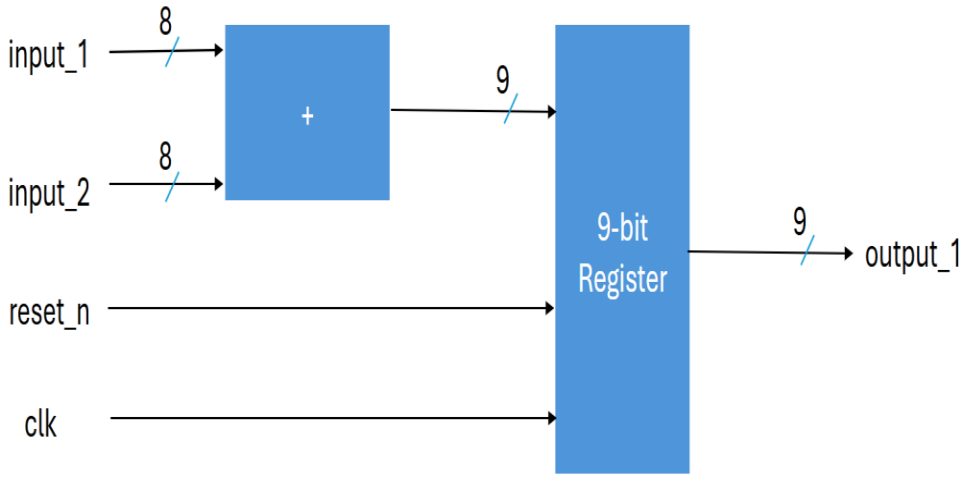
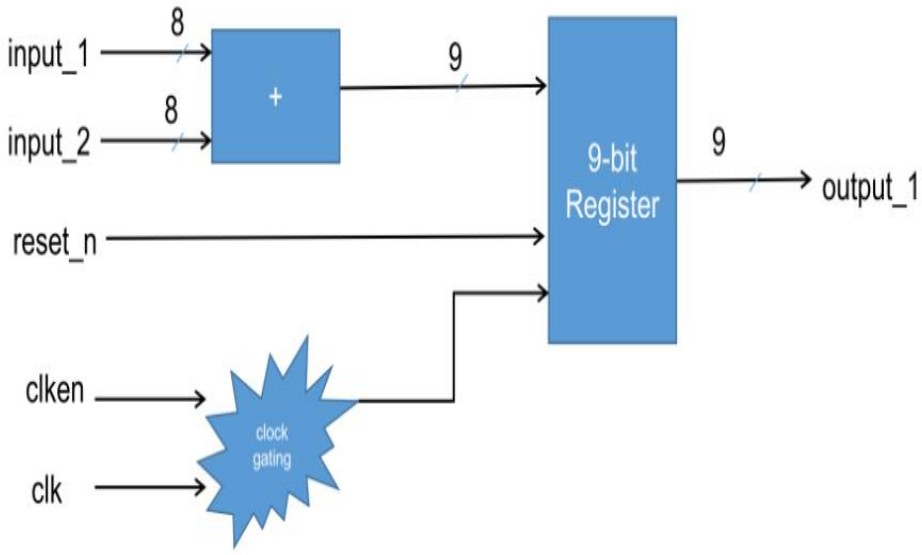
Clock gating (1)

conventional (non-clock-gated) adder



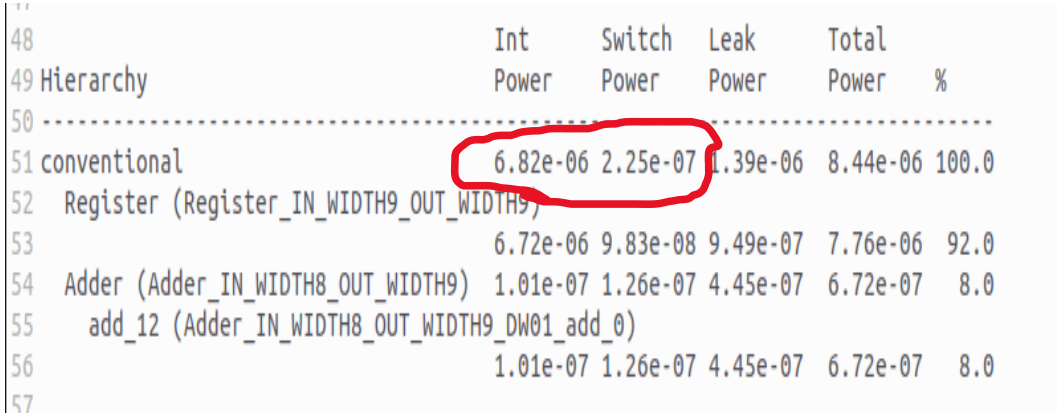
clock gated adder



Clock gating (2)

Dynamic Power = Internal Power + Switching Power

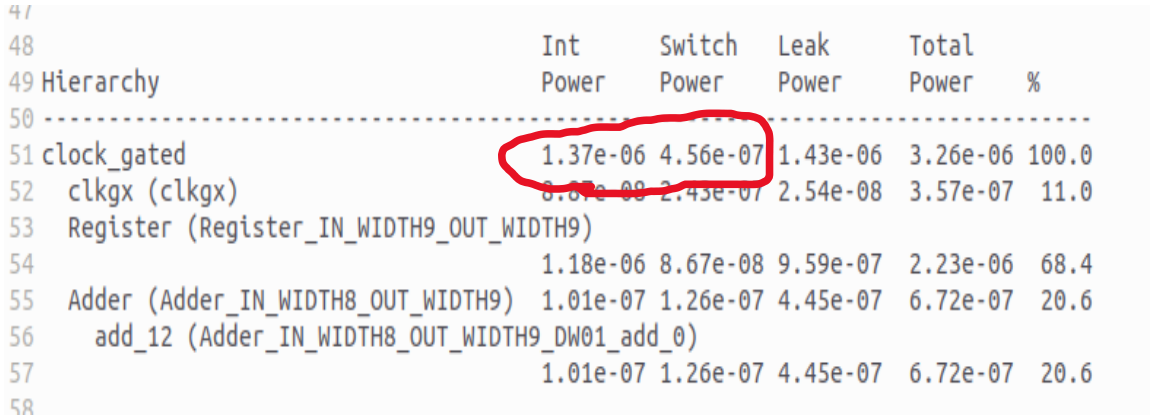
conventional (non-clock-gated) adder



Hierarchy	Int Power	Switch Power	Leak Power	Total Power	%
conventional	6.82e-06	2.25e-07	1.39e-06	8.44e-06	100.0
Register (Register_IN_WIDTH9_OUT_WIDTH9)	6.72e-06	9.83e-08	9.49e-07	7.76e-06	92.0
Adder (Adder_IN_WIDTH8_OUT_WIDTH9)	1.01e-07	1.26e-07	4.45e-07	6.72e-07	8.0
add_12 (Adder_IN_WIDTH8_OUT_WIDTH9_DW01_add_0)	1.01e-07	1.26e-07	4.45e-07	6.72e-07	8.0

Dynamic Power : 7.045e-06

clock gated adder



Hierarchy	Int Power	Switch Power	Leak Power	Total Power	%
clock_gated	1.37e-06	4.56e-07	1.43e-06	3.26e-06	100.0
clkgx (clkgx)	8.87e-08	2.43e-07	2.54e-08	3.57e-07	11.0
Register (Register_IN_WIDTH9_OUT_WIDTH9)	1.18e-06	8.67e-08	9.59e-07	2.23e-06	68.4
Adder (Adder_IN_WIDTH8_OUT_WIDTH9)	1.01e-07	1.26e-07	4.45e-07	6.72e-07	20.6
add_12 (Adder_IN_WIDTH8_OUT_WIDTH9_DW01_add_0)	1.01e-07	1.26e-07	4.45e-07	6.72e-07	20.6

Dynamic Power : 1.826e-06

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Research Progress | Done

- Coding in verilog hdl
- RTL simulation
- Synthesis
- Post-synthesis simulation
- Power estimation
- Implementing a clock-gated adder

Research Progress | Doing

- Implementing a clock-gated neuron model

Research Progress | Todo

- Implementing a clock-gated system

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Schedule

Task	Deadline
Implementing a clock-gated neuron model	18 June 2024
Implementing a clock-gated neuron system	undecided
Submission of a slide for graduate school entrance exam	24 June 2024

Thank you for your attention!