Title: TSV-OCT: A scalable online multiple TSV defects localization for 3D-ICs
Authors: Khanh N. Dang, Akram Ben Ahmed, Abderazek Ben Abdallah, and Xuan-Tu Tran
Manuscript NO: TVLSI-00334-2019

August 31, 2019

Dear Editors

We would like to thank you for your earlier letter regarding our manuscript. We greatly appreciate your comments and those of the reviewers. The comments have helped us to considerably improve our manuscript. We have revised the manuscript to meet each of the reviewers' suggestions. Point-by-point responses to these suggestions can be found on the following pages.

We also thank the reviewers for their insightful commentary, and we hope that the revised version of our paper is now acceptable for publication in the IEEE Transactions on Very Large Scale Integration Systems.

Thank you for reconsidering our manuscript.

Respectfully yours,
Khanh N. Dang

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On behalf of all authors.

Response to the reviewers

We thank the reviewers for their critical assessment of our work. In the following, we address their concerns point by point.

The styles are shown in the following table:

Content	**Style**
The reviewers' comments	blue color, roman style
The authors' answers	black color, sans serif
The manuscript's changes	highlighted

To avoid any confusion with the revised manuscript, the numbering for tables and figures that are only used for explanation purpose in this document start with the prefix "A-".

Reviewer 1

Reviewer Point P 1.1 — In the introduction section, the author raises 5 problems to solve, and one of the problems is intermittent defect of TSV. However, the author did not give specific solutions for localization and detection of intermittent defect.

Reply: We agree with the reviewer on this important point. We would like to clarify that our method can only ensure the detection and localization of intermittent faults only if they last more than the Intermittent Detection Window (IDW). We define this window as $2\times$ the Worst Case Execution Time (WCET) of TSV-OCT. For instance, with a 32-bit data, the WCET is evaluated to 16,488 cycles. If the intermittent fault lasts for more than IDWs ($2 \times 16,488 = 32,976$ cycles), a run of the proposed TSV-OCT can detect the faulty position.

When it comes to the types of faults that TSV-OCT can deal with, there are different intermittent fault sources such as voltage, frequency, temperature and stress/vibration as stated in [Ref 1] by Cristian Constantinescu from AMD: *"Extensive laboratory tests have shown that voltage, frequency, and temperature variations may activate or deactivate intermittent faults"*.

For TSVs, stress or vibration could be other sources of intermittent defects. [Ref 2] also points out the aging factor that could affect intermittent defects. Single event upsets (SEU) could also cause intermittent faults or transient faults. The fast-changing intermittent or transient faults could be corrected by the built-in ECC module in the proposed TSV-OCT

Beside SEUs, which usually last for only one or several cycles, the other sources last for hundred thousands cycles or even more. For instance, the temperature or stress related faults stay for several seconds or minutes which can be millions of cycles for a given design. This duration is always greater than the required IDW constraint; thus, allowing the proposed methodology to easily detect such faults. In DFVS (Dynamic voltage and frequency scaling), voltage and frequency could quickly change; however, it is not efficient in terms of power and reliability (timing violations) to change them too frequently.

To understand how TSV-OCT could detect intermittent faults under IDW, let us consider an intermittent open defect which creates an open resistance between two terminals of a TSV. As a textbook theory, the resistance increases together with the temperature. Figure A-1.1 illustrates the thermal activated intermittent case where the open defect cause timing violations or even electrical disconnections at high temperatures. When the temperature is lowered, the defect disappears and could not be detected. As shown in Figure A-1.1, TSV-OCT operates in parallel with the TSV data transactions. Right after the intermittent defect is activated, one run of TSV-OCT could detect and localize this defect. Therefore, it could catch the defect during the high temperature interval. This is in contrast to the *P-BIST*, as depicted in Figure A-1.1, since its periodic execution runs at the lower temperature intervals; thus, the defect is missed.

In conclusion, to ensure that the proposed TSV-OCT can localize intermittent defects, Intermittent Detection Window (IDW) must be at least $2\times$ Worst Case Execution Time (WCET).

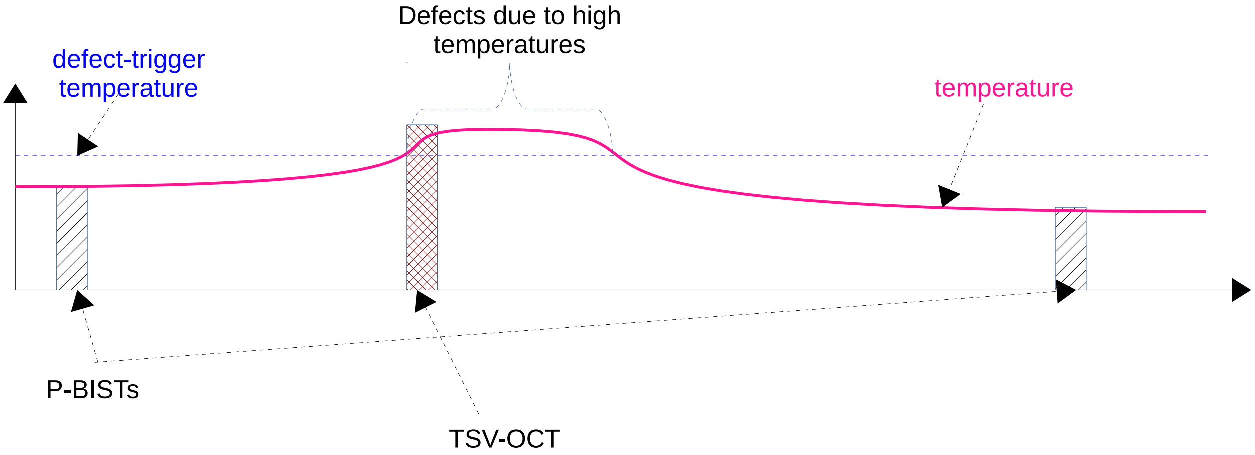


Figure A-1.1: Intermittent behavior of TSV.

To highlight the reviewer's comment, we edited the manuscript as follows:

- In line 59 left column to line 51 right column, page 6:
"Because intermittent faults occur in certain conditions and may vary among the products due to process variation, *TSV-OCT* detects TSV intermittent defects by constantly

monitoring the operation of TSVs. However, it is important to mention that the condition to successfully execute this detection is that these intermittent faults must last at least $2\times$ WCET. Such a duration ensures at least one complete run of TSV-OCT to detect the fault. Nevertheless, last changing intermittent or transient faults could be corrected by the built-in ECC in *TSV-OCT*. "

- In line 19-23, right column, page 12, we added a sub-section "Discussion" with the following text:
  "As previously mentioned, *TSV-OCT* also tackles intermittent faults. Since the WCETs of *TSV-OCT* are fixed, designers could choose a proper configuration to ensure the detection and localization of this type of faults during the Intermittent Detection Window (IDW), which is defined as $2\times$ WCET. "

[Ref 1] Constantinescu, Cristian. "Intermittent faults and effects on reliability of integrated circuits." 2008 Annual Reliability and Maintainability Symposium. IEEE, 2008.

[Ref 2] Qi, H., Ganesan, S., & Pecht, M. (2008). No-fault-found and intermittent failures in electronic products. Microelectronics Reliability, 48(5), 663–674. doi:10.1016/j.microrel.2008.02.003

Reviewer Point P 1.2 — From the title and the introduction section of the manuscript, one advantage is the scalability as the author said. However, it has not been strongly reflected in the manuscript.

Reply: We thank the reviewer for this important comment. In terms of scalability, the proposed TSV-OCT provides parallel testing and diagnosis. In conventional testing methods, for n TSVs, serial testing could take $O(n)$ cycles, and parallel testing takes $O(n)$ cycles for collecting the faulty information. Here, by dividing into groups of X TSVs ($n = X \times G$; where G is the number of groups), the testing and collection time is $O(X)$. In our 3D-NoC implementation, the execution time (testing and localizing defects) only depends on the size of the TSV connections, not on the total amount of TSVs in the chip. This makes our design scalable without adding any substantial overhead to the execution time.

To reflect the reviewer's comment we added the following passage to the revised manuscript:

Line 51-59, right column, page 7:

"In terms of scalability, by using TSV-OCT in each X-bit connection, the WCET of the system is equal to the WCET of one X-bit connection. In other words, assuming that n is the total number of TSVs in the system, conventional testing methods either require $O(n)$ for testing time (serial test) or $O(n)$ for faulty information collection time (parallel test). On the other hand, the WCET of the proposed TSV-OCT system is always $O(X)$ regardless of the total number of TSVs employed in the system."

Reviewer Point P 1.3 — In the evaluation section, the area cost in table II of encoder and decoder should be introduced in detail. How is it calculated?

Reply: We think that the reviewer is referring to Table III regarding the area cost of the encoder and decoder. The details of encoder and decoder area cost are depicted in Table II. For better clarity, we added a footnote in Table III on line 26, page 12 of the revised manuscript, as follows: "The area cost details of the employed encoder and decoder are shown in Table II"

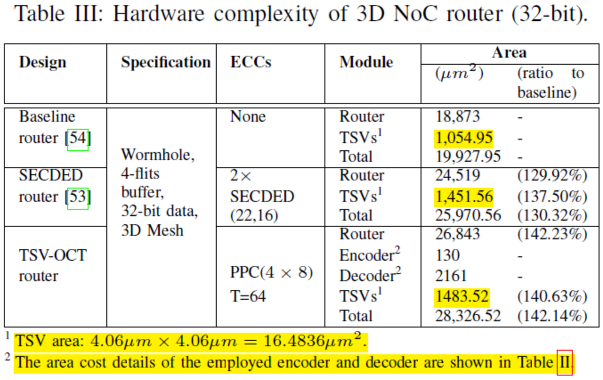


Table III: Hardware complexity of 3D NoC router (32-bit).

Design	Specification	ECCs	Module	Area	
				(μm^2)	(ratio to baseline)
Baseline router [54]	Wormhole, 4-flits buffer, 32-bit data, 3D Mesh	None	Router	18,873	-
			TSVs[1]	1,054.95	-
			Total	19,927.95	-
SECDED router [53]		2× SECDED (22,16)	Router	24,519	(129.92%)
			TSVs[1]	1,451.56	(137.50%)
			Total	25,970.56	(130.32%)
TSV-OCT router		PPC(4 × 8) T=64	Router	26,843	(142.23%)
			Encoder[2]	130	-
			Decoder[2]	2161	-
			TSVs[1]	1483.52	(140.63%)
			Total	28,326.52	(142.14%)

[1] TSV area: $4.06\mu m \times 4.06\mu m = 16.4836\mu m^2$.

[2] The area cost details of the employed encoder and decoder are shown in Table II.

Figure A-1.2: The revised Table III.

Reviewer Point P 1.4 — As we know, the size of TSV does not change with the technology node, therefore, the conversion in table III is unnecessary. Meanwhile, the test time described in table IV is usually related to test structure and test scheduling, however, the detailed test structure and scheduling process were not given.

Reply: We think that the reviewer is referring to Table IV which uses the conversion of area cost: $\texttt{Area}_{\texttt{45nm}} = \texttt{Area}_{\texttt{original}} \times (\texttt{Node}_{\texttt{original}}/45)^2$. We agree that TSV is does not scale with the technology. Our conversion is only made to compare the hardware complexity with other works.

Following the reviewer's comment, we reverse back the original values of each cited work. We also updated in more detail the information regarding the test structure and test scheduling. The new Table IV can be found on page 13 of the revised manuscript. Below in Fig. A-1.3, we included a screenshot of the revised Table IV.

Minor problems

Reviewer Point P 1.5 — In references section, [17] and [32] is the same one reference, but inconsistent.

Reply: We thank the reviewer for pointing out this mistake. We merged the reference [17] and [32] to reference [11] in the revised manuscript.

Reviewer Point P 1.6 — At line 28 and line 29 on page 3, the author depicts that "Works in [44] and [14] also proposed a test pattern generator to test open TSV defects". However, S. Mitra et. al. proposed a fault tolerance scheme, but not test pattern generator.

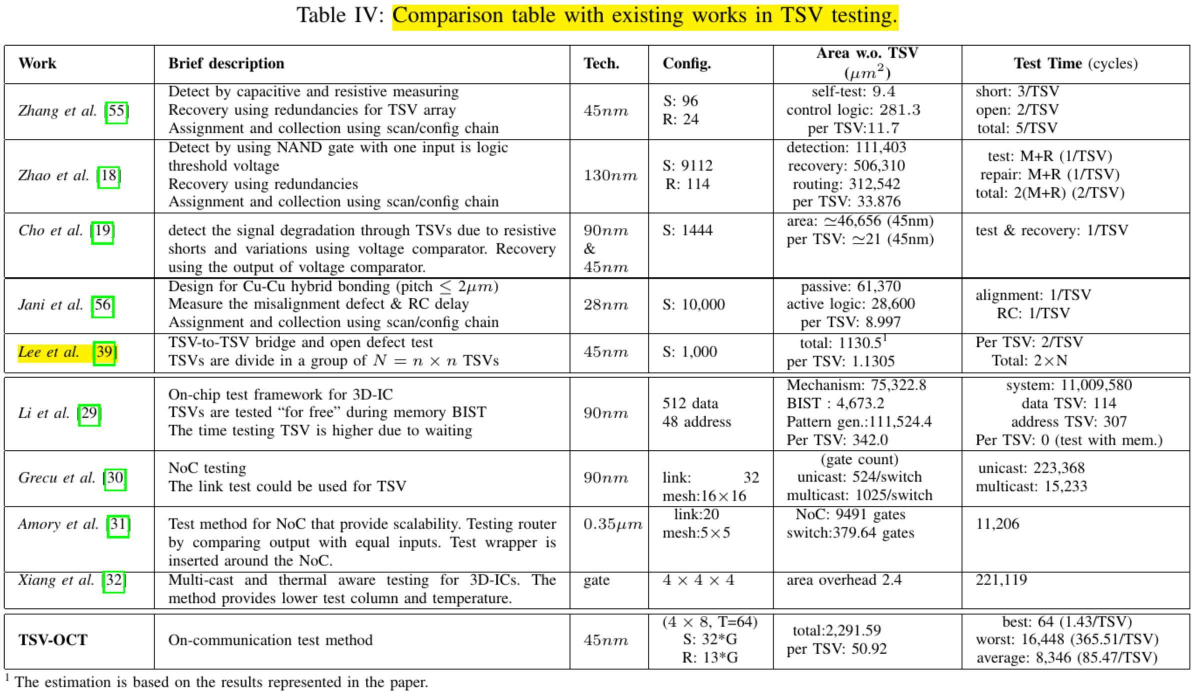


Table IV: Comparison table with existing works in TSV testing.

Work	Brief description	Tech.	Config.	Area w.o. TSV (μm^2)	Test Time (cycles)
Zhang et al. [55]	Detect by capacitive and resistive measuring Recovery using redundancies for TSV array Assignment and collection using scan/config chain	$45nm$	S: 96 R: 24	self-test: 9.4 control logic: 281.3 per TSV:11.7	short: 3/TSV open: 2/TSV total: 5/TSV
Zhao et al. [18]	Detect by using NAND gate with one input is logic threshold voltage Recovery using redundancies Assignment and collection using scan/config chain	$130nm$	S: 9112 R: 114	detection: 111,403 recovery: 506,310 routing: 312,542 per TSV: 33.876	test: M+R (1/TSV) repair: M+R (1/TSV) total: 2(M+R) (2/TSV)
Cho et al. [19]	detect the signal degradation through TSVs due to resistive shorts and variations using voltage comparator. Recovery using the output of voltage comparator.	$90nm$ & $45nm$	S: 1444	area: ≃46,656 (45nm) per TSV: ≃21 (45nm)	test & recovery: 1/TSV
Jani et al. [56]	Design for Cu-Cu hybrid bonding (pitch $\leq 2\mu m$) Measure the misalignment defect & RC delay Assignment and collection using scan/config chain	$28nm$	S: 10,000	passive: 61,370 active logic: 28,600 per TSV: 8.997	alignment: 1/TSV RC: 1/TSV
Lee et al. [39]	TSV-to-TSV bridge and open defect test TSVs are divide in a group of $N = n \times n$ TSVs	$45nm$	S: 1,000	total: 1130.5[1] per TSV: 1.1305	Per TSV: 2/TSV Total: 2×N
Li et al. [29]	On-chip test framework for 3D-IC TSVs are tested “for free” during memory BIST The time testing TSV is higher due to waiting	$90nm$	512 data 48 address	Mechanism: 75,322.8 BIST : 4,673.2 Pattern gen.:111,524.4 Per TSV: 342.0	system: 11,009,580 data TSV: 114 address TSV: 307 Per TSV: 0 (test with mem.)
Grecu et al. [30]	NoC testing The link test could be used for TSV	$90nm$	link: 32 mesh:16×16	(gate count) unicast: 524/switch multicast: 1025/switch	unicast: 223,368 multicast: 15,233
Amory et al. [31]	Test method for NoC that provide scalability. Testing router by comparing output with equal inputs. Test wrapper is inserted around the NoC.	$0.35\mu m$	link:20 mesh:5×5	NoC: 9491 gates switch:379.64 gates	11,206
Xiang et al. [32]	Multi-cast and thermal aware testing for 3D-ICs. The method provides lower test column and temperature.	gate	$4 \times 4 \times 4$	area overhead 2.4	221,119
TSV-OCT	On-communication test method	$45nm$	(4×8, T=64) S: 32*G R: 13*G	total:2,291.59 per TSV: 50.92	best: 64 (1.43/TSV) worst: 16,448 (365.51/TSV) average: 8,346 (85.47/TSV)

[1] The estimation is based on the results represented in the paper.

Figure A-1.3: New Table IV in the revised manuscript.

Reply: We thank the reviewer for this comment. We agree that the work in [44] by I. Loi, S. Mitra *et al.* did not propose a test pattern generator. We have updated the corresponding passage at line 53-56, right column, page 3 as follows:

“The work presented in [8] also proposed a test pattern generator to test open TSV defects while *Loi et al.* [41] used a test access point for injecting and collecting test vectors.”

The above reference numbers are changed in the revised manuscript from [44] to [41], and from [14] to [8].

Reviewer Point P 1.7 — At line 41 on page 3, BIST scheme on chip is used in [23], not as expressed by the author ”probing method with external testers”.

Reply: We also agree with the reviewer on this point. We removed reference [23] and only kept reference [22] as the only cited work. The work presented in [23] belongs to circuit-based testing; therefore, we cite it at line 18-20, left column, page 4:

“Probing before bonding with external testers [16] is also helpful to improve the overall yield rate.”

The above reference number is changed in the revised manuscript from [22] to [16].

Reviewer Point P 1.8 — At line 55 on page 10, smaller T values give higher average response time. The reason should be explained clearly.

Reply: This can be explained by the fact that multiple defects cause more hidden faults in the detection process. By using small T values, *TSV-OCT* concludes the detection process quicker

than with larger T, which increases the probability of missing hidden defects. Here, we define the response time as the time from which the detection process begins to the time where all faults are found. Because of the missing fault pattern, lower T values need more iterations than higher ones to complete. We also want to note that the average WCET is calculated for the successful cases only. We clarify this point in line 54-56, right column, page 10:
"This is due to the fact that having smaller T values leads to higher hidden fault probabilities which need more iterations for localization."

Reviewer Point P 1.9 — At line 30 on page 11, the size of TSV should be 15 um * 15 um, not "15 u * 15 u". And the size here is different from the data given on page 7

Reply: We understand the reviewer's comment and we apologize for the confusion. In the revised manuscript, we removed the text in page 11 to avoid repetition. We also corrected this point in the revised manuscript at line 49-50, left column, page 8 as follows:
"The TSV size and pitch are $4.06\mu m \times 4.06\mu m$, and $15\mu m$, respectively."

Figure A-1.4 shows the corrected area and pitch size of TSV.

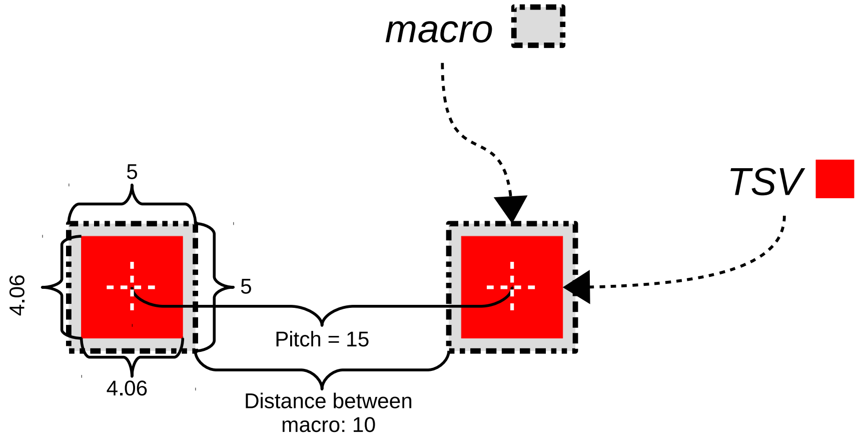


Figure A-1.4: TSV Layout in our design: TSV in red box, the macro area in gray box.

Reviewer Point P 1.10 — At line 31 on page12,the literature [26] from table IV aims to detect the signal degradation through TSVs due to resistive shorts, which is not as the author said "for open-defect". Meanwhile, IBM 90 nm CMOS technology is used in [26], which is not comparable with this manuscript.

Reply: We thank the reviewer for this correction. As previously mentioned in Review Point P 1.4, we have accordingly updated Table IV. The screenshot of this table was previously shown in Figure A-1.3 of this document).

Also , as recommended by the reviewer, we also corrected the description for the work presented [26] and kept the original value of their papers. We refer to the work in [26] for both IBM 90nm and 45nm and we picked 45nm for comparison since our work is on 45nm.

Reviewer 2

Reviewer Point P 2.1 — In the abstract, “On the other hand, an implementation of TSV-OCT on 3D Network on-Chip router shows only 8.66% of logic area overhead while showing no performance degradation for testing.” Here what method is compared to obtain the result 8.66%?

Reply: We agree with the reviewer on this important point. In the initial manuscript, we aimed to compare with the SECDED-based 3D-NoC design in [53]. However, we realize that this comparison can be confusing and cannot fully demonstrate the trade-offs of *TSV-OCT*. To avoid any confusion for the readers about this number, we removed the comparison from the abstract in the revised manuscript. The following new sentence is updated in line 26-28, page 1 as follows: “On the other hand, an implementation of *TSV-OCT* on a 3D Network-on-Chip router shows no performance degradation for testing while having a reasonable area overhead.”

[53] K. N. Dang et al., “A low-overhead soft–hard fault-tolerant architecture, design and management scheme for reliable high-performance many- core 3D-NoC systems,” The Journal of Supercomputing, vol. 73, no. 6, pp. 2705–2729, Jun 2017.

Reviewer Point P 2.2 — Page 1, Line 44-47: “we can observe that on-line detection is still one of the major challenges for safety critical applications which require short response times to newly occurred faults.” This conclusion can not be drawn from the previous paragraph. This part lacks evidence, and the research motivation is not clear. In addition, it seems better to use “response time” instead of “response times”.

Reply: We would like to thank the reviewer for this comment. Our major argument is that real-time 3D-IC systems must tackle the TSV reliability on-line. Manufacturing test/recovery could solve this problem at the initial state; however, aging devices encounter new faults that could lead to undesirable consequences. Taking into account the reviewer’s comment, we updated the sentences as follows to link the issues to our motivation in line 43-51, right column page 1 as follows:

“To maintain highly reliable real-time systems, fault detection and recovery is an important task. So, it must be deadline-driven and still maintain other tasks’ operations [27]. However, most of the existing methods on solving the reliability issues of TSVs focus on manufacturing test and recovery while the online lifetime reliability is not properly addressed. Because of the consequences of silent defects could be expensive, the defect detection tasks require short response time and less performance degradation.”

We also took into consideration the reviewer’s comment and we changed the “response times” to “response time” for the entire manuscript.

Reviewer Point P 2.3 — Page 2, Line 26, 2) “The testing epoch or period is also a critical parameter” lacks the definition of period and respond time, it is difficult for readers to clarify the internal logic connection of this content. Furthermore, it is said that 10000 circles are considered as a reasonable period in 2) subsection, however, “hundred thousands or even millions of cycles" is mentioned in 1) subsection. There is contradiction between these, and in fact which cycle is considered as a period?

Reply: We thank the reviewer for this important comment. We would like to address it as follows:

- Since "epoch" and "period" in our paper have the the same meaning, we removed "epoch" from the manuscript and used "testing period" for consistency.
- We clarified the definition of the "testing period" at line 13-14, left column, page 2: "The testing period, which is the interval between two consecutive testings, is also a critical parameter."
- The reason why the work by Wang et al. [11] and Kakoee et al. [33] have smaller testing period (10,000 and 16,000) while conventional SoC BISTs take hundred thousands or even millions of cycles is that they use the free time slot for testing. To understand this point, we added a new "Figure 2" to the revised manuscript (Figure A-2.5 in this answer document) Strategy (d) in Figure A-2.5 shows the method of Wang et al. [11], while Strategy (b) is the conventional BIST mechanism. Therefore, we clarified this difference in line 3-4, left column, page 2 of the revised manuscript:
  "Reusing BIST as P-BIST usually takes a considerable amount of time while blocking the system operation."
- We also added in line 10-12, left column, page 2:
  "Online testing with data traffic priority [11, 33] could lower the testing time while maintaining the system's operation."
- If Wang et al. [11] and Kakoee et al. [33] reduce their testing period, the impact on performance is significant.

Reviewer Point P 2.4 — Page 2, Line 8,what does ΔTask and ΔBist mean?

Reply: As suggested by the reviewer we clarified the corresponding passage in line 51-52, left column, page 2 as follows:

"In normal P-BISTs, depicted as the periodic test, the response time is $\Delta_{Task} + \Delta_{BIST}$ ($\Delta_{Task} \leq Period$) where Δ_{Task} and Δ_{BIST} are the execution time of regular tasks and BIST, respectively ."

Reviewer Point P 2.5 — Page3, in Section II-B, the description of previous work is too general, and it is more like the current research situations, which is better to be placed in Section I. Related works (Section II-B) should introduce the concrete idea and the merits and demerits illustrated with graphics.

Reply: Taking into account the reviewer's comment, we have significantly improved the related work section. First, we added a discussion on the merits and demerits as follows:

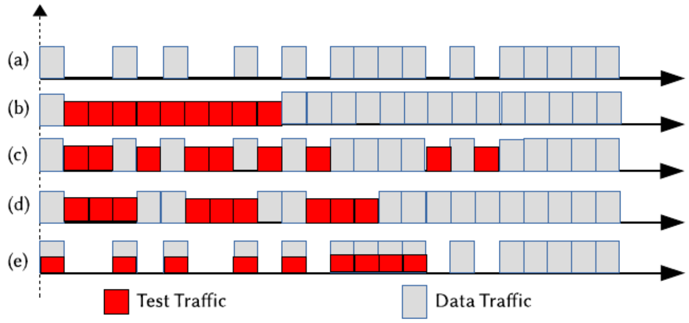


Figure 2: The sequence of data and test traffic under different strategies: (a) application traffic; (b) block test; (c) free time test traffic injection; (d) split free time test [11]; (e) on-communication test.

Figure A-2.5: New Figure 2

- Line 40-42, right column, page 3 discussed about coding techniques:
  “While EDCs/ECCs usually provide immediate response time, they are limited by a certain number of detectable/correctable defects.”

- Line 20-25, left column, page 4 discuss about BISTs and dedicate circuits:
  “ While this type of methods (BISTs/dedicated circuits) could provide good faults coverage , their main problem is the need of detaching tested devices/modules from the system which is not affordable in critical applications.”

- Line 37-41, left column, page 4 discuss about scheduling P-BIST:
  “The common goal between these methods is to provide a smart schedule to avoid creating congestion/degradation on the system. Because their experiments are limited in terms of size, the execution time could escalate by complicating the system.”

- Line 48-51, left column, page 4 discuss about other methods (redundant execution, dynamic verification, and anomaly detection):
  “Although these methods are efficient with deep integration into the system, the vulnerability of TSVs should be delicately addressed (i.e. defect location, real-time detection).”

Second, to better illustrate the previous testing methods and ours, we added a new “Figure 2” to the revised manuscript (previously introduced in this answer document as Figure A-2.5). We added the following paragraph to discuss “Figure 2” at line 53-59, left column, page 4:

“Figure 2 illustrates the different testing strategies. While the blocking test (i.e. P-BIST), depicted in Strategy (b) needs to block the data traffic in order to send the test traffic, Strategies (c) and (d) schedule the test traffic to have less congestion. Strategy (e) represents our OCT methods, where the test is performed together with the data transaction causing no congestion nor performance degradation.”

Reviewer Point P 2.6 — Page 7, pitch already includes keep-out zone, why define 10μm, 15μm repeatedly?

Reply: We have corrected this information in the revised manuscript. The new sentence is in page 8, left column, line 50-51 as follow:
"The TSV size and pitch are $4.06\mu m \times 4.06\mu m$, and $15\mu m$, respectively."

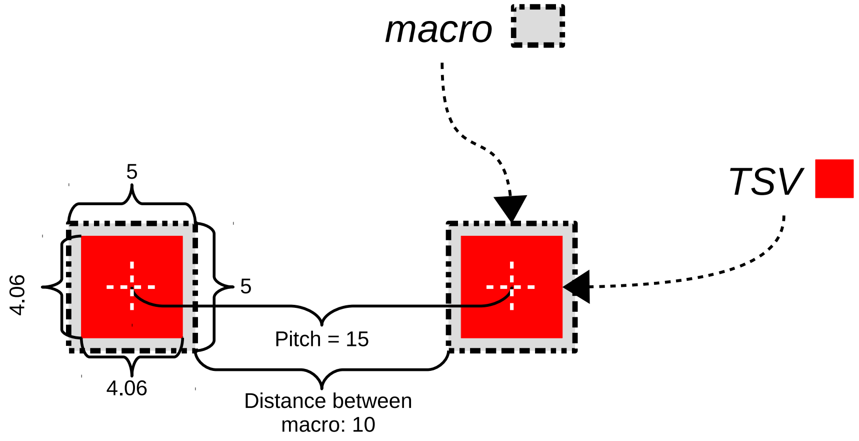


Figure A-2.6: TSV Layout in our design: TSV in red box, the macro area in gray box.

Reviewer Point P 2.7 — Page 11, Line 30, "For a TSV of 15u * 15u", here should be 15 um * 15 um. Page 7 defines TSV size: 10 um * 10 um, which is different from Page 11. What size in fact is the TSV size, and the experimental results may need total change

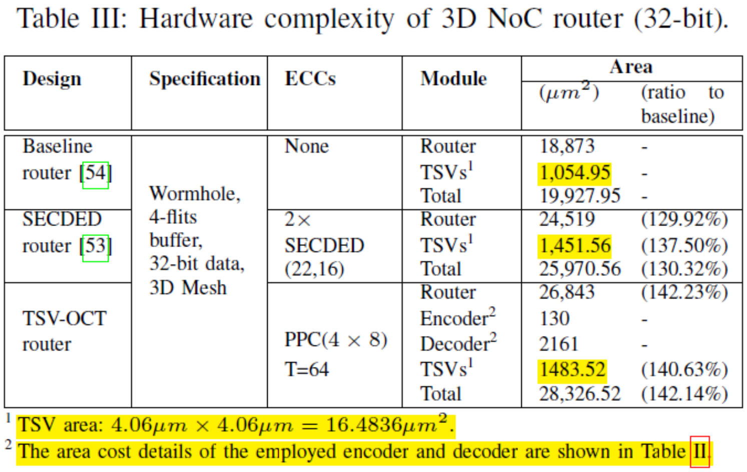
Reply: We thank the reviewer for pointing out this confusing point. Figure A-2.6 of this document explains our TSV design parameters. As can be seen in this figure, the pitch is be $15\mu m$ which has also been corrected in the revised manuscript.

We also updated Table III (page 12) with the correct TSV area cost as depicted in Figure A-2.7:

Reviewer Point P 2.8 — Page 12, in Table IV, Cho et al [26] used IBM 90 nm CMOS technology, which is not the same technology condition with this manuscript.

Reply: We thank the reviewer for suggesting this correction. We have updated Table IV (page 13) as shown in the below Figure A-2.8. We have also corrected the description for reference [26] and kept the original values of their papers. We refer to the work in [26] for both IBM 90nm and 45nm and we picked 45nm for comparison since our work is on 45nm.

Reviewer Point P 2.9 — Page 2, 5) subsection mentioned "Intermittent defect of TSV", however, the proposed scheme seems not be able to detect and localize the intermittent defects.



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[1] TSV area: $4.06\mu m \times 4.06\mu m = 16.4836\mu m^2$.

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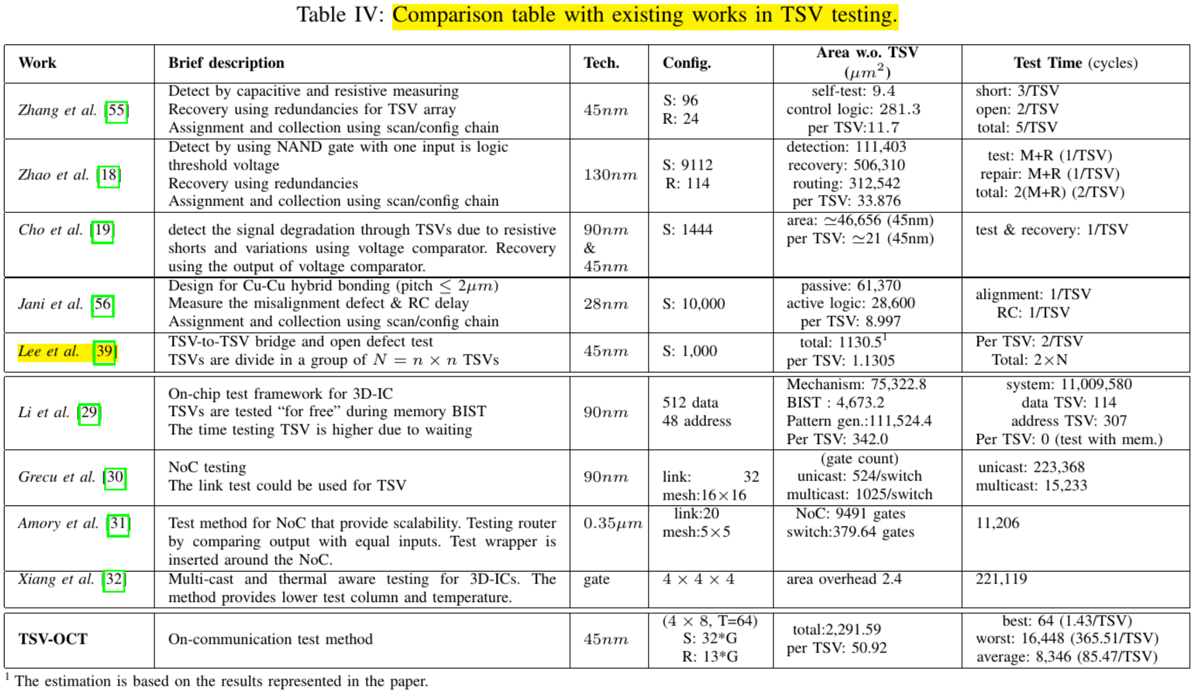
Figure A-2.7: Revised Table III.



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Zhang et al. [55]	Detect by capacitive and resistive measuring Recovery using redundancies for TSV array Assignment and collection using scan/config chain	$45nm$	S: 96 R: 24	self-test: 9.4 control logic: 281.3 per TSV:11.7	short: 3/TSV open: 2/TSV total: 5/TSV
Zhao et al. [18]	Detect by using NAND gate with one input is logic threshold voltage Recovery using redundancies Assignment and collection using scan/config chain	$130nm$	S: 9112 R: 114	detection: 111,403 recovery: 506,310 routing: 312,542 per TSV: 33.876	test: M+R (1/TSV) repair: M+R (1/TSV) total: 2(M+R) (2/TSV)
Cho et al. [19]	detect the signal degradation through TSVs due to resistive shorts and variations using voltage comparator. Recovery using the output of voltage comparator.	$90nm$ & $45nm$	S: 1444	area: ≃46,656 (45nm) per TSV: ≃21 (45nm)	test & recovery: 1/TSV
Jani et al. [56]	Design for Cu-Cu hybrid bonding (pitch $\leq 2\mu m$) Measure the misalignment defect & RC delay Assignment and collection using scan/config chain	$28nm$	S: 10,000	passive: 61,370 active logic: 28,600 per TSV: 8.997	alignment: 1/TSV RC: 1/TSV
Lee et al. [39]	TSV-to-TSV bridge and open defect test TSVs are divide in a group of $N = n \times n$ TSVs	$45nm$	S: 1,000	total: 1130.5[1] per TSV: 1.1305	Per TSV: 2/TSV Total: 2×N
Li et al. [29]	On-chip test framework for 3D-IC TSVs are tested “for free” during memory BIST The time testing TSV is higher due to waiting	$90nm$	512 data 48 address	Mechanism: 75,322.8 BIST : 4,673.2 Pattern gen.:111,524.4 Per TSV: 342.0	system: 11,009,580 data TSV: 114 address TSV: 307 Per TSV: 0 (test with mem.)
Grecu et al. [30]	NoC testing The link test could be used for TSV	$90nm$	link: 32 mesh:16×16	(gate count) unicast: 524/switch multicast: 1025/switch	unicast: 223,368 multicast: 15,233
Amory et al. [31]	Test method for NoC that provide scalability. Testing router by comparing output with equal inputs. Test wrapper is inserted around the NoC.	$0.35\mu m$	link:20 mesh:5×5	NoC: 9491 gates switch:379.64 gates	11,206
Xiang et al. [32]	Multi-cast and thermal aware testing for 3D-ICs. The method provides lower test column and temperature.	gate	4 × 4 × 4	area overhead 2.4	221,119
TSV-OCT	On-communication test method	$45nm$	(4 × 8, T=64) S: 32*G R: 13*G	total:2,291.59 per TSV: 50.92	best: 64 (1.43/TSV) worst: 16,448 (365.51/TSV) average: 8,346 (85.47/TSV)

[1] The estimation is based on the results represented in the paper.

Figure A-2.8: New Table IV in the revised manuscript.

Reply: We agree with the reviewer on this important point. We would like to clarify that our method can only ensure the detection and localization of intermittent faults only if they last more than the Intermittent Detection Window (IDW). We define this window as $2\times$ the Worst Case Execution Time (WCET) of TSV-OCT. For instance, with a 32-bit data, the WCET is evaluated to 16,488 cycles. If the intermittent fault lasts for more than IDWs ($2 \times 16,488 = 32,976$ cycles), a run of the proposed TSV-OCT can detect the faulty position.

When it comes to the types of faults that TSV-OCT can deal with, there are different intermittent fault sources such as voltage, frequency, temperature and stress/vibration as stated in [Ref 1] by Cristian Constantinescu from AMD: *"Extensive laboratory tests have shown that voltage, frequency, and temperature variations may activate or deactivate intermittent faults"*. For TSVs, stress or vibration could be other sources of intermittent defects. [Ref 2] also points out the aging factor that could affect intermittent defects. Single event upsets (SEU) could also cause intermittent faults or transient faults. The fast-changing intermittent or transient faults could be corrected by the built-in ECC module in the proposed TSV-OCT

Beside SEUs, which usually last for only one or several cycles, the other sources last for hundred thousands cycles or even more. For instance, the temperature or stress related faults stay for several seconds or minutes which can be millions of cycles for a given design. This duration is always greater than the required IDW constraint; thus, allowing the proposed methodology to easily detect such faults. In DFVS (Dynamic voltage and frequency scaling), voltage and frequency could quickly change; however, it is not efficient in terms of power and reliability (timing violations) to change them too frequently.

To understand how TSV-OCT could detect intermittent faults under IDW, let us consider an intermittent open defect which creates an open resistance between two terminals of a TSV. As a textbook theory, the resistance increases together with the temperature. Figure A-2.9 illustrates the thermal activated intermittent case where the open defect cause timing violations or even electrical disconnections at high temperatures. When the temperature is lowered, the defect disappears and could not be detected. As shown in Figure A-2.9, TSV-OCT operates in parallel with the TSV data transactions. Right after the intermittent defect is activated, one run of TSV-OCT could detect and localize this defect. Therefore, it could catch the defect during the high temperature interval. This is in contrast to the *P-BIST*, as depicted in Figure A-2.9, since its periodic execution runs at the lower temperature intervals; thus, the defect is missed.

In conclusion, to ensure that the proposed TSV-OCT can localize intermittent defects, Intermittent Detection Window (IDW) must be at least $2\times$ Worst Case Execution Time (WCET).

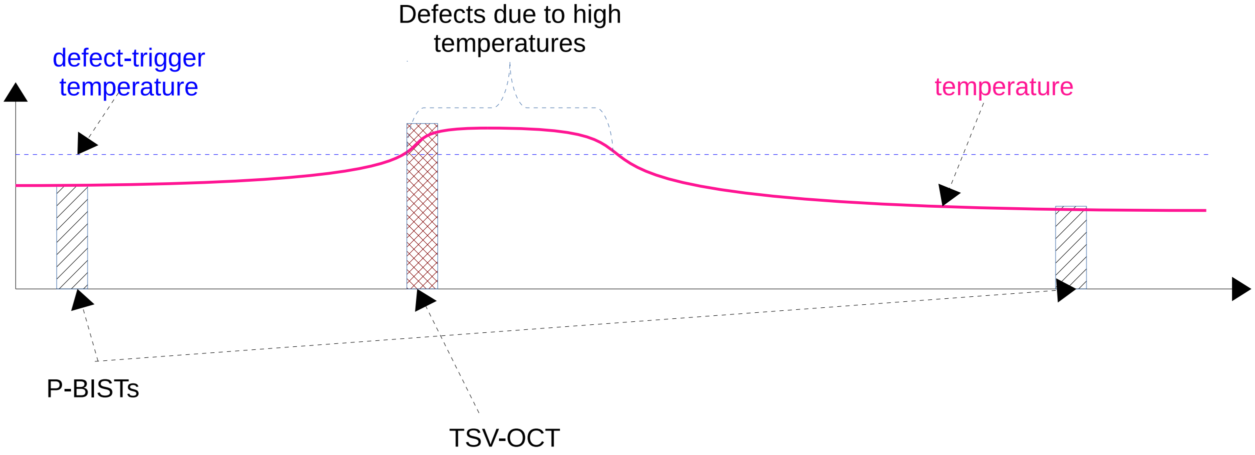


Figure A-2.9: Intermittent behavior of TSV.

To highlight the reviewer's comment, we edited the manuscript as follows:

- In line 59 left column to line 51 right column, page 6:
  "Because intermittent faults occur in certain conditions and may vary among the products due to process variation, *TSV-OCT* detects TSV intermittent defects by constantly monitoring the operation of TSVs. However, it is important to mention that the condition to successfully execute this detection is that these intermittent faults must last at least $2\times$ WCET. Such a duration ensures at least one complete run of TSV-OCT to detect the fault. Nevertheless, last changing intermittent or transient faults could be corrected by the built-in ECC in *TSV-OCT*. "
- In line 19-23, right column, page 12, we added a sub-section "Discussion" with the following text:
  "As previously mentioned, *TSV-OCT* also tackles intermittent faults. Since the WCETs of *TSV-OCT* are fixed, designers could choose a proper configuration to ensure the detection and localization of this type of faults during the Intermittent Detection Window (IDW), which is defined as $2\times$ WCET. "

[Ref 1] Constantinescu, Cristian. "Intermittent faults and effects on reliability of integrated circuits." 2008 Annual Reliability and Maintainability Symposium. IEEE, 2008.

[Ref 2] Qi, H., Ganesan, S., & Pecht, M. (2008). No-fault-found and intermittent failures in electronic products. Microelectronics Reliability, 48(5), 663–674. doi:10.1016/j.microrel.2008.02.003

Reviewer Point P 2.10 — According to the title and the introduction section, this scheme is scalable, however, this manuscript doesn't strongly reflect the scalability.

Reply: We thank the reviewer for this important comment. In terms of scalability, the proposed TSV-OCT provides parallel testing and diagnosis. In conventional testing methods, for n TSVs, serial testing could take $O(n)$ cycles, and parallel testing takes $O(n)$ cycles for collecting the faulty information. Here, by dividing into groups of X TSVs ($n = X \times G$; where G is the number of groups), the testing and collection time is $O(X)$. In our 3D-NoC implementation, the execution time (testing and localizing defects) only depends on the size of the TSV connections, not on the total amount of TSVs in the chip. This makes our design scalable without adding any substantial overhead to the execution time.

To reflect the reviewer's comment we added the following passage to the revised manuscript:
Line 51-59, right column, page 7:

"In terms of scalability, by using TSV-OCT in each X-bit connection, the WCET of the system is equal to the WCET of one X-bit connection. In other words, assuming that n is the total number of TSVs in the system, conventional testing methods either require $O(n)$ for testing time (serial test) or $O(n)$ for faulty information collection time (parallel test). On the other hand, the WCET of the proposed TSV-OCT system is always $O(X)$ regardless of the total number of TSVs employed in the system."

Reviewer Point P 2.11 — The detailed calculation of hardware area,response time and test time are not given, thus, the results in Table II and III seems not evidential.

Reply: Taking into consideration the reviewer's comment, we added the response time (min and max) to Table II in page 12. Furthermore, details about localization rate, average execution time could be found on separated evaluation sections. The details of hardware, response time of Table III could be seen in Table II.

We added a footnote for the Table II (screenshot in Figure A-2.10 bellow) at page 12 as follows:

"More details about the response time and localization rate could be seen in Section IV-C and IV-D."

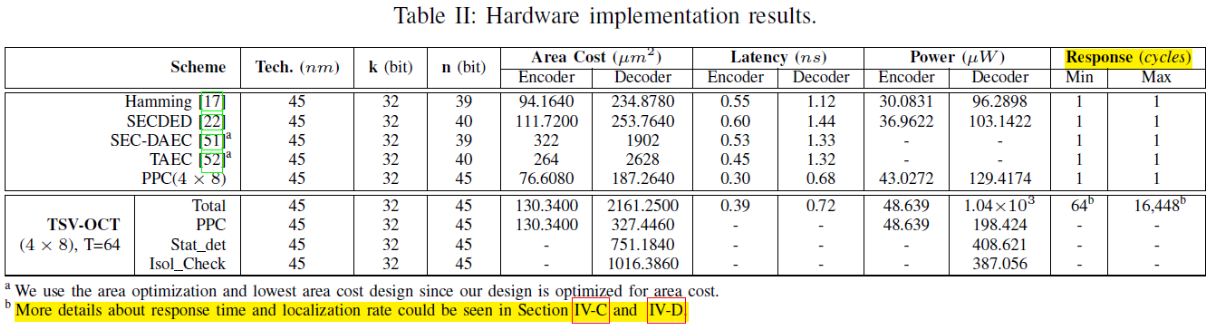


Table II: Hardware implementation results.

Scheme		Tech. (nm)	k (bit)	n (bit)	Area Cost (μm^2)		Latency (ns)		Power (μW)		Response (*cycles*)	
					Encoder	Decoder	Encoder	Decoder	Encoder	Decoder	Min	Max
Hamming [17]		45	32	39	94.1640	234.8780	0.55	1.12	30.0831	96.2898	1	1
SECDED [22]		45	32	40	111.7200	253.7640	0.60	1.44	36.9622	103.1422	1	1
SEC-DAEC [51][a]		45	32	39	322	1902	0.53	1.33	-	-	1	1
TAEC [52][a]		45	32	40	264	2628	0.45	1.32	-	-	1	1
PPC(4 × 8)		45	32	45	76.6080	187.2640	0.30	0.68	43.0272	129.4174	1	1
TSV-OCT (4 × 8), T=64	Total	45	32	45	130.3400	2161.2500	0.39	0.72	48.639	1.04×10^3	64[b]	16,448[b]
	PPC	45	32	45	130.3400	327.4460	-	-	48.639	198.424	-	-
	Stat_det	45	32	45	-	751.1840	-	-	-	408.621	-	-
	Isol_Check	45	32	45	-	1016.3860	-	-	-	387.056	-	-

[a] We use the area optimization and lowest area cost design since our design is optimized for area cost.
[b] More details about response time and localization rate could be seen in Section IV-C and IV-D.

Figure A-2.10: Revised Table II.

For better clarity, we added a footnote in Table III (screenshot in Figure A-2.11) on page 12 (line 26) of the revised manuscript, as follows:

"The area cost details of the employed encoder and decoder are shown in Table II."

Reviewer 3

Reviewer Point P 3.1 — The novelty of this paper is not good enough because the idea of the row and column check in the statistical detector is not new, for example see Ref [A], that shows the detailed DFT for the TSV test architecture by devising a two-dimensional (row and column) method. Please review and compare proposed work with Ref [A].

Ref [A]: Y. Lee et al, "Grouping-Based TSV Test Architecture for Resistive Open and Bridge Defects in 3-D-ICs," IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, vol. 36, no.10, pp.1759-1763, 2017.

Reply: We thank the reviewer for this critical comment. We agree that the idea of row and column check is not new. In fact, we put the *Parity Product Code*, which uses column and row check, in the Background section.

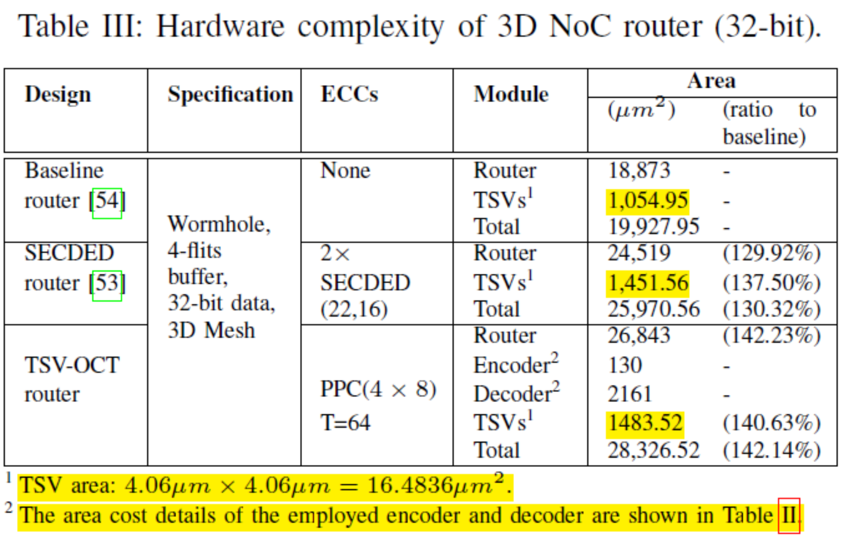


Table III: Hardware complexity of 3D NoC router (32-bit).

Design	Specification	ECCs	Module	Area	
				(μm^2)	(ratio to baseline)
Baseline router [54]	Wormhole, 4-flits buffer, 32-bit data, 3D Mesh	None	Router	18,873	-
			TSVs[1]	1,054.95	-
			Total	19,927.95	-
SECDED router [53]		2× SECDED (22,16)	Router	24,519	(129.92%)
			TSVs[1]	1,451.56	(137.50%)
			Total	25,970.56	(130.32%)
TSV-OCT router		PPC(4 × 8) T=64	Router	26,843	(142.23%)
			Encoder[2]	130	-
			Decoder[2]	2161	-
			TSVs[1]	1483.52	(140.63%)
			Total	28,326.52	(142.14%)

[1] TSV area: $4.06\mu m \times 4.06\mu m = 16.4836\mu m^2$.

[2] The area cost details of the employed encoder and decoder are shown in Table II.

Figure A-2.11: Revised Table III.

Although the *Parity Product Code* is not our novelty, in the introduction, we showed that our contributions are in the proposed two algorithms: *Statistical Detection* and *Isolation and Check*. This method is based on the row/column check; but, we believe that their additional contributions are significant for publication. Also, while Ref [A] is for BIST, our method is for online and non-blocking testing which focuses on different stages of reliability.

Taking into consideration the reviewer's comment, we cited Ref [A] and added comparison with it in the following passages highlighted in the revised manuscript.

- line 29-30, left column, page 4:
  "The TSV grouping method and column/row check can also be found in [39]."

- line 46-47, right column, page 4:
  "In [39],the authors presented a grouping method with column and row check for testing both open and bridge defects and reduce the testing time."

- page 13: We added comparison with Lee et al. [39] in Table IV, page 13 (see Figure A-3.12 in the next page).

Reviewer Point P 3.2 — The paper is not yet considered the TSV-to-TSV bridge fault model. It is required to add the TSV-to-TSV bridge defect cases with the statistical detector in order to prove its detectability of the TSV-to-TSV bridge defect in the revised draft.

Reply: We thank the reviewer for another critical comment. We agree that the TSV-to-TSV bridge is not explicitly considered in the manuscript. However, we argue that the proposed TSV-OCT consists of algorithms that can also work with bridge defects without any modifications. In fact, after careful analysis of our Monte-Carlo simulations, which have 10,000 cases for each

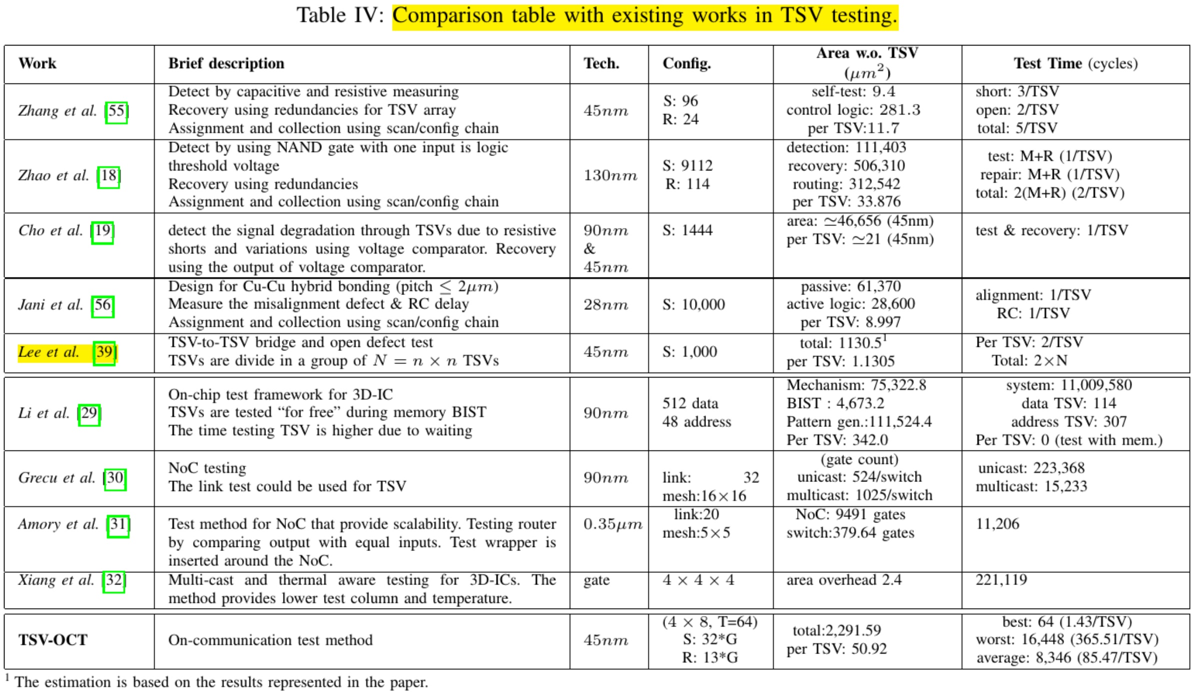


Table IV: Comparison table with existing works in TSV testing.

Work	**Brief description**	**Tech.**	**Config.**	**Area w.o. TSV** (μm^2)	**Test Time** (cycles)
Zhang et al. [55]	Detect by capacitive and resistive measuring Recovery using redundancies for TSV array Assignment and collection using scan/config chain	$45nm$	S: 96 R: 24	self-test: 9.4 control logic: 281.3 per TSV:11.7	short: 3/TSV open: 2/TSV total: 5/TSV
Zhao et al. [18]	Detect by using NAND gate with one input is logic threshold voltage Recovery using redundancies Assignment and collection using scan/config chain	$130nm$	S: 9112 R: 114	detection: 111,403 recovery: 506,310 routing: 312,542 per TSV: 33.876	test: M+R (1/TSV) repair: M+R (1/TSV) total: 2(M+R) (2/TSV)
Cho et al. [19]	detect the signal degradation through TSVs due to resistive shorts and variations using voltage comparator. Recovery using the output of voltage comparator.	$90nm$ & $45nm$	S: 1444	area: ≃46,656 (45nm) per TSV: ≃21 (45nm)	test & recovery: 1/TSV
Jani et al. [56]	Design for Cu-Cu hybrid bonding (pitch $\leq 2\mu m$) Measure the misalignment defect & RC delay Assignment and collection using scan/config chain	$28nm$	S: 10,000	passive: 61,370 active logic: 28,600 per TSV: 8.997	alignment: 1/TSV RC: 1/TSV
Lee et al. [39]	TSV-to-TSV bridge and open defect test TSVs are divide in a group of $N = n \times n$ TSVs	$45nm$	S: 1,000	total: 1130.5[1] per TSV: 1.1305	Per TSV: 2/TSV Total: 2×N
Li et al. [29]	On-chip test framework for 3D-IC TSVs are tested "for free" during memory BIST The time testing TSV is higher due to waiting	$90nm$	512 data 48 address	Mechanism: 75,322.8 BIST : 4,673.2 Pattern gen.:111,524.4 Per TSV: 342.0	system: 11,009,580 data TSV: 114 address TSV: 307 Per TSV: 0 (test with mem.)
Grecu et al. [30]	NoC testing The link test could be used for TSV	$90nm$	link: 32 mesh:16×16	(gate count) unicast: 524/switch multicast: 1025/switch	unicast: 223,368 multicast: 15,233
Amory et al. [31]	Test method for NoC that provide scalability. Testing router by comparing output with equal inputs. Test wrapper is inserted around the NoC.	$0.35\mu m$	link:20 mesh:5×5	NoC: 9491 gates switch:379.64 gates	11,206
Xiang et al. [32]	Multi-cast and thermal aware testing for 3D-ICs. The method provides lower test column and temperature.	gate	$4 \times 4 \times 4$	area overhead 2.4	221,119
TSV-OCT	On-communication test method	$45nm$	(4×8, T=64) S: 32*G R: 13*G	total:2,291.59 per TSV: 50.92	best: 64 (1.43/TSV) worst: 16,448 (365.51/TSV) average: 8,346 (85.47/TSV)

[1] The estimation is based on the results represented in the paper.

Figure A-3.12: New Table IV in the revised manuscript.

test, we found that some cases of TSV-to-TSV bridge defects were considered during our initial simulation. Hereafter, we would like to explain this point in two arguments:

1) **The logic-level behavior of TSV-to-TSV defects is similar to open/short defect's**. Assuming two TSVs are bridged together, if we send two different values, the output terminal will be in a floating voltage (metastability), which is faulty. If both TSVs send the same value, the output terminal is correct. At the end of a possible metastability, the logic-level could be either 0 or 1. In terms of probability, the hidden defect probability will be 0.75 which is higher than the current defect model (open/short) which needs higher T-values to localize.

2) **In our Monte-Carlo simulation, because the faulty positions are randomized, the bridge defects are already simulated**. Figure A-3.13 shows the case of 3 defects on 5x5 TSVs, where Figure A-3.13 (a) is just a random case. However, Figure A-3.13 (b) shows two nearby TSVs having defects. Therefore, their faulty behavior is similar to a bridge defect between TSV(0,1) and TSV(0,2) and an open/short defect in TSV(2,1). Finally, Figure A-3.13 (c) shows a similar case to a bridge defect between TSV(0,1), TSV(0,2) and TSV(1,1).

Because we performed 10,000 Monte-Carlo simulation cases for each test, the bridge defects are already included in this evaluation. For instance, let us consider the 4x4 case which has 25 TSVs, the number of cases are:

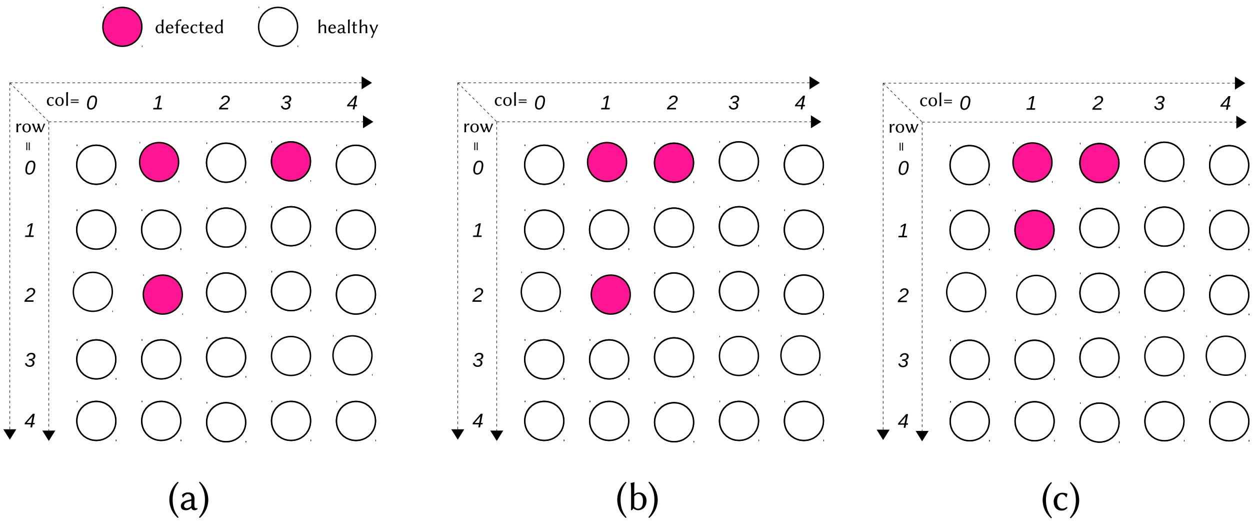


Figure A-3.13: A Monte-Carlo simulation for 3 defects in a group of 5x5 TSVs.

$$\text{2 defects in 25 TSV has } \binom{25}{2} = 300 \text{ cases}$$

$$\text{3 defects in 25 TSV has } \binom{25}{3} = 2300 \text{ cases}$$

$$\text{4 defects in 25 TSV has } \binom{25}{4} = 12650 \text{ cases}$$

Therefore, we could say that we already covered all possible combinations of 2 and 3 TSVs defect. Consequently, the bridge between 2-3 TSVs are already included.

Because the manuscript did not target the TSV-to-TSV bridge defects, we did not change the results. Instead, we included some discussions to help clearing out the concern of the reviewer. Line 40-47, right column, page 12:

"Testing methods for TSV-to-TSV bridge defects [39] have not been evaluated in our paper. However, because of the inconsistency of TSV-to-TSV bridge defects (i.e. hidden faults occurring if the bridged TSVs send the same value), our proposal could handle the defect without any modification. We would like to note that among the conducted 10,000 Monte-Carlo simulation cases for each configuration, there are multiple cases having two or more adjacent defected TSVs."

Also, to validate our claim for the ability of our proposal to work around bridge defects, we performed the simulation of 2-10 faults and PPC(4x8) while only considering bridge defects. To not over-complicate the paper with many different contents, we decided not to include the following analysis in the revised manuscript to avoid any confusion for readers. The method to generate the fault positions is described as follows:

1. Randomly generate the first defect position.

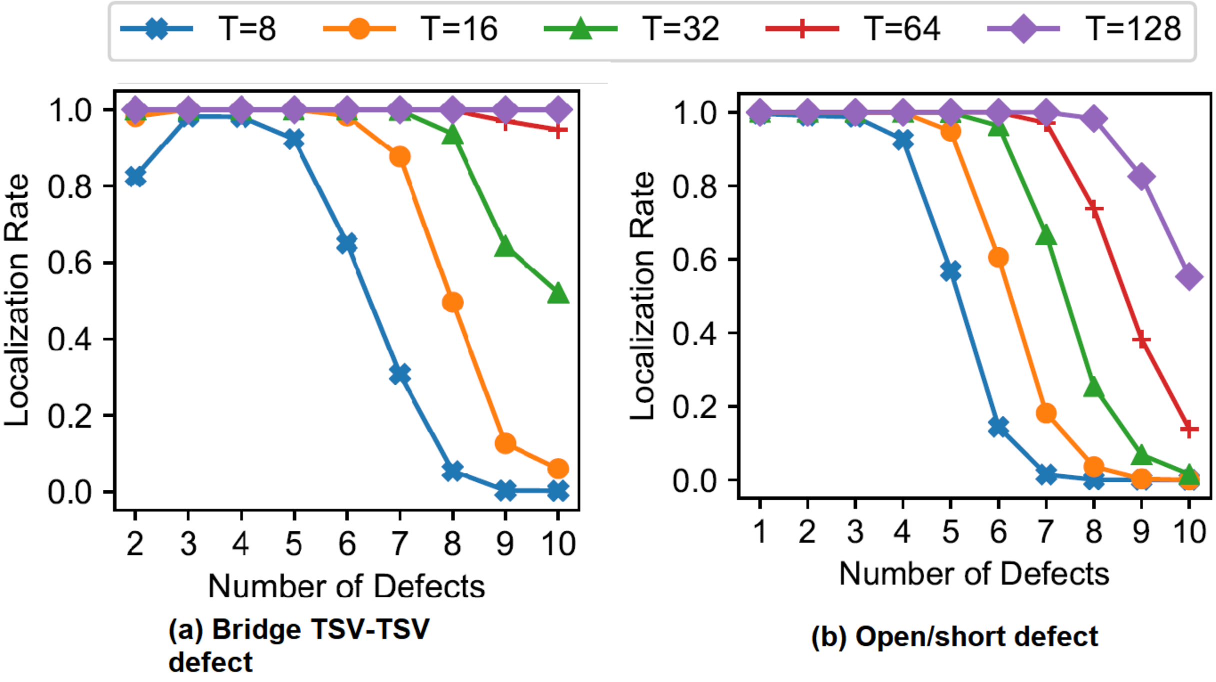
2. List the neighboring TSVs of the defected TSV in a 2D Mesh (X-, X+, Y-, Y+), the border TSV has less neighbors.

3. Randomly generate new defect positions based on the list of neighboring TSVs

4. Repeat Steps (2) and (3) until enough defects are populated.

5. Execute with the following rules:

   - If the inputs of bridged TSVs have different values, start deciding the new value.
   - If most inputs of bridged TSVs are 1, assign 1 as the outputs.
   - If most inputs of the bridged TSVs are 0, assign 0 as the outputs.
   - If the number of ’1’ and ’0’ are the same, randomly assign the output value to 0 or 1.



(a) Bridge TSV-TSV defect

(b) Open/short defect

Figure A-3.14: Defects Monte-Carlo simulation for: (a) TSV-to-TSV bridge (b) Open/short.

Figure A-3.14 shows the comparison between the defect localization performance without false positive of TSV-OCT with bridge and open/short defect. The configuration of this simulation is as follows: 1000 Monte-Carlo simulation tests, 32 data-bit (4x8), T = 8, 16, 32, 64, and 128. Figure A-3.14 (b) is a copy of Figure 12 (c) in the revised manuscript. As can be observed in Figure A-3.14, the behavior of bridge defects with T>=16 is similar to the open/short case. However, TSV-OCT is more effective with this type of defects than the open/short one. This is due to the fact that the bridge patterns are on the nearby TSVs which help the TSV-OCT to easily localize the defects. However, we also observe an abnormal drop in accuracy when considering two TSV-TSV bridge defects with lower T values. This can be explained by the fact that the probability of hidden faults is higher than open/short defect. In open/short defect, a random input has a one-cycle hidden fault probability of 0.5 (50%). With bridge defects, the probability of a one-cycle hidden fault is 0.75 (75%) due to the following reasons:

- If two inputs are 1, the fault is hidden.
- If two inputs are 0, the fault is hidden.
- If one input is 1 and the other is 0, one of them is hidden.

In Step 1-3 of Algorithm 2 (Page 6 of the revised manuscript), the localization rate is 100%. However, in Step 4-5, each suspicious TSV is re-enabled and checked again to confirm its correctness. In this phase, if the bridge defect is hidden, TSV-OCT will assume that the TSV is healthy. When we increase the T values, the chance of hidden faults is smaller and the TSV-OCT can determine it correctly.

In summary, we have validated that the proposed TSV-OCT could also work around TSV-to-TSV bridge defects. However, with the behavior shown in Figure A-3.14, we believe that we need to further investigate this particular type of defects. An optimized version of TSV-OCT might be needed to remove the aforementioned abnormal cases. Nevertheless, with a proper T values, the currently proposed TSV-OCT can localize TSV-to-TSV defects without any modifications.

Reviewer Point P 3.3 — The paper does not have any hardware results, which means all results are only for simulation not real chip. To convince the practicality of your technique, it is required to add at least PVT variations in the result section.

Reply: Although we provide hardware results in terms of area cost, timing and power consumption of the design in Table II, and we also have integration results in 3D-NoC in Table IV, we agree with the reviewer that these results are not based on real-chip testing.

We also agree with the reviewer that PVT simulations can provide different aspects on timing and potential defects; however, we would like to emphasize that our proposed method mainly focus on providing a non-blocking undegradable performance online testing by dealing with the defects at the logic level and enhancing the coding technique (PPC). Also, since our method is algorithm-based, it could be applied to different types of TSVs or even normal wires.

Due to the lack of time and budget for fabricating and testing a real-chip prototype, we could not further conduct the proper experiments in an accurate and timely way. However, we strongly believe that the reviewer's comment could actually open more possibility for extending our research in the future. Therefore, due to the importance of this comment, we modified the following passages in the revised manuscript to reflect these points:

At Section V.G "Discussion" in line 30-35, right column, page 12:

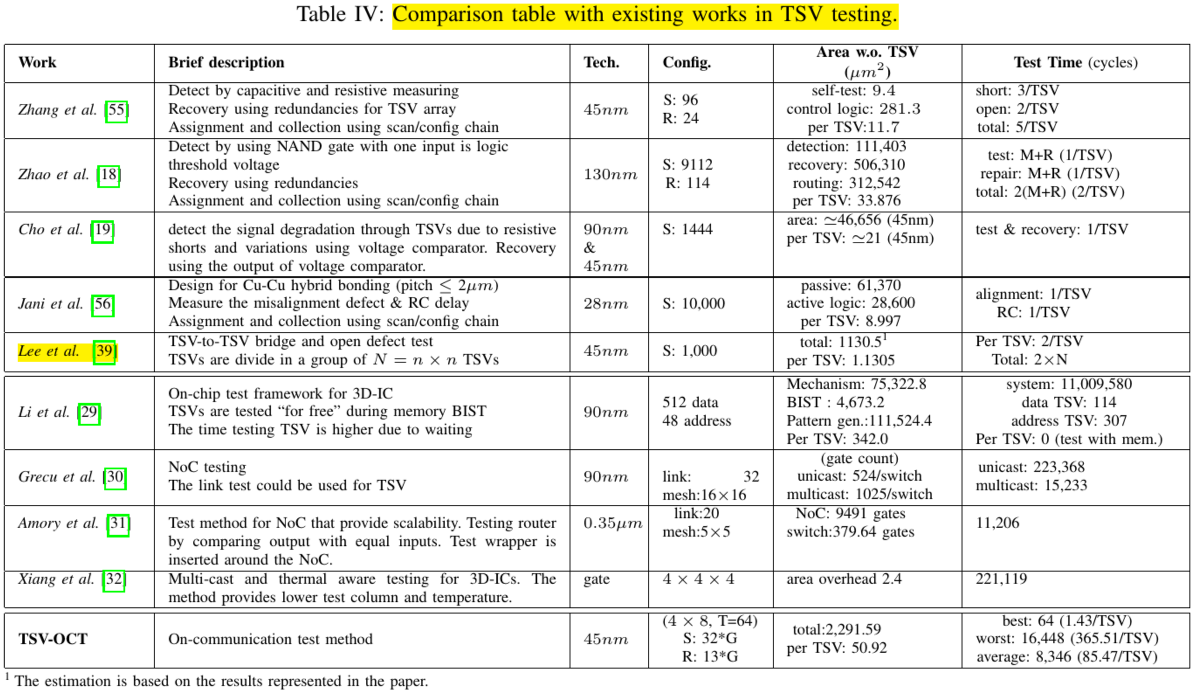
"Although this work has been evaluated and compared in detection and localization efficiencies, the impact of real-chip fabrication and Process Voltage Temperature (PVT) variations have not been studied. The PVT or real-chip measurement could provide more realistic result on the timing behavior of the circuit; however, theses variations have small impact on the efficiency of the algorithm. Nevertheless, PVT or real-chip measurement should be studied in the future to provide better understanding of our proposal."

At Section VI "Conclusion" in line 49-53 , left column, page 13:

"In depth analyses using PVT simulation and real-chip fabrications could provide different aspects on the efficiency of our method. Also, since TSV-OCT could work with different mediums, applying our proposal to normal wires or memories could also be a viable direction."

Reviewer Point P 3.4 — The hardware overhead of the proposed method is compared to prior papers using the area per TSV $(< i > um < /i >< sup > 2 < /sup >)$ in Table IV. This metric doesn't look a fair comparison, because most of the previous methods usually share their test circuits to test multiple TSVs. I recommend that the hardware size is compared to prior papers using the actual TSV numbers in 3D-ICs under conditions of the same number of TSVs.

Reply: We thank the review for this comment. In order to have a better comparison, we have significantly updated Table IV in the revised manuscript on page 13. We added the number of TSVs (signal and redundant) and further details on the testing time and area cost. A capture of Table IV could be seen in Figure A-3.15 of this document.



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Zhang et al. [55]	Detect by capacitive and resistive measuring Recovery using redundancies for TSV array Assignment and collection using scan/config chain	$45nm$	S: 96 R: 24	self-test: 9.4 control logic: 281.3 per TSV:11.7	short: 3/TSV open: 2/TSV total: 5/TSV
Zhao et al. [18]	Detect by using NAND gate with one input is logic threshold voltage Recovery using redundancies Assignment and collection using scan/config chain	$130nm$	S: 9112 R: 114	detection: 111,403 recovery: 506,310 routing: 312,542 per TSV: 33.876	test: M+R (1/TSV) repair: M+R (1/TSV) total: 2(M+R) (2/TSV)
Cho et al. [19]	detect the signal degradation through TSVs due to resistive shorts and variations using voltage comparator. Recovery using the output of voltage comparator.	$90nm$ & $45nm$	S: 1444	area: ≃46,656 (45nm) per TSV: ≃21 (45nm)	test & recovery: 1/TSV
Jani et al. [56]	Design for Cu-Cu hybrid bonding (pitch $\leq 2\mu m$) Measure the misalignment defect & RC delay Assignment and collection using scan/config chain	$28nm$	S: 10,000	passive: 61,370 active logic: 28,600 per TSV: 8.997	alignment: 1/TSV RC: 1/TSV
Lee et al. [39]	TSV-to-TSV bridge and open defect test TSVs are divide in a group of $N = n \times n$ TSVs	$45nm$	S: 1,000	total: 1130.5[1] per TSV: 1.1305	Per TSV: 2/TSV Total: 2×N
Li et al. [29]	On-chip test framework for 3D-IC TSVs are tested "for free" during memory BIST The time testing TSV is higher due to waiting	$90nm$	512 data 48 address	Mechanism: 75,322.8 BIST : 4,673.2 Pattern gen.:111,524.4 Per TSV: 342.0	system: 11,009,580 data TSV: 114 address TSV: 307 Per TSV: 0 (test with mem.)
Grecu et al. [30]	NoC testing The link test could be used for TSV	$90nm$	link: 32 mesh:16×16	(gate count) unicast: 524/switch multicast: 1025/switch	unicast: 223,368 multicast: 15,233
Amory et al. [31]	Test method for NoC that provide scalability. Testing router by comparing output with equal inputs. Test wrapper is inserted around the NoC.	$0.35\mu m$	link:20 mesh:5×5	NoC: 9491 gates switch:379.64 gates	11,206
Xiang et al. [32]	Multi-cast and thermal aware testing for 3D-ICs. The method provides lower test column and temperature.	gate	4 × 4 × 4	area overhead 2.4	221,119
TSV-OCT	On-communication test method	$45nm$	(4 × 8, T=64) S: 32*G R: 13*G	total:2,291.59 per TSV: 50.92	best: 64 (1.43/TSV) worst: 16,448 (365.51/TSV) average: 8,346 (85.47/TSV)

[1] The estimation is based on the results represented in the paper.

Figure A-3.15: New Table IV in the revised manuscript.

Reviewer Point P 3.5 — The test time of previous works has been omitted in Table IV, please fill out the blanks.

Reply: We took into consideration the reviewer's comments and updated Table IV with the testing time in the revised manuscript on page 13. A capture of Table IV was previously presented in Figure A-3.15.

Reviewer Point P 3.6 — The experimental results show that the TSV-OCT could not give any solid performance with more than 6 faults. Please calculate the probability of its inability to detect the defects (false negative and false positive) with considering the actual TSV defect rate.

Reply: We thank reviewer for this critical comment. We agree with the reviewer that TSV-OCT could not give any solid performance with more than 6 faults which might seem small. However, when taking into consideration the average practical defect rate, we believe that this amount is reasonable. According to reference [39] in the revised manuscript, the failure rate of TSV varies from 0.005% to 5%, and they assumed 0.5% for bridge defect during their simulation. In our case, we assumed the highest failure rate which is 5% for $N \times M$ (which has $(N+1) \times (M+1)$ TSVs):

$$\text{for 2x4 } : 1 \text{ defect} \tag{1}$$
$$\text{for 4x4 } : 2 \text{ defects} \tag{2}$$
$$\text{for 4x8 } : 3 \text{ defects} \tag{3}$$
$$\text{for 8x8 } : 5 \text{ defects} \tag{4}$$

These worst-case configurations still assume less than 6 defects. Based on the results in Figure 12, our method excluding *false positive* can successfully localize defects at a 5% rate with T=128. For smaller defect rates, we could use smaller T values. In our manuscript, we discuss this point in line 53, right column, page 9 to line 27, left column, page 10:

"Considering the realistic defect rate of TSVs, the rate could vary between 0.001% to 5% [39]. Here, we assume the defect rate is 5% where 8, 16, 32, and 64 data-bit have about 1, 2, 3, and 5 defects respectively. As shown in Figure 12, our method can cover 5 faults in all cases with T=128, which is enough to satisfy the assumed 5% maximum defect rate. Also, even the defects are not completely matched with lower T values, the system is still aware of the non-localized defects, as shown in Equation 3."

[39]: Y. Lee et al, "Grouping-Based TSV Test Architecture for Resistive Open and Bridge Defects in 3-D-ICs," IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, vol. 36, no.10, pp.1759-1763, 2017.

Reviewer Point P 3.7 — It is not clear why the illustration in Fig. 2 doesn't match the TSV region with 16 data bits, PPC (4×4). The row and column numbers start from 0, so it is supposed to be 5×5.

Reply: Figure 2 represents the TSV region for PPC (4×4) since the TSV region of PPC(NxM) is (N+1)x(M+1). We added an extra row and an extra column for checking purposes. PPC (4×4) has 16 data-bit and 25 codeword bit.

Minor

Reviewer Point P 3.8 — Minor correction:

1. The term “Figure” appears to be continuously intermixed with the “Fig. (abbreviation)”.
2. Typo: Page 11, Figure III is supposed to be the Table III.

Reply: We changed all instances of "Fig." to "Figure" in the revised manuscript. We also corrected Figure III to Table III. We thank the reviewer for pointing out these corrections.

Reviewer 4

Reviewer Point P 4.1 — It seems that the problem of TSV defects is oversimplified in the proposed solution. It is assumed that TSV defects are the source of just catastrophic faults and TSV faults are limited to stuck-at faults. While in practice, most of the TSV defects are parametric faults resulting in performance degradation such as propagation delay variation which are much harder than stuck-at faults to detect.

Reply: We thank the reviewer for this important comment. We totally agree that modeling to stuck-at faults cannot express the realistic behavior of defected TSVs. Therefore, we also consider the open/short defects and perform the corresponding evaluation.

For timing violations due to open defects, we discuss that in the hidden error effect section of the submitted manuscript (line 30-32, right column, page 4 in revised manuscript) as follows:

“If a timing violation occurs due to an open defect, sending the same value as the last transmitted value causes no errors, while sending a different value may cause a flipped bit.”

This is the situation that we model where an open defect creates a delay that shifts the signal after the hold-time. We understand that metastability could happen with timing violations. Therefore, to tolerate these violations, special circuits could be used (i.e. double latches). As the metastability resolves later, the output signal either becomes 0 or 1. Based on this value, we could use the ECC to detect and localize it.

Because of the open defect is modeled as "late", we could observe the same inconsistency as we model: (1) repeating the value on TSV does not cause fault; (2) changing the logic value causes fault.

To reflect the reviewer’s comment, we updated the evaluation part at page 8, left column, line 55-57:

“We use two fault models: (1) stuck-at-0 for short-to-substrate defects; and (2) delay value of one clock cycle for open defects. Because the data is randomly generated, the hidden fault probability is about 0.5 for both models.”

Also, we discussed about the metastability phenomenon at page 13, right column, line 24-29: “In our two fault models, we have not considered the metastability phenomenon. We assume that this phenomenon disappears after a certain time and the voltage falls to '0' or raises to '1'. To completely avoid this situation, metastability immune circuits could be used for TSVs which require double-latches."

Reviewer Point P 4.2 — The observability and controllability of a TSV has not been discussed in the paper and therefore it is difficult to evaluate how the data is applied to a TSV and how its response is observed. TSVs do not exist in isolation as Figure 2 and Figure 3 imply, they can be deeply embedded inside a chip. In the proposed methods, it is not clear how the fault of a TSV is isolated from the circuits connected to the TSV.

Reply: We would like to thank the reviewer for this important comment as it points out to a possible confusion in our explanation. About the observability and controllability of a TSV, we first clarify how a TSV is connected to the bits in Section II-A, page 3, left column, line 29-30: "One TSV handles the transmission of a bit in flit F."

$$F_k = \left[\begin{array}{cccccc} b_{0,0} & b_{0,1} & b_{0,2} & \dots & b_{0,N-1} & r_0 \\ b_{1,0} & b_{1,1} & b_{1,2} & \dots & b_{1,N-1} & r_1 \\ \multicolumn{6}{c}{\dotfill} \\ b_{M-1,0} & b_{M-1,1} & b_{M-1,2} & \dots & b_{M-1,N-1} & r_{M-1} \\ c_0 & c_1 & c_2 & \dots & c_{N-1} & u \end{array}\right]$$

and page 3, left column, line 46-47:
"where the bits $b_{i,j}$, c_j, r_i and u are taken from the corresponding TSVs."

For the "Isolation" method, here we want to emphasize that we meant a virtual isolation, not a physical one, since TSVs are already integrated. Specifically, *TSV-OCT* disconnects the isolated TSV from the ECC, which means that the isolated TSV's bit value is no longer taken into the parity encoder/decoder. During the "Isolation", the TSV is not physically isolated, and it in fact still transfers data flits as usual. This approach aims to achieve two main goals: (1) it never blocks and slows down any communication; (2) false positive cases have no impact on the performance because data flits are still being transferred.

To omit any confusion, we took into account the reviewer remark and updated the contributions part of the introduction at line 6-11, left column, page 3:
"It first virtually isolates the suspicious TSVs by disconnecting them from the encoding/decoding process to find more hidden defects. After no more defects are found, it re-attaches these TSVs back to the encoding/decoding to ensure the faulty status."

We also updated at line 29-31, right column, page 5:
"The system virtually isolates the *suspicious TSVs* from encoding/decoding process; but, they are still being used for data transaction."

Reviewer Point P 4.3 — If a TSV is considered an on-chip wire with just stuck-at fault defect model, commercial CAD tools can be used to generate tests and cover their faults. Integrated circuit are currently tested for stuck-at faults by commercial tools and solutions for this type of faults is considered mature. What is the motivation to develop a new testing method for on-chip interconnects?

Reply: We agree that CAD tools and existing BISTs have been mature enough to capture or prevent the defects of TSVs. However, as we discussed in the motivation behind of OCT, having an online and non-blocking test like TSV-OCT helps the system to monitor the health of TSVs during operation. Our method is in fact not just a testing method. It is first built on-top of a coding method that can correct transient errors. By using an enhanced algorithm, we provide the ability to detect the defects on TSVs.

Moreover, since aging affects the reliability and the quality of TSVs, capturing the new occurred defects is also important for highly reliable devices. The fault caused by stress or high temperature is also important to capture because it is difficult to troubleshot. To clarify this, we added to the following to the revised manuscript at line 38-42, right column, page 1 as follows: " Although commercial CAD tools and existing solution have become mature for defect localization and detection, having an online and non-blocking solution helps preventing expensive consequences of operating systems under faults."

Reviewer Point P 4.4 — While the topic of detecting two or more concurrent defects may be interesting for certain applications, how important the problem is for TSVs in 3D-ICs considering the fact that the defect detection for a single TSV is far from satisfactory.

Reply:

Regarding the reviewer's concern about the important of having two or more concurrent defects, reference [39] give some statistics about the defect rates of TSV. Considering the highest rate of 5% in [39], a PPC(8x8) (64 TSVs data, 81 TSVs in-total) should be able to work be able to work around 5 defected TSVs. Also, recent works have investigated the clustering defects where the defects occur in neighboring TSVs. As a result, having multiple defects in the same group could happen, and our motivation to localize them becomes more relevant and crucial.

One more thing to be mentioned is that the aging/wear-out is significantly caused by the temperature. Because the temperature of large chips and 3D-ICs are nonuniform, the higher average temperature could have more defects.

To reflect the reviewer's comments, we added the below discussion on multiple defects in the same group in line 55, right column, page 9 as follows:

"Considering the realistic defect rate of TSVs, the rate could vary between 0.001% to 5% [39]. Here, we assume the defect rate is 5% where 8, 16, 32, and 64 data-bit have about 1, 2, 3, and 5 defects respectively. As shown in Figure 12, our method can cover 5 faults in all cases with T=128, which is enough to satisfy the assumed 5% maximum defect rate. Also, even the defects are not completely matched with lower T values, the system is still aware of the non-localized defects, as shown in Equation 3."

[39]: Y. Lee et al, "Grouping-Based TSV Test Architecture for Resistive Open and Bridge Defects in 3-D-ICs," IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, vol. 36, no.10, pp.1759-1763, 2017.

Reviewer 5

Reviewer Point P 5.1 — p.6: In Fig.3, it says "only case (a) and (c) indicate two positions where a false positive case occurs," however, case (c) seems to identify the defect TSV correctly (true negative).

Reply: We thank the reviewer for pointing out this mistake. We have corrected the corresponding passage in the revised manuscript, Figure 4 at line 38-39, page 6 as follows:
"Due to the transmitted data values, only cases (a) and (c) indicate two positions as faulty where a false positive case occurs in (a)."

Reviewer Point P 5.2 — p.5 right l.57: in Step 1, the option for Statistical Detector should be given. Is it used with the greedy localization option?

Reply: Yes, we use *greedy localization*. The main reason is to capture as much as possible suspicious positions in the *Statistical Detector*. Because during the *Isolation and Check* the isolated TSV still transfers its data as usual, capturing more faults ensure that we can capture the hidden fault cases without interrupting data transaction. If *Statistical Detector* is only used and the fault rate is low, we believe that using *conservative localization* could be more efficient. Taking into consideration the reviewer's comment, we added the following sentences to Step 1 to clarify the option at line 25-27, right column, page 5:
"We use *Greedy localization* to catch as much as suspicious TSVs as possible. The *false positive* TSVs will be re-checked and corrected later."

Reviewer Point P 5.3 — p.6 left l.32: It is not clear what kind of the case is called "TSV region is detected as faulty". If a fault is localized by the method, is the TSV region not called as faulty?

Reply:

Here, we meant that if after the whole process, the TSV region is still faulty with an isolated position, there are some undetected faults. As we target real-time applications, the defect localization task must be constrained by time (number of cycles) instead of running endlessly. Therefore, there are possible missing faults after the localization task. The second situation is the number of faults being higher than the localization limitation (i.e, 7-8 defects) which leads *TSV-OCT* to fail localizing all defects. To ensure the awareness of the system, *TSV-OCT* informs it about this situation for a suitable reaction.

To clarify this point, we edited Step 5 as follows at line 42-45, right column, page 5:
"After Step 4, if the TSV region with isolated TSVs is still detected as faulty, there are unrecognizable faults by *Isolation and Check*. Here, we consider that the whole TSV region as faulty."

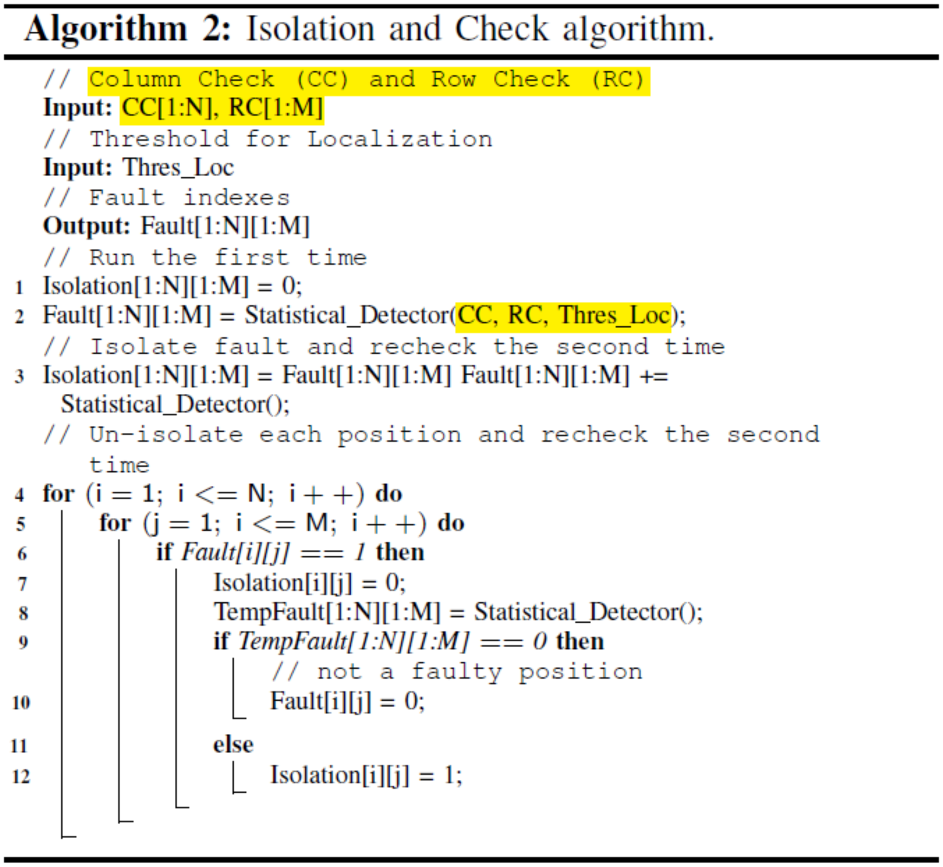
Reviewer Point P 5.4 — p.6: In Algorithm 2, it is not clear how the syndrome from the ECC is used. Symd and Thres_Loc never appear in the algorithm.

Reply: We thank the reviewer for suggesting this point. We agree that there is a missing link between the two algorithm in the submitted manuscript. $Symd$, the output of ECC, can be mapped from the column and row check (CC, RC): Symd[i][j] = 1 if CC[i] == RC[j] = 1. This information and Thres_Loc is used by the "Statistical Detector".

We updated Algorithm 2 at page 6 as follows:

- We replace Symd by CC and RC.
- We added CC, RC and Thres_Loc to the input of the "Statistical Detector".

Please see Figure A-5.16 of this document for the screen shot of the updated Algorithm 2 (page 8).



Algorithm 2: Isolation and Check algorithm.

```
// Column Check (CC) and Row Check (RC)
Input: CC[1:N], RC[1:M]
// Threshold for Localization
Input: Thres_Loc
// Fault indexes
Output: Fault[1:N][1:M]
// Run the first time
Isolation[1:N][1:M] = 0;
Fault[1:N][1:M] = Statistical_Detector(CC, RC, Thres_Loc);
// Isolate fault and recheck the second time
Isolation[1:N][1:M] = Fault[1:N][1:M] Fault[1:N][1:M] +=
  Statistical_Detector();
// Un-isolate each position and recheck the second
   time
for (i = 1; i <= N; i + +) do
    for (j = 1; i <= M; i + +) do
        if Fault[i][j] == 1 then
            Isolation[i][j] = 0;
            TempFault[1:N][1:M] = Statistical_Detector();
            if TempFault[1:N][1:M] == 0 then
                // not a faulty position
                Fault[i][j] = 0;
            else
                Isolation[i][j] = 1;
```

Figure A-5.16: Revised Algorithm 2.

Reviewer Point P 5.5 — p.8 left l42: ”With T = 128 and T = 8” the following results correspond only for T = 128 and not for T = 8.

Reply: We thank the reviewer for pointing out this mistake. In line 45, right column, page 8 of the revised manuscript, we made the following correction:

"With $T = 128$, the *Statistical Detect* localizes at least 45% of 6 faults, 99% of 3 faults and 100% of 2 faults."

Reviewer Point P 5.6 — p.9 right l.50: "With only T=8, it successfully detects less than 40% of the two defects." There are no such results in Fig. 11. Fig. 11 shows almost 100% detection can be achieved for two defects even with T=8.

Reply: We thank the reviewer for pointing out this mistake. We corrected "two defects" to "six defects" which could be observed in Fig.11. The new sentence is in line 42, right column, page 9:
"With only $T = 8$, it successfully detects less than 40% of the six defects."

Reviewer Point P 5.7 — p.11: The figures about the area cost may be mismatched with the tables.

Reply: We took into consideration the reviewer's comments and we change "Figure III" to "Table III" in the revised manuscript in page 11, right column, line 12.

Reviewer Point P 5.8 — p.11 left l.55: "8.66%" should be 8.34%.

Reply: We thank the reviewer for pointing out this mistake. We corrected 8.66% to 9.17% because we update the TSV area cost to $4.06\mu m \times 4.06\mu m$ in the revised manuscript on page 11, right column, line 18.

Reviewer Point P 5.9 — p.11 right l.30: "22.63% area overhead" I cannot understand where the number comes from.

Reply: This number illustrates the proposal's hardware overhead when compared to the previous work [53]. However, because this paragraph is about Table IV, we realize that comparing to previous work on NoC is not suitable nor fair. Therefore, in the revised manuscript we used instead the exact value of the proposed design's area in page 11, right column, line 52-53:

For a 32-bit design, the proposed TSV-OCT area is $50.92\mu m^2$ per TSV.

[53]: K. N. Dang et al., "A low-overhead soft–hard fault-tolerant architecture, design and management scheme for reliable high-performance many- core 3D-NoC systems," The Journal of Supercomputing, vol. 73, no. 6, pp. 2705–2729, Jun 2017.

Reviewer Point P 5.10 — Other typos:
p.5 right l.58: Theses → These
p.11 left l.50: Figure III → Table III

Reply:

We thank the reviewer for pointing out these typos. We have updated the revised manuscript as follows:

- Theses → These : We fixed this in page 5, right column, line 24.
- Figure III → Table III: We fixed this in page 11, right column, line 12.