On-Chip Communication Fault-Resilient Adaptive Architectures and Algorithms for 3D-IC Technologies

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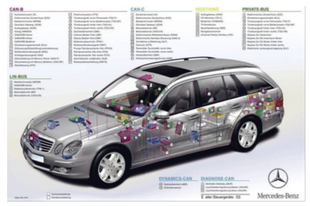
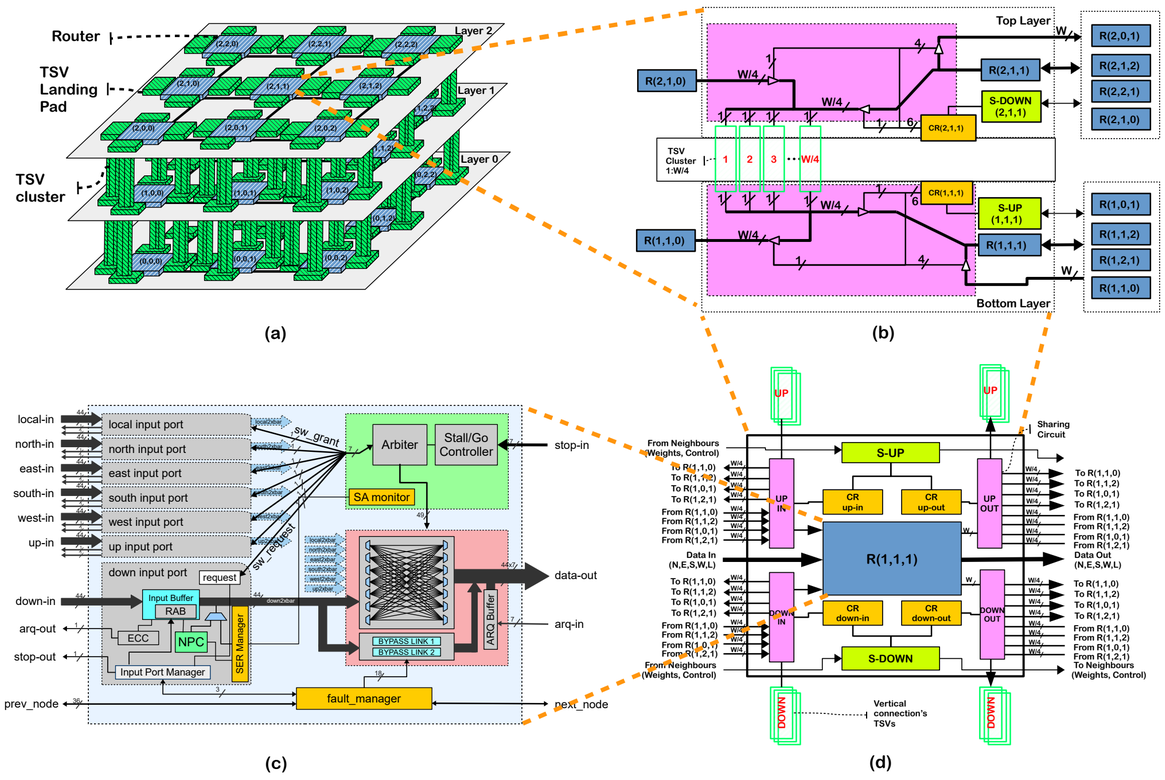
Era of Many-core Chips

Hundreds of cores integrated on chip:

- Technology scaling.
- 3D integration.
- Several examples:
  - STMicro P2012/STHORM
  - picoChip
  - Scale-out
  - Tilera Tile GX, Tile Pro
  - Intel Polari
- Complex apps, stringent constraints:
  - Massively parallel applications
  - Performance, power, scalability, reliability are key challenges.



3D Network-on-Chip

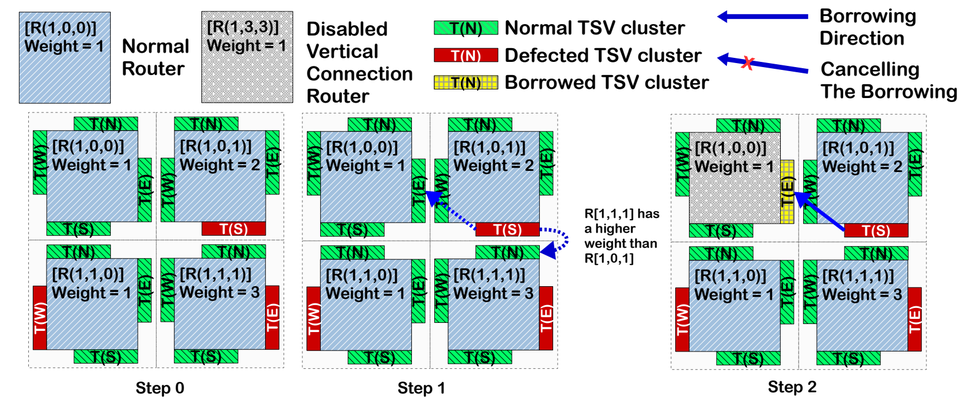


System architecture: (a) Network; (b) Vertical connection; (c) Router; (d) Wrapped router.

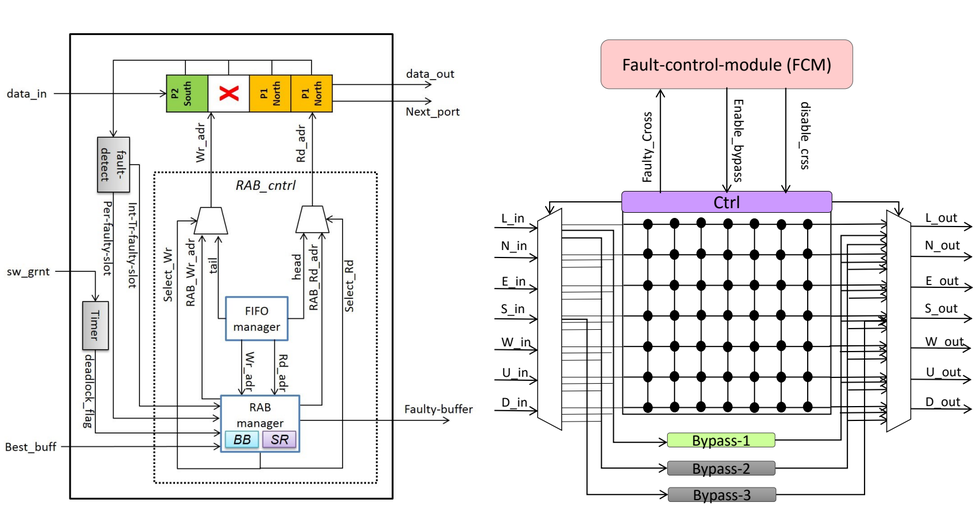
Reliability Demand

- NoCs are exposed to a variety of manufacturing and design factors making them vulnerable to different faults that cause corrupted message transfer or even catastrophic system failures.
- The single-point-failure nature of NoC introduces a big concern to their reliability as they are the sole communication medium.
- Several works have dealt with separated types of faults; however, there is a demand of a comprehensively reliable 3D NoC system which can handle soft errors, hard faults and TSV defects.

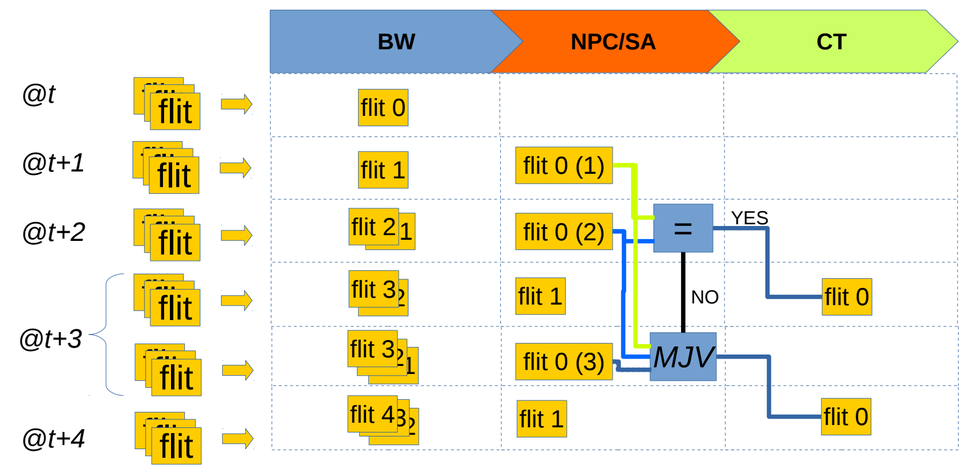
Technology Features



TSV Sharing Process.



Hard Fault Tolerance: (a) Random Access Buffer; (b) Bypass-Link-on-Demand.



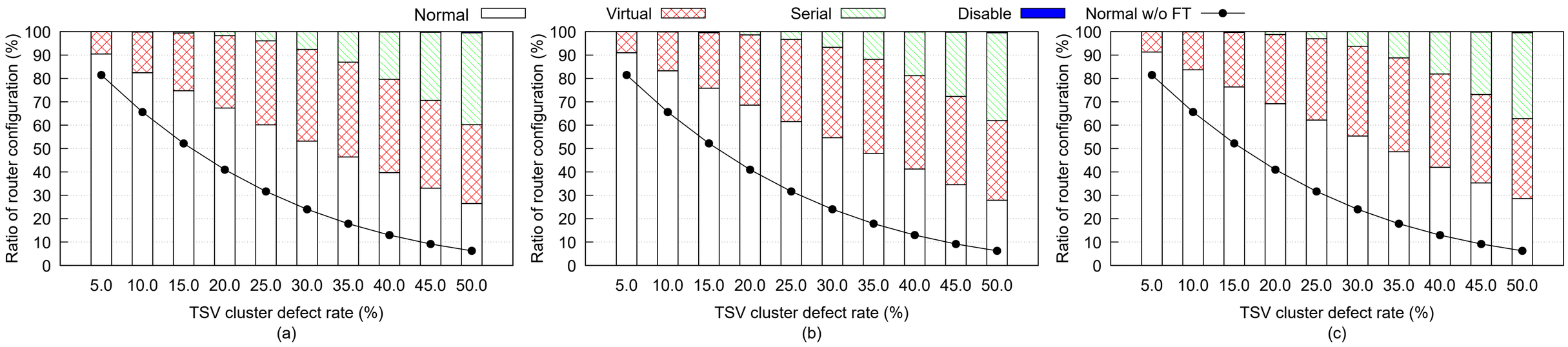
Soft Error Tolerance: Pipeline Computation Redundancy.

References

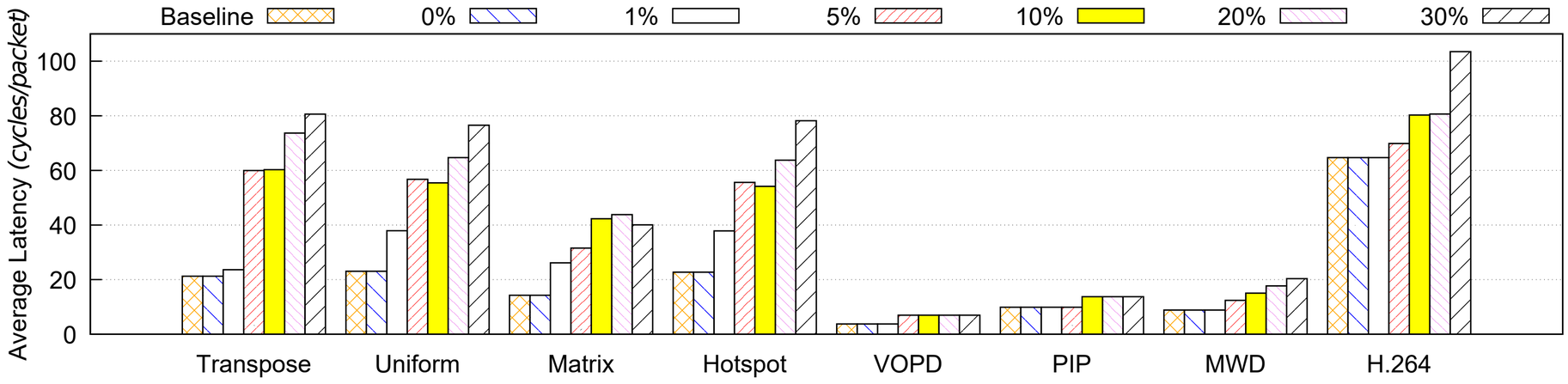
[1] Dang Nam Khanh: *Development of On-Chip Communication Fault-Resilient Adaptive Architectures and Algorithms for 3D-IC Technologies*, Doctoral Thesis, The University of Aizu, 2017.

[2] Akram Ben Ahmed: *High-throughput Architecture and Routing Algorithms Towards the Design of Reliable Mesh-based Many-Core Network-on-Chip Systems*, Doctoral Thesis, The University of Aizu, 2015.

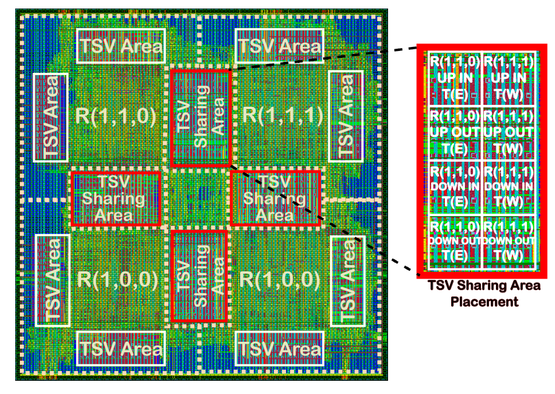
Result: Reliability, Performance and Layout



Reliability evaluation. Layer size: (a) 16 × 16; (b) 32 × 32; (c) 64 × 64.



Performance evaluation.



Layout of a 2 × 2 layer.