Low-Power Spiking Neural Network with Clock-gating technique

S1290033

Rui Shiota

Content

- Research Introduction
- FPGA Demonstration of SNN
- Research progress
  - Done
  - Doing
  - Todo
- Schedule

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Research introduction

- My research is about clock gating in LIF neuron.
- My goal is to reduce power consumption.

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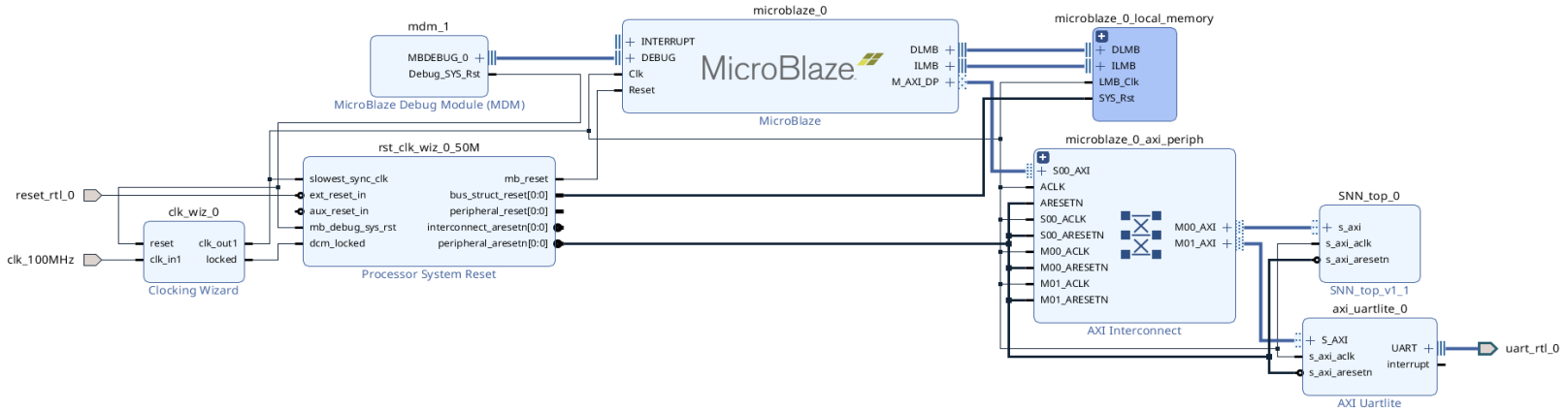
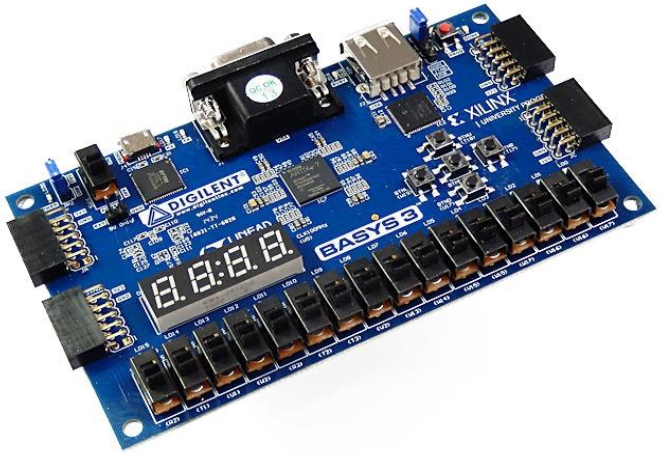
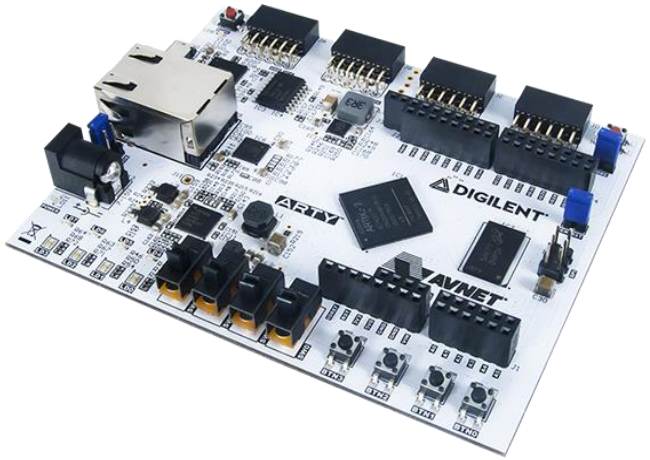
FPGA Demonstration of SNN







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Research Progress | Done

- Implementation of clock gating
- Tutorial of PyTorch and snnTorch

Research Progress | Doing

- Modification of poster
- FPGA Demonstration

Research Progress | Todo

- Preparation for RPR and RPS

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Schedule

Task	Deadline
Modification of poster	November 5
FPGA Demonstration	November 5
RPR	November 6
RPS	November 8

Thank you for your attention!