

Low-Power Spiking Neural Network with Clock-gating technique

Rui Shiota

S1290033@u-aizu.ac.jp

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- Research Introduction
- LIF neuron
- Clock gating
- Research progress
- Schedule

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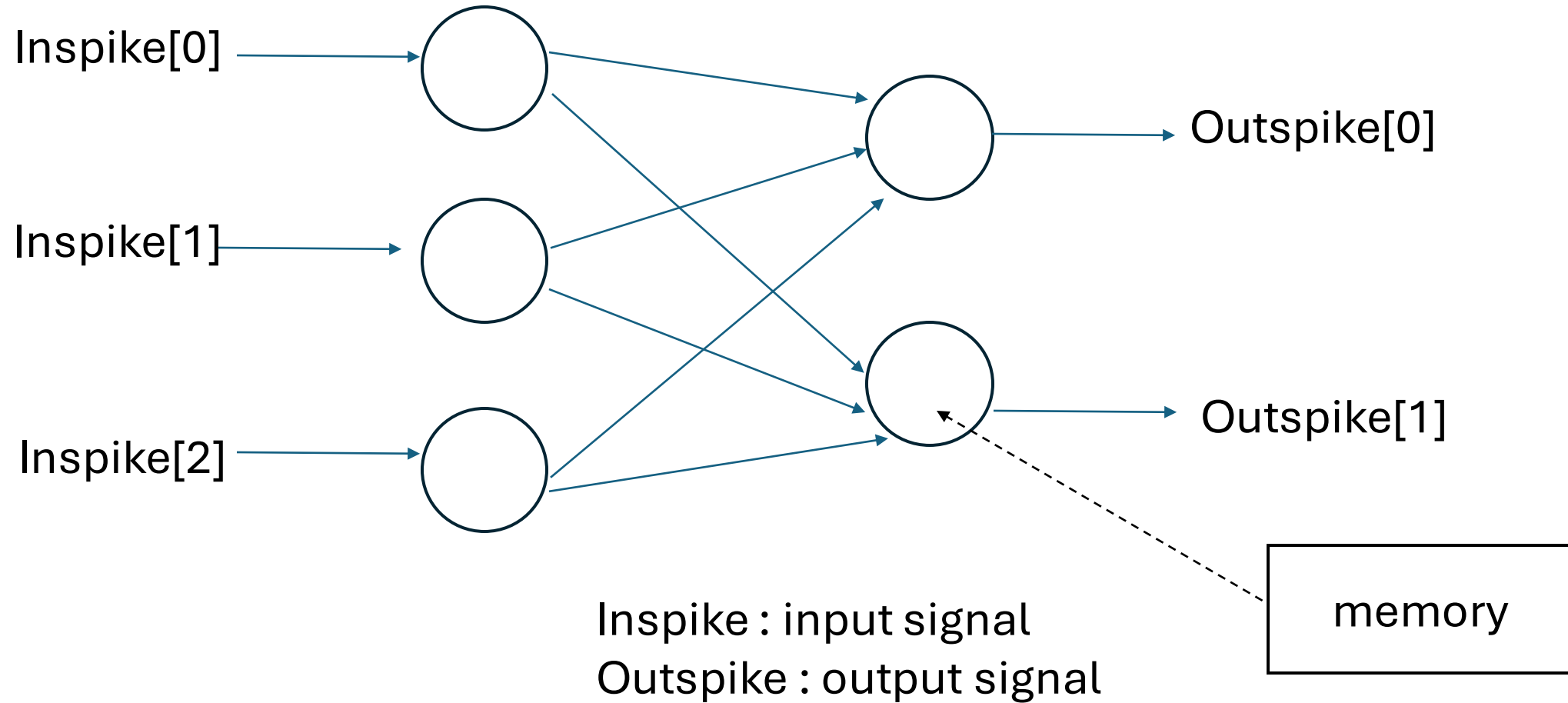
Research introduction

- My research is about clock gating in LIF neuron.
- My goal is to reduce power consumption.

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LIF neuron (1)

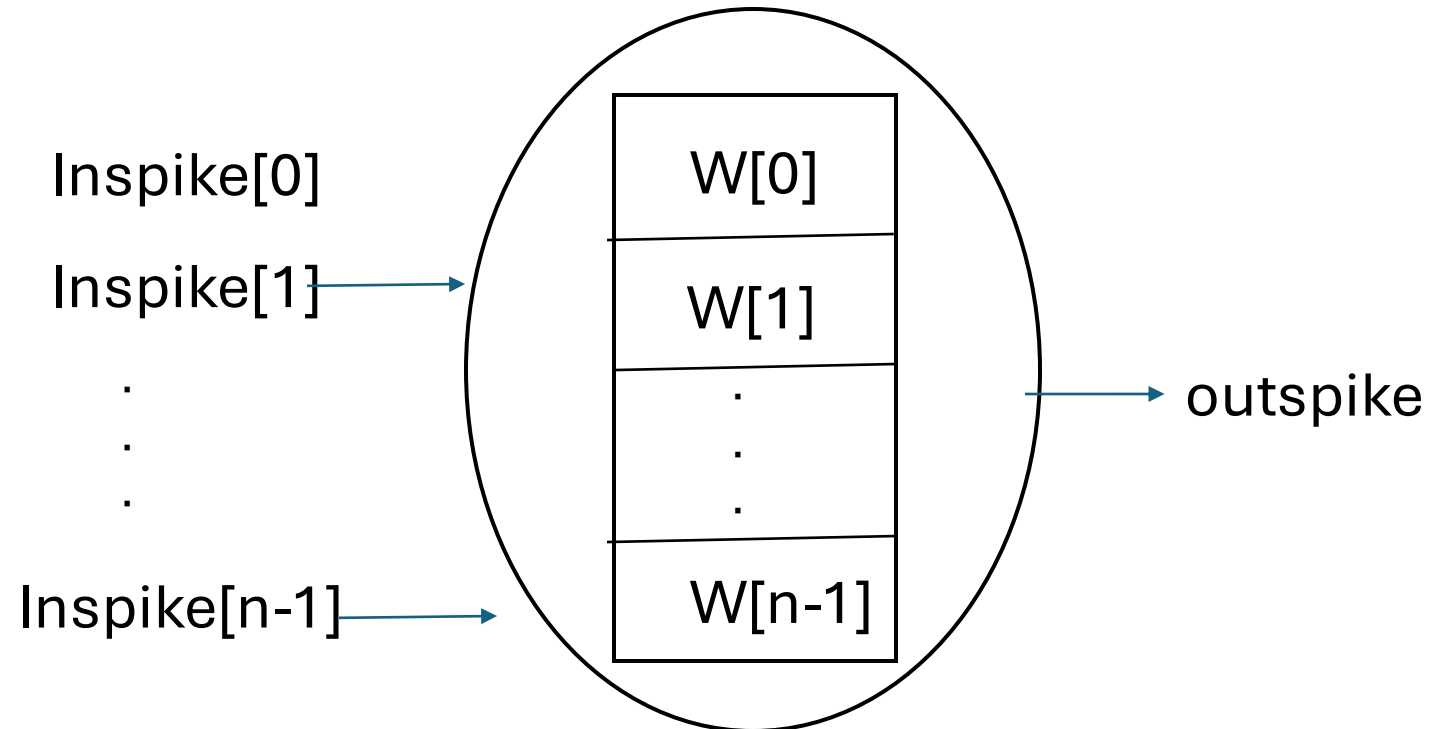


LIF neuron (2)

```
V = 0;  
for (i = 0 ; i < n ; i++)  
    V = V + inspike[i] * w[i] ;
```

```
if (V >= Vth)  
    outspike = 1 ;  
else  
    outspike = 0;
```

n : the width of inspike
Vth : threshold voltage
w : weight

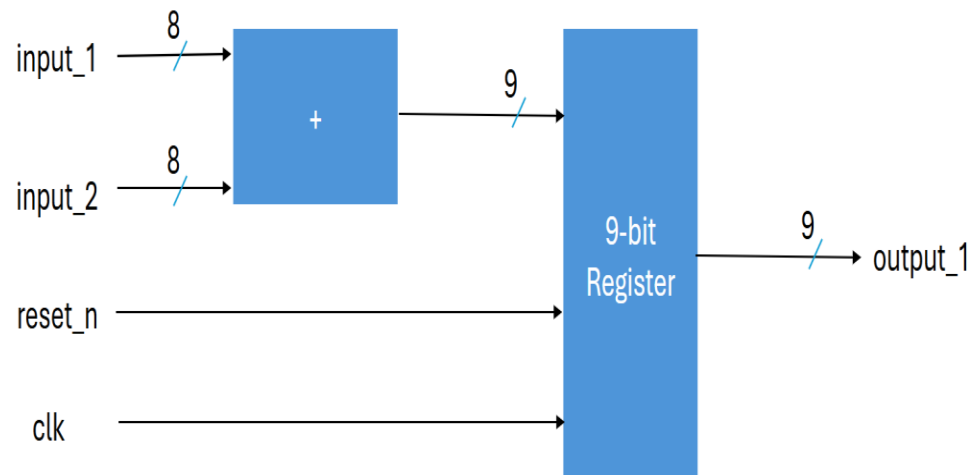


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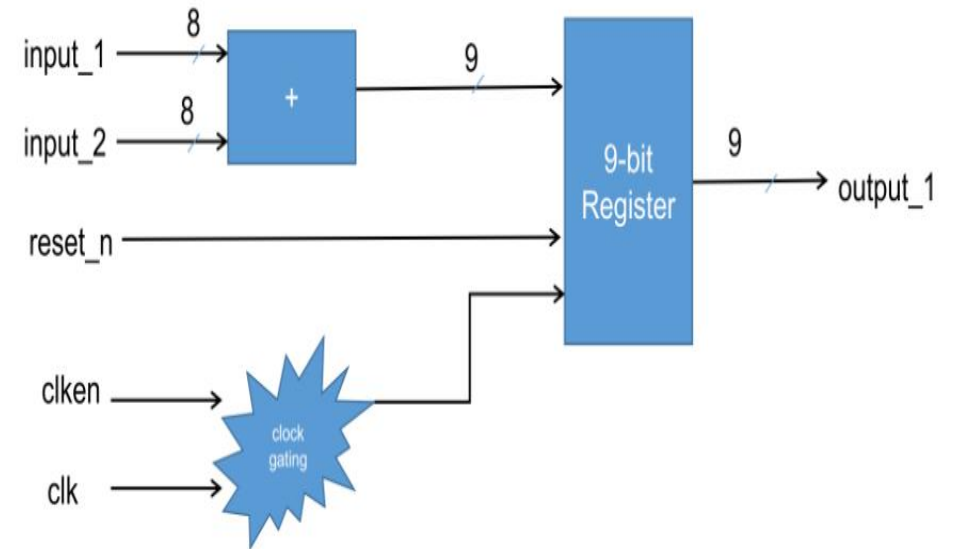
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Clock gating (1)

conventional (non-clock-gated) system



clock gated system



Clock gating (2)

Dynamic Power = Internal Power + Switching Power

conventional (non-clock-gated) system

	Int	Switch	Leak	Total	
48	Power	Power	Power	Power	%
49 Hierarchy					
50 -----					
51 conventional	6.82e-06	2.25e-07	1.39e-06	8.44e-06	100.0
52 Register (Register_IN_WIDTH9_OUT_WIDTH9)					
53	6.72e-06	9.83e-08	9.49e-07	7.76e-06	92.0
54 Adder (Adder_IN_WIDTH8_OUT_WIDTH9)	1.01e-07	1.26e-07	4.45e-07	6.72e-07	8.0
55 add_12 (Adder_IN_WIDTH8_OUT_WIDTH9_DW01_add_0)					
56	1.01e-07	1.26e-07	4.45e-07	6.72e-07	8.0
57					

Dynamic Power : 7.045e-06

clock gated system

	Int	Switch	Leak	Total	
48	Power	Power	Power	Power	%
49 Hierarchy					
50 -----					
51 clock_gated	1.37e-06	4.56e-07	1.43e-06	3.26e-06	100.0
52 clkgx (clkgx)	8.87e-08	2.43e-07	2.54e-08	3.57e-07	11.0
53 Register (Register_IN_WIDTH9_OUT_WIDTH9)					
54	1.18e-06	8.67e-08	9.59e-07	2.23e-06	68.4
55 Adder (Adder_IN_WIDTH8_OUT_WIDTH9)	1.01e-07	1.26e-07	4.45e-07	6.72e-07	20.6
56 add_12 (Adder_IN_WIDTH8_OUT_WIDTH9_DW01_add_0)					
57	1.01e-07	1.26e-07	4.45e-07	6.72e-07	20.6
58					

Dynamic Power : 1.826e-06

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Research Progress

- Coding in verilog hdl
- RTL simulation
- Synthesis
- Post-synthesis simulation
- Power estimation
- Implementing a clock-gated system

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[illegible]

Thank you for your attention!