UNIVERSITY OF NEW BRUNSWICK - FREDERICTON
DEPARTMENT OF ELECTRICAL AND COMPUTER ENGINEERING

ECE3221 Computer Organization

R.Tervo Version 1.45

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Hardware Reference Guide

Introduction

For the ECE3221 labs, a customized *NIOS-II* processor is configured on an *Altera Cyclone II* FPGA found on an *Altera DE2 Development Board*. This DE2 board is the same one used in ECE2213 and in many other courses at UNB and at universities around the world.

The NIOS-II processor is a full featured 32-bit processor provided by Altera. Its architecture and circuit behaviour are completely specified in Verilog HDL [c.f. VHDL] and a special configuration of this processor has been developed in the ECE3221 labs. Consequently there may at times be slight variations between the processor used in the lab and the generic NIOS-II documentation found on the Altera website. Specifically, various onboard I/O devices have been specially designed and configured for ECE3221 labs. In any case, you need only to load the supplied processor file and setup the FPGA once at the beginning of each lab day.

The DE2 board is connected to a workstation through a USB cable. The supplied software used for the ECE3221 labs includes the *Altera Quartus II* program to load and install the processor and the *Altera Monitor Program* to program and to control the processor.

This document describes the customized peripherals connected to the NIOS-II processor as installed in the ECE3221 lab.

Both newer (DE2-115) and older (DE2) Altera FPGA boards may be found in the ECE3221 lab. This document refers to both as "DE2" and any minor differences are noted. The default configuration assumes the DE2-115 board.

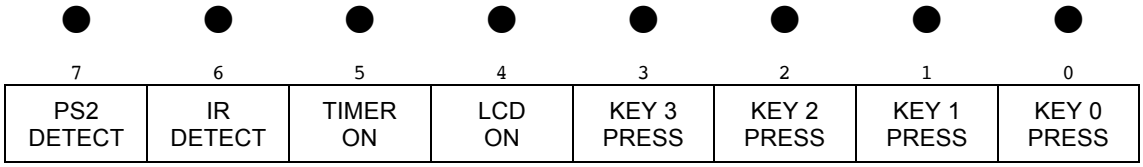
BE SURE TO USE ONLY THE MOST RECENT VERSION OF THIS DOCUMENT

The custom ECE3221 processor is under development and the available peripherals and their details may change from time to time and this document will be updated accordingly.

Raising toggle switch SW16 will produce a hardware version message on the LCD screen.

System Status Display (default)

The eight green LEDs (LEDG7…LEDG0) located above the pushbuttons serve as system status indicators. These LEDs serve to confirm correct operation of the ECE3221 computer.



BITS	LABEL	DESCRIPTION
7	PS2 DETECT	Flashes when activity is detected at the PS2 connector clock (CLK) line. Normally OFF.
6	IR DETECT	Flashes when a modulated infrared (IR) signal is detected at the onboard sensor. Normally OFF.
5	TIMER ON	Directly connected to timer control register bit TIMER ON If this LED is OFF the timer is inoperative.
4	LCD ON	Directly connected to LCD display register bit LCD ON If this LED if OFF the LCD display is inoperative.
3..0	KEY3..KEY0	Directly connected to pushbuttons KEY3..KEY0 If an LED is OFF, the corresponding pushbutton is pressed.

Eight Green LEDs (optional)

The above assignments can be disabled using a bit in the I/O Control Register. In that case, these LEDs can be controlled directly using an output port as described below.

Toggle Switches SW16 and SW17

These toggle switches must be in the closed (down) position in normal operation. The corresponding red LEDs will flash if either of these switches is open (up).

SW17 – shows a test pattern on the red 7-segment displays. Any previous contents on the displays are not lost when the switch is closed.

SW16 – shows hardware version information in the LCD screen. Any previous text on the screen is overwritten.

I/O Port Map

The available I/O devices are described on the following pages. The individual pins for each input and output port are shown in detail, where 'x' indicates a *don't care* condition. Unless otherwise indicated output ports are "write only" and it would not be possible to read back the current value of an output port. Exceptions include the I/O Control Registers (*) below.

The address and external connections for each I/O port are summarized below:

I/O PORT ADDRESS	I/O TYPE	CONFIGURATION	CONNECTION
0x00008840	INPUT/OUTPUT	Debug Monitor Window	JTAG UART
0x00008850	INPUT	Toggle Switches	SW15..SW0
0x00008860	INPUT	Blue Pushbuttons	KEY3..KEY0
0x00008870	INPUT	Decade Timer	Internal timing circuit
0x00008880	OUTPUT	Red LEDs	LEDR15..LEDR0
0x00008890	OUTPUT	Other LEDs	LEDG7..LEDG0
0x000088A0	OUTPUT	Hex Displays	HEX7..HEX0
0x000088B0	OUTPUT*	Hex Control Register	HEX7..HEX0 control
0x000088C0	OUTPUT	LCD Control	2 x 16 LCD display
0x000088D0	INPUT	Infrared Detector	IRDA Rx
0x000088E0	OUTPUT*	I/O Control Register	Internal circuits
0x000088F0	INPUT/OUTPUT	PS2 Serial Data/Clock	PS2 Connector
0x00008900	CONFIGURABLE	External I/O Port PA	UNB Expansion Board attached to the **JP5** Connector (**JP2** for DE2)
0x00008910	CONFIGURABLE	External I/O Port PB	
0x00008920	CONFIGURABLE	External I/O Port PC	
0x00008930	CONFIGURABLE	External I/O Port PD	
0x000089A0	CONFIGURABLE	External I/O Port PX	**JP4** (DE2-115 only)

Interrupt Configuration

Input pins on the following ports are configured to generate interrupts (edge sensitive) if the corresponding bit in the interrupt mask register is 1. Any write operation to the interrupt pending register clears all the bits on that port.

INT #	DEVICE
2	Decade Timer
3	Pushbuttons
4	Switches
5	External I/O Port PA (JP2)
6	External I/O Port PB (JP2)
7	External I/O Port PC (JP2)
8	External I/O Port PD (JP2)
9	PS2 Connector
10	Codec Status
11	External I/O Port PX (JP4)
16	JTAG UART (see documentation)

ADDRESS (hex)	SIZE (bits)	Read/Write	COMMENTS
BASE+8	8 or 16	R/W	Interrupt mask register
BASE+12	8 or 16	R/W	Interrupt pending register

Toggle Switches (16 switches)

The sixteen toggle switches are directly connected to this input port as shown below. Each bit is 1 when the corresponding switch is in the up position.

ADDRESS (hex)	SIZE (bits)	I/O	COMMENTS
00008850	16	INPUT	Switch UP = 1

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SW15	SW14	SW13	SW12	SW11	SW10	SW9	SW8	SW7	SW6	SW5	SW4	SW3	SW2	SW1	SW0

Pushbuttons (4 keys)

The four blue pushbuttons are directly connected to this input port as shown below. Each bit is 0 when the corresponding button is pressed.

ADDRESS (hex)	SIZE (bits)	I/O	COMMENTS
00008860	16	INPUT	Key Pressed = 0

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
X	X	X	X	X	X	X	X	X	X	X	X	KEY 3	KEY 2	KEY 1	KEY 0

Red LEDs (16)

The sixteen red LED's are directly connected to this output port as shown below. Each LED is ON when the corresponding bit is 1.

ADDRESS (hex)	SIZE (bits)	I/O	COMMENTS
00008880	16	OUTPUT	1 = LED ON

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
LEDR 15	LEDR 14	LEDR 13	LEDR 12	LEDR 11	LEDR 10	LEDR 9	LEDR 8	LEDR 7	LEDR 6	LEDR 5	LEDR 4	LEDR 3	LEDR 2	LEDR 1	LEDR 0

Other LEDs (4 + 8)

Other LED's on the DE2 board and on the UNB Expansion Board can be controlled directly from this output port as shown below. Each LED is ON when the corresponding bit is 1.

ADDRESS (hex)	SIZE (bits)	I/O	COMMENTS
00008890	16	OUTPUT	1 = LED ON

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
X	X	X	X	LED 40	LED 39	LED 38	LED 37	LEDG 7	LEDG 6	LEDG 5	LEDG 4	LEDG 3	LEDG 2	LEDG 1	LEDG 0
				FOUR LEDS ON THE UNB EXPANSION BOARD JP2/5				EIGHT GREEN LEDS ON THE DE2 BOARD – SEE BELOW							

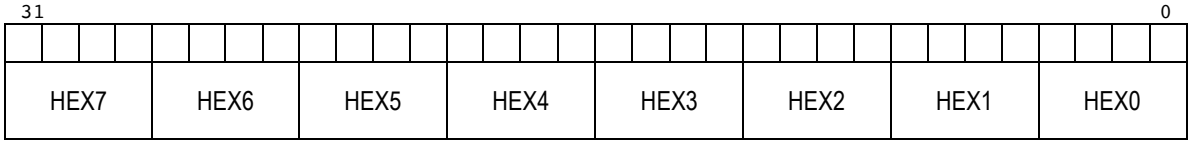
The eight green LED's on the DE2 board are accessible only when the display control bit is set in the I/O Control Register. The default I/O Control Register setting is OFF and these eight LEDs are normally configured as pre-assigned system status indicators.

The four LED's on the UNB expansion board are available only when this custom board is properly attached to the DE2 system on connector JP5 (or JP2 on the DE2).

Hexadecimal Display (8 digits)

The eight 7-segment red LED displays on the DE2 board are configured to show hexadecimal digits when each is supplied with a corresponding 4-digit value. Individual digits or the entire display can be turned on and off using bits in the control register (default is OFF). An alternate set of 7-segment patterns for 4-bit input values can also be selected in the control register.

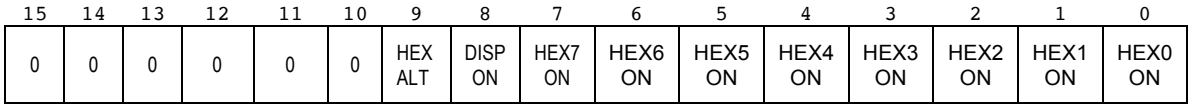
ADDRESS (hex)	SIZE (bits)	I/O	COMMENTS
000088A0	32	OUTPUT	See Hex Control Register



The default is all bits zero, all displays show digit 0000 = zero.

Hexadecimal Display Control Register

ADDRESS (hex)	SIZE (bits)	I/O	COMMENTS
000088B0	16	OUTPUT	Controls Hex Display



BITS	LABEL	DESCRIPTION
15..10	0	Must be zero at all times
9	HEX ALT	Selects an alternative set of 7-segment display patterns for the binary inputs 0000..1111. Normally this bit is always 0.
8	DISP ON	Switch ON and OFF the 8-digit hex display (1= ON) When ON, individual digits must be separately enabled (bits 7..0)
7..0	HEX7..HEX0 ON	Enable individual HEXn displays (1= ON) Display (bit 8) must be ON to see these digits.

The default is all bits zero, all hex displays OFF

Decade Timer (8 bits)

This device generates squarewaves with periods varying in multiples of ten from 10^{-5} sec to 100 sec. The signals are derived directly from the 50 MHz system clock. Each of these signals can be directly observed on this port as shown below. This port is active only when the corresponding bit is set in the I/O control register; the default control bit setting is OFF.

ADDRESS (hex)	SIZE (bits)	I/O	COMMENTS
00008870	8	INPUT	See Control Register

7	6	5	4	3	2	1	0
100 s	10 s	1 s	100 ms	10 ms	1 ms	100 µs	10 µs

These same pins may also be labeled with the fundamental frequency of each signal, as:

7	6	5	4	3	2	1	0
0.01 Hz	0.1 Hz	1 Hz	10 Hz	100 Hz	1 kHz	10 kHz	100 kHz

I/O Control Register

ADDRESS (hex)	SIZE (bits)	I/O	COMMENTS
000088E0	8	OUTPUT	I/O Device Control

7	6	5	4	3	2	1	0
X	x	x	x	JP2 BLINK	X	GREEN LEDS	TIMER ON

BITS	LABEL	DESCRIPTION
7..4	x	Unused
3	JP2/5 BLINK	Expansion Board LEDS controlled by the Green LED output port. 0 = Blink when the LEDs are off. (default) 1 = No blinking.
2	x	
1	GREEN LEDS	Sets display mode of the eight green LEDS on the DE2 board. 0 = The LEDS serve as system status indicators (default) 1 = The LEDS are controlled by the Green LED output port.
0	TIMER ON	Stops and starts the decade timer (1= OFF) Must be 0 for the decade timer to operate normally (default).

The default is all bits zero, decade timer ON and green LEDs showing status indicators

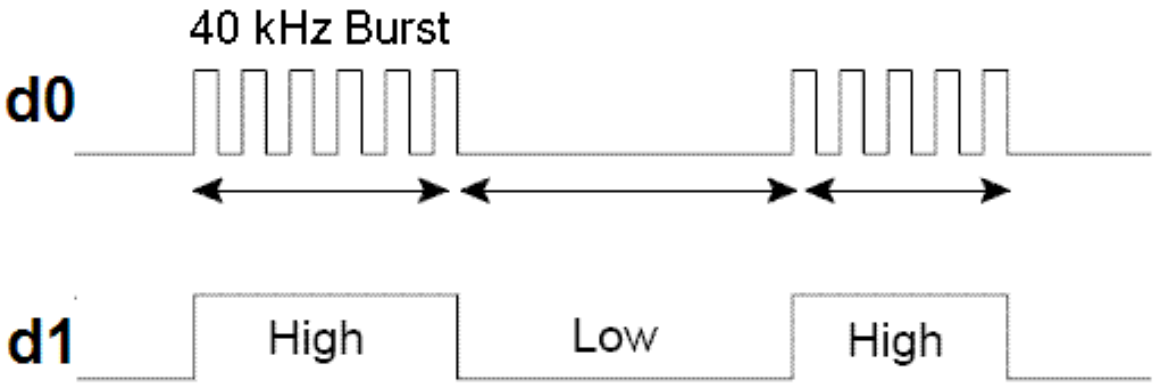
Infrared Signal Detector

The DE2 board includes a sensitive infrared (IR) light sensor labeled IRDA and located on the right hand edge near the gold connector. This input may be used to monitor the modulated IR signal emitted by a handheld remote control. *Whenever an IR signal is present at the sensor, a green status LED (LEDG6) flashes.*

ADDRESS (hex)	SIZE (bits)	I/O	COMMENTS
000088D0	8	INPUT	Reads IR Detector

7	6	5	4	3	2	1	0
x	x	x	x	x	x	IR DETECT	IR SIGNAL

BITS	LABEL	DESCRIPTION
7..2	x	Unused
1	IR DETECT	The bit is 1 whenever a modulated IR light source is present. Specifically, if the received IR signal is modulated at 40 kHz, this bit remains high as long as the signal is present.
0	IR SIGNAL	The bit is 1 whenever an IR light source is present. Specifically, if the received IR signal is modulated at 40 kHz, this bit changes at 40 kHz as long as the signal is present.



PS2 Communications

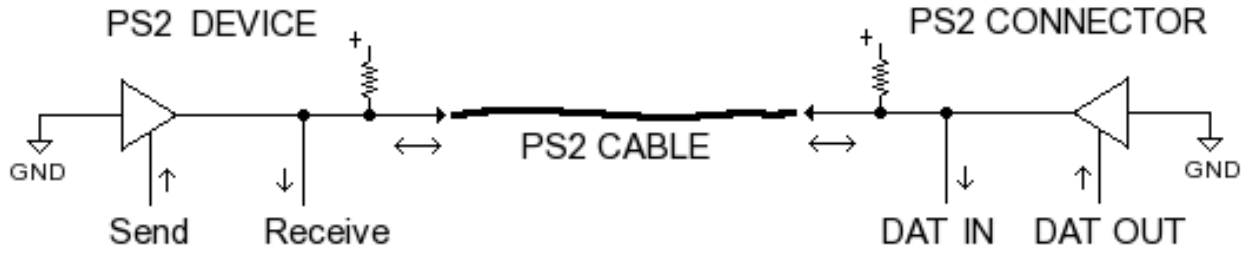
The DE2 board includes a standard PS2 connector as may be used to communicate with a standard keyboard or mouse on many (older) computers. *Whenever any activity is present at the PS2 clock (CLK) pin, a green status LED (LEDG7) flashes.*

ADDRESS (hex)	SIZE (bits)	I/O	COMMENTS
000088F0	8	MIXED	PS2 Clock/Data Lines

7	6	5	4	3	2	1	0
x	x	x	x	CLK OUT	DAT OUT	CLK IN	DAT IN

BITS	LABEL	DESCRIPTION
7..4	x	Unused
3	CLK OUT	Writing a 1 to this bit forces the PS2 clock line (CLK IN) low, while sending data to an external PS2 device. Normally, this bit is held at 0 when receiving data from a PS2 device. Default = 0.
2	DAT OUT	Writing a 1 to this bit forces the PS2 data line (DAT IN) low while sending data to an external PS2 device. Normally, this bit is held at 0 when receiving data from a PS2 device. Default = 0.
1	CLK IN	Reads the value present on the PS2 clock line (CLK), supplying a timing reference for data bits sent/received by a PS2 device.
0	DAT IN	Reads the value present on the PS2 data line (DAT), supplying serial data bits sent/received by an external PS2 device.

The PS2 connector uses a single line to send and to receive bits from an external device as shown below for the data (DAT) line. An identical circuit is used for the clock (CLK) line. This line is configured for bidirectional communications using an *open collector* approach. In this configuration, the data line is held high by pull-up resistors as long as both tri-state gates are not enabled. To send data, the circuit at either end can switch the line from 1 to 0 by enabling a tri-state gate. In particular, DAT OUT must be zero while data is being received at DAT IN.

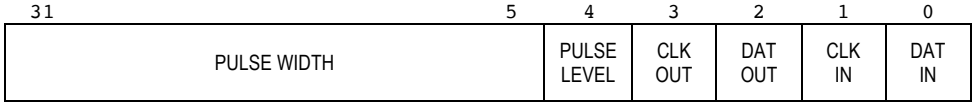


Note that when the output bits (CLK OUT / DATA OUT) are set to 1 the tri-state gate is enabled and the PS2 line goes low. Consequently, *binary values on the CLK OUT or DAT OUT bits are inverted when sent from the NIOS-II computer.*

PS2 Communications (As used for the Barcode Reader)

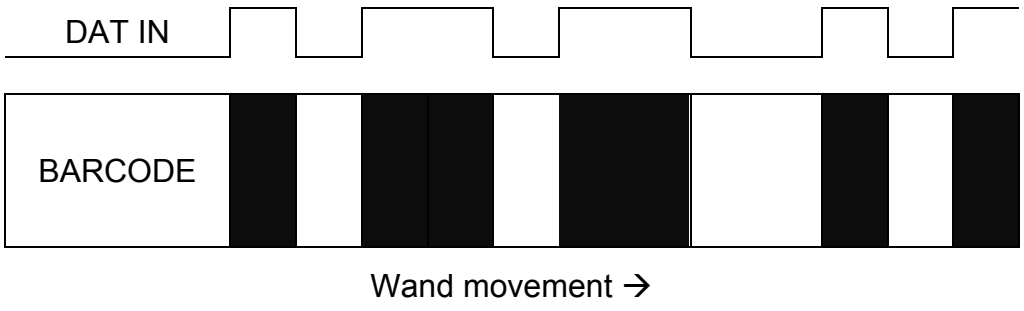
The PS2 port is also configured to measure the duration of a 1 or 0 state on the PS2 DAT IN line. This feature allows the PS2 DAT IN pin to be used by a barcode wand, in which case the level duration reflects the width of a barcode element (white or black bar) as the wand is passed across a barcode.[1] No special port configuration is required; however the DAT OUT bit must be set to 0 (default) to ensure that the open-collector DAT IN line is functional.

ADDRESS (hex)	SIZE (bits)	I/O	COMMENTS
000088F0	32	INPUT	PS2 Barcode Reader



BITS	LABEL	DESCRIPTION
31 .. 5	PULSE WIDTH	Duration of the most recent DAT IN state. (27 bits x 2 μ sec)
4	PULSE LEVEL	DAT IN state (on/off) measured for the pulse duration.
3	CLK OUT	Not used
2	DAT OUT	Must be 0 (default) to read barcode levels on DAT IN
1	CLK IN	Not used
0	DAT IN	The state (black/white) of the barcode wand input.

The barcode wand returns a high/low level as it passed over the black and white bars as shown below. The duration of each DAT IN level (on or off) is determined by the bar width and the speed at which the wand is moved by hand across the barcode.



[1] The barcode wand is in no way a standard PS2 device; however, the PS2 DAT IN pin provides a convenient means to attach the barcode wand to the DE2 boards in the ECE3221 lab.

LCD Display (2x16 characters)

The LCD display is controlled from this register by specifying 9-bits (8..0) to enter various command codes (such as 'clear display') or to display 8-bit character codes (ASCII).

ADDRESS (hex)	SIZE (bits)	I/O	COMMENTS
000088C0	16	OUTPUT	Controls LCD Display

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
X	x	x	x	x	LCD ON	EN	CMD	8-BIT DATA							

BITS	LABEL	DESCRIPTION
15..11	x	Unused
10	LCD ON	Turn the LCD display on and off (1= ON) Must be 1 at all times during normal operation
9	EN	Pulse input ON & OFF to input data bits (8..0) Pulse ON is typically >1 msec in duration.
8	CMD	CMD = 1 + 8-bits command code, or CMD = 0 + 8-bit ASCII character code
7..0	8-BIT DATA	

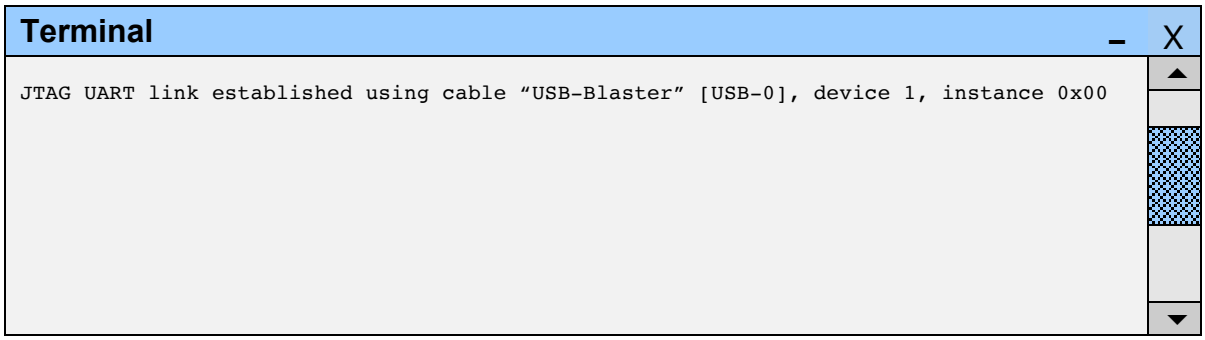
	10	9	8	7	6	5	4	3	2	1	0
SAMPLE OPERATIONS	**LCD ON**	**EN**	**CMD**	**8-BIT DATA**							
DISPLAY OFF	0	x	x	x	x	x	x	x	x	x	x
DISPLAY ASCII CHARACTER e. g 'A' = 0x41	1	PULSE	0	0	1	0	0	0	0	0	1
CLEAR DISPLAY	1	PULSE	1	0	0	0	0	0	0	0	1
RETURN HOME	1	PULSE	1	0	0	0	0	0	0	1	x
ENTRY MODE SET	1	PULSE	1	0	0	0	0	0	1	I/D	SH
DISPLAY ON/OFF CONTROL	1	PULSE	1	0	0	0	0	1	D	C	B
CURSOR or DISPLAY SHIFT	1	PULSE	1	0	0	0	1	S/C	R/L	x	x
SET DISPLAY ADDRESS e.g. 0x00 = Line 1, 0x40 = Line 2	1	PULSE	1	1	AD6	AD5	AD4	AD3	AD2	AD1	AD0

Other commands must be used with care if the LCD display device is to work properly.

Debug Monitor Window

The Altera Monitor Program features a built-in terminal window in the lower left hand corner that can be used to communicate with a NIOS-II program over the attached USB cable. This device is called the *JTAG UART* and uses two 32-bit registers as shown below. Any ASCII characters written to this address will appear directly in the window. Conversely, ASCII characters typed into this window can be read from within a NIOS-II program.

ADDRESS (hex)	SIZE (bits)	I/O	COMMENTS
00008840	32	MIXED	JTAG UART Terminal Interface



0x00008840

31 .. 16	15	14 .. 8	7 .. 0
RAVAIL	*RVALID*	*unused*	8-BIT DATA

BITS	LABEL	DESCRIPTION
31..16	RAVAIL	Number of characters available in the input buffer.
15	RVALID	This bit is 1 when an input character is ready
7..0	DATA	ASCII data to write to or read from the display

0x00008844

31 .. 16	15 .. 11	10	9	8	7 .. 2	1	0
WAVAIL	*unused*	AC	WI	RI	*unused*	WE	RE

BITS	LABEL	DESCRIPTION
31..16	WAVAIL	Amount of space (characters) available in the output buffer.
10	AC	This bit is 1 if activity has occurred (can be written to 0)
9	WI	This bit is 1 if a Write Interrupt is pending
8	RI	This bit is 1 if a Read Interrupt is pending
1	WE	Set this bit to 1 to enable write interrupts. Default = 0
0	RE	Set this bit to 1 to enable read interrupts. Default = 0

Stereo Codec

The DE2 board includes analog input and output connectors (microphone input, line input, and line output). These signals are interfaced through a *codec* (coder/decoder), which is essentially a pair of analog-to-digital (ADC) and digital-to-analog (DAC) converters useful for audio signal processing on two channels (stereo) labeled 'right' and 'left'. The codec configuration may be defined through a set of 16-bit control registers. While the sampling rate and certain other parameters may be modified individually, this interface can be readily initialized for 16-bit samples at a rate of 8000 samples per second.

DAC/ADC Status Register

ADDRESS (hex)	SIZE (bits)	I/O	COMMENTS
00008940	8	INPUT	DAC / ADC Status

7	6	5	4	3	2	1	0
X	X	X	X	ADC RCK	ADC LCK	DAC RCK	DAC LCK

BITS	LABEL	DESCRIPTION
3	ADC RCK	ADC RIGHT CLOCK - The complement of Bit 2. This bit is a square wave at the ADC sampling frequency. On a rising edge, Right channel data may be read from the ADC Input Register.
2	ADC LCK	ADC LEFT CLOCK – The complement of Bit 3. This bit is a square wave at the ADC sampling frequency. On a rising edge, Left channel data may be read from the ADC Input Register.
1	DAC RCK	DAC RIGHT CLOCK - The complement of Bit 0. This bit is a square wave at the DAC sampling frequency. On a rising edge, Right channel data may be written to the DAC Output Register.
0	DAC LCK	DAC LEFT CLOCK – The complement of Bit 1. This bit is a square wave at the DAC sampling frequency. On a rising edge, Left channel data may be written to the DAC Output Register.

DAC/ADC Data Register

ADDRESS (hex)	SIZE (bits)	I/O	COMMENTS
00008960	16	IN/OUT	DAC / ADC Data Word

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
16-bit 2's COMPLEMENT DAC OUTPUT DATA (WRITE) OR ADC INPUT DATA (READ) (SEE STATUS REGISTER ABOVE)															

Codec Control Registers

The internal WM8731 codec configuration registers may be configured through this address.

ADDRESS (hex)	SIZE (bits)	I/O	COMMENTS
00008970	16	OUTPUT	CODEC control registers

1. Write Single Register Contents (Bit 10 = 0)

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CONTROL REGISTER 00..15				CLK	0	BUSY	CONTROL REGISTER DATA								

When Bit 10 is 0, the specified write-only control register is loaded on a rising edge of CLK. Bit 9 (busy) is a status input bit that must be clear (0) before a new value can be written.

2. Set to Predefined Configuration (Bit 10 = 1)

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
X	X	X	X	CLK	1	BUSY	X	X	X	X	X	X	X	X	X

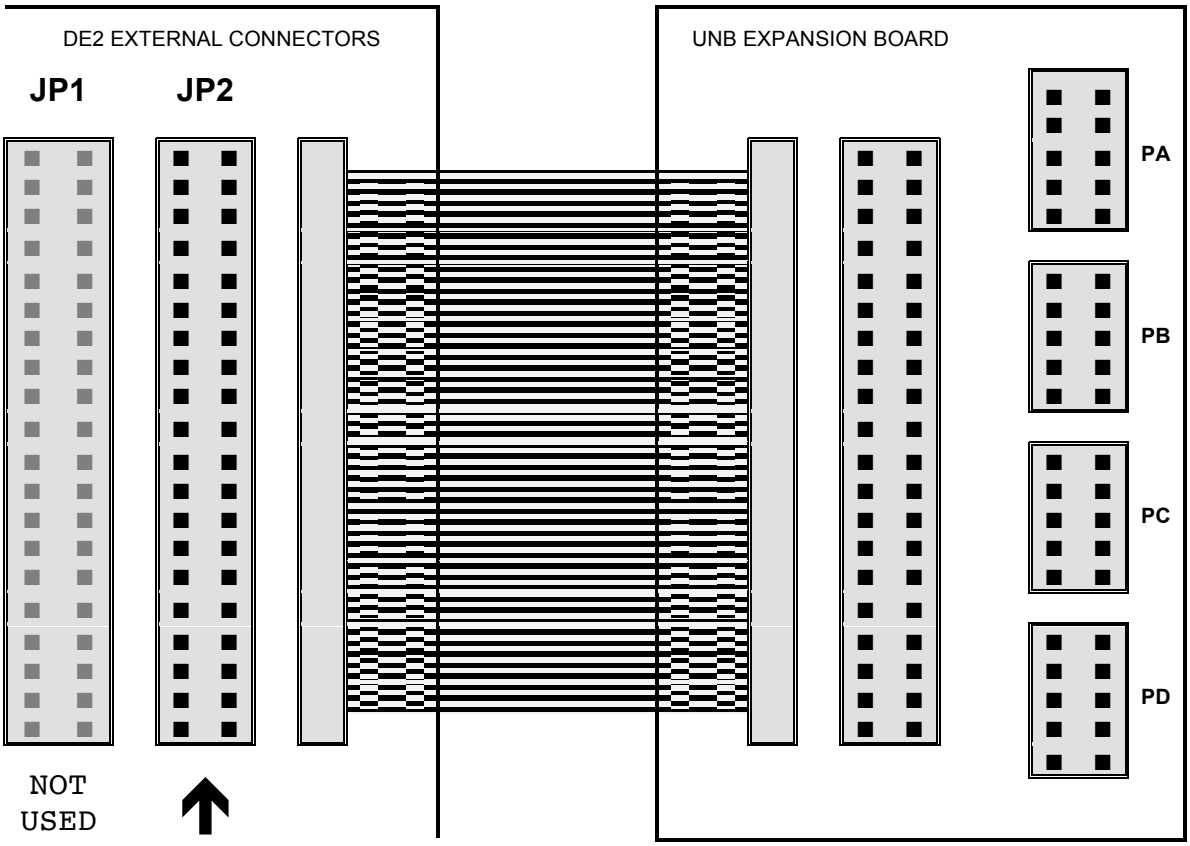
When Bit 10 is 1, the codec is loaded with a set of predefined values on a rising edge of CLK. The following specific values are written to the registers shown.

REG	Value (hex)	Description
15	000	Reset
0	017	ADC Line Input Volume Left
1	017	ADC Line Input Volume Right
2	079	DAC Output Volume Left
3	079	DAC Output Volume Right
4	012	Analog Audio Path Setup (ADC fed from Line Input)
5	001	Digital Audio Path Control
6	000	Power Down Control (power down disabled)
7	041	Digital Interface (Master Mode, 32 bits per sample)
8	00C	Sampling Rate (ADC = DAC = 8000 samples per second)
9	001	Activate…

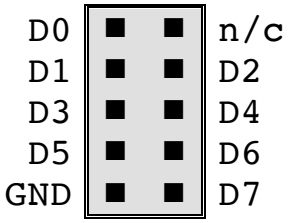
UNB EXPANSION BOARD

External I/O Connections (DE2 Board)

The DE2 board includes two 40-pin connectors labeled JP1 and JP2 on the right hand edge under the plastic cutout. The UNB Expansion Board attaches to JP2 only and provides four 8-bit I/O ports labeled PA, PB, PC, and PD, each with a 10-pin connector as shown below.

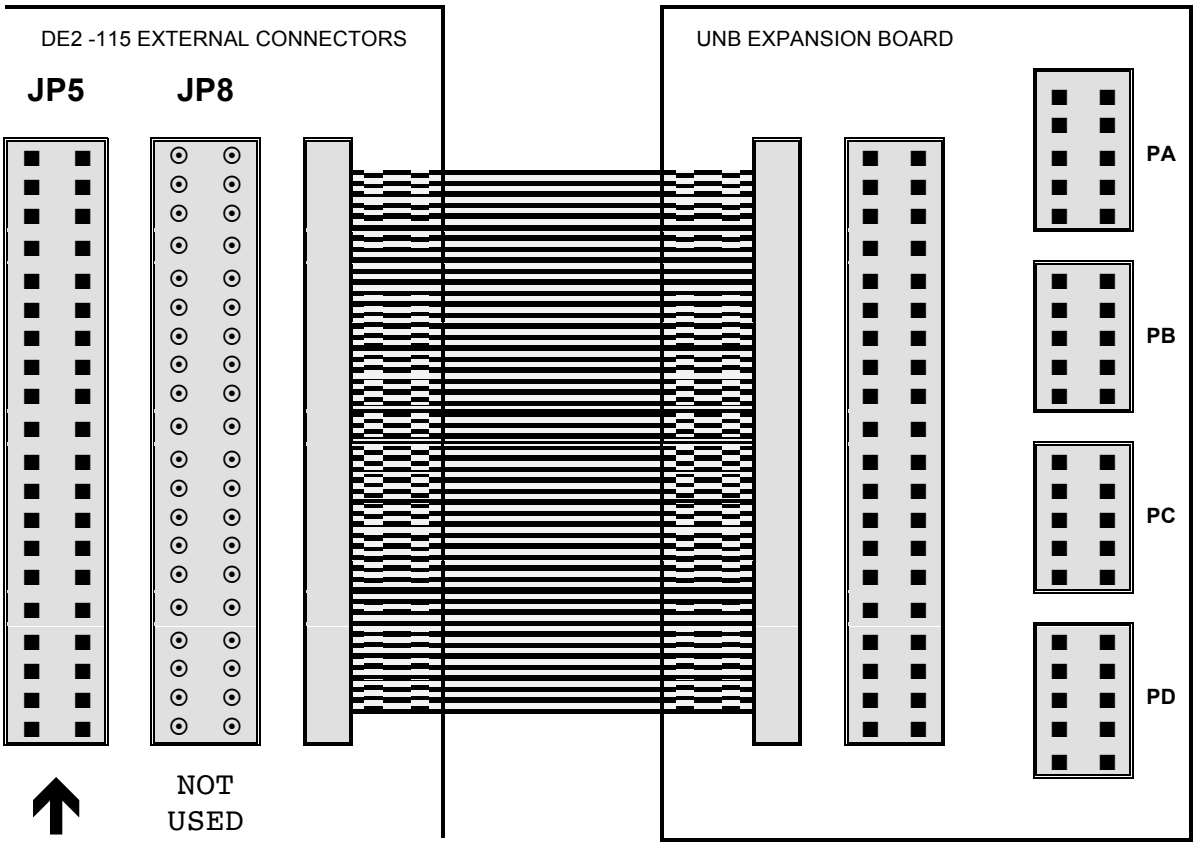


External I/O Connections - 10-pin Cable Headers (PA, PB, PC, PD)

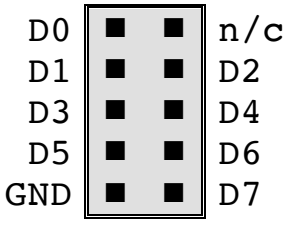


External I/O Connections (DE2-115 Board)

The DE2-115 board includes two 40-pin connectors labeled JP5 and JP8 on the right hand edge under the plastic cutout. The UNB Expansion Board attaches only to JP5 and provides four 8-bit I/O ports labeled PA, PB, PC, and PD, each with a 10-pin connector as shown below.



External I/O Connections - 10-pin Cable Headers (PA, PB, PC, PD)



JP5

JP2

External 8-bit I/O Ports - The UNB Expansion Board connected to JP5 (JP2 on the DE2-115) provides four 8-bit I/O ports labeled PA, PB, PC, and PD. Each pin on each port can be configured for general purpose use as an input or output.

THE FOUR EXPANSION BOARD LEDS REGULARLY FLASH TWICE WHEN CONNECTED HERE

ADDRESS (hex)	SIZE (bits)	I/O	COMMENTS
00008900	8	INDIVIDUAL PINS IN/OUT (set in control register)	I/O Pins → PA
00008910	8	INDIVIDUAL PINS IN/OUT (set in control register)	I/O Pins → PB
00008920	8	INDIVIDUAL PINS IN/OUT (set in control register)	I/O Pins → PC
00008930	8	INDIVIDUAL PINS IN/OUT (set in control register)	I/O Pins → PD

7	6	5	4	3	2	1	0
D7	D6	D5	D4	D3	D2	D1	D0

BITS	LABEL	DESCRIPTION
7..0	D7..D0	Each 8-bit I/O port is connected to a separate10-pin ribbon cable.

Each pin on the UNB expansion board I/O ports (PA, PB, PC, PD) can be input or output as set through this control register. The default setting (0) leaves all pins as inputs.

ADDRESS (hex)	SIZE (bits)	READ/WRITE	COMMENTS
BASE+4	8	R/W	I/O Direction (1 = OUTPUT)

7	6	5	4	3	2	1	0
OUT/IN	OUT/IN	OUT/IN	OUT/IN	OUT/IN	OUT/IN	OUT/IN	OUT/IN