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Good

Mandatory laboratory exercise 3 - Low pass characteristics and Miller effect

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IN3170 - Microelectronics

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Introduction

In this lab we are looking at common source gain stages and their high gain, which makes them good amplifiers. Because of their high input resistance they don't have good bandwidth. To achieve a desired good bandwidth we need to add a buffer stage or source follower and look at how they change the bandwidth.

Tools

We are using Cadence to simulate the circuit and plotting the results.

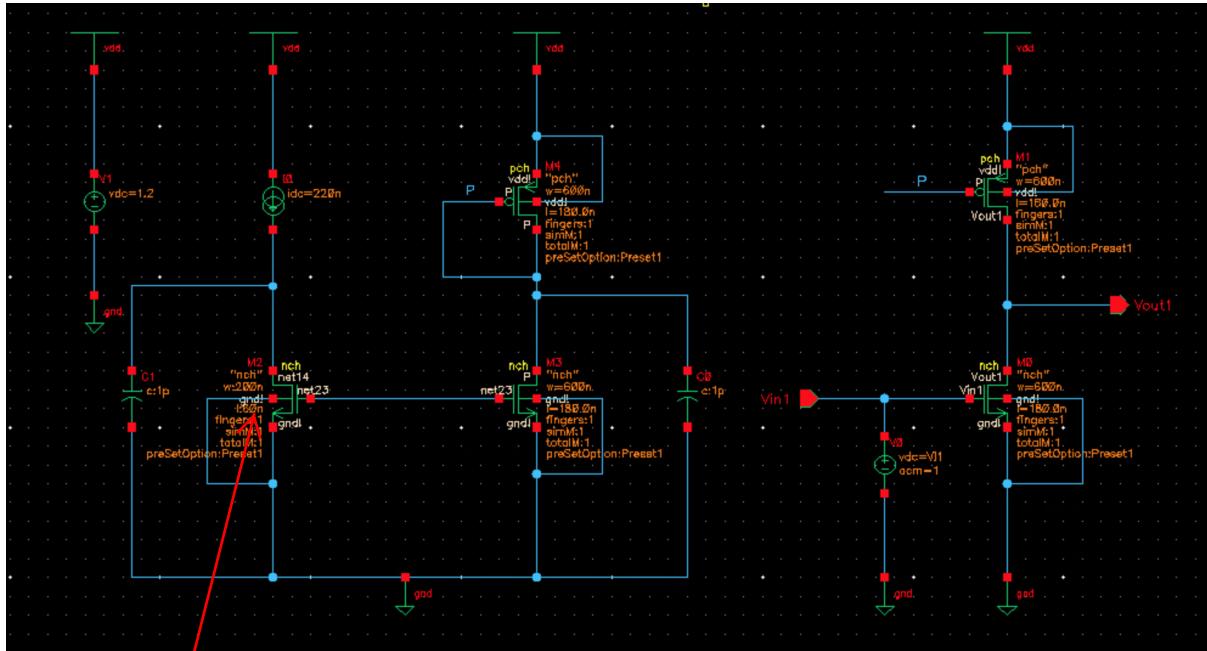
Simulation

Task 1

In this task we are going to simulate a common source (CS) gain stage. We are using a V_{DD} of 1.2 V. As the CS-transistor we are using an nFET transistor with

$\frac{W}{L} = \frac{600 \text{ nm}}{180 \text{ nm}}$. The biasing current source is implemented by a pFET with the same dimensions.

The current mirror is used to provide bias currents and active loads to circuits. We are using a current mirror to find a point of operation V_{I1} when the pFET is in saturation and is approximately 220 nA. The circuit:



Zooming in I see the problem: you need to use the same transistor dimensions for this transistor as well as for the other one in the current mirror. That's why you get a wrong bias current.

Figure 1. Circuit of Common Source with current mirror

The other condition are already met, we can now just sweep V_B^P .

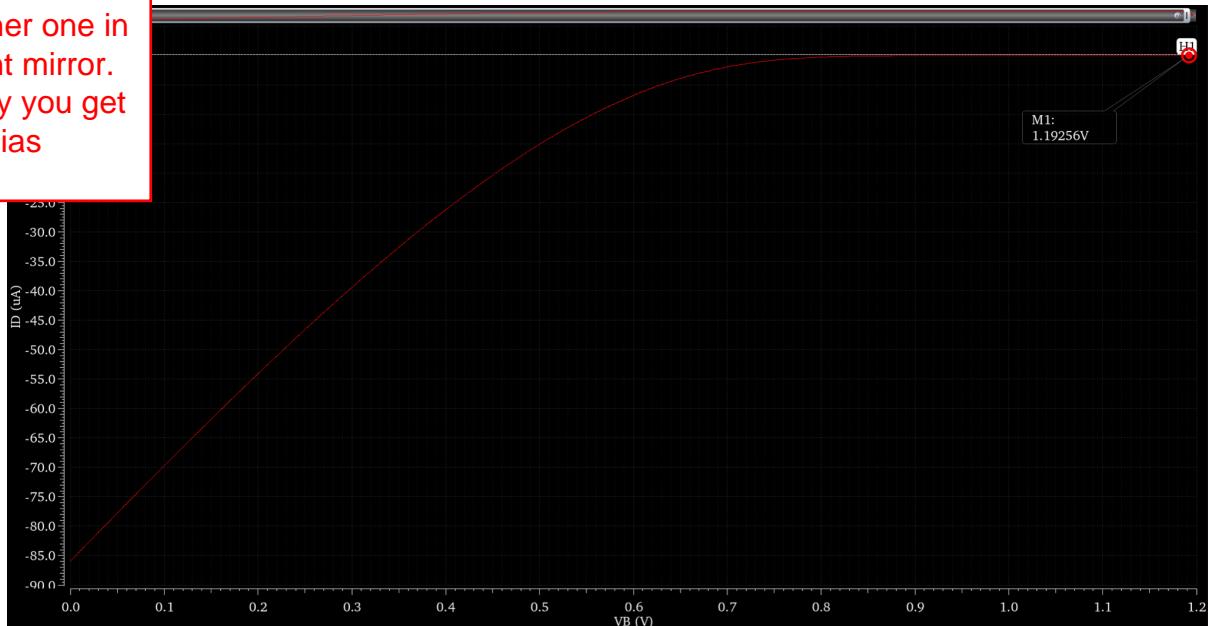


Figure 2. Gate voltage V_B^P

The gate voltage V_B^P is 1.19256 V.

Now we are using a DC analysis to choose an input voltage V_{I1} such that the output point of operation V_{O1} is as

Hmm, you get quite a different result from others, because of your different W/L for one transistor in the current mirror.

operation at $6V$.

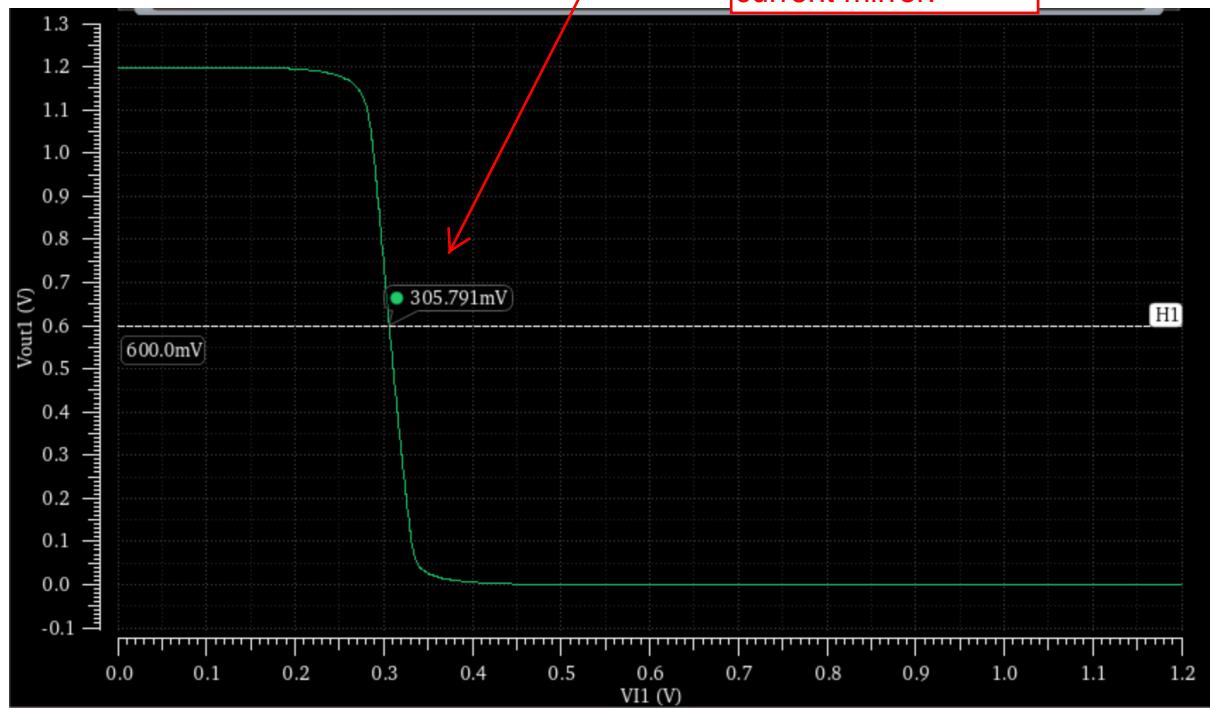


Figure 3. DC analysis of the output signal while sweeping the input signal.

We are using a AC-analysis with logarithmic sweep type to determine the

- $3\text{ dB } BW_1$ and DC gain A_{DC1} .

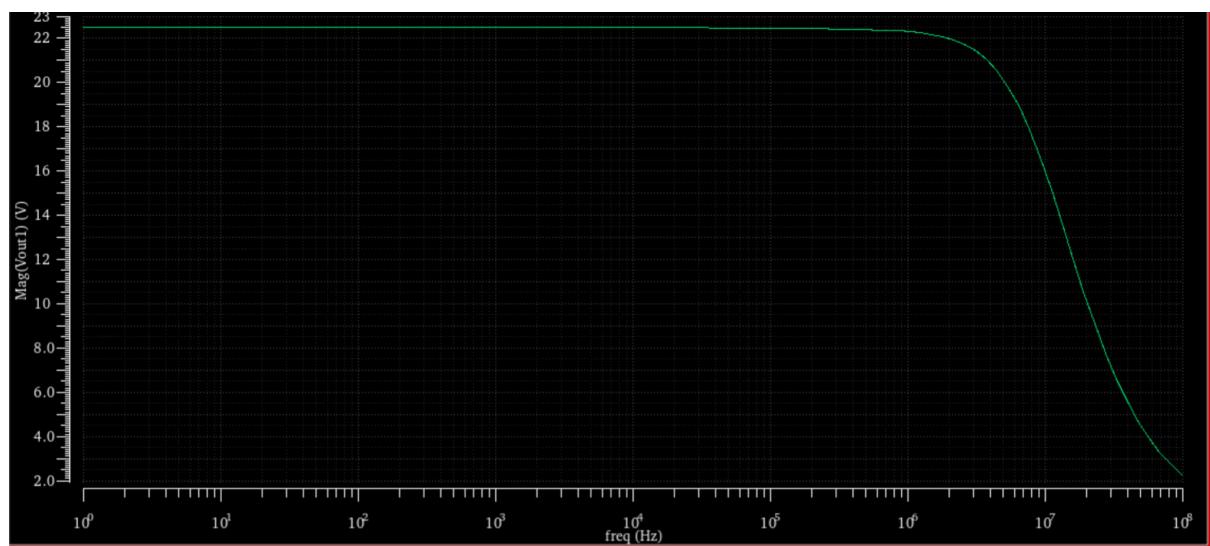


Figure 4. AC analysis of the output signal

By looking at the signal is 1V.

All of these values indicate that you are operating at a bias current that is significantly below 220nA. Not much harm done, if you use the same for the following tasks...

2.5 V/V, when the input

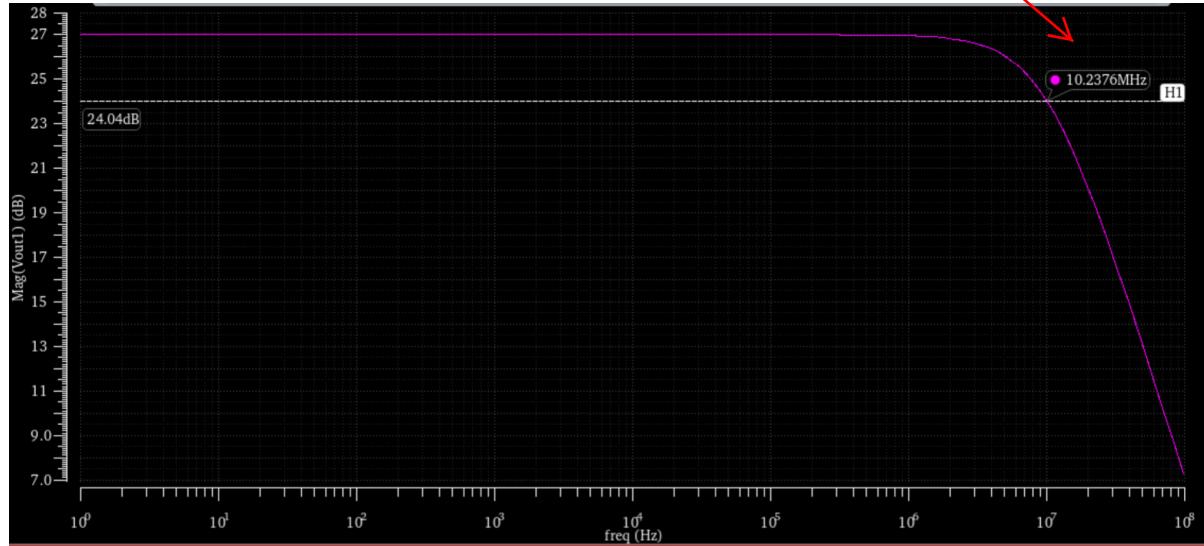


Figure 5. Bode magnitude plot

By looking at the figure 4, we see that $-3 \text{ dB } BW_1$ is 24.04 dB , this gives us a cutoff frequency on $f_{c1} = 10.2376 \text{ MHz}$.

task 1:
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Task 2

In this task we are using two identical CS stages as described in task 1 in series.

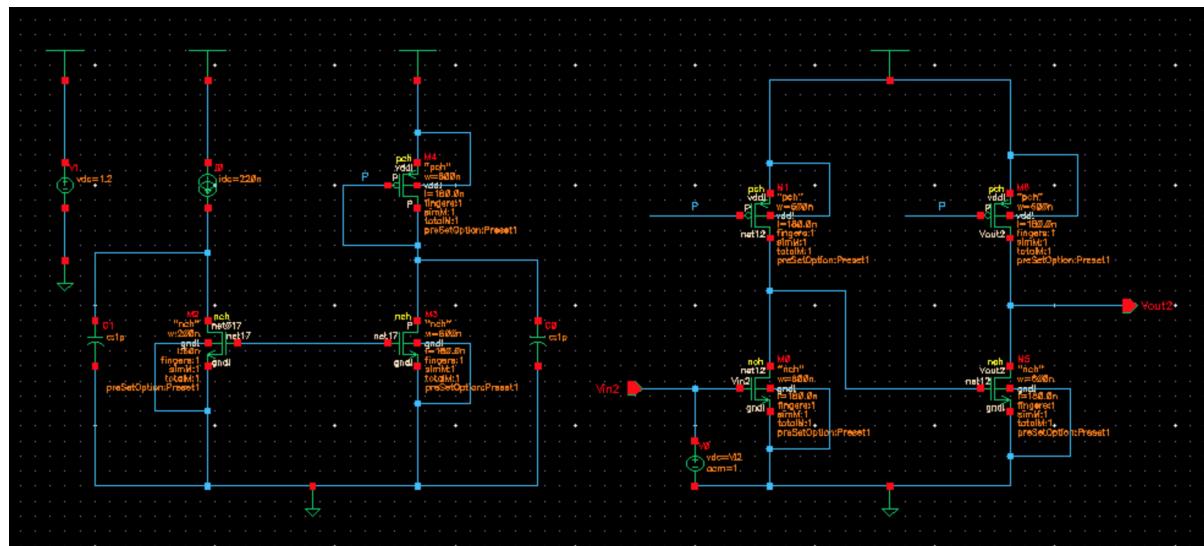


Figure 6. Circuit

We are using a DC analysis to determine the input DC point of operation V_{I2} . Output of the first stage should match the right input DC point of the second stage and again the output point of operation after the second stage V_{O2} is again close to 0.6V.

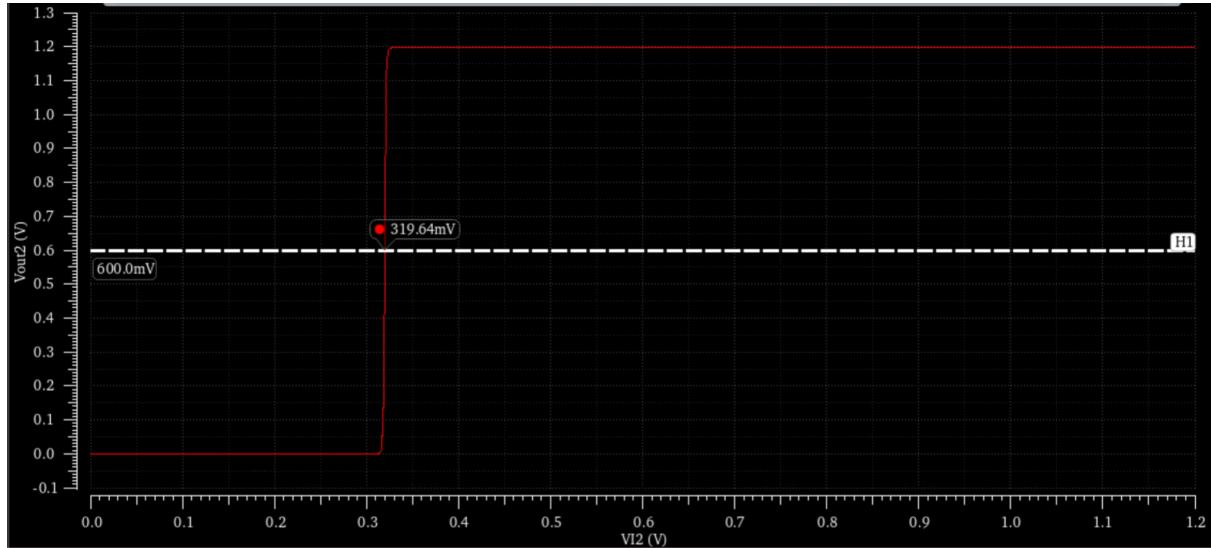


Figure 7. DC analysis

The DC analysis gives us a $V_{I2} = 319.64$ V. We are using an AC analysis to determine BW and DC gain.

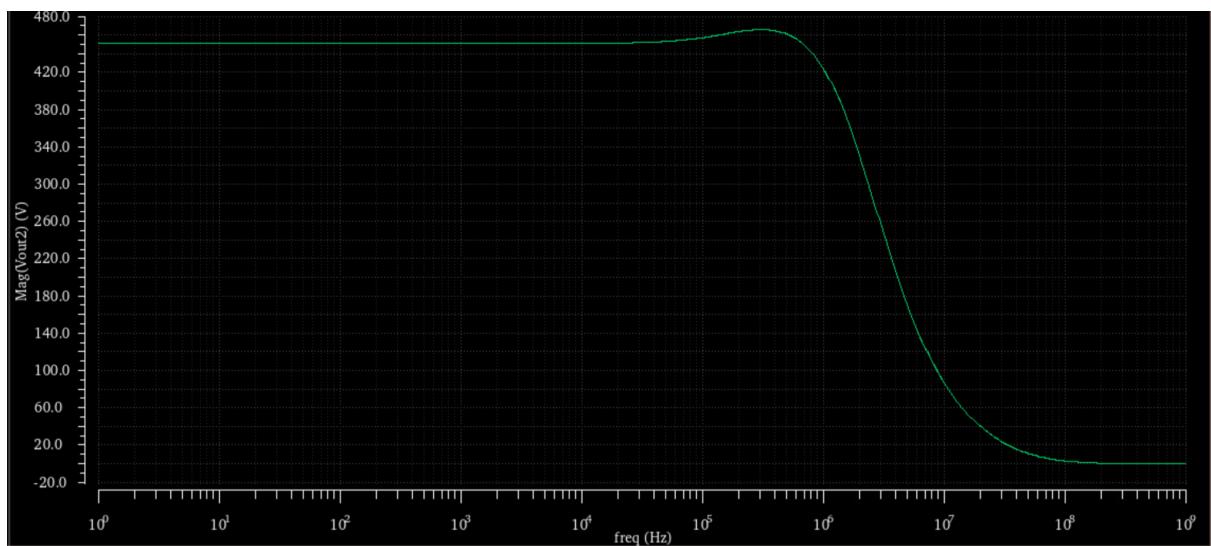


Figure 8. AC analysis

The DC gain A_{DC2} is 451.466 V/V when the input signal is 1V.

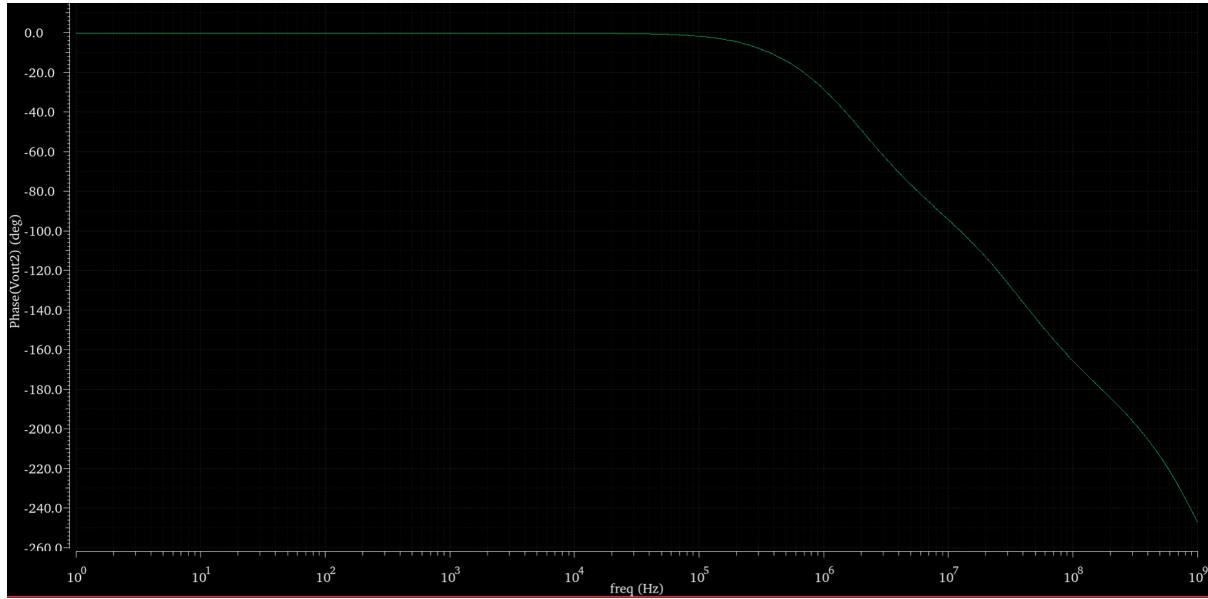


Figure 9. Bode Phase plot

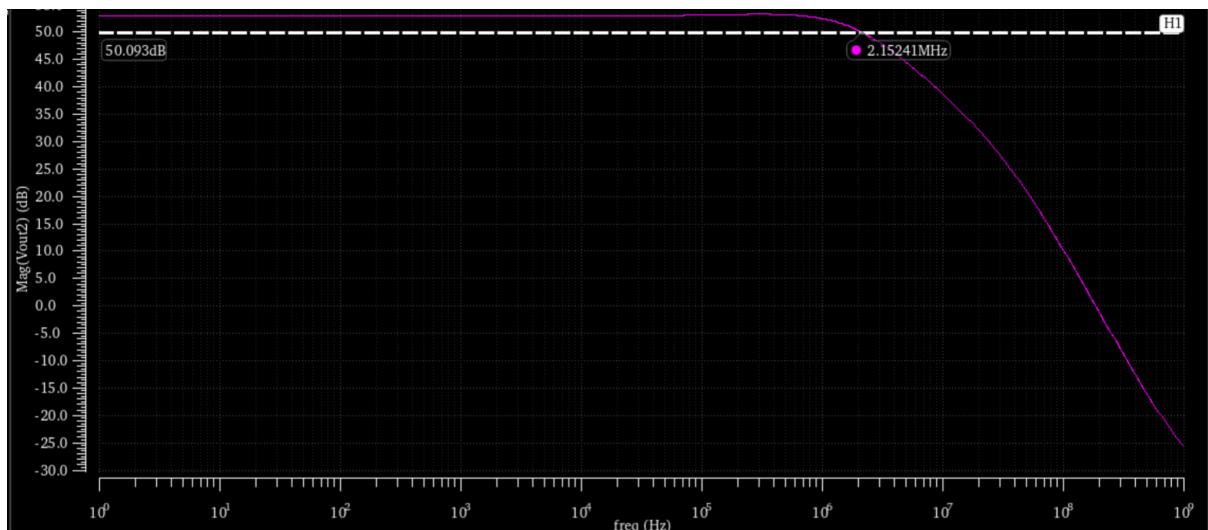


Figure 10. Bode magnitude plot

The $-3\text{ dB } BW_2$ is 50.093 dB , which gives us a cutoff frequency on

$$f_{c2} = 2.15241\text{MHz.}$$

$A_{DC1}^2 = 506.25V/V$ and $A_{DC2} = 451.466V/V$. The combined DC gain A_{DC2} should ideally be close to being A_{DC1}^2 , but is smaller than expected. The second $-3\text{ dB } BW$ is around $\frac{1}{6}$ of the $-3\text{ dB } BW_1$.

The formula for cutoff frequency is : $f_c = 1/(2 * \pi * R * C)$. We see that the f_{c1} is a lot bigger than the f_{c2} when we have two source.

I am missing the term 'Miller effect' here to explain why the capacitance seen at the internal node between the two CS stages is so much bigger...

Task 3

the capacitance of the circuit is a lot bigger series rather than one single common

task 2:
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We are adding a source follower (SF) as a buffer between the stages. We are using an nFET SF with a nFET current source transistor at its source.

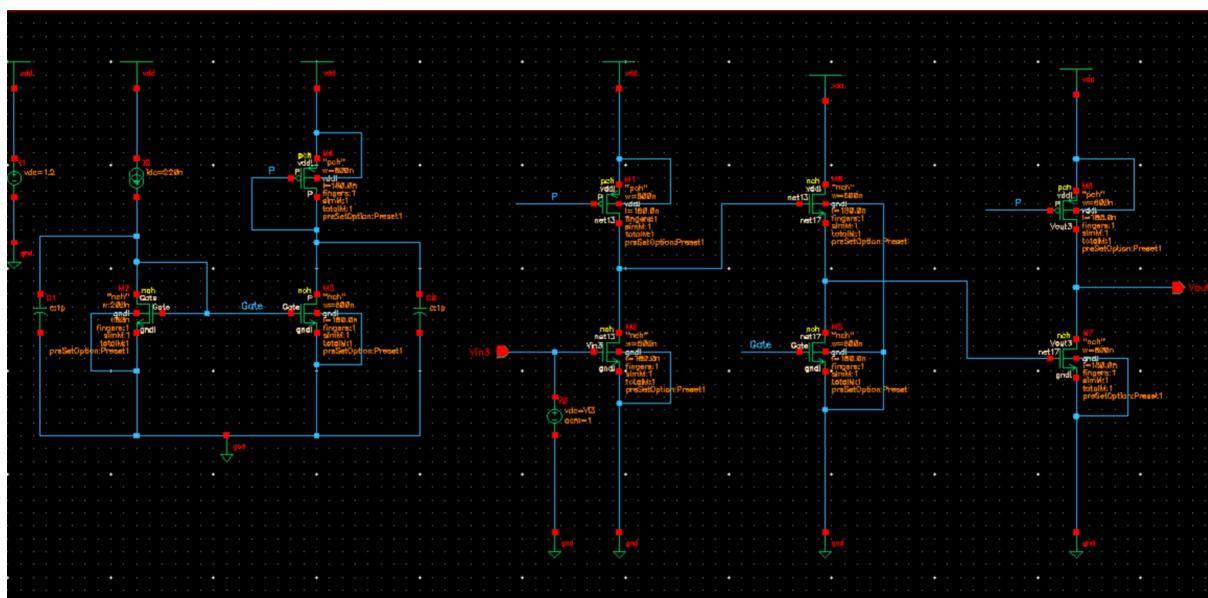


Figure 11. Circuit

Now we adapting the input point of operation such that each of the now three stages' output DC point matches the appropriate input point of operation of the next stage

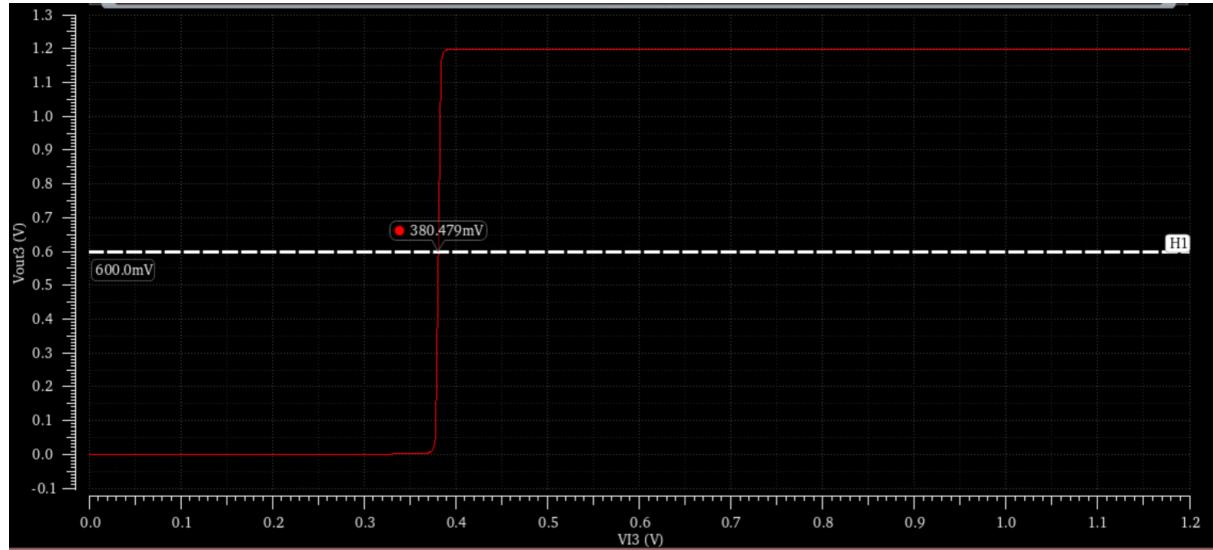


Figure 12. DC analysis

V_{I3} is 380.479 mV . Once again we are using AC analysis to determine gain A_{DC3} and the $-3 \text{ dB } BW_3$.

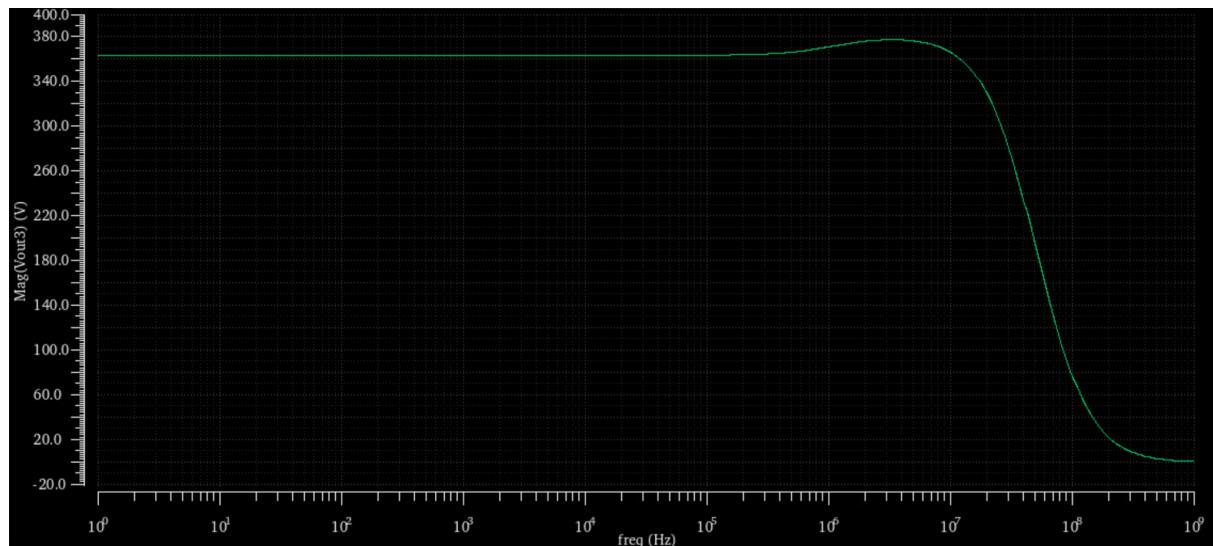


Figure 13. AC analysis

The A_{DC3} gain is 363.883 V/V .

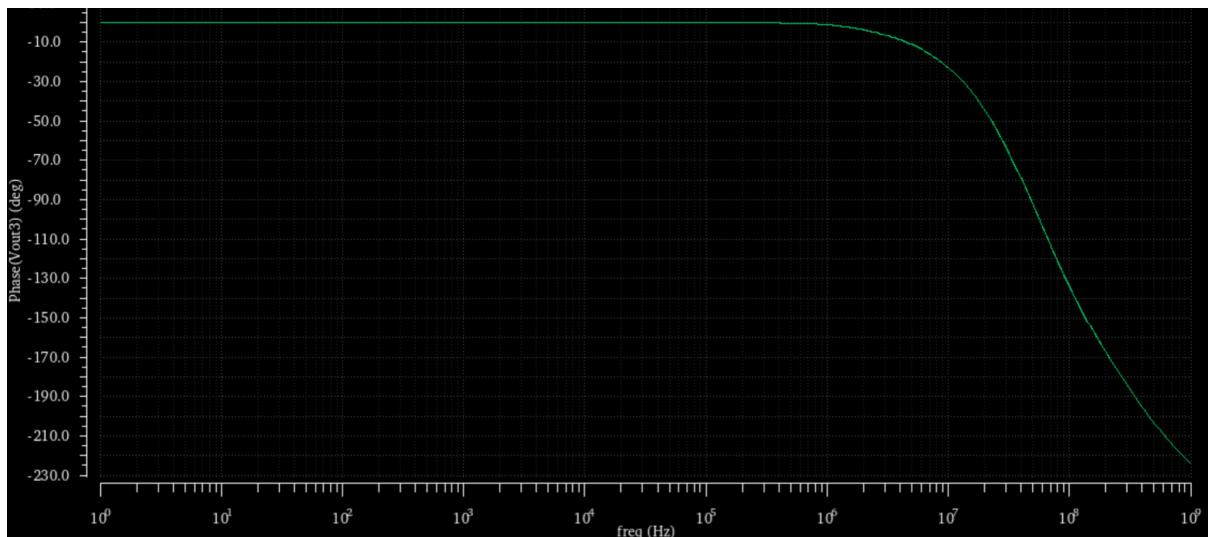


Figure 14. Bode Phase plot

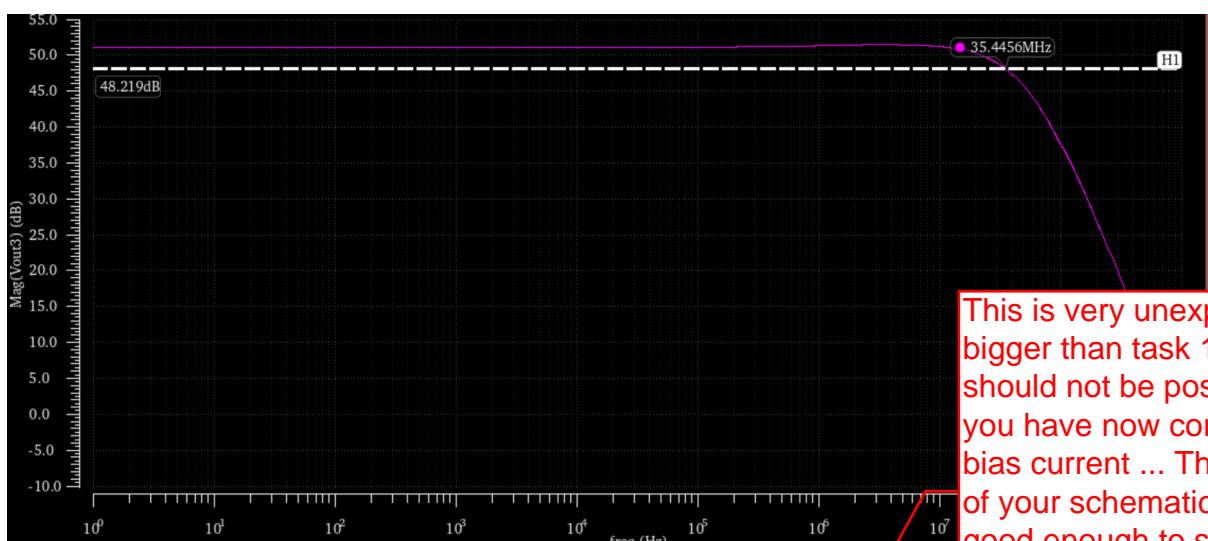


Figure 15. Bode magnitude plot

This is very unexpected: much bigger than task 1, which should not be possible! Unless you have now corrected the bias current ... The resolution of your schematic is not really good enough to see ... but maybe you changed the dimension of the diode connected pFET?

The $-3\text{ dB } BW_3$ is 48.219 dB , which gives us a $f_{c3} = 35.4456\text{MHz}$

After f_{c3} the steepness of the gain is a lot steeper than for task 2, and looking phase plot for both magnitudes for task 2 and task 3, we see that the phase f decreases a lot slower than for task 3.

Good observation, although by changing the bias current, you can no longer really compare the two directly.

In this task we have the source follower that works like a buffer between the two stages of amplifier, with a very high input impedance ideally infinite and very low output impedance. The magnitude plot is a lo

Yes, the important part is what happens at the SF output. At its input it's more important that you do not see a Miller effect, i.e. not the resistive part of the input impedance (which as you correctly state is very high) but the capacitive part, which is now smaller than at the input of a CS stage!.

task 3:
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because the transition of the input to output is a lot better with a source follower than without, which is the case for task 2

Task 4

Now it would be interesting to know about the bias settings: is this comparable to what you used for task 2 or for task 3 ...?

We are now repeating task 2, but now with $\frac{W}{L} = \frac{200 \text{ nm}}{60 \text{ nm}}$

The circuit
It would have helped me debugging if I could read the dimensions of the transistors .. it looks like they are now all 200nm/60nm?

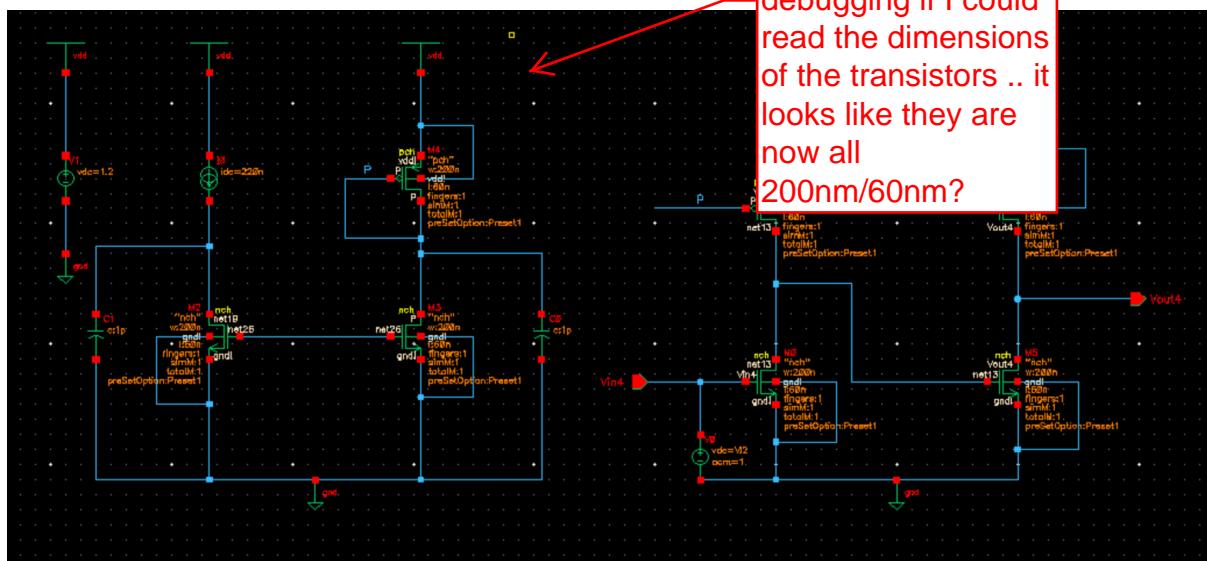


Figure 16. Circuit

We are using a DC analysis to determine the input DC point of operation V_{I4} .

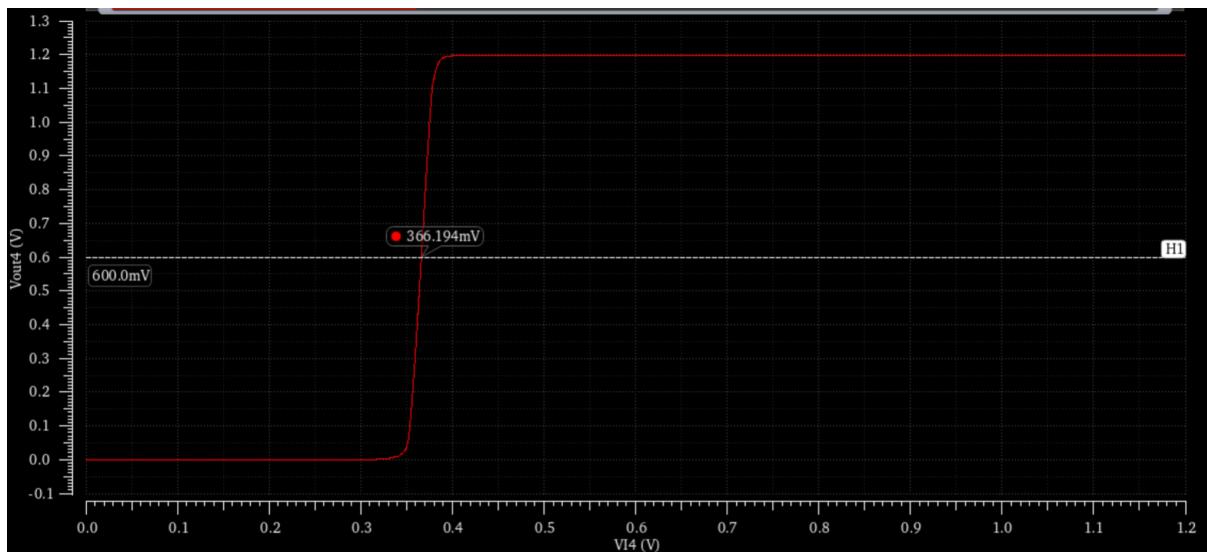


Figure 17. DC analysis

V_{I4} is 366.194 mV. Once again we are using AC analysis to determine gain A_{DC4} and the $-3\text{ dB } BW_4$.

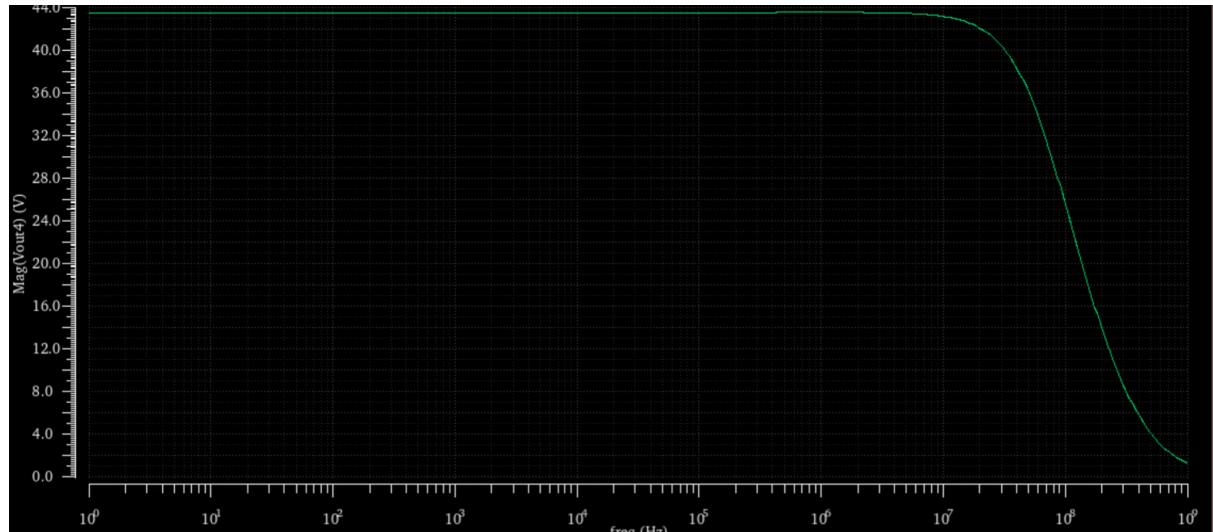


Figure 18. AC analysis

The gain A_{DC4} is 43.508V/V.

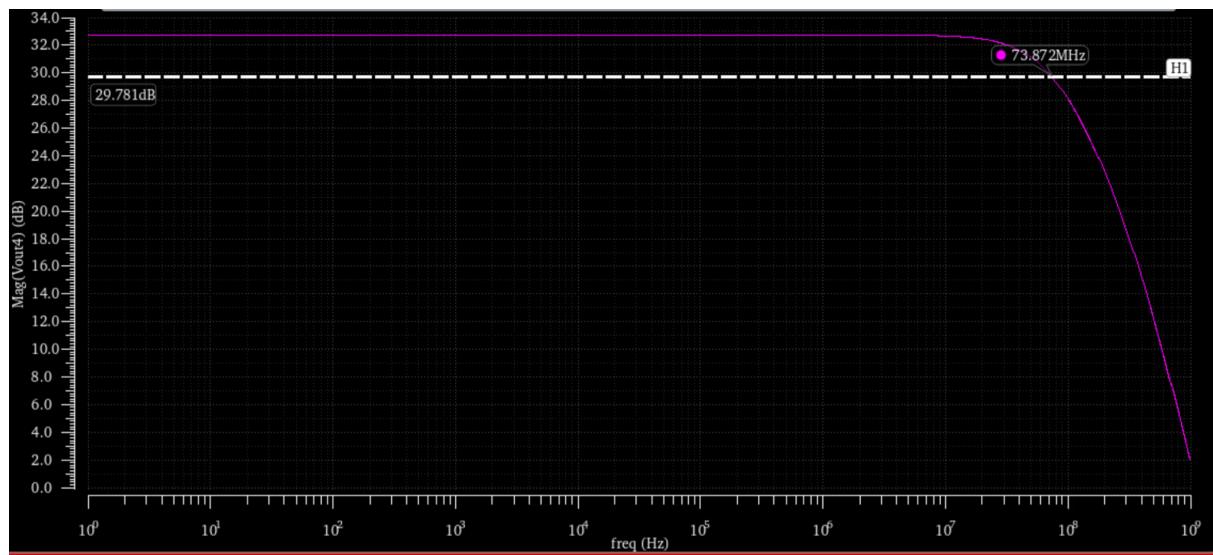


Figure 19. AC analysis

The $-3\text{ dB } BW_4$ is 29.781 dB, which gives us a cut off frequency $f_{c4} = 73.872\text{MHz}$.

The gain A_{DC4} is a lot smaller than A_{DC2} , this is as predicted because the size of the transistor is now a lot smaller than what it is in task 2. The cut off frequency f_{c4} is lot

higher than f_{c2} . This is as expected because

$$A = V_{out}/V_{in} = 1/(j2 * \pi * R * C * f_c +$$

frequencies and for low gain we will have hi

ld f_c your cut off frequency or your input frequency here? Probably the latter, but then this formula says that your DC gain is 1 ... so smth not right here (apart from this seemingly referring to a simple RC filter, which is not exactly what we do have here)

task...

3/4

I'd have expected a discussion on the change of C at the crucial point in the circuit, mainly C_gd and the reduced Miller effect due to reduced gain and reduced C_gd ...