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Mandatory laboratory exercise 2: Inverter gain and speed

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Introduction

In this lab exercise we will look at the speed and gain of an inverter, which can also be regarded as a single ended amplifier.

Tools

We are using Cadence to simulate the circuit and MATLAB for plotting the results

Simulation

Task 1

In this task we are going to simulate two different inverters with different size transistors. For the first inverter the nFET have $W_{n1} = 360\ nm$ and $L_{n1} = 60\ nm$. The pFET have the same length $L_{p1} = L_{n1} = 60\ nm$, but we have to find the width W_{p1} so the switching point of the inverter is as close to $V_{dd}/2$.

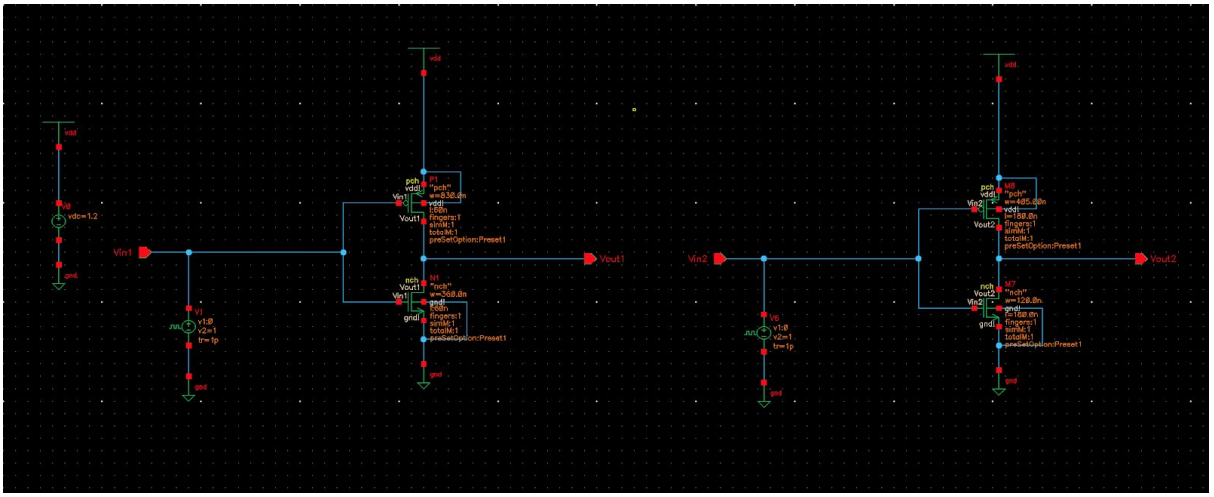


Figure 1: Schematic for inverter 1 and inverter 2.

To find the right width for the inverter we ran a DC simulation where we sweep the input and also sweep the width to get close to a switching point $V_{dd}/2$. We sat the width to a parameter and used “Parametric analysis” to sweep the width. To minimize propagation delay, the width to pFET are chosen to be wider than to nFet in digital circuits. The ratio between them is that the width to pFET is two to three times bigger than the width to nFETs. So we start sweeping the width from 720nm to 1080nm and see what width gives us a switching point close to $V_{dd}/2$.

Figure 2: Setup for the parametric analysis

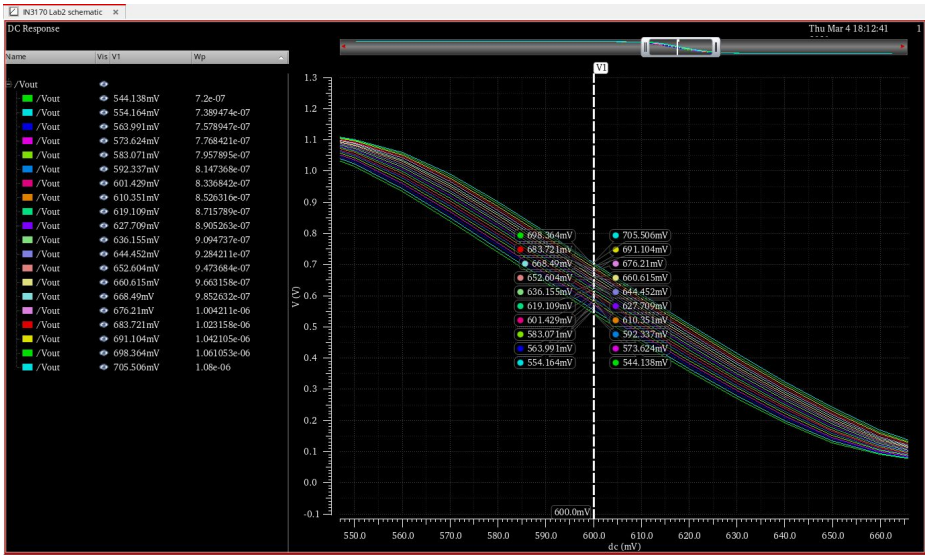


Figure 3: DC response

With the parametric analysis, we run a DC simulation and get a DC response. In Figure 3 we can see the overview over the different switching points and the corresponding width. We see from the two tables to the left for wp and V1 that the width must be around somewhere between 825nm to 833nm. We do a new sweep for those values and get a more exact value for width for the desired switching point.

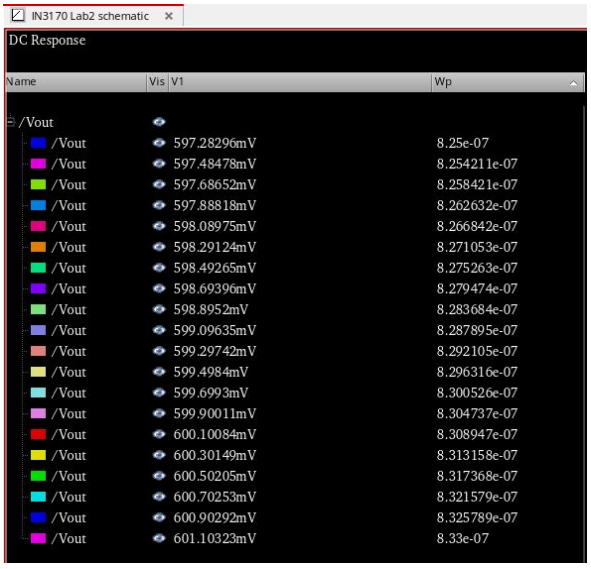


Figure 4: DC response for inverter 1. A close up to values close to the desired switching point.

In Figure 4 we can see a more exact value for the desired width. From the analysis we get a width $W_{p1} = 830\ nm$ gives us a switching point on $599.900nV$, which is very close to $V_{dd}/2$. We have a ratio $W_{p1}/L_{p1} = 830nm / 60\ nm = 13.83$.

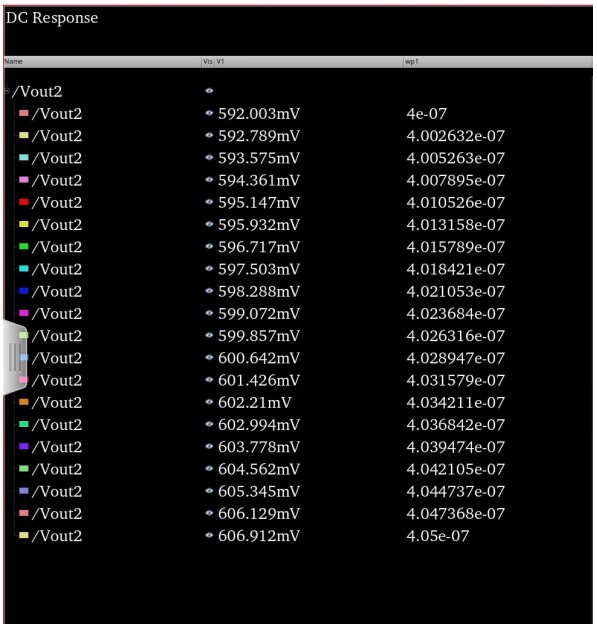
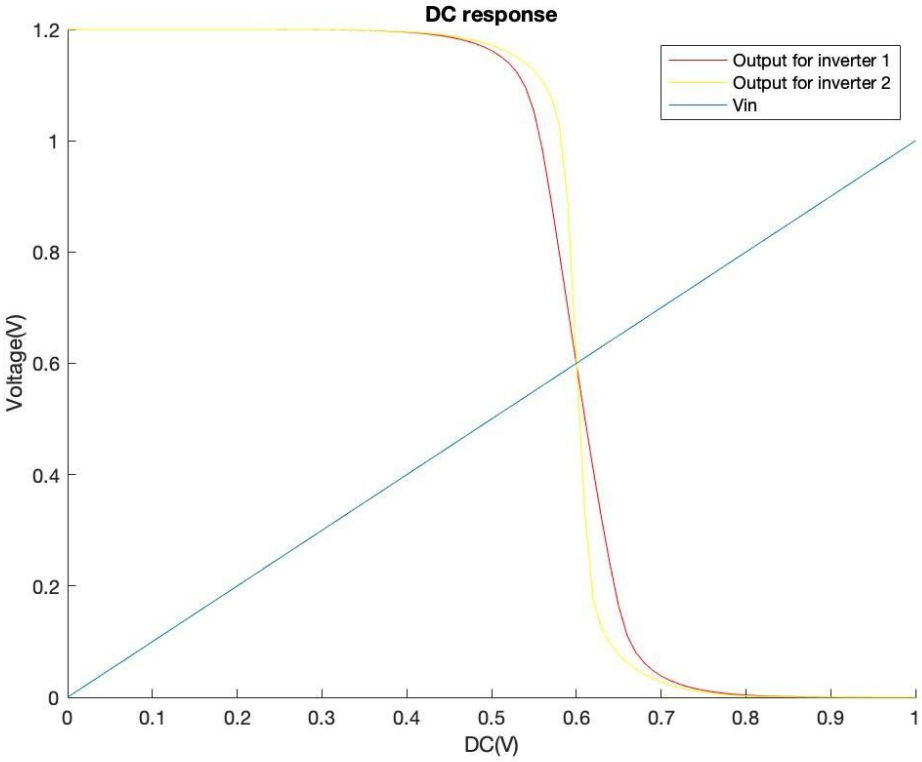


Figure 5: DC response for inverter 2. A close up to values close to the desired switching point

For the second inverter the nFET have $W_{n2} = 120\ nm$ and $L_{n2} = 180\ nm$. The pFET have the same length $L_{p2} = L_{n2} = 180\ nm$. We have to find the width W_{p2} so the switching point of the inverter is as close to $V_{dd}/2$.

We repeat the same process with the “Parametric analysis” for the second inverters W_{p2} and run a sweep for the width from 300nm to 600nm. From that we see that the width is somewhere between 400nm to 410nm. The closest we get to $V_{dd}/2$ is with a width on 403nm but because Cadence does not allow values that don't end with 0 or 5. We have to set the width to 405nm and get a switching point on 606.9mV. The ratio $W_{p2}/L_{p2} = 405\ nm / 180\ nm = 2.25$.

So to summarize the $W_{p1} = 830\ nm$ and $W_{p2} = 405\ nm$. In Figure we have the DC response for both inverter and the input voltage. We can see from the graphs that both inverters have switching point close to $V_{dd}/2$.



task 1: 4/4

Figure 6: DC response for both inverters and the input voltage.

Task 2

In this task we are going to look at the inverter as a single ended amplifier and calculate the DC voltage gain right around the switching point. We can do this either with a DC simulation, sweeping the input, or with a slow ramp input transient simulation.

When using an input transient simulation there is a delay between the input and output, meaning the output values we read are the corresponding values to an input that happened some (very short) time ago. By using a slow ramp we can reduce the inaccuracy caused by this delay.

However this time we will use a DC simulation sweeping the input, as shown in figure 6. We use the following formula to calculate the DC voltage gain: $\delta V out/\delta V in$. To do this we zoom in on the graph to find points for our calculation. We then get the following for the two inverters:

For the first inverter we get: $\delta V\,out/\delta V\,in = |(0.607V - 0.6V)/(0.599V - 0.6V)| = 7$

For the second inverter we get: $\delta V\,out/\delta V\,in = |(0.628V - 0.6V)/(0.599V - 0.6V)| = 28$

The second inverter has a bigger gain. The gain of the second inverter is 28, and the first inverter is 7. The gain of the inverters is dependent on the length of the transistors. The length of the transistors in the first inverter is 60nm, and 180nm in the second inverter, so we can expect about 3 times higher gain on the secor inverter. As we see from the calculations above the second inverter has 4 tim higher gain than the first inverter, this might be due to the fact that Wp1 is abc times larger than Wp2, and might cause higher resistance and therefore lower gain.

task 2: 3.5/4

Task 3

For both variants of inverters, we create two double inverters. First, we create a variant where $W_{n1} = 360nm$, $L_{n1} = 60nm$, $L_{p1} = L_{n1}$ and $W_{p1} = 830nm$ (from Task 1) and $W_{n2} = W_{n1}$, $L_{n2} = L_{n1}$, $L_{p2} = L_{p1}$ and $W_{p2} = W_{p1}$.

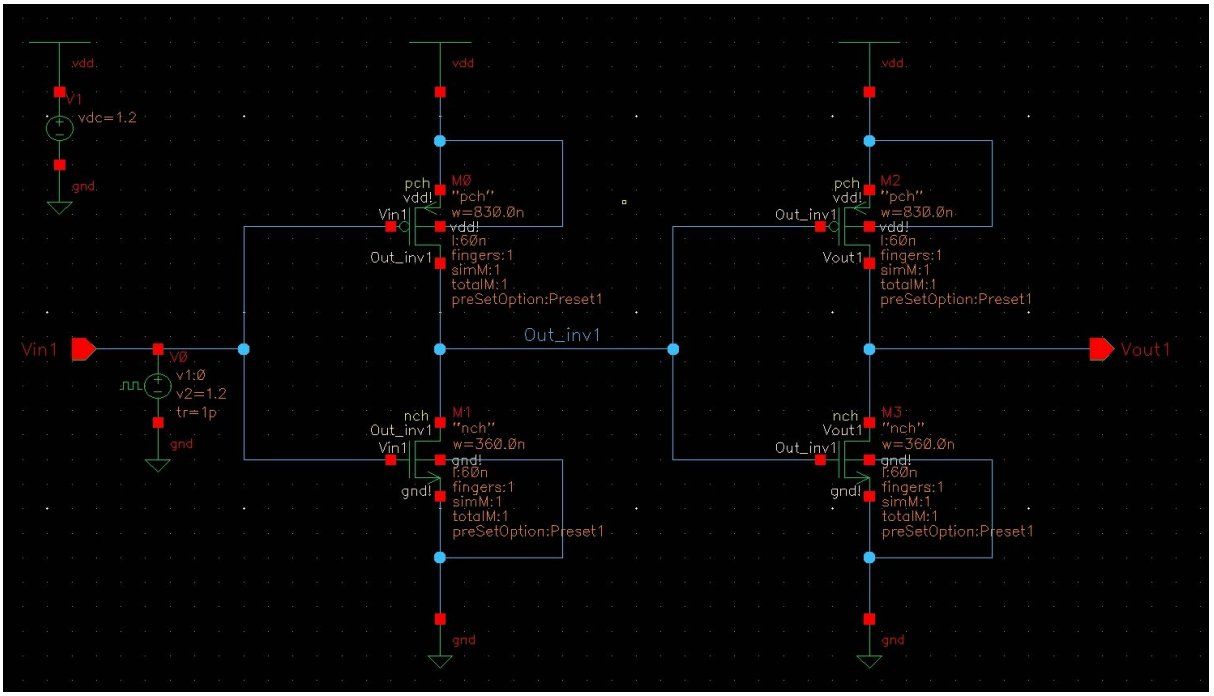


Figure 7. Schematic for inverter 1

Now we create a variant where $W_{n1} = 120nm$, $L_{n1} = 180nm$, $L_{p1} = L_{n1}$ and $W_{p1} = 405nm$ (from Task 1) and $W_{n2} = W_{n1}$, $L_{n2} = L_{n1}$, $L_{p2} = L_{p1}$ and $W_{p2} = W_{p1}$.

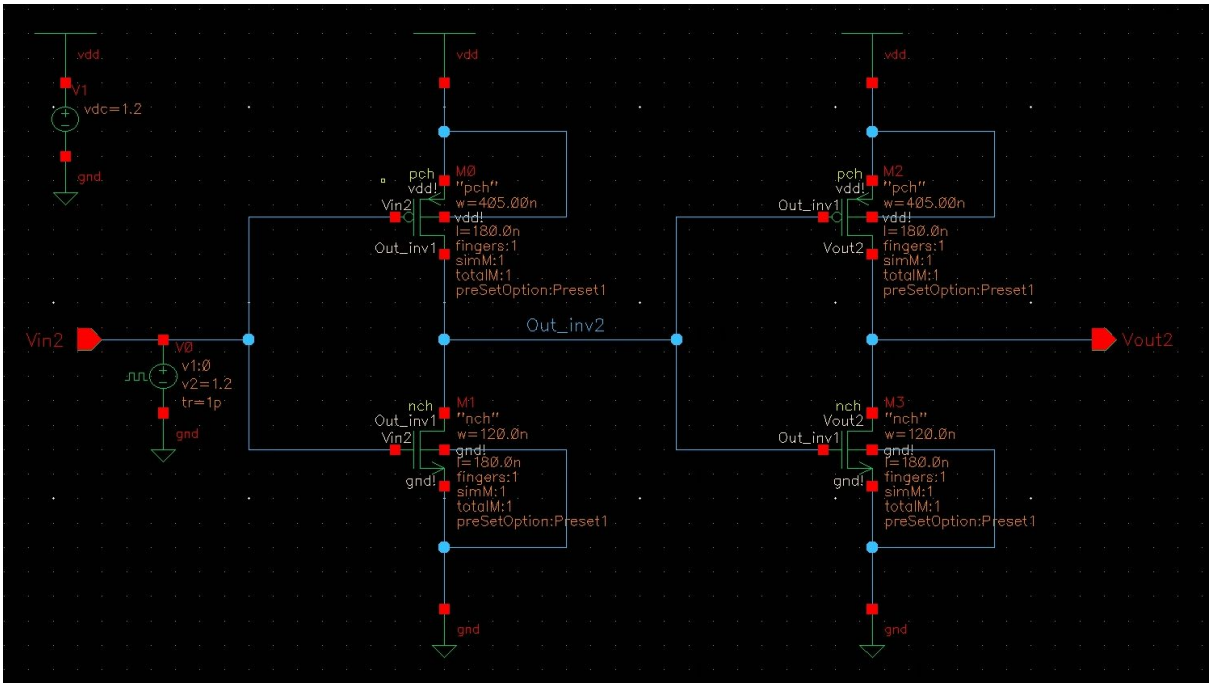


Figure 8. Schematic for inverter 2

We need to provide a square wave input of $10M\ Hz$ with $1ps$ rise and fall time. We create a new instance. As we know the frequency, and we can only provide a period in Cadence, we are using that $T = \frac{1}{f} = \frac{1}{10MHz} = 100ns$. The setup is shown in the figure below.

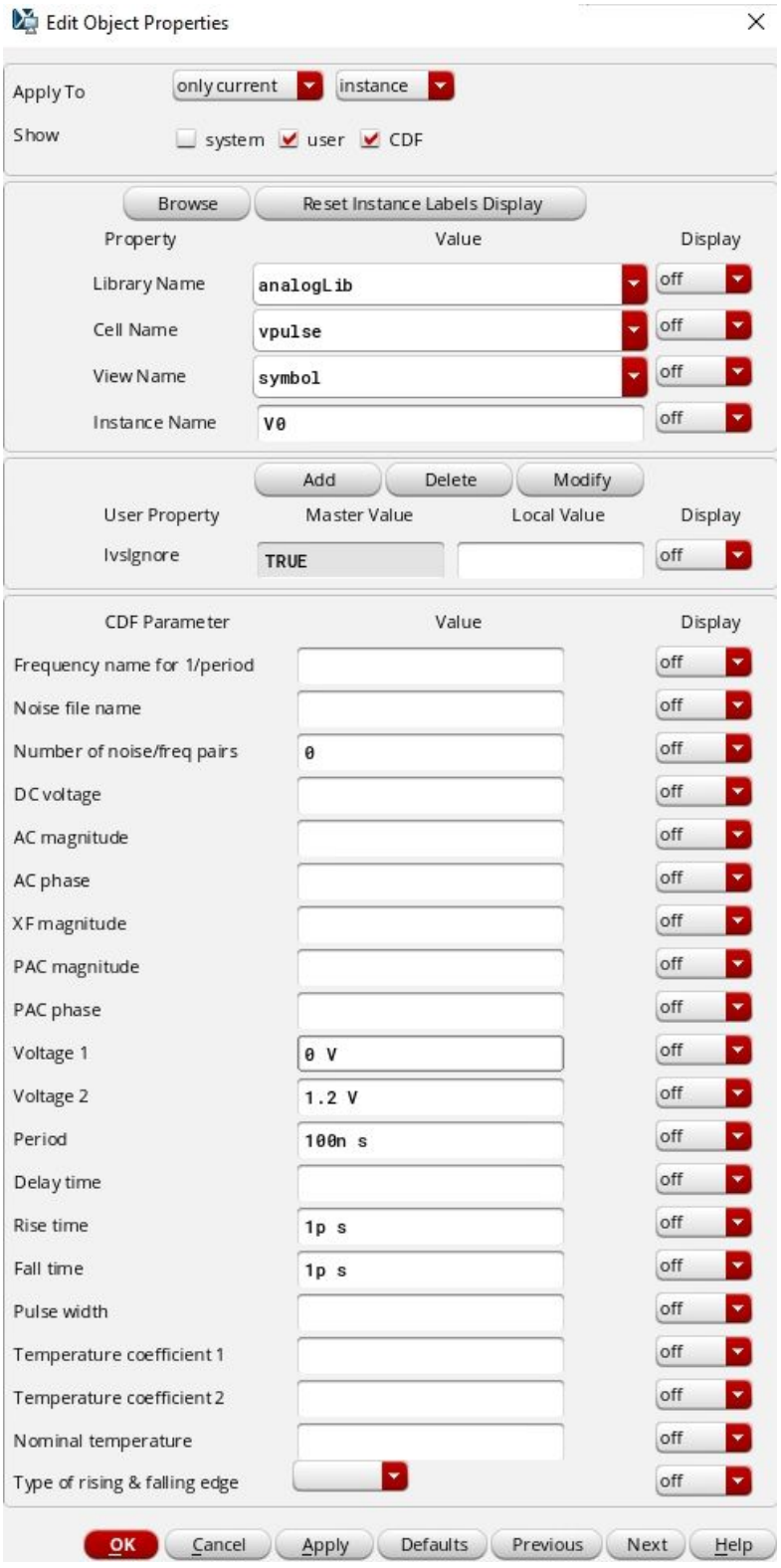


Figure 9. Add instance – square wave

We place it as shown in figure 7. and figure 8. We want to show the high to low and low to high transition. We choose a transient analysis

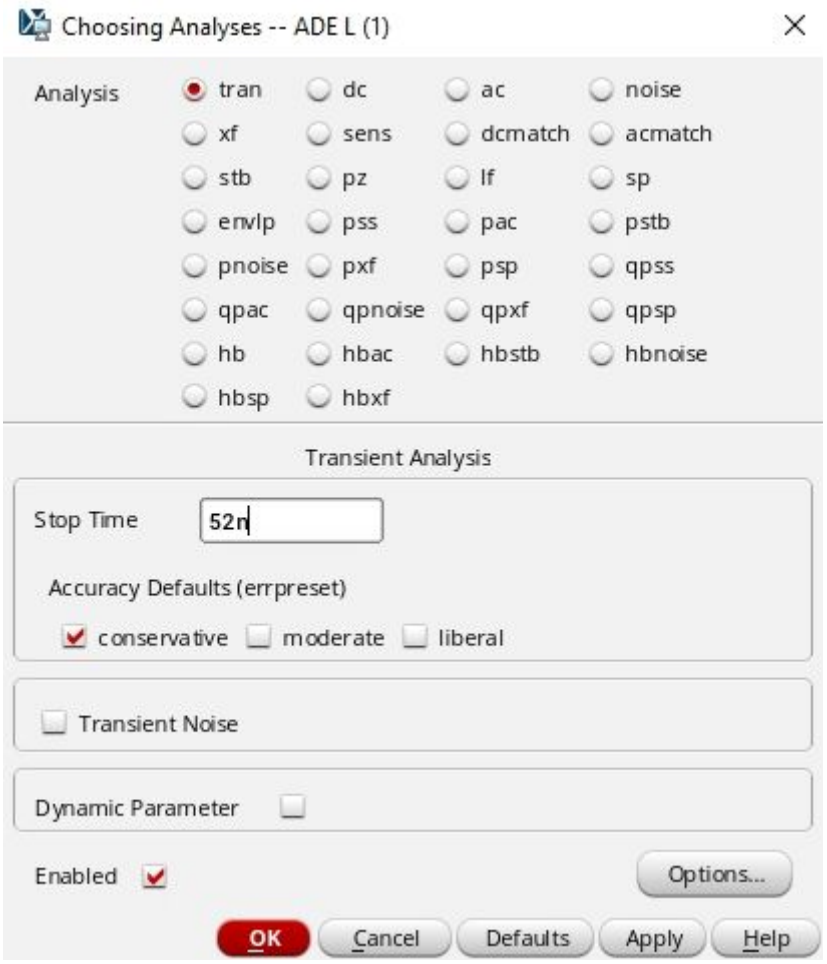


Figure 10. Choosing analyses

And we choose the outputs in the ADE L window

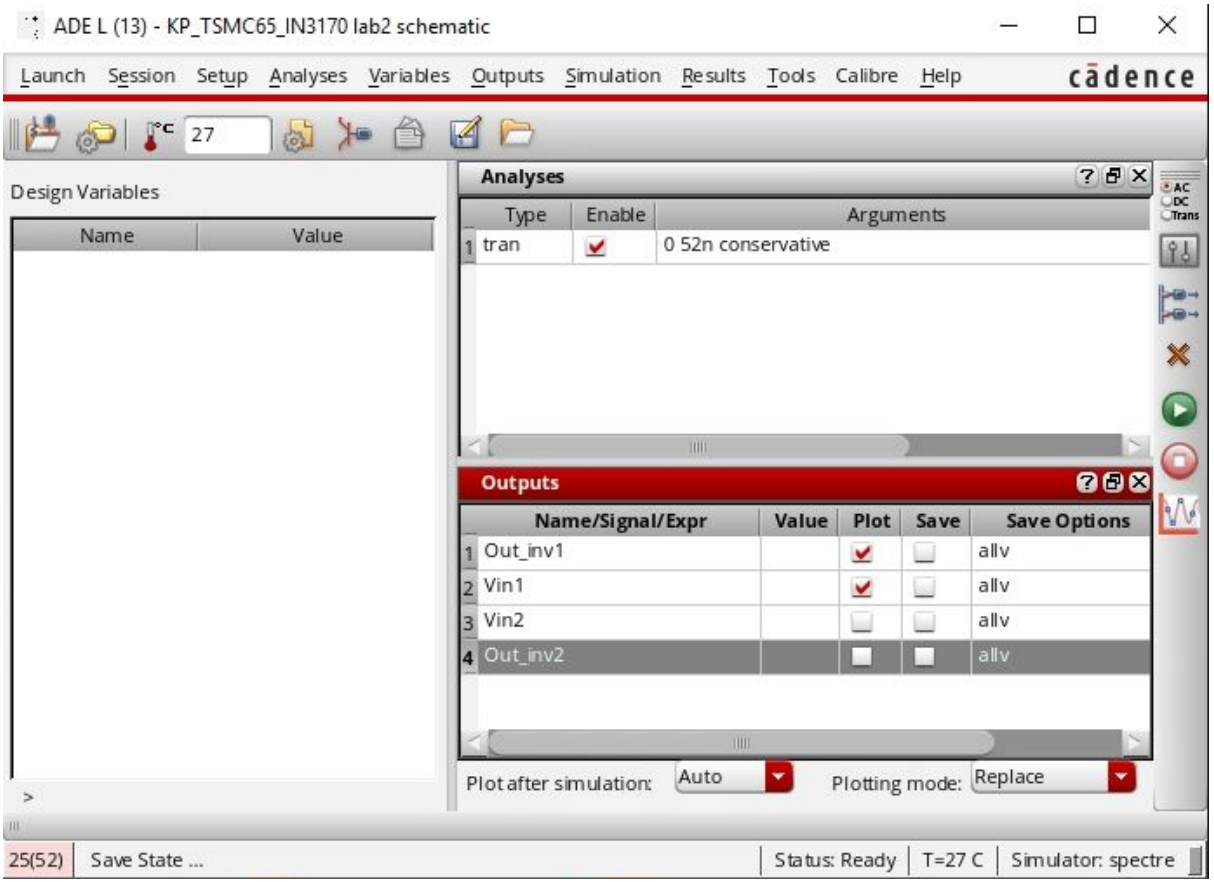


Figure 11. ADE L setup

We now run the simulations and export the data to MATLAB. The results:

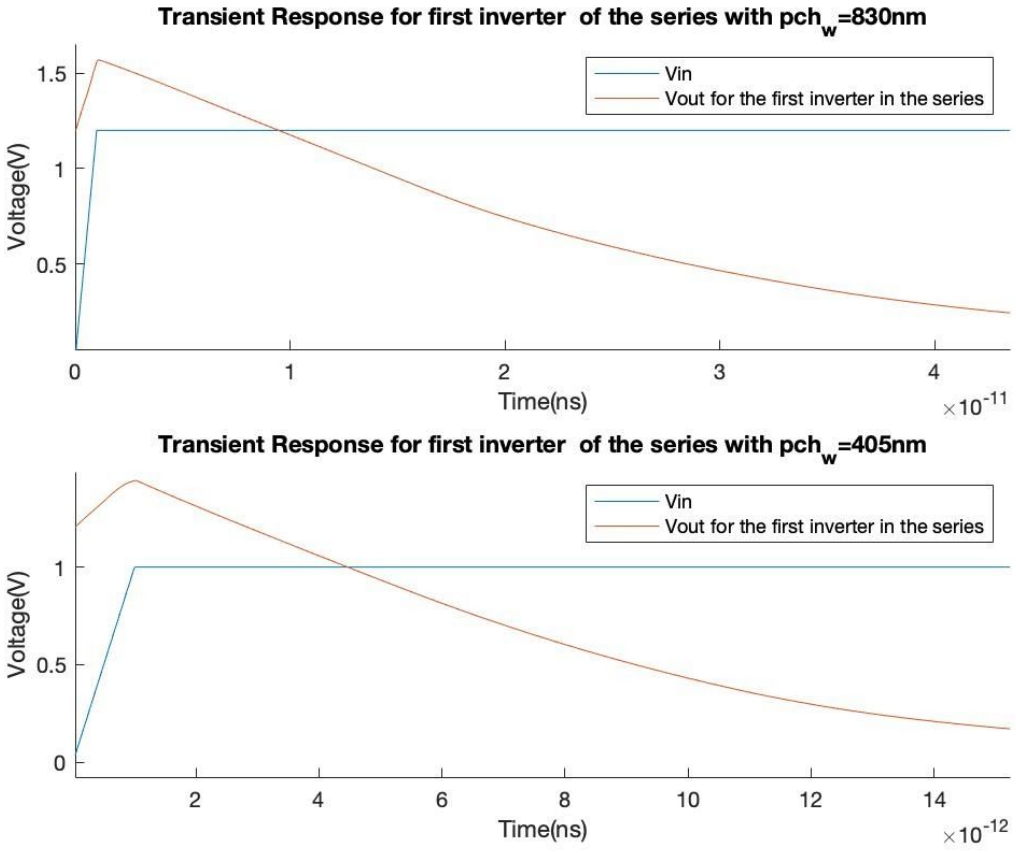


Figure 12. Transient Response for both inverters for high to low transition.

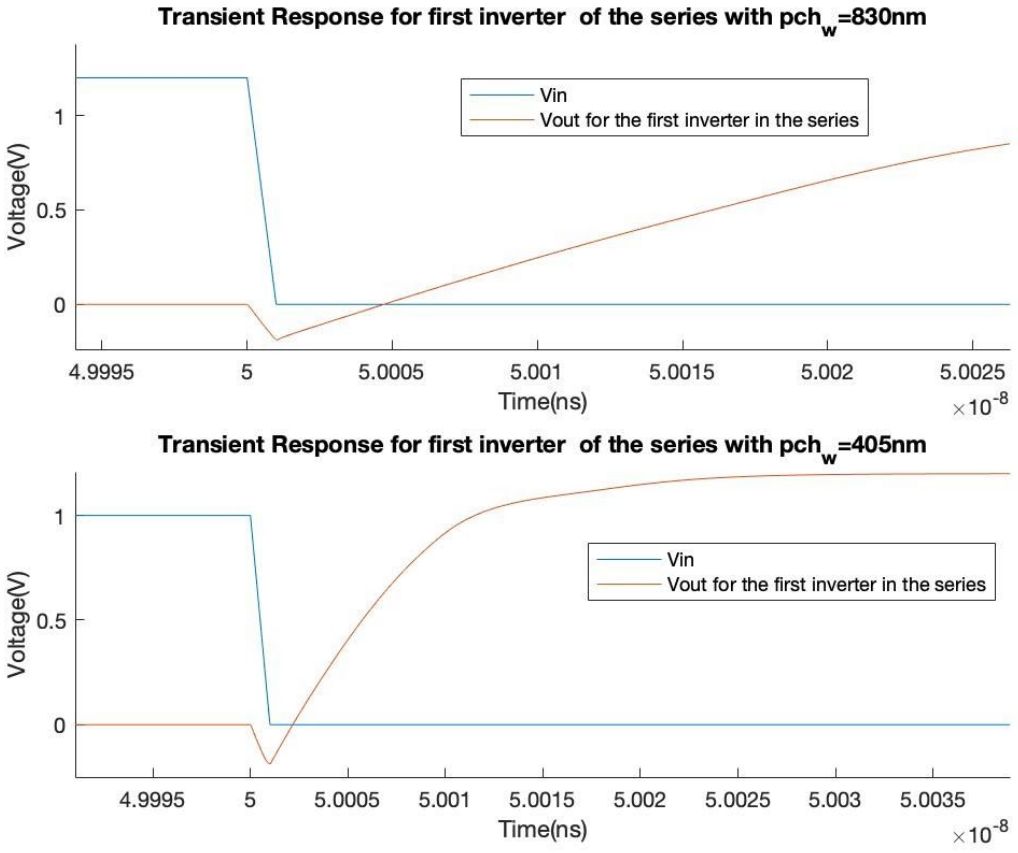


Figure 13. Transient Response for both inverters for low to high transition.

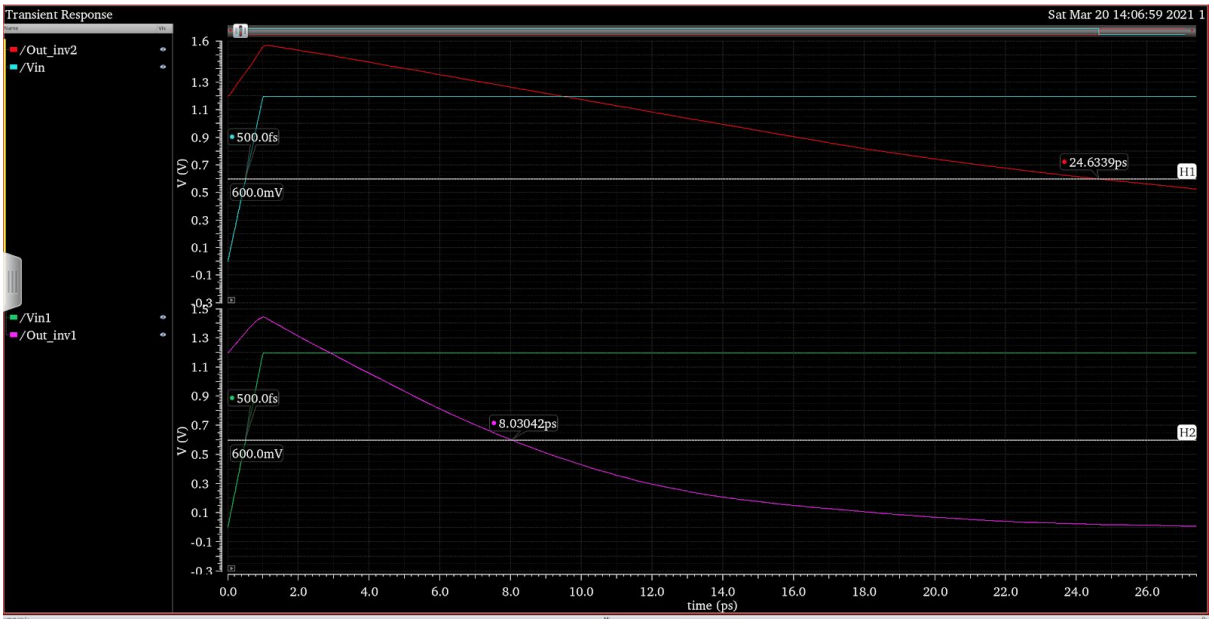


Figure 14. Transient Response for both inverters for high to low transition.

In Figure 14 we have the propagation delay for the high to low transition. We can see that the

$t_{PHL_{inverter\ 1}} = 24.6339ps - 500fs = 0.241339ps$ and

$t_{PHL_{inverter\ 2}} = 8.03042ps - 500fs = 7.53042ps$.

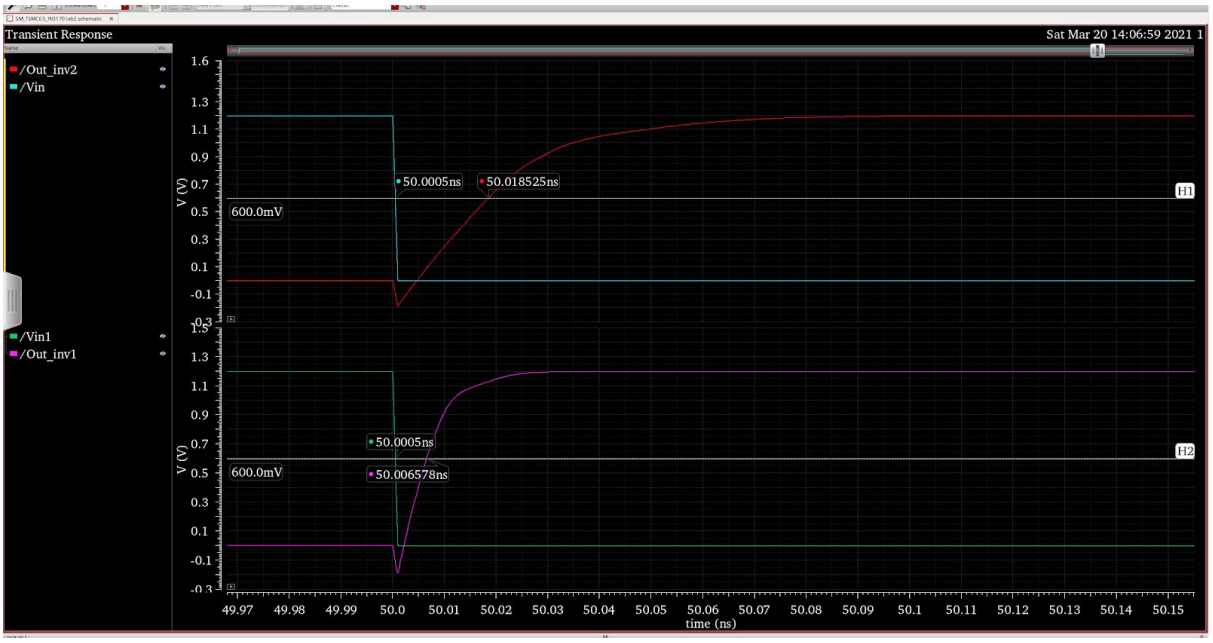


Figure 15. Transient Response for both inverters for low to high transition.

In Figure 15 we have the propagation delay for the low to high transition. We have

$t_{PLH_{inverter\ 1}} = 50.006578ns - 50.0005ns = 6.078ps$ and

$t_{PLH_{inverter\ 2}} = 50.018525ns - 50.0005ns = 18.025ps$.

The average propagation delay for inverter 1 is :

$t_{p_{inverter\ 1}} = 1/2\ (t_{PHL_{inverter\ 1}} + t_{PLH_{inverter\ 1}}) = 1/2(\ 0.241339ps +$

$6.078ps) = 2.50073 * 10\hat{}^{-8}s = 3.1596695ps$

The average propagation delay for inverter 2 is :

$t_{p_{inverter\ 2}} = 1/2(t_{PHL_{inverter\ 2}} + t_{PLH_{inverter\ 2}}) = 1/2\ (7.53042ps + 18.025ps) = 1.27777 * 10\hat{}^{-11}s = 12.7777ps$

The ratio $t_{p_{inverter\ 2}}/t_{p_{inverter\ 1}} = 12.7777ps/3.1596695ps = 4.044$

We see from the ratio that inverter 2 has 4 times bigger delay then inverter 1. Which means that inverter 2 is four times slower to respond to change of input.

Here is the results from the task 1:

$$W_{p1}/L_{p1} = 830nm / 60\ nm = 13.83$$

$$W_{p2}/L_{p2} = 405\ nm / 180\ nm = 2.25$$

Using large W/L ratio can result in a reduction in t_P , which in our case makes sense. We have a bigger ratio W_p/L_p for inverter 1 then for inverter 2, so we have a smaller t_P for inverter 1 than for inverter 2. Which is as expected.

task 3:
3/4

Here is the MATLAB code that we are using:

```
%task1 plotting the id vs vgs plot for different values for vds
inv1 = csvread("lab2_task1_inv1.csv",1); % Read the data
inv2 = csvread("lab2_task1_inv2.csv",1);
vin = csvread("lab2_task1_vin.csv",1);

vin_inv1_series = csvread("lab2_task3_vin_inv1series.csv",1);
vout_inv1_series = csvread("lab2_task3_vout_inv1series.csv",1);
vin_inv2_series = csvread("lab2_task3_vin_inv2series.csv",1);
vout_inv2_series = csvread("lab2_task3_vout_inv2series.csv",1);

yL = ylim;
figure()
hold on;
plot(inv1(:,1),inv1(:,2), "r")
plot(inv2(:,1),inv2(:,2), "y")
plot(vin(:,1), vin(:,2))
%line([0.6 0.6], yL)
title("DC response")
xlabel("DC(V)")
ylabel("Voltage(V)")
legend("Output for inverter 1", "Output for inverter 2", "Vin")
hold off;

figure()
hold on;
plot(vin_inv1_series(:,1), vin_inv1_series(:,2))
plot(vout_inv1_series(:,1), vout_inv1_series(:,2))
title("Transient Response for first inverter  of the series with
   pch_w=830nm")
xlabel("Time(ns)")
ylabel("Voltage(V)")
legend("Vin", "Vout for the first inverter in the series")
hold off;

figure()
hold on;
plot(vin_inv2_series(:,1), vin_inv2_series(:,2))
plot(vout_inv2_series(:,1), vout_inv2_series(:,2))
title("Transient Response for first inverter  of the series with
   pch_w=405nm")
xlabel("Time(ns)")
ylabel("Voltage(V)")
legend("Vin", "Vout for the first inverter in the series")
hold off;
```