Digital Design and Computer Architecture LU

Lab Protocol

Exercise IV

Group 11

Klaus Botschen, Matr. Nr. 8625499

klaus.botschen@student.tuwien.ac.at

Manuel Fischer, Matr. Nr. 11905171

manuel.fischer@tuwien.ac.at

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Forwarding Simulation

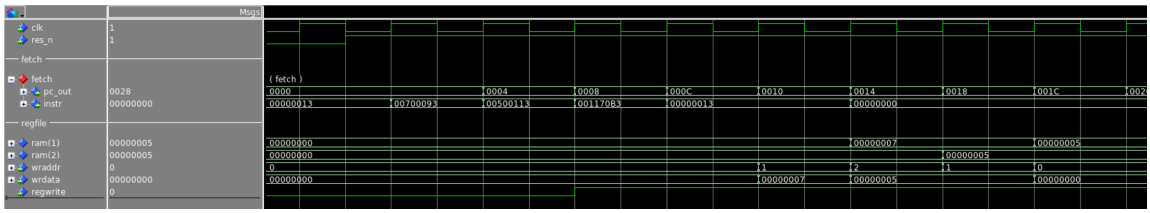

Figure 1: Simulation screenshot for Listing 1.

Make sure that at least the following signals are visible in Figure 1: the program counter in the fetch stage, the instruction being fetched, the content of registers `x1` and `x2` as well as the signals `wraddr`, `wrdata` and `regwrite` of the register file.

Listing 1: Assembler example with forwarding

```
addi x1, x0, 7
addi x2, x0, 5
and x1, x2, x1
nop
nop
```

Branch Hazards Simulation

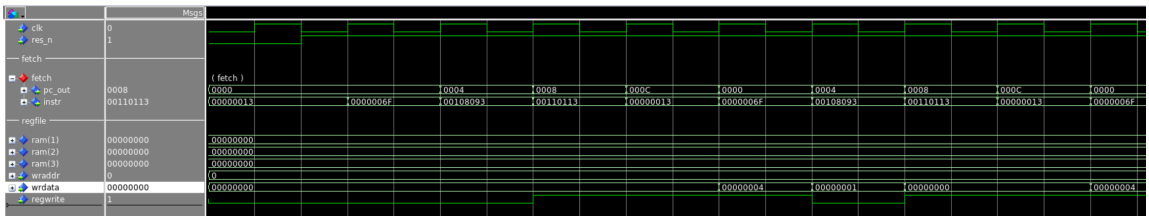

Figure 2: Simulation screenshot for Listing 2.

Make sure that at least the following signals are visible in Figure 2: the program counter in the fetch stage, the instruction being fetched, the content of registers `x1`, `x2` and `x3` as well as the signals `wraddr`, `wrdata` and `regwrite` of the register file.

Listing 2: Assembler example for branches

```
loop:   j loop
        addi x1, x1, 1
        addi x2, x2, 1
        addi x3, x3, 1
```

Cache Simulation

Table 1: Resource usage by entity, including resources used by sub-entities.

	LC Combinationals	LC Registers	Memory Bits
Fetch Stage	83	16	0
Decode Stage	443	209	2048
– Register File	232	162	2048
Execute Stage	1177	152	0
– ALU	696	0	0
– Forwarding Unit	10	0	0
Memory Stage	290	113	0
– Memory Unit	107	0	0
Write-Back Stage	106	88	0
Control Unit	24	20	0
Cache	636	380	0
Sum (core_inst)	2515	978	2048

Question: What is the maximum frequency of your design?

Answer: According to the compilation report, $f_{max} = 73.07MHz$ at 85Â°C with performance optimization turned on. When the critical path is excluded (see next answer) the new $f_{max} = 90.19MHz$.

Question: Where is the critical path of your design?

Answer: The critical path is the forwarding data path, from data memory through MEMU and MEM via the EXEC forwarding mux through the ALU bit shift combinatorial logic finally to the alu_next register in the MEM stage. BUT when this data path is activated, a stall is asserted by CTRL, so actually this path is not critical. When it is excluded, the next critical path is from the input register of EXEC via the FWD logic and aluB mux through the ALU bit shift logic to the alu_next register in the MEM stage.