Lesson EPSI-08-01 Download the pdf copy of the slides

Course EPSI: Essential Principles of Signal Integrity

With Eric Bogatin,
Signal Integrity Evangelist, Teledyne LeCroy Front Range Signal Integrity Lab
Dean, Teledyne LeCroy Signal Integrity Academy
Adjunct Professor, University of Colorado, Boulder, ECEE

- EPSI-08-01: recorded live, Dec 1, 2013
  - PDN and EMI design
  - Wrap up
  - Download a pdf copy of the slides by clicking on the link on this page

Lesson EPSI-08-10 Summary of the EPSI course

Course EPSI: Essential Principles of Signal Integrity

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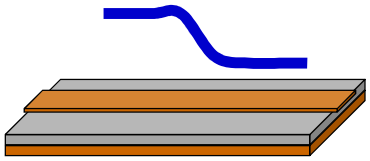
- EPSI-08-10: recorded live, Dec 1, 2013
  - The process to solve signal integrity problems
  - The 9 essential principles
  - The 10 habits of successful designers
  - The 6 families of SI problems

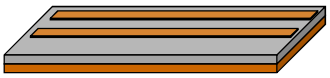
- Day 1
  - EPSI 1 Transmission Lines
  - EPSI 2 Differential Pairs and Lossy Lines
  - Lunch
  - EPSI 3 Reflections and Terminations
  - EPSI 4 Routing Topologies and Discontinuities
- Day 2
  - EPSI 5 Eliminating Ground Bounce
  - EPSI 6 Navigating Return Path Discontinuities
  - Lunch
  - EPSI 7 NEXT and FEXT Features
  - **EPSI 8 PDN and EMI Design**

Why Interconnects are Not Transparent:
The Six Families of Signal Integrity Problems

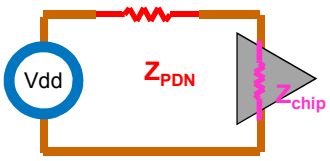


1. Reflection noise

2. Cross talk



3. Ground (and power) bounce
4. Losses (@ Gbps)
5. Rail collapse, voltage droop, power supply noise
6. EMI



The Nine Essential Principles of Signal Integrity

1. All interconnects are transmission lines
2. Signals are dynamic
3. Signals see an instantaneous impedance
4. Current propagates as a signal-return path loop with a direction of propagation and a direction of circulation
5. Reflections occur whenever the instantaneous impedance changes
6. Inductance is fundamentally about how efficient a conductor is in generating rings of magnetic field lines
7. Current in a conductor redistributes at higher frequency driven by minimizing loop inductance
8. Dielectric materials absorb electrical field energy causing attenuation
9. Common currents in conductors radiate and often cause EMC failures

The Ten Habits of Highly Successful Designers

1. Design all interconnects as controlled impedance and terminate when necessary
2. Minimize all branch lengths and stub lengths. Route with linear topology
3. Space out signals as far as possible, or at least 2 x the line width
4. Don't screw up the return path, or share return paths
5. Corollary to #4: Do not allow signals to cross gaps in return planes
6. Corollary to #4: Use return vias adjacent to EVERY signal via
7. Under 1 Gbps, use tightly coupled differential pairs, over 1 Gbps, consider loosely coupled diff pairs, with symmetrical lines
8. Use multiple power and ground planes on adjacent layers with thin dielectric between them, close to the surface
9. Use shortest, widest surface traces possible for decoupling capacitors, as close to via in pad as possible
10. Use enough total capacitance for low frequency and enough capacitors for low inductance at high frequency. Use simulation to optimize capacitor values to minimize peak impedance at parallel resonances

Lesson EPSI-08-20 Intro to the Power Distribution Network

Course EPSI: Essential Principles of Signal Integrity

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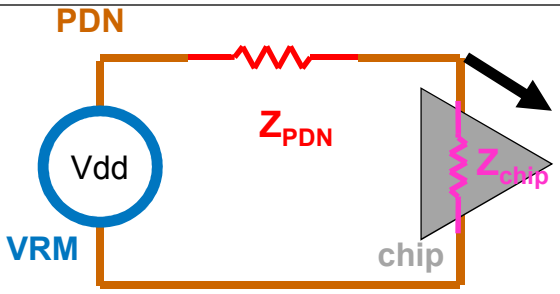
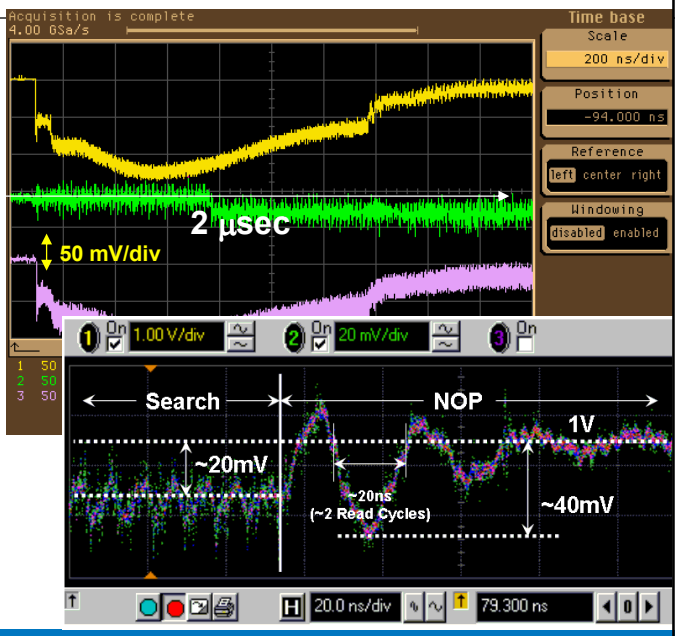
- EPSI-08-20: recorded live, Dec 1, 2013
  - The fundamental problem in PDN design and its root cause
  - The impedance profile and structures that influence it
  - The Bandini Mountain and why it is the most important problem
  - What it looks like when we get the PDN design correct

Identify the Problem: Rail Collapse

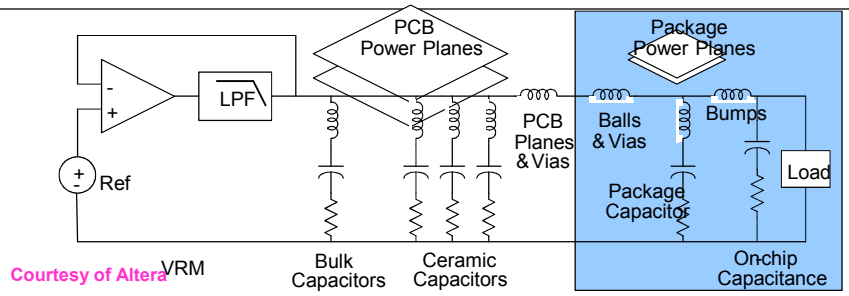


Voltage drop on the pads of the chip may exceed the noise threshold, will contribute to jitter

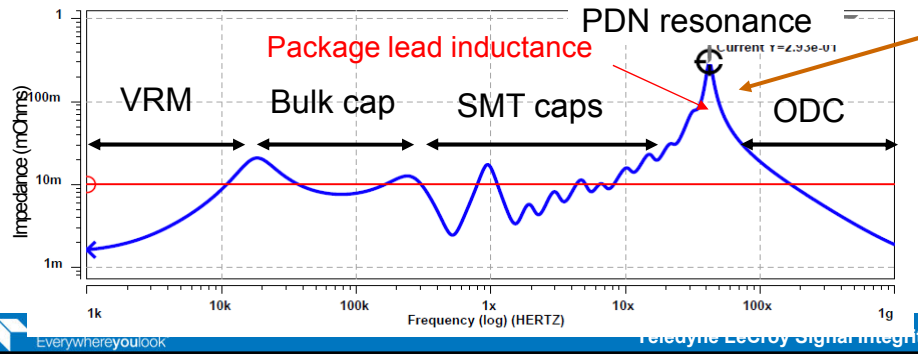
Design Goal: engineer the impedance of the PDN low enough to keep the rail collapse acceptable.



Features of the PDN

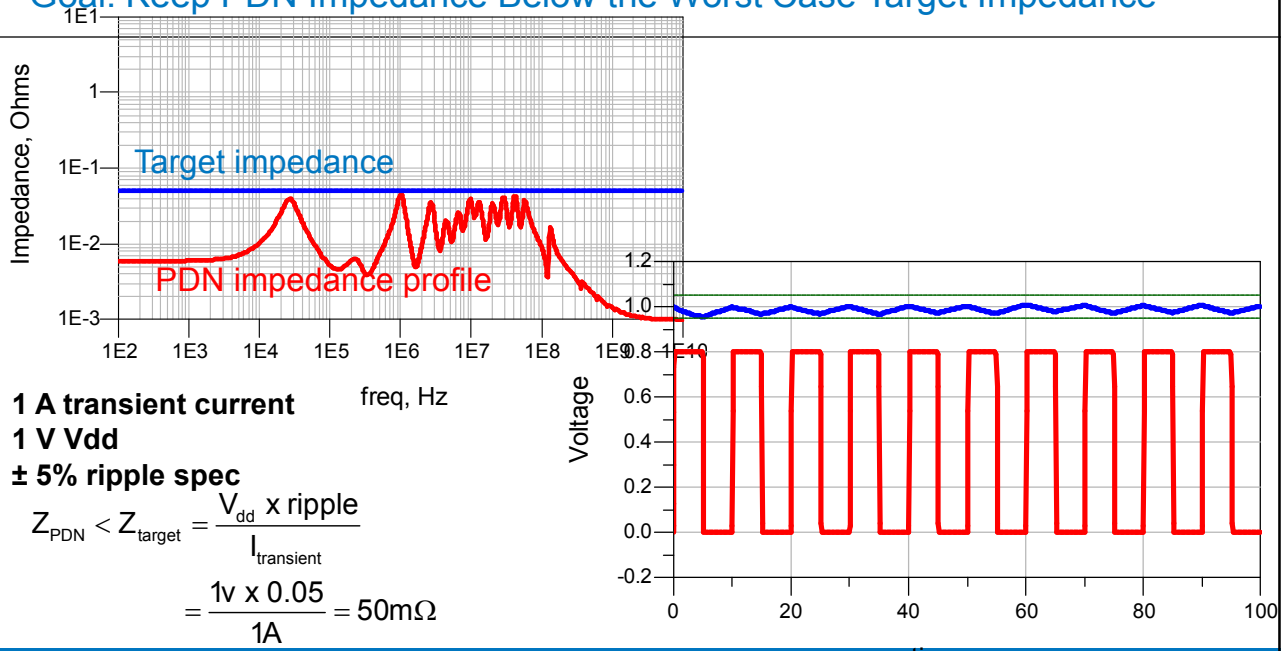


What we see looking into the PDN from the Chip's perspective



The "Bandini Mountain"

Goal: Keep PDN Impedance Below the Worst Case Target Impedance



1 A transient current
1 V Vdd
± 5% ripple spec

$$Z_{PDN} < Z_{target} = \frac{V_{dd} \text{ x ripple}}{I_{transient}}$$

$$= \frac{1v \text{ x } 0.05}{1A} = 50m\Omega$$

Lesson EPSI-08-30 The consequence of getting the PDN wrong

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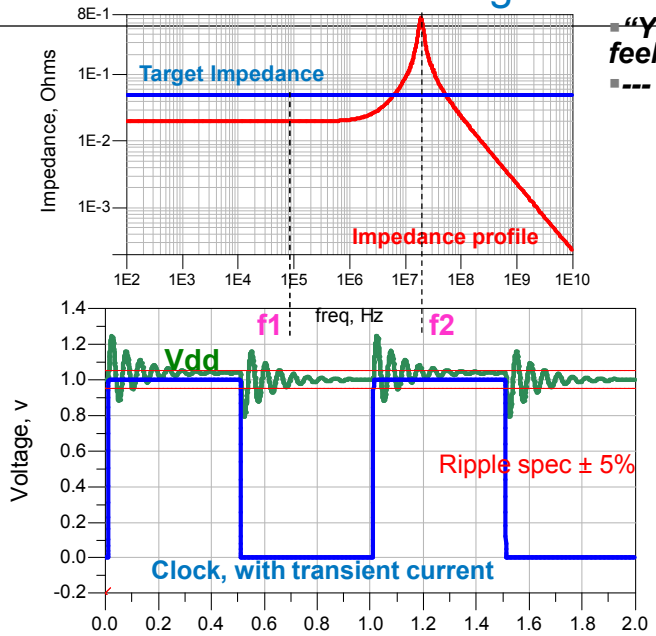
- EPSI-08-30: recorded live, Dec 1, 2013
  - What does a "bad" PDN impedance profile look like?
  - Why "bad" PDNs may still "work"
  - What it means to have a robust PDN design
  - Which is better, 3 capacitors the same value or 3 capacitors with different values

What if You Get it Wrong? "How Lucky Do You Feel?"

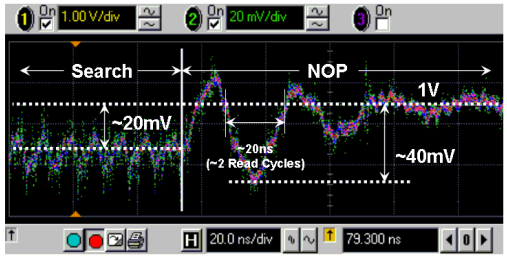


- ***"You've gotta ask yourself one question, do I feel lucky? Well, do ya, punk?"***
- ***--- Clint Eastwood as Dirty Harry***

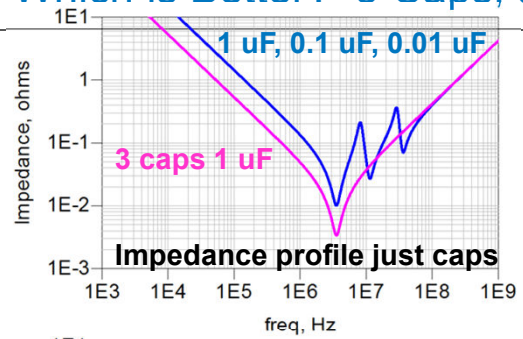
How lucky do you feel?

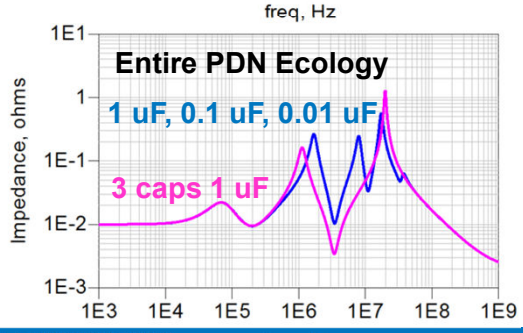
Golden Rule in PDN Design:

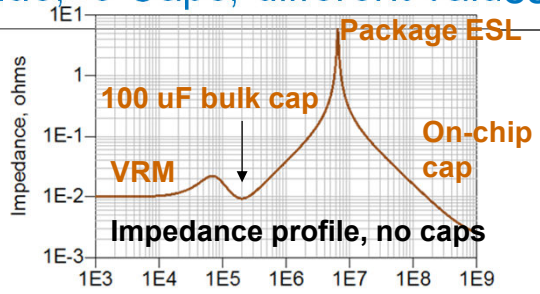
For robust PDN design, keep peak impedances below target impedance, across entire frequency range from DC to BW of signals



Which is Better? 3 Caps, same value, 3 Caps, different values







- Which is better?
  - The low impedance dips are irrelevant
  - The high impedance peaks are what can cause a problem
  - Both options may work, or they may not work
- Depends on
  - Spectrum of the current from chips
  - Noise sensitivity of the devices
  - How lucky you are
- Do you feel lucky?- how can you increase your luck?

Lesson EPSI-08-40 The Secret to a Robust PDN

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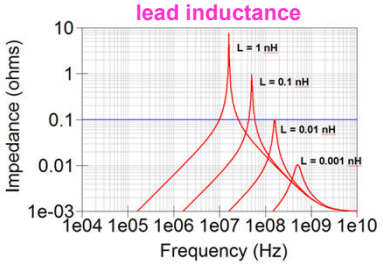
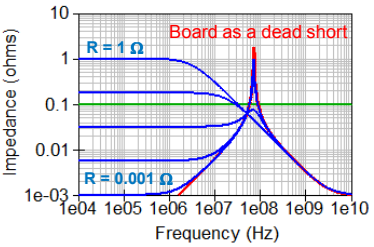
- EPSI-08-40: recorded live, Dec 1, 2013
  - A PDN with a board that has 1000 capacitors will still have a Bandini Mountain
  - How to reduce the Bandini Mountain if you can't change the package
  - Why the specific values of capacitors you choose is so important
  - The optimum selection of capacitor values

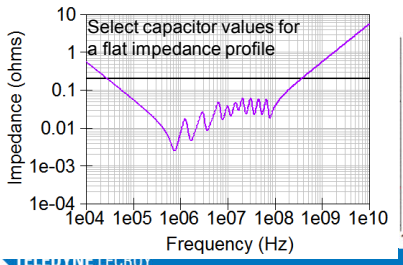
How to Reduce the Bandini Mountain?

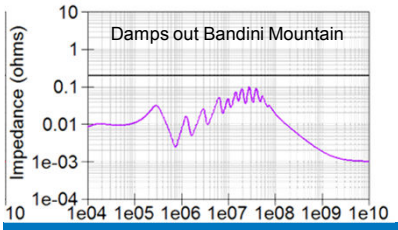
- Even if the board is a dead short, there is a Bandini Mountain @ ~ 10 MHz to100 MHz
- Reduce Bandini Mountain by
  - Higher on-chip capacitance
  - Lower package lead inductance
- What can be done at the board level?
  - Do everything possible to reduce the ESL of the capacitors- so it does not add to the package lead inductance
  - Make the board look like a resistor to damp out the parallel LC circuit
- How do you make the board look like a resistor?

Bandini Mountain: on-die capacitance and package lead inductance



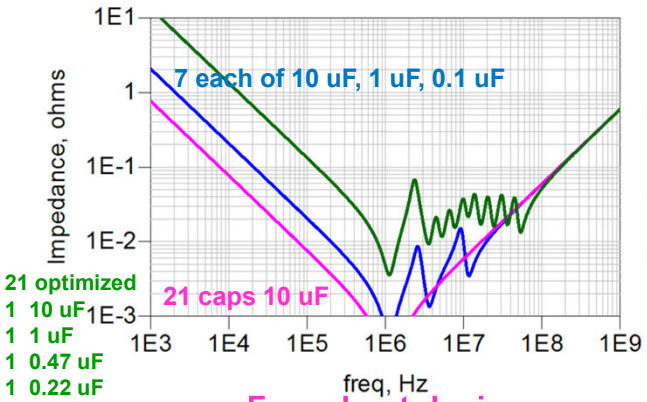




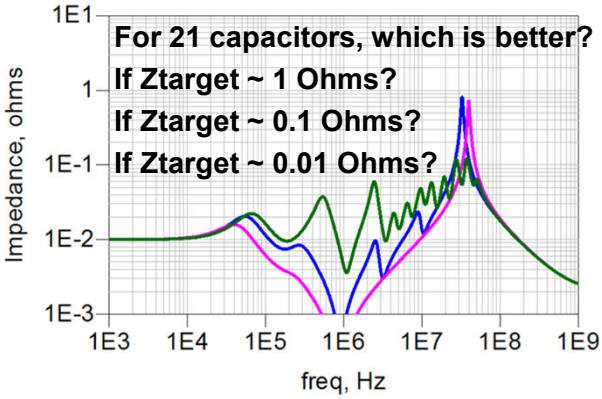


Increase Your Luck by Optimizing Capacitors for Flat Response

"You've gotta ask yourself one question, do I feel lucky? Well, do ya, punk? "
--- Clint Eastwood as Dirty Harry



21 optimized
1 10 uF
1 1 uF
1 0.47 uF
1 0.22 uF
1 0.1 uF
2 0.047 uF
3 0.022 uF
4 0.01 uF
7 0.0047 uF



- **For robust design:**
  - Reduce ESL
  - Engineer a flat impedance profile to damp out Bandini Mountain
  - Optimize N, capacitor values for peak impedance < Ztarget
  - The more on-package caps, the less you need on the board

Lesson EPSI-08-50 Steps to Reduce the Bandini Mountain

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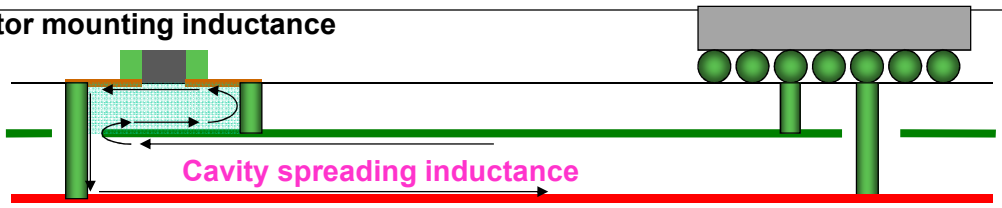
- EPSI-08-50: recorded live, Dec 1, 2013
  - Make the PDN look like a resistor to damp out peaks
  - Reduce the ESL of capacitors
  - The structures which contribute to ESL of capacitors
  - How to increase your luck in PDN design

Increase Your Luck by Reducing the ESL of the Capacitors

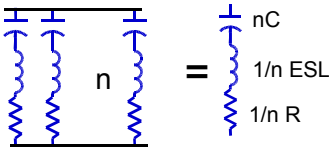
Capacitor mounting inductance



1st order effects: reduce capacitor mounting inductance
- Minimum length surface traces (fewer number of squares)
- Maximum width surface traces (fewer number of squares)
- Power and ground plane pair cavity, close to the surface
- Multiple capacitors in parallel (individual or IDC)

1st order effects: reduce cavity spreading inductance
- Minimum spacing between power and ground plane pairs

2nd order effects
1. Place capacitors in proximity to the package
2. Multiple via pairs per capacitor



Typical ESL values:
- **Poor design ~ 5 nH**
- **Ok design ~ 2 nH**
- **Good design ~ 1 nH**
- **Great Design ~ 0.5 nH**

How to Increase Your Luck and Decrease the Peak Impedances?

- If you don't simulate, it doesn't mean your product won't work. …you just won't know until you build it and test it – ***does your test suite include worst case?***
- Good habits to improve your luck:
  - Design lower ESL capacitor mounting
  - Select lower ESL capacitors: x2y, InterDigitated Capacitors (IDC)
  - Add more capacitors (reduces ESL)
  - Use higher ESR capacitors (damps resonances) (smaller value capacitors)
  - Use more different capacitor values (flatter response)
  - Optimize capacitor values (based on simulation)

Lesson EPSI-08-60 The most common sources of EMC Failures

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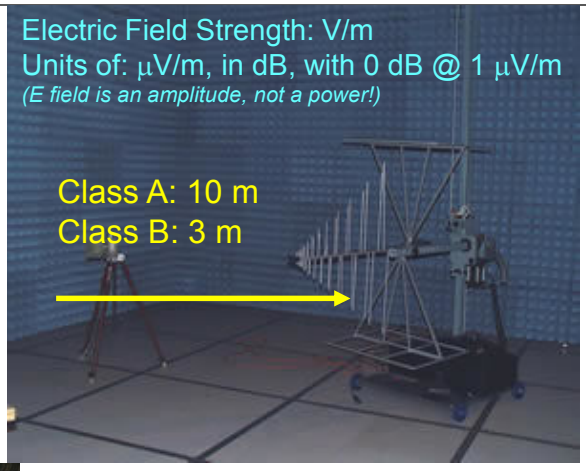
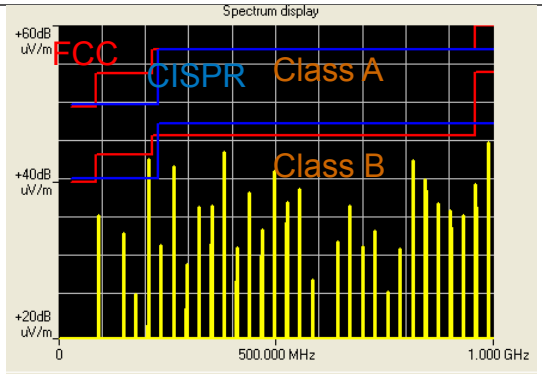
- EPSI-08-60: recorded live, Dec 1, 2013
  - FCC certification tests and what is needed to pass
  - The most important type of antenna: electric dipole
  - Estimating the amount of common current needed to fail an FCC test
  - How ground bounce contributes to EMC failures

Typical EMC Certification Testing



To be safe, keep E < ~ 100 μV/m



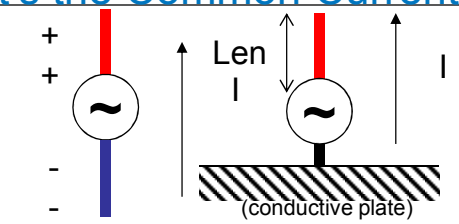
Class B- more sensitive:

Freq (MHz)	μV/m	dB μV/m
30-88	100	40
88-216	150	43.5
216-960	200	46
> 960	500	54

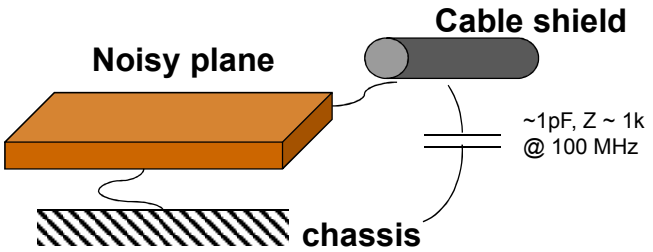
Strategy for Passing Certification Tests

- Identify the test specs and passing requirements
- Understand the fundamental antenna principles
- Manage source of radiating currents
  - Ground bounce, from signals and PDN
  - PDN differential noise in the planes
  - Resonances: packages, boards, enclosures
  - Connectors to external cables
  - Mode converted common currents on twisted pair cables
- Patch what can't be prevented
  - SSCG
  - Ferrites
  - Common mode chokes (magnetics)
  - Enclosures

Essential Principle #9:
It's the Common Currents that Radiate and Fail FCC Tests



Isolated dipole



$$E = 4\pi \times 10^{-7} \frac{f \times I \times Len}{R} = 0.4\ \mu V/m \times f \times I$$

$$I_{comm} = \frac{V_{comm}}{Z_{comm}} \sim \frac{0.1v}{1k\Omega} = 100uA$$

@ 100 MHz, Len = 1 m, E ~ 100 uV/m is FCC limit

f in MHz, I in microAmps

$$I_{max} = \frac{100uV/m}{0.4uV/m \times 100MHz} = 3uA$$

Only takes ~ 3 uA common current to fail FCC!

Lesson EPSI-08-70 Reducing EMC problems with connectors

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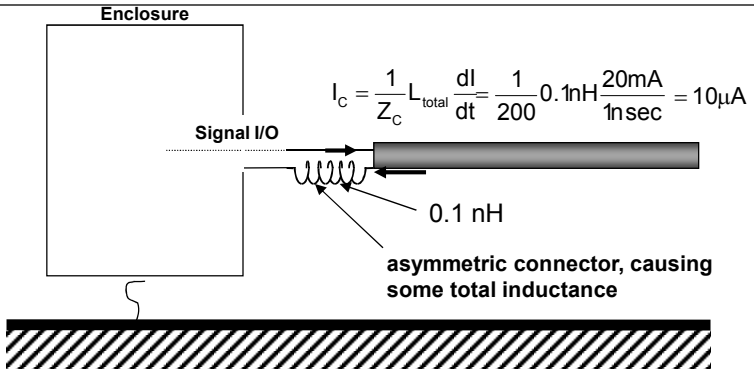
- EPSI-08-70: recorded live, Dec 1, 2013
  - How connectors contribute to FCC failures
  - How to engineer a good connector
  - How ferrites help to reduce radiated emissions
  - Summary of the 6 families of problems and the 9 essential principles

Radiated Emission from Cables Really Comes from the Connectors



- Asymmetrical connector causes total inductance in return path
- Return current through total inductance causes voltage noise
- Voltage noise drives common currents in cable
- Cable radiates

Common Currents and Connector Quality

Relationship between Connector Contact Points and Common-Mode Current on a Coaxial Transmission Line

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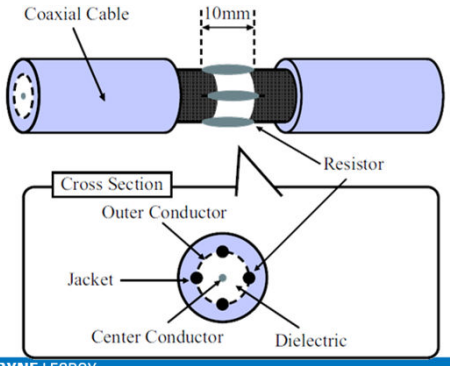
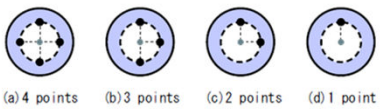
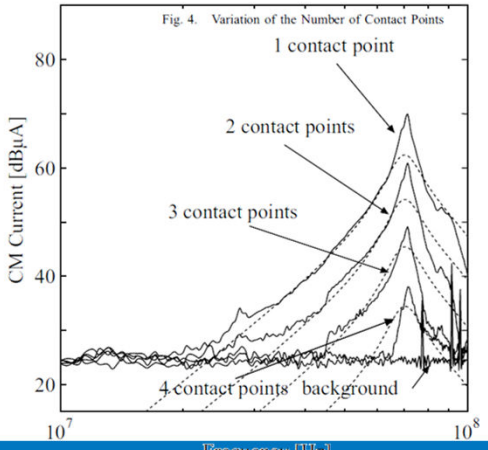
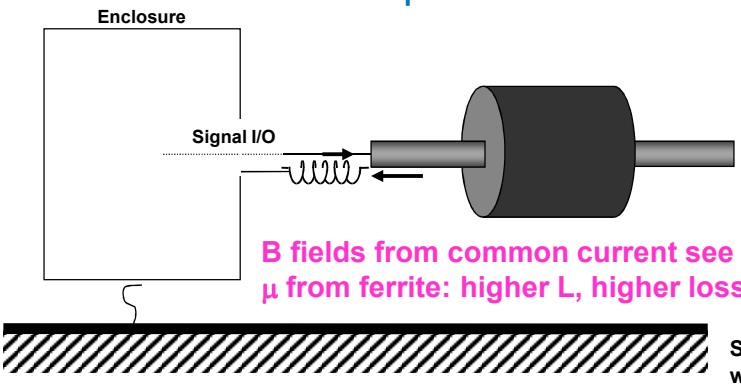


IEEE EMC Symposium 2009

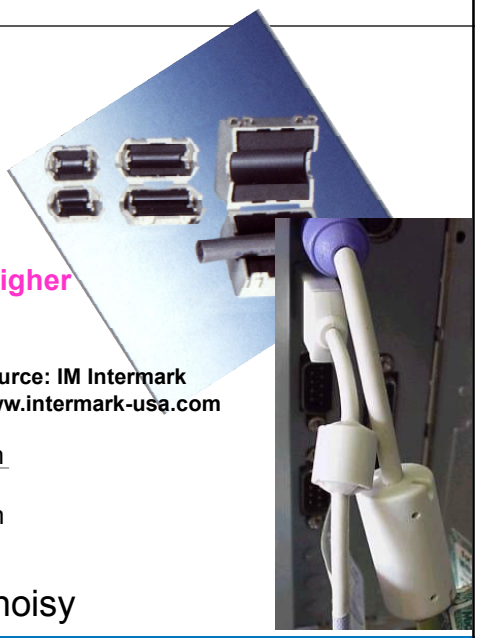




Addition of a Ferrite Choke Will Increase the Impedance of the Common Current Loop



B fields from common current see higher μ from ferrite: higher L, higher loss



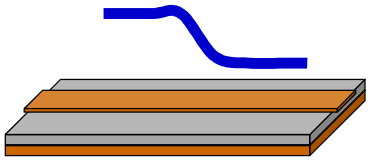
Source: IM Intermark
www.intermark-usa.com

Impedance of the CM current path is increased.
CM current on the external cable is reduced

$$I_{cm} = \frac{V_{cm}}{Z_{cm}}$$

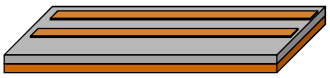
1. Place as close as possible to the connector
2. Can be used on both ends if both boxes are noisy

Why Interconnects are Not Transparent:
The Six Families of Signal Integrity Problems

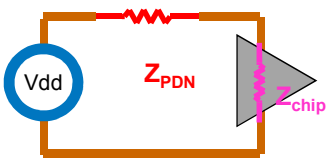


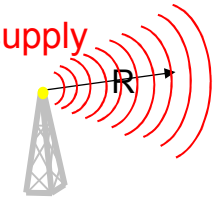
1. Reflection noise

2. Cross talk



3. Ground (and power) bounce
4. Losses (@ Gbps)
5. Rail collapse, voltage droop, power supply noise
6. EMI





The Nine Essential Principles of Signal Integrity

1. All interconnects are transmission lines
2. Signals are dynamic
3. Signals see an instantaneous impedance
4. Current propagates as a signal-return path loop with a direction of propagation and a direction of circulation
5. Reflections occur whenever the instantaneous impedance changes
6. Inductance is fundamentally about how efficient a conductor is in generating rings of magnetic field lines
7. Current in a conductor redistributes at higher frequency driven by minimizing loop inductance
8. Dielectric materials absorb electrical field energy causing attenuation
9. Common currents in conductors radiate and often cause EMC failures

The Ten Habits of Highly Successful Designers

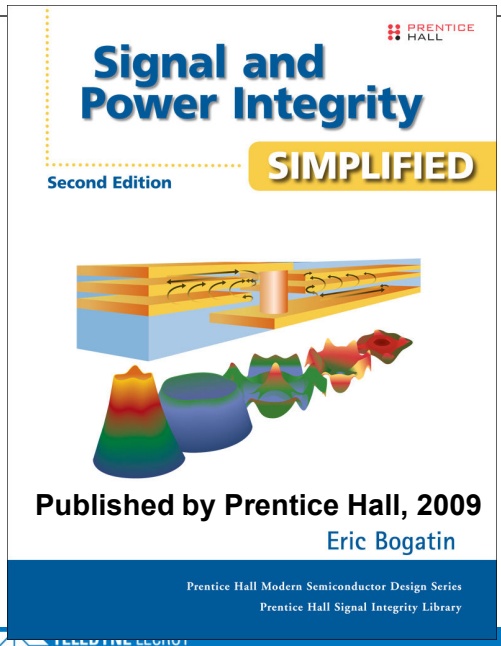
1. Design all interconnects as controlled impedance and terminate when necessary
2. Minimize all branch lengths and stub lengths. Route with linear topology
3. Space out signals as far as possible, or at least 2 x the line width
4. Don't screw up the return path, or share return paths
5. Corollary to #4: Do not allow signals to cross gaps in return planes
6. Corollary to #4: Use return vias adjacent to EVERY signal via
7. Under 1 Gbps, use tightly coupled differential pairs, over 1 Gbps, consider loosely coupled diff pairs, with symmetrical lines
8. Use multiple power and ground planes on adjacent layers with thin dielectric between them, close to the surface
9. Use shortest, widest surface traces possible for decoupling capacitors, as close to via in pad as possible
10. Use enough total capacitance for low frequency and enough capacitors for low inductance at high frequency. Use simulation to optimize capacitor values to minimize peak impedance at parallel resonances

"Mr. Osborne, may I be excused? My brain is full."

Rule #9: Never do a measurement or simulation without first anticipating what you expect to see.

- If you are wrong, there is a reason- either the set up is wrong or your intuition is wrong. Either way, by exploring the difference, you will learn something
- If you are right, you get a nice warm feeling that you understand what is going on.

For More Information



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- Teledyne LeCroy Signal Integrity Academy
- Other signal integrity classes