Blackhawk – Analog Module Specification (AMS)

3.75 – 56.4 Gb/s PAM4/NRZ SerDes Transceiver, 16nm FinFet+ Process

ANA_BLACKHAWK_8X_TS16FF_S5, ANA_BLACKHAWK_4X_PLL2X_TS16FF_S6

Version 1.02 – February 17, 2017

Metal Stackup 13ML, 11ML – A0

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1. Key Features

- Based on the Falcon16 PMD core, but with the major changes listed in Sec 4 to support ~56G PAM4 with an octal floorplan
- Supports new PAM4 modes and all legacy, NRZ line rates and standards between 15.0 and 28.3 Gb/s, plus half and quarter rates. Any rates lower than 3.75 Gb/s, e.g. 1.25 Gb/s, have to be enabled with over/under sampling in the digital core
- An independent lane mode is now fully supported with clk muxes in the RX and TX
- See the Electrical Spec section for a list of standard's compliance
-
- Programmable 3-stage RX equalizer with 0-TBD dB boost, approx 0.5 dB/step.
- 14-tap DFE with adaptive control and VGA with AGC
- Full range H and V eye diagnostics supported by a 3rd phase interpolator
- Quarter rate, peak, zero and error slicing with 1:20 de-serializer receiver.
- Transmitter with fully programmable 7-bit DAC, and large swing driver
- One phase interpolator per TX lane to support individual lane loop timing
- Internal PLL with wide tuning range, 15.0 – 30 GHz.
- Dual VCO architecture with clock phase interpolation in receiver timing recovery.
- Programmable PLL feedback divider with 5-bit control, plus a fractional-N mode
- Input reference frequency, typically 312.5, 156.25 or 125 MHz. Can select from between an external or an internal reference clock source
- Includes AC-JTAG test circuits for both RX and TX
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- Circuit die area, 4.16 mm^2 (est) for an octal lane core, 8 RX/TX + 2 PLL
- Power per RX/TX lane with shared PLLs at ~53 Gb/s, LR mode, 230 mW typ (est)
- Main supply voltage ~0.8+ V, typical (+/-3% tolerance at pkg/PCB interface)
  - Might require AVS or higher supply, +3%, for SS process corner
- TX driver supply voltage 1.20 V, typical (+/-5% tolerance at pkg/PCB interface)
- 16 nm FinFet+, FFP, process, flip chip (FC) package only
- Supported metal stack-ups are 13ML and 11ML with 2Mr

2. AMS Revision History

Version	Date	By	Changes
1.02	Feb 17, 2017	Anthony Brewster	- add refclk1x, DFE summer BW +12% - update VCO tuning and test port control desc for refclk, Vbg - more detail for power and current
1.01	Oct 10, 2016	“” “”	- add summary table with all output clocks - update 8X and 4X core block diagrams - misc updates to a few rx_ctrl bits
1.0	July 22, 2016	“” “”	New for post-Sinai version - add RX and TX 66T clocks - expand modes for clk4pcs - add 6T mode to clk4sync - prelim info for 4X version Misc general updates for pre/post Sinai - set max RX Vin = 1.1 V - define use of pll_ctrl<73:72> - add M and A formulas for frac-N bypass - update misc TX info and bits - misc integration info from FC16 ver 1.1
0.99	May 12, 2016	“” “”	- set default for clk rptr buffers to ON for “0” - prelim info for frac-N bypass mode - use rx_ctrl<46> to program VGA3 inductor
0.98	Mar 29, 2016	“” “”	- update area - define pll_ctrl<175:160>
0.97	Feb 11, 2016 Feb 10, 2016	“” “”	- swap misc rx_ctrl bits - increase DFE tap-4 to <4:0> - update data slicer assignments per emails - remove TX FIFO pins - update AMS ctrl for RX, TX and PLL
0.96	Dec 2, 2015	“” “”	- add 16-bits to rx_ctrl - add HF peaking filter - add pwr/gnd for RX/TX clk buffer block - enable refout buffer to use lcref input - add DAC code 16d for Elec Idle and reset - match misc info from Falcon16 AMS
0.95	Oct 16, 2015	”” “”	Final changes for test chip version - expand RX data and phase slicer thresholds for PAM4 - RX FFE code range to approx. +/-40 - PF control to 5-bits - add one bit to DC offset calibration range - misc update to SD cal - TX PI to 5-bits - add 2-bit rescal for TX driver - use Vdiff for Vthresh in PLL - add 16-bits for PLL control - max line rate = 28.3G, not 30G - placeholder output for “SYNC” clock - fix misc typos
0.92	Sep 23, 2015	“” “”	Intermediate version, prelim for Oct 1 - Remove old Yellow highlighting from F16 - Correct suffix to S5 for 13ML and match IPX - Slicer offset coding - RX FFE, clkmux, SD cal - PLL vco res cs, Vthresh = 50mV, PTAT/CTAT tables - TX block diagram
0.90	Aug 1, 2015	“” “”	Modified from Falcon16 AMS, ver 0.99 and Falcon16 with 2PLL AMS, ver 0.90 - Update many sections with BH octal info - Prelim floorplan, power and area

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4. Major Changes from Falcon16 PMD/RPTR and PLL2X A0 – AMS ver 0.90

General
Add support for 50G PAM4 signals, but the final line rates depend on the usage channels and FEC overhead
Tentative max line rate is ~56.4 Gb/s
Add prelim support for IEEE 802.3bs 400G std, aka CDAUI
Retain support for all 25G and 10G NRZ modes in Falcon16
Lower power modes for short reach and lower speeds, eg 50G PAM4 SR/MR, VSR
Octal floorplan with side by side quad cores and added clock buffers
Remove support for the low latency mode
Internally, built as two quads for easier development of a single quad
Available process and metal stackups, 16FFP with 13ML and 11ML, both with 2Mr

PLL
Add 2nd PLL and buffers
Keep all PLL modes, eg frac-N and refclk re-distribution, from Falcon16
Lower the jitter to improve the PAM4 mode performance
Using refclk = 312.5 MHz is recommended for lower jitter
Add 300 and 400 ohm termination options for external refclk inpus
Misc control bit and default changes
Add high freq Nano Sync clock outputs
Add mux for refout to select from refclk bumps, or lcref channel, or integer divider output

RX
Add five more slicers to enable support for PAM4 LR and MR/SR
Power down modes to reduce power for lower performance modes
Add a per lane mux to select a clock from either PLL
Keep 32T clock output from F16 PLL2X core
Add 3-tap FFE, used mainly for LR channels and with the ES slicer mode
Add control bits for signal detect calibration
Add a 3rd peaking filter to extend freq range

TX
Change driver design to a true 7-bit DAC, and move the FIR to the PMD logic
Add a per lane mux to select a clock from either PLL
LDO bypass option for lower power and only one TX power supply, 0.8V
Keep 32T clock output from F16 PLL2X core

AMS WIP
Add new block diagrams and descriptions
Misc electrical specs
More detailed descriptions

5. Top Level Cell Names and Versions in IMP and IPX

ANA_BLACKHAWK_8X_TS16FF_S5
13ML with 2Mr

Test
A0 – A0_prelim_22, with MIM caps, and A0_prelim_23, without MIM caps
Chips – Sinai test chip in late June 2016

Production, height reduced
A0 – A0_patch_0
Chips – Ramon, Jericho2, OP2, TH3

ANA_BLACKHAWK_8X_TS16FF_S6
11ML with 2Mr

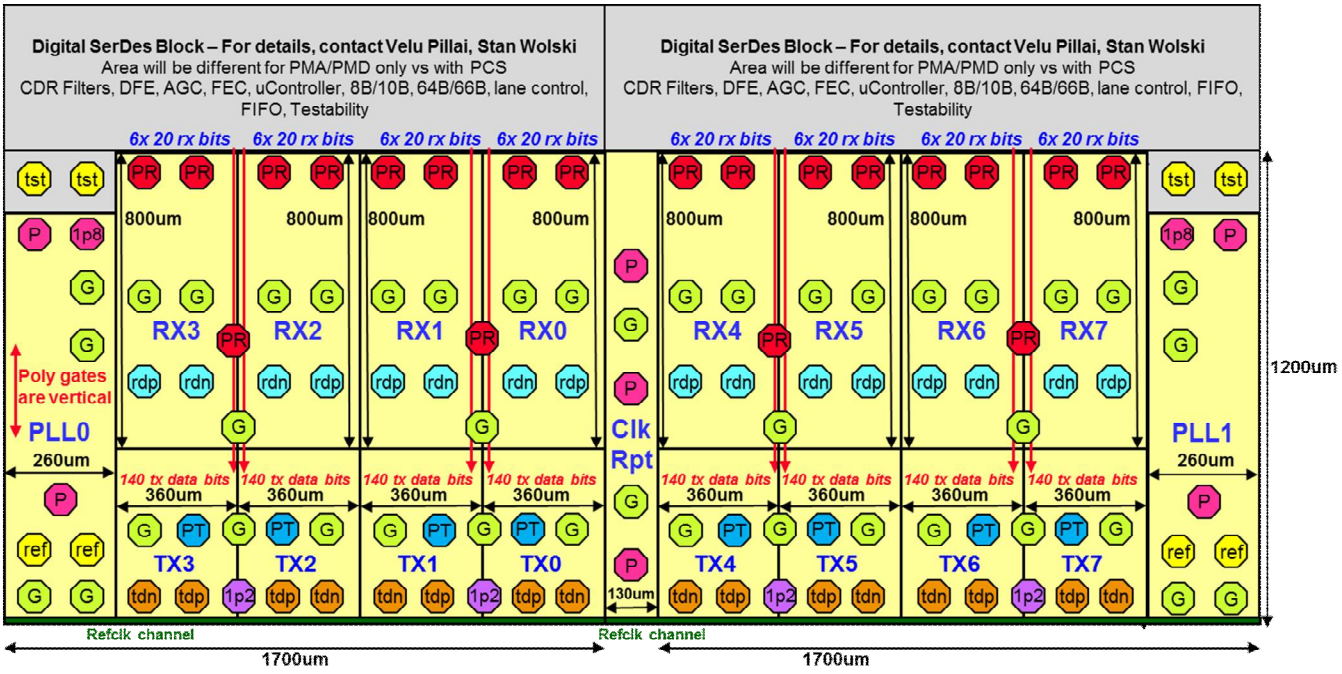
Based on 13ML Ramon version

Production
A0 – A0_patch_TBD
Chips – Barchetta

ANA_BLACKHAWK_4X_PLL2X_TS16FF_S6
11ML with 2Mr

Production
A0 – A0_patch_0
Chips – Estoque, coherent products

6. **Top Level Block Diagram and Layout –** This AMS covers only the blocks in yellow, and all the dimensions and bump locations are final for the production A0 version. Note that lanes 3 and 1 flipped are flipped around the vertical axis. Based on a request by the pkg and SI teams, the upper pair of P/G bumps in each PLL has been swapped. The middle clock repeater buffer, width 130 um, between the two quad cores is now included. The 4X version is shown on the next page.



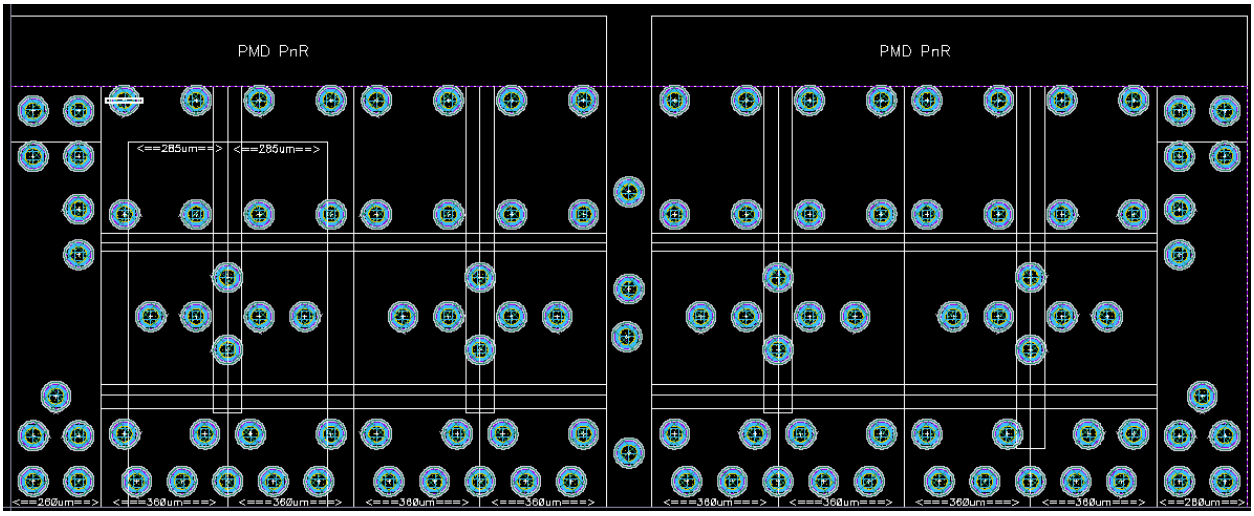
All units in diagram above are um, drawn and physical, as there is no optical shrink for 16 nm. The width = 3530 um, height = 1200 um, and area, ~4.16 mm^2. As shown above, the height of the PLLs is only ~1055 um. For future versions, there is a possibility of reducing the height of the RX/TX lanes by ~6%, but this is TBD pending test results and a formal request for a change. All the poly gates are in the vertical direction, and min bump pitch = 130 um.

The lcrefp/n_h pins, M13, are located along the left, bottom edge at approx X = 8 um.
The refout pins are located in the middle of each PLL at approx X, Y = 93 um, 264 um. The horizontal refclk channel is included in the IP because it is used to supply the same refclk signal to both PLLs.

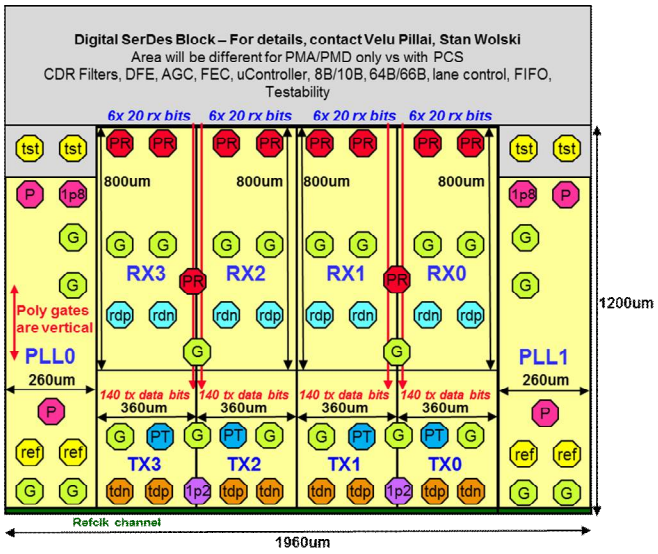
For cores that are placed on the vertical edges of a chip, a better location for the refclk channel is along the left edge of the core. This location will minimize the routing length and parasitic capacitance. Due to a DRC rule for bump to die edge spacing, a 25um gap must be made between the left edge of the IP and a die edge. This space can be used for a low jitter refclk channel to connect multiple cores, and which does not cross any digital sections.

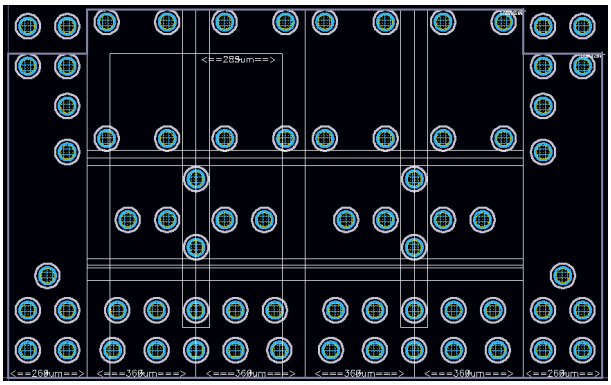
All the needed TX ctrl and data pins are brought to the ana/dig interface at the top of the analog along the left edge of RX/TX lanes 2 and 0, and the right edges of RX/TX lanes 3 and 1. There are ten locations along the top edge for the ESD related bbd2core<9:0> pins (UTRDL), which must be well connected to the digital VSS mesh and bumps. The 4X version has six similar connections.

The bump map for side-by-side octal with a clock buffer channel in the middle is shown below.



The 4X version with 2 PLLs is shown below. The width is 1960 um, and like the 8X version, there are ~150 um notches above the PLLs.





7. Flip Chip Bump List

I/O	Pad name	Description
I	pad_pll0_pvdd0p8	PLL supply voltage, 0.8 V Typical Current = 96 mA, Power down ~= 1 mA
I	pad_pll0_pvdd1p8	PLL supply voltage, 1.8 V, used for bandgap Typical Current = 0.5 mA
I	pad_pll0_pgnd	PLL ground
I	pad_pll1_pvdd0p8	PLL supply voltage, 0.8 V Typical Current = 96 mA, Power down ~= 1 mA
I	pad_pll1_pvdd1p8	PLL supply voltage, 1.8 V, used for bandgap Typical Current = 0.5 mA
I	pad_pll1_pgnd	PLL ground
I	pad_rvdd0p8	Receiver supply voltage, 0.8 V Typical Current = 8 x 200 mA
I	pad_rgnd	Receiver ground
I	pad_tvdd0p8	Transmitter supply voltage, 0.8 V Typical Current = 8 x 35 mA
I	pad_tvdd1p2	TX driver supply voltage, 1.2 V, but can be connected to 0.8 to ~1.0 V in certain cases to save power and simplify a PCB design Typ Current = 8 x 18 mA
I	pad_tgnd	Transmitter ground
I	pad_clkvdd0p8	Supply voltage, 0.8 V, for RX/TX clock repeater buffers between quads in 8X version Typical Current = 100 mA, Power down ~= 1mA
I	pad_clkgnd	Ground for RX/TX clk buffers between quads pad_clkvdd0p8 and pad_clkgnd are not used in the 4X version
		The above current values are typical for 50G PAM4 LR, ie 26.56 GS/s. For each supply domain, the max current is approx 20-25% higher than typical and assuming no use of AVS or process control. The power is lower for some other modes such as 25G and 10G NRZ, and the details are in the Electrical Specification section.
		The power supplies should not be connected to GND in the pkg or PCB without checking with the IO team for any latch-up or floating gate issues.
I	pad_pll0_refclkp	PLL reference clock input, typically 156.25 MHz, but 312.5MHz is recommended for lower jitter. The refclkp/n signals must be AC coupled with external, 10nF or larger, capacitors. If not used, can be left floating or tied to AGND, which can simplify the pkg routing.
I	pad_pll0_refclkn	PLL reference clock input, complement

I	pad_pll1_refclkp	PLL reference clock input, typically 156.25 MHz, but 312.5MHz is recommended for lower jitter. In many cases, the refclkp/n signals must be AC coupled with external, 10nF or larger, capacitors. If not used, can be left floating or tied to AGND, which can simplify the pkg routing.
I	pad_pll1_refclkn	PLL reference clock input, complement
I	pad_rdp*i*	Receiver *i* input data If not used in a pkg, tie P and N together per lane, and leave each combined node floating
I	pad_rdn*i*	Receiver *i* input data, complement
O	pad_tdp*i*	Transmitter *i* output data If not used in a pkg, leave floating
O	pad_tdn*i*	Transmitter *i* output data, complement
O	pad_pll0_ptestp	PLL / Receiver analog test port, also see Sec 36 for more details about the use of the test port
O	pad_pll0_ptestn	PLL / Receiver analog test port, complement
O	pad_pll1_ptestp	PLL / Receiver analog test port, also see Sec 36 for more details about the use of the test port
O	pad_pll1_ptestn	PLL / Receiver analog test port, complement
I	bbd2core[9:0] for 4X bbd2core[5:0]	Not an actual pad/bump pin, but ESD related, and should be well connected to the serdes digital GND mesh, and as close as possible to a VSS bump. These pins are the “digital side” of the ESD back2back diodes between the analog and digital GNDs.
Receiver / Transmitter: i = [7:0]		

8. Control and Status Register Bit Map – placeholder from Falcon16, and might be removed to avoid duplication with the text descriptions in the *ctrl* sections

Register Map for ANA_FALCON16_TS16FF_S5/S6 A0 Production

Green indicates default '1', yellow indicates default '0', and changes vs 28nm Falcon RPTR/FC are in bright yellow

pll_ctrl[159:0], 16'h	159	158	157	156	155	154	153	152	151	150	149	148	147	146	145	144
0xD119, 0000	fracn_sel	ditheren	fracn_ndiv_int<9:0>										fracn_bypass	fracn_divrange	fracn_div<17:16>	
	143	142	141	140	139	138	137	136	135	134	133	132	131	130	129	128
0xD118, 0000	fracn_div<15:0>															
	127	126	125	124	123	122	121	120	119	118	117	116	115	114	113	112
0xD117, 2700	Mix3P1CR_PTAT[4:0]					Mix3P1CR_CTAT[4:0]					reserved	reserved	reserved	reserved	reserved	reserved
	111	110	109	108	107	106	105	104	103	102	101	100	99	98	97	96
0xD116, 0000	refclk_doubler	doubler_res<2:0>			reserved	doubler_cap<2:0>			reserved	reserved	reserved	TBD	TBD	refclk_div4	refclk_div2	Rterm200
	95	94	93	92	91	90	89	88	87	86	85	84	83	82	81	80
0xD115, 2700	Mix3P1CcalR_PTAT[4:0]					Mix3P1CcalR_CTAT[4:0]					test_pnp<1:0>		vbypass	bgint	bgip	tp_max_amp
	79	78	77	76	75	74	73	72	71	70	69	68	67	66	65	64
0xD114, 0077	force rescal	force_kvh_bw	kvh_force[1:0]		vddr_bgb	test_vddr4bg	pll2rx_clkbw[1:0]		ctatadj[3:0]				ptatadj[3:0]			
	63	62	61	60	59	58	57	56	55	54	53	52	51	50	49	48
0xD113, 0000	test_rx	test_pll	test_vc	test_vref	itest[2]	itest[0]	itest[1]	icomp[2]	icomp[0]	icomp[1]	icmldiv[2]	icmldiv[0]	icmldiv[1]	irxclkbuf[2]	irxclkbuf[0]	irxclkbuf[1]
	47	46	45	44	43	42	41	40	39	38	37	36	35	34	33	32
0xD112, 000F	ick[2]	ick[0]	ick[1]	icp[2]	icp[0]	icp[1]	ibmax	ibmode	ibmin	refh_pll	refl_pll	vdd88_en	iqp<3:0>			
	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
0xD111, 8004	enable_ftune	pll_reset	ivco[2]	ivco[0]	ivco[1]	test_vco2_cssw	VCOIctrl[1:0]		vco2_15g	vco_autogm	vco_res_cs	reserved	drv_hv_disable	comp_thresh<2:0>		
	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0xD110, 0200	rescal_aux[3:0]				reserved	lpf_Rz<1:0>		fp3_rh	fp3_ctrl<3:0>				cp_cmfdbk_iadj<1:0>		set_clk4pcs<1:0>	

pll_sts[15:0]	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0xD11C	kvh[1:0]		pll_range[7:0] - contains VCO tuning code								pll_low	pll_Ndiv[4:0], copy of pll_mode[4:0] bits				

tx*i*_ctrl[63:0]	63	62	61	60	59	58	57	56	55	54	53	52	51	50	49	48
0xD0D3, 0000	reserved	reserved	reserved	reserved	reserved	reserved	reserved	pdet_ll_clk	sel_txmaster	sel_ll	pdet_mode[1]	pdet_mode[0]	sel_fifo_pol	fifo_depth<2:0>		
	47	46	45	44	43	42	41	40	39	38	37	36	35	34	33	32
0xD0D2, 000F	Elec_Idle	fir_tap_load	sign_post1	sign_post2	post2_coef[3:0]				sign_post3	post3_coef[2:0]			slew_rate	reserved	hpf_ctrl<1:0>	
	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
0xD0D1, 2000	txclk32_en	pulse_polarity	ldo_vref<1:0>		ildo [mode, max, min]			icml [mode, max, min]			iphint [mode, max, min]		ibias, master [2:0, mode, max, min]			
	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0xD0D0, 00C0	rescal_aux[3:0]				rescal_off	dcc_dis	dcc_sel	vddr_bgb	ticksel[1:0]		test0011	test0101	skew_enable	skew polarity	skew_pn<1:0>	

tx*i*_sts[15:0]	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0xD0D9	tx_lane_id[1:0]		reserved	drv_hv_disable	ana_rescal[3:0]				**Version ID = A**				**Version ID = 0**			

rx*i*_ctrl[159:0]	159	158	157	156	155	154	153	152	151	150	149	148	147	146	145	144
0xD0C9, 0300	data12T_ll_en	d2c_clk_buf (ibias - max, mode, min)			sel_d2clp	reserved	clk_bw_ctrl<1:0>		en_tapdelay<1:0>		dac4ck_dat_q[2:0]		dac4ck_dat[2:0]			
	143	142	141	140	139	138	137	136	135	134	133	132	131	130	129	128
0xD0C8, 0x0000	reserved	reserved	dac4ck_phs_q[2:0]			dac4ck_phs[2:0]			reserved	reserved	dac4ck_lms_q[2:0]			dac4ck_lms[2:0]		
	127	126	125	124	123	122	121	120	119	118	117	116	115	114	113	112
0xD0C7, 0x0000	vga_step<1:0>		VGA low gain[1:0]		reserved	VGA short	dc_offset_pd	dcoff_2x	dcoff_force	dc_offset[6:0]						
	111	110	109	108	107	106	105	104	103	102	101	100	99	98	97	96
0xD0C6, 0x0000	eq_pkcomp_dis	eq_ind_dis	vga_bw_ctrl<1:0>		cml_lp	dfesum_lp	vsr_nodfe	rxclk32_en	offset_correction_rescal_mux (force, ctrl[3:1])				peaking_filter_rescal_mux (force, ctrl[3:1])			
	95	94	93	92	91	90	89	88	87	86	85	84	83	82	81	80
0xD0C5, 0x0000	sd_cal_en	testclk_mux	testclk_div<1:0>		sd_cal_polarity	sd_cal_pos[2:0]			sd_cal_neg[2:0]			VGA2_rescal_mux (force, ctrl[3:0])				
	79	78	77	76	75	74	73	72	71	70	69	68	67	66	65	64
0xD0C4, 0x0000	VGA1_rescal_mux (force, ctrl[3:0])				VGA0_rescal_mux (force, ctrl[3:0])						TBD (ibias - max,mode,min)			reserved	reserved	reserved
	63	62	61	60	59	58	57	56	55	54	53	52	51	50	49	48
0xD0C3, 0x0000	reserved	DFE slicer (ibias - max,mode,min)			DFE sum (ibias - max,mode,min)			DC_offset (ibias - max, mode, min)			DLL (ibias - max,mode,min)			Vthresh_Rmet (ibias - max,mode,min)		
	47	46	45	44	43	42	41	40	39	38	37	36	35	34	33	32
0xD0C2, 0x0E00	pd_ftap	sigdet_10g	pd_ch_p1	sel_th4dfe<1:0>		dfe_sumbw<1:0>		DFE tap (ibias - max,mode,min)			phase interp (ibias - max,mode,min)			sigdet (ibias - max,mode,min)		
	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
0xD0C1, 0x0000	input Vcm (ibias - max,mode,min)			reserved	reserved	reserved	VGA2 (ibias - max,mode,min)			VGA1 (ibias - max,mode,min)			VGA0 (ibias - max,mode,min)			resereved
	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0xD0C0, 0x0010	peak filter (ibias - max,mode,min)			DC couple	dfe_hgain_en	eq_lz_en	vga_10g_bw	tport_en	sigdet_byp	sigdet_pd	offset_ctrl[2:0], Gray code			master diodes (ibias - max,mode,min)		

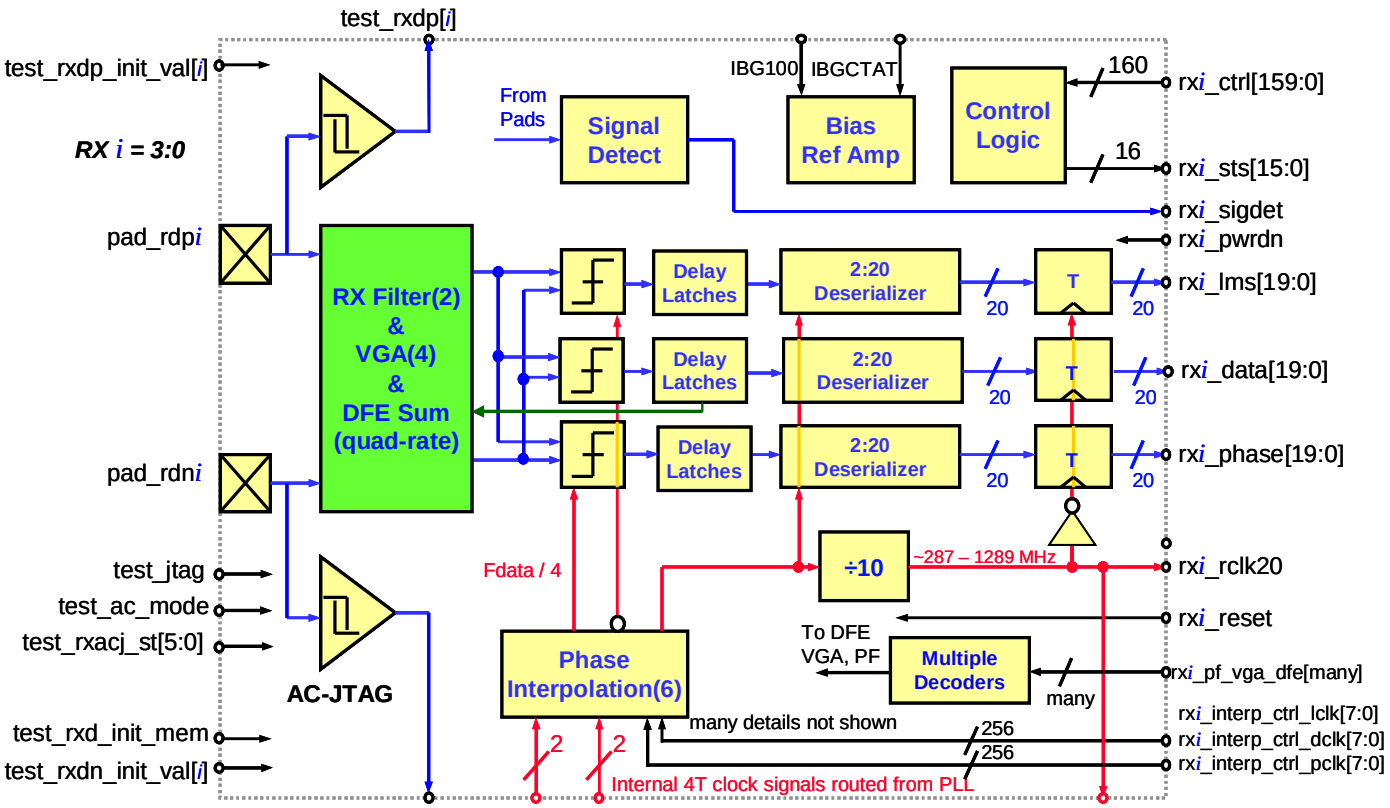
rx*i*_sts[15:0]	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0xD0CB	sigdet	rx_pf_ctrl<3:0>				rx_data_thresh_sel<5:0> == DFE tap1 without sign bit							rx_vga_ctrl<4:0>, truncated to fit			

All the default values are “0”, except for the bits with the lt green background.

9. Block diagram of Receiver – some placeholder info from Falcon16 or now, inc diagram

Key features include

1. Many TBD changes to support 50G PAM4, but include more data and phase slicers and associated output signals
2. On chip, ~85 ohm differential termination with local Vbias for pad_rdp/n
3. On chip, inductive termination and large CM cap to meet diff and CM RL specs
4. Dual band peaking filter with 0-8 dB of boost for the high freq band, and 0-3 dB of boost for the low freq band, and both use ~0.5 dB steps
5. 3-stage VGA with optional mode for low-gain, high BW
6. 14-tap DFE, 6 fixed and 8 floating, tap weight ranges listed in Sec 10
7. Quarter-rate architecture with six phase interpolators. With the appropriate PI phase position settings, both Baud Rate and OS CDR modes are supported.
8. Full support for a H/V eye diagnostics mode
9. Digital data is launched on the falling edge of the 20T word clock, rx_rclk20, which has a 60 H, 40 L duty cycle.
10. Signal Detect, LOS, is CX-4 compliant, and can be calibrated to reduce offsets
11. AC-JTAG with programmable hysteresis
12. Bandgap based bias currents for better performance over VT
13. Due to the complex design and the many pins, not all features and pins are shown in the diagram below. Please see the complete pin list in the following pages for more detailed descriptions of the pin functions. Needs updating for Falcon RPTR. Add design targets from system spec?



10. Receiver Pin List – very few changes for 16nm, but should be reviewed

	Receiver Lane		**(i) = [0, 1, 2, 3, 4, 5, 6, 7], refers to the 8 core lanes**
I/O	**Pin Name by Section**	**Coding**	**Description**
	DC		
I	rx(i)_dc_offset[7:0]	S, Gray	Approx 0.3 mV steps (nominal), +/- 40 mV range at the EQ output, and +/- 80 mV at the RX input due to the loss in the EQ.
	EQ		
I	rx(i)_pf2_ctrl[2:0]	Gray	DC cut (Low PF), add details, gain loss TBD, ???
I	rx(i)_pf_ctrl[4:0]	Gray	Main PF, add details such as gain loss and step size, final BH version is TBD pending more system work
	VGA		
I	rx(i)_vga_ctrl[6:0]	Gray	Only bits [5:0] and codes 0 to 36 are used, approx gain per step = 0.5dB, and the net usable gain range over PVT ~= ??dB
	FFE taps		**(a) = [a, b, c, d], refers to the 4 interleaves**
I	rx(i)(a)_ffe_tap1[6:0]	S, Gray[5:0]	+/-(valid codes 0-40), 1 LSB = 0.25*tap0/(40), where tap0 is the main signal path
I	rx(i)(a)_ffe_tap2[6:0]	S, Gray[5:0]	+/-(valid codes 0-40), 1 LSB = 0.25*tap0/(40)
	SLICER and DFE tap 1		**(a) = [a, b, c, d], refers to the 4 interleaves per lane**
I	rx(i)(a)_slicer_offset_adj[59:0]	Ten 6-bit sets, S, Gray[4:0]	Sign, 5-bit Gray +/-23, valid code range +/-15 for slicer offsets +/-8 for DCD

rx(i)(a)_slicer_offset_adj[59:0]	slicer name	definition	usage
<59:54>	cal_d5<5:0>	data slicer 5	ES, p5, NS, p2
<53:48>	cal_d4<5:0>	data slicer 4	ES, p3, only
<47:42>	cal_d3<5:0>	data slicer 3	ES, p1, NRZ-DFE
<41:36>	cal_d2<5:0>	data slicer 2	ES, m1, NRZ-DFE
<35:30>	cal_d1<5:0>	data slicer 1	ES, m3, NS, 0
<29:24>	cal_d0<5:0>	data slicer 0	ES, m5, NS, m2
<23:18>	cal_ph2<5:0>	phase slicer 2	ES, p2, NS, p2, NRZ-DFE
<17:12>	cal_ph1<5:0>	phase slicer 1	ES, 0, NS, 0
<11:6>	cal_ph0<5:0>	phase slicer 0	ES, m2, NS, m2, NRZ-DFE, NRZ-VSR
<5:0>	cal_lms<5:0>	lms slicer	ES, NS, NRZ-DFE, NRZ-VSR

Per email from Jan 5, 2016

The data threshold control on reference ladder will be redefined as:

Slicer 5:0, ES mode, rx_data23_thresh_sel<7:0> (+ for slicer 3 (+1), - for slicer 2 (-1)), rx_data14_thresh_sel<7:0> (+ for slicer 4 (+3), -for slicer 1 (-3)), rx_data05_thresh_sel<7:0> (+ for slicer 5 (+5), - for slicer 0 (-5))

Slicer 5, 1, 0: NS mode (heavy load due to pam4 DFE tap2), rx_data05_thresh<7:0> for slicer5/0 (+ for slicer 5 (+1), - for slicer 0 (-1)) and rx_data14_thresh<7:0> for slicer 1 (0)

Slicer 3, 2: NRZ mode (heavy load due to NRZ DFE tap2), rx_data23_thresh<7:0> (+ for slicer 3 (+1), - for slicer 2 (-1))

I	rx(i)_data23_thresh_sel[7:0]	S, Gray	Selects threshold voltage for -/+1 slicers -127 to 127, 127 = 300mV, but TBD and might be smaller for better linearity
I	rx(i)_data14_thresh_sel[7:0]	S, Gray	Selects threshold voltage for -/+3 slicers -127 to 127, 127 = 300mV
I	rx(i)_data05_thresh_sel[7:0]	S, Gray	Selects threshold voltage for -/+5 slicers -127 to 127, 127 = 300mV
I	rx(i)_phase1_thresh_sel[7:0]	S, Gray	Selects threshold voltage for 0 slicer -127 to 127, 127 = 300mV
I	rx(i)_phase02_thresh_sel[7:0]	S, Gray	Selects threshold voltage for -/+2 slicers -127 to 127, 127 = 300mV
I	rx(i)_lms_thresh_sel[7:0]	S, Gray	+/-127, 127 = 300mV (2x Vrefdata LSB)
	DFE taps >= 2		**(a) = [a, b, c, d], refers to the 4 interleaves**
I	rx(i)(a)_dfe_tap2[4:0]	S, Gray, B	+/-15, 1 LSB = 150mV/64 Additional gain settings will allow adjustment for higher slicer targets, or small boost for bandwidth loss
I	rx(i)(a)_dfe_tap3[4:0]	S, Gray, B	+/-15, 1 LSB = 150mV/64
I	rx(i)(a)_dfe_tap4[4:0]	S, Gray, B	+/-15, 1 LSB = 150mV/64
I	rx(i)(a)_dfe_tap5[3:0]	S, Gray, B	+/-7, 1 LSB = 150mV/64
I	rx(i)(a)_dfe_tap6[3:0]	S, Gray, B	+/-7, 1 LSB = 150mV/64
I	rx(i)(a)_dfe_tap(7)[3:0]	S, Gray, B	+/-7, 1 LSB = 150mV/64
I	rx(i)(a)_dfe_tap(8)[3:0]	S, Gray, B	+/-7, 1 LSB = 150mV/64
I	rx(i)(a)_dfe_tap(9)[3:0]	S, Gray, B	+/-7, 1 LSB = 150mV/64
I	rx(i)(a)_dfe_tap(10)[3:0]	S, Gray, B	+/-7, 1 LSB = 150mV/64
I	rx(i)(a)_dfe_tap(11)[3:0]	S, Gray, B	+/-7, 1 LSB = 150mV/64
I	rx(i)(a)_dfe_tap(12)[3:0]	S, Gray, B	+/-7, 1 LSB = 150mV/64
I	rx(i)(a)_dfe_tap(13)[3:0]	S, Gray, B	+/-7, 1 LSB = 150mV/64
I	rx(i)(a)_dfe_tap(14)[3:0]	S, Gray, B	+/-7, 1 LSB = 150mV/64
I	rx(i)(a)_dfe_tap(7)_mux[1:0]		tapN cancels ISI from location (N + *value), where value is 0,1,2,3 Mux selects, 0 is early, 3 is later
I	rx(i)(a)_dfe_tap(8)_mux[1:0]		tapN cancels ISI from location (N + *value), where value is 0,1,2,3 Mux selects, 0 is early, 3 is later

I	rx(i)(a)_dfe_tap(9)_mux[1:0]		tapN cancels ISI from location (N + 4*value), where value is 0,1,2,3 Mux selects, 0 is early, 3 is later
I	rx(i)(a)_dfe_tap(10)_mux[1:0]		tapN cancels ISI from location (N + *value), where value is 0,1,2,3 Mux selects, 0 is early, 3 is later
I	rx(i)(a)_dfe_tap(11)_mux[1:0]		tapN cancels ISI from location (N + *value), where value is 0,1,2,3 Mux selects, 0 is early, 3 is later
I	rx(i)(a)_dfe_tap(12)_mux[1:0]		tapN cancels ISI from location (N + *value), where value is 0,1,2,3 Mux selects, 0 is early, 3 is later
I	rx(i)(a)_dfe_tap(13)_mux[1:0]		tapN cancels ISI from location (N + *value), where value is 0,1,2,3 Mux selects, 0 is early, 3 is later
I	rx(i)(a)_dfe_tap(14)_mux[1:0]		tapN cancels ISI from location (N + *value), where value is 0,1,2,3 Mux selects, 0 is early, 3 is later
	Phase Interpolator		changed to 9-bits and LSB = UI/128
I	rx(i)_interp_ctrl_dclk[8:0]	Gray	reference code is 0 inc to the binary code, adds delay
I	rx(i)_interp_ctrl_pclk[8:0]	Gray	pclk will be at approx -4 to +TBD codes relative to data (m1)
I	rx(i)_interp_ctrl_lclk[8:0]	Gray	lclk will be at -64 to +64 codes relative to data (p1)
I	rx(i)_interp_ctrl_dclkq[8:0]	Gray	Delayed by ~ 128 +/- 4 codes vs the non-q version. The +/- 4 codes are used for DCD correction.
I	rx(i)_interp_ctrl_pclkq[8:0]	Gray	Delayed by ~ 128 +/- 4 codes vs the non-q version. The +/- 4 codes are used for DCD correction.
I	rx(i)_interp_ctrl_lclkq[8:0]	Gray	Delayed by ~ 128 +/- 4 codes vs the non-q version. The +/- 4 codes are used for DCD correction.
	General		
I	rx(i)_pwrdn		Receiver power down, active high. Powers down all RX blocks except Signal Detect and rclk20, which have separate pwrdn control pins. All three pwrdn controls must be asserted to completely power down the RX.
I	rx(i)_reset		Receiver reset, active high. Gates the 32T clock, but not rclk20 or the data.
I	rx(i)_sigdet_pwrdn		Powers down Signal Detect, active high
O	rx(i)_sts[15:0]		Receiver status bits, see end of Sec 11
I	rx(i)_osr_mode[1:0]		Enables local, per lane clock dividers which scale rxi_rclk20, rxi_clk32, rxi_clk66 00 - full rate 01 - half rate, aka OSx2 10 - quarter rate, aka OSx4

			11 - undefined
I	rx(i)_ctrl[175:0]		Analog control bits, see Sec 11
O	rx(i)_data[59:0] See more details below	Bit 0 is earliest Complete bit list per interleave for data, phase, lms a – 0,4,8,12,16 b – 1,5,9,13,17 c – 2,6,10,14,18 d – 3,7,11,15,19	dp and dn are muxed based on **previous** data Data is launched on the falling edge of rx(i)_rclk20, which has a 60 H, 40 L duty cycle
O	rx(i)_phase[39:0]	Bit 0 is earliest	zp and zn are muxed based on the **current** data bit
O	rx(i)_lms[19:0]	Bit 0 is earliest	
O	rx(i)_rclk20		Recovered word clock to digital core, 20T wrt the freq set by rx(i)_osr_mode[1:0] 60 High, 40 Low duty cycle Drives all data outputs Not gated by rx(i)_reset
O	rx(i)_sigdet		CX4 signal detect output, not filtered
I	rx(i)_rclk20_pwrdn		Powers down rx(i)_rclk20, active high. After de-assertion, rx(i)_rclk20 should be stable in ~200ns
O	rx(i)_clk32		Recovered clock, 32T wrt the freq set by rx(i)_osr_mode[1:0] 50% duty cycle Enabled by rx_ctrl<104> and gated by rx(i)_reset
I	rx(i)_pam4_mode[1:0]		Selects between the main NRZ and PAM4 modes of operation for the slicers and DFE 00 – NRZ w DFE, same as Falcon16 01 – NRZ VSR, no DFE 10 – PAM4 NS, approx. for VSR, maybe MR/SR, but TBD pending standards 11 – PAM4 ES, must use for LR
O	rx(i)_clk66		Recovered clock, 66T wrt the freq set by rx(i)_osr_mode[1:0] 48/52, H/L duty cycle Enabled by rx_ctrl<7> and gated by rx(i)_reset

New pins and functions for Blackhawk

Receive Datapath

Databus name (k is lane number)	**Receive Datapath (1 symbol widths specified)**	**PAM4-ES (n = symbol index)**	**PAM4-NS**	**NRZ**
rx*k*_data[59:0]	data, 3 bits * 20	{3*n, 3*n+1, 3*n+2} 110 (+6) 101 (+4) 100 (+2) 011 (0) 010 (-2) 001 (-4) 000 (-6)	bit #3*n+2: slicer @ +2 bit #3*n+1: slicer @ 0 bit #3*n: slicer @ -2 {3*n, 3*n+1, 3*n+2} 111 (+3) 110 (+1) 100 (-1) 000 (-3)	{3*n, 3*n+1, 3*n+2} 001: +1 000: -1
rx*k*_phase[39:0]	phase, 2 bits * 20	Format: encoded value (3 slicers) {2*n, 2*n+1} 11 (111) 10 (011) 01 (001) 00 (000) The 3 slicers above are @ {+2,0,-2}	same as pam4es The 3 slicers are @ {+1,0,-1}	{2*n, 2*n+1} 01 (+1) 00 (-1)
rx*k*_lms[19:0]	lms, 1bit * 20	1:+1 0:-1	1:+1 0:-1	1:+1 0:-1
rx*k*_dfe_data[39:0]	dfe_data, 2bits * 20	2 bits per symbol, output of the transmitted symbol estimator. [2]	X (powered down)	X (powered down)
	Power down modes	Mode 1: all slicers on; Mode 2: power down the +2,-2 (~+/-86mV)phase slicers	3 data slicers always powered down Mode 1: all phase slicers on Mode 2: power down +1,-1 (+/-86mV) phase slicers	4 data slicers, 1 phase slicer always powered down;

Note:

1. Interpretation of the Kp4 spec: In a symbol pair of bits {2*n+1, 2*n} , where n is the symbol number, the symbols are mapped as follows : 11 is +3, 01 is +1, 10 is -1 and 00 is -3
2. Dfe_data estimates the transmitted PAM4 symbol from the extended symbol.

11. Description of RX Control and Status Register Pins –- default = 0, except for xxx = 1 Ibias (max, mode/sign, min) controls provides +/- 25 and 12 % variation of bias currents, and where mode = 1 is +

Receiver – *common for all for all eight lanes*	
Pin name	**Description**
0x????<15:0>	PMD Register Name = AMS RX CONTROL
rx_ctrl<175:174>	vga_bw_ctrl_ind<1:0> – coarse BW control for the VGA stages, removes shunt peaking inductors, VGA3, VGA10
rx_ctrl<173:172>	vga_bw_ctrl_cap<1:0> – fine BW control for the VGA stages, adds caps to VGA01.
rx_ctrl<171>	pf3_pkcomp_dis – disables the residual peaking compensation cap at the PF3 output. Peaking ~3-5dB at ~11GHz over PVT. Test mode.
rx_ctrl<170>	pf3_ind_dis – shunts and disables inductor peaking which reduces the PF3 BW, usage TBD, overridden by rx_ctrl<169> pf3_lz_en. Test mode.
rx_ctrl<169>	pf3_lz_en – shift zero/pole pair to lower freq
rx_ctrl<168>	pf3_max_bw – increases rolloff pole BW 20%, lowers DC gain 2 dB, rescal still valid, bias currents not auto scaled, see rx_ctrl<28:26>
rx_ctrl<167:164>	pf3_rescal_mux (force, ctrl[3:1]) - rescal override with ~6% steps. Can be used to adjust the BW vs gain & possibly peaking
rx_ctrl<163:160>	pf3_ctrl<3:0> - controls boost for new PF with higher freq range, Gray code
0xD0C9<15:0>	
rx_ctrl<159>	TBD, clock_cal_en – send PLL clock to slicer inputs for phase alignment calibration – not in Sinai ver
rx_ctrl<158:156>	d2c and clk buffer ibias (max, mode, min) – one control bus for six 100uA currents
rx_ctrl<155>	sel_d2clp: 0, high power for 25-28g; 1, low power for <25g, default=0, data path d2c only for NRZ DFE mode, data path, keep 0 for now or maybe 10G only
rx_ctrl<154>	rxclk_mux – selects between 4T IQ clks from PLL0, default 0, and PLL1 was reserved, copied from rx_ctrl<95>
rx_ctrl<153:152>	clk_bw_ctrl<1:0> for 15G to 28G, controls the BW for the clocks that drive the six PIs 00 15-21.875G, 01 23G, 10 25-26.25G, **11 27-28G** Must use 00 for all OSx2 and OSx4 modes
	4-bit for each clock: dac4ck[3:0], sign+binary(2:0). 0000 or 1000 is default without adjustment. 0111 (+) and 1111(-) is maximum value. LSB ~= 0.4 ps
rx_ctrl<151:148>	dac4ck_dat_q<3:0>

rx_ctrl<147:144>	dac4ck_dat_i<3:0>
0xD0C8<15:0>	
rx_ctrl<143:140>	dac4ck_phs_q<3:0>
rx_ctrl<139:136>	dac4ck_phs_i<3:0>
rx_ctrl<135:132>	dac4ck_lms_q<3:0>
rx_ctrl<131:128>	dac4ck_lms_i<3:0>
0xD0C7<15:0>	
rx_ctrl<127:126>	vga_step_mode 00: stage sequential from VGA2 to VGA0, best linearity, worst offset jump 01: ping-pong bit sequence from VGA0 to VGA2 10: stage sequential from VGA0 to VGA2, worst linearity, best offset jump 11: stage sequential as VGA0, VGA2, VGA1, modest linearity and offset jump, ucode default
rx_ctrl<125>	eq_pkcomp_dis – disables the residual peaking compensation cap at the EQ output. Peaking ~3-5dB at ~11GHz over PVT. Test mode.
rx_ctrl<124>	eq_ind_dis – shunts and disables inductor peaking which reduces the EQ BW for OS2 modes, overridden by rx_ctrl<10> eq_lz_en. Test mode.
rx_ctrl<123>	dc_offset_half_range – reduces DC offset range and LSB by 50% to improve accuracy
rx_ctrl<122>	short VGA output – used for slicer calibration
rx_ctrl<121>	rx_offset_pd – pwrdn AFE offset cancellation DAC
rx_ctrl<120>	force dc_offset, enables override using register bits
rx_ctrl<119:112>	dc_offset[7:0]
0xD0C6<15:0>	
rx_ctrl<111:110>	dfe_summer_vcm<1:0> - adjusts summer Vcm to match ladder Vcm. Levels are wrt below RX VDD. def 00: 225 mV, 01: 257 mV, 1x: 200 mV
rx_ctrl<109:108>	en_tap9delay<1:0> - increased to 2-bits for 16nm 00(default) = >25G, 01 = 22-25G, 1x = <22G, moved from rx_ctrl<151:150>, both N/P
rx_ctrl<107>	cml_lp – DFE mux selection and latch, assert for OS2 and OS4 rates to lower power, ~10mW. Only for NRZ modes. Not part of the 25G VSR mode.
rx_ctrl<106>	dfesum_lp – adds peaking at 17G, intended for VSR mode with no DFE, lower power, -5mW. Usage is TBD pending test results.
rx_ctrl<105>	pd_phs_slr – power down +2, -2 phase slicers
rx_ctrl<104>	rxclk32_en – enables 32T clock
rx_ctrl<103:100>	offset correction rescal mux (force, ctrl[3:1]) - rescal override
rx_ctrl<99:96>	peaking filter rescal mux (force, ctrl[3:1]) - rescal override. Can be used to adjust the BW vs gain &

	possibly peaking
0xD0C5<15:0>	
rx_ctrl<95>	sd_cal_en – enables the calibration of the signal detect circuits to cover about +/-20mV, (~4-sigma)
rx_ctrl<94>	testclk_mux – selects between local test clock defined by rx_ctrl<93:92>, and from adjacent lane, 0 = local, 1 = adjacent
rx_ctrl<93:92>	testclk_div[1:0] – divides/muxes rclk20 for test port 00 – div1, 01 div2, 10 div 4, 11 div8 also see rx_ctrl<8>
rx_ctrl<91>	sd_cal_polarity – selects the pos or neg threshold path for signal detect calibration
rx_ctrl<90:88>	sd_cal_pos<2:0> – offset adj bits for SD pos, <2> sign, <1:0> binary, LSB ~= 6.6mV at SD input
rx_ctrl<87:85>	sd_cal_neg<2:0> – offset adj bits for SD neg, <2> sign, <1:0> binary, LSB ~= 6.6mV
rx_ctrl<84:80>	VGA2 rescal mux (force, ctrl[3:0]) - rescal override
0xD0C4<15:0>	
rx_ctrl<79:75>	VGA1 rescal mux (force, ctrl[3:0]) - rescal override
rx_ctrl<74:70>	VGA0 rescal mux (force, ctrl[3:0]) - rescal override
rx_ctrl<69:67>	ffe_sha_ibias (max, mode, min) – FFE sample and hold bias, BGR – n/a
rx_ctrl<66:64>	ffe_summer_tap_ibias (max, mode, min) – FFE tap weight bias, 3P1CcalR – n/a
0xD0C3<15:0>	
rx_ctrl<63>	dfe_sum_bw12 – reduce Rload by ~12% to increase BW. Should set rx_ctrl<59:57> = 011 to keep operating point – was ffe_enable
rx_ctrl<62:60>	DFE slicer ibias (max, mode, min), only mux/latch
rx_ctrl<59:57>	DFE sum/buf ibias (max, mode, min)
rx_ctrl<56:54>	offset correction ibias (max, mode, min)
rx_ctrl<53:51>	DLL ibias (max, mode, min) – clkgen for 4-phase div and mux
rx_ctrl<50:48>	met R ibias (max, mode, min) – threshold voltage ladder, can be used to adjust the +/- 300 mV range
0xD0C2<15:0>	
rx_ctrl<47>	pwrdn_ftap – power down for the DFE floating taps, use for 25G-SR and all OS2 and OS4 modes such as 10G-KR and 6G-LR, power ~-1mW
rx_ctrl<46>	vga3_ind – increases the shunt peaking inductor value for VGA3 by ~25% was sigdet_10g – use for 10G and lower rates
rx_ctrl<45>	pd_ch_p1 – power down for the p1, aka lms, channel, reduces the power by ~10mW
rx_ctrl<44>	sel_th4dfe[1] – DFE tap threshold voltage
rx_ctrl<43>	sel_th4dfe[0] – 00 125mV, **01 150 mV**, 10 175mV,

	11 200mV, shift all by -25mV??, use for FFE??
rx_ctrl<42:41>	dfesum_bw<1:0> – set BW of DFE summer stage 00 = <15G, 01 = 15-20G, 10 = 20-25G, **11 = >25G** Need more details for final BH design, not true BW
rx_ctrl<40:38>	DFE tap weight ibias (max, mode, min)
rx_ctrl<37:35>	phase interpolators ibias (max, mode, min) – one control bus for six 100uA currents
rx_ctrl<34:32>	signal detect ibias (max, mode, min)
0xD0C1<15:0>	
rx_ctrl<31:29>	input CM voltage ibias (max, mode, min)
rx_ctrl<28:26>	pf3_ibias (max, mode, min) – was VGA3 ibias
rx_ctrl<25:23>	VGA2 ibias (max, mode, min)
rx_ctrl<22:20>	VGA1 ibias (max, mode, min)
rx_ctrl<19:17>	VGA0 ibias (max, mode, min)
rx_ctrl<16>	bypass AC cap – test mode to bypass the internal AC cap to measure the internal DC voltages. The BW is low and this mode is not intended for normal operation with data traffic.
0xD0C0<15:0>	
rx_ctrl<15:13>	peaking filter ibias (max, mode, min)
rx_ctrl<12>	DC couple, for QSGMII DC mode with 50 Ohm pull-up to RVDD0P8
rx_ctrl<11>	dfe_hgain_en – enables high, fixed gain for the DFE summer and buffer for non-DFE modes
rx_ctrl<10>	eq_lz_en – enables lower freq EQ peaking used in 10G mode. For the complete 10G mode, rx_ctrl<173:172> must also be asserted.
rx_ctrl<9>	pf_max_bw – increases rolloff pole BW ~25%, lowers DC gain 2.5 dB, rescal still valid, bias currents not auto scaled, see rx_ctrl<15:13> - was vga_10g_bw
rx_ctrl<8>	tport_en - output rx_rclk20 to PLL test port
rx_ctrl<7>	rxclk66_en – enables 66T clock was sigdet bypass – force sigdet output = 1
rx_ctrl<6>	sigdet_pwrdn, default=0 for enable signal detector
rx_ctrl<5>	Signal Detect threshold adjust, offset cntl <2:0>, default <010> ~= 80mVppd, Gray code Controlled by digital logic and register 0xD0E2 000: 20mV **010: 80mV for use** 101: 140mV 001: 40mV 110: 100mV 100: 160mV 011: 60mV for screen 111: 120mV These thresholds can now be calibrated. See rx_ctrl<95, 91:85> for the new control bits. LSB size ~= 17.5mV for 16nm
rx_ctrl<4>	
rx_ctrl<3>	
rx_ctrl<2:0>	master diodes ibias, (max, mode, min) – current change is reversed vs the current sources Common all biasgen blocks.

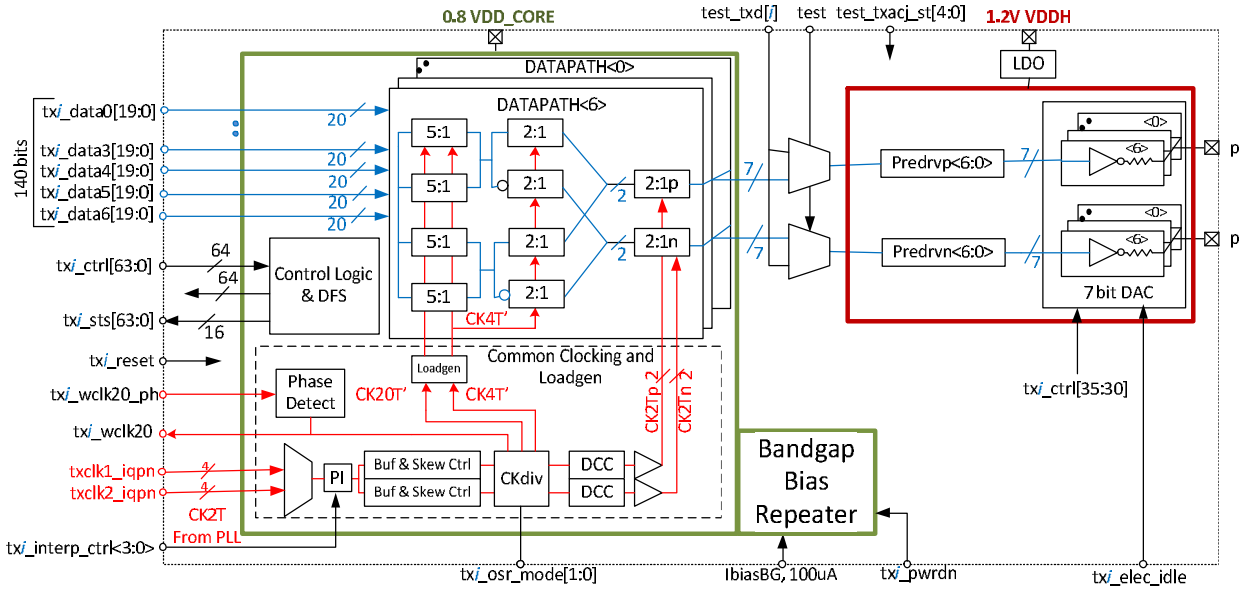
0xD0CB<15:0>	**RX Status** – also in register map
rx_sts<15>	Signal detect output, no digital filtering
rx_sts<14:11>	Direct copy of rx_pf_ctrl<3:0> as sent from the digital which is Gray coded
rx_sts<10:5>	rx_data23_thresh_sel<5:0>
rx_sts<4:0>	rx_vga_ctrl<4:0>, only first 32 codes

12. Block Diagram of Transmitter – many changes needed to account for the new DAC design shown in the diagram below

Key features include

1. The analog design is a true 7-bit DAC and the FIR function is now in the digital PMD block.
2. Max scale amplitude ~1.0 Vppd, for code 127, ➔ LSB ~= 8 mVppd
3. Reduced PI LSB to UI/128, moved PI decoder to analog to reduce skew and routing
4. Removed support for low latency mode.
5. Reduce data word width to 20-bits to minimize the latency
6. Support for Transmit Clock Align with programmable master clock source lane
7. One 2T phase interpolator per lane to support independent lane repeater mode
8. Low power, half-rate SST driver architecture
9. On chip, 40 ohm single-ended termination
10. Electrical Idle mode for power saving and EEE support
11. Bandgap based bias currents
12. TX driver with integrated LDO for better PSRR and tighter amplitude control. This requires that the TVDD1P20 supply pin be connected to 1.20 V +/-5%. Optional for low swing, VSR modes where the min amplitude is <800 mVppd.
13. Independent lane OS2x and OS4x modes are supported with local clock dividers and muxes per lane.
14. Full support for AC_JTAG
15. Test mode to generate 0101 and 0011 data patterns with only analog registers

Note that the block diagram below is somewhat conceptual, as all details are not shown.



13. Transmitter Pin List

Transmitter *i* = [0, 1, 2, 3, 4, 5, 6, 7]		
I/O	**Pin name**	**Description**
I	tx_drv_hv_disable	Default = 0, ie assume High Voltage Driver (HVD) mode and 1.2V. To avoid damage, it must not be set = 1 if TVDD1P2 = 1.2V. This is required for both functional and scan modes, eg during LBIST and burn-in. For correct driver performance, set = 1 when TVDD1P20 = 0.8-1.0 V. Lower power by ~10mW. Use for VSR mode.
I	tx*i*_ctrl[63:0]	Transmitter control bits, see Sec 14
I	tx*i*_data[139:0]	PMD core data to transmitter, now 7x20 bits for the DAC input. Bit 0 is transmitted first. See Sec 29 for ana/dig timing info. tx_data[139:0] = { tx_dac_bit6[19:0], tx_dac_bit5[19:0], tx_dac_bit4[19:0], tx_dac_bit3[19:0], tx_dac_bit2[19:0], tx_dac_bit1[19:0], tx_dac_bit0[19:0]}
I	tx*i*_elec_idle	Forces driver output to Vcm, used for EEE support. The clocks are active. Same as tx_ctrl[47], and they are OR'd together. Per detailed email thread, requires setting tx_dac_bit4[19:0] = 20'b1 and tx_dac_bit3[19:0] = 20'b0 to fully enable the idle mode. Overrides tx_reset.
I	tx*i*_interp_ctrl[4:0]	Phase interpolator, 5-bits, and MSB is a resetb signal for the PI // bit[3] indicate 1: inc freq, ie less delay, 0: dec freq, bits [2:0] is phase jump from 0, 1, 2, 4, 8 active high Driven by a 4-phase, 2T PLL0/1 clock from the output of the mux controlled by tx_ctrl<34>
I	tx*i*_osr_mode[1:0]	Enables local, per lane clock dividers which scale txi_wclk20 and txi_clk32 00 - full rate 01 - half rate 10 - quarter rate 11 - undefined
I	tx*i*_pwrdn	Transmitter power down mode, active high, see Sec 32 Forces TX output to Vcm, and Hi-Z, and shuts down all TX clocks.

I	tx*i*_reset	Transmitter reset, active high. Forces TX output to TBD, and does not affect the phase detector output. Digital will send +3/-3 as needed.
O	tx*i*_sts[15:0]	Transmitter status bits, see Sec 14
O	tx*i*_wclk20	PLL + TX PI divide by 20. Duty cycle is 50%. Scales with the VCO freq plus the per lane OS2/4 modes. Gated by pll_iddq, pll_pwrdn, pll_reset from the PLL that is selected with the clkmux, tx_ctrl<34> A derivative of this clock is used by the TX analog to latch in the data from the digital core.
O	tx*i*_clk32	PLL + TX PI divide by 32. Duty cycle is 50%. Scales with the VCO freq plus the per lane OS2/4 modes. Enabled by tx_ctrl<31>, and gated by pll_iddq, pll_pwrdn, pll_reset from the PLL that is selected with the clock mux, tx_ctrl<34>
O	tx*i*_clk66	PLL + TX PI divide by 66. Duty cycle is 48/52, H/L. Scales with the VCO freq plus the per lane OS2/4 modes. Enabled by tx_ctrl<30>, and gated by pll_iddq, pll_pwrdn, pll_reset from the PLL that is selected with the clock mux, tx_ctrl<34>
O	tx*i*_phsdet	Phase detector output for transmit clock align (TCA). The PD compares the master and local 20T clocks, and the PD is clocked by the “external” clock, ie the master lane clock,

14. Description of TX Control and Status Register Pins – default = 0, except for xxx = 1
Imax, imode, imin control provides +- 12 and 25 % variation of bias currents

Transmitter *common for all eight lanes*	
Pin name	**Description**
0xD0D3<15:0>	PMD Register Name = AMS TX CONTROL_*
tx_ctrl<63:59>	reserved, might use tx_ctrl<63:56> for RX
tx_ctrl<58:57>	reserved, was pibuf_ctrl<1:0> - adjust bias for PI d2c, add DFT mux
tx_ctrl<56>	reserved – there is no LL option in BH, was pdet_ll_clk
tx_ctrl<55>	sel_txmaster – select TX lane as master (active high) to sync up all independent lanes Only one TX lane can be set to master, and which drives a common clock bus across all lanes. To minimize residual lane to lane phase differences, it is recommended to use lanes 3 or 4 as a master.
tx_ctrl<54>	reserved ~~– was sel_ll – select low latency data path~~
tx_ctrl<53>	pdet_mode[1] – select update rate for phase detect (pdet) output 0 = Fwclk, 1 = Fwclk/5
tx_ctrl<52>	reserved – pdet_mode[0] – select div2 of read clock in FIFO mode, reserved per Anand?
tx_ctrl<51>	reserved – sel_fifo_pol – invert FIFO data polarity
tx_ctrl<50:48>	reserved – fifo_depth[2:0] - select the depth, 0-3, of the FIFO, and bit[2] is the enable bit
0xD0D2<15:0>	
tx_ctrl<47>	Elec_Idle_aux, force electrical idle mode
tx_ctrl<46:40>	reserved
tx_ctrl<39:38>	driver_res_cal[1:0] – dedicated rescal code for the DAC driver, tables to follow default 00 for LDO mode and 01 for 0.8V mode, needs a mapping table
tx_ctrl<37>	test_data[1], generates ..00110011.. output pattern at full data rate, overrides test_data[0]
tx_ctrl<36>	test_data[0], generates ..010101.. output pattern
tx_ctrl<35>	slew_rate – enables both the HPF bits to add loading to the TX output and increase the transition time for compliance with lower speed standards
tx_ctrl<34>	txclk_mux – selects between 2T IQ clks from PLL0, default 0, and PLL1

tx_ctrl<33>	hpf_ctrl[1] – used only as a slew rate cap, and when tx_ctrl<35> = 1
tx_ctrl<32>	hpf_ctrl[0] – when tx_ctrl35> = 0, adds a feed forward zero to the TX output, and the range is TBD. Helps to cancel the pkg loss without using any of the FIR range.
0xD0D1<15:0>	
tx_ctrl<31>	txclk32_en – enables 32T clock
tx_ctrl<30>	txclk66_en – enables 66T clock
tx_ctrl<29:28>	ldo_vref[1:0] – adjusts internal driver supply voltage **00**→0.92 V, 01→0.96 V, 10→1.0 V, 11→1.04 V and also scales the output amplitude ~2% per step. With code 00, the output amplitude, ~= 1.02 V, typ, for 8 1s, 8 0s pattern
tx_ctrl<27>	ildo[2], LDO opamp bias current control (mode)
tx_ctrl<26>	ildo[1] (max)
tx_ctrl<25>	ildo[0] (min)
tx_ctrl<24>	reserved, was icml[2], clock input buffer current control, not used?
tx_ctrl<23>	reserved, was icml[1]
tx_ctrl<22>	reserved, was icml[0]
tx_ctrl<21>	iphint[2], phase interpolator current control
tx_ctrl<20>	iphint[1]
tx_ctrl<19>	iphint[0]
tx_ctrl<18>	ibias[2], master bias diode
tx_ctrl<17>	ibias[1]
tx_ctrl<16>	ibias[0]
0xD0D0<15:0>	
tx_ctrl<15>	cal_aux[3], rescal manual control when cal_off=1
tx_ctrl<14>	cal_aux[2]
tx_ctrl<13>	cal_aux[1]
tx_ctrl<12>	cal_aux[0]
tx_ctrl<11>	cal_off, disable RESCAL[3:0], enable cal_aux[3:0]
tx_ctrl<10>	tx_dcc_dis, disable differential DC correction, common mode feedback only
tx_ctrl<9>	reserved
tx_ctrl<8>	vddr_bgb – bias mode control for LDO reference, selects between a bandgap reference, default, or a scaled voltage from TVDD1P2, also see tx_ctrl<29:28>
tx_ctrl<7>	ticksel[1] – timing control of load signal at

tx_ctrl<6>	ticksel[0] – ana/dig interface, use 01 for all rates
tx_ctrl<5>	reserved
tx_ctrl<4>	skew enable
tx_ctrl<3>	skew polarity, 0 = delay TX N, 1 = delay TX P
tx_ctrl<2:0>	skew_pn[2:0] – adjusts the skew between the TX P and N outputs, ~0.5 ps per step
0xD0D9<15:0>	**TX Status** – also in register map
tx_sts<15:14>	TX lane ID<1:0>
tx_sts<13>	reserved, but could be used for core ID
tx_sts<12>	tx_drv_hv_disable
tx_sts<11:8>	ana_rescal<3:0> - copy of value sent from chip level ResCal instances. This is the best monitor point to determine the value received and used by the analog circuits.
tx_sts<7:0>	Version ID, eg A0, A1, B0

15. **TX Amplitude Settings, TVDD1P2 = 1.2 V (typ)** – the final settings are TBD for BH and will be based on a 7-bit DAC

- This is the main TX driver mode for Blackhawk, and is properly enabled when TVDD1P2 = 1.2V, and tx_drv_hv_disable is set to its default value, “0”.
- To prevent damage to the output driver, this bit must **always** be “0” if TVDD1P2 = 1.2V
- If TVDD1P2 = 0.8V, use the amplitude table in Sec 17, and in this case, tx_drv_hv_disable must be asserted to enable proper driver operation in the 0.8V mode.
-
- The amplitudes can also be adjusted with the LDO output voltage that is controlled by tx_ctrl<29:28>
- The two table lines in Bold are for
  - **76d** – approx setting for the low swing modes, eg XFI+, XLAUI, SFP+
  - **100d** – default, and approx setting for 25G-LR and 10G-KR

tx_fir_tap_main<6:0> reg 0xD095<6:0> decimal, binary	**TX Amplitude (Vppd)**	**TX Amplitude (Vppd)**
0d, 0000000b	0	
4, 0000010	0.04	
10, 0001010	0.10	
16, 0010000	0.16	
22, 0010110	0.22	
28, 0011100	0.28	
34, 0100010	0.34	
40, 0101000	0.40	
46, 0101110	0.46	
52, 0110100	0.52	
58, 0111010	0.58	
64, 1000000	0.64	
70, 1001010	0.70	
76, 1001100	**0.76**	
82, 1010010	0.82	
88, 1011000	0.88	
94, 1011110	0.94	
100, 1100100	**1.04**	

16. TX FIR Pre-Emphasis Settings for F16 PMD/RPTR A0 **– delete for DAC in BH**

The 2nd and 3rd post-cursor taps, which are typically used to optimize the SFP+ DDJ and DDPWS jitter, are not part of the CL72 logic, and their pre-emphasis levels are controllable through digital REG TBD. For the SFP+ and QSFP XLPPI modes, post2 is typically set to 0100.

Also, setting the pre tap to ~1-3 can help to reduce the DDJ and DDPWS jitter for max loss channels.

The pre tap is generally only used for 100G-KR4/CR4 and 10G-KR and is controlled through the Clause 72/93 tuning.

For the best near end eye results for the 25G modes, and to compensate for the losses in the pkg and test setup, approx 15-20% of post-cursor1 pre-emphasis should be used.

For more information on setting the equalization, please refer to the Falcon Equalization user guide by Magesh V.

Also, see tx_ctrl<33:32> for a new mode to boost the high frequency content of the TX output.

17. TX Amplitude Settings, TVDD1P2 = 0.8V (typ) – very prelim for 16nm

Approx 7 mVppd for the DAC in BH

The normal operating mode for the Falcon TX driver is with TVDD1P2 = 1.2V. Finalizing the support for the 0.8V mode is a WIP, but it is unlikely to be valid for 25G-LR or 100G-KR4 in a large pkg with 2+dB of IL.

However, it is usable for lower performance modes such as 25G-VSR, and any of the lower speed rates that are supported by a 10G core like Eagle, eg 10G-KR, XLAUI, etc. In this case, the two TX supplies can be combined in the pkg to a single 0.8V domain.

The main drawbacks to using this mode are more sensitivity of the output amplitude to the TX supply voltage, and possibly, worse PSRR. The power is ~10mW lower per TX lane.

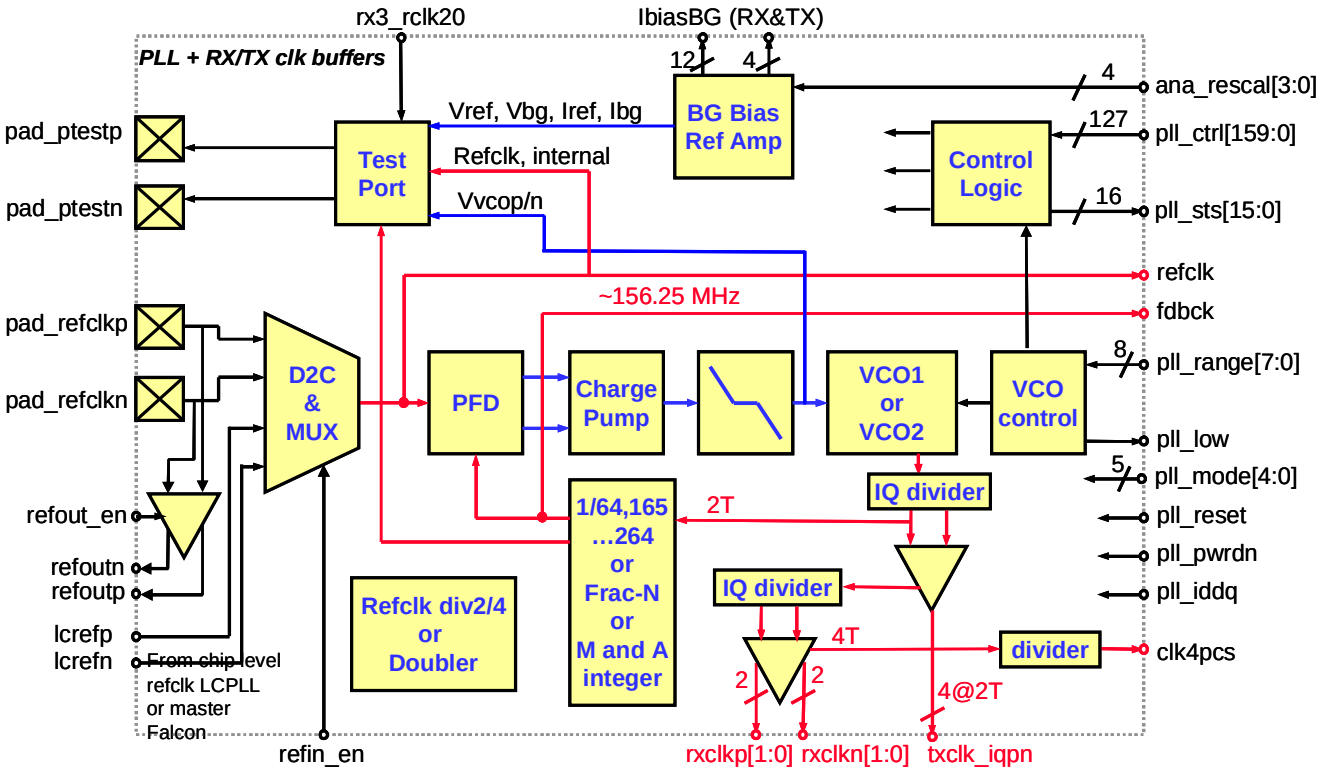
- The two table lines in Bold are for
  - **1011** – approx setting for the low swing modes, eg XFI+, XLAUI, SFP+, etc
  - **1111** – approx setting for 10G-KR

amp_ctrl[3:0]	TX Amplitude (Vppd)		TX Amplitude (Vppd)
reg 0xD0D2 bits [3:0] == tx_ctrl[35:32]			**Test mode only ~12% shift lower tx_ctrl[45]=1, but higher Zout**
0000	0.53		
0001	0.55		
0010	0.57		
0011	0.59		
0100	0.61		
0101	0.63		
0110	0.65		
0111	0.67		
1000	0.69		
1001	0.72		
1010	0.75		
1011	**0.79**		
1100	0.82		
1101	0.85		
1110	0.88		
1111	**0.91**		

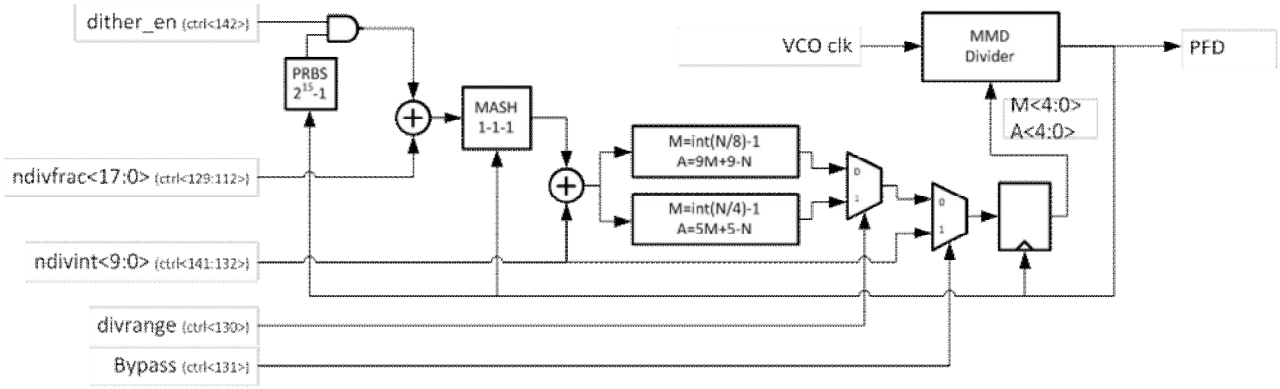
18. Block Diagram of PLL, same for both PLLs

Key features include

1. Add clk4sync, 8T and 6T
2. Add fractional-N mode to support additional refclk freqs and divider ratios
3. Add clk4pcs with 2-bit ➔ 3-bit control
4. Includes 2nd VCO to support 15-22.6 GHz
5. Wide range primary LC VCO, 22.6-30.0 GHz
6. On chip, 100 ohm differential termination with local Vbias for the common-mode voltage of the pad_refclkp/n pins. Plus internal AC caps.
7. Options for 200, 300, 400 ohm termination
8. Contains the bandgap which supplies the bias currents to the RX and TX. The resistors in these bias circuits must be calibrated with the RESCAL IP.
9. Refclk routing channel along the die edge instead of between the analog and digital
10. See Sec 24 for more details on the refclk options
11. Very flexible and useful test port, see Sec 36



Prelim diagram for the fractional-N block. The register locations are copied from Eagle and need updates for Blackhawk. See pll_ctrl<> descriptions for the final usage.



19. PLL and RX/TX Clkgen Pin List

PLL and RX/TX Clockgenerator *i* = [0, 1]		
I/O	**Pin name**	**Description**
I	pll*i*_ctrl[175:160]	Control bits for clock repeater buffers between quads 0 and 1, plus misc
I	pll*i*_ctrl[159:128]	Control bits for fractional-N mode, which is similar to Falcon16
I	pll*i*_ctrl[127:0]	PLL control bits, see Sec 20
O	pll*i*_sts[15:0]	PLL status bits, see Sec 20
I/O	pll*i*_lcrefp	Reference clock from LCPLL or another serdes core.
I/O	pll*i*_lcrefn	LCPLL Reference clock complement
I/O	pll*i*_lcrefp_h	Pass through pins for horizontal
I/O	pll*i*_lcrefn_h	LCREF routing at bottom of core
O	pll*i*_refoutp	Buffered, CML copy of pad_refclkp/n or lcrefp/n, and active when refout_en=1. The refclk source is controlled by pll_refin_en. Vswing = TBD
O	pll*i*_refoutn	The frequency is not affected by pll_ctrl<98:97> and is always the same as the input freq to the bumps, pad_refclkp/n, or lcrefp/n
I	pll*i*_refin_en	LCPLL Reference clock Enable. Selects the refclk from the lcrefp/n pins.
I	pll*i*_refout_en	Enables serdes PLL to drive refclk bus if refoutp/n are connected to the lcrefp/n bus as described in Sec 24 Adds ~4mW when enabled
O	pll*i*_refclk	PLL reference clock, CMOS, frequency typically 125-312.5 MHz, and is not changed if the refclk doubler is enabled Always on unless pll_iddq is asserted, but many bias control bits must be set to their defaults and stable for a glitch free clock
O	pll*i*_fdbck	PLL divider output, CMOS, ~same freq as refclk, 125-312.5 MHz, but in the frac-N mode, and due to dither, the instantaneous freq vary ~12% vs the long term freq Not valid if either pll_iddq, pll_pwrdn, or pll_reset are asserted

O	plli_clk4pcs	PLL divided clk with no PI in the path. Duty cycle is 50%. Gated by pll_iddq, pll_pwrdn and pll_reset. Programmable to 16T, 24T, 32T, 40T, 33T, OFF based on pll_ctrl<107,1:0>, and where T = 1/VCOfreq pll_ctr[107],pll_ctrl[1:0] divider ---------- ---------- 000 16 001 24 010 32 011 40 100 33 101 reserved, off 110 reserved, off 111 power down clk4pcs
O	plli_clk4sync	PLL/8 or PLL/6 clock with no PI in the path. Duty cycle is 50%. Gated by pll_iddq, pll_pwrdn and pll_reset. See pll_ctrl<103:102> for settings.
I	plli_mode[4:0]	PLL integer divider control, N=64, .. 96, 120, 80, .. 264. See Sec 22
I	plli_range[7:0]	VCO frequency range control, 8-bits, all codes from 0-255 are possible, see expected code values in Sec 22
O	plli_low	VCO tuning output, HI = 1 when VCO Vctrl is high, i.e. above comparator threshold and PLL freq is lower than the target. The pll_range[7:0] should be increased until pll_low is LO = 0.
I	plli_reset	PLL reset, active high. Gates all downstream PLL, RX, TX clocks.
I	plli_pwrdn	PLL power down mode, active high. Gates all downstream PLL, RX, TX clocks, but refclk input buffer still active.
I	plli_iddq	Power downs all PLL circuits including refclk and BG bias. Overrides JTAG mode.

<table>
<tr>
<td>I</td>
<td>ana_rescal[3:0]

Check step sizes and W for 16nm
<table>
<tr><th>Code</th><th>Resistor Change in BH (%)</th></tr>
<tr><td>0000</td><td>+22.5</td></tr>
<tr><td>0001</td><td>+19.5</td></tr>
<tr><td>0010</td><td>+16.5</td></tr>
<tr><td>0011</td><td>+13.5</td></tr>
<tr><td>0100</td><td>+10.5</td></tr>
<tr><td>0101</td><td>+7.5</td></tr>
<tr><td>0110</td><td>+4.5</td></tr>
<tr><td>0111</td><td>+1.5</td></tr>
<tr><td>1000</td><td>-1.5</td></tr>
<tr><td>1001</td><td>-4.5</td></tr>
<tr><td>1010</td><td>-7.5</td></tr>
<tr><td>1011</td><td>-10.5</td></tr>
<tr><td>1100</td><td>-13.5</td></tr>
<tr><td>1101</td><td>-16.5</td></tr>
<tr><td>1110</td><td>-19.5</td></tr>
<tr><td>1111</td><td>-22.5</td></tr>
</table>
IP Owner
RESCAL, 16nm – Marc Loinaz</td>
<td>Control code for global resistor calibration, and should be connected to a chip level RESCAL block.

The calibration range is approx +/- 22%, with 3% steps, and the internal resistances in Blackhawk decrease as the ana_rescal code value increases.

The RESCAL mode should be configured to use the vertical, W=1um

This code must be tuned and stable before using any function in the Blackhawk analog, and especially the PLL tuning. This is required for both functional and DFT modes.
A good default, mid-range value is 4’b0111, and an override option in the digital PMD is required.

The resistors do not need to be re-calibrated as the temperature and voltage change. Only process variations are compensated for, and so a one-time calibration after each power up is sufficient.

Expected range, ~code 3 to 12</td>
</tr>
</table>

20. Description of PLL Control and Status Register Pins –- default = 0, except for xxx = 1

Imax, imode(sign), imin control provides +- 12 and 25 % variation of bias currents

PLL / TX Clock Generator, same definitions for both PLLs	
Pin name	**Description**
TBD	PMD Register Name = AMS PLL CONTROL_*
pll_ctrl<175:174>	reserved
pll_ctrl<173:172>	tx_clkrptr_bw<1:0> – similar to pll_ctrl<73:72>
pll_ctrl<171:169>	tx_clkrptr, max, mode, min – bias currents for TX clock repeater buffers, 3P1C/calR
pll_ctrl<168>	tx_clkrptr_pd – power down for the clock repeater buffers which send the TX IQ clks from one quad to the other one
pll_ctrl<167:166>	reserved
pll_ctrl<165:164>	rx_clkrptr_bw<1:0> – similar to pll_ctrl<73:72>
pll_ctrl<163:161>	rx_clkrptr, max, mode, min – bias currents for RX clock repeater buffers, 3P1C/calR
pll_ctrl<160>	rx_clkrptr_pd – power down for the clock repeater buffers which send the RX IQ clks from one quad to the other one
0xD119<15:0>	
pll_ctrl<159>	fracn_sel – master enable and select for the frac-N mode, disables the original integer mode controlled by pll_mode<4:0>
pll_ctrl<158>	ditheren – now only a test mode, enables dithering to reduce the refclk spur, and can be used during frac-N integer mode
pll_ctrl<157:148>	fracn_ndiv_int<9:0> – fractional-N feedback divider integer control (divider ratio = code) This value is added to fractional part (value is restricted to 12 to 251) or can be used directly to generate any integer divide ratio (value is 8 to 255). **A programmed value must account for the initial div2 stage after the VCO, eg 147.2 = 2x 73.6, where the 2x is fixed and the 73.6 is the programmed integer + fractional value for franc_div_int<9:0>**
pll_ctrl<147>	fracn_bypass – test option to bypass the integer mode of the frac-N SDM block div8/9: fracn_ndiv_int<9:4> = M = ceil(N/9 – 1), fracn_ndiv_int<3:0> = A = 9M + 9 – N div4/5: fracn_ndiv_int<9:4> = M = ceil(N/5 – 1), fracn_ndiv_int<3:0> = A = 5M + 5 – N
pll_ctrl<146>	fracn_divrange – selects MMD integer range for the value programmed by fracn_ndiv_int<9:0> 0 = 8/9, ndiv range 60-251 1 = 4/5, ndiv range 12-123

<table>
<tr><td></td><td>Based on jitter and timing margin, it does not matter which mode is used for the overlap range, 60-123. For both modes, the duty cycle of the fdbck clock is typically not close to 50%, eg could be 80%, or the same for the two fracn_divrange modes.</td></tr>
<tr><td>pll_ctrl<145:144></td><td>fracn_div<17:16> - upper two MSB bits for fractional divider <17:0></td></tr>
<tr><td>0xD118<15:0></td><td></td></tr>
<tr><td>pll_ctrl<143:128></td><td>fracn_div<15:0> - lower 16 bits
Fractional control of feedback divider
Divider fraction = fracn_div<15:0>/2^{18}
E.g., for fractional value 0.6; this value is set to hex(0.6*2^{18}) = 18'h26666</td></tr>
<tr><td>0xD117<15:0></td><td></td></tr>
<tr><td>pll_ctrl<127></td><td>Mix3P1CR_PTATADJ[4:0] – PTAT bias control for Mix3P1C/R, which is used in the RX</td></tr>
<tr><td>pll_ctrl<126>
pll_ctrl<125>
pll_ctrl<124>
pll_ctrl<123></td><td><table>
<tr><td>00000:OFF</td><td>00001:+65.2%</td><td>00010:+60.9%</td><td>00011:+56.5%</td></tr>
<tr><td>00100:+52.2%</td><td>00101:+47.8%</td><td>00110:+43.5%</td><td>00111:+39%</td></tr>
<tr><td>01000:+34.8%</td><td>01001:+30.4%</td><td>01010:+26.1%</td><td>01011:+21.8%</td></tr>
<tr><td>01100:+17.5%</td><td>01101: +13.0%</td><td>01110: +8.7%</td><td>01111: 4.4%</td></tr>
<tr><td>10000: 0%</td><td>10001: -4.4%</td><td>10010: -8.7%</td><td>10011: -13.0%</td></tr>
<tr><td>10100:-17.5%</td><td>10101:-21.8%</td><td>10110:-26.1%</td><td>10111:-30.4%</td></tr>
<tr><td>11000:-34.8%</td><td>11001:-39%</td><td>11010:-43.5%</td><td>11011:-47.8%</td></tr>
<tr><td>11100:-52.5%</td><td>11101:-56.5%</td><td>11110: -60.9%</td><td>11111: -65.2%</td></tr>
</table></td></tr>
<tr><td>pll_ctrl<122></td><td>Mix3P1CR_CTATADJ[4:0] – CTAT bias control for Mix3P1C/R</td></tr>
<tr><td>pll_ctrl<121>
pll_ctrl<120>
pll_ctrl<119>
pll_ctrl<118></td><td>Same decoding table as for PTAT, but the default is 11100, -52.2%</td></tr>
<tr><td>pll_ctrl<117></td><td>vcodiv_refout – enables VCO divided by integer value, eg 80, set by pll*_mode<4:0> and sent to pll*_refoutp/n</td></tr>
<tr><td>pll_ctrl<116></td><td>ndiv_frac_valid – toggle high, then low to load in a new value for fracn_div<17:0>. This new mode should minimize any glitches when the fractional value is changed dynamically.</td></tr>
<tr><td>pll_ctrl<115></td><td>pfd_ref_skew – adds ~150ps of delay in refclk path</td></tr>
<tr><td>pll_ctrl<114></td><td>pfd_fb_skew – adds ~150ps of delay to fdbck path</td></tr>
<tr><td>pll_ctrl<113></td><td>pfd_skew_enlarge – increases above delays to ~300ps. All are optional settings for frac-N mode.</td></tr>
<tr><td>pll_ctrl<112></td><td>test_fracn_en – test mode to power up fracn block when using the integer block and check for noise</td></tr>
<tr><td>0xD116<15:0></td><td></td></tr>
<tr><td>pll_ctrl<111></td><td>refclk_doubler – test mode pending lab data, increases internal refclk freq by 2x and should be useful for the frac-N mode to reduce the Q noise</td></tr>
<tr><td>pll_ctrl<110:108></td><td>doubler _res[2:0] – increases supported refclk freq by reducing delay with lower res. For 156.25 MHz</td></tr>
</table>

<table>
<tr><td></td><td>input freq, the default is 110 for the best duty cycle of the 2x output clock, ~30-50% over PVT. Must also set pll_ctrl<106:104> = 011.</td></tr>
<tr><td>pll_ctrl<107></td><td>set_clk4pcs<2> - add 3rd bit to expand divider options, see complete table in defintion for pll*_clk4pcs</td></tr>
<tr><td>pll_ctrl<106:104></td><td>doubler _cap[2:0] – increases supported refclk freq by reducing delay with lower cap</td></tr>
<tr><td>pll_ctrl<103></td><td>clk4sync_en – enables clk4sync</td></tr>
<tr><td>pll_ctrl<102></td><td>clk4sync_div – sets clk4sync output freq
0 8T, 1 6T, and T = 1/VCO freq</td></tr>
<tr><td>pll_ctrl<101></td><td>Rterm300 – set refclk termination impedance to 300 ohm differential, and typically used if three cores are connected together in the package and share a common external clock source.</td></tr>
<tr><td>pll_ctrl<100></td><td>TBD - RtermHiZ – set refclk termination impedance to HiZ, and typically used if the ptestp/n bumps are connected to the refclkp/n bumps in the pkg TBD</td></tr>
<tr><td>pll_ctrl<99></td><td>Rterm400 – set refclk termination impedance to 400 ohm differential, and typically used if four cores are connected together in the package and share a common external clock source.</td></tr>
<tr><td>pll_ctrl<98></td><td>refclk_div4 – divides the input refclk by 4, and is applied to a refclk that is sourced from either the bumps or the internal lcref clk channel.</td></tr>
<tr><td>pll_ctrl<97></td><td>refclk_div2 – divides the input refclk by 2. Bits pll_ctrl <98> and <97> must not be asserted at the same time. To avoid glitches on the refclk, these two bits should be set with strap pins, or similar.</td></tr>
<tr><td>pll_ctrl<96></td><td>Rterm200 – set refclk termination impedance to 200 ohm differential, and typically used if two cores are connected together in the package and share a common external clock source.
To avoid glitches on the refclk, this bit should be set with a strap pin, or a register bit that is not driven by the BH refclk.
The package routing should use ~200 ohm routing impedances as needed and where feasible.</td></tr>
<tr><td>0xD115<15:0></td><td></td></tr>
<tr><td>pll_ctrl<95></td><td>Mix3P1CcalR_PTATADJ[4:0] – bias control for Mix3P1C/calR</td></tr>
<tr><td></td><td></td></tr>
<tr><td>pll_ctrl<94>
pll_ctrl<93>
pll_ctrl<92>
pll_ctrl<91></td><td>
<table>
<tr><td>00000:OFF</td><td>00001:+65.2%</td><td>00010:+60.9%</td><td>00011:+56.5%</td></tr>
<tr><td>00100:+52.2%</td><td>00101:+47.8%</td><td>00110:+43.5%</td><td>00111:+39%</td></tr>
<tr><td>01000:+34.8%</td><td>01001:+30.4%</td><td>01010:+26.1%</td><td>01011:+21.8%</td></tr>
<tr><td>01100:+17.5%</td><td>01101: +13.0%</td><td>01110: +8.7%</td><td>01111: 4.4%</td></tr>
<tr><td>10000: 0%</td><td>10001: -4.4%</td><td>10010: -8.7%</td><td>10011: -13.0%</td></tr>
<tr><td>10100:-17.5%</td><td>10101:-21.8%</td><td>10110:-26.1%</td><td>10111:-30.4%</td></tr>
<tr><td>11000:-34.8%</td><td>11001:-39%</td><td>11010:-43.5%</td><td>11011:-47.8%</td></tr>
<tr><td>11100:-52.5%</td><td>11101:-56.5%</td><td>11110: -60.9%</td><td>11111: -65.2%</td></tr>
</table>
</td></tr>
</table>

pll_ctrl<90>	Mix3P1CcalR_CTATADJ[4:0] – bias control for Mix3P1C/calR
pll_ctrl<89>	Same decoding table as for PTAT, but the default is 11100, -52.5%
pll_ctrl<88>	
pll_ctrl<87>	
pll_ctrl<86>	
pll_ctrl<85:84>	test_pnp<1:0> - measure internal BG nodes, NPN 00 – off, 01 – Vbe, 10 – Vbe2, 11 – Vbe_low To fully enable this mode, pll_ctrl<83,82,81> = 010
pll_ctrl<83>	vbypass – test, bypass test port opamp buffer for Vbias and Vbg modes
pll_ctrl<82>	bgint – test enable and measure Vbg internal, ~0.4V, using BG res, and P/CTAT portions. Must not be enabled during functional operation.
pll_ctrl<81>	bgip – test, measure Ibg internal PMOS current, ~40 uA, or 20 uA each for P/CTAT
pll_ctrl<80>	max test port amplitude – 325 mVppse, with 50 ohm termination, default ~250 mVppse. Also, see pll_ctrl<59:57>.
0xD114<15:0>	
pll_ctrl<79>	force_rescal with pll_ctrl<15:12>
pll_ctrl<78>	force_kvh_bw – enable force KVH, BW, test_vco2_cssw modes
pll_ctrl<77>	kvh_force[1] – force Kvco, override tuning control
pll_ctrl<76>	kvh_force[0]
pll_ctrl<75>	vddr_bgb – select between PVDD or BG, default, Vreference for the PLL bias currents
pll_ctrl<74>	test_vddr4bg – test mode to force VddR bias to BG. Also set pll_ctrl<67:64> = 1111, and both 3P1C CTAT to 10000 and PTAT to 00000
pll_ctrl<73:72>	pll2rx_clkbw<1:0> - controls BW of PLL output buffers for the RX/TX clks, helps to reduce the TX PI INL, valid only when pll_ctrl<78>=1 Use 11 15-22.6G, 01 23-25.78G, 00 26-30G
pll_ctrl<71>	BGR_CTATADJ[3] – BG CTAT bias control 0000: 117.5% 1000: 98% 0001: 115% 1001: 95% 0010: 112.5% 1010: 92.5% 0011: 110% 1011: 90.0% 0100: 107.5% 1100: 87.5% 0101: 105% 1101: 85% 0110: 102.5% 1110: 82.5% 1111: OFF, force PTAT 2x, both CTAT and PTAT = F to set Ibg = 0 **0111: 100% (default)**
pll_ctrl<70>	CTATADJ[2]
pll_ctrl<69>	CTATADJ[1]
pll_ctrl<68>	CTATADJ[0]
pll_ctrl<67>	BGR_PTATADJ[3] – BG bias, same decoder as CTAT
pll_ctrl<66>	PTATADJ[2]

pll_ctrl<65>	PTATADJ[1]
pll_ctrl<64>	PTATADJ[0]
0xD113<15:0>	
pll_ctrl<63>	test_rx (send RX word ck to PLL test port)
pll_ctrl<62>	test_pll (output divided VCO ck), both on – test LC
pll_ctrl<61>	test_vc (test Vcontrol) – see Sec 36
pll_ctrl<60>	test_vref
pll_ctrl<59>	imax (iop[2] – test current, and bias for test port
pll_ctrl<58>	imode (iop[0])
pll_ctrl<57>	imin (iop[1])
pll_ctrl<56>	imax (icomp[2] – VCO comparator)
pll_ctrl<55>	imode (icomp[0])
pll_ctrl<54>	imin (icomp[1])
pll_ctrl<53>	imax (icmldiv[2] – CML dividers after VCO mux/div
pll_ctrl<52>	imode (icmldiv[0]) – ibias is BGR
pll_ctrl<51>	imin (icmldiv[1])
pll_ctrl<50>	imax (irxclkbuf[2] – VCO mux/div and RX/TX clock output buffers
pll_ctrl<49>	imode (irxclkbuf[0]) – ibias is 3P1CcalR
pll_ctrl<48>	imin (irxclkbuf[1])
0xD112<15:0>	
pll_ctrl<47>	imax (ick[2] – refclk input buffer)
pll_ctrl<46>	imode (ick[0])
pll_ctrl<45>	imin (ick[1])
pll_ctrl<44>	imax (icp[2] -- charge pump)
pll_ctrl<43>	imode (icp[0])
pll_ctrl<42>	imin (icp[1])
pll_ctrl<41>	imax (ibias all 6 above) – master diode in biasgen
pll_ctrl<40>	imode (ibias) – sign is reversed vs current sources
pll_ctrl<39>	imin (ibias)
pll_ctrl<38>	refh_pll – when pll_ctrl<75>=1, increase Ibias 10%
pll_ctrl<37>	refl_pll – when pll_ctrl<75>=1, decrease Ibias 10%
pll_ctrl<36>	vdd88_en – keep bias currents at 100uA if PVDD0P8 = 0.88V, typ
pll_ctrl<35>	iqp[3] - charge pump current, 50,100,150,..800uA
pll_ctrl<34>	iqp[2] - default = 800uA
pll_ctrl<33>	iqp[1] - but ~300-400uA seems best for over PVT
pll_ctrl<32>	iqp[0]
0xD111<15:0>	
pll_ctrl<31>	enable_ftune – comparator for VCO tuning

pll_ctrl<30>	pll_reset, active high – OR'd with dedicated bit
pll_ctrl<29>	ivco<2>, max, min, mode
pll_ctrl<28>	ivco<1>
pll_ctrl<27>	ivco<0>
pll_ctrl<26>	test_vco2_cssw – test mode to disable current bias and convert the current source to a switch. Could help with start up problems. Was vco_inductor
pll_ctrl<25:24>	VCOIctrl<1:0> - adjusts VCO bias current, ~6% steps. Only active if pll_ctrl<21> = 0.
pll_ctrl<23>	vco2_15g – enable and select the 15-22.6G VCO
pll_ctrl<22>	muxdiv_ictrl<1> – bias current control, was autogm 00 default 01 10% more current 10 5% less current 11 10% less current
pll_ctrl<21>	vco_res_cs – test mode to enable a resistor only current bias for the main VCO, should reduce RJ, but with possibly worse PSRR
pll_ctrl<20>	muxdiv_ictrl<0> – bias current control
pll_ctrl<19>	drv_hv_disable, must be 1'b0 if TVDD1P20=1.20V, should now be in the TX section
pll_ctrl<18,17,16>	comp_thresh<2:0> - VCO tuning threshold 000 = 0mV, 001 = -100mV, **010 = -150mV**, 011 = -200mV, 100 = -250mV, 101 = -300mV, 110 = -350mV, 111 = -400mV, all Vdiff at internal comparator. The measured voltage at PTESTP/N will typically be about 30mV lower. After tuning the PLL, if these bits are swept and the state of pll_low is monitored, the internal VCO voltage can be roughly measured without using the analog PLL test port.
0xD110<15:0>	
pll_ctrl<15:12>	rescal_aux[3:0] – over-ride ana_rescal<3:0> if force_rescal, pll_ctrl<79> = 1
pll_ctrl<11>	refclk1x – keeps refclk output freq at 1x even if refclk_div2 or refclk_div4 are enabled
pll_ctrl<10:9>	lpf_Rz<1:0> - adjust Rz in loop filter 00 = 0.71K, **01 = 1K**, 10 = 1.7K, 11 = 5K
pll_ctrl<8>	fp3_rh – adjust res in 3rd pole by 4x
pll_ctrl<7:4>	fp3_ctrl<3:0> - adjust caps in 3rd pole, typically used in the frac-N mode, and with fp3_rh, higher code = lower pole freq
pll_ctrl<3:2>	cp_cmfdbk_iadj<1:0> - increase CP opamp current 00: 50uA, x1: CMF = 100uA, 1x: UG = 100uA
pll_ctrl<1:0>	set_clk4pcs<1:0> – program clock freq for clk4pcs, combine with pll_ctrl<107> See list of modes in pll*_clk4pcs description

0xD11C<15:0>	**PLL Status** – also in register map
pll_sts<15:14>	KVH<1:0>
pll_sts<13:6>	pll_range<7:0>, copy of VCO tuning code sent from digital tuning block in PMD
pll_sts<5>	pll_low
pll_sts<4:0>	pll_mode<4:0> - copy of value sent from digital

21. PLL Frequency Range and Programming – very similar to Falcon16

The VCO and PLL output frequency range is in two bands from 15-22.6GHz, and 22.6-30.0GHz, which are based on two VCOs. The first two tables below lists the division ratios for supported PLL output frequencies (OS1x data rate) and reference clock frequency pairs for VCO1 and VCO2. The VCO selection is controlled by this bit, pll_ctrl<23>, vco2_15g.

All the Ndiv division ratios are supported by the original 28nm integer mode divider table based on pll_mode<4:0>, and the new ones that must be supported with the integer block in the frac-N block have an asterisk, eg 100*, 240*, and 280*. For all divider modes, the frequency ranges for the two VCOs are the same, and so the correct VCO must be chosen based on the programmed frequency.

The fractional mode does increase the output jitter by a small amount and at this time, only a few OS2x and OS4x modes are supported by this mode. Test results are needed to determine if the added jitter is low enough for the high performance OS1x modes. In general, it is better to use as high a reference clock freq as is practical, but the max allowed refclk frequency is 425 MHz. This limit is set by the timing closure for the SDM block.

The OS2x and OS4x line rates are supported with local dividers in the RX and TX lanes, and are programmed using the rx(i)_osr_mode<1:0> and tx(i)_osr_mode<1:0> bits. These bits do not control the PLL, and so are listed here for reference only. A complete list is in the Falcon16 User Specification which is available from the PMD design team. Most of the half and quarter rates listed below are ones that have been used in the past with previous serdes cores such as 28nm Eagle, 40nm Warpcore and 65nm Hypercore.

More frac-N info to be added later?

Better definition of the force modes?

Use 312.5MHz for lower jitter for 50G modes

VCO1 (GHz) / Refclk (MHz)	23.0	24.0	24.576	24.75	25.0	25.6608	25.78125	26.25	26.5625	26.6672	27.34375	27.9525	28.0	28.05	28.125	30.0
100		240*											280*			
106.25 FC														264		
122.88 CPRI			200													
125 Ethernet	184			198	200								224			
155.52 SONET						165										
156.25 Ethernet	147.2			158.4	160		165	168	170		175				180	192
161.1328125 Ethernet							160									
166.67										160						
174.703125 OTU4												160				
212.5 FC														132		
312.5 Ethernet	73.6			79.2	80		82.5	84	85		77.5		89.6		90	96
KVH[1:0]	01	01	01	01	01	01	01	01	01	01	01	00	00	00	00	00
VCO tuning code, pll_range (typ)	50														245	250
RX/TX Lanes after Div2 (Gb/s)	11.5	12.0		12.375	12.5								14.0	14.025	14.0625	15.0
RX/TX Lanes after Div4 (Gb/s)	5.75	6.0	6.144		6.25			6.5625					7.0			

VCO2 (GHz) / Refclk (MHz)	15.0	15.625	16.0	16.5	16.667	17.0	18.75	19.6608	19.90656	20.0	20.625	21.0375	21.875	22.39488	22.5
100			160	165						200					
106.25 FC						160									
122.88 CPRI								160							
125 Ethernet	120									160	165		175		180
155.52 SONET									128					144	
156.25MHz Ethernet	96	100*					120		127.401984	128	132		140		
159.375 FC10G												132			
161.1328125 Ethernet											128				
166.67					100*					120					
212.5 FC						80									
312.5 Ethernet											66		70		
KVH[1:0]	11	11	11	11	11	11	11	01	01	01	01	01	01	01	01
VCO tuning code, pll_range (typ)	60														
RX/TX Lanes after Div2 (Gb/s)	7.5		8.0					9.8304	9.95328	10	10.3125	10.51875	10.9375		11.25
RX/TX Lanes after Div4 (Gb/s)	3.75							4.9152		5	5.15625				

The rates below are from Furia.

11.0957Gbps	OTU2e	158.51	PLL_DIV = 140 / OS2
		173.37	PLL_DIV = 128 / OS2
11.049107Gbps	OTU1e	157.844	PLL_DIV = 140 / OS2
		172.64	PLL_DIV = 128 / OS2
10.7546Gbps	OTL3.4	156.637	PLL_DIV = 140 / OS2
		168.04	PLL_DIV = 128 / OS2

The PLL output frequency is given by, $F_{vco} = F_{ref}$ x *Ndiv*
where, F_{ref} : reference clock frequency, typically 156.25MHz, 125MHz, or ~161.1MHz, and which can be from an external source or an internal on-chip source, eg from a step-up LCPLL or a master Falcon core

Ndiv : PLL feedback divider division ratio, programmable through *pll_mode[4:0]* :

pll_mode [4:0]	**Ndiv**	**Typ VCO Freq (GHz)**	**KVH[1:0]** (auto default) **TBD**	**PAD_PTEST / Refclk (freq ratio)**	**VCO2(2) pll_ctrl <23> = 1**	**Notes**
00000	64	20.625	11	8	2	refclk ~= 300+MHz
00001	66	20.625	11	1	2	“”
00010	80	25.78125	00	10	0	“”
00011	128	20.625	11	8	2	
00100	132	20.625	11	2	2	OS2 for main 10.31G
00101	140	21.875	11	2	2	
00110	160	25.0 25.78125	00	10	0	typ for OS2, OS4 refclk ~= 161.1MHz
00111	165	25.78125 25.6608	00	3	0	main 100G/25G std refclk = 155.52MHz
01000	168	26.25	10	6	0	typ for OS4
01001	170	26.5625	10	17	0	FEC for IEEE PAM4
01010	175	27.3475	01	5	0	HiGig27
01011	180	28.125	00	9	0	max rate
01100	184	23.0	10	23	0	Dune
01101	200	25.0	00	10	0	
01110	224	28.0	00	8	0	refclk = 125MHz
01111	264	28.05	00	4	0	FC32/16, 106.25MHz
10000	96	15.0	11	4	2	HMC and other
10001	120	18.75	00	5	2	
10010	144	22.39488	10	9	2	refclk = 155.52MHz
10011	198	24.75	01	3	0	OS2 for OTN
			(force values)		(force values)	other rates with force KVH and TF are TBD
00010	80	17.0	01?	10	2	FC8/4, 212.5MHz
00100	132	28.05	00	2	0	FC32/16, 212.5MHz
00110	160	17.0	01?	10	2	FC8/4, 106.25MHz
00110	160	27.9525	00	10	0	refc=174.703125MHz
10001	120	15.0	01	5	2	refclk = 125MHz

New for 16nm						
pll_mode [4:0]	**Ndiv_fr**	**Typ VCO Freq (GHz)**	**KVH[1:0]** force	**PAD_PTEST / Refclk (freq ratio)**	**VCO2(2) pll_ctrl <23>=1**	**Notes**
10001	120	20.0			2	Refclk = 166.67MHz
00110	160	26.6672	00			“”
00110	160	20.0			2	125MHz
00111	165	16.5			2	100MHz

VCO Freq (GHz)	Refclk Fref (MHz)	Ndiv	Integ	Frac	VCO2 force	KVH force	Notes, Application
15.625	156.25	100	50	0	2		PTEST = Refclk
16.667	166.67	100	50	0	2		
24.0	100	240	120	0		01	
28.0	100	280	140	0		00	
30.0	156.25	192	96	0		00	The RX and TX do not support 30G
		Fractional Modes					**Only OS2, 4x**
23.0	156.25	147.2	73	0.6			Dune
24.75	156.25	158.4	79	0.2			OTN

22. VCO Frequency Range Tuning – partial update

- The VCO range is typically tuned upon power up or a rate change by a state machine in the serdes digital. The usage of the tuning logic should be reviewed with the PMD team.
- Before tuning the PLL, the RESCAL code must be calibrated and stable
- The tuning algorithm starts with the PLL reset asserted, i.e., pll_reset =1, for at least 50us while pll_range[7:0] is set to 00h, the lowest VCO frequency range setting.
- Release the PLL reset and wait for up to 50us. If the PLL status signal pll_low = 0, stop tuning and set pll_range [7:0] to 00h; otherwise,
- Increment pll_range[7:0] by 1 and wait for at least 2us. If pll_low = 0, stop tuning and freeze pll_range [7:0] to the current value; otherwise,
- Repeat the above step until pll_low=0, and generally expect pll_range to tune to 3-252d.
- After the step sequence is done, wait for 50us and check for full frequency lock
- Make the step and wait times programmable from at least 2us to 50us
- A manual PLL re-tune can be forced by toggling the pll_seq_start bit, reg 0xD144, [15] to 1'b0 and back to 1'b. Expect vco_step_time = 8 for ~2us for refclk = 156.25 MHz.
- The tuned VCO control code, pll_range[7:0] can be read from 0xD11C, [13:6], or from 0xD149, [7:0]. Also, there is a force option using 0xD143, [15:8], [7].

23. PLL Bandwidth programming (optional)

The PLL bandwidth can be adjusted through the setting of charge pump current Iqp and loop filter zero resistor value Rz. The target BW = TBD MHz. This bandwidth programming is optional and Iqp, Rz should be set to their default values, which are 800 uA and 1.1 KOhm. Setting Rz = 1.7K may be needed for Ndiv >= TBD.

Charge Pump current setting:

iqp[3:0] (pll_ctrl[36:33])	Iqp
0000	50uA
0001	100uA
0010	150uA
0011	200uA
0100	250uA
0101	300uA
0110	350uA
0111	400uA
1000	450uA
1001	500uA
1010	550uA
1011	600uA
1100	650uA
1101	700uA
1110	750uA
1111	**800uA**

Rz setting:

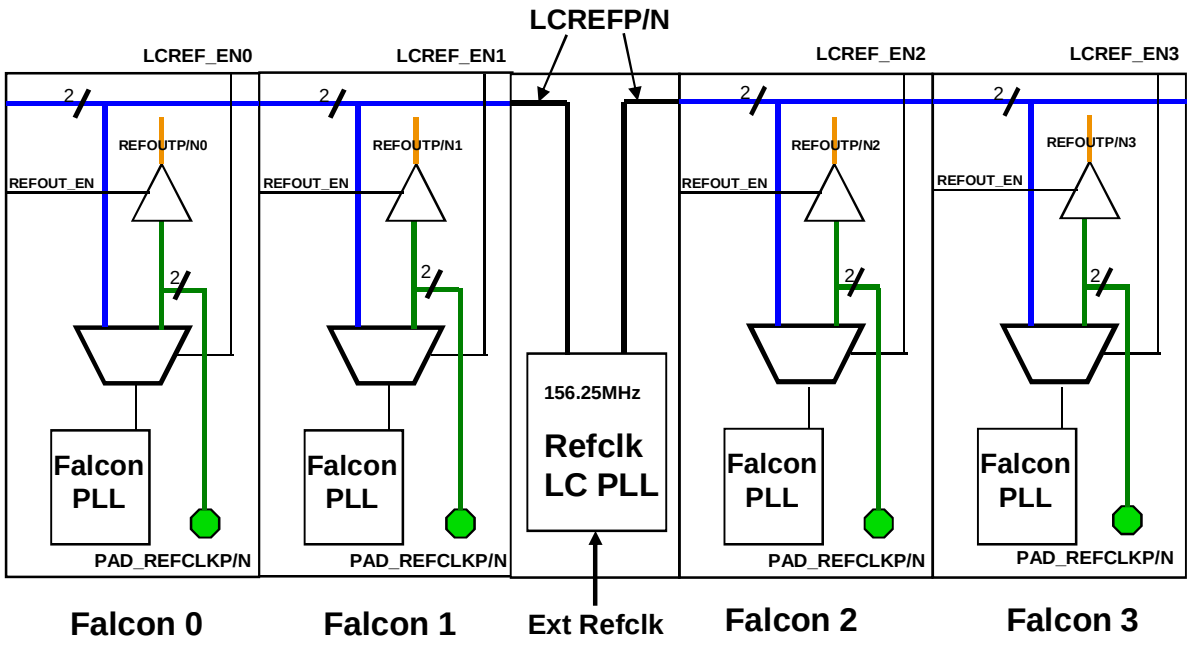
lpf_Rz[1:0] (pll_ctrl[10:9])	Rz
0	0.7KOhm
1	**1.1KOhm**
2	1.7KOhm
3	5.0KOhm

24. LC PLL Connections and Master/Slave Refclk Mode – updated for ver 0.99, more details needed for new refout mux mode

Up to seven Blackhawk serdes IPs can be driven by one LCPLL output buffer with differential, CML clock outputs. The total number also depends on the total routing length, ~10-11mm, and the best configuration is when all the cores are abutted to each other.

To fully enable this mode, set Blackhawk control lcref_en=1 for each receiving core/PLL. Also, see the next pages for info about how to set a couple of metal jumpers.

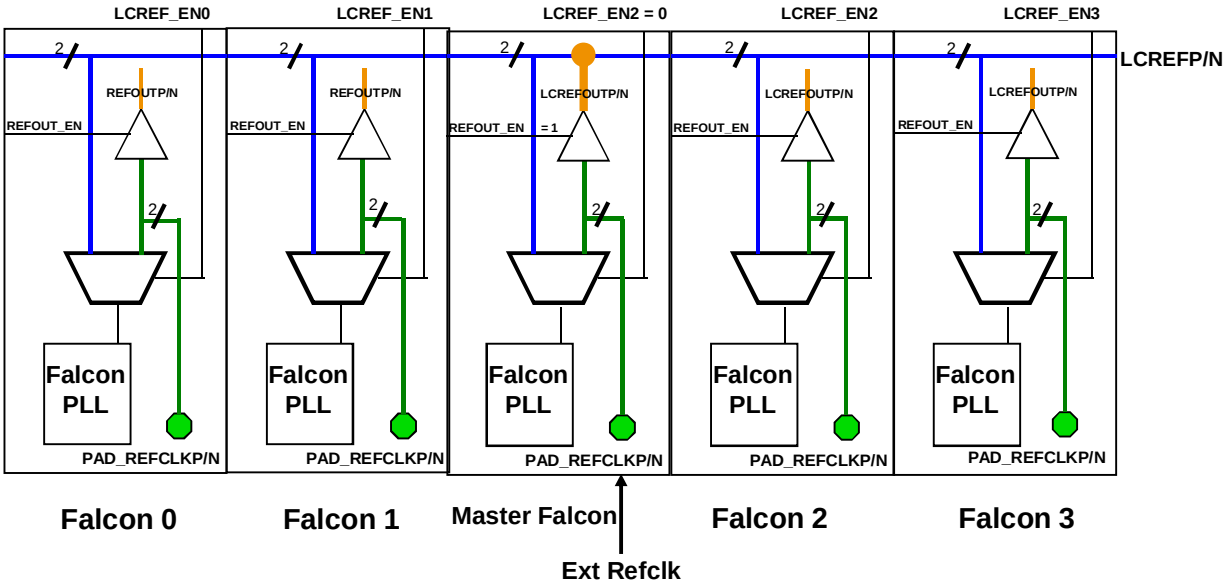
The LCREFP/N clocks are routed in Mr13 or Mr11 along the bottom or left side edges of the layout. Each trace is 2um wide, the P to N differential trace spacing is 5um, and the side spacing to a shield wall is 3um. The channel is passive, and there are no re-buffer stages.



Also, as shown below, each Blackhawk PLL has the ability to drive the LCREF bus with a buffered copy of the external PAD_REFCLK if it is connected. This “master” mode is enabled when REFOUT_EN=1, and if the refoutp/n pins are connected to the lcrefp/n, and sometimes the lcrefp/n_h, pins at the chip level. With this feature, a LCPLL is not needed if a low jitter, 156.25 MHz, or hihjer freq, external clock is available.

To fully enable this mode, set Blackhawk control lcref_en=1 for each receiving core, and lcref_en=0 for the master core. Also, see the next page for info about how to set a couple of metal jumpers.

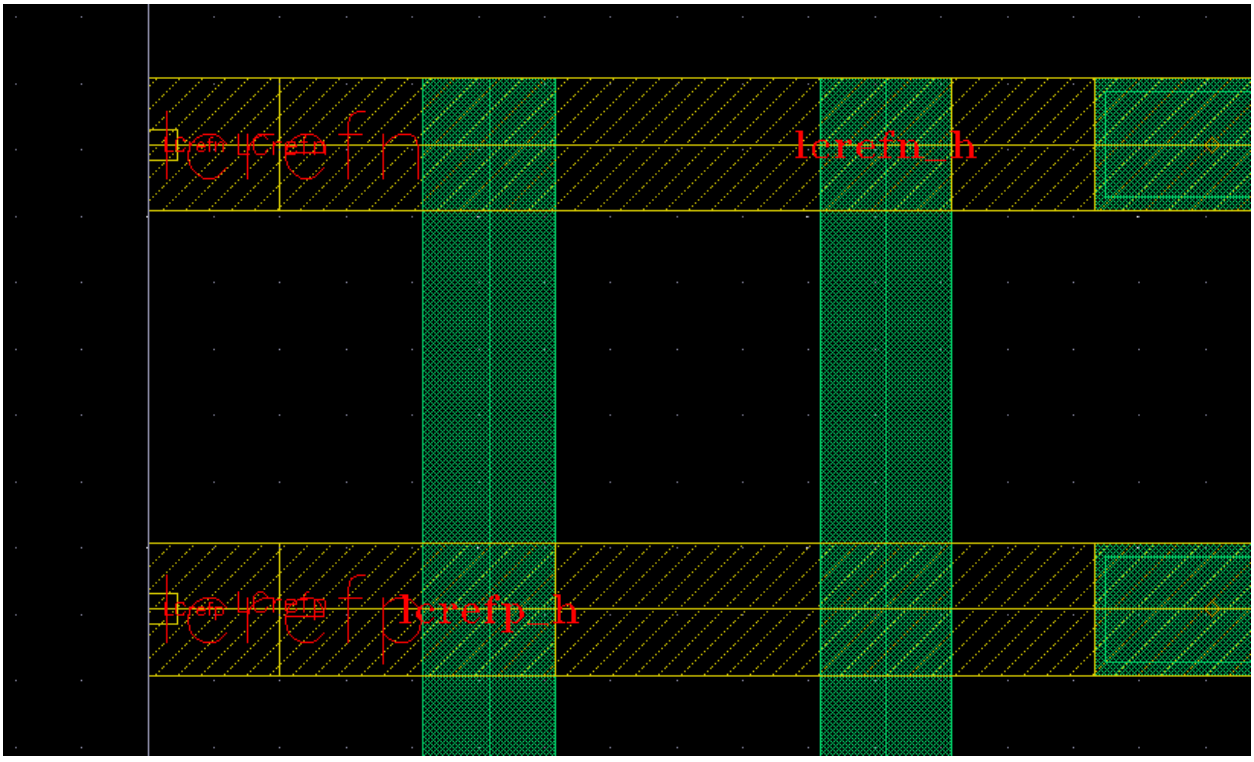
The maximum number of cores in a master/slave group is eight, and the maximum routing length ~= 11mm. The master mode cannot be enabled if there is a refclk LCPLL connected to the LCREF bus unless the LCPLL has a HiZ mode that is enabled.



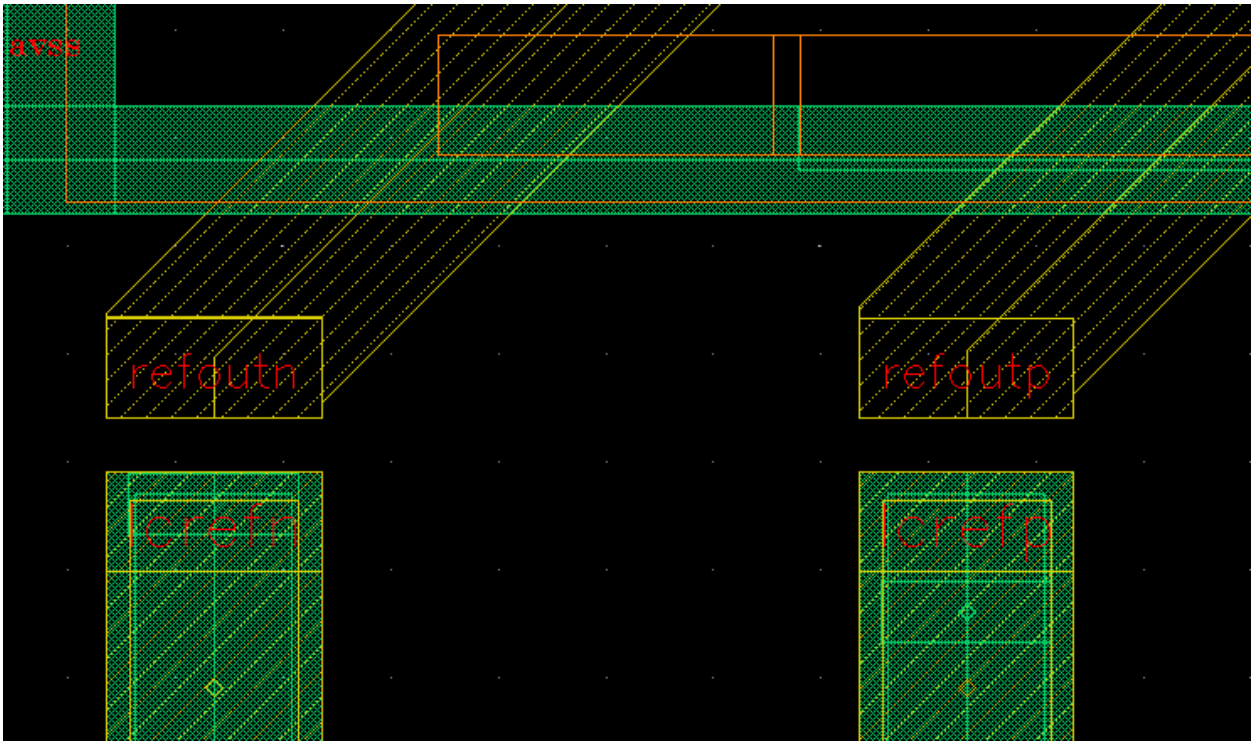
As mentioned above, there are a couple of metal jumpers than might need to be “set” in order to fully configure the use of the internal refclk routing.

For any receiving core, there are lcrefp/n pins along the left edge of the PLL and lcrefp/n_h pins along the bottom edge. The lcrefp/n pins are used when a vertical refclk channel is used, and the lcrefp/n_h pins are used when a horizontal refclk channel is used.

The side edge pins, lcrefp/n in M13/11, are always connected to the internal refclk buffer, but the lcrefp/n_h pins, M12/10, are floating and if used, must be connected to the lcrefp/n pins and the internal buffer by adding a 2x2 VIA12 or VIA10 in the two locations shown below at approx. X,Y = 8,243. In this case, the lcrefp/n and lcrefp/n_h signals are connected together.

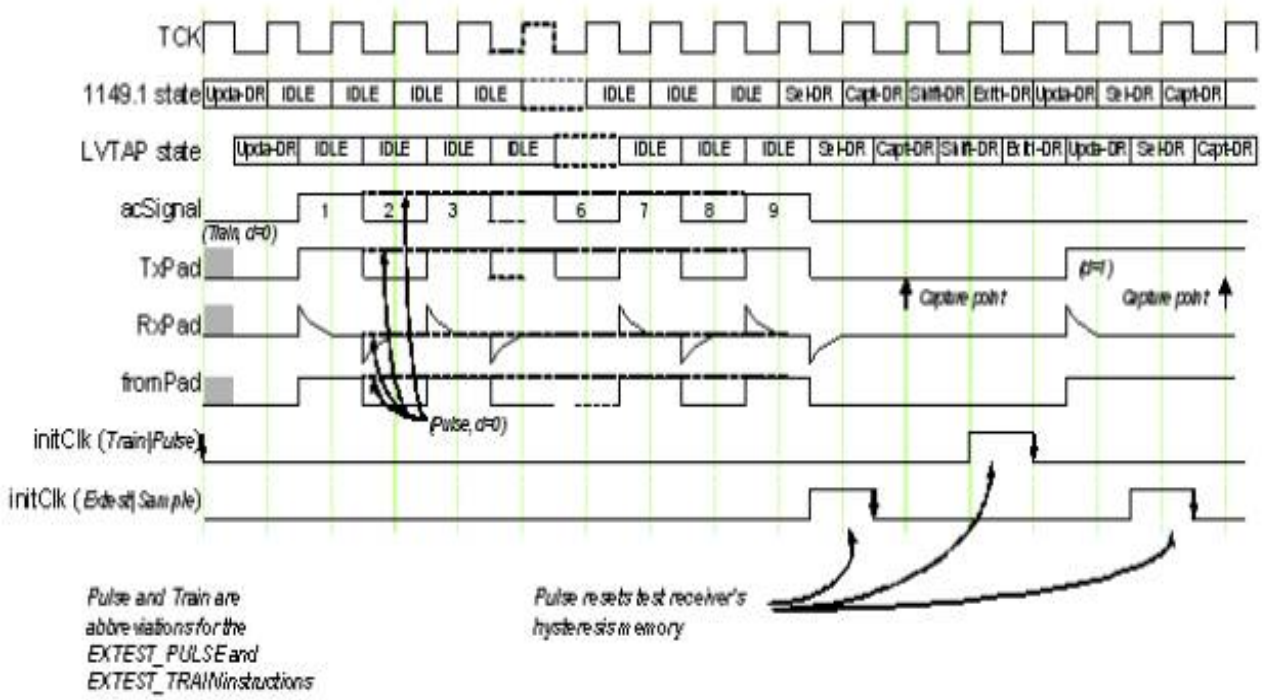


To configure a core as a master, M13 jumpers must be added at approx. X,Y = 93,263



25. AC-JTAG Timing Diagram

Figure 1-1. Waveforms Illustrating IEEE 1149.6 Timing



26. AC-JTAG Pin List

ACJTAG *i* = [7:0] The default setting for all JTAG inputs = 0		
I/O	**Pin name**	**Description**
I	test_jtag	Asserts AC or DC JTAG operation, but over-ridden by pll_iddq
I	test_ac_mode	ac_mode=1 enables AC testing, allow 0.5ms to 5ms, which depends on the AC cap values, for complete power up and voltage settling before executing TRAIN or PULSE mode
I	test_rxacj_st[5:0]	Receiver configuration bits [5] Enable internal AC cap Default, '0", is for external AC cap [4:2] Hysteresis – see table in Sec 21 [1:0] Filter BW 00 – 8.5MHz, default 01 – 11MHz 10 – 16MHz 11 – Force Vcm, final default mode
O	test_rxdn[*i*]	Single-ended received data from RDN
O	test_rxdp[*i*]	Single-ended received data from RDP
I	test_rxd_init_mem	Initial value set enable for rxdp/n_init_val[*i*]
I	test_rxdn_init_val[*i*]	Initial value of hysteresis comparator -
I	test_rxdp_init_val[*i*]	Initial value of hysteresis comparator +
I	test_txacj_st[3:0]	Transmitter configuration bits ~~[7:3] reserved~~ ~~[4] Clock or pulse to load [3:0], expect TCK to drive this bit, allow >= 2 cycles~~ [3:0] Driver output amplitude, mapped to upper 4-bits of main tap see table in Sec 21, needs updates
I	test_txd[*i*]	Transmit data from boundary scan
All digital interface signals are standard 0.8V CMOS logic signals with pin terminals generally in metal layers 3 and 5		

27. Drive Strength of Analog CMOS Outputs to Digital Core – updated for ver 0.99

Signal name	NMOS size	PMOS size	Digital 10-track std cell
refclk			P10U16A_CKINVX8
fdbck			P10U16A_CKINVX8
pll_low			P10S20A_AND2X4
tx_wclk20			P10U16A_BUFX4
rx*i*_data[59:0]			P10L16A_BUFX12
rx*i*_p1_err[39:0]			P10L16A_BUFX12
rx*i*_m1_err[19:0]			P10L16A_BUFX12
rx*i*_rclk20			P10L16A_CKINVX6 x4
rx*i*_sigdet			P10S20A_INVX16
test_rxd[p:n]			P10L16A_INVX16

28. Duty Cycle and Jitter Specifications for the PLL, RX, and TX Digital Clocks – most max clock freqs are based on max VCO freq ~= 28.3 GHz

Signal Name	Max Frequency (MHz)	Duty Cycle, High, +/-5%	Long Term (RJ) (ps-rms)	Period Jitter (+/-, ps)
PLL – no PI				
pll*i*_clk4pcs	1770	50	0.5	25
pll*i*_clk4sync	3510	50	0.5	15
pll*i*_fdbck	425	varies 15% - 85% with pll_mode and fracN divider settings	0.5	large, ~12%, for fracN mode
pll*i*_refclk	425	varies with input refclk source, 40-60%	0.5	50
TX – after PI				
tx*i*_clk32	885	50	0.5	35
tx*i*_clk66	430	48	0.5	35
tx*i*_wclk20	1415	50	0.5	25
RX – after PI				
rx*i*_clk32	885	50	0.5	35
rx*i*_clk66	430	48	0.5	35
rx*i*_wclk20	1415	60	0.5	25

29. Analog/Digital Interface Timing – TBD, and add timing digram

- Data is launched from the analog core on the falling edge of the RX 20T word clock, which has a 60% High, 40% Low, duty cycle. The clock to data delay is approx one clk2q of a std cell FF.
- The data from the digital TX must be available at the inputs to the analog TX no later than 360 ps after the rising edge of the TX 20T word clock. Therefore, at the max data rate of 28.3 GBd, Tsu = 350 ps. There is also a hold requirement of 100 ps. TBD for BH
- The max transition time for the TX data and the phase interpolator inputs is 100 ps.
- The timing for the digital control lines for the phase interpolator should be constrained so that the maximum skew between any two lines is < 100 ps.
- The duty cycles of the RX and TX word clocks are accurate to within +/-5%.
- To avoid logic glitches, the max allowed digital noise is TBD, but probably ~100 mV.
- A detailed verilog model of the analog behavior is available. In general, the PLL is modeled at the behavioral level, but the RX and TX signal paths are more similar to a gate level netlist.

30. Electrical specifications – Not fully updated for 16nm and PAM4 stds

Falcon25G is designed for compliance to the electrical specs of many standards, including

CEI 6G-LR, SR
XFI – all specs except for Return Loss
XFI+, XLAUI
SFP+ Optical and DAC
QSFP, XLPPI and 40G-CR4, 802.3, 10G-KR
CEI 11G-SR, CEI 25G-LR, SR
IEEE 100G-KR4/CR4 std, 802.3bj
CEI 28G-VSR, SR
CEI 28G-LR is TBD
FC32 is TBD, add CAUI4

However, in some cases, e.g. Return Loss, the actual tested compliance will depend on other factors such as, the package substrate design, and the signal integrity of the test setup.

Standard/Document	Abbreviation	Description
OIF CEI 56G drafts	CEI-56G-LR CEI-56G-MR CEI-56G-VSR	
IEEE 802.3bs-draft	CDAUI-8-c2m CDAUI-8-c2c	
OIF CEI 25G drafts	CEI-25G-LR CEI-25G-SR CEI-25G-VSR	
IEEE 802.3-2008	803.3-2008	All Ethernet speeds up to 10G Backplane Ethernet – clause 69 Backplane channel specs – Annex 69B 1G KX – clause 70 KX4 – clause 71 KR – clause 72 AN – clause 73 FEC – clause 74 10G SR & LR XAUI
IEEE 802.3ba -2010	802.3ba	XLAUI, CR4, SR4, LR4, PPI (Quad SFI)
Specifications for Enhanced Small Form Factor Pluggable Module SFP+	SFF-8431	SFI for optics, copper
FIBRE CHANNEL Physical Interface-3 (FC-PI-3) REV 3.0	XFI+	Updated spec for XFI
OIF CEI 2.0	CEI-6G-SR CEI-6G-LR	

PARAMETER	SYMBOL	DESCRIPTION	MIN.	TYP.	MAX.	UNIT
Operating conditions and Power Dissipation						
Process		13ML, 11ML, flip-chip only, SVT, LVT, ULVT, D-Nwell	16nm FinFet+			
Supply voltage 1 for RX, TX, PLL	VDD0P8	Measured at the outside of the package, and assumes 10mV max IR drop in the package. Might need AVS for SS lots.	0.776	0.80	0.84	V
Supply voltage 2 for TX driver	VDD1P2	Using 1.2 V is required for 20-28G LR, but might be optional for 25G-VSR, 10G and lower rates. If 0.8 V is used, the TX amplitude will be marginal for 800 mVppd, min	1.14	1.20	1.26	V
Operating temperature	Tj	Junction temperature Max 125C for 1000 hours	-40		110	^{o}C
Power dissipation, quad 53G KR/LR, eg 200G port over 30 dB channel	$P_{TOT-KR4}$	DFE on and 1.0 Vppd TX output, add ~10 mW/lane for independent clock lane mode with clk rtpr buffers enabled. For 28G, increase ~4%		920	1150	mW
Power dissipation, quad 53G SR/VSR, eg 200G port over 20/10 dB channel	$P_{TOT-SR4}$	Reduced DFE and 0.8 Vppd TX output. For 28G, increase ~4%		800	1000	mW
Power dissipation, quad 25.78G, 100G-KR4	$P_{TOT-KR4}$	DFE on and 1.0 Vppd TX output. For 28G, increase ~8%		780	970	mW
Power dissipation, quad 10G-KR	P_{TOT-KR}	Reduced DFE and 1.0 Vppd TX output.		460	575	mW
Current consumption - IDDQ	I_{DDQ}	All blocks off		15		mA
Baud, symbol rate	B_{PS}	Lower rates, eg 1.25G, might be supported in the digital core	3.75		28.3	Gbd
Unit interval	UI		35.33		266.6	ps

PLL and Clock Generator						
Clock frequency	F_{pll}	LC VCO #1 LC VCO #2	22.6 15.0		30.0 22.6	GHz
PLL output jitter	Δt_{ϕ}	Random, RMS value		8	10	mUI
	Δt_{PLLdet}	Deterministic, peak-peak. Requires a well filtered power supply for PVDD1P0.			20	mUI
Output clock phases	N_{ϕ}	Internal, to both RX and TX		4		
Loop bandwidth	BW			TBD		MHz
Lock time		varies with VCO freq, which affects the tuning code value Lock time = Tpre + Tstep + Tfreqcheck			TBD	
Reference clock frequency	F_{ref}	From either the external or internal differential inputs	106.25	156.25	425	MHz
Reference clock amplitude	V_{ref}	Differential p-p, AC coupled, or from internal LCref bus	0.8	1.0	1.4	V
Reference clock rise time	t_{refLH}	20%/80% for min amplitude		300	400	ps
Reference clock fall time	t_{refHL}			300	400	ps
Reference clock phase noise	$\phi_n$ref	@ 10KHz			-110	dBc/Hz
		@100KHz			-130	dBc/Hz
		@1MHz			-130	dBc/Hz
		@10MHz			-150	dBc/Hz
		@ 100MHz			-150	dBc/Hz
Reference clock jitter	σ	Integrated, 12kHz – 20MHz			0.3	psrms
Reference clock input impedance, DC	$R_{inrefclk}$	Differential, integrated on-chip	80	100	120	Ω
Reference clock input common-mode voltage	V_{CM-PLL}	Should be AC coupled with an external cap, and Vcm-pll is set by an internal bias circuit Now with internal AC cap.		0.4		V
Current consumption	I_{PLL}	Includes all RX and TX clock buffers in one PLL		98		mA

PARAMETER	SYMBOL	DESCRIPTION	MIN.	TYP.	MAX.	UNIT
Receiver						
Input voltage. differential	V_{id}	Input eye must meet RX Eye Templates from applicable stds. For Vid = 1.6Vppd, lower Vcm, set rx_ctrl<29> = 1	85		1600	mV
Input voltage, common-mode wrt RX ground	V_{CM-RX}	An AC cap is included on die, and the input Vcm is ~floating. For inputs with a higher Vcm voltage than the Max, an external AC cap is still needed, and which should be 100nF.		750	900	mV
Input referred offset	V_{off}	data / phase comparator		1		mV
Input referred noise	V_{off}	data / phase comparator		???		mVrms
Input impedance, DC	R_{in}	Differential, integrated on-chip	80	95	120	Ω
Input impedance, AC	RL_{RX}	Meets 100G-KR4, OIF-CEI 25/11/6G, XLAUI, XFI+, SFP+, QSFP, 10G-KR, XAUI, CX-4, return loss templates				
Input bandwidth	BW_{in}	-3dB level	12			GHz
Input gain	$Gain_{in}$	From filter input to slicer input, VGA code 0			-2	dB
Input gain	$Gain_{in}$	From filter input to slicer input, VGA code 39	10			dB
Bit error rate	BER				10^{-12}	s^{-1}
Jitter tolerance – Meets XAUI, XLAUI, XFI+, SFP+, QSFP, KR jitter tolerance templates.	Δt_{RXtot}	Total, peak-peak			0.65	UI
	Δt_{RXdet}	Deterministic, peak-peak			0.37	UI
Input differential skew	t_{skewi}	50% rising/falling versus 50% falling/rising edge			TBD	UI
Signal detect threshold	V_{id}	CX-4 compliant at 3.125Gb/s	50		175	mV
Latency, data path	T_{DRX}	From input to internal digital		23	TBD	UI
Latency, phase interpolator				TBD		
Current consumption	I_{RX-V1}	Per lane for 53G PAM4 KR/LR		200		mA

PARAMETER	SYMBOL	DESCRIPTION	MIN.	TYP.	MAX.	UNIT
Transmitter						
Output voltage, differential, TVDD1P2=1.2V	$V_{od1p25V}$	Programmable in ~100 steps. Approx. range. See Sec 15	0	1	1.05	V_{ptpd}
Output voltage, common-mode	V_{ocm}	Vocm ~= 0.9V/2 when the TX is terminated with 100 Ohm, diff .		0.45		V
Output impedance, DC	R_o	Differential, integrated on-chip	70	85	110	Ω
Output impedance, AC	RL_{TX}	Meets 100G-KR4, OIF-CEI 25/11/6G, XLAUI, XFI+, SFP+, QSFP, 10G-KR, XAUI, CX-4, return loss templates when properly configured				
Output voltage fall time	t_{fall}	80% to 20%, based on 25G-LR waveform, 8 1s, 8 0s		TBD		ps
Output voltage rise time	t_{rise}	20% to 80%, per 25G-LR std		TBD		ps
Output differential skew	t_{skewo}	50% rising/falling versus 50% falling/rising edge			2	ps
TX output jitter	Δt_{TX}	Random, wideband, RMS value. Typically much less than 10mUI for lower rates		8	10	mUI
	Δt_{TXdet}	Deterministic, peak-peak for integer over/under sampling modes		0.05		UI
	Δt_{TXtot}	Total, peak-peak		0.15	0.28	UI
Latency	T_{DTX}	From tx*_data<19:0> to TX driver output		24	46	UI
Current consumption, per lane	$I_{TX-25GLR}$	53G-LR PAM4 mode, full swing, some pre-emphasis on TVDD0P8 35 mA TVDD1P2 18 mA		35 18		mA mA

PARAMETER	SYMBOL	DESCRIPTION	MIN.	TYP.	MAX.	UNIT
AC-JTAG						
Fault Resistance Detect	R_{SC}	SHORT circuit	0		5	Ω
	R_{OC}	OPEN circuit	20			kΩ
Transmitter						
Transmit Voltage Levels	V_{TX}	Differential output	0.68	1.0	1.1	V
Data Rate	T_{DATA}	EXTEST_TRAIN	1		30	Mb/s
Output Resistance	R_{DRV}	DP or DM to VDD		50		Ω
Supply Current	I_{DD}	Operating mode		56		mA
Receiver						
Input Capacitance	C_{IN}	DP or DM to GND		0.5	0.6	pF
Common-mode Voltage	V_{CM}				V_{DD}-0.25	V
Comparator Hysteresis	V_{HYS}	Peak-to-peak	0	100	300	mV
Data Rate	T_{DATA}	EXTEST_TRAIN	1		30	Mb/s
Supply Current	I_{DD}	Operating mode		500		uA

31. AC-JTAG Settings – update amplitudes? Now binary for TX?

The following are typical values only, and are now listed as single-ended voltages instead of differential. The “se” units are more relevant to the JTAG mode and how the signals are typically measured.

test_txacj_st [3:0]	TX Amplitude (Vpp)	test_rxacj_st [4:2]	RX Hysteresis, ac_mode=1 (mVpp)
0111	0.34	011	0
0110	0.35	010	90
0101	0.36	001	80
0100	0.38	**000**	**75**
0011	0.40	111	65
0010	0.41	110	58
0001	0.43	101	35
0000	**0.44**	100	20
1111	0.45		
1110	0.47		
1101	0.48		
1100	0.50		
1011	0.52		
1010	0.53		
1001	0.54		
1000	0.55		

32. Low Power Modes for Short Channels and Lower Speeds – Preliminary and TBD

- The default settings for most circuits are for 25G-LR and the maximum performance and therefore power, 140mW typ. The power can be reduced for a few common modes as follows, but these settings are **preliminary** pending complete DVT tests.

25G-SR/VSR with 6-tap DFE and reduced TX amplitudes, TBDmW	
rx_ctrl<47>	pwrdn_ftap – power down floating DFE taps, leave fixed 6-taps active
rx_ctrl<2:0>	master diodes ibias, (max, mode, min) – reduce RX bias currents ~12%, set = 011
tx_drv_hv_disable	Use TVDD1P2 = 0.8V, and set = 1
20G-SR/VSR with 6-tap DFE and reduced TX amplitudes, TBDmW	
	similar to 25G-SR/VSR and with lower bias and frequency scaling
rx_ctrl<2:0>	master diodes ibias, (max, mode, min) – reduce RX bias currents ~25%, set = 110
pll_ctrl<18:16>	ickgen bias master (mode, max, min) – set = 110
tx_ctrl<18:16>	ibias tx master (mode, max, min) – set = 110

- The final 25G-VSR settings with no DFE are TBD, but see rx_ctrl<106:105> and tx_drv_hv_disable
- 10G settings are TBD
- Individual RX/TX lane power down and reset controls are in the register, 0xD1A1

33. EEE Support – very prelim

- TX Electrical Idle – similar to PCIE Idle, and enabled by txi_ctrl[47]. Reduces the TX power to TBD
- RX Signal Detect Power Down

34. External and Internal I/O

- In general, the transmitter outputs must be AC coupled to a RX with either external 100nF capacitors, or equivalent internal RC, eg what is in an Eagle or Falcon RX.
  - DC coupled links to other RX are only supported under limited conditions. Please contact the analog serdes team for more details. One known restriction is that a Blackhawk TX cannot be DC coupled to a 40 nm Warpcore10G RX and this is because the TX and RX common-mode voltages do not match.
- The receiver inputs have on-die AC caps with a low corner freq, ~70KHz, and in most cases, an external AC cap is not needed. The main limitation is that the absolute max RX input voltage must not exceed 1.1 V, and so limits the max input Vcm to ~0.7V. The peak amplitude limit should not be exceeded over all PVT and any transient effects such as reflections and power supply ramps.
  - The general design plan for the RX AC caps is to support DC links with TX link partners that are designed in recent ~1 V process such as 28 and 16 nm, and not to support DC links to older designs that use higher supply voltages such as 1.8-3.3 V.
- For both directions, and where possible, only one AC cap should be used in a link to minimize baseline wander. Many front panel modules for standards such as SFP+ and QSFP contain AC coupling caps, and so do some newer backplane connectors.
- The PLL refclk inputs now have on-die AC caps, and in some cases, an external cap is not needed. Similar to the RX, the max Vin is 1.1 V. For higher input voltages, eg LVPECL, an external AC cap, ~10 nF, must be used. Also, attenuation resistors might be needed to reduce the amplitude.
- The RX and TX IOs, and the PLL refclk IOs are terminated with internal resistors.
  - RX, 90 Ohm differential with internal Vcm, ~0.5 V
  - TX, 40 Ohm to internal 0.9 V from LDO and GND, Vcm ~0.45 V
  - PLL, 100 Ohm differential with internal Vcm, ~0.4 V

35. Power/Ground and ESD Connections

- The following power supply bumps within each group, must be shorted in the package substrate for ESD compliance:
  - Group 1: Receiver power supplies: pad_rvdd0p8, 10 bumps
  - Group 2: Transmitter power supplies: pad_tvdd0p8, 4 bumps
  - Group 3: PLL power supplies: pad_pvdd0p8, 2 bumps
  - Group 4: Transmitter driver power supplies: pad_tvdd1p2, 4 bumps
- The three analog grounds, pad_rgnd, pad_pgnd, and pad_tgnd, must be shorted in the package substrate, but the combined analog ground should be separate from any digital grounds in the package.
- However, a "weak short" in the package substrate between the analog and digital gnds should be used to improve the CDM ESD performance. This is typically done on the bottom layer.
- Five different types of IO pad cells are included in the core and connected as follows.

I/O Pad Cell and (# of instances)	Falcon Core Pad name
BCM16FFXCORE_X08AV_ESD_INT (2, 8, 8)	pad_pvdd0p8, pad_rvdd0p8, pad_tvdd0p8
BCM16FFXCORE_X18AV_ESD_INT (4)	pad_tvdd1p2
BCM16FFXCORE_X18AV_ESD_INT (2)	pad_pvdd1p8
BCM16FFXCORE_XXGV_BBDIODE (10)	pad_pgnd, pad_rgnd, pad_tgnd
BCM16FFXCORE_X18AV_DIODE_1U1D	pad_refclkp, pad_refclkn, pad_ptestp, pad_ptestn
BCM16FFXCORE_X33AV_DIODE_1U1D_RF plus 2nd UP/DN diodes and metal resistors	pad_rdp*i*, pad_rdn*i*, *i=7:0*
BCM16FFXCORE_X33AV_DIODE_1U1D_RF	pad_tdp*i*, pad_tdn*i*, *i=7:0*

- To comply with the latest ESD requirements, ten BBD2CORE pins using the AP layer have been added to the top edge of the core above each RX and the PLL. These pins should be connected to the serdes core digital gnd with a low impedance path, and ideally, with AP routing, directly to a VSS bump within 200um.
- Every internal analog input pin connected to the digital has 2nd ESD cells.
- It is not required, but it is preferred for the power supply for the PMD and/or PM digital to be powered up before the supply for the Falcon analog

36. PLL Test Port

- The PLL test port is used to observe several important PLL clock and bias signals.

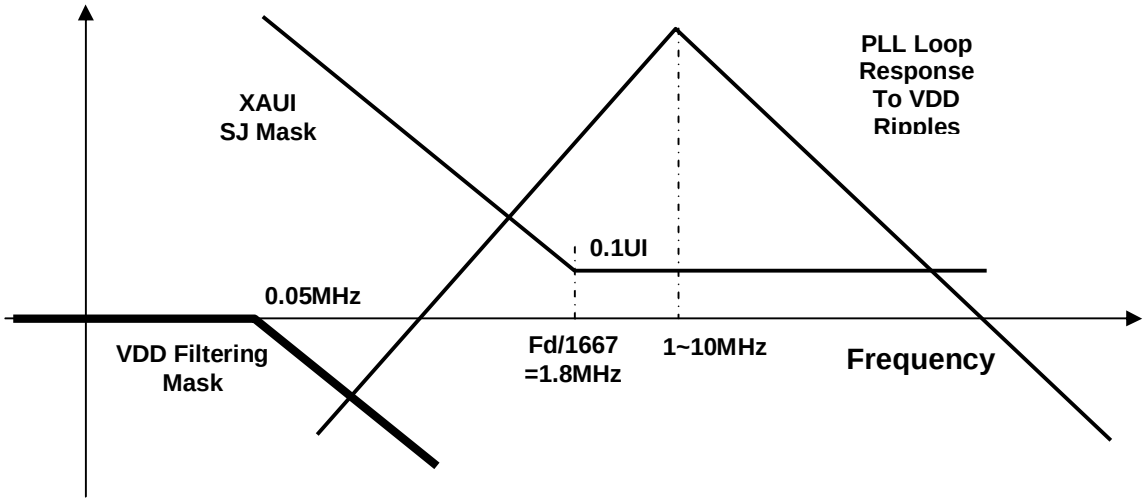
PLL_CTRL bit reg 0xD113, 15:12				PAD_PTEST	
63	**62**	**61**	**60**	**P**	**N**
				Clock Outputs	
1	0	0	0	Recovered clock from RX Lane 3 if rx3_ctrl<8>=1 RX line rate freq / 20 for OS1x mode Also, see rx_ctrl<94:92> for other test clock options	
0	1	0	0	PLL divider feedback clock freq varies with Ndiv setting, see pll_mode table in Sec 21 or is the same as final refclk freq, eg after refclk div1/2/4, if the frac-N integer mode is used	
1	1	0	0	Internal refclk, either from LCPLL, or another serdes core, or external bumps, typ 156.25 MHz, also see Sec 24	
				Bias Outputs	
0	0	1	0	VCO control voltage, VCP, ~300 mV	--
1	0	1	0	--	VCO control voltage, VCN, ~500mV
				VCO control voltage, calculated ~-175mV (VCP-VCN)	
0 Vbs 1 Vbg	0	0	1	Vbias, ~480 mV, or 60% of PVDD0P8, wrt AGND PLL reg 0xD114, bit 11 = 1	VbiasBG, ~-350 mV +/-5% wrt PVDD0P8 PLL reg 0xD114, bit 11 = 0 Default is 3P1C_calR from pll_ctrl<95:86>
0	0	1	1	Ibgp, 100 uA to gnd PLL reg 0xD114, bit 11 = 0	Ibgn, 100 uA to 0.8V 3P1C_calR
0	0	1	1	Ivddr, ~100 uA to gnd Varies with PVDD and YH resistor process, not calib PLL reg 0xD114, bit 11 = 1	--

- To use this feature, the pad_ptestp/n signals should be routed over 50 Ohm traces directly to a test point which supports high speed signals, e.g. SMA, etc. No additional components, e.g. AC coupling caps or local pull down res, are needed on a PCB.
- To observe the clocks, use a scope with AC coupled, 50 Ohm to GND inputs. The default amplitude is approx. 250 mVppse, or 325 mVppse if pll_ctrl<80>=1.
- To measure the bias and VCO voltages, use a high impedance DMM referenced as needed.
- To measure the bias currents and to avoid unexpected leakage currents, use a current meter referenced to 0.3 V for Ibgp and Ivddr, and to 0.5 V for Ibgn.
- Additional bias tests can be enabled with pll_ctrl<85:81> and pll_ctrl<74>.

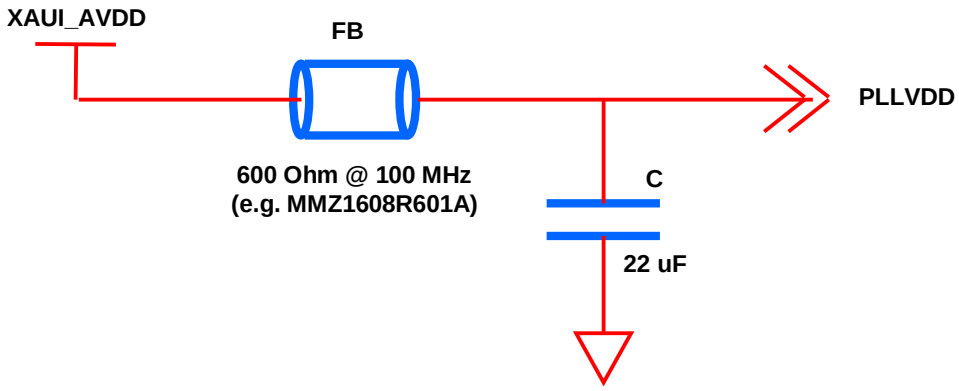
37. Power Supply Filtering – add ripple specs for PLL vs RX/TX

- A LC filter, i.e. ferrite bead + caps, with a bandwidth less than 50 kHz over PVT is required for the 3 supplies to improve the PSRR of the core.
- The use of such a filter is especially critical for the PLL supply, pad_pvdd0p8, and a proven LC filter is 1uH and 22uF, ~35kHz, which is shown below.
- The RX and TX supplies can be combined on the PCB and share a common filter.
- For chips which use multiple instances of the WC, each PLL supply should have its own filter, and approx 2-3 RX/TX supply pairs can be grouped together and share one filter.
- Where possible, local decoupling caps should be placed as close to the chip as possible, eg on the bottom of the board under the vias for the power supplies.

A. PLL VDD filtering mask. The SJ mask is similar for many stds.



B. PLL VDD filter schematic



- **Integration Review Checklist – prelim list**
- Core placement and orientation in floorplan
- ResCal IPs must be placed within 8-10 mm, and properly connected and enabled before using any operational modes of the Blackhawk IP.
- The long term operating temperature is 110C, and temp information is used for calibrating several operating modes of the design. If PVTMON info is used for this, the max temp delta should be <5C after accounting for all operating modes, thermal gradients, and any variations in the PVTMON accuracy. Thus, the maximum allowed temp for even a nearby PVTMON could be 5-10C lower than 110C in order to ensure that the max temp for the Blackhawk circuits is not exceeded.
- Use CE verilog model and check all needed modes of operation
- Coding schemes for all decoders
- DFT modes, eg AC-JTAG and LBIST, and connections
- 1.2V, driver protect control bit usage
- BBD2CORE connections
- Refclk routing and controls, master/slave usage
- NATN guard ring for stacked cores
- Spacing from IO and PVDD to noisy, digital bumps – noise and RL
- PVTMON, LCPLL, and RESCAL placements and connections to Falcon
- Sense points and high speed cal traces in PCB designs
- Datasheet specifications should match those in the applicable IEEE and other standards. Much of the information in the AMS should not be placed in a datasheet, and in general, compliance is only claimed to limits in the public standards.

38. DFT Modes and Settings

- If the PLL is used for LBIST or other DFT modes, then all the pll_ctrl and dedicated control bits must be configured as needed for full functionality, eg refclk control, VCO tuning and test port, of the PLL. Similar control is needed for the entire clock path and bias circuits of any used RX or TX clocks.
- During the DFT modes, eg scan, any unused analog blocks should be powered down or configured in a known state in order to avoid random states which might lead to high currents and possible damage. This is especially important during burn-in.
- For other burn-in requirements, see Sec 42

39. Package Substrate and Local PCB Design Guidelines – prelim list

- To reduce possible ESD damage, avoid placing package balls for the RX inputs next to the pkg edge
- Target Impedances for pkg substrate, and use 95 Ohm for PCB
  - RX – 95 Ohm differential, 25 Ohm common-mode
  - TX – 90 Ohm differential, 25 Ohm common-mode
- Return Loss Target
  - Use SFI Channel Spec, -14.6dB up to 5 GHz, etc
  - Plus add at least 3dB margin for manufacturing variations, etc
  - Most likely, the PCB PTH vias for the RX/TX IOs should be back drilled or blind
- Crosstalk, and including the local PCB escape area
  - From the systems team, the Power Sum of all xtalks measured at a given RX die bump < -52dB @ 14GHz

    - Higher levels of xtalk are allowed for lower rates, eg XAUI, QSGMII, RXAUI
    - Xtalk definitions
        - RX NEXT - TX bump to RX bump, most critical for best BER
          RX FEXT - RX ball to RX bump
          TX FEXT - TX bump to TX ball, power sum <-40dB @ 14GHz
          TX NEXT - RX ball to TX ball
- Differential P/N trace length matching, within <50um
- Extraction setup for RX/TX IOs
    - Max freq ~60GHz, and add a DC term
    - Include Surface Roughness, ~0.7 um-rms, or as needed for different materials
    - Plot IL, RL, SCD, and TDR
    - Provide s8p files for pairs of two RX or two TX lanes with the following order
    -
- Power and Ground routing
    - Max IR drop from ball to bump for power and gnd combined, <15 mV over PVT
    - Avoid overlap and close spacing between the analog and the digital pwr/gnd planes. This is very important for the PVDD0P8 routing and vias
    - Extract the power domains, s9p example from Exp7 and FE3200
- Decoupling caps
    - To improve the PSRR and maximize the TX jitter performance, it is recommended to add ~1 uF caps in the pkg substrate to the TVDD0P8 supply. These caps should be as close to the die as possible and have low ESR.

40. ATE Board Design and Tests – prelim list

- Design targets for load board
    - Target Impedances
        - RX and TX – 95 Ohm differential, 25 Ohm common-mode
    - Return Loss
        - Use SFI Channel Spec, -14.6dB up to 5 GHz, etc
        - Skew, Diff to CM?
        - Plus margin for manufacturing variations, etc
    - Crosstalk
        - From the systems team, the Power Sum of all xtalks measured at a given RX pkg ball < -52dB @ 13GHz
- For each product, there should be a test pattern to check each unique data rate and OS mode listed in the datasheet. Each OS1x data rate typically uses a different PLL divider setting and circuit. The OS2x and OS4x modes generally use different clock dividers and are not simply digital OS modes.
    - If different refclk freq are listed in the datasheet, then that can create other unique PLL modes of operation that should be tested, and this is especially important if a fractional-N mode is used.
    - To minimize test time for products that support many data rates, the required test patterns can be a mix of functional PRBS and PLL lock tests.
    - Based on common stds and usage cases, it's likely that the following rates will always be part of a test suite, 27.34375G, 25.78125G and for OS2x, 10.3125G.
    - The worst case VT stress condition is expected to be low VDD and high temperature.
- In addition to pass/fail checks for PRBS and PLL lock, the following information should be measured and recorded.

- KVH range and VCO tuning code in pll_sts<15:14> and pll_sts<13:6>. The value in pll_sts<13:6> should be converted to decimal for easier comparisons to the limits.
- VCO control voltages and bias voltages and currents from the PLL test port
- See Sec 36 and 41 for more details of the PLL test port capability and programming, which is very similar to what is in the 28nm Falcon/Eagle cores and 40nm Warpcore.

41. ATE Tests with PLL Test Port for Pre-Production Characterization – prelim list

- In addition to the PRBS and other tests which will be used for ATE screening, the following are some details about the required tests related to the PLL test port
- The listed steps are essentially the same information that is in the table in Sec 36, but they are listed in a more sequential way for easier pattern development.
- These tests should be done after bringing the core out of reset or running the 25.78125G PRBS pattern and should be done for all of the Falcon cores that have a PLL test port routed to pkg balls. The results for each core should be uniquely named.
- The approx. test limits are included.
- Configure the tester in a high impedance mode to measure DC voltages from pad_ptestp/n
  - VCO Control Voltage, VCP, ~-325mV +/-100mV
    - Write register 0xD113<15:12> = 0010, and measure PAD_PTESTP wrt gnd.
  - VCO Control Voltage, VCN, ~-475mV +/-100mV
    - Write register 0xD113<15:12> = 1010, and measure PAD_PTESTN wrt gnd.
  - Calculate VCdiff = (VCP-VCN) ~-150mV, and VCcm = (VCP+VCN)/2 ~+400mV ~= PVDD0P8/2.
  - VddR bias voltage, Vvddr, ~480mV +/-50mV
    - Write register 0xD114<11> = 1
    - Write register 0xD113<15:12> = 0001, and measure PAD_PTESTP wrt gnd.
    - Calculate Vvddr/PVDD0P8, ~= 60% +/-5%
  - VddR bias voltage, bypass op-amp, Vvddrbyp, ~480mV +/-50mV
    - Write register 0xD114<11> = 1
    - Write register 0xD115<3> = 1
    - Write register 0xD113<15:12> = 0001, and measure PAD_PTESTP wrt gnd.
    - Calculate Vvddroffset = Vvddr-Vvddrbyp, expected mean ~0mV, stdev = 5mV, min/max, 4-sigma limits = +/- 20 mV
    - Disable bypass mode, 0xD115<3> = 0
  - Vbg3pcalR bias voltage, bypass op-amp, Vbg3pcalrbyp, ~350mV +/-100mV, temp dependent, ~15%/100C
    - Write register 0xD114<11> = 0
    - Write register 0xD115<3> = 1
    - Write register 0xD113<15:12> = 0001, and measure absolute(PAD_PTESTN wrt PVDD0P8).
    - Disable bypass mode, 0xD115<3> = 0

- Configure the tester to measure DC currents from pad_ptestp/n. Use positive polarities.
  - VddR bias current, Ivddr, ~100uA +15/-20uA
    - Write register 0xD114<11> = 1
    - Write register 0xD113<15:12> = 0011, and measure PAD_PTESTP wrt gnd
  - BGR bias current, Ibgrp, ~100uA +15/-20uA
    - Write register 0xD114<11> = 0
    - Write register 0xD113<15:12> = 0011, and measure PAD_PTESTP wrt gnd
  - BG 3P1CcalR bias current, Ibg3pcalrn, ~100uA +20/-30uA, temp dependent
    - Write register 0xD114<11> = 0
    - Write register 0xD113<15:12> = 0011, and measure PAD_PTESTN wrt PVDD0P8 or other 0.8V supply

42. Burn In Requirements – prelim list

- Use valid refclk freq, eg 156.25MHz, that is connected in the same way as done in normal operation, which is typically through a refclk LCPLL or a master serdes core
- The rescal value on ana_rescal<3:0> should be valid and stable at all times
- All blocks should be powered up and operated in a normal mode for a significant amount of the burn-in time, and with some level of active traffic in the data path. This could be functional PRBS, or a well-defined, DC balanced, idle pattern, eg 8 1s, 8 0s.
- When switching between several different modes, eg functional, LBIST, MBIST, etc, it is better to run each mode longer with fewer resets and power down cycles between them which is closer to a normal operating mode.
- It is not enough to simply power up the analog block and leave it in a random state. This does not provide the correct coverage and could possibly lead to false failures.
- However, it is not necessary to run real-time BER checks during the BI, and such checks will be done on ATE at each read point, eg 24, 192 hours, etc.
- The TX outputs should be connected to the RX inputs in a loopback mode which is similar to the normal operating mode. External AC caps are not needed because the Falcon RX inputs have on-die caps. A backup option is to place 0 Ohm resistors in the loopback path on the PCB which can be replaced with caps, if needed.
- To avoid false HTOL failures, good ESD handling practices should be followed for all aspects of the stress and pre/post test procedures.
- Also, please see Sec 39

43. Appendix 1 – Misc prelim info

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Prelim cal code for TX driver

Decimal PON code	%	Cal Code 0p8V
0	-21	0
1	-18	0
2	-15	0
3	-12	0
4	-9	0
5	-6	1
6	-3	1
7	0	1
8	0	1
9	3	2
10	6	2
11	9	2
12	12	3
13	15	3
14	18	3
15	21	3

Decimal PON code	%	Cal Code 0p92V
0	-21	0

1	-18	0
2	-15	0
3	-12	0
4	-9	0
5	-6	0
6	-3	0
7	0	0
8	0	0
9	3	0
10	6	0
11	9	1
12	12	1
13	15	1
14	18	1
15	21	1