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Course EPSI: Essential Principles of Signal Integrity

With Eric Bogatin,
Signal Integrity Evangelist, Teledyne LeCroy Front Range Signal Integrity Lab
Dean, Teledyne LeCroy Signal Integrity Academy
Adjunct Professor, University of Colorado, Boulder, ECEE

- EPSI-06-01: recorded live, Dec 1, 2013
  - Ground bounce when signals change layers
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Lesson EPSI-06-10 Signals Transitioning Planes

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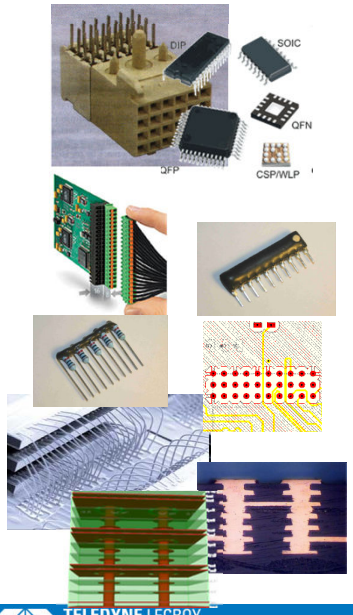
- EPSI-06-10: recorded live, Dec 1, 2013
  - Ingredients for ground bounce
  - Ground bounce in packages and connectors
  - When a signal changes return planes- why DC voltage is not an issue
  - The real problem when return planes change

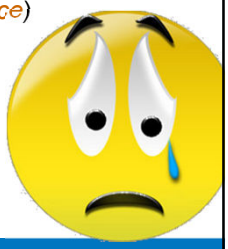
- **Day 1**
  - EPSI 1 Transmission Lines
  - EPSI 2 Differential Pairs and Lossy Lines
  - Lunch
  - EPSI 3 Reflections and Terminations
  - EPSI 4 Routing Topologies and Discontinuities
- **Day 2**
  - EPSI 5 Eliminating Ground Bounce
  - **EPSI 6 Navigating Return Path Discontinuities**
  - Lunch
  - EPSI 7 NEXT and FEXT Features
  - EPSI 8 PDN and EMI Design

In Which Interconnect Structures Will Ground Bounce Arise?



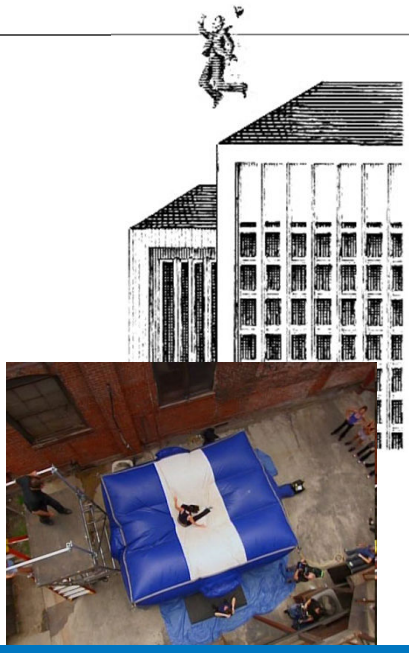
- Two ingredients for ground bounce:
  - Higher inductance (*impedance*) in return path (not a wide plane)
  - Overlapping return currents for different signal lines
- Narrow package traces
- Narrow connector pins
- Resistor SIPS
- Plane transitions (*return path impedance*)
  - Vcc to Vss connections (*return path impedance*)
  - Gaps in planes (*return path impedance*)
  - Vias- signals changing layers (*return path impedance*)

Ground bounce is not about "ground" it's about return path!



The Real Problem with Different Voltage Return Planes: when the return plane changes

- Jumping off a tall building is not a problem.
- The problem is in the landing
- Using an arbitrary voltage for the reference plane is not a problem.
- The problem is when the return plane changes
- Minimize the problem by reducing the impedance when the return plane changes



Lesson EPSI-06-20 How return current flows between planes

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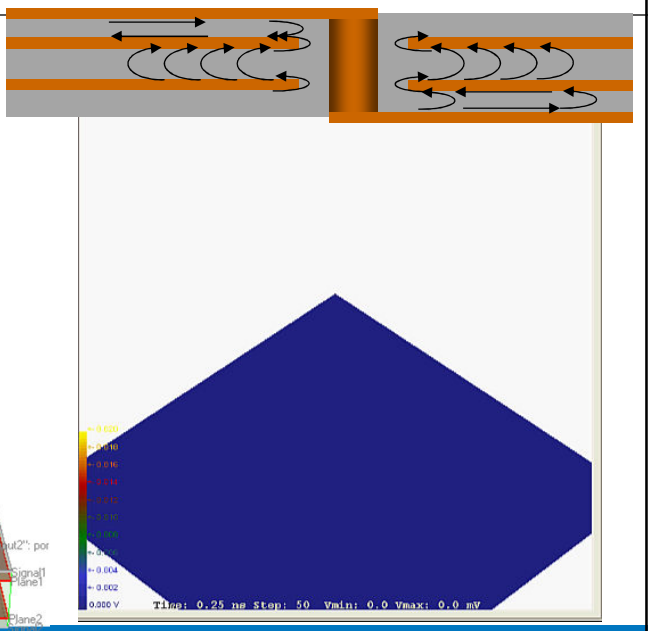
- EPSI-06-20: recorded live, Dec 1, 2013
  - How return current flows when the signal goes through a via
  - The real way to think about two planes as a cavity
  - Why two adjacent planes are a transmission line and why this is so important
  - The behavior of the trapped return current in the cavity

Ground Bounce Between Two Return Planes

- How does the return current get from one plane to the other?
  - Current travels like a radial wave through the impedance of the plane-plane cavity
  - This is the most important way high frequency noise is injected into the board planes
- Set up:
  - 50 ohm microstrip top and bottom
  - 30 mil thick dielectric between the planes
  - 10 inch x 10 inch board
  - 1 v signal, 20 mA at 0.3 nsec rise time
  - Simulated voltage between the planes with HyperLynx/PI (~20 mV full scale (~2%)



Lesson EPSI-06-30 The origin of via to via cross talk

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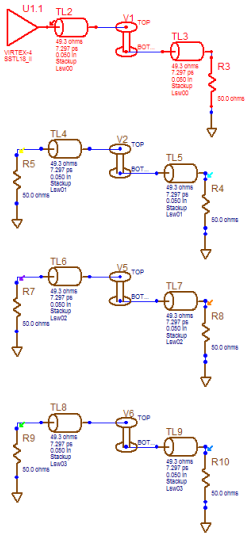
- EPSI-06-30: recorded live, Dec 1, 2013
  - How to think about via to via cross talk
  - Via to via cross talk as voltage noise in the cavity
  - Why the cavity impedance determines the via to via cross talk
  - Most important features that influence the impedance of the cavity

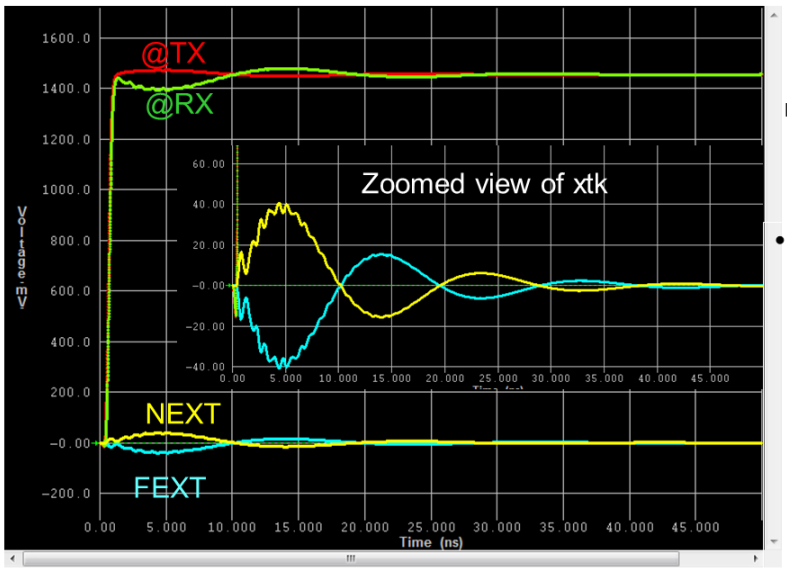
Via to Via XTK Example (ground bounce because it is a RPD)

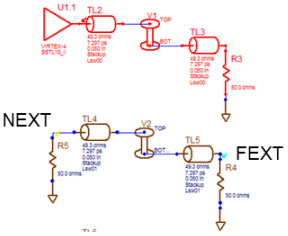


- Set up:
  - Board is 5 in x 5 in
  - H = 30 mils
  - 3 victim vias: close, farther, very far away
  - 1.5v signal, 0.3 nsec rise time, BW ~ 1 GHz
  - Simulating NEXT, FEXT between adjacent vias
  - VRM between planes: 1 mOhm, 10 nH

VRM

Nearest Via Cross talk





- Observations
  - ✓ NEXT = FEXT ~ 40 mV/1.4 v = 3%
  - ✓ RX signal sees the cavity noise
  - ✓ What accounts for the initial rapid ripple ~1 GHz?
  - ✓ What accounts for the slow period of ~ 50 MHz?

Lesson EPSI-06-40 Cavity impedance profile and cavity noise

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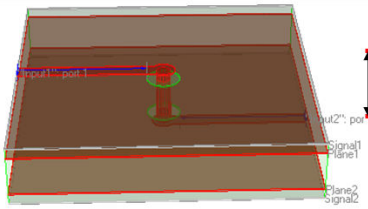
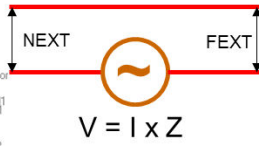
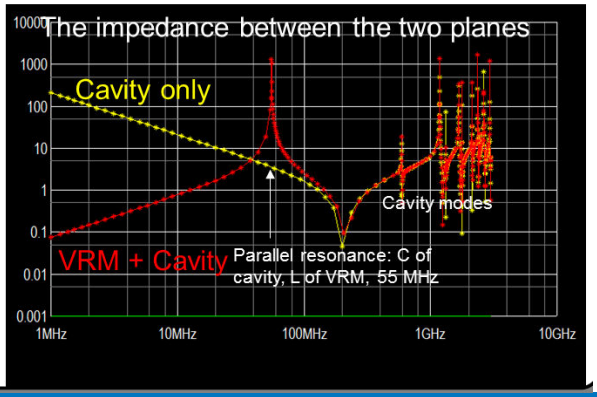
- EPSI-06-40: recorded live, Dec 1, 2013
  - The features of the cavity impedance profile with a bare board
  - New impedance features with a VRM attached
  - Spreading inductance in a cavity
  - Impedance peaks and via to via cross talk peak noise

Where Does the Noise Come From?

- Current through an impedance generates a voltage
- Any other signal paths passing through the cavity see the voltage between the planes as part of their signal-return path voltage.
- Noise is the signal current passing through the impedance between the planes
- Peak noise voltage will be dominated by peak impedances and frequency components of the signal



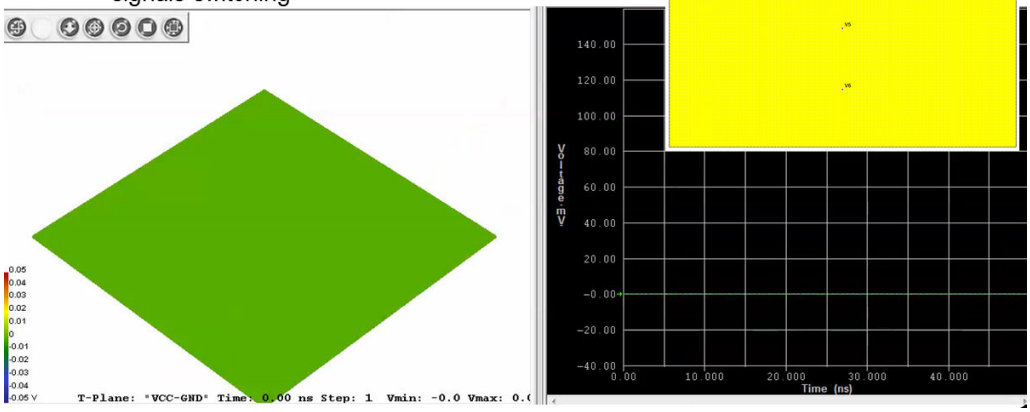




Features of Via to Via XTK

- Long range:
  - ✓ Cavity modal noise selective with location
  - ✓ Cavity global noise everywhere the same
  - ✓ Global noise will scale with number of signals switching

4 vias, very close, very far



Lesson EPSI-06-50 Using shorting vias

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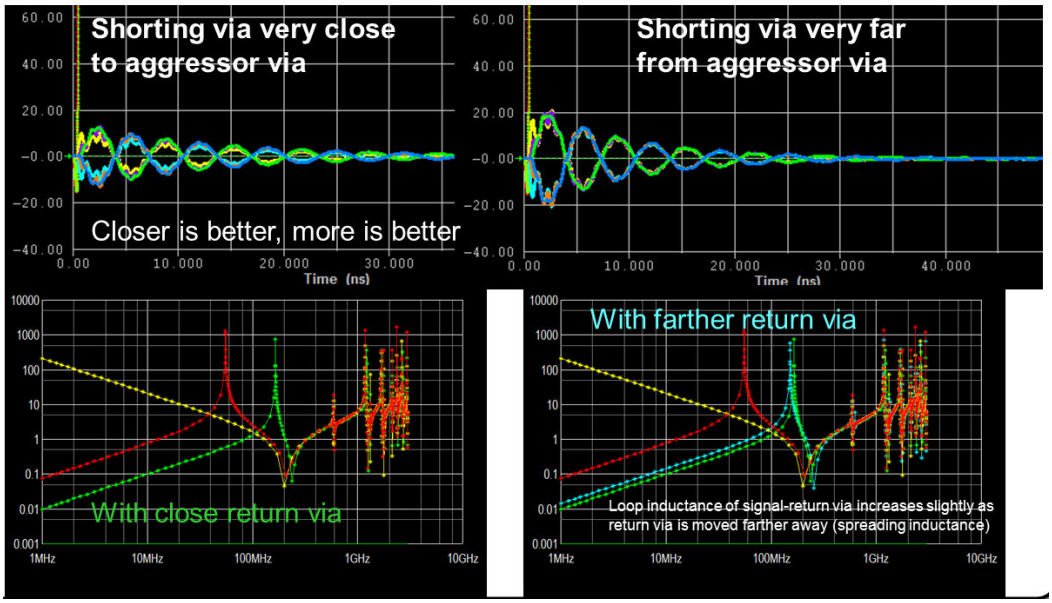
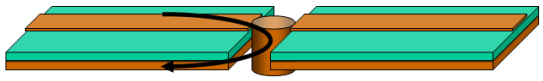
- EPSI-06-50: recorded live, Dec 1, 2013
  - Impact on cavity impedance from one shorting via
  - Via to via cross talk with a shorting via
  - Role of spreading inductance and cavity thickness
  - Best location of shorting vias and signal vias

How to Reduce Cavity Noise #1: add return vias



Estimating the Total Inductance of a Via



h = 64 mils
Diameter = 50 mils, r = 25 mils

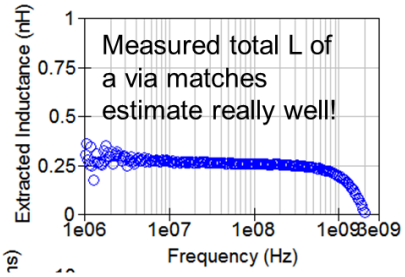
$$L_{total}[pH] \sim 5 \times h[mils]\left\{\ln\left(\frac{2h}{r}\right) - 0.75\right\}$$

Partial self inductance
Neglecting mutual to the loop

$$L_{total}[pH] \sim 5 \times 64\left\{\ln\left(\frac{2 \times 64}{25}\right) - 0.75\right\} = 280pH$$

If h = 30 mils, r = 5 mil

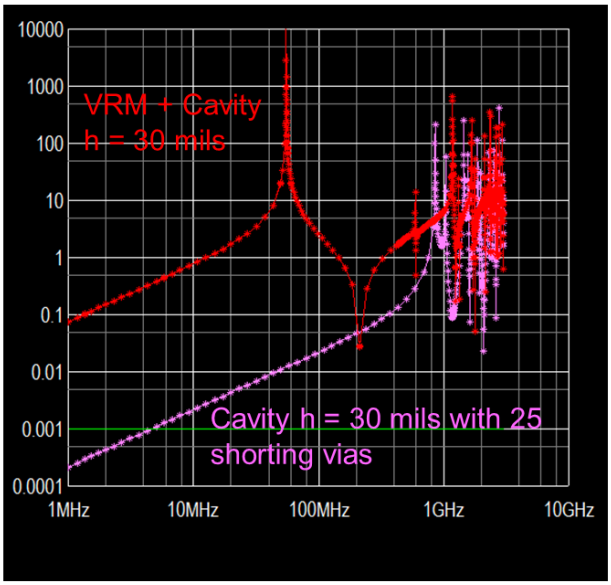
$$L_{total}[pH] \sim 5 \times 30\left\{\ln\left(\frac{2 \times 30}{5}\right) - 0.75\right\} = 260pH$$



Inductance of a via ~ 260 pH/30 mils ~ 10 pH/mil = 10 nH/inch
Doesn't that sound familiar?

More Return Vias Push the PRF to Higher Frequency

- Lowest noise is when all the return planes are the same voltage
- With many shorting vias
- Cavity modal peaks pushed to higher frequency
- Difficult to estimate impact of number of vias on magnitude of the noise due to plane resonances + freq components of signal:
- In this example: 1 via, 1 signal, ~ 1% noise
- Rough rule of thumb: ~5 signals per return via for 5% cross talk

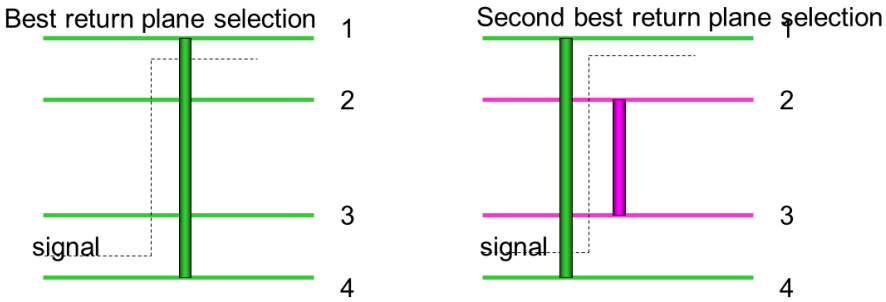


The Use of Return Vias Drives Reference Plane Selection

A Good Habit:
drop a return via
at every signal via

Reduces the spreading of the return currents from each via

- Voltage on return plane has no impact on the impedance of the signal line
- Return plane selection is all about the option to add a return via



For robust strategy, always use Vss as the return planes and shorting vias between all layers

Lesson EPSI-06-60 Using DC blocking capacitors

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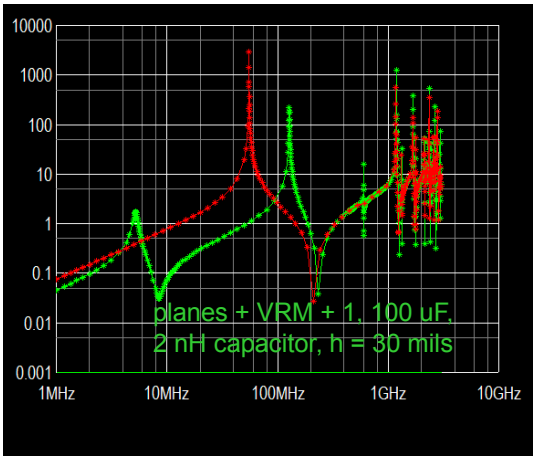
- EPSI-06-60: recorded live, Dec 1, 2013
  - When the two planes in the cavity are not the same voltage
  - How much capacitance for a bypass capacitor?
  - Optimizing the bypass capacitor design
  - Multiple capacitors and loop inductance

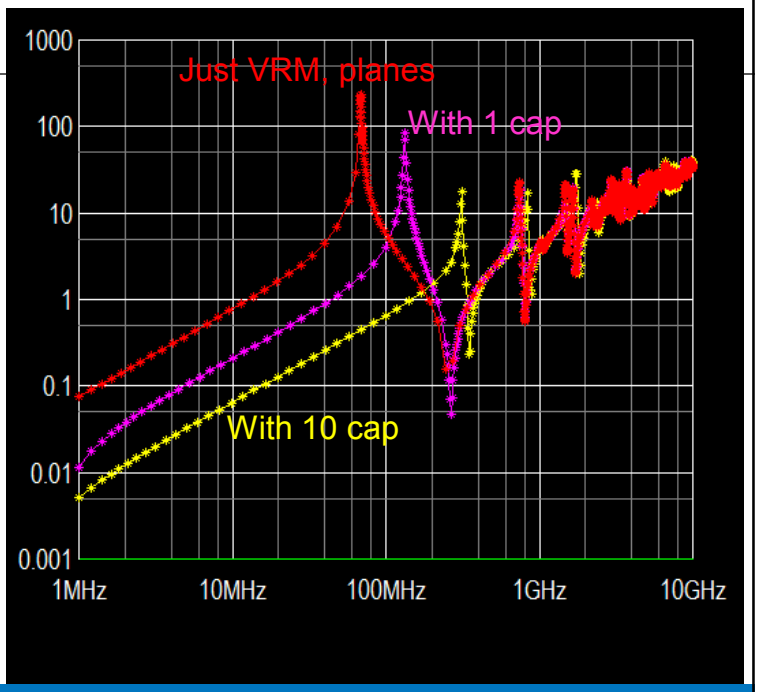
But what if they are Vcc and Vss Planes?

- The noise comes from the overlap of spectral components of the current overlapping with impedance peaks in the planes.
- Secret to reduce plane noise: via to via cross talk, I/O switching noise
  - Reduce the peak impedances when looking into the cavity
- Add capacitors:
  - Lowest mounting L
  - Highest ESR
  - Use controlled ESR capacitors, typical value: 10 uF and 0.2 Ohms
- Increase cavity C as much as possible
  - Larger width
  - Thinner h



Nominal Conditions

- VRM
  - R = 1 mOhms
  - L = 10 nH
- Planes
  - 4 inches x 4 inches
  - H = 30 mils
- Capacitors:
  - each 10 uF,
  - ESL = 3 nH,
  - ESR (typical) ~ 5 mOhms
- 3 features of impedance profile
  - Inductance of the capacitors
  - Parallel resonant peaks
  - Modal peaks of the plane resonances



Lesson EPSI-06-70 How many bypass capacitors

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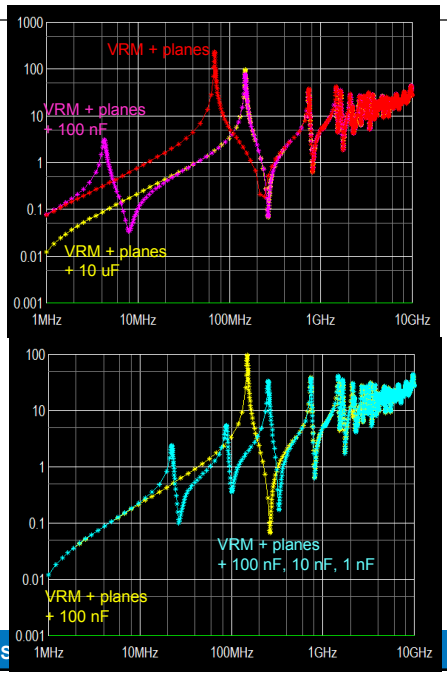
- EPSI-06-70: recorded live, Dec 1, 2013
  - Estimating the inductance in a capacitor
  - Estimating the number of capacitors per signals switching
  - Optimized board stack up for lowest via to via cross talk
  - Just how low can the via to via cross talk be engineered?

Does it Matter What Capacitor Values You Use?

- If only 1 value C: no (It's about the ESL)
  - VRM + plane cavity
  - + 100 nF cap, ESR = 25 mOhms
  - Or + 10 uF, ESR = 5 mOhms
  - Larger value C is better
- Multiple C values: difficult to optimize without all the details
  - Arbitrary values may reduce peaks, may increase peaks …it depends
  - 1st order estimate: Select C to match SRF to peak

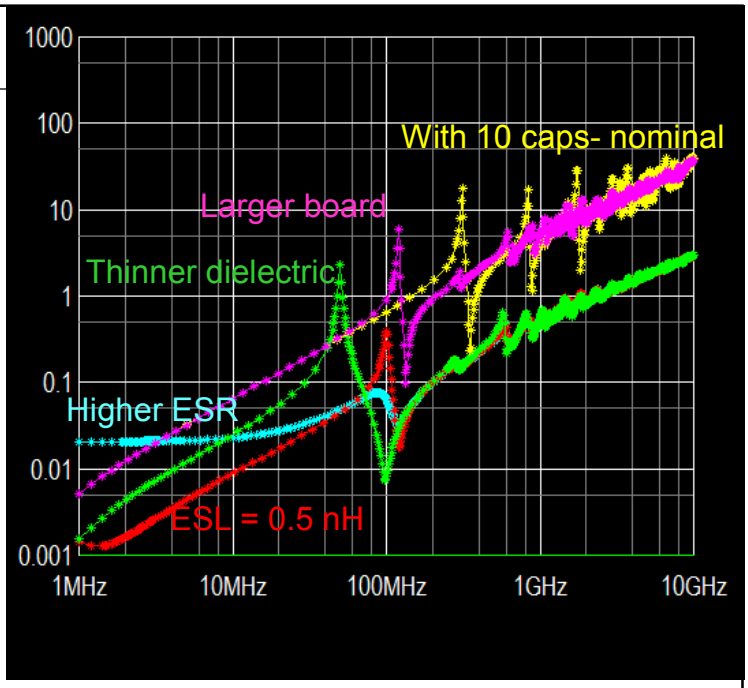
$$SRF = \frac{159MHz}{\sqrt{ESL[nH] \times C[nF]}}$$

  - Peak @ ~ 160 MHz, ESL = 1 nH, C ~ 1 nF
  - There is a better way of reducing peaks



Best Conditions

- Larger planes, thinner h
  - 10 inches x 10 inches
  - h = 3 mils (damps plane modal resonances)
- More capacitors with low ESL, higher ESR
  - 10 caps, each 10 uF
  - ESL = 0.5 nH
  - controlled ESR = 200 mOhms
- Most important way of damping peak resonances is with higher ESR capacitors



How Many Capacitors Needed?

- … it depends
  - Impedance peaks, frequency components of the current
  - Difficult to select capacitor values to reduce peaks: if peaks > 150 MHz, requires sub 1 nF capacitors.
- Best case:..good damping- no peaks
  - Impedance of the cavity limited by the ESL of all the caps

$$V_{noise} \sim ESL_{allCaps}\frac{dI_{total}}{dt} = \left(\frac{ESL_{cap}[nH]}{n_{caps}}\right)\left(n_{signals}\frac{V_{signal}}{50 \times RT}\right) \qquad \frac{n_{signals}}{n_{caps}} = \%noise\frac{50 \times RT[n\,sec]}{ESL_{cap}[nH]}$$

For noise =10%

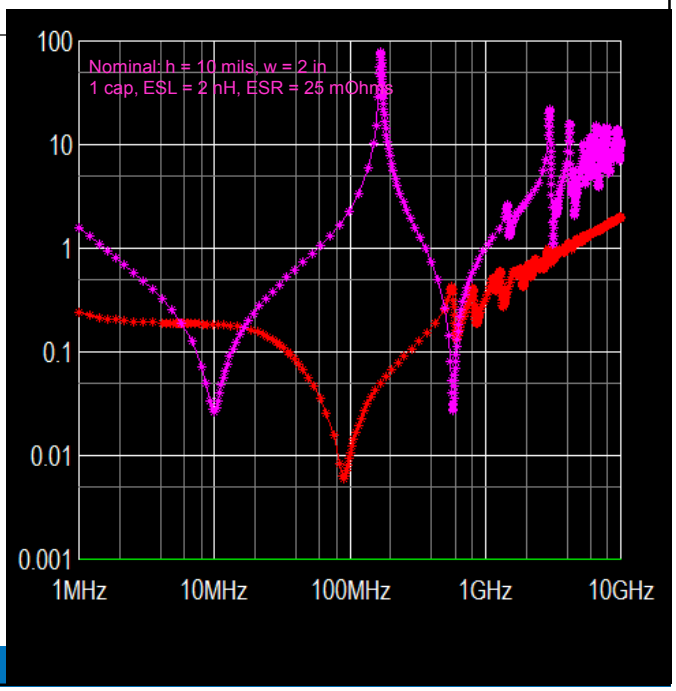
$$\frac{n_{signals}}{n_{caps}} = 5\frac{RT[n\,sec]}{ESL_{cap}[nH]}$$

Example: RT = 0.5 nsec
ESL = 2 nH
n_{signal}/n_{caps} = 5 x 0.5/2 = 1

Example: RT = 1 nsec
ESL = 1 nH
n_{signal}/n_{caps} = 5 x 1/1 = 5

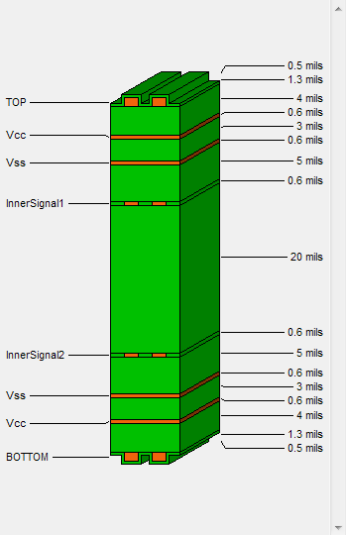
Doing Everything Right

- Cavity:
  - 2 inch x 2 inch → 10 x 10
  - h = 10 mils → 2 mils
- Capacitor:
  - C = 100 nF → 1 uF
  - L = 2 nH → 0.5 nH
  - R = 25 mOhms → 200 mOhms
- Features:
  - Thinnest dielectric
  - Largest size cavity
  - Smallest mounting inductance
  - Highest ESR (controlled ESR caps)



8 layer Board Stackup for Minimum Switching Noise

- Features
  - Adjacent power and ground layers
  - Power and ground layers near component surfaces (low C ESL)
  - Thin dielectric between power and ground
  - Similar planes for pairs of signal layer
  - Dielectric fill between adjacent signal layers
- Capacitor selection
  - Engineer as low ESL mounting inductance as possible
  - Select controlled ESR caps
  - Value of C is not important



Lesson EPSI-06-80 Cross talk with Differential Vias

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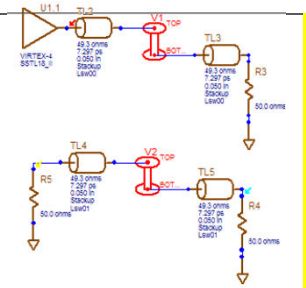
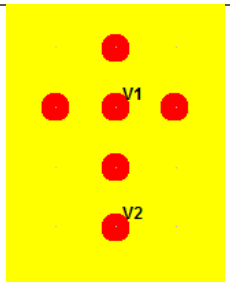
- EPSI-06-80: recorded live, Dec 1, 2013
  - Why cavity noise is dramatically reduced with differential vias
  - How common signal components dramatically increase cavity noise
  - Why you should always add a return via even with differential vias
  - Summary of minimizing the switching noise when changing signal layers

Just How Low Noise Can You Get?



Cavity is 30 mils thick

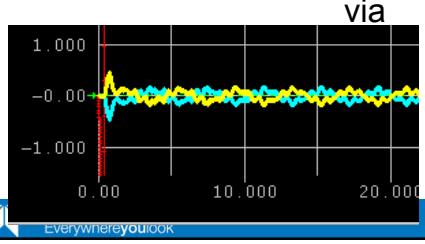


Using 4 shorting vias around signal via

With just h = 30 mils cavity, NEXT ~ 40 mV (-32 dB)

With just h = 4 mil cavity, NEXT ~ 10 mV (-43 dB)

With h = 30 mils and 4 shorting vias, NEXT ~ 0.1 mV (-80 dB)

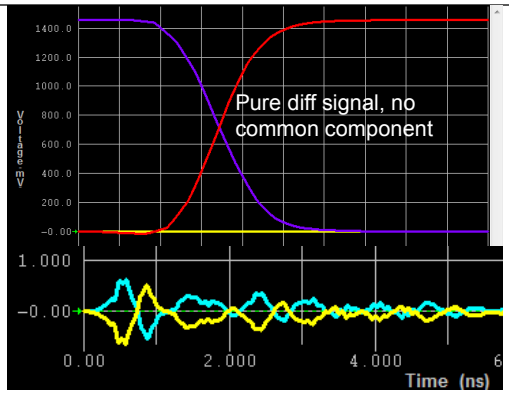


For ultra low noise, < -80 dB, need 4 return vias, thin dielectric

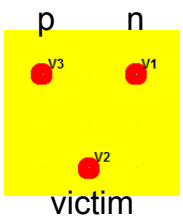
Only an issue in mixed signal applications

Differential Signaling Reduces "Common" Noise Injected into Cavity

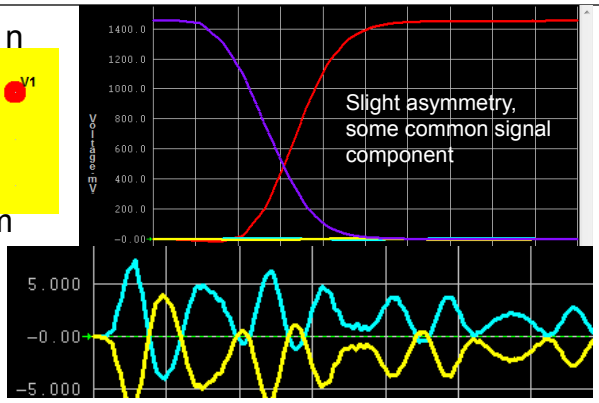
(worst case, h = 30 mils)



Tight coupled diff signal vias, minimal common signal component
NEXT ~ 0.5 mV (-70 dB)



victim



Tight coupled diff signal vias, with a small common signal component
NEXT ~ 6 mV (-48 dB)

Even with diff signals, still a good practice to use robust return path designs to reduce gnd bounce from common signal components

Lesson EPSI-06-90 Termination Strategies and Ground Bounce

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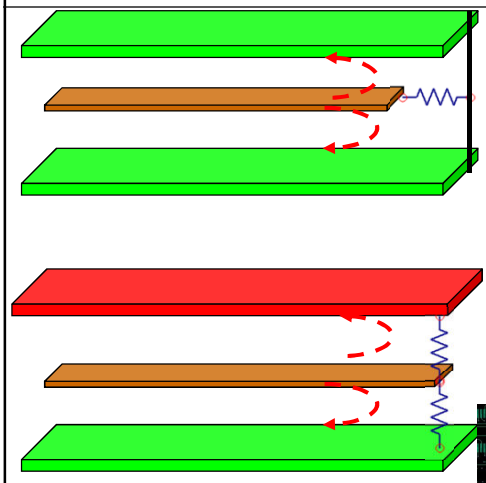
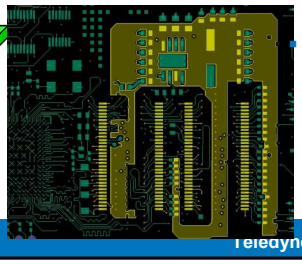
- EPSI-06-90: recorded live, Dec 1, 2013
  - When the return planes are both the same- how to terminate?
  - When the return planes are different voltages- how to terminate?
  - Reducing ground bounce when signals switch at the TX
  - Bypass capacitors when the TX switches

Return Plane Selection and Termination Topologies

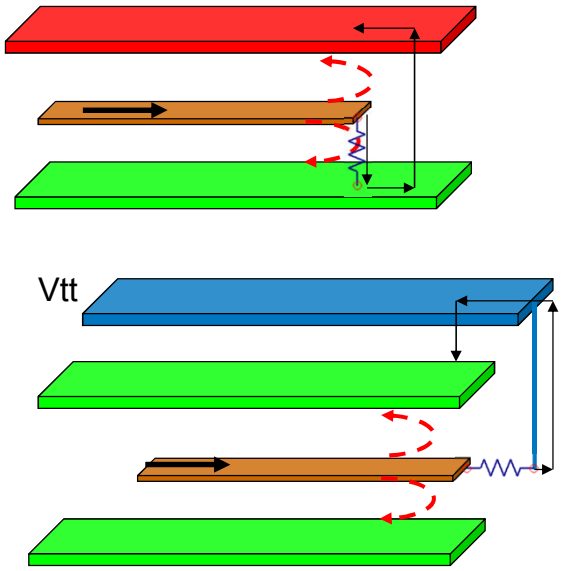


Vtt routed as narrow sections- guaranteed ground bounce



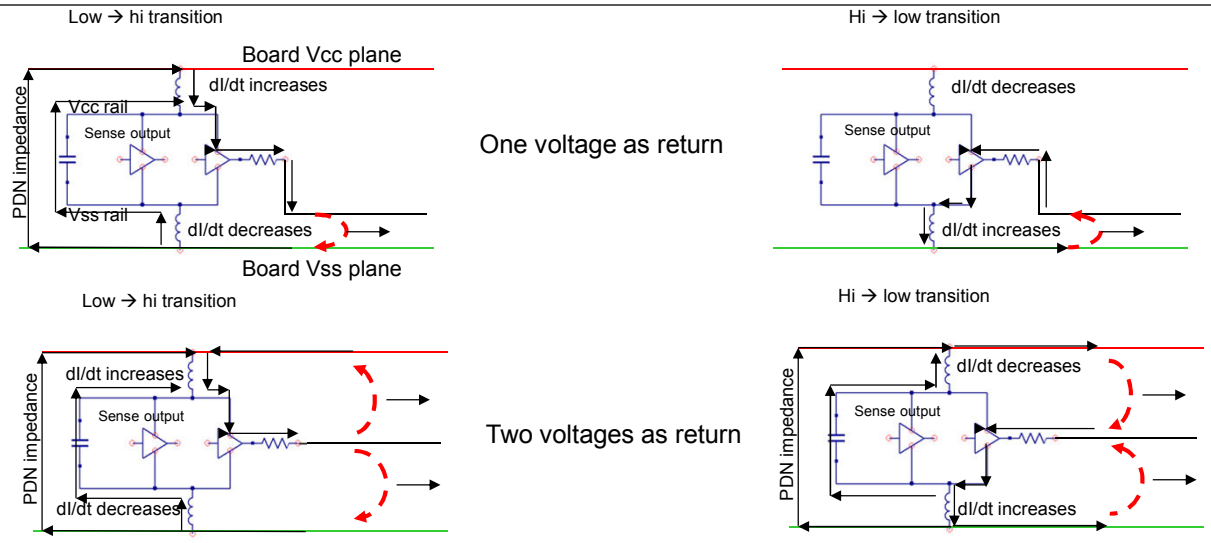
- Best case:
  - Single return voltage planes
  - Resistor terminated to return planes
  - Both Vss, Vcc, Vtt
  - Vss and Vcc planes and thevenin termination
- Sometimes termination topology pushes the switching noise problem to the TX
- Source series termination can reduce ground bounce @ termination
- Watch out if Vtt is not a wide plane:
  - Return current flowing through narrow Vtt paths = ground bounce between multiple RX
  - Still need to provide low impedance between Vtt and Vss, Vcc: thin dielectric, low L capacitors

Potential Ground Bounce at Termination



- Case 1:
  - Mixed return planes
  - Single resistor
  - Vss-Vcc impedance sees half of the return path- injects noise into cavity
  - All signals sharing cavity return path see ground bounce
  - Reduce ground bounce by engineering low impedance, low L caps
- Case 2:
  - Using Vss returns and Vtt termination
  - How does return current get form Vtt to Vss?
  - Need to provide low impedance between Vtt and Vss, or all signals sharing Vtt will see ground bounce

Switching Noise @TX: Follow the Return Current



Switching noise from package lead inductance and PDN impedance
The more on-die capacitance at I/O, the better

For Low and Robust Ground Bounce When Signals Change Return Layers

- Always use Vss (ground) as the return plane
- Place at least one return via adjacent to every signal via
  - (may be able to get away with 5 signals per return via)
- Use differential signals for all high speed signals, minimize common signal component (mode conversion)
  - Still add return vias to reduce gnd bounce from common signals
- When return planes are not the same voltage, use return vias between similar planes: Vcc to Vcc and Vdd to Vdd
- When none of the return planes are the same: re-design the stack up
- As fall back, use as thin a dielectric as possible between different voltage planes add low L decoupling capacitors between them
  - For ~ 2 nH capacitors, maybe 3 signals per capacitor

Lesson EPSI-06-100 Ground bounce and split planes

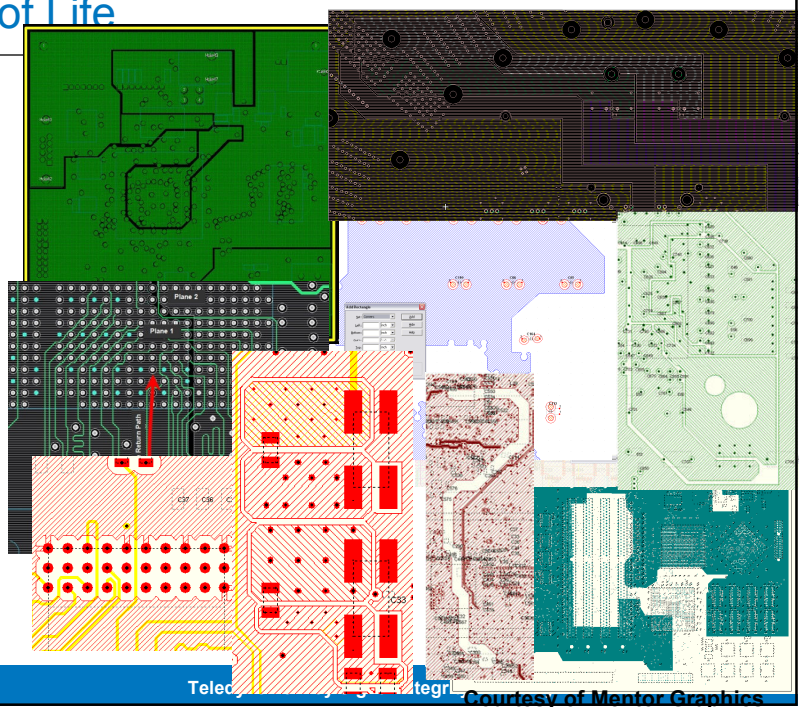
Course EPSI: Essential Principles of Signal Integrity

With Eric Bogatin,
Signal Integrity Evangelist, Teledyne LeCroy Front Range Signal Integrity Lab
Dean, Teledyne LeCroy Signal Integrity Academy
Adjunct Professor, University of Colorado, Boulder, ECEE

- EPSI-06-100: recorded live, Dec 1, 2013
  - Split power planes are inevitable with 5 to 50 power rails
  - Why return currents on split planes generates ground bounce
  - How to think about return current passing through the splits in planes
  - 7 important design fixes to reduce ground bounce in splits planes

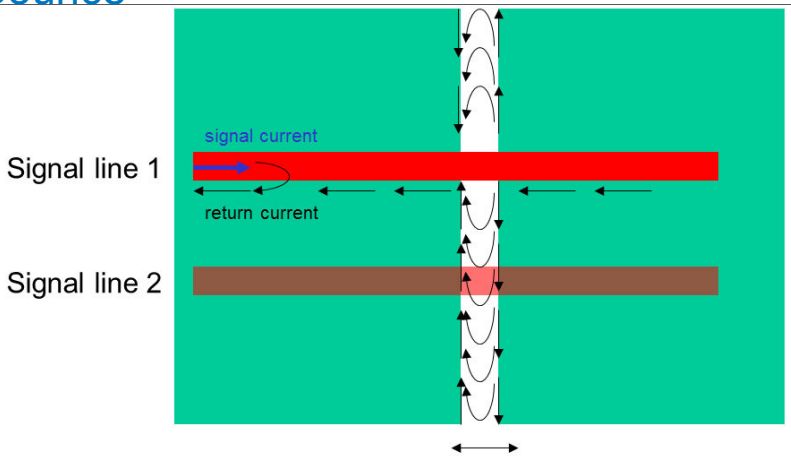
Split Planes are a Fact of Life

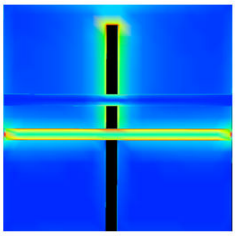
- Proliferation of independent supply voltages
  - Typically 3-30
- Many share a common plane
- Ground bounce arises when signals' return current crosses a split
- When one return plane in stripline has a gap, half the return current will see ground bounce
- Always use solid ground planes- need VERY compelling reason to split
  - Sensitive to low frequency IR drop noise ~ 1 mOhm x 0.1 A ~ 100 uV



Courtesy of Mentor Graphics

Signal Crossing Gaps Generates Long Range Ground Bounce

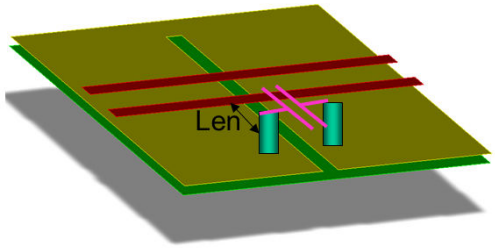


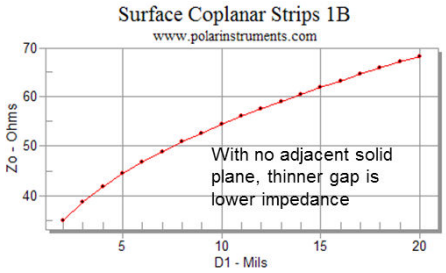


Return current spreads along the "slot wave mode" between the plane edges, leaving voltage drop in its wake

Ground bounce voltage across the gap
More signals crossing gap, more dI/dt
Any signals sharing this return path see the voltage in their path
How to reduce the impedance of the gap?

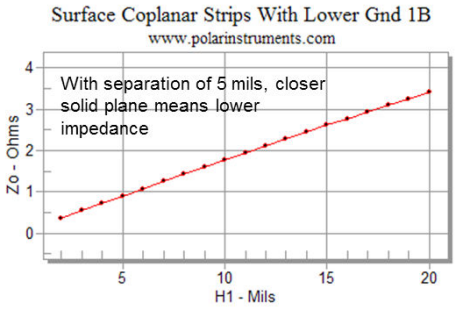
Reduce Ground Bounce by Reducing Impedance of the Gap





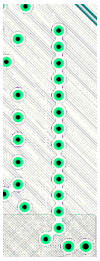
1. Engineer narrow gap
2. In stack up, use adjacent solid plane
3. Add caps across the gap, close to signals
   ~ 2 x 10 nH/inch x Len + 2 nH ~ 4 nH
   (how many signals per cap?)

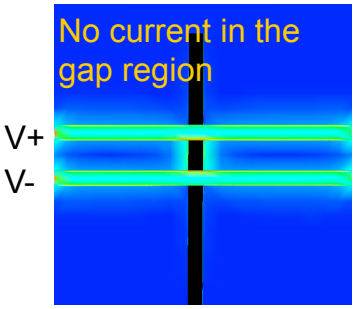
$$\frac{n_{signals}}{n_{caps}} = \frac{V_{gnd}}{V_{sig}} \times 50 \times \frac{RT[n\,sec]}{L_{cap}[nH]} = 0.1 \times 50 \times \frac{1n\,sec}{4[nH]} \sim 1$$



Reducing Ground Bounce With Gaps in Planes

1. Don't allow gaps in return planes
2. Stack planes-with-gaps between solid ground planes
3. Route around the gaps
4. Watch out for unintentional gaps
5. Route as differential signals
6. Use an adjacent solid plane, as thin a dielectric as possible
7. Span gap with low inductance capacitors.



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