Lesson AGCD-01-01 Download the pdf slides here

Course AGCD: Advanced Gigabit Channel Design

With Eric Bogatin,
Signal Integrity Evangelist, Teledyne LeCroy Front Range Signal Integrity Lab
Dean, Teledyne LeCroy Signal Integrity Academy
Adjunct Professor, University of Colorado, Boulder, ECEE

- AGCD-01-01: recorded live, Dec 1, 2013
  - Opening your eyes by optimized channel design
  - Download a pdf copy of the slides by clicking on the link on this page

Lesson AGCD-01-10 High speed serial links and differential pairs

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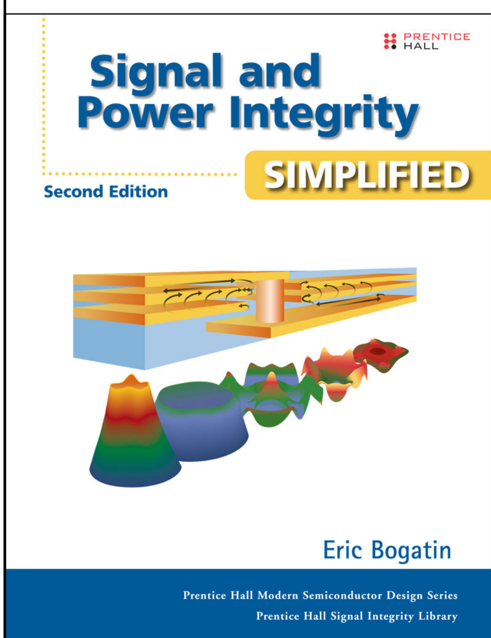
- AGCD-01-10: recorded live, Dec 1, 2013
  - Common elements to all high speed serial links like PCIe and USB
  - Why differential pairs and differential signaling
  - The nature of signal and return current flow in a differential pair
  - Reduced ground bounce sensitivity in differential pairs

Outline

- Day 1
  - ✓ AGCD 1 Opening eyes
  - ✓ AGCD 2 Differential pairs and routing
  - ✓ Lunch
  - ✓ AGCD 3 Lossy Lines and ISI
  - ✓ AGCD 4 Channel to channel cross talk
- Day 2
  - ✓ AGCD 5 Mode conversion
  - ✓ AGCD 6 Discontinuities
  - ✓ Lunch
  - ✓ AGCD 7 Transparent Via Design
  - ✓ AGCD 8 Practical consideration

For More Information



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AGCD: A 2-Day Workshop

- **Day 1**
  - ✓ **AGCD 1 Opening eyes**
  - ✓ AGCD 2 Differential pairs and routing
  - ✓ Lunch
  - ✓ AGCD 3 Lossy Lines and ISI
  - ✓ AGCD 4 Channel to channel cross talk
- Day 2
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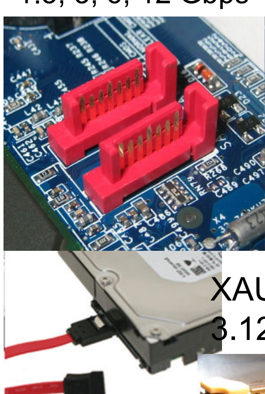
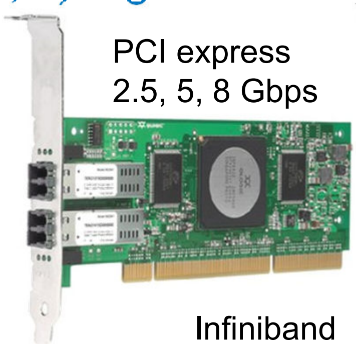
  - ✓ Lunch
  - ✓ AGCD 7 Transparent Via Design
  - ✓ AGCD 8 Practical consideration

Three Important Trends:
1) Differential pairs, 2) High data rates, 3) Always increasing

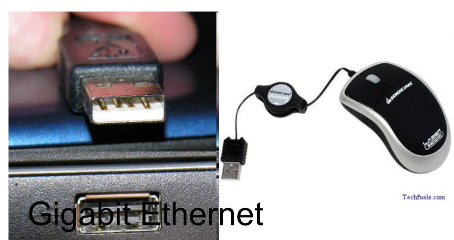
SATA (serial ATA)
1.5, 3, 6, 12 Gbps



PCI express
2.5, 5, 8 Gbps

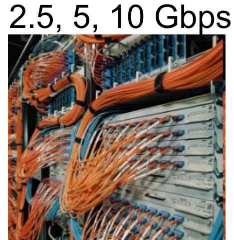


USB
0.012, 0.48, 5 Gbps

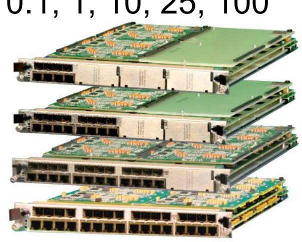


XAUI
3.126, 6.25, 10 Gbps

Infiniband
2.5, 5, 10 Gbps

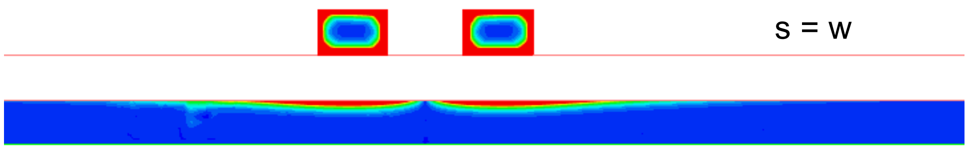


Gigabit Ethernet
0.01, 0.1, 1, 10, 25, 100



Why Differential Signaling?

- Differential signaling: using two transmission lines to transport 1 bit of information: a bit and its complement
- Most important advantages:
  - Greater noise margin for received signal (higher data rate possible with lower SNR than single ended)
  - Can be lower voltage and less power consumption
  - Less power distribution transients and switching noise (SSO) at TRX
  - Less sensitivity to return path discontinuities (vias, gaps, connectors, sockets) (ground bounce)
- Re-think differential interconnect properties- very different properties than single-ended:
  - When the return path is an adjacent plane (microstrip, stripline)
  - When the return path is NOT an adjacent plane (connectors, vias, twisted pair, sockets, packages,…)



Lesson AGCD-01-20 The right way to think about differential pairs

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- AGCD-01-20: recorded live, Dec 1, 2013
  - The right way of thinking about current propagation in differential pairs
  - The importance of the return plane to a differential pair
  - A major source of confusion in the industry
  - Why board level differential pairs are very different than twisted pairs

Lesson AGCD-01-30 The major problems with interconnects - 1

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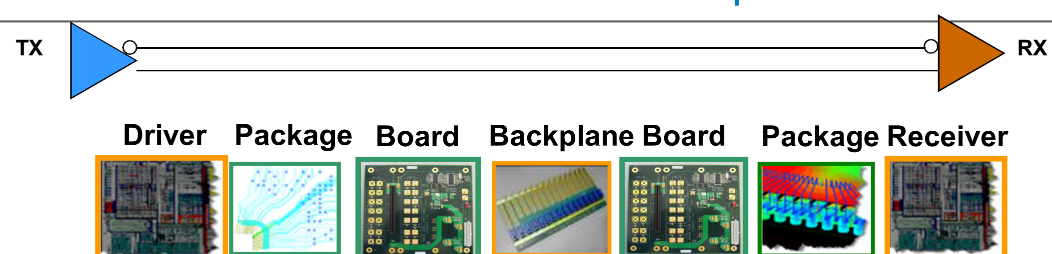
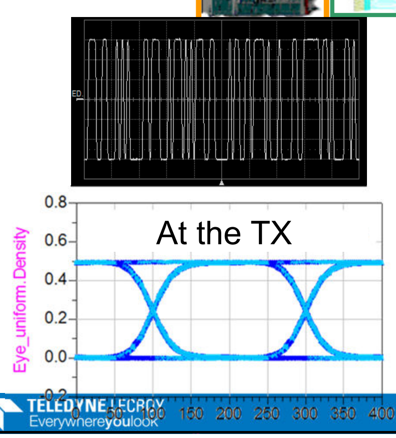
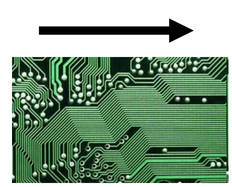
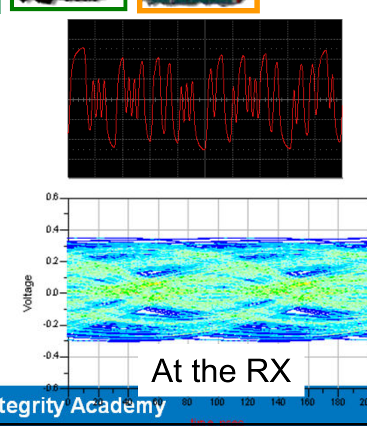
- AGCD-01-30: recorded live, Dec 1, 2013
  - Interconnects are not transparent
  - Most important step: finding the root cause
  - The first two chief deterministic problems with interconnects
  - Reflections and losses

The Real World: Interconnects are Not Transparent









1. What is the root cause
2. What can be done to eliminate these problems?

The Most Important Design Principle

- Fastest way to solve a problem is to identify its root cause
- If you have the wrong root cause, you will only fix the problem by luck

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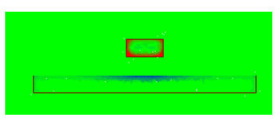
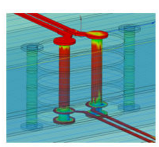
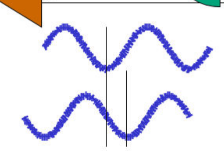
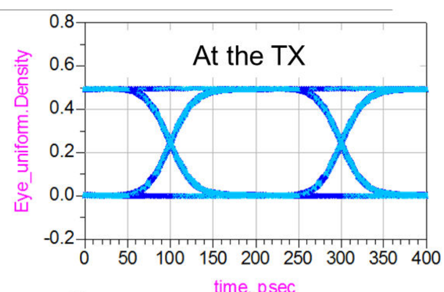
Four Chief Deterministic Problems to Manage

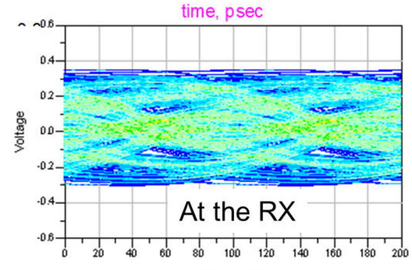
- Losses
  - ✓ Boards
  - ✓ Cables
- Reflections
  - ✓ Between all interfaces
  - ✓ Vias
- Noise: cross talk
  - ✓ Boards (return planes)
  - ✓ Packages
  - ✓ Connectors, vias
- Mode conversion
  - ✓ Routing
  - ✓ Fiber weave
  - ✓ Connectors











Mantra: LRN-M: “Losses, Reflections, Noise, Mode conversion”

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Lesson AGCD-01-40 The major problems with interconnects - 2

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- AGCD-01-40: recorded live, Dec 1, 2013
  - The last of the four problems with interconnects
  - Cross talk and mode conversion
  - The root cause of each interconnect problem

Lesson AGCD-01-50 The role of simulation in interconnect design

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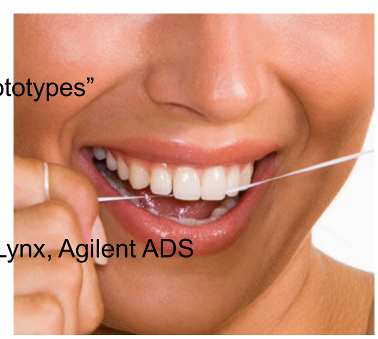
- AGCD-01-50: recorded live, Dec 1, 2013
  - The process of analyzing interconnect problems
  - Why simulation is so important
  - Step response and single bit response
  - PRBS signals and eye diagrams

General Approach to Multi Giga Bit Serial Link Design

- Understand the essential principles (intuition still drives the design process)
- Find the root cause of the problems
- Translate the root cause into design guidelines, technology selection
- Do everything that is free (habits) whenever possible, including signal processing- equalization
- If it costs extra, estimate "bang for the buck" with first-order estimates, then simulation (virtual prototypes)
- Most interconnect/TRX properties interact in complex ways- leverage simulations
  - Time domain: step response (TDR, TDT), single bit response (SBR), peak distortion analysis (PDA), pseudo random bit sequence (PRBS), eye diagram
  - Frequency domain: signal spectra, transfer functions, S-parameters,

Simulation and Measurement Tools as Risk Reduction

- If you don't simulate, it doesn't mean your product won't work.   …you just won't know until you build it and test it
  - ***"You've gotta ask yourself one question, do I feel lucky? Well, do ya, punk? " --- Clint Eastwood as Dirty Harry***
- Simulation is like flossing- everyone should do it for risk reduction, but not everyone does
  - Reduce the risk of failure ("simulation will increase your luck")
  - Reduce the number of board spins
  - Enable you to predict product margins- how robust the design is
  - Enable you to explore "bang for the buck" tradeoffs: build "virtual prototypes"
- Examples of simulation and measurement tools:
  - Circuit simulator: QUCS (Quite Universal Circuit Simulator)
  - 2D field solver: Polar Instruments SI9000
  - 3D field solver: Simberian Simbeor
  - Circuit simulator with integrated 2D, 3D field solver: Mentors' HyperLynx, Agilent ADS
  - TDR/VNA instruments: LeCroy SPARQ
  - Hi bandwidth scopes: LeCroy WaveMaster
  - Measurement analysis software: LeCroy SI Studio



Five Important Simulation Types

- Signal quality @RX (includes driver properties, w, wo equalization):

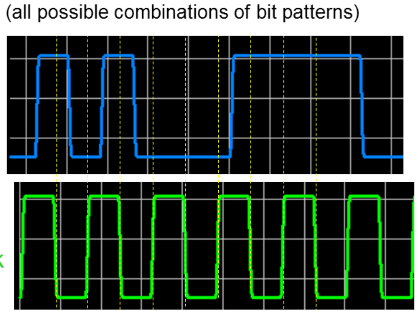
The Eye Diagram:

The Most Important FINAL Metric of Performance

A Pseudo Random Bit Sequence (PRBS)
(all possible combinations of bit patterns)

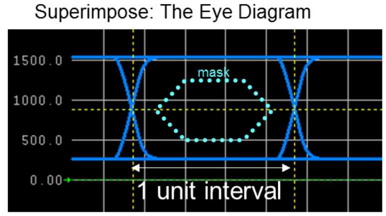
data

clock



A synchronous clock
2 bits per clock (double data rate)
Data read edge-triggered

Take every bits,
Align synchronous with the clock
Superimpose: The Eye Diagram



If ALL RX voltage is outside the mask, bit error ratio (rate) will be acceptable ($< 10^{-12}$)

If any signal "violates" the mask, there may be a bit error

Vertical collapse: noise margin (noise)
Horizontal collapse: timing margin (jitter)

Eye is affected by signal quality within one UI- distortion of initial bit, and noise from one bit to other bits

Lesson AGCD-01-60 S-parameter simulation examples

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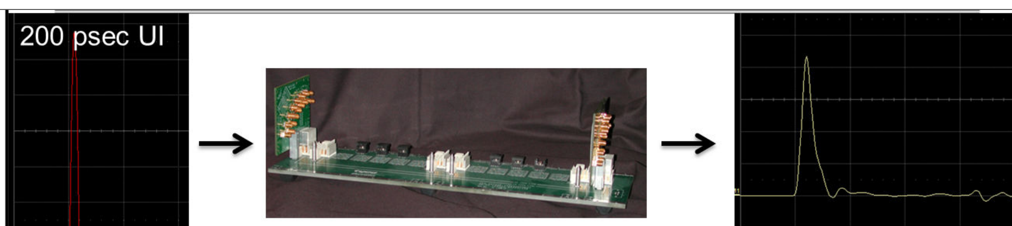
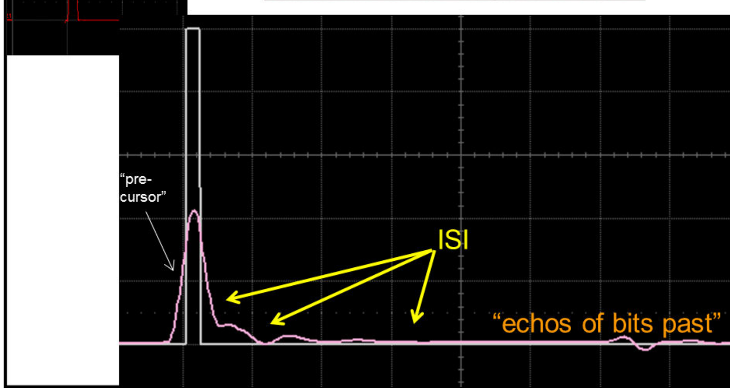
- AGCD-01-60: recorded live, Dec 1, 2013
  - Single bit response and ISI
  - Important figures of merit: how many bits are in the channel, interacting?
  - Insertion and return loss in the time or frequency domains

Single Bit Response of a Channel Identifies Inter-Symbol Interference (ISI)

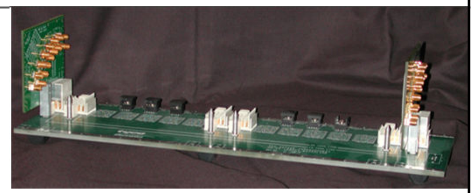




Some ISI, within ~ 6 bits can be compensated with FFE, DFE, CTLE equalization

Long time echoes, generally due to reflections- hard to equalize

Important Figures of Merit for a Channel

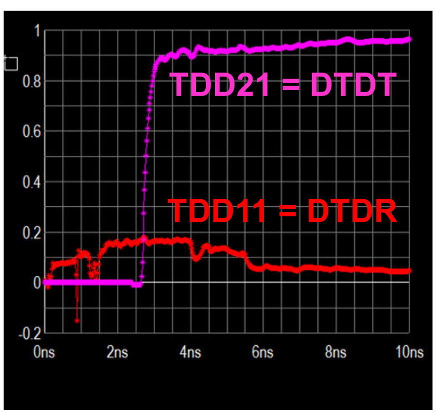


- How many bits in the channel:
  - Time delay of channel/Unit interval = TD/UI
  - Ex: 36 inch channel, TD ~ 36in/6 inch/nsec = 6 nsec
  - @ 10 Gbps, UI = 0.1 nsec
  - TD/UI = 6 nsec/0.1 nsec = 60 bits in the channel!!
- How long does a bit stay in the channel:
  - If there are two reflections: worst case round trip = 2 x TD = 12 nsec
- With reflections, how many bits will see ISI?
  - 2 x TD/UI = 12 nsec/0.1 nsec = 120 bits!!
  - Reflections can cause very long term ISI

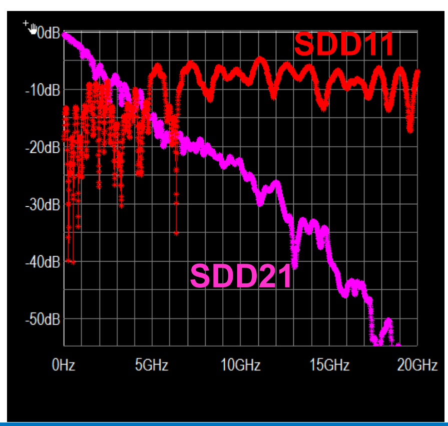
Five Important Simulation Types (con't)

- Interconnect behavior (S-parameters):
  4. Time domain: TDR, TDT or DTDR (differential TDR)
  5. Frequency domain: return loss, SDD11, and insertion loss, SDD21

Time domain



Frequency domain



And all the other S-parameters….but what frequency to worry about?

Lesson AGCD-01-70 PRBS signals in the frequency domain

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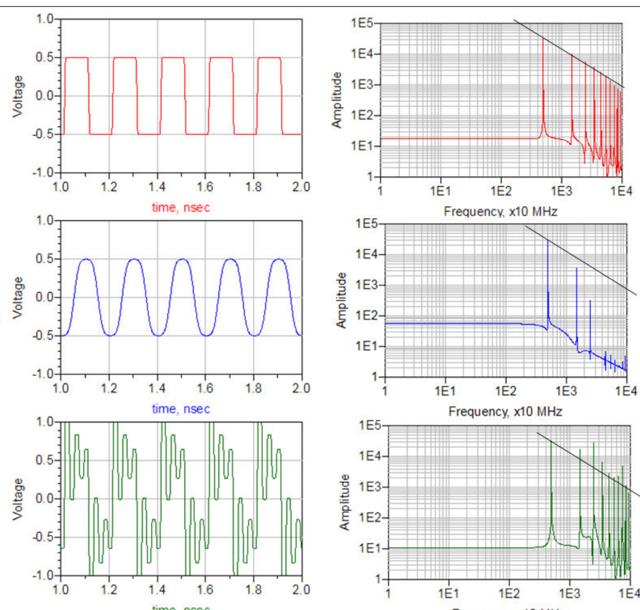
- AGCD-01-70: recorded live, Dec 1, 2013
  - Clock signals in the frequency domain
  - Rise time and the bandwidth in the frequency domain
  - PRBS signals and their spectra
  - Structure within the unit interval and its impact in the frequency range

Periodic Waveforms and Spectra

Ideal square wave:
5 GHz clock frequency
Period = 200 psec
RT = 1 psec

Square wave:
With 10-90 RT = 40 psec
~ 20 % period

Ideal square wave:
5 GHz clock frequency
RT = 1 psec
With ringing



Amplitude drops off with 1/f

Above 1st harmonic, Amplitude drops off faster than 1/f

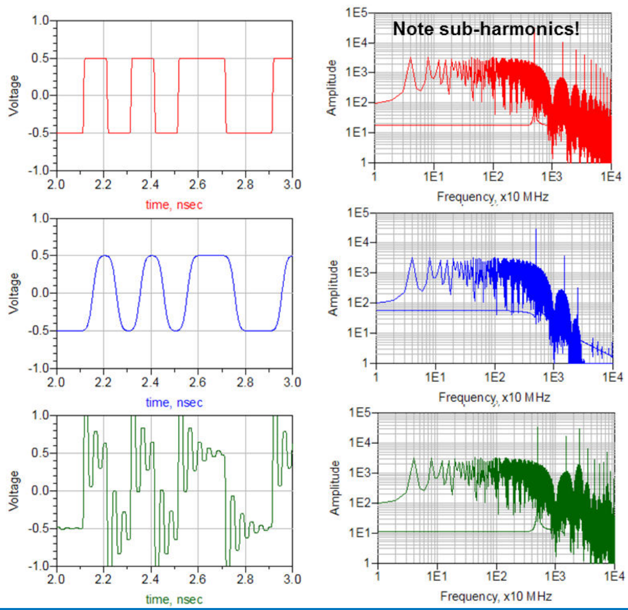
Above 1st harmonic, Amplitude can be larger than ideal square wave!

PRBS Waveforms and Spectra

10 Gbps PRBS
5 GHz Nyquist frequency
UI = 100 psec
RT = 1 psec

10 Gbps PRBS
With 10-90 RT = 40 psec
~ 40 % UI

10 Gbps PRBS
5 GHz Nyquist frequency
RT = 1 psec
With ringing



Information about features within the UI encoded in harmonics > 1st

Information about the data encoded in harmonics < 1st

Lesson AGCD-01-80 PRBS signals in the frequency domain

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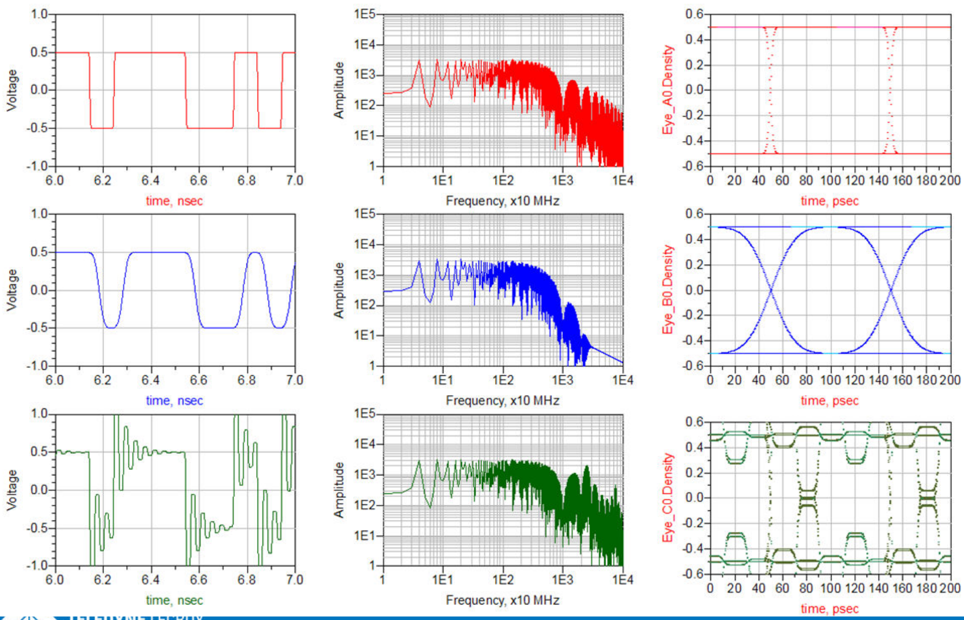
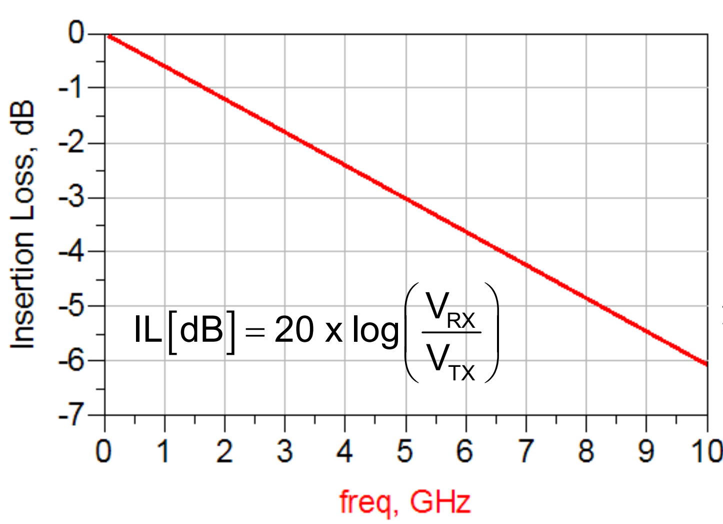
- AGCD-01-80: recorded live, Dec 1, 2013
  - PRBS signals in the time and frequency domain and eye diagrams
  - Mapping data patterns and unit intervals to frequency domain
  - Impact from frequency dependent attenuation on the spectrum of signals
  - The bandwidth of PRBS signals in a lossy channel and the Nyquist frequency

PRBS Waveforms, Spectra and Eyes- no attenuation



Typical Attenuation (Insertion Loss) Behavior

Typical Frequency Dependent Attenuation



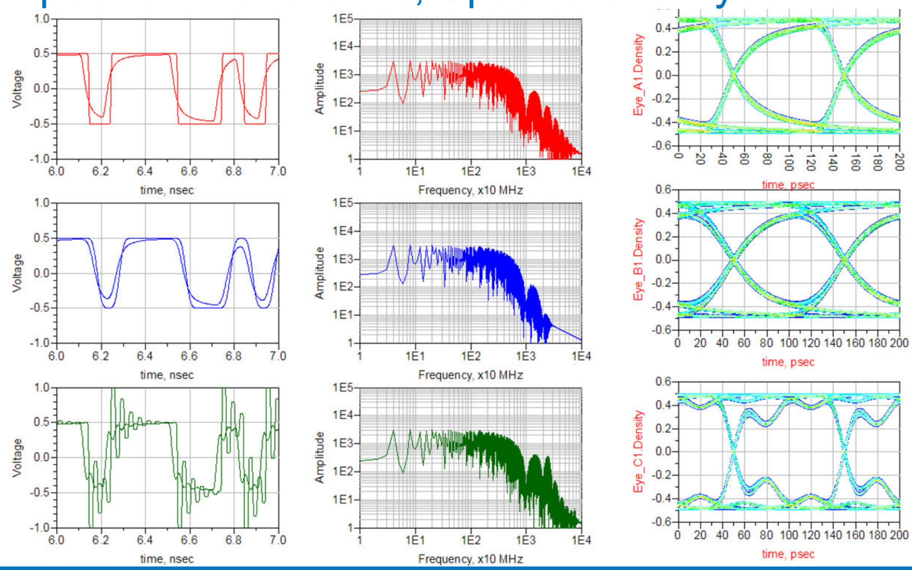
$$IL[dB] = 20 \text{ x } \log\left(\frac{V_{RX}}{V_{TX}}\right)$$

In this example:

@ 5 GHz (Nyquist for 10 Gbps)
Attenuation = -3 dB
V_{RX} = 70% x V_{TX}

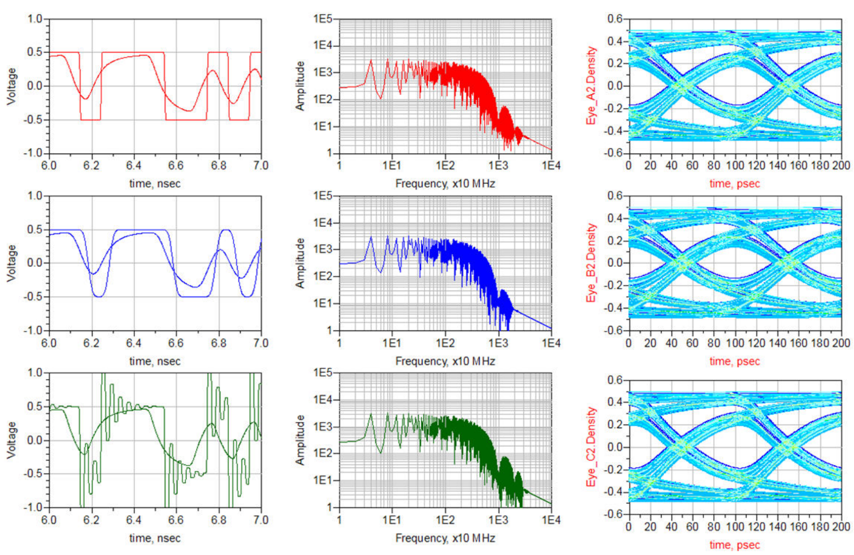
-3 dB@ Nyquist

Impact on Waveforms, Spectra and Eyes from Attenuation



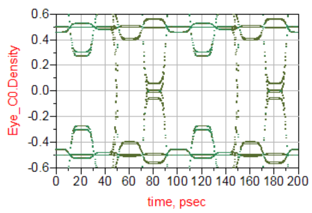
-8 dB@ Nyquist

Impact on Waveforms, Spectra and Eyes from Attenuation

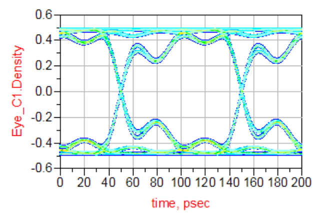


Observations

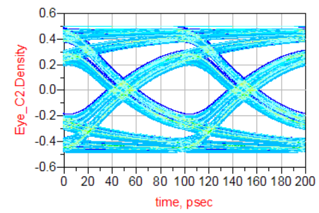
- Loss can dramatically reduce impact from reflection noise (a little loss can be your friend)



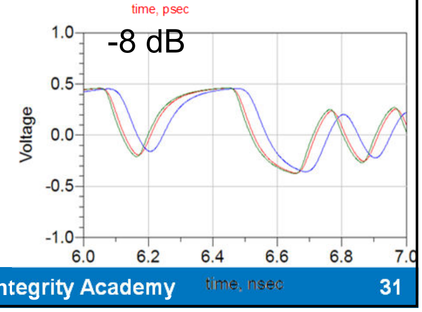
0 dB



-3 dB



-8 dB



- When attenuation @ Nyquist ~> -8 dB,
  - Structure within UI not important
  - Attenuation is the "great equalizer"
  - The highest freq component significant is the Nyquist

Figures of Merit in the Frequency Domain

- Given bit rate of BR[Gbps]
  - ex: 10 Gbps
- Unit interval, UI [nsec] = 1/ BR[Gbps]
  - Ex: 0.1 nsec = 100 psec
- Nyquist [GHz]= ½ x BR[Gbps], 1st harmonic = Nyquist = ½ x BR
  - ex: 5 GHz
- 5th harmonic = 5 x Nyquist = 2.5 x BR (~BW @ TX, with fast TX)
  - ex: 25 GHz
- In lossy interconnect (SDD21 > ~ -8 dB)
  - Signal BW @RX ~ Nyquist = ½ BR (ex: 5 GHz)

Summary

- All high speed serial links are differential pairs
- Data rates are only going to increase
- Interconnects are not transparent
- The process for successful high speed design is
  - Identify the problems
  - Find the root cause
  - Apply essential principles to translate root cause into design guidelines
  - Do everything possible that is free to design out problems
  - Use analysis tools to evaluate cost-performance tradeoffs using virtual prototypes