BLACKHAWK CORE

56.25G PAM4 SERDES PMD

USER SPECIFICATION

VERSION: 0.15

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Revision History

Revision	Date	Change Description
0.1	5/1/2015	Initial version
0.2	5/19/2015	Updated pam4 mode, OSR mode
0.3	6/15/2015	Updated information about line voltages
0.4	6/22/2015	Corrected rx/tx reset description. Also updated PCS interface description for the RX low latency mode and back channel encoder and decoder.
0.5	7/13/2015	Added section on analog signals required for simulation on serial pins
0.6	8/21/2015	Updated for changes related to AMS version 0.90
0.7	8/26/2015	Added refclk and micro_clk rates, updated PLL block diagram
0.8	9/9/2015	Cleanup and add rate table for supported clocks and line rates
0.9	9/16/2015	Added afe_rx***k***_clk32 and afe_tx***k***_clk32 output clock pin description.
0.10	10/7/2015	Added new PRBS polynomials
0.11	10/16/2015	Updated NRZ,PAM4 modes. Updated rate table.
0.12	11/10/2015	Updated description for pmd_fec_fdbk_status_***k*** and fec_fdbk_ctrl_***k***. Also updated rate table.
0.13	12/1/2015	Updated analog voltage levels from mV to V on serial inputs and outputs
0.14	12/3/2015	Added new analog supply pads pad_clkvdd0p8 and pad_clkgnd
0.15	1/15/2016	Updated analog voltage modeling section

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Abbreviations

BR	Baud-Rate	PMI-LP	Low Priority Parallel Management Interface
CDR	Clock Data Recovery	RMIC	Register Management Interface Controller
DSC	Digital Signal Conditioning block.	RS	Reconciliation Layer
EEE	Energy Efficient Ethernet	TLB	Test and Loopback
FC	Fiber Channel	TR	Timing Recovery
FEC	Forward Error Correction	TS	Training Sum
KR	Refers to IEEE802.3 10G backplane standard		
LD	Local Device		
LIF	1G EPON Line Interface		
LP	Link Partner		
MDIO	IEEE serial management interface		
MIC	Management Interface Controller		
MLD	Multi-Lane Distribution		
NRZ	Non-Return-to_zero binary code		
OSR	Over-sample Ratio		
OSxN	Oversampled mode N		
PAM4	Pulse Amplitude Modulation with 4 levels		
PAM4-NS	PAM4 normal slicer 4 levels		
PAM4-ES	PAM4 extended slicer 7 levels		
PCS	Physical Coding Sub-layer		
PI	Phase interpolator		
PMD	Physical Medium Dependent		

TABLE 1: LIST OF ABBREVIATIONS

Blackhawk User Specification

INTRODUCTION

The Blackhawk core is a completely independent octal (x8) lane 56.25Gbps PAM4/28.125 Gbps NRZ SerDes core suitable for Optical and Backplane applications. The Blackhawk core has 2 independent PLLs that can be configured completely independently with separate refclks and each transmitter and receiver for each lane can select between the 2 VCO clocks. It is targeted primarily for high density integration in high bandwidth products and it is optimized for low power consumption and area efficient design. Blackhawk core supports data rates from 1.00Gbps to 28.125Gbps in NRZ model same as Blackhawk core and date rates upto 56.25Gbps in PAM4 mode. Each lane can be configured independently to run in PAM4 or NRZ modes with different date rates.

Blackhawk SerDes Core data path interface is designed to work well with an IEEE PCS or other coding layers for various high-speed serial link applications. Independent parallel management interface (PMI) enables interface for fast management access. The core can also be managed through a serial MDIO port. The main design focus is not only to meet industry requirements in terms of reduced area and power consumption to the greatest extent, but also to achieve superior performance.

Blackhawk has a built-in remote loopback mode, digital loopback mode, Fixed-Pattern generator and PRBS generator & checker to support testing. The core also supports a micro subsystem with 4 ARM M0+ processor cores.

The digital functionality, register address mapping and test features of the base core are designed to be protocol agnostic. The core provides control and status interfaces that may be used by an upper layer to implement standards compliant registers.

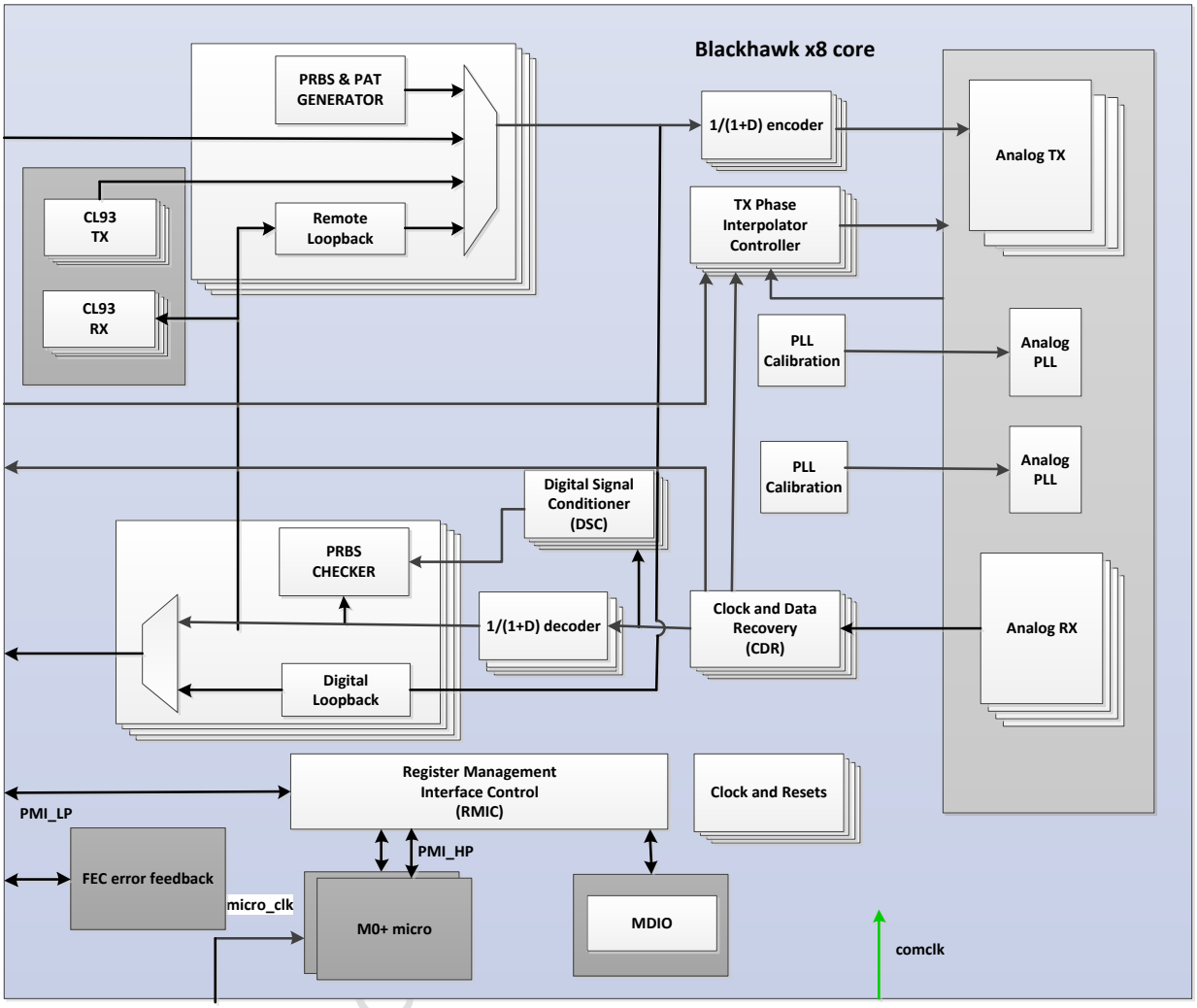


FIGURE 1: BLACKHAWK FUNCTIONAL BLOCK DIAGRAM.

Figure 1 shows the high level details of an octal lane Blackhawk configuration.

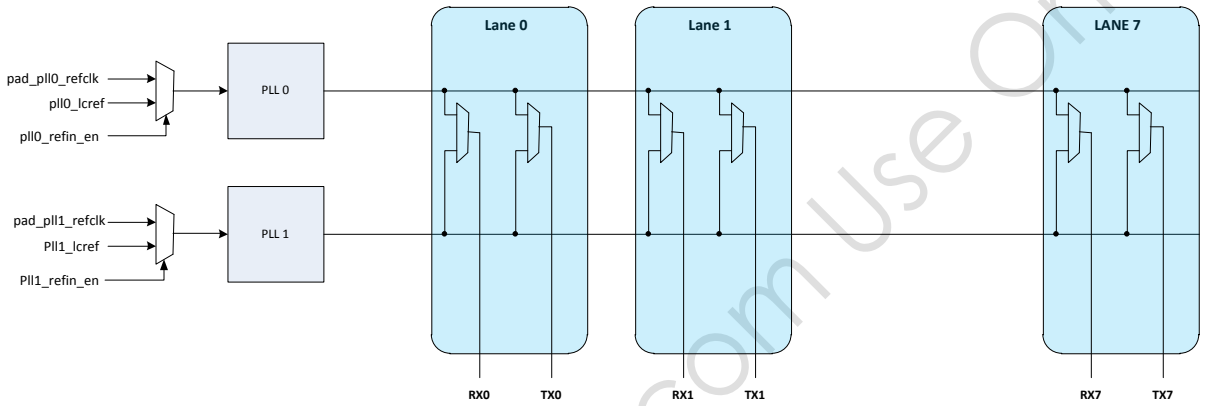
The digital logic of the core is designed for a multi-lane delivery. The core requires 3 continuous clocks:

1. Differential Reference clock for each analog PLL: Primary clock frequencies are 106MHz, 125MHz, 156.25MHz, and 312.5MHz. Other refclk frequencies are supported as well. See AMS document for a complete list of refclk frequencies and VCO rates.
2. Digital reference clock for the digital logic (comclk): This is the primary clock for the digital control path. Its frequency needs to be between 125MHz to 175MHz and may be connected externally to the core output

pin "pmd_pll0_refclk_out" or pmd_pll1_refclk_out if the frequency meets the requirements for comclk.

3. Clock for the micro subsystem (micro_clk): Based on performance requirements, this is currently targeted to be 312.5 MHz.

This core supports 2 independent PLLs in the AFE with 2 separate pll calibration functions in the digital logic as shown in the block diagram.



Features

- Octal (x8) PAM4 56.25Gbps/NRZ 28.125Gbps SERDES optimized for Backplane and Front Panel applications.
- Supports per lane speeds of 1.00 to 56.25Gbps.
- 2 independent PLLs with wide tuning range 22.6 – 30.0 GHz.
- Each PLL also supports a separate 15.0-22.6 GHz VCO for lower frequency operation
- Transmitter with fully programmable 10-tap FIR.
- Integrated AC coupling on RX inputs
- Programmable 2-stage RX equalizer with 0-8 dB boost, approx 0.5 dB/step.
- Includes a 14-tap DFE with adaptive control and VGA with AGC.
- Each reference clock is differential and typical clock frequencies are 106.25MHz, 125MHz, 156.25MHz, 161.13MHz, and 312.5MHz. Other frequencies are supported as well. See AMS document for complete list.

Suports 2X and 4X reference clock frequencies using internal div2/div4 dividers.

- Maximum BER of 10^-15 without FEC across all operating conditions in NRZ mode.
- Maximum BER of 10^-15 with FEC across all operating conditions in PAM4 mode.
- Max Power: PMA + PMD: TBD mW per Serdes (Octal Macro).
- TSMC 16nm FF process 13 layer Metal stack
- Supply Voltage range: 1.2V Transmit Driver and separate 0.8V analog transmit +/- 5%, Receiver and PLL 1.8V core +/- 5%.
- Junction temperature range -20C to 110C.
- LINKEYE simulation model and IBIS-AMI Model availability.
- PRBS 7, 9, 10, 11, 13, 15, 20, 23, 31, 49, 58 and QPRBS 13 Generator and Checker w/ Burst Error length measurement.
- PRBS Error Analyzer.
- Fixed Pattern Generator which also includes PAM4 fixed patterns of JP03A, JP03B and Transmitter Linearity Test Pattern.
- Remote and Digital Loopbacks.
- Programmable TX and RX polarity inversion
- Clause 93/72 De-Emphasis Training Module.
- MDIO Management Interface: Clause 45 based MDIO. Supports a max speed of 25 MHz for only comclk =125MHz and up.
- Micro Sub System Module with 4 ARM M0+ micro cores
    - A standalone module with one dual-port program SRAM (64KB) shared between 4 M0+ cores and one dual port data SRAM (32KB) shared between the 4 M0+ cores.
- Separate Transmit Phase Interpolator Controls
- Transmit clock alignment circuit to align all transmit clocks to a selected master transmit lane clock.

- Arbitrary logical lane addressing for RX and TX lanes.

Blackhawk Pin Description

The Blackhawk SerDes PMD core is designed for easy integration with a PCS or Chip level logic. The following table shows the pin description of all the analog and digital data path interfaces; control and status pins.

Analog Pins.

Analog bump pads and control pins are copied from the Blackhawk AMS documentation. For details and up to date information, the user is advised to refer to the AMS document and consult the Analog design engineering.

Analog Bonding Pads / Bump List

k = [0, 1, 2, 3] The default setting for all pads		
Pad name	**Direction**	**Description**
pad_pll0_pvdd0p8	In	PLL0 analog supply voltage, 0.8v.
pad_pll1_pvdd0p8	In	PLL1 analog supply voltage, 0.8v.
pad_pll0_pvdd1p8	In	PLL0 analog supply voltage, 1.8V.
pad_pll1_pvdd1p8	In	PLL1 analog supply voltage, 1.8V.
pad_pll0_pgnd	In	PLL0 analog ground
pad_pll1_pgnd	In	PLL1 analog ground
pad_clkvdd0p8	In	Supply voltage 0.8V for RX/TX clk buffers between quads
pad_clkgnd	In	Ground for RX/TX clk buffers between quads
pad_rvdd0p8	In	Receiver supply voltage, 0.8V.
pad_rgnd	In	Receiver ground
pad_tvdd0p8	In	Transmitter supply voltage 0.8V.
pad_tvdd1p2	In	High voltage transmitter supply voltage 1.2V.
pad_tgnd	In	Transmitter ground

pad_pll0_refclkp	In	PLL 0 reference clock input
pad_pll0_refclkn	In	PLL 0 reference clock input, complement
pad_pll1_refclkp	In	PLL 1 reference clock input
pad_pll1_refclkn	In	PLL 1 reference clock input, complement
pad_rdp*k*	In	Receiver *k* input data
pad_rdn*k*	In	Receiver *k* input data, complement
pad_tdp*k*	Out	Transmitter *k* output data
pad_tdn*k*	Out	Transmitter *k* output data, complement
pad_pll0_ptestp	Out	PLL0/Reciever Analog test port
pad_pll0_ptestn	Out	PLL0/Receiver Analog test port, complement
pad_pll1_ptestp	Out	PLL1/Reciever Analog test port
pad_pll1_ptestn	Out	PLL1/Receiver Analog test port, complement

TABLE 2: ANALOG PIN DESCRIPTION

AC-JTAG

ACJTAG *k* = [0, 1, 2, 3] The default setting for all JTAG inputs = 0		
Pin name	**Direction**	**Description**
test_jtag	In	Asserts AC or DC JTAG operation , but over-ridden by pll_iddq 0: ACJTAG is OFF 1: ACJTAG is ON
test_ac_mode	In	0: For DC testing Comp reference is RX Vcm 1: Enables AC testing Allow 0.5ms-5ms for complete power up, depends on the AC cap value. Comp reference is LPF output
test_rxacj_st[5:0]	In	Receiver configuration bits [5] Input Vcm ~100mV [4:2] Hysteresis – see AMS document [1:0] Filter BW 00 – 8.5MHz, default 01 – 11MHz 10 – 16MHz 11 – Force Vcm during AC mode

test_rxd_init_mem	In	Initial value set enable for rxdp_init_val[i]
test_rxdp_init_val[*k*]	In	Initial value of hysteresis comparator
test_rxdn_init_val[*k*]	In	Initial value of hysteresis comparator
test_txacj_st[3:0]	In	Transmitter Configuration bits Driver output amplitude, mapped to upper 4-bits of main tap. See table in sec 21 of AMS.
test_txd[*k*]	In	AC-JTAG input to transmitter
test_rxdp[*k*]	Out	Single-ended received data from RDP
test_rxdn[*k*]	Out	Single-ended received data from RDN

TABLE 3 : ACJTAG PIN DESCRIPTION

Analog Control and Status Pins

Pin Name	**Direction**	**Description**
pll0_lcrefn	In/Out	PLL0 LCPLL Reference Clock
pll0_lcrefp	In/Out	PLL0 LCPLL Reference Clock, complement
pll1_lcrefn	In/Out	PLL1 LCPLL Reference Clock
pll1_lcrefp	In/Out	PLL1 LCPLL Reference Clock, complement
pll0_refin_en	In	PLL0 Reference Select 0 – pad_pll0_refclkp/n 1 – pll0_lcrefp/n
pll1_refin_en	In	PLL1 Reference Select 0 – pad_pll1_refclkp/n 1 – pll1_lcrefp/n
pll0_refout_en	In	PLL0 Enables the SerDes to drive internal refclk bus 0 – pll0_refoutp/n = hiZ 1 – pll0_refoutp/n = pad_pll0_refclkp/n
pll1_refout_en	In	PLL1 Enables the SerDes to drive internal refclk bus 0 – pll1_refoutp/n = hiZ

		1 – pll1_refoutp/n = pad_pll1_refclkp/n
pll0_refoutp	Out	Buffered copy of pad_pll0_refclkp
pll0_refoutn	Out	Buffered copy of pad_pll0_refclkn
pll1_refoutp	Out	Buffered copy of pad_pll1_refclkp
pll1_refoutn	Out	Buffered copy of pad_pll1_refclkn
rescal[3:0]	In	Resister Calibration Control code for global resistor calibration, and should be connected to a chip level RESCAL/PVTMON block. **This code must be tuned and stable before releasing Core reset for Blackhawk core, and especially the PLL tuning. This is required for both functional and DFT modes.**
tx_drv_hv_disable	In	High voltage driver strap. 0 - High Voltage mode (1.2V supply) 1 - 1V mode
pmd_pll0_refclk_div4	In	Enable divide by 4 on pll0_refclk input
pmd_pll0_refclk_div2	In	Enable divide by 2 on pll0_refclk Input
pmd_pll1_refclk_div4	In	Enable divide by 4 on pll1_refclk input
pmd_pll1_refclk_div2	In	Enable divide by 2 on pll1_refclk Input
pmd_pll0_rterm200	In	set refclk0 termination impedance to 200 Ohm if two cores share a common, 100 Ohm refclk source
pmd_pll0_rterm300	In	set refclk0 termination impedance to 300 Ohm if three cores share a common, 100 Ohm refclk source
pmd_pll0_rterm400	In	set refclk0 termination impedance to 400 Ohm if four cores share a common, 100 Ohm refclk source
pmd_pll0_rtermhiz	In	set refclk0 termination impedance to HiZ, and typically used if the ptestp/n bumps are connected to the refclkp/n bumps in the pkg
pmd_pll1_rterm200	In	set refclk1 termination impedance to 200 Ohm if two cores share a common, 100 Ohm refclk

		source
pmd_pll1_rterm300	In	set refclk1 termination impedance to 300 Ohm if three cores share a common, 100 Ohm refclk source
pmd_pll1_rterm400	In	set refclk1 termination impedance to 400 Ohm if four cores share a common, 100 Ohm refclk source
pmd_pll1_rtermhiz	In	set refclk1 termination impedance to HiZ, and typically used if the ptestp/n bumps are connected to the refclkp/n bumps in the pkg

TABLE 4 : ANALOG CONTROL AND STATUS PINS DESCRIPTION

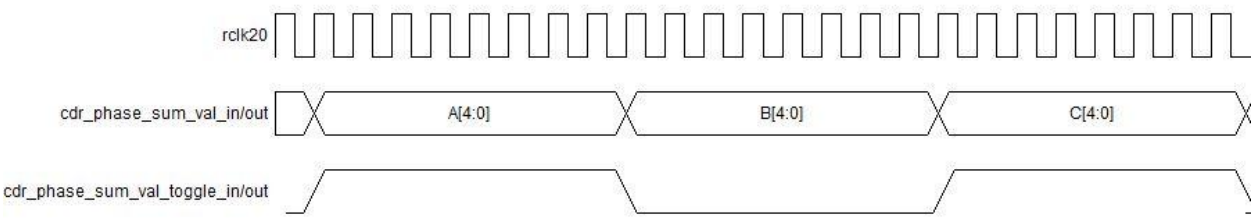
Note: rescal[3:0] inputs may be overridden via register access. If using software override, it must be set before release of core reset. Rescal must not be changed after release of reset.

CDR lock and external TX PI interface pins

Pin Name	Direction, Clk	Description
cdr_phase_sum_val_in_***k***[4:0]	In, async	CDR Phase Sum Value IN.
cdr_phase_sum_val_toggle_in_***k***	In async	CDR Phase Sum Value toggle IN
cdr_phase_sum_val_out_***k***[4:0]	Out pmd_rclk20_***k***	CDR Phase Sum Value OUT
cdr_phase_sum_val_toggle_out_***k***	Out pmd_rclk20_***k***	CDR Phase Sum Value toggle OUT
pmd_tx_pi_ext_pd_dec_***k***	In pmd_tclk20_***k***	TX phase Interpolator controls from an external phase detector. Decrement signal = 1 will remove some phase/delay inside the TX PI.

pmd_tx_pi_ext_pd_inc_***k***	In pmd_tclk20_***k***	TX phase Interpolator controls from an external phase detector. Increment signal = 1 will add some phase/delay inside the TX PI.
cdr_phase_step_cnt_ ***k*** [2:0]	Out pmd_rclk20_***k***	Each step is 1/64 of UI (for OSR1,2,4). This is 2's complement signed number and the range is -2/+2. This is the amount that RX_PI moves by.

TABLE 5 : CDR LOCK AND EXTERNAL TX PI INTERFACE PINS DESCRIPTION



cdr_phase_sum_val_in/out_***k***[4:0]
Sum of CDR phase steps accumulated over 8 rclk20 cycles. Valid value range is -8 to +8. This is a signed number. cdr_phase_sum_val_in_ ***k***[4:0] inputs can be tied off to 5'd0 in non-repeater application.

cdr_phase_sum_val_toggle_in/out_***k***
Toggles every 8 rclk20 clock cycles and coincides with the change in the cdr_phase_sum_val. cdr_phase_sum_val_toggle_in_ ***k*** *can be tied off to 1'b0 in non*-repeater applications.

Val and Val_toggle are generated from the CDR. Val_toggle is toggled every 8th rclk20 clock and also new phase_sum val is latched at the toggle of the signal. At top level, connect the *_in to *_out and vice versa between the system and line side Merlin cores.

Skew requirements for these signals will be furnished later.

Digital Pins

Digital Clocks, Resets and Power Down

Pin Name	Direction	Description
pmd_pll0_refclk_out	Out	Selected refclk output from the analog macro for pll 0.
pmd_pll1_refclk_out	Out	Selected refclk output from the analog macro for pll 1.
pmd_comclk	In	Digital Common clock. comclk is a free running, uninterrupted clock with 50-50 duty cycle and frequency between 125MHz and 175MHz.
micro_clk	In	312.5 MHz clock for running the micro subsystem.
pmd_por_h_rstb	In	PMD main reset, resets registers, data path for entire core including all lanes. Active Low. Minimum assertion time: 25 comclk period.
pmd_core_pll0_dp_h_rstb	In	Datapath reset for all lanes and core logic associated with pll0. Does not reset registers. Active Low. Minimum assertion time: 50 comclk period.
pmd_core_pll1_dp_h_rstb	In	Datapath reset for all lanes and core logic associated with pll1. Does not reset registers. Active Low. Minimum assertion time: 50 comclk period.
pmd_ln_rx_h_rstb_***k***	In	Lane ***k*** *RX* reset registers and data path. Active Low. Minimum assertion time: 25 comclk period.
pmd_ln_tx_h_rstb_***k***	In	Lane ***k*** *TX* reset registers and data path. Active Low. Minimum assertion time: 25 comclk period.
pmd_ln_rx_dp_h_rstb_***k***	In	Lane ***k*** RX datapath reset, does not reset registers. Active Low. Minimum assertion time: 25 comclk period.
pmd_ln_tx_dp_h_rstb_***k***	In	Lane ***k*** TX datapath reset, does not reset registers. Active Low. Minimum assertion time: 25 comclk period.

pmd_iddq	In	Pin to power down the entire core for measuring quiescent current. Active high signal. Should normally be tied low . Minimum assertion time: 25 comclk period.
		All the power down pins are active high. These should be driven low to activate lane.
pmd_ln_rx_h_pwrdn_***k***	In	Lane ***k*** RX power down. . Minimum assertion time: 25 comclk period.
pmd_ln_tx_h_pwrdn_***k***	In	Lane ***k*** TX power down. . Minimum assertion time: 25 comclk period.

TABLE 6 : DIGITAL CLOCKS, RESETS AND POWER DOWN PIN DESCRIPTION

pmd_pll0_refclk_out
This is the final selected digital reference clock coming out of the analog module for pll 0.

pmd_pll1_refclk_out
This is the final selected digital reference clock coming out of the analog module for pll 1.

pmd_comclk
This is the digital common clock that the Blackhawk PMD core uses for all the management ports, common user registers and digital logic. This clock should be a free running, uninterrupted clock with 50-50 duty cycle and frequency between 125 – 175MHz. The user can choose to connect the pmd_refclk_out, if it satisfies the frequency requirement.

micro_clk

This is the clock for running the micro susbsystem. This can be separate from comclk and could be running with a faster clock.

pmd_por_h_rstb
Hard reset. Fundamental Power on Reset from the chip. This resets the whole core and is an active low reset signal. Assertion of this reset will keep all the logic under reset, including the MDIO and RMIC. Minimum assertion time: 25 comclk period.

pmd_core_pll0_dp_h_rstb
Datapath reset for all lanes and core logic associated with PLL0 through a pin. This reset will keep the common logic and data path of all the lanes in both directions associated with pll0 under reset. Including the PLL0 and TX PI. All the user registers will be on comclk and will be available for read and write. This is an active low reset signal. Minimum assertion time: 50 comclk period.

pmd_core_pll1_dp_h_rstb
Datapath reset for all lanes and core logic associated with PLL1 through a pin. This reset will keep the common logic and data path of all the lanes in both directions associated with pll1 under reset. Including the PLL1 and TX PI. All the user registers will be on comclk and will be available for read and write. This is an active low reset signal. Minimum assertion time: 50 comclk period.

pmd_ln_rx_h_rstb_***k***
This is a logical RX lane ***k*** reset through a pin. Resets all the registers and data path associated with receive physical lane ***k***. This is an active low reset signal. Minimum assertion time: 25 comclk period.

pmd_ln_tx_h_rstb_***k***
This is a logical TX lane ***k*** reset through a pin. Resets all the registers and data path associated with transmit physical lane ***k*** including TX PI. This is an active low reset signal. Minimum assertion time: 25 comclk period.

pmd_ln_rx_dp_h_rstb_***k***
Logical RX Lane "***k***" reset through a pin that will keep the receive analog and data path associated with lane "***k***" under reset. Lane user registers are available for read and write. Minimum assertion time: 25 comclk period.

pmd_ln_tx_dp_h_rstb_***k***
Logical TX Lane "***k***" reset through a pin that will keep the transmit analog and data path associated with lane "***k***" under reset including TX PI. Lane user registers are available for read and write. Minimum assertion time: 25 comclk period.

pmd_iddq
Assertion of pmd_iddq pin will gate off all the lane clocks and comclk. None of the resets will be asserted. Hence registers will hold the programmed values. The user is expected to program the analog registers values and power down bits before asserting the pmd_iddq pin. Deassertion of pmd_iddq pin will not guarantee a normal operation. A POR sequence is the only way to recover to a normal status. Minimum assertion time: 25 comclk period.

pmd_ln_rx_h_pwrdn_***k***
Assertion of this power down pin will put the logical receive lane "***k***" datapath under reset and lane clocks will be switched to comclk, as well as AFE receive lane reset/pwrdn pins will be asserted. The lane registers will not be under reset so user should be able to read/write the lane registers.

This pin goes through a dual-meta synchronizer which is reset by POR reset to default value of 1'b1 which means AFE RX lane pwrdn pin will be asserted while POR is asserted. Minimum assertion time: 25 comclk period.

pmd_ln_tx_h_pwrdn_***k***
Assertion of this power down pin will put the logical transmit lane "***k***" datapath under reset and lane clocks will be switched to comclk, as well as AFE transmit lane reset/pwrdn pins will be asserted. The lane registers will not be under reset so user should be able to read/write the lane registers.

This pin goes through a dual-meta synchronizer which is reset by POR reset to default value of 1'b1 which means AFE TX lane pwrdn pin will be asserted while POR is asserted. Minimum assertion time: 25 comclk period.

Digital Data Path Interface Pins

Pin Name	**Direction**	**clock for synchronous signals**	**Description**
pmd_rx_data_***k***[39:0]	Out	pmd_rclk20_***k***	Data (40bits) from the receiver.
pmd_rx_data_vld_***k***	Out	pmd_rclk20_***k***	Receiver data (40bit) valid . The source logic should sample this signal and launch the pmd_rx_data_***k*** at the pmd_rclk20_***k*** rising edge.
pmd_rx_data_1g_***k***[9:0]	Out	pmd_rclk20_***k***	1G OSR modes OS16.5 and OSR20.625 data & AUTONEG/DME data from the receiver.

pmd_rx_data_vld_1g_ ***k***	Out	pmd_rclk20_***k***	1G OSR modes OS16.5 and OSR20.625 receive data valid. Indicates the data on pmd_rx_data_1g_***k*** is valid.
pmd_rclk20_***k***	Out		Receiver data div/20 clock for lane ***k*** .
pmd_tx_data_***k***[39:0]	In	pmd_tclk20_***k***	Data (40bit) to the transmitter. All the 40 bits are valid data bits irrespective of the oversample rate.
pmd_tx_data_vld_***k***	Out	pmd_tclk20_***k***	Transmit data (40bit) valid . The source logic should sample this signal and launch the pmd_tx_data_***k*** at the pmd_tclk20_***k*** rising edge.
pmd_tclk20_***k***	Out		TX data(40bit) clock for lane ***k.*** Data on the pmd_tx_data_***k***[39:0] pins should be launched on the rising edge of this clock.
pmd_pll0_vcoclk4pcs	Out		Transmit clock from pll 0. It can be programmed to 40T, 48T, 64T or OFF (before PI). No specific phase wrt to data or 40T.
pmd_pll1_vcoclk4pcs	Out		Transmit clock from pll 1. It can be programmed to 40T, 48T, 64T or OFF (before PI). No specific phase wrt to data or 40T.
pmd_pll0_vcoclk4pcs_vld	Out		pmd_vcoclk4pcs clock valid from pll 0. This signal is asserted when when the pll is locked and the pmd_pll0_vcoclk4pcs has switched from comclk to vcoclk

pmd_pll1_vcoclk4pcs_vld	Out		pmd_vcoclk4pcs clock valid from pll 1. This signal is asserted when when the pll is locked and the pmd_pll1_vcoclk4pcs has switched from comclk to vcoclk
afe_rx***k***_clk32	Out		Recovered clock, 32T wrt the freq set by the osr_mode[1:0]. It is 50% duty cycle and gated by AFE's rx***k***_reset input. This pin is directly driven from the AFE output clock pin rx***k***_clk32 so refer to AMS for more details.
afe_tx***k***_clk32	Out		PLL + TX PI divide by 32. Duty cycle is 50% and it scales with the VCO freq plus the per lane OS2/4 modes. It is gated by AFE's pll_iddq, pll_pwrdn, pll_reset pins. This pin is directly driven from the AFE output clock pin tx***k***_clk32 so refer to AMS for more details.
pmd_fec_fdbk_diffprec_state_***k***[39:0]	Out	pmd_rclk20_***k***	Differential precoder state. This will be sent with every 40-bit data word.
pmd_fec_fdbk_data_vld_***k***	In	pmd_rclk20_***k***	Valid signal from the PCS to send FEC feedback information to the PMD core.

pmd_fec_fdbk_data_***k***[8:0]	In	pmd_rclk20_***k***	FEC feedback expected data from the PCS to the PMD core. It is three consecutive symbols with the symbol with error as the middle symbol.
pmd_fec_fdbk_pmd_data_***k***[2:0]	In	pmd_rclk20_***k***	PMD receive data which has an error. The corresponding expected receive data is pmd_fec_fdbk_data_***k***[5:3].

TABLE 7 : DIGITAL DATA PATH INTERFACE PINS DESCRIPTION

pmd_plli_vcoclk4pcs (i=0,1)
Transmit clock - always present It can be programmed to 40T, 48T, 64T or OFF (before PI). No specific phase wrt to data or 40T. This should be FLOAT if not used. No specific phase wrt to data or 40T. This clock is gated by pll_iddq, pll_pwrdn, and pll_reset but not tx*_reset.

pmd_plli_vcoclk4pcs_vld (i=0,1)
This signal is asserted when when the pll is locked and the pmd_plli_vcoclk4pcs has switched from comclk to vcoclk. This signal will change state during assertion of resets or power down. This signal is synchronous to comclk.

TX PCS Interface Description:

1. pmd_tclk20_***k***: per lane TX clock. This is the transmit data clock used in PMD core . When pmd_tx_clk_vld_***k*** is asserted then it is derived from VCO clock as per the OSR mode shown in table below otherwise it will be pmd_comclk.

2. pmd_tx_data_vld_***k***: per lane TX data valid/request for pmd_tx_data_***k***[39:0] tx data bus. TX data should be latched by PCS logic on the PCS-PMD TX interface data bus pmd_tx_data_***k***[39:0] at the rising edge of pmd_tclk20_***k*** when pmd_tx_data_vld_***k*** pulse is sampled as 1'b1 by PCS and data should be held until it is latched again on the next pmd_tx_data_vld_***k*** pulse. This signal can be ignored by PCS block in case of 'TX Native Analog Format' as PCS block sends the over-sampled data in this case which is sent to AFE directly.

3. pmd_tx_data_***k***[39:0]: per lane TX 40 bit Egress data bus. Please look at the timing diagram below for timing relationship between pmd_tx_data_vld_***k*** and pmd_tx_data_***k***[39:0]. This data is expected to be launched with rising edge of pmd_tclk20_***k*** when pmd_tx_data_vld_***k*** is sampled to 1'b1. The data is synchronous to the rising edge of pmd_tclk20_***k*** clock. And all the 40 bits should be valid data bits irrespective of the oversampled speed. Bit 0 is the first bit and bit 39 is the last bit transmitted on the serial transmitter output.

Signalling	OSR	pmd_tclk20_k	pmd_tx_data_vld_k
PAM4		VCO/20	Always 1 after lane datapath reset deassertion. Note that if back channel encoder (reg field: bc_enc_en) is enabled then data_vld will be de-asserted for 1 cycle every N clock cycles (Refer to the back channel encoder spec for details) to allow insertion of the 40 bits back channel word/frame.
NRZ	OSR1	VCO/20	Asserted every other clock cycle
NRZ	OSR2	VCO/40	Asserted every other clock cycle
NRZ	OSR4	VCO/80	Asserted every other clock cycle
NRZ	OSR8	VCO/40	Asserted every 8 clock cycles
NRZ	OSR16	VCO/40	Asserted every 16 clock cycles
NRZ	OSR32	VCO/40	Asserted every 32 clock cycles
NRZ	OSR16.5	VCO/20	Asserted every 32 or 34 clock cycles (average 33 clock cycles)
NRZ	OSR20.625	VCO/20	Asserted in a sequence of {40, 42, 40, 42, 42, 40, 42, 42} clock cycles which repeats every 330 clock cycles to provide a valid on average every 330/8=41.25 clock cycles.

Table 8 : Transmit data path

4. PMD also supports a 'Native Analog Format' mode in the TX direction where PCS can oversample the data in NRZ OSR modes (OSR1/2/4/8/16/32/16.5/20.625 and pmd_tx_data_k is sent directly to AFE TX for transmission without any oversampling/bit-replication in the PMD

logic. In that case, pmd_tx_data_vld_***k*** will be driven to 1'b1 for the NRZ OSR modes as well.

In 'Native Analog Format' mode, 40 bits of AFE TX data input pmd_tx_data_***k***[39:0] is expected to be in the format where each oversampled bit is replicated in 2 bit positions (even and next odd bit) in the 40 bit PMD TX data bus. For example, once PCS logic has the 20 bits oversampled data for a given NRZ OSR mode, call it 'nrz_os_data_***k***[19:0]' then on PMD 40 bits input data bus pmd_tx_data_***k***[39:0]', it is assigned as per the below equation.

```
pmd_tx_data_k[2*i]   = nrz_os_data_k[i];  // i = 0 to 19
pmd_tx_data_k[2*i+1] = nrz_os_data_k[i];  // i = 0 to 19
```

5. Figure below shows the timing relationship between the transmit data path interface signals.

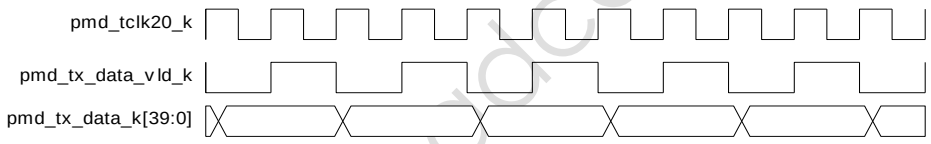


FIGURE 2: TRANSMIT DATA PATH TIMING FOR NRZ OSR1, OSR2, OSR4 MODES

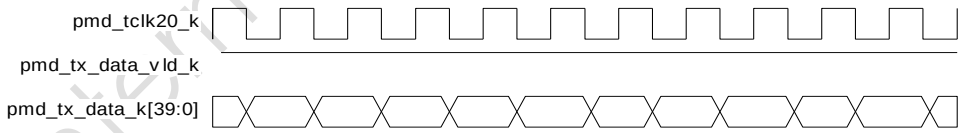


FIGURE 3: TRANSMIT DATA PATH TIMING FOR PAM4 MODE

RX PCS Interface Description:

1. pmd_rclk20_***k***: per lane RX clock. This is the receiver data clock for lane ***k.*** When pmd_rx_clk_vld is asserted, frequency of this clock will always be derived from the VCO clock as per the OSR mode otherwise it will be same as pmd_comclk. Refer to the table below for the clock rate for various OSR modes.

2. pmd_rx_data_***k***[39:0]: per lane RX Ingress data bus from lane ***k*** that is coming from the PMD core to the upper layer logic. It is valid for PAM4 mode, NRZ OSR1, OSR2, OSR4, OSR8, OSR16, and OSR32 modes and over-sampled (bit-replicated) data for 1G OSR modes of OS16.5 and OS20.625 for repeater applications. The data is synchronous to the rising edge of pmd_rclk20_***k*** clock. Data is valid when pmd_rx_data_vld_***k*** = 1 at the rising edge of the pmd_rclk20_***k***. This data bus also provides the over-sampled (bit-replicated) data for 1G OSR modes OS16.5 and OS20.625 for repeater applications. Bit 0 is the earliest bit and bit 39 is the latest bit received on the serial receiver input.

3. pmd_rx_data_vld_***k*** : per lane RX data valid, when 1'b1 then it indicates valid data on pmd_rx_data_***k***[39:0] databus. PCS logic should capture the data on bus pmd_rx_data_***k*** [39:0] at the rising edge of the clock pmd_rclk20_***k*** when pmd_rx_data_vld_***k*** is 1'b1. This signal is launched on the rising edge of the pmd_rclk20_***k.***

Signalling	OSR	pmd_rclk20_k	pmd_rx_data_vld_k
PAM4		VCO/20	Always 1 after lane datapath reset deassertion. Note that if back channel decoder (reg field: bc_dec_en) is disabled then data_vld will be de-asserted for 1 cycle every N clock cycles (Refer to the back channel decoder spec for details) to allow removal of the 40 bits back channel word/frame.
NRZ	OSR1	VCO/20	Asserted every other clock cycle
NRZ	OSR2	VCO/40	Asserted every other clock cycle
NRZ	OSR4	VCO/80	Asserted every other clock cycle
NRZ	OSR8	VCO/40	Asserted every 8 clock cycles
NRZ	OSR16	VCO/40	Asserted every 16 clock cycles
NRZ	OSR32	VCO/40	Asserted every 32 clock cycles

Table 9: Receive data path

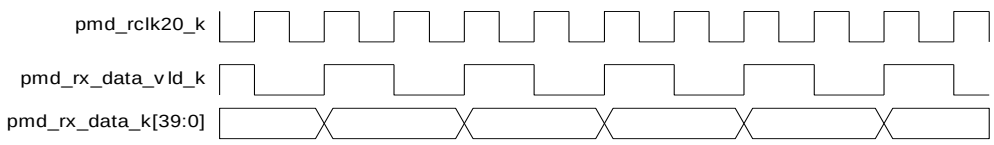


FIGURE 4: RX DATA PATH TIMING FOR NRZ OSR1, OSR2, OSR4 MODES

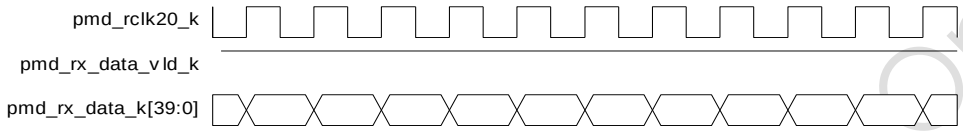


FIGURE 5: RX DATA PATH TIMING FOR PAM4 MODE

4. pmd_rx_data_1g_***k***[9:0]: per lane RX data bus for 1G OSR modes of OSR16.5, and OSR20.625. When pmd_rx_data_vld_1g_***k*** is 1'b1 then it indicates valid data on this bus for PCS logic to latch. For 1G OSR16.5, OSR20.625 modes, 5 even bits are the peaks (i.e. eye center) and 5 odd bits are zeros (i.e. zero crossing) and all the 10 bits are valid in AUTONEG/DME mode but only 5 even bits are valid for 1G PCS data traffic. Bit 0 is the earliest bit and bit 9 is the latest bit received on the serial receiver input. This bus is not applicable for PAM4 mode, NRZ OSR1, OSR2, OSR4, OSR8, OSR16, and OSR 32 modes. Launched with rising edge of pmd_rclk20_***k***.

5. pmd_rx_data_vld_1g_***k*** : per lane RX data valid, when 1'b1 then it indicates valid data on pmd_rx_data_1g_***k***[9:0] databus. PCS logic should capture the data on bus pmd_rx_data_1g_***k*** [9:0] at the rising edge of the clock pmd_rclk20_***k*** when pmd_rx_data_vld_1g_***k*** is 1'b1. This signal is launched on the rising edge of the pmd_rclk20_***k.***

Signalling	OSR	pmd_rclk20_k	pmd_rx_data_vld_1g_k
NRZ	OSR16.5	VCO/20	Asserted on average every 16.5/4 clock cycles
NRZ	OSR20.625	VCO/20	Asserted on average every 20.625/4 clock cycles

Table 10: Receive data path for 1G interface

6. In RX direction, for repeater or low latency applications, PMD also supports a 'RX PCS NRZ Low latency mode' enabled by reg field

tlb_rx_nrz_ll_mode_en. In this mode, PMD provides the oversampled data and replicated data in adjacent ODD/EVEN bits on pmd_rx_data_***k*** in all the NRZ OSR modes (OSR1/2/4/8/16/32 and OSR16.5/20.625) with pmd_rx_data_vld_***k*** driven to 1'b1.

In repeater mode, pmd_rx_data_***k*** can be directly connected to the pmd_tx_data_***k*** to another PMD's TX PCS interface for transmission where TX is programmed in 'native analog format' without any oversampling/bit-replication in the PMD TX logic.

In 'RX PCS NRZ Low latency mode', 40 bits pmd_rx_data_***k*** have following mapping of the 20 bits NRZ OSR modes over-sampled data.

```
pmd_rx_data_k[2*i]   = nrz_os_data_k[i];  // i = 0 to 19
pmd_rx_data_k[2*i+1] = nrz_os_data_k[i];  // i = 0 to 19
```

FEC feedback Interface Description:

Figure 6 shows the timing relationship between pmd_fec_fdbk_data_vld_***k***, pmd_fec_fdbk_data_***k***, and pmd_fec_fdbk_pmd_data_***k*** with respect to pmd_rclk20_***k***. pmd_fec_fdbk_data_k and pmd_fec_fdbk_pmd_data_***k*** are stable until pmd_fec_fdbk_vld_***k*** toggles. In other words, they should be stable for at least 2 pmd_rclk20_***k*** cycles.

FIGURE 6 : FEC FEEDBACK DATA PATH TIMING

Digital Control and Status Pins

Pin Name	Direction	Description
PMD Control		

pmd_rx_pam4_mode_*k*[2:0]	In	PAM4 signalling mode for RX lane *k*. Asynchronous signal to the PMD
pmd_tx_pam4_mode_*k*[2:0]	In	PAM4 signalling mode for TX lane *k*. Asynchronous signal to the PMD
pmd_rx_osr_mode_*k*[3:0]	In	Oversample mode for RX lane *k*. Asynchronous signal to the PMD
pmd_tx_osr_mode_*k*[3:0]	In	Oversample mode for TX lane *k*. Asynchronous signal to the PMD
pmd_tx_disable_*k*	In	Pmd_tx_disable is asserted to squelch the transmit signal for lane *k*.
pmd_ext_los_*k*	In	External Loss of signal. LOS = 1. Signal presence = 0.
pmd_tx_lane_mode_*k*[15:0]	In	Reserved mode bus for tx lane *k*. Mode bus for tx lane k used by the PCS to communicate lane info to PMD firmware. This bus should only be written to when the lane is in reset since the microcode will only read this after coming out of reset. Asynchronous signal to the PMD
pmd_rx_lane_mode_*k*[15:0]	In	Reserved mode bus for rx lane *k*. Mode bus for rx lane k used by the PCS to communicate lane info to PMD firmware. This bus should only be written to when the lane is in reset since the microcode will only read this after coming out of reset. Asynchronous signal to the PMD
pmd_pll0_core_mode [15:0]	In	Reserved mode bus for the core associated with pll0. Mode bus for core used by the PCS to communicate core info to PMD . This bus should only be written to when the core is in reset since the microcode will only read this after coming out of reset. Asynchronous signal to the PMD

pmd_pll1_core_mode [15:0]	In	Reserved mode bus for the core associated with pll1. Mode bus for core used by the PCS to communicate core info to PMD . This bus should only be written to when the core is in reset since the microcode will only read this after coming out of reset. Asynchronous signal to the PMD
PMD Status		
pmd_pll**i**_lock	Out	Assertion of this signal indicates that the pll **i (0 or 1)** has achieved lock. This is an information only status. Not recommended for state-machines, use clk_vld or pmd_lock signals instead.
pmd_rx_lock_***k***	Out	Receive PMD lock for lane ***k***. When this signal is low, the receiver is acquiring lock. During this period the phase of the receive clock and alignment of data are not reliable.
pmd_rx_clk_vld_***k***	Out	Receive clock valid for lane ***k***.
pmd_tx_clk_vld_***k***	Out	Transmit clock valid for lane ***k***.
pmd_signal_detect_***k***	Out	Signal detect status from the analog for lane ***k***. This signal is not related to any interface clock or data validity. This is an information only status. Not recommended for state-machines, use rx_pmd_lock signal instead.
EEE Control		
pmd_tx_mode_***k***[1:0]	In	EEE tx mode function for lane ***k***. Asynchronous signal to the PMD
pmd_rx_mode_***k***	In	EEE rx mode function for lane ***k***. Asynchronous signal to the PMD
EEE Status		
pmd_energy_detect_***k***	Out	EEE energy detect for lane ***k***.
FEC feedback control/status Pins		

pmd_fec_fdbk_status_***k***[15:0]	In	FEC feedback status bus [15:10]: reserved [9]: fec_frame_sync_ll FEC frame synchronization complete has been deasserted since last frc_idx_on_diffprec synchronized to pmd_rclk20 [8]: fec_frame_sync FEC frame synchronization complete synchronized to pmd_rclk20 [7]: corrected_data_valid corrected_data_valid synchronized to pmd_rclk20 [6]: fec_fdbk_idx_lock The interleave index is locked in the FEC feedback [5:0]: fec_fdbk_err_loc[5:0] The error symbol location where the error is found

pmd_fec_fdbk_ctrl_***k***[16:0]	Out	FEC feedback register control bus. [16]: pam4_es_mode PAM4-ES mode [15:14]: rg_fec_fdbk_idx[1:0] interleave index to use when fec_fdbk_monitor_en is set [13]: rg_fec_fdbk_idx_monitor_en 0: FEC feedback error detection for all interleave index 1: FEC feedback error detection for only interleave index set in rg_fec_fdbk_idx [12]: rg_frc_idx_on_diffprec When set, mux interleave index onto diffprec_state[39:0] [11]: rg_fec_fdbk_err_mode FEC feedback error calculation mode: 0: continuous mode 1: only the first error in the FEC frame [10:8]: rg_fec_fdbk_no_err_cnt[2:0] Calculation of the 4/7-level symbol of the error should be followed by a programmable number of cycles that is error free. rg_fec_no_err_cnt[2:0] corresponds to a programmable range of 4->11. [7]: fec_fdbk_sym_bit_swap Bit order for each symbol: 0: {LSB, MSB} 1: {MSB, LSB} [6]: fec_fdbk_dp_invert Invert FEC feedback datapath [5]: fec_fdbk_pam4_precoder_en PAM4 encoder enable [4]: diffprec_state_invert Invert diffprec_state [3]: rx_data_gray_enc_en Enable gray encoding for rx_data[69:0] [2]: fec_data_gray_enc_en Enable gray encoding for corrected_data[69:0] [1]: rg_diffprec_state_gray_en Enable gray encoding for diffprec_state_start [1:0] [0]: rg_fec_fb_processor_en FEC feedback processor enable

Scan Pins		
scanmode	In	Scan Mode pin for DFT. All the scan_* inputs are only applicable when scanmode == 1.
scan_rstb	In	Scan Reset pin for DFT.
scan_en_clk	In	Scan control for the clock gator cell. When scan_en_clk is 1'b1 then all the clock gators instantiated in RTL will be ON. Note that this input is ANDed with scanmode so in functional mode, this signal is driven to 1'b0 internally.
scan_atspeed	In	Scan at-speed control. If 1'b1 then AFE clocks (from PLL) will be selected as scan clock for RX and TX lane clocks. This has higher priority than scan_rclk_ctl_***k*** and scan_tclk_ctl**.**
scan_rclk20_***k***	In	Scan clock for RX lane ***k***
scan_rclk20_ctl_***k***	In	Scan clock control for RX lane ***k*****.** scan_rclk_ctl_***k***== 1'b1 will select scan_rclk_***k*** as scan clock for RX Lane ***k*** otherwise pmd_comclk will be selected.
scan_rclk20_***k***	In	Scan clock for RX divide by 20 clock lane ***k***
scan_rclk20_ctl_***k***	In	Scan clock control for RX divide by 20 clock lane ***k*****.** scan_rclk_ctl_***k***== 1'b1 will select scan_rclk_***k*** as scan clock for RX Lane ***k*** otherwise pmd_comclk will be selected.
scan_plli_vcoclk4pcs	In	Scan clock for vco clk for pll **I (i=0 or1)**
scan_plli_vcoclk4pcs_ctl	In	Scan clock control for vco clk pll **I (i= 0 or 1)**
scan_tclk20_***k***	In	Scan clock for TX
scan_tclk20_ctl_***k***	In	Scan clock control for TX scan_tclk20_ctl_***k*** == 1'b1 will select scan_tclk20_***k*** as scan clock otherwise pmd_comclk will be selected.
scan_plli_refclk	In	Scan clock for refclk for pll **i (i = 0 or 1)**.

scan_pll**i**_refclk_ctl	In	Scan clock control for refclk for pll **i (I = 0 or 1)** scan_pll0_refclk_ctl == 1'b1 will select scan_pll0_refclk as scan clock otherwise pmd_comclk will be selected. scan_pll1_refclk_ctl == 1'b1 will select scan_pll1_refclk as scan clock otherwise pmd_comclk will be selected.
scan_pll**i**_fdbck_clk	In	Scan clock for fdbck clock for pll **i (i = 0 or 1)**
scan_pll**i**_fdbck_clk_ctl	In	Scan clock control for fdbck_clk for pll **i (i = 0 or 1)** scan_pll0_fdbck_clk_ctl == 1'b1 will select scan_pll0_fdbck_clk as scan clock otherwise pmd_comclk will be selected. scan_pll1_fdbck_clk_ctl == 1'b1 will select scan_pll1_fdbck_clk as scan clock otherwise pmd_comclk will be selected.
Management Signal		
pmd_mdio_trans	In	MDIO transaction indicator needs to be asserted in a configuration where an external mdio controller is trying to access the internal PMD registers directly.

TABLE 11: DIGITAL CONTROL AND STATUS PINS

pmd_rx_pam4_mode_*k*[2:0]/ pmd_tx_pam4_mode_*k*[2:0]

PAM4 signalling mode for lane k. Asynchronous signal to the PMD.

pam4 Mode	Value
NRZ	3'd0
PAM4	3'd1
reserved	3'd2 – 3'd7

TABLE 12: PAM4 SIGNALLING MODE

pmd_rx_osr_mode_*k*[3:0]/ pmd_tx_osr_mode_*k*[3:0]

Oversample mode for lane ***k***. Asynchronous signal to the PMD. OSR mode has to be programmed to OSRx1 (4'd0) for PAM4 mode.

OSR Mode	Value
OSRx1	4'd0
OSRx2	4'd1
OSRx4	4'd2
OSRx8	4'd5
OSRx16	4'd9
OSRx32	4'd13
OSRx16P5	4'd8
OSRx20P625	4'd12

TABLE 13: OSR MODE

pmd_tx_disable_*k*

Assertion of this signal will disable the transmitter's output, putting both analog outputs at common mode voltage (~0mV differential). This signal is treated as asynchronous. It is expected to be used during Clause 73 auto negotiation transmit disable state.

pmd_ext_los_*k*

External Loss of signal. LOS = 1 when signal is absent. pmd_ext_los is treated as asynchronous signal. This pin is expected to be connected to external modules' optical LOS.

pmd_tx_lane_mode_*k*[15:0]

Reserved mode bus for tx lane k. Mode bus for tx lane k used by the PCS to communicate lane info to PMD. This bus should only be written to when the tx lane is in reset since the microcode will only read this after coming out of reset. This signal will be latched to a lane based register during core_dp_rstb.

Asynchronous signal to the PMD. Data is presented in status registers such that microcontroller can read lane mode mode information from system.

pmd_rx_lane_mode_*k*[15:0]

Reserved mode bus for rx lane k. Mode bus for rx lane k used by the PCS to communicate lane info to PMD. This bus should only be written to when the rx lane is in reset since the microcode will only read this after coming out of reset. This signal will be latched to a lane based register during core_dp_rstb. Asynchronous signal to the PMD. Data is presented in status registers such that microcontroller can read lane mode mode information from system.

pmd_plli_core_mode[15:0]

Reserved mode bus for core associated with pll i (i = 0 or 1). Mode bus for core used by the PCS to communicate core info to PMD . This bus should only be written to when the core is in reset since the microcode will only read this after coming out of reset. This signal will be latched to a lane based register during core_dp_rstb. Asynchronous signal to the PMD. Data is presented in status registers such that microcontroller can read core mode information from system.

pmd_rx_lock_*k*

When this signal is low, the receiver is acquiring lock. During this period the phase of the receive clock and alignment of data are not reliable. All decode functions in the PCS or higher level logic should wait for the assertion of this signal. Synchronous to pmd_rclk20_k.

pmd_rx_clk_vld_*k*

This signal is asserted when rclk20 is at the VCO clock/20 rate and the data valid generation logic is stable. This signal will change state during assertion of resets or power down. This signal is synchronous to comclk.

pmd_tx_clk_vld_*k*

This signal is asserted when tclk20 is at the VCO clock/20 rate and the data valid generation logic is stable. This signal will change state during assertion of resets or power down. This signal is synchronous to comclk.

pmd_tx_mode_*k*[1:0]

This primitive is generated by the PCS Transmit Process when EEE is supported to indicate that the PMA and PMD transmit functions may go into a low power mode and to disable the PMD transmitter. See subclause 72.6.5. When EEE is not supported, the primitive is never invoked and the PMD behaves as if tx_mode =

DATA. The tx_mode parameter takes on one of three values: QUIET, ALERT, or DATA.

2'b00 – DATA

2'b01 – QUIET

2'b10 - ALERT

Note: These are placeholders for future EEE support. They should be tied to 2'b00.

pmd_rx_mode_*k*

The PCS Receive Process generates this primitive when EEE is supported to indicate that the input signal is quiet and the PMA and PMD receiver may go into a low power mode. When EEE is not supported, the primitive is never invoked and the PMD behaves as if rx_mode = DATA. The rx_mode parameter takes on one of two values: QUIET or DATA.

1'b0 – DATA

1'b1 - QUIET

Note: These are placeholders for future EEE support. They should be tied to 1'b0.

pmd_energy_detect_*k*

During Energy-Efficient Ethernet (EEE) mode energy_detect indicates whether the PMD sublayer has detected a signal at the receiver. This is defined by the IEEE 802.3 in context of Clause 93/72 PMD. This signal is synchronous to comclk.

scanmode

Scan Mode pin for DFT. All the scan_* inputs are only applicable when scanmode == 1.

scan_rstb

Scan Reset pin for DFT.

scan_en_clk

Scan control for the clock gator cell. When scan_en_clk is 1'b1 then all the clock gators instantiated in RTL will be ON. Note that this input is ANDed with scanmode so in functional mode, this signal is driven to 1'b0 internally and any functional clock gating controls with control the clock gator cells.

scan_atspeed
Scan at-speed control. If 1'b1 then AFE clocks (from PLL) will be selected as scan clock for RX and TX lane clocks. This has higher priority than scan_rclk20_ctl_***k*** and scan_tclk20_ctl**.**

scan_rclk20_*k*
At speed Scan clock for RX lane ***k***

scan_rclk20_ctl_*k*
Scan clock control for RX lane ***k*****.** scan_rclk20_ctl_***k*** == 1'b1 will select scan_rclk20_***k*** as scan clock for RX Lane ***k*** otherwise pmd_comclk will be selected.

scan_tclk20_*k*
At speed Scan clock for TX

scan_tclk20_ctl_*k*
Scan clock control for TX lane ***k*****.** scan_tclk20_ctl == 1'b1 will select scan_tclk20 as scan clock for TX otherwise pmd_comclk will be selected.

pmd_mdio_trans
MDIO transaction indicator needs to be asserted in a configuration where an external mdio controller is trying to access the internal PMD registers through the pmi_lp port. This signal holds off internal clock switching resulting from going into or out of lane reset that might cause up to 3 additional clock cycles in getting the data back for an mdio read transaction. This signal needs to be asserted 2 mdio clock cycles before asserting pmi_lp_en and should be deasserted when the pmi_lp_ack is returned.

Parallel Management Interface Pins

Blackhawk core provides a parallel management interfaces, pmi_lp and this is primarily for chip level management interface. This interface can be used for accessing the registers space. There are also internal pmi buses tied to the ARM M0+ micro cores that can also access the internal registers. A transaction request through the external pmi_lp bus and from the internal micro for a register

bank in the same lane and same clock domain at the exact same clock, then micro transaction will go through first and then the LP will be serviced in the next clock.

The pmi_lp port also has a 16-bit maskdata bus along with the 16-bit wrdata bus to mask bits for a write transaction to avoid doing a software based read-modify write which is very costly for the microprocessor. The maskdata bus is 0 for no mask and 1 for mask operation where the wrdata bit is ignored for that bit. The maskdata bus is driven by the bus master along with the addr and wrdata buses. The maskdata can be all 0 for no mask operation where all bits are written to the register. The micro subsystem clears the maskdata bus at the end of each transaction. A masked write operation can also be used with broadcast or multicast writes to multiple lanes.

For more details, please refer to the RMIC micro architectural document.

Low Priority Parallel Management Interface

PIN	DIRECTION (from MIC)	DESCRIPTION
pmi_lp_addr[31:0]	In	32-bit address driven by master for read or write transaction. This should be asserted before or with the pmi_lp_en and should be driven until the next transaction.
pmi_lp_wrdata[15:0]	In	16-bit data bus driven by master for write transaction. This should be driven before or with the pmi_lp_en and should be driven until the next transaction.
pmi_lp_maskdata[15:0]	In	16-bit mask bus driven by master for write transaction. 0 means no mask (wrdata bit is written to register), 1 means mask (wrdata bit is ignored). This bus has no affect during a read operation. This should be asserted before or with the pmi_lp_en and should be driven until the next transaction.
pmi_lp_write	In	Read/Write control from master. 1-write, 0-read. This should be asserted before or with the pmi_lp_en and should be driven until the next transaction.
pmi_lp_en	In	Transaction enable control from master. This is treated as asynchronous to the rmic. The bus master should wait for pmi_lp_ack to be deasserted before pmi_lp_en is asserted. The bus master should then wait for pmi_lp_ack to be asserted indicating that the transaction is complete before it deasserts pmi_lp_en.

pmi_lp_ack	Out	Ack response back from the RMIC slave indicating that the write or read transaction is complete. This signal is driven in the registers blocks clock domain and should be treated as an asynchronous input by the master.
pmi_lp_read_vld	Out	This signal indicates that the read data is available for a read operation. This can be asserted before the pmi_lp_ack and the bus master can take advantage of this signal for read transactions. This signal will be asserted for both read and write transactions but is only used for read transactions.
pmi_lp_error	Out	Error response from RMIC slave indicating an address error which means that either the block address does not exist or that the devid did not match the strap value. The ack signal indicates that the transaction is complete and the error signal indicates that there was an address error with this transaction. This signal is asserted along with the ack signal and should be treated an asynchronous signal the same way as the ack signal.
pmi_lp_rddata[15:0]	Out	16-bit data bus driven RMIC slave during a read transaction. This data is latched in the register clock domain but this data is guaranteed to be stable by the end of the read transaction so this does not have to metastabilized.

TABLE 14: LOW PRIORITY PARALLEL MANAGEMENT INTERFACE PINS

More details regarding the low priority PMI bus interface is available in the functional description section of this document. Figure below shows the timing relationship between the PMI lp signals during a write transaction.

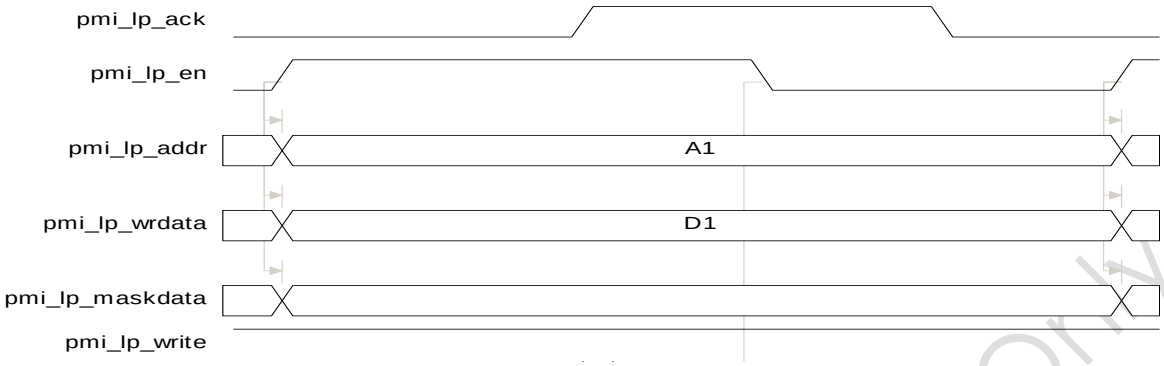


FIGURE 7: PMI LP WRITE TRANSACTION.

Figure below shows the timing relationship between the PMI signals during a read transaction.

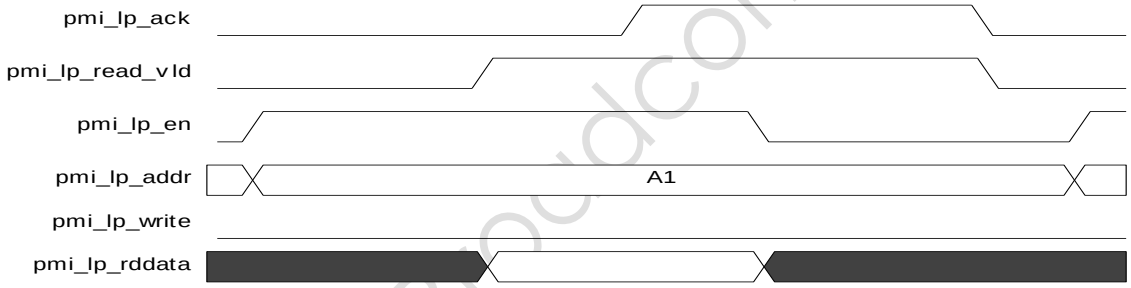


FIGURE 8: PMI_LP READ TRANSACTION.

Microcontroller Memory Interface

PIN	DIRECTION (W.R.T RMIC)	DESCRIPTION
pram_clk	In	Program RAM clock. Same or lower frequency than micro_clk/comclk
pram_cs	In	Program RAM chip select
pram_datain[7:0]	In	Program RAM write data
ovstb	In	Over voltage stress test signal; goes to memories

otp_enable_mrdten_inversion	In	Test mode pin for memory
otp_mlvm_control	In	Memory test pin connected to mlvm input of all memories
otp_lvm_control	In	Memory test pin connected to lvm input of all memories
pmd_micro_ext_intr	Out	external interrupt to external microcontroller. Includes ECC Errors

TABLE 15: MICROCONTROLLER MEMORY INTERFACE

Please refer to microcontroller_subsystem documentation for more details.

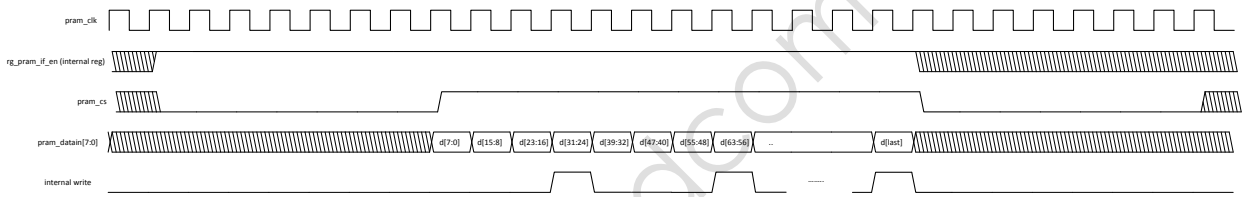


FIGURE 9: PRAM INTERFACE TIMING

Microcontroller Debugger Interface

PIN	DIRECTION (W.R.T RMIC)	DESCRIPTION
swclktck	In	ARM Micro Serial Wire Debugger Clock. Connects to input pad for SWCLK/TCK
swditms	In	ARM Micro Serial Wire Debugger Data In. Connects to tristate pad for SWDIO
swdo	Out	ARM Micro Serial Wire Debugger Data output . Connects to tristate pad for SWDIO
swdoen	Out	ARM Micro Serial Wire Debugger Data output pad control. Connects to tristate

		pad for SWDIO
swdetect	Out	ARM Micro Serial Wire protocol detect. Can be used to disable JTAG if swclktck input pad is shared.

TABLE 16: MICROCONTROLLER DEBUGGER INTERFACE

Management Port: MDIO

Pin Name	Direction	Description
mdio_clk	In	MDIO clock. Max frequency is 25MHz
mdio_in	In	Serial input
mdio_out	Out	Serial output
mdio_oeb	Out	Active low output enable going to tristate output driver for bidirectional mdio pin

TABLE 17: MANAGEMENT MDIO PIN DESCRIPTION

Please refer to IEEE 802.3 Clause 45 for the timing details. For more detailed MDIO features, refer to the MDIO architectural document.

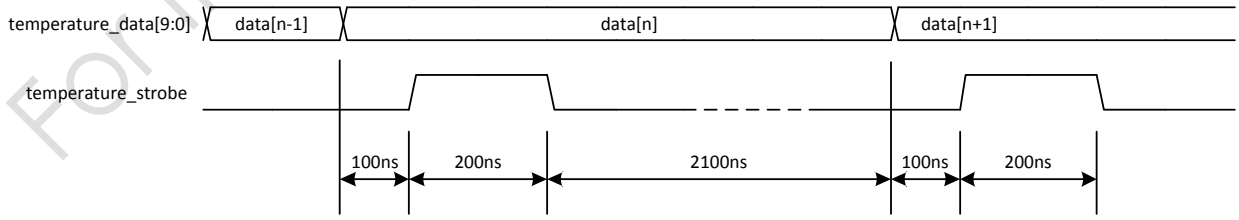


FIGURE 10: TEMPERATURE SENSOR INTERFACE

Temperature data provided should be accurate to within 5degC of the die temperature of the AFE circuit. Temperature data is used for Clause 93/72 to calculate how much TXEQ to request to ensure future temperature change can be handled by the receiver. Temperature based compensation is being performed for VCO calibration and we are looking into other places where it can be used to reduce temperature variation effects.

The number of temperature sensors per Blackhawk core that can be achieved within the desired accuracy depends on chip layout and temperature variation across the die. Packaging team has provided thermal time constants as 100-500ms for large die and may play a role in the assessment.

The temperature value may be overridden via register access. Temperature is queried periodically (~5-10ms) by SerDes microcode and a software based update needs to be done often enough for temperature accuracy.

Programmers Sequence

The Programming Sequence provides instruction on how to program the Blackhawk core is covered in the following IP release document:

TBD

Functional Description

Blackhawk core is the 56.25Gbps Serdes IO designed for 16nm TSMC process. This core will support speeds of 1.25Gbps to 56.25Gbps. The core also supports MDIO management interface, Arm M0+ micro subsystem and IEEE 802.3 Clause 93/72 De-emphasis training.

Blackhawk Architecture

The 16nm Blackhawk core design has enhanced data path architecture, simplified clocking structure, new register organization and improved RTL hierarchy. Blackhawk core is architected for low latency, power and area. There is a parallel management interfaces pmi_lp available for accessing the core register interface. Apart from this pmi_lp port, the MDIO offers an IEEE 802.3 Clause 45 protocol based serial interface. The core supports up to 25MHz serial clock rate. Blackhawk core supports low power modes and transmit disable to lower the power statically.

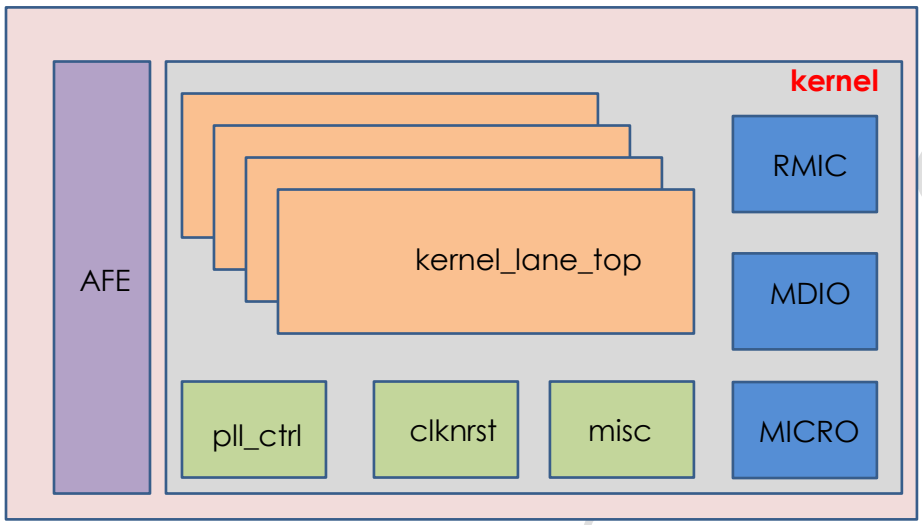
The core is partitioned into analog front end, digital signal conditioning, test-loopbacks, PLL calibration logic and register management interface controller. The analog hard macro consists of the high speed receiver, transmitter and the 2 PLLs. Digital signal conditioning logic performance clock and data recovery, the receive equalization and other adaptive loops that improves the performance in different speed modes. PRBS generation, checking, pattern generation are the support testing features. The core also has a remote loopback to loop the received data through the transmitter and a digital loopback to loop the system side transmit data through the receive data path, just before the analog interface.

Several aspects in the Blackhawk Series are different from the previous generation SerDes cores. The key differences are listed below:

- The core is designed to be as much as protocol agnostic as possible.
- Simplified clocking architecture. The core contains only 2n+m+1 register clock domains. (n = number of lanes)(m=number of PLLs).
- Simplified register address map. All the PMA/PMD addresses are in the vendor specific space. The base PMD does not support any standards based registers (IEEE or OIF).

- IEEE 802.3 CL93/72 base transmit de-emphasis training. This module comes with IEEE registers associated with CL93/72 functionality.
- A digital data path interface that is consistent across the oversample rates.
- Area efficient remote and digital loopback data paths.
- RDB based register documentation.
- Integrated quad Arm M0 Micro subsystem.

The following top level block diagram shows the main functional blocks of the core and how they are organized.



Blackhawk Speed Modes

Blackhawk core is targeted for line speed from 1.0 Gbps to 56.25 Gbps. Through over sampled modes and mode selection between NRZ and PAM4, the user has a choice to select lines speeds anywhere from 1.0 Gbps to 56.25 Gbps. The core supports 1/2/4/8/16/32/16.5/20.625 oversampled rates achieve all these line speeds.

The following table shows all the data rates supported and the various refclk and OSR modes required to support these data rate. The rates highlighted in yellow are the supported rates for Blackhawk.

Blackhawk User Specification

Refclk (MHz)	Div	Mode	VCO RATE (GHz)	PAM4 (Gbps)	NRZ (Gbps)							
					OSx1	OSx2	OSx4	OSx16P5	OSx20P625	OSx8	OSx16	OSx32
156.25	96	Integer-N	15	30	15	7.5	3.75	0.90909	0.72727273	1.875	0.9375	0.4688
156.25	120	Integer-N	18.75	37.5	18.75	9.375	4.69	1.13636	0.90909091	2.34375	1.1719	0.5859
156.25	127.4	Frac-N	19.907	39.813	19.907	9.953	4.98	1.20646	0.96516655	2.48832	1.2442	0.6221
156.25	128	Integer-N	20	40	20	10	5	1.21212	0.96969697	2.5	1.25	0.625
156.25	132	Integer-N	20.625	41.25	20.625	10.31	5.16	1.25	1	2.57813	1.2891	0.6445
156.25	140	Integer-N	21.875	43.75	21.875	10.94	5.47	1.32576	1.06060606	2.73438	1.3672	0.6836
156.25	147.2	Frac-N	23	46	23	11.5	5.75	1.39394	1.11515152	2.875	1.4375	0.7188
156.25	158.4	Frac-N	24.75	49.5	24.75	12.38	6.19	1.5	1.2	3.09375	1.5469	0.7734
156.25	160	Integer-N	25	50	25	12.5	6.25	1.51515	1.21212121	3.125	1.5625	0.7813
156.25	165	Integer-N	25.781	51.563	25.781	12.89	6.45	1.5625	1.25	3.22266	1.6113	0.8057
156.25	168	Integer-N	26.25	52.5	26.25	13.13	6.56	1.59091	1.27272727	3.28125	1.6406	0.8203
156.25	170	Integer-N	26.563	53.125	26.563	13.28	6.64	1.60985	1.28787879	3.32031	1.6602	0.8301
156.25	175	Integer-N	27.344	54.688	27.344	13.67	6.84	1.6572	1.32575758	3.41797	1.709	0.8545
156.25	179	Frac-N	27.969	55.938	27.969	13.98	6.99	1.69508	1.35606061	3.49609	1.748	0.874
156.25	179.2	Frac-N	28	56	28	14	7	1.69697	1.35757576	3.5	1.75	0.875
156.25	180	Integer-N	28.125	56.25	28.125	14.06	7.03	1.70455	1.36363636	3.51563	1.7578	0.8789
125	120	Integer-N	15	30	15	7.5	3.75	0.90909	0.72727273	1.875	0.9375	0.4688
125	165	Integer-N	20.625	41.25	20.625	10.31	5.16	1.25	1	2.57813	1.2891	0.6445
125	175	Integer-N	21.875	43.75	21.875	10.94	5.47	1.32576	1.06060606	2.73438	1.3672	0.6836
125	180	Integer-N	22.5	45	22.5	11.25	5.63	1.36364	1.09090909	2.8125	1.4063	0.7031
125	184	Integer-N	23	46	23	11.5	5.75	1.39394	1.11515152	2.875	1.4375	0.7188
125	198	Integer-N	24.75	49.5	24.75	12.38	6.19	1.5	1.2	3.09375	1.5469	0.7734
125	200	Integer-N	25	50	25	12.5	6.25	1.51515	1.21212121	3.125	1.5625	0.7813
125	224	Integer-	28	56	28	14	7	1.69697	1.35757576	3.5	1.75	0.875

		N										
161.133	128	Integer-N	20.625	41.25	20.625	10.31	5.16	1.25	1	2.57813	1.2891	0.6445
161.133	160	Integer-N	25.781	51.563	25.781	12.89	6.45	1.5625	1.25	3.22266	1.6113	0.8057
106.25	264	Integer-N	28.05	56.1	28.05	14.03	7.01	1.7	1.36	3.50625	1.7531	0.8766
106.25	160	Integer-N	17	34	17	8.5	4.25	1.0303	0.82424242	2.125	1.0625	0.5313
312.5	73.6	Frac-N	23	46	23	11.5	5.75	1.39394	1.11515152	2.875	1.4375	0.7188
312.5	79.2	Frac-N	24.75	49.5	24.75	12.38	6.19	1.5	1.2	3.09375	1.5469	0.7734
312.5	80	Integer-N	25	50	25	12.5	6.25	1.51515	1.21212121	3.125	1.5625	0.7813
312.5	82.5	Frac-N	25.781	51.563	25.781	12.89	6.45	1.5625	1.25	3.22266	1.6113	0.8057
312.5	84	Frac-N	26.25	52.5	26.25	13.13	6.56	1.59091	1.27272727	3.28125	1.6406	0.8203
312.5	85	Frac-N	26.563	53.125	26.563	13.28	6.64	1.60985	1.28787879	3.32031	1.6602	0.8301
312.5	87.5	Frac-N	27.344	54.688	27.344	13.67	6.84	1.6572	1.32575758	3.41797	1.709	0.8545
312.5	89.6	Frac-N	28	56	28	14	7	1.69697	1.35757576	3.5	1.75	0.875
312.5	90	Frac-N	28.125	56.25	28.125	14.06	7.03	1.70455	1.36363636	3.51563	1.7578	0.8789
212.5	80	Integer-N	17	34	17	8.5	4.25	1.0303	0.82424242	2.125	1.0625	0.5313
212.5	132	Integer-N	28.05	56.1	28.05	14.03	7.01	1.7	1.36	3.50625	1.7531	0.8766
174.703	160	Integer-N	27.953	55.905	27.953	13.98	6.99	1.69409	1.35527273	3.49406	1.747	0.8735
158.51	140	Integer-N	22.191	44.383	22.191	11.1	5.55	1.34493	1.07594667	2.77393	1.387	0.6935
173.37	128	Integer-N	22.191	44.383	22.191	11.1	5.55	1.34493	1.07594473	2.77392	1.387	0.6935
157.844	140	Integer-N	22.098	44.196	22.098	11.05	5.52	1.33928	1.07142594	2.76227	1.3811	0.6906
172.64	128	Integer-N	22.098	44.196	22.098	11.05	5.52	1.33927	1.0714143	2.76224	1.3811	0.6906
156.637	140	Integer-N	21.929	43.858	21.929	10.96	5.48	1.32904	1.06323297	2.74115	1.3706	0.6853
168.04	128	Integer-N	21.509	43.018	21.509	10.75	5.38	1.30358	1.04286642	2.68864	1.3443	0.6722
159.375	132	Integer-N	21.038	42.075	21.038	10.52	5.26	1.275	1.02	2.62969	1.3148	0.6574
100	240	Frac-N	24	48	24	12	6	1.45455	1.16363636	3	1.5	0.75
100	280	Frac-N	28	56	28	14	7	1.69697	1.35757576	3.5	1.75	0.875
122.88	160	Integer-N	19.661	39.322	19.661	9.83	4.92	1.19156	0.95325091	2.4576	1.2288	0.6144
122.88	165	Integer-N	20.275	40.55	20.275	10.14	5.07	1.2288	0.98304	2.5344	1.2672	0.6336
122.88	198	Integer-N	24.33	48.66	24.33	12.17	6.08	1.47456	1.179648	3.04128	1.5206	0.7603
122.88	200	Integer-N	24.576	49.152	24.576	12.29	6.14	1.48945	1.19156364	3.072	1.536	0.768

122.88	206.25	Frac-N	25.344	50.688	25.344	12.67	6.34	1.536	1.2288	3.168	1.584	0.792
155.52	128	Integer-N	19.907	39.813	19.907	9.953	4.98	1.20646	0.96516655	2.48832	1.2442	0.6221
155.52	144	Integer-N	22.395	44.79	22.395	11.2	5.6	1.35727	1.08581236	2.79936	1.3997	0.6998
155.52	165	Integer-N	25.661	51.322	25.661	12.83	6.42	1.5552	1.24416	3.2076	1.6038	0.8019
166.67	100	Frac-N	16.667	33.334	16.667	8.334	4.17	1.01012	0.80809697	2.08338	1.0417	0.5208
166.67	120	Integer-N	20	40.001	20	10	5	1.21215	0.96971636	2.50005	1.25	0.625
166.67	160	Integer-N	26.667	53.334	26.667	13.33	6.67	1.61619	1.29295515	3.3334	1.6667	0.8334

Blackhawk Programmers model

TBD

Blackhawk test and loopback

Blackhawk TLB (test and loopback) module supports various test and loopback functions that includes following features. All the functions are per lane basis unless stated otherwise.

TLB_TX features:

- PRBS Generator for all OSR modes
- Pattern Generator for all OSR modes
- PAM4 Fixed pattern generator modes
- PMD TX data invert
- Remote Loopback using Phase Detector for all OSR modes
- TX Datapath Mux
- Oversample modes where each transmitted bits are repeated (N times) based on the OSRxN mode.
- Bit transmission order is LSB bit first and MSB bit last on the parallel data to the Kernel/AFE.
- Low latency TX data path for TX PCS data in Native Analog Format.
- Differential Encoder for TX PCS datapath for OSR1/2/4 modes.

TLB_RX features:

- PMD RX data invert
- Digital Loopback using Phase Detector for all OSR modes.
- PRBS Checker for all OSR modes.
- Remote Loopback mux for 1G OSR modes and OSR1/2/4.
- Bit receive order is assumed to be LSB bit first and MSB bit last on the parallel data bus from the Kernel/AFE.
- Differential decoder for RX PCS datapath for OSR1/2/4 modes.
- PRBS checker auto-detect mode.
- PRBS Error Anayzer.

TLB_RX and TLB_TX modules supports test and loopback functions of the PMD core which are debug/test capabilities of the core like loopbacks, PRBS/pattern generators and PRBS checkers, RX/TX data path invert etc. Various features are described below.

PRBS Generator and Pattern Generator:

Following are the description of the features, design assumptions and register configuration controls which will be supported:

1. PRBS Generation capability for PRBS 7, 9, 10, 11, 13, 15, 20, 23, 31, 49, 58 and QPRBS13 which is the polynomial used by the 66B/64B PCS scrambler. Following are the list of all the PRBS polynomials supported by the PRBS generator.

   $1+x^{6}+x^{7}$ (CL 48.2.4 PRBS7)

   $1+x^{5}+x^{9}$ (CL 68.6.1 PRBS9)

   $1+x^{9}+x^{11}$ (CL 72.6.10 PRBS11)

   $1+x^1+x^2+x^{12}+x^{13}$ (CEI-56G PRBS13)

   $1+x^1+x^2+x^{12}+x^{13}$ (CEI-56G QPRBS13 for PAM4 mode: invert 8191 bits From PRBS13 after every 8191 bits)

   $1+x^{14}+x^{15}$ (PRBS15)

   $1+x^{18}+x^{23}$ (PRBS23)

   $1+x^{28}+x^{31}$ (CL 49.2.8 PRBS31)

   $1+x^{39}+x^{58}$ (CL 49.2.6 PRBS58 is also used by the PCS scrambler)

   $1+x^{3}+x^{20}$ (FC PRBS20)

   $1+x^{7}+x^{10}$ (FC PRBS10)

   $1+x^{40}+x^{49}$ (PRBS49)

2. Single bit error generation capability in the PRBS generator where MSB bit 39 of the PRBS data bus will be inverted/flipped to create a single bit error upon toggling of the control register bit **prbs_gen_err_ins** from 0 to 1.

3. Fixed pattern generation capability. IEEE 8x1s+8x0s square wave signal generation is the default pattern. There is a 240 bit fixed pattern sequence which will be shared between all the lanes. Each lane can chose from 20 bit to 240 bit pattern in increments of 20 bit chunks by programming the start and stop index of the 20 bit chunks. It is user's responsibility to make sure they program **patt_gen_start_pos[3:0] and patt_gen_stop_pos[3:0]**

registers correctly for each lane based on the requirement. By default, same 240 bit pattern will be generated on all the lanes.

There is also new PAM4 fixed test patterns for the PAM4 modes which includes PAM4 fixed patterns of **JP03A**, **JP03B** and **Transmitter Linearity Test Pattern**. Refer to the register html for details about enabling these new modes.

4. PRBS invert. Inverts all the data bits when **prbs_gen_inv** control register is set to 1'b1. This is applicable to all the PRBS gen modes.

5. Assuming 20 symbols/40 bits wide data bus with worst case freq around 28.125 Ghz/20 = ~1.4 Ghz.

6. Assuming that LSB bit 0 of the output data bus [39:0] will be transmitted first. Note that in case of fixed pattern mode, MSB bit of the fixed pattern sequence will be transmitted. There is a bus reverse function right at the output data bus to reverse the data bus so that LSB bit 0 is the first transmitted bit otherwise inside the PRBS / Pattern generator module, it is assumed that MSB bit 39 will be transmitted first.

7. All the PRBS modes will use an **initial PRBS seed** of {1b'1, lane_id[4:0],1'b1} which can support different seed for up to 32 lanes. Initial PRBS Seed value is loaded at reset or when PRBS Gen Enable bit is 1'b0.

PRBS Checker:
Following PRBS Checker/Monitor features will be supported :

1. PRBS Checker Polynomials supported are same as the PRBS generator.

2. PRBS Checker Invert: Invert all the received PRBS data bits if register **prbs_chk_inv** is 1'b1.

3. **PRBS LOCK/SYNC detection**: Once PRBS checker is enabled and if the PRBS data is received consistently without any error for M consecutive clock cycles (default: 3) defined by the register **prbs_chk_lock_cnt [4:0]** then PRBS_LOCK status indication will be asserted to 1'b1 and error counter will start counting bit errors in case of errors. Once in LOCKED state, if PRBS data is received continuously with 1 or more bit errors for N clock cycles (default: 7) defined by the register **prbs_chk_lol_cnt [4:0]** then

PRBS LOCK will be de-asserted to 1'b0 indicating that PRBS_LOCK is lost. There are 2 PRBS_LOCK related status registers:

- **PRBS_LOCK** – indicates the live status of the PRBS LOCK indication.

- **PRBS_LOCK_LOST_LH** - Indicates latched HIGH status of the PRBS Lost condition. Captures the 1->0 transition of the live PRBS_LOCK indication since the last read of this register. This is a clear on read register and it is concatenated with the 15 bits of the MSB error counter register and reported in single address.

PRBS_LOCK_LOST_LH status bit also indicate other PRBS checker states as below.

- PRBS Checker is currently not enabled | |
- PRBS Checker is currently not locked | |
- PRBS_LOCK was lost when checker was enabled since the last read

Reset default for **PRBS_LOCK_LOST_LH** register is 1'b1.

There are following 3 modes supported for PRBS LOCK detection.

1. **Self-sync Mode (w/ hysteresis) :** In this PRBS checker mode, once PRBS checker is enabled and enough data is received (80 bits for PRBS 58 and 40 bits for all other PRBS modes) then expected data is calculated from the previous received data bits based on the PRBS polynomial configuration and then expected data is compared with the next received data and any mismatch is counted as a bit error.

Once PRBS checker is enabled, if the received data has no bit errors for M consecutive clock cycles (default: 3) defined by the register **prbs_chk_lock_cnt [4:0]** then PRBS_LOCK is asserted to 1'b1 and it stays locked until there are N consecutive clock cycles (default: 7) defined by the register **prbs_chk_lol_cnt [4:0]** with 1 or more bit errors which makes the PRBS_LOCK to get de-asserted to 1'b0. PRBS_LOCK is also de-asserted as soon as PRBS checker is disabled.

Error Counter starts counting PRBS bit errors after 2 clock cycles (for PRBS 58) and 1 clock cycle (for all other than PRBS polynomial) of the assertion of PRBS Checker Enable irrespective of the status of the PRBS_LOCK.

2. **Locked Mode (w/ hysteresis):** In this PRBS checker mode, once PRBS checker is enabled, PRBS shift register flops are loaded with the

received data until PRBS is locked and once PRBS is locked, shift registers are loaded with next seed data which is calculated from the current shift register values based on the selected PRBS polynomial. Once PRBS is locked, then calculated next seed data is compared with the next received data and any mismatch is counted as a bit error.

Once PRBS checker is enabled, if the received data has no bit errors for M consecutive clock cycles (default: 3) defined by the register **prbs_chk_lock_cnt [4:0]** then PRBS_LOCK is asserted to 1'b1 and it stays locked until there are N consecutive clock cycles (default: 7) defined by the register **prbs_chk_lol_cnt [4:0]** with 1 or more bit errors which makes the PRBS_LOCK to get de-asserted to 1'b0. PRBS_LOCK is also de-asserted as soon as PRBS checker is disabled.

Error Counter only counts PRBS bit errors during the time PRBS_LOCK is asserted to 1'b1.

3. **Locked Mode (w/o hysteresis):** This mode is similar to the **Locked Mode (w/ hysteresis)** except that once LOCKED, it does not go out of lock irrespective of PRBS bit errors until PRBS Checker is disabled.

Error Counter only counts PRBS bit errors during the time PRBS_LOCK is asserted to 1'b1.

4. PRBS error counter: Following are the description and features of the error counter.

- PRBS error counter is a 31 bits long counter and it is clear on read register. Only way to clear the counter is by reading it or by reset. Counter value will be held during the period when PRBS Checker is disabled.

- It is a saturate counter which will saturate at the max value of {31{1'b1}} until it is cleared by reading it.

- It is divided into 2 register fields, MSB bits [30:16] and LSB bits [15:0]. MSB bits [30:16] are organized in the same 16 bit register along with the **PRBS_LOCK_LOST_LH register** in the MSB bit 15 so that they can be read together.

MSB bits should be read before the LSB bits of the counter. When MSB portion is read then it latches the LSB portion and clears the internal 31 bit counter to start counting the error for next interval.

- There are 2 modes of counting the errors.
    - **Bit error counting mode** – Each bit in error will be counted.
    - **Burst error counting mode** – A burst of errors will be counted as 1 error. Single burst of errors can span across more than 1 clock cycle (40 bits) but one burst will be counted as one irrespective of number of bit errors in that burst. Each burst of errors should be separated by at least 1 clock cycle (40 bits) of no errors.

5. Assuming 20 symbols/40 bits wide data bus with worst case freq around 28.125 Ghz/20 = ~1.4 Ghz.

6. PRBS checker module is designed with the assumption that the MSB bit 39 of the input received data is the first received bit and LSB bit 0 is the last received bit on the parallel data bus but the parallel data from the Kernel has bit order reversed where LSB bit 0 is the first received bit and MSB bit 39 is the last received bit so there is a bus reverse function at the PRBS checker block input which converts the received data so that MSB bit 39 is the first received bit.

7. It is recommended that any PRBS checker control/configuration change be followed by disabling and re-enabling of the PRBS Checker Enable. In most cases, Error Counter and **PRBS_LOCK_LOST_LH** should be read before starting the PRBS Checking again to clear the previous history in case there is a change in the PRBS configuration like a different polynomial etc.

8. PRBS checker have various ways to determine the duration of the PRBS checking.

    A. Mode A : In this mode, PRBS checker enable is controlled directly by writing **prbs_chk_en register to 1'b1. This is the default mode.**
    B. Mode B : When **rg_prbs_chk_en_auto_mode register is 1'b1 then** PRBS checker enable is turned ON when both rx_pmd_lock and rg_prbs_chk_en are 1'b1. Will be used in EEE mode to check the CDR lock timer after signal_detect/energy_detect.
    C. Mode C : In this mode, PRBS checker is either enabled in mode A or B but additionally PRBS checker can be programmed to stop using a timer. PRBS checking will start as soon as mode A or B is enabled but PRBS checking will be stopped automatically after a timer value or if the mode A or B depending on which one was selected is disabled. To re-start the PRBS checking again, PRBS checker has to be disabled by disabling the mode A or B depending on which one is selected

and then re-enabling it again. Timer is implemented using 1us (if rg_prbs_chk_en_timer_mode = 2'b10) or 1 ms (if rg_prbs_chk_en_timer_mode = 2'b11) heartbeat timers and a timeout value controlled by the register rg_prbs_chk_en_timeout[4:0]. rg_prbs_chk_en_timeout[4:0] can have valid values from 0 to 31 which translates to 0 to 448 counts. All the mode and timeout registers are expected to be programmed before enabling the PRBS checker.

Remote Loopback.

Blackhawk core supports remote loopback, which will enable the receive data to be looped back through the logically paired transmit lane. The following block diagram highlights the data path that is enabled during this mode.

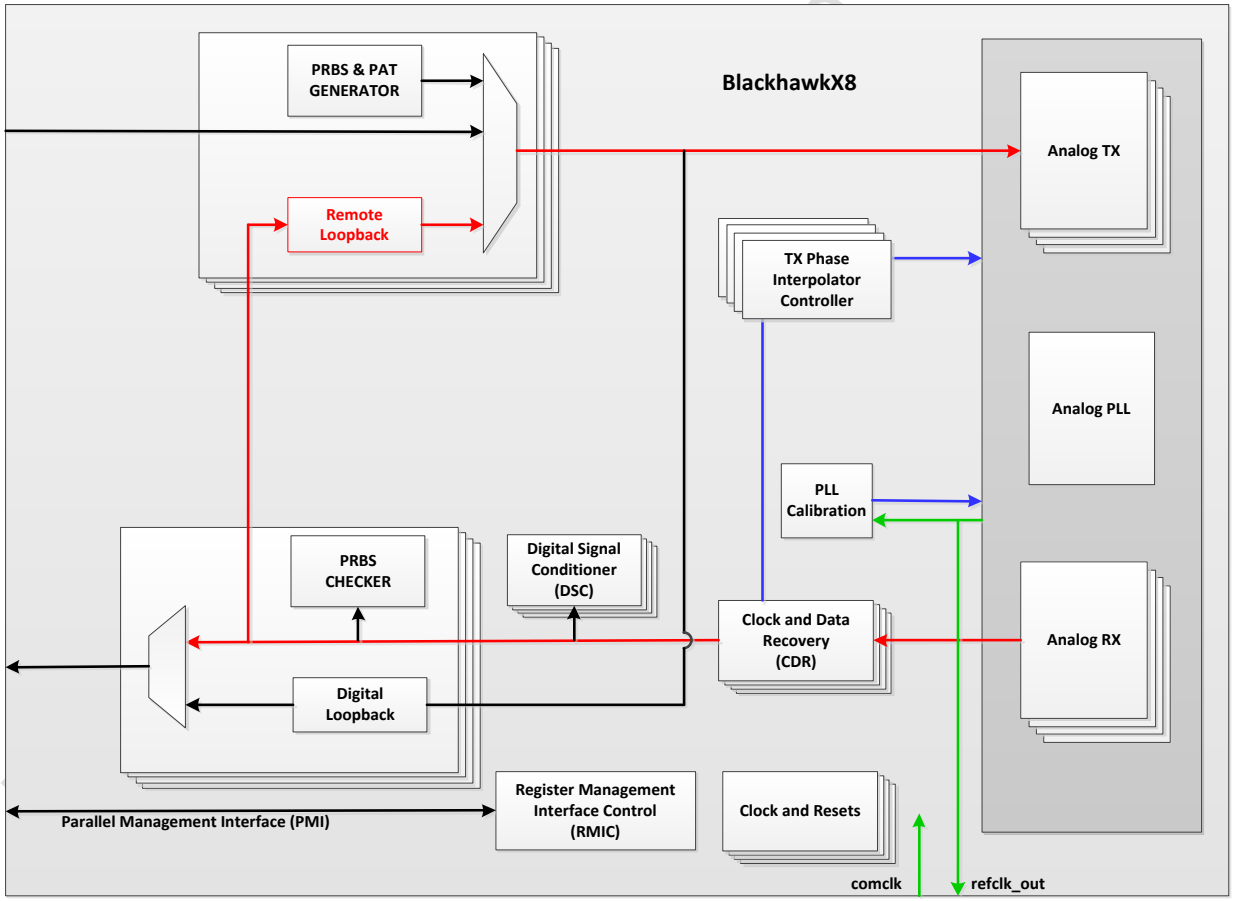


FIGURE 11: REMOTE LOOPBACK

Digital Loopback

Blackhawk supports a digital loopback that turns around the transmit data before it goes into the analog macro. Basically, this is a digital data path loopback for the data coming from the PCS/MAC transmit side. Instead of using a typical phase fifo or muxing in the transmit clock, a new design technique is used to control the rx clock phase. Please refer to the micro architectural document/section to find out more details about the process of sampling the data and controlling the receive side phase interpolator to achieve this loopback. The following block diagram highlights the data path that is enabled during this mode.

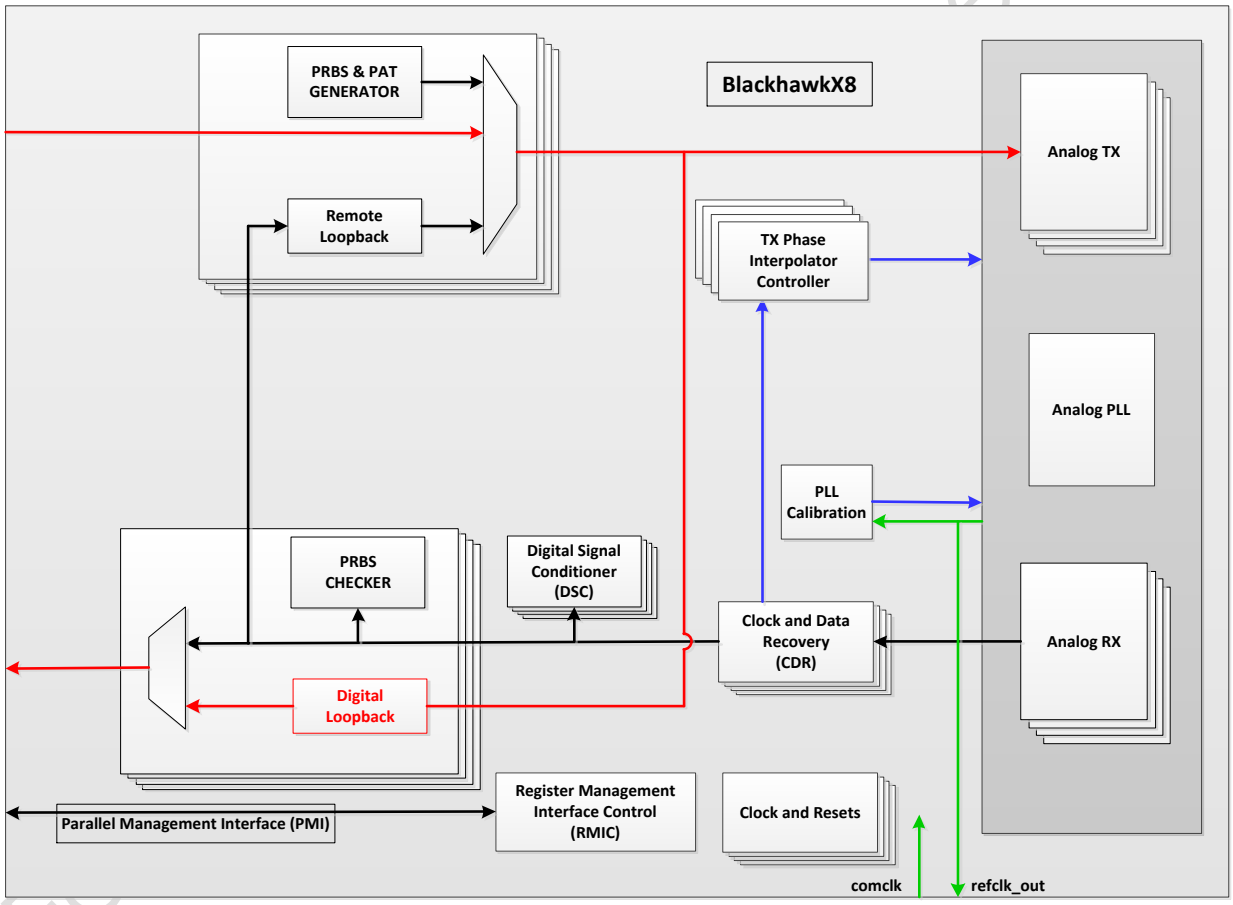


FIGURE 12: DIGITAL LOOPBACK

PMD RX/TX Data Invert:

Core supports the inversion of all the data bits in both RX and TX direction at the parallel data to/from the Kernel/AFE to account for P/N swap on the board. Registers are : ***rx_pmd_dp_invert*** and ***tx_pmd_dp_invert.***

RX Operating Modes Summary

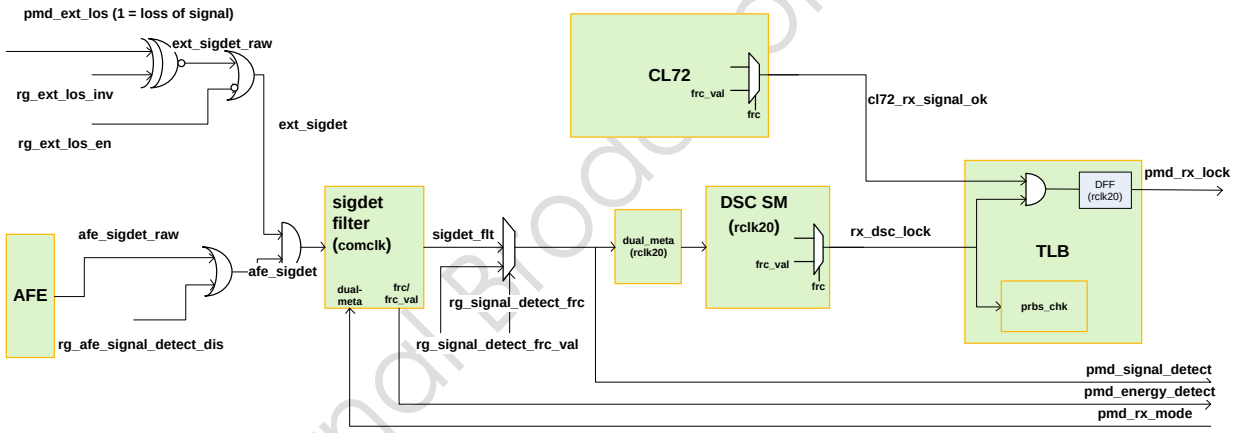
1) RX lane configuration shall be independent for each lane, except for shared VCO.
2) Nomenclature
    a. "…xN" mode implies ratio of VCO clock to lane signaling rate is N:1
    b. "OSRxN" implies OS CDR
    c. "OSR" implies Over-Sampled Receiver
    d. "KRxN", implies CDR auto-selection during Clause 72 negotiation or equivalent software emulation
    e. "BRxN" implies baud-rate (BR) CDR, typically used with TXFIR pre-cursor on long channels
3) In theory, every OSR mode can be supported from every VCO rate, however to reduce verification and validation burden many of the unlikely use cases have been trimmed in the table below.
4) Supported line rates are a function of scrambling and desired equalization
    a. Scrambling
        i. 64b/66b and scrambled 8b/10b are considered "scrambled"
        ii. 8b/10b with unscrambled data or unscrambled idles is considered "unscrambled"
        iii. Unscrambled 8B/10B with DFE is supported only up to 6.5625Gbd
        iv. Unscrambled 8B/10B without DFE is supported only up to 8.5Gbd (for FC 8.5G)
    b. Equalization
        i. Only x1,x2 and x3 are fully adaptive
        ii. Only x1 and x2 modes can support DFE
        iii. DFE is **not supported** for rates below 5.75Gbd
        iv. DFE is **required** for rates above 10.3125Gbd
            1. Rationale - AFE BWs are low, reduces effort in maintaining a DFE and non-DFE version
        v. Clause 72 is supported for electrical links at rates ≥ 8.125 Gbd
            1. Clause 72 hardware may be enabled in the absence of auto-negotiation
            2. Clause 72 like operation may be emulated using software

vi. Adaptive equalization can further be specialized to the Medium as
    1. PCB traces or Backplane
    2. Optical
    3. Copper cables

5) **Clause 73 DME detection** is supported only in **OSRx16P5 and OSRx20P625** modes (generates 2.5GHz data)

PMD Rx Lock signal.

The section describes the signal propagation of the signal detect and ext LOS to PMD RX lock signal. When PMD RX Lock signal is low, the receiver is acquiring lock. During this period the phase of the receive clock and alignment of data are not reliable. All decode functions in the PCS or higher level logic should wait for the assertion of this signal. The diagram is self-explanatory and the override bits are available under the user register list.



Block Diagram of RX_PMD_LOCK implementation in Eagle/Merlin

User registers and clock domains.

The clocking scheme in Blackhawk has been carefully crafted to reduce the number of clock domains, synchronous register interface and reduced latency data path.

Receive Clock Domain

All the receive data path logic in any given lane runs off of the recovered clock. The user registers associated with receive logic is also running on the same recovered clock. There are individual controls to gate off the data path clock. During pll configuration and oversampled mode programming, the clocks to the data path will be gated off and the clocks to the registers will be switched to

comclk for user access. Figure 13: Logic in rclk20 domain highlights the blocks running on rclk20.

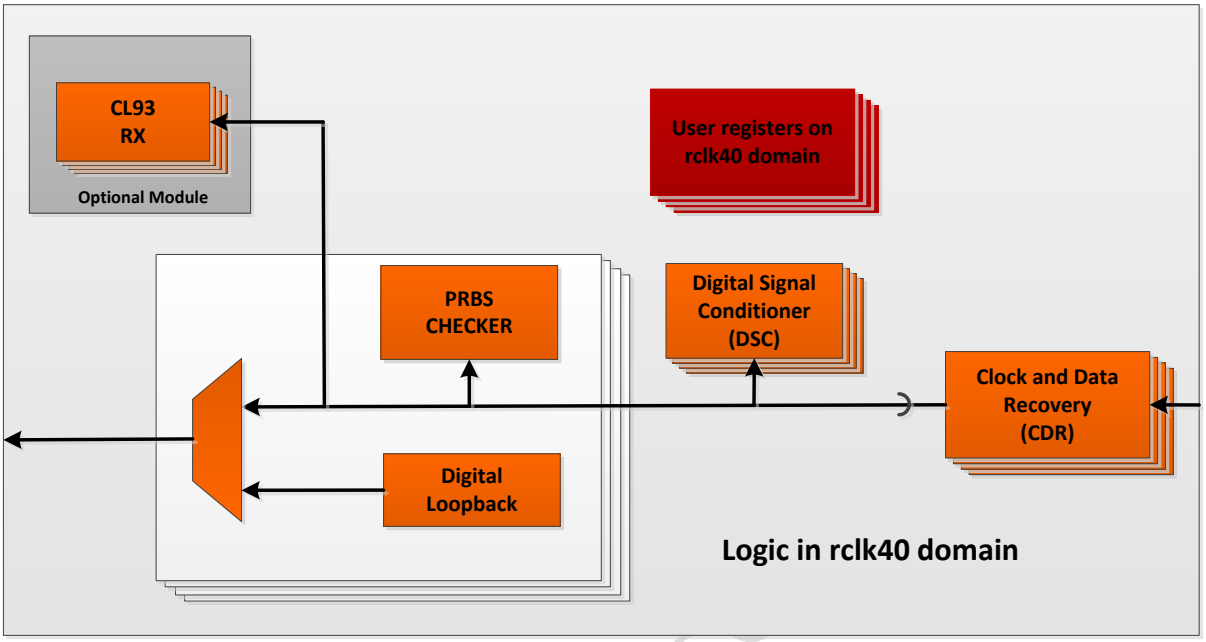


FIGURE 13: LOGIC IN RCLK20 DOMAIN

Transmit Clock Domain

All the transmit data path logic in any given lane runs off of the same transmit clock. The user registers associated with transmit logic is also running on the same transmit clock. There are individual controls to gate off the data path clock. During pll configuration and oversampled mode programming, the clocks to the data path will be gated off and the clocks to the registers will be switched to comclk. Figure 14 : Logic in tclk20 domain highlights the blocks running on tclk20.

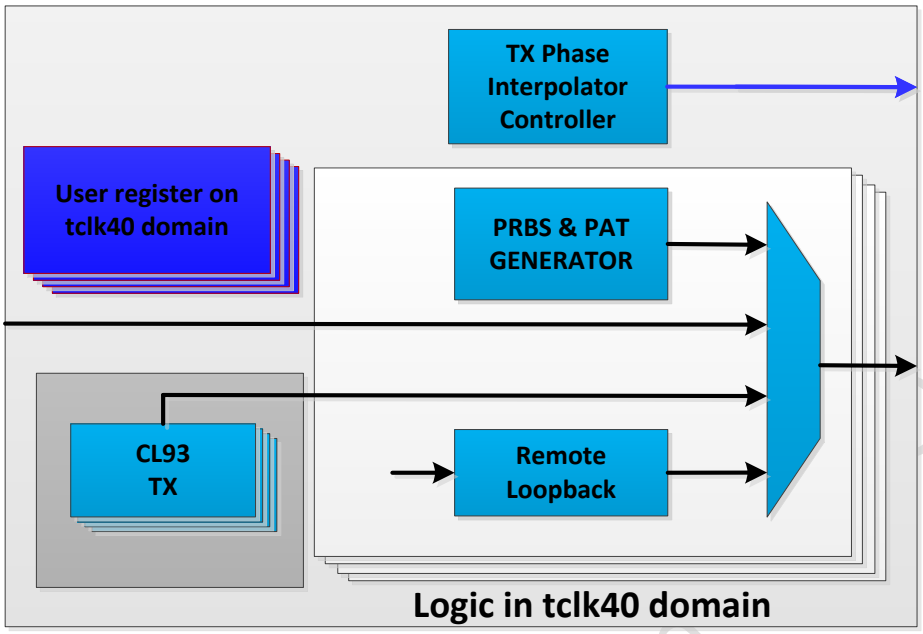


FIGURE 14 : LOGIC IN TCLK20 DOMAIN

Communication Clock Domain

All the common core level logic, PLL calibration, some of the lane side control logic and RMIC runs on comclk domain. Figure 15 : Logic in comclk domain highlights the associated logic.

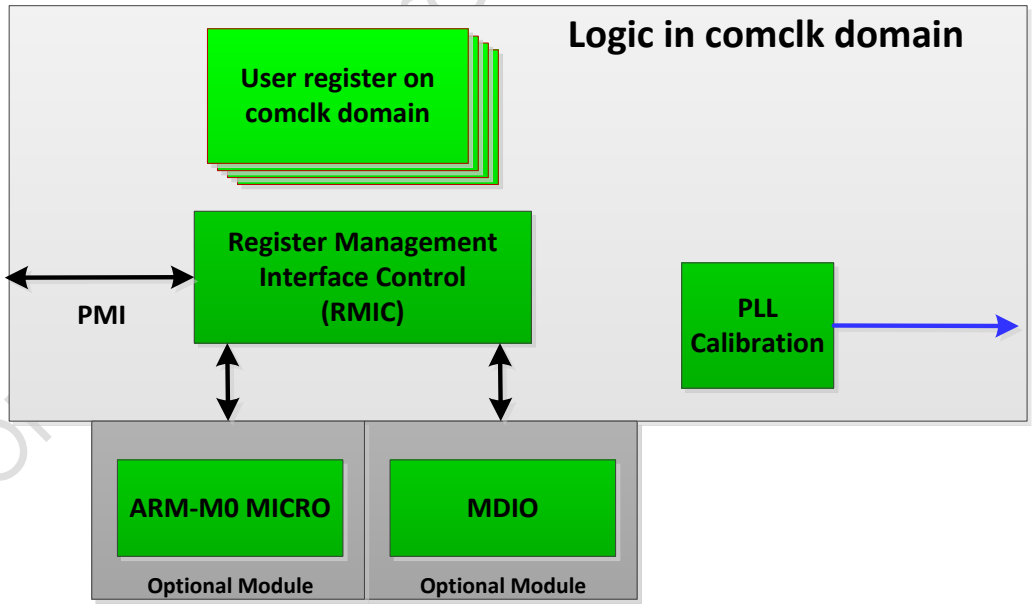


FIGURE 15 : LOGIC IN COMCLK DOMAIN

Core and Lane level Resets.

Blackhawk supports several core-level and lane-level resets through hardware pins or software registers. The table below lists the resets with the defaults and description. The user registers associated with this logic is also running on comclk clock.

Event	Core level			RX Lane[i]				TX Lane [i]				Description
	Logic		Clk Domain	Logic		Clk Domain		Logic		Clk Domain		
	DP	User Reg	comclk	DP	User Reg	comclk	rxclk20/rxclk40	DP	User Reg	comclk	txclk20/txclk40	
Functional Mode	Active	Active	comclk	Active	Active	comclk	rxclk20/ rxclk40	Active	Active	comclk	txclk20/ txclk40	
pmd_por_h_rstb	Under reset	Under reset	comclk	Under reset	Under reset	comclk	comclk	Under reset	Under reset	comclk	comclk	The entire core is under reset, including the MDIO and RMIC
pmd_core_pll*k*_dp_h_rstb	Under reset	Active	comclk	Under reset	Active	comclk	comclk	Under reset	Active	comclk	comclk	Core level data path reset through a pin. This will reset the PLLk and RX datapath and TX data path (including TX_PI) in all the lanes which are selected to use PLLk where ***k*** is 0 and 1. Active low.
pmd_ln_rx_h_rstb[i]	Active	Active	comclk	Under reset	Under reset	comclk	comclk	Active	Active	comclk	txclk20/ txclk40	RX Logical Lane "I" reset through a pin that will keep the receive analog, data path and all the registers associated with RX lane "I" under reset.
pmd_ln_rx_dp_h_rstb[i]	Active	Active	comclk	Under reset	Active	comclk	comclk	Active	Active	comclk	txclk20/ txclk40	RX Logical Lane "I" reset through a pin that will keep the receive analog and data path associated with RX lane "I" under reset. Lane user regsiters are available for read and write.
pmd_ln_tx_h_rstb[i]	Active	Active	comclk	Active	Active	comclk	rxclk20/ rxclk40	Under reset	Under reset	comclk	comclk	TX Logical Lane "I" reset through a pin that will keep the receive analog, data path and all the registers associated with TX lane "I" under reset including TX PI
pmd_ln_tx_dp_h_rstb[i]	Active	Active	comclk	Active	Active	comclk	rxclk20/ rxclk40	Under reset	Active	comclk	comclk	TX Logical Lane "I" reset through a pin that will keep the receive analog and data path associated with TX lane "I" under reset including TX PI. Lane user regsiters are available for read and write.
core_s_rstb	Under reset	Under reset	comclk	Under reset	Under reset	comclk	comclk	Under reset	Under reset	comclk	comclk	Pmd core reset though a user register. The entire core will be under reset, MDIO/RMIC/MICRO blocks/interfaces. The user should be able to clear this reset through MDIO or PMI_LP/HP.
core_dp_s_rstb[k] (k = 0, 1)	Under reset	Active	comclk	Under reset	Active	comclk	comclk	Under reset	Active	comclk	comclk	Core level data path reset through a register at the core digital registers in the comclk domain. This will reset the PLLk and RX datapath and TX data path (including TX_PI) in all the lanes which are selected to use PLLk where ***k*** is 0 and 1. Active low.
rx_ln_s_rstb[i]	Active	Active	comclk	Under reset	Under reset	comclk	comclk	Active	Active	comclk	txclk20/ txclk40	RX Logical Lane "I" reset through a register that will keep the receive analog, data path and all the registers associated with RX lane "I" under reset.
rx_ln_dp_s_rstb[i]	Active	Active	comclk	Under reset	Active	comclk	comclk	Active	Active	comclk	txclk20/ txclk40	RX Logical Lane "I" reset through a register that will keep the receive analog and data path associated with RX lane "I" under reset. Lane user regsiters are available for read and write.
tx_ln_s_rstb[i]	Active	Active	comclk	Active	Active	comclk	rxclk20/ rxclk40	Under reset	Under reset	comclk	comclk	TX Logical Lane "I" reset through a register that will keep the receive analog, data path and all the registers associated with TX lane "I" under reset including TX PI
tx_ln_dp_s_rstb[i]	Active	Active	comclk	Active	Active	comclk	rxclk20/ rxclk40	Under reset	Active	comclk	comclk	TX Logical Lane "I" reset through a register that will keep the receive analog and data path associated with TX lane "I" under reset including TX PI. Lane user regsiters are available for read and write.
pmd_ln_rx_h_pwrdwn[i]	Active	Active	comclk	Under reset	Active	comclk	comclk	Active	Active	comclk	txclk20/ txclk40	Assertion of this power down pin will put the logical receive lane "I" datapath under reset. The registers will not be under reset. Also the lane registers that are on comclk will have active clocks. The user should be able to read/write the lane registers. **AFE RX pwrdwn pins will also be asserted.**
pmd_ln_tx_h_pwrdwn[i]	Active	Active	comclk	Active	Active	comclk	rxclk20/ rxclk40	Under reset	Active	comclk	comclk	Assertion of this power down pin will put the logical transmit lane "I" datapath under reset. The registers will not be under reset. Also the lane registers that are on comclk will have active clocks. The user should be able to read/write the lane registers. **AFE TX pwrdwn pins will also be asserted.**
pmd_ln_rx_s_pwrdwn[i]	Active	Active	comclk	Under reset	Active	comclk	comclk	Active	Active	comclk	txclk20/ txclk40	Assertion of this power down register will put the logical receive lane "I" datapath under reset. The registers will not be under reset. Also the lane registers that are on comclk will have active clocks. The user should be able to read/write the lane registers. **AFE RX pwrdwn pins will also be asserted.**
pmd_ln_tx_s_pwrdwn[i]	Active	Active	comclk	Active	Active	comclk	rxclk20/ rxclk40	Under reset	Active	comclk	comclk	Assertion of this power down register will put the logical transmit lane "I" datapath under reset. The registers will not be under reset. Also the lane registers that are on comclk will have active clocks. The user should be able to read/write the lane registers. **AFE TX pwrdwn pins will also be asserted.**
pmd_iddq	Active	Active	No Clk	Active	Active	No Clk	No Clk	Active	Active	No Clk	No Clk	Assertion of pmd_iddq pin will gate off all the lane clocks and comclk. None of the resets will be asserted. Hence registers will hold the programmed values. The user is expected to program the analog registers values and power down before asserting the pmd_iddq pin. Deassertion of pmd_iddq pin will not guarantee a normal operation. A POR sequence is the only way to recover to a normal status.
ln_rx_s_rstb[i]	Active	Active	comclk	Under reset	Under reset	comclk	comclk	Active	Active	comclk	txclk20/ txclk40	Assertion of this software reset on recevie lane I will resets all the registers and dp associated with logical receive lane i. Active low. This is a debug feature. Software restoration is not supported if any of this reset is asserted.
ln_rx_dp_s_rstb[i]	Active	Active	comclk	Under reset	Active	comclk	comclk	Active	Active	comclk	txclk20/ txclk40	Assertion of this software reset on recevie lane I will resets dp associated with logical receive lane i. Active low. This is a debug feature. Software restoration is not supported if any of this reset is asserted.
ln_tx_s_rstb[i]	Active	Active	comclk	Active	Active	comclk	**rxclk20/rxclk40**	Under reset	Under reset	comclk	comclk	Assertion of this software reset on transmit lane I will resets all the registers and dp associated with logical transmit lane i. Active low. This is a debug feature. Software restoration is not supported if any of this reset is asserted.
ln_tx_dp_s_rstb[i]	Active	Active	comclk	Active	Active	comclk	**rxclk20/rxclk40**	Under reset	Active	comclk	comclk	Assertion of this software reset on trasnmit lane I will resets dp associated with logical transmit lane i. Active low. This is a debug feature. Software restoration is not supported if any of this reset is asserted.

TABLE 18: TEST CORE RESETS

Transmit Clock Alignment (TCA)

Blackhawk TCA aligns all or group of the TX lane clocks pmd_tclk20_i. One of the lanes of the group can be selected as master lane and rest of the lanes (called slave lanes) will be aligned to the master lane. There can be multiple TCA groups and each group can be aligned to it's master lane. TX lanes will be aligned within TBD ps.

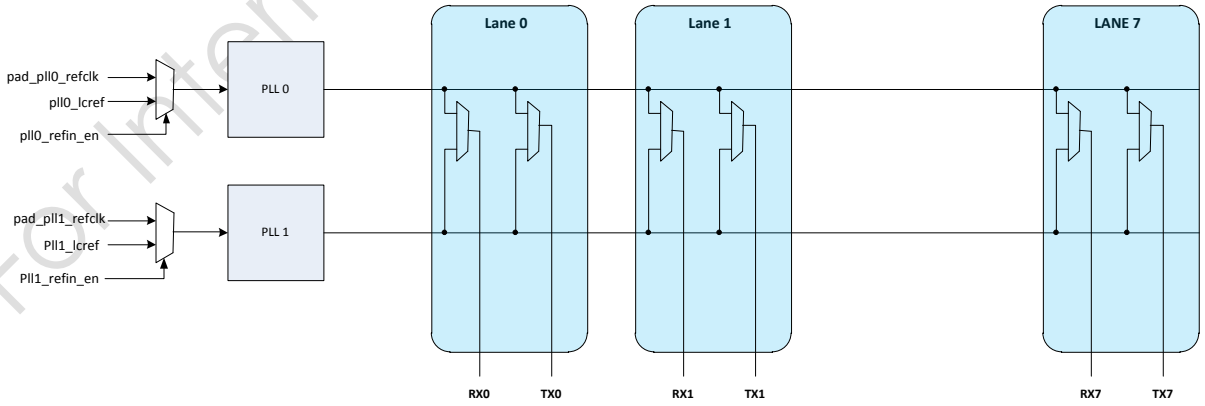
TCA sequence needs to be done whenever any TX lane of that group comes out of the datapath reset. While TCA is being done, TX can be set into elec_idle mode.

There is a detailed programming sequence for TCA included in function. serdes_tca_sequence ();

For PMD applications, only TCA Phase Lock Sequence portion is required but full sequence might be needed for the RPTR applications.

2 PLL usage

Blackhawk core supports 2 independent PLLs with separate refclk and lcref inputs. Here is a block diagram showing how this is configured.



Addressing each PLL register

Register fields are common for each PLL. The field for each PLL is selected by using the address bits 25:24 in the 32-bit address to select the PLL. A value of 0 in this field will select PLL0 and a value of 1 will select PLL1.

Selecting clock source for PLL

Each PLL can select between either refclk pad input or lcref input using the core input pins pll0_refin_en and pll1_refin_en. A value of 0 selects refclk pad input. A value of 1 selects the lcref input source.

Selecting vco clock for each lane

The transmit and receive part of each lane can independently select the VCO clock from any PLL. The lane has to be in reset before this field can be reconfigured to select a different PLL. This is done by using the following per lane register fields.

- tx_pll_select (0=PLL0, 1=PLL1)
- rx_pll_select (0=PLL0, 1=PLL1)
- In addition to the RX and TX registers, there is a virtual field pll_select that can be used to address both RX and TX if RX and TX have to be set to the same value.

core_dp_rstb

The core_dp_rstb has been split up into the 2 PLLs and the pins and regiser bits have been separated out. The pins are:

- pmd_core_pll0_dp_h_rstb
- pmd_core_pll1_dp_h_rstb

The register bits are

- core_dp_s_rstb (This is addressed separately for PLL0 and PLL1)

This resets the PLL and also the lanes associated with that PLL. This reset has to be asserted before any PLL reprogramming can happen.

MDIO Controller

The mdio block supports these features:

- Support for clause 45 mdio frames. Clause 22 is not supported.
- A 16-bit AER register provides the upper 16-bits of the address to provide a 32-bit address output.
- A 5-bit strap input devid_strap[4:0] is provided for device id which is typically set to 5'h01 for PMD device.
- A 5-bit strap input prtad_strap[4:0] is provided for port address to select the port address to decode for the mdio slave. In addition, a broadcast port address register provides a way for the mdio controller to respond to a port broadcast.
- The mdio block provides an early indication of a decoded read transaction to the clock and reset block to hold off clock switching if a reset or any event had occurred that would initiate clock switching. This early indication is provided 2 mdio clock cycles before the enable for a read transaction.
- Debug bit mdio_fast_mode to remove preamble decode from an mdio frame for faster mdio access.
- All the logic in mdio slave block runs in comclk domain. Only one flop at the input is clocked by mdio_clk for mdio_in pin and one flop at the output is clocked by mdio_clk for mdio_out data.

Management registers

The management registers and the access interface is targeted for a standards or protocol agnostic scheme. The register interface or address mapping are planned to support Clause 45 protocol. And all the addresses for registers are mapped to the IEEE vendor space. This means the core will not have any IEEE Clause 45 specified registers; basically, it will be a standards agnostic PMA/PMD core. A chip level software driver or any coding layer, such as PCS, is expected to handle any specific IEEE registers.

The chapter on Blackhawk registers gives more details about the address mapping; register partitioning and logical to physical address remapping for certain transmit registers.

Arm M0 Micro Sub System

The Blackhawk Microcontroller Subsystem receives instructions to program and enable microcontrollers from the Blackhawk core via the register interface. It uses the pmi_hp* interfaces to configure and monitor status of the Blackhawk PMD/PCS cores.

The primary PMD functions of Micro are:

1) adapting analog settings to achieve good BER
2) providing feedback to Clause 72/93 to make requests to the link partner's transmitter
3) provide abstracted interfaces to debug tools to measure link and channel quality
4) Provide corrections to register defaults upon register reset events (core, TX lane, RX lane)
5) Implement software emulation of Clause 72/93 function
6) Implement timeouts and restarts for Clause 72/93 without Clause 73 AN.

Microcontroller Subsystem Document is located here:

TBD

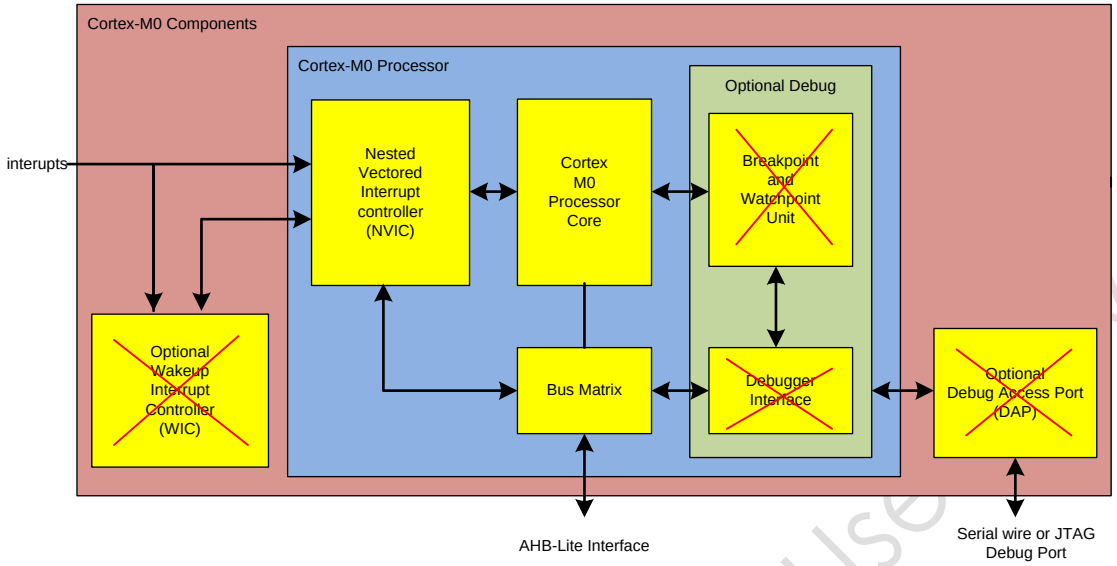


FIGURE 16 CORTEX-M0 COMPONENTS

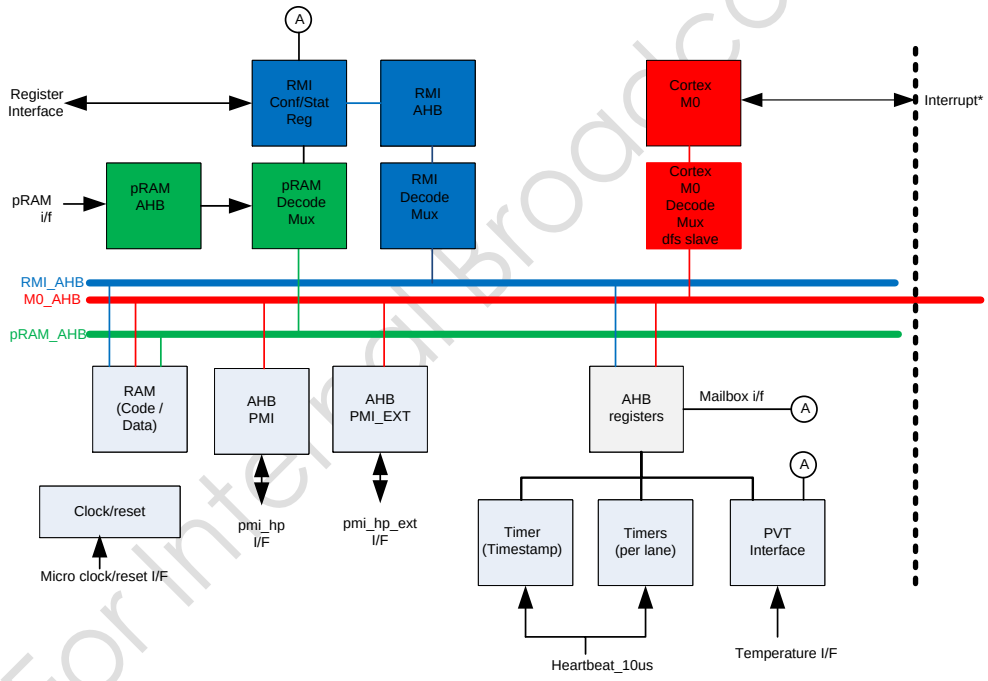


FIGURE 17 BLACKHAWK MICROCONTROLLER SIMPLIFIED DIAGRAM

Simulation

For details about programming and initialization routines please refer to the Blackhawk Programmers Guide.

Define Statements

`PMD_SIMULATION – Should be defined during simulations. Do not define during synthesis

`BLACKHAWK_GATESIM: The default behavior of the analog behavioral model is to drive x's on the clk and data buses during powerdown or reset. Setting this define forces the model to drive 0's during powerdown or reset which is useful for gatesims. This define does not apply when running with the ce model.

`CE_ANA_MODEL: This selects the Central engineering analog verilog model for simulation instead of the default simple analog verilog model provided by the digital PMD team.

AFE Simulation Models

There are 2 simulation models available with the Blackhawk SerDes.

AFE Model is a simplified functional model developed by PMD team and supports most features of the AFE. To use the AFE model users should call the blackhawk_filelist in simulation command-line.

CE Model is a logical model developed by CE Analog team and is the GOLD standard and supports all functional modes and test modes. This model simulates slower but is most accurate representation. To use the CE model users should call the blackhawk_ce_filelist in simulation command-line.

Simulation Speedup Mode

There are procedures for speeding up simulations. Please refer to Programmers Guide for details.

Analog modeling of line voltages

The simulation models for the AFE models the serial RX and TX lines as a real number to model analog voltages in mV that can be used to encode PAM4 data. Here is how these are modeled for the transmit and receive sides.

Transmitter model for PAM4/NRZ

MODE	PAM4 code {MSB,LSB}	DAC code	TDP (Volt)	TDN (clock=VCO/2)
NRZ	11	127	+0.750	Clock
	00	1	+0.2539	Clock
PAM4	11	127	+0.750	Clock
	10	85	+0.5846	Clock
	01	43	+0.4193	Clock
	00	1	+0.2539	Clock
	Idle		0.0	0.0
	Pwrdn		0.0	0.0
	Reset		0.0	0.0

Receiver Model for PAM4/NRZ

MODE	RDP (Volt)	RDN (Volt)	PAM4 code {MSB,LSB}
NRZ	+0.750	+0.2539	11
	+0.2539	+0.750	00
PAM4	+0.750	Clock	11
	+0.5846	Clock	10
	+0.4193	Clock	01
	+0.2539	Clock	00
	0	0	Idle (loss of signal)

Electrical Characteristics

Blackhawk core is designed for compliance to the electrical specs of many standards, including

Compliance spec	Line Rates Relevant to spec (Gbd)	Notes
Standards Based Rates		
1000Base-KX		which is also used for the SGMII mode
10G CX-4		
CEI-6G-SR	5.75 to 6.5625	
CEI-6G-LR	5.75 to 6.5625	
10G KR	10.3125	
XFI+	10.3125	
XLAUI	10.3125	
SFI	10.3125	
40G nPPI	10.3125	
40G CR4	10.3125	
40G KR4	10.3125	
CEI-11G-SR	10.3125 to 12.5	
CEI-28G-VSR	19.6-28.125	
CEI-28G-SR	19.9-28.125	
CEI-25G-LR	19.9-25.8	
100G CR4	25.78125	
100G KR4	25.78125	
Proprietary Extensions and Rates		
Extended KR,	10.3125	Amax of 32dB, with better Xtlk and RL than IEEE spec

KR4		
10.9G KR	10.9375	TX & RX: scaled KR spec Channel: same as KR
11.5G KR	11.5	Scaled KR spec
12.5G KR	12.5	Scaled KR spec, Amax of 18dB @ 6.25GHz
Super XFI	10.3125	Assumed 16dB loss with 6dB de-emphasis (need to verify)
Scaled XLAUI	10.3125 to 12.5	Frequency scaled XLAUI spec
Extended SFI	10.3125	Adds 2.4dB to PCB traces
Extended nPPI	10.3125	Adds 2.4dB to PCB traces
Extended CR4	10.3125	Adds 2.4dB to PCB traces

However, in many cases, the actual tested compliance will depend on other factors such as, the package substrate design, and the signal integrity of the test setup.

Detailed Electrical specification is available as part of the Analog Module Specification (AMS).

Datapath Latency for OSRx1, OSRx2 and OSRx4 Modes

Datapath Latency	AFE Latency (S2P/P2S) from AMS, (typical)	AFE-Digital Interface	PCS Interface	Digital Clock-Tree	Total Latency (UI)
RX (in UI)	23	8 (half-cycle transfer at the AFE I/F 20 bit with 60/40 duty cycle clock)	40	10 (0 –cycle transfer from 20 to 40 bits rely on clock skew on rclk20)	81 (Note1)
TX (in UI)	24	40	40	0 (N/A)	104 (Note1)

Note1:

1. RX side latency in UI terms is same for OSRx1, 2, 4.
2. TX side latency in UI terms is same for OSRx1, 2, 4 due to clock scaling.
3. Please note that if PCS interface retiming flops are removed for a core then it is the responsibility of the chip team to meet the interface timing as datapath signals will have combinatorial logic in the timing path.
4. These latency numbers are for the middle bit of the parallel data bus at the PCS interface to/from the serial output/input pads.

Validation

Recommended Core validation will be furnished in the next revision of this document.

Marketing Requirements Document

Blackhawk Marketing Requirements Document can be located at Blackhawk Sharepoint.

Relevant Standards and Documents

Standard/Document	Abbreviation	Description
OIF CEI	CEI-11G-SR CEI-6G-SR CEI-6G-LR CEI-28G-VSR CEI-28G-LR	
IEEE 802.3-2008	803.3-2008	All Ethernet speeds up to 10G Backplane Ethernet – clause 69 Backplane channel specs – Annex 69B KR – clause 72 AN – clause 73 FEC – clause 74 10G SR & LR
IEEE 802.3ba -2010	802.3ba	XLAUI, CR4, SR4, LR4, PPI (Quad SFI)
Specifications for Enhanced Small Form Factor Pluggable Module SFP+	SFF-8431	SFI for optics, copper
FIBRE CHANNEL Physical Interface-3 (FC-PI-3) REV 3.0	XFI+	Updated spec for XFI
Fiber Channel	TBD	TBD
JESD204B	JEDEC 12.5G	Very similar to CEI-11G-SR

Standard/Document	Abbreviation	Description
Super XFI	TBD	Doc Unavailable