Lesson EPSI-04-01 download the pdf file here

Course EPSI:
Essential Principles of Signal Integrity

With Eric Bogatin,
Signal Integrity Evangelist, Teledyne LeCroy Front Range Signal Integrity Lab
Dean, Teledyne LeCroy Signal Integrity Academy
Adjunct Professor, University of Colorado, Boulder, ECEE

- EPSI-04-01: recorded live, Dec 1, 2013
  - An introduction to section 4: engineering routing topologies
  - Download a pdf copy of the slides by clicking the link on this page

Lesson EPSI-04-10 Routing Topologies

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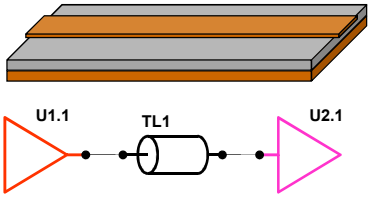
EPSI-04-10: recorded live, Dec 1, 2013

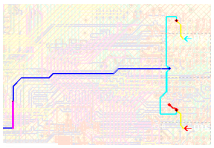
- Why branches cause reflections
- Point to point
- Clustered load topology
- Daisy chain or linear route

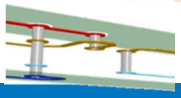
Applying the Youngman Principle:
Turn root cause into best design practices

- Reflections can cause signal distortion and collapse of the eye.
- If the root cause of reflections is changes in the instantaneous impedance, what general guideline do we follow to eliminate reflection noise?
  - ✓ Keep the instantaneous impedance the signal sees constant
- Four typical situations to engineer:

1. Problem: non-uniformity of the transmission lines
   - ✓ *Solution: use controlled impedance lines*
2. Problem: the ends of the lines
   - ✓ *Solution: use a termination strategy*
3. Problem: routing topology
   - ✓ *Solution: use a linear route, keep branches short*
4. Problem: discontinuities
   - ✓ *Solution: keep them short, match to line impedance*

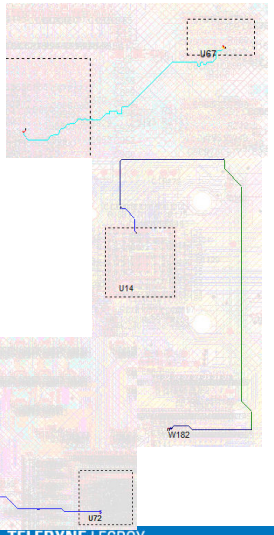






Routing Topologies

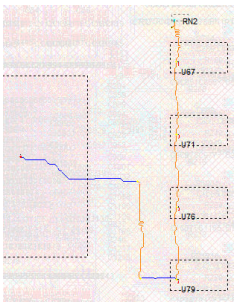
Point to point

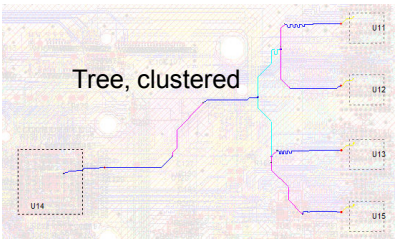


Branched

ALL branched topologies will suffer from multiple reflections that limit highest acceptable data rate

Linear





Lesson EPSI-04-20 Clustered Load Topologies

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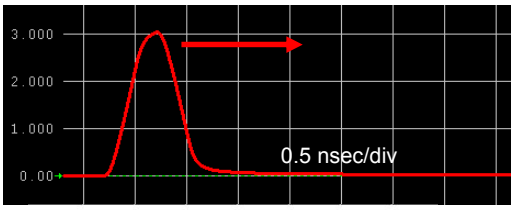
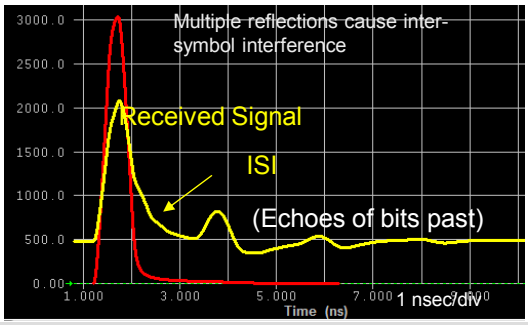
- EPSI-04-20: recorded live, Dec 1, 2013
  - Tree topologies
  - Clustered load
  - Which is better tree or cluster topologies?
  - What limits the maximum data rate?

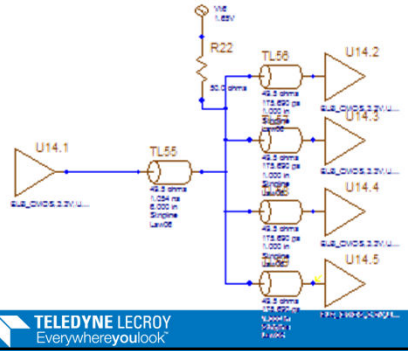
Most Important Principle: A Terminated, Branched Topology Will Always Have Reflection Noise and ISI

0.5 nsec UI, Single bit response (2 Gbps data rate)

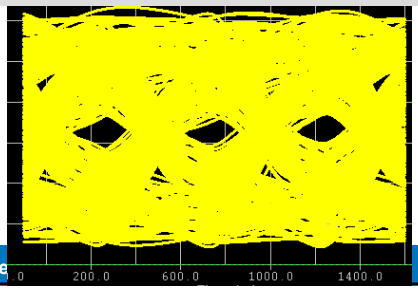




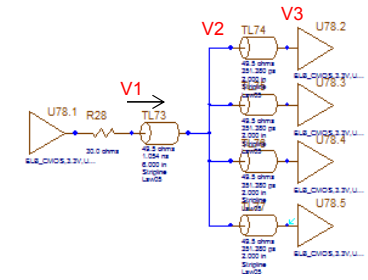
2 Gbps, branch topology, terminated



2 Gbps, point to point topology, terminated



Tree vs Clustered Load: Which one is better?



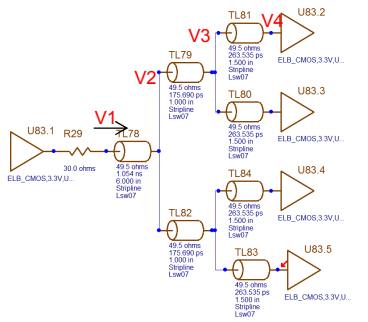
$V1 = \frac{1}{2} V0$

$t2 = \frac{2 \times Z_2}{Z_1 + Z_2} = \frac{2 \times 50/4}{50 + 50/4} = \frac{2}{5}$

$V2 = \frac{2}{5} V1$

$V3 = 2 \times V2$

$V3 = 2 \times \frac{2}{5} \times \frac{1}{2} V0 = \frac{4}{10} 3.3 = 1.32v$



$V1 = \frac{1}{2} V0$

$t2 = \frac{2 \times Z_2}{Z_1 + Z_2} = \frac{2 \times 50/2}{50 + 50/2} = \frac{2}{3}$

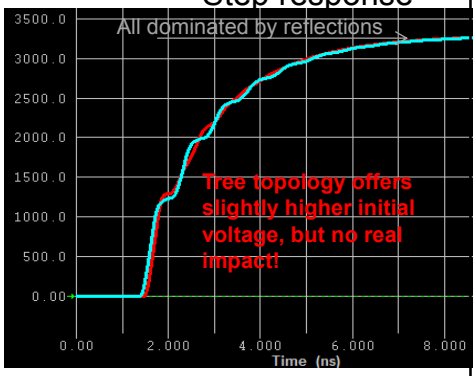
$V2 = \frac{2}{3} V1$

$V3 = \frac{2}{3} V2$

$V4 = 2 \times V3$

$V4 = 2 \times \frac{2}{3} \times \frac{2}{3} \times \frac{1}{2} V0 = \frac{4}{9} 3.3 = 1.47v$

Step response



Lesson EPSI-04-30 Clustered Load Features

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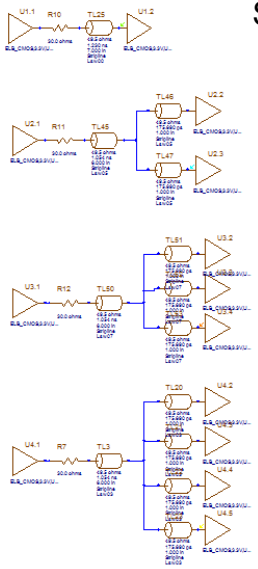
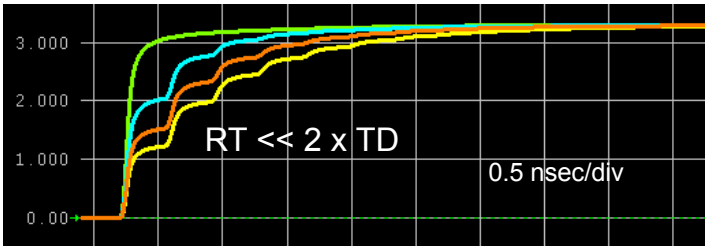
- EPSI-04-30: recorded live, Dec 1, 2013
  - How to optimize a branch topology?
  - Why equal length branches are important
  - Which is a better termination topology?
  - Why it is almost impossible to get above 1 Gbps

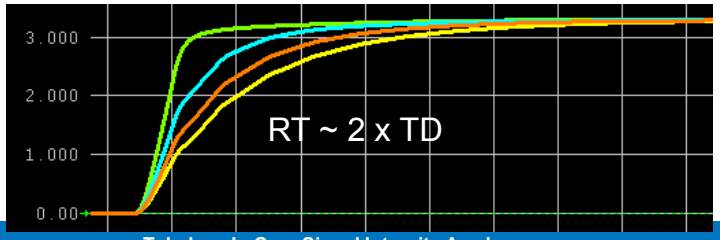
The More Branches, the Longer to Reach Final Voltage @RX



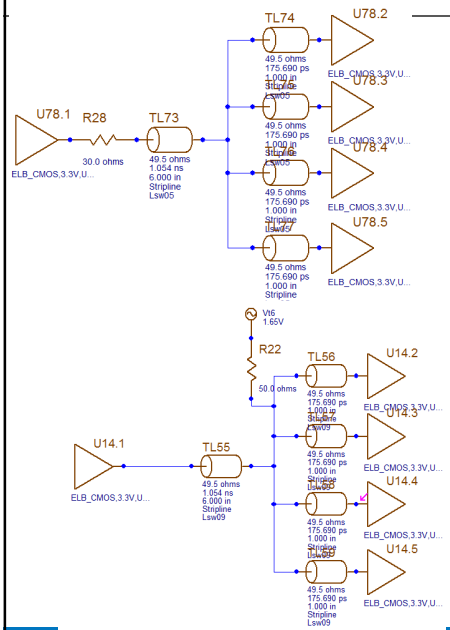
Step response

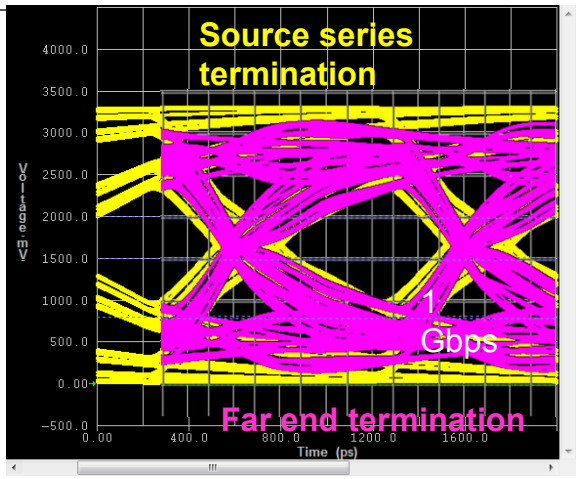


When RT ~ reflection time, reflections are smeared out, it looks like the rise time of RX signal is increasing.



Which is Better: Source Series or Far End Termination?





Generally, far end results in shorter rise time, but both are limited by reflections. You cannot terminate away reflections from branched topologies.

If Branch Lengths are Unequal, More Reflection Noise

- For highest possible data rate in branched topology:
  - Shortest length branches
  - All equal length branches
  - Far end termination
  - Max possible data rate ~ 1 Gbps for 1 inch branches

Lesson EPSI-04-40 Daisy Chain

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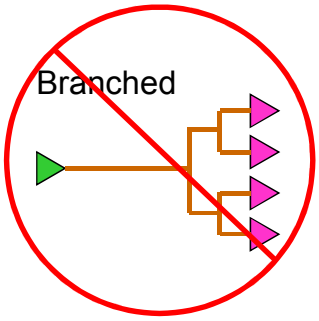
- EPSI-04-40: recorded live, Dec 1, 2013
  - Why DDR3 changed routing topology to DDR4
  - Terminating daisy chain routing
  - How to optimize the Daisy chain route
  - How high a data rate can be achieved with daisy chain

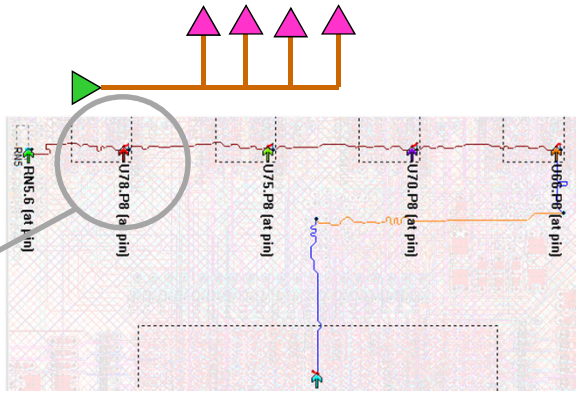
How to Break the 1 Gbps Barrier?

- Don't use branched topology: route with linear topology
  - Key feature: enables shorter branch lengths

Branched

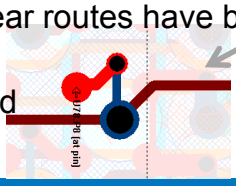


Linear routing (daisy chain)



…but even linear routes have branches!

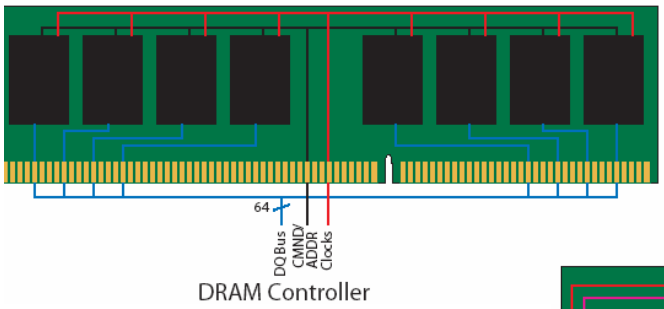
Plus package lead



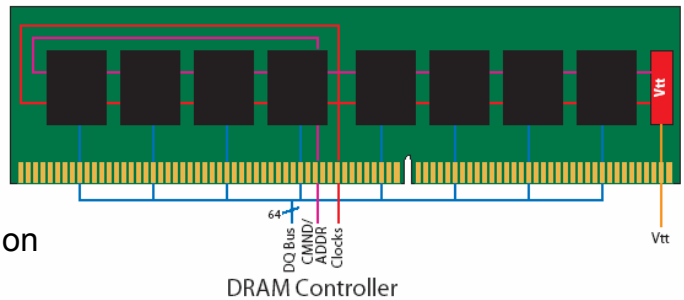
Linear route enables shorter branches, higher possible data rate

Transition from DDR2 to DDR3

DDR2: tree topology

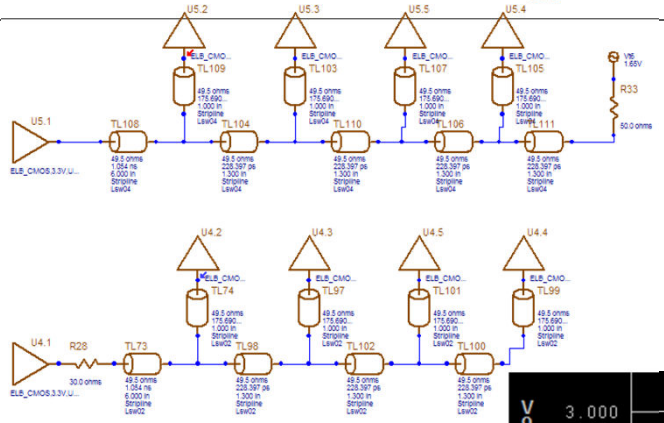


DDR3: linear topology



Linear route with fly-by termination

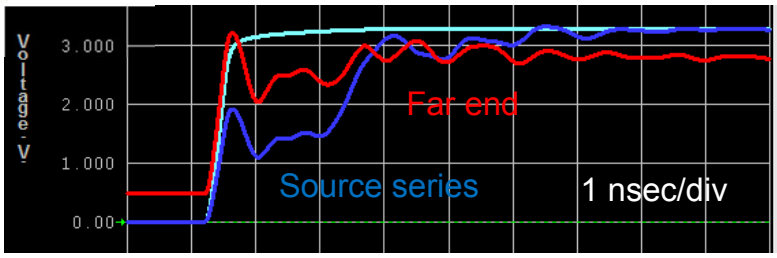
Which Termination Strategy for Daisy Chain?



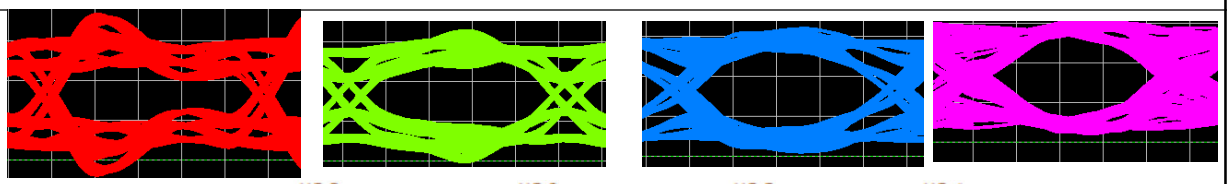
Flyby termination

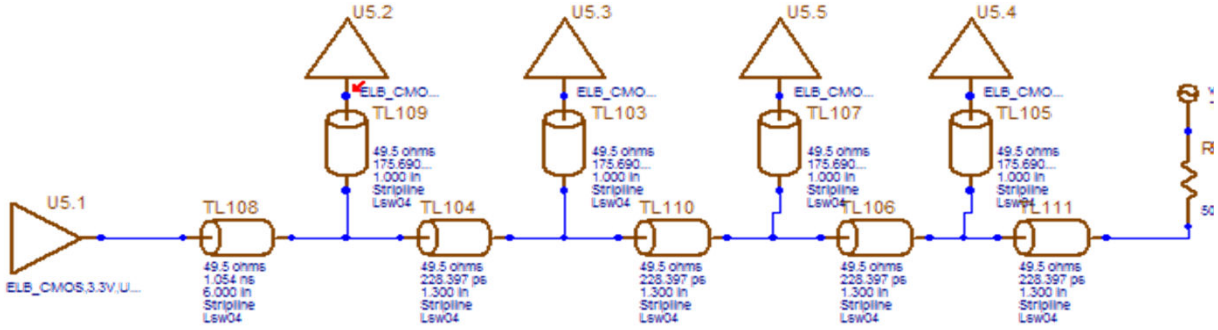
Essential to use far end termination for daisy chain for highest possible data rate

First RX signal in the chain



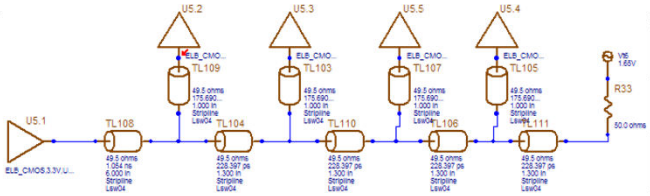
Each RX is Different (@ 1 Gbps, 1 inch stubs))

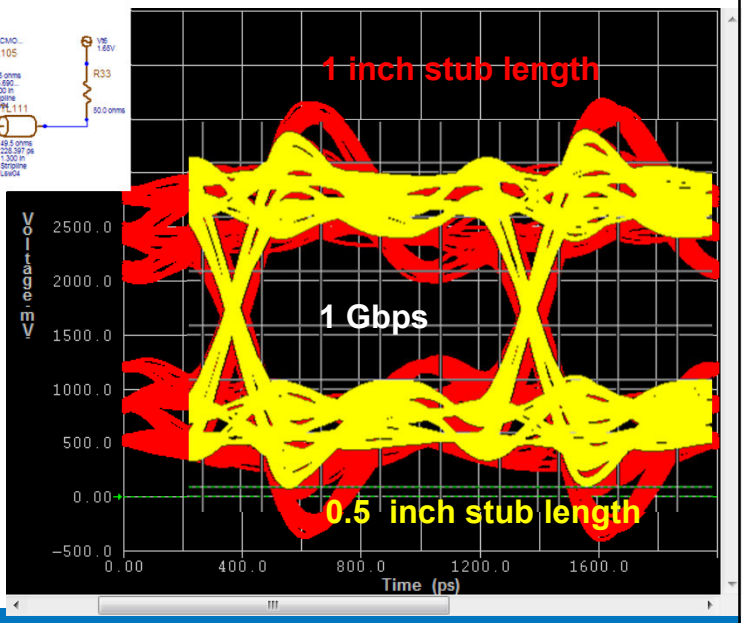




Worst case RX is always the first on the chain

Shorter Stub Length = Higher Possible Data Rate

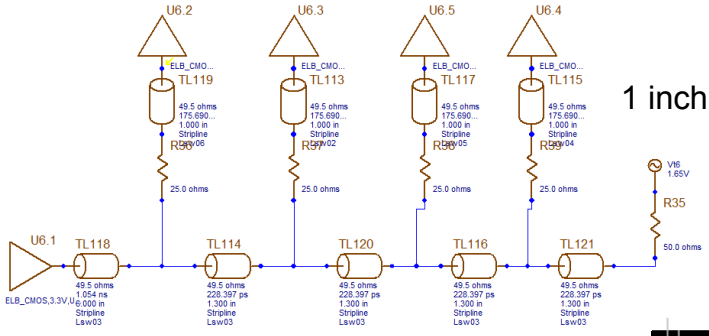




But where are the reflections occurring?

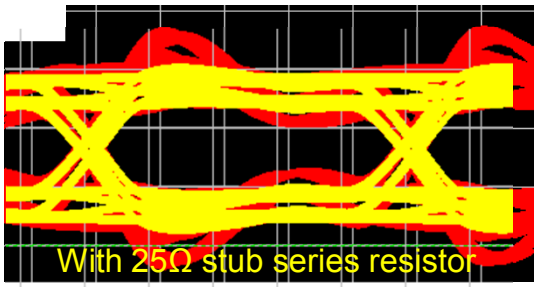
How can they be further reduced?

A Possible Fix: Add a Stub-Series Resistor



1 inch long stubs

No stub series resistor



<u>Selecting resistor value:</u>
R too small, no impact
R too large, rise time degradation at RX
Optimum value ~ 25-50 Ohms
Depends on stub length, trunk lengths, input gate capacitance

Routing Design Features to Enable Higher Data Rate

- Only point to point routing topology supports a data rate > 2 Gbps
- #1 design guideline to increase highest supported data rate:
  - ✓ Reduce branch lengths, everywhere
  - ✓ In tree topology, keep branch lengths equal, far end Vtt termination
  - ✓ Linear route enables shorter branch lengths
  - ✓ Minimum length termination stubs (flyby termination)
- Trick:
  - ✓ Stub series resistor
  - ✓ Terminate both ends in bi-directional buses
  - ✓ There are often multiple right answers
- Will a specific routing, termination strategy work at a specific data rate?
- "it depends"
  - ✓ RT of driver (shortest), Driver output impedance (lowest), Input gate capacitance (smallest)
  - ✓ Z0 (controlled)
  - ✓ Routing topology (linear)
  - ✓ Stub length (shortest)
  - ✓ Distribution of stub lengths (all the same)
  - ✓ Termination topology (far end, source?)
  - ✓ Other discontinuities (short, matched to the line Z0)
- ***Only point to point routing topology supports a data rate > 2 Gbps***

Will it work? Simulate to find out

Lesson EPSI-04-50 Input Gate Capacitance

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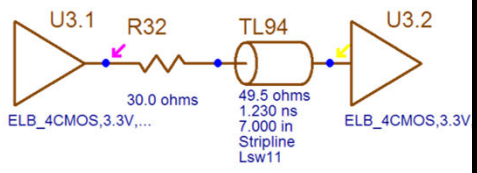
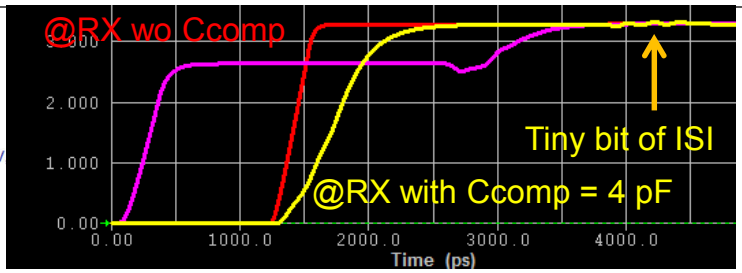
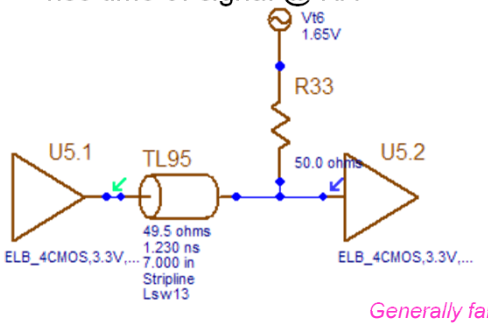
- EPSI-04-50: recorded live, Dec 1, 2013
  - Input gate capacitance- the most important property of the RX
  - Measuring the input gate capacitance of the receiver
  - Impact of termination and rise time at the RX from input gate capacitance
  - Why source series termination is sometimes not capable of as high a data rate as far end termination

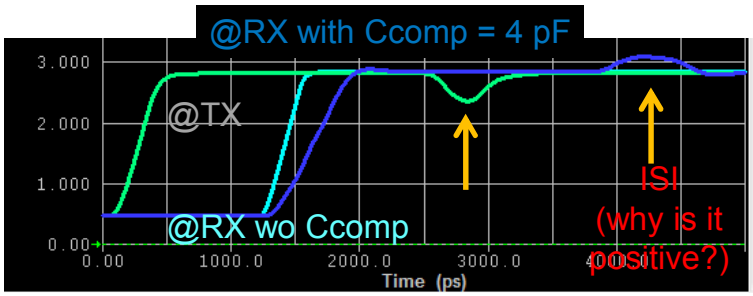
Impact from Input Capacitance and Termination Strategy



Impact of Ccomp is to increase rise time of signal @ RX



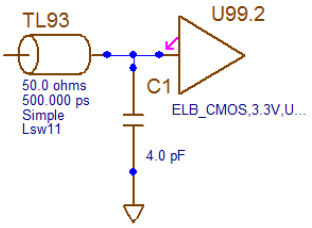


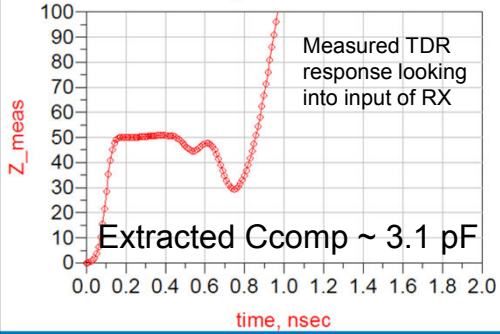


Generally far end termination results in slightly faster edge @RX and high possible data rate

Input Gate Capacitance of RX: Ccomp

Real RX really behaves like:






```
|*************************************************
[MODEL] Buffer1
|
Model_type          3-state
Polarity            Non-Inverting
Enable              Active-High
Vinl =    0.8V
Vinh =    2.0V
C_comp              3.32pF              3.69pF              2.96pF
|
```

Typical values range from 1 pF to 8 pF

Depends on ESD protection diodes and I/O pad size and gate capacitance

So what?

Lesson EPSI-04-60 Discontinuities

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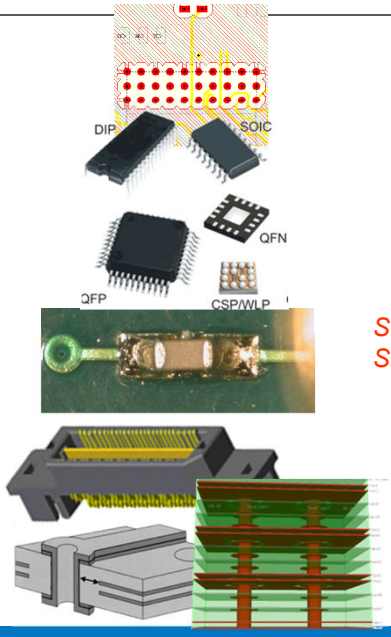
- EPSI-04-60: recorded live, Dec 1, 2013
  - Two types of discontinuities
  - Return path discontinuities and stubs are the worst
  - The five most important steps in reducing the impact form discontinuities
  - Modeling a discontinuity as a transmission line
  - Shorter is always better

Two Types of Discontinuities

Continuous return path
Linear route topology

- Neck down, corners
- DC blocking cap
- Some connectors
- IC packages
- Thru vias (with return vias)
- Corners
- Serpentines



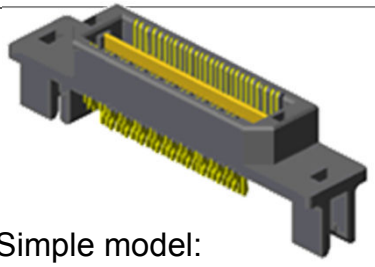
Screwed up return path (RPD)
Stub topology

- Gaps in planes
- Test points
- Termination, routing stubs
- Via stubs
- Some connectors
- Some vias

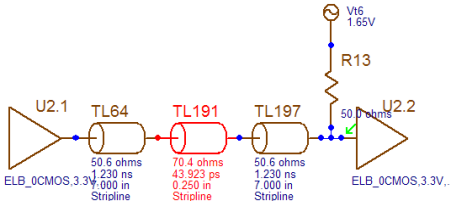
Five Most Important Design Principles for Discontinuities

1. Try to simulate the reflection noise using simple transmission line models to get a quick, 1st order estimate of impact
2. If TD << RT, discontinuity may be transparent- don't worry about it! Move on to more important problems
3. Keep stub lengths short
4. Consider adding "relief anti-pad" under large surface pads
5. Avoid return path discontinuities (RPD)

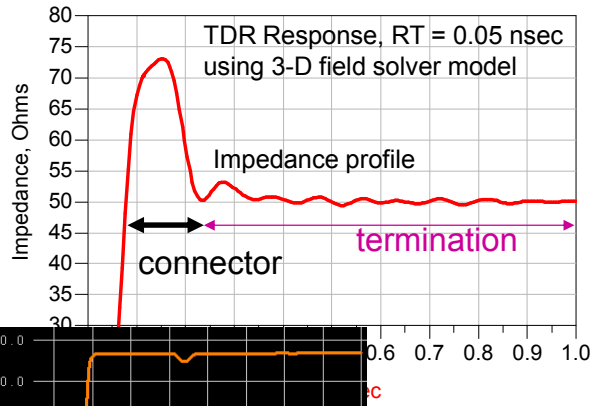
Approximate Most Connectors as a Transmission Line

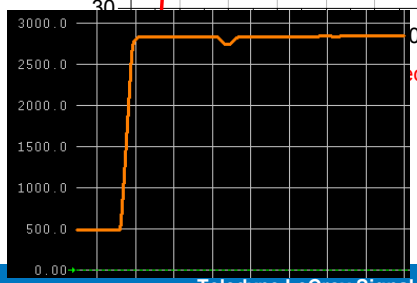


Simple model:
Z_0 = 73 Ohms
TD = 0.06 nsec
Len ~ 0.36 inches



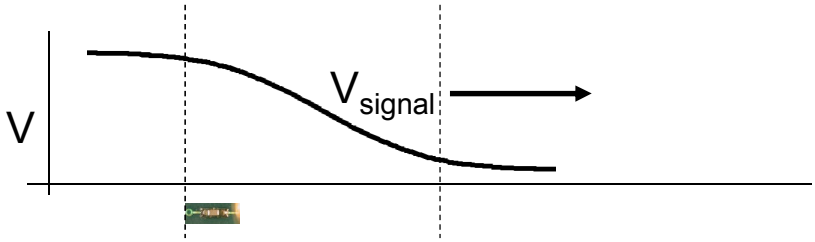
Pad stack on board may compensate for pin impedance





Signal @ RX
for RT = 0.3 nsec

How Short is Short Enough?



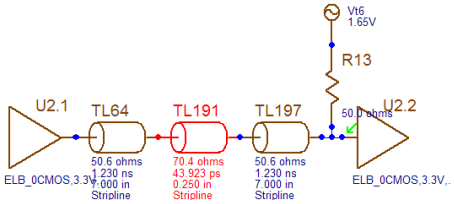
If TD << RT, discontinuity may be transparent- don't worry about it! Move on to more important problems

Len < ~ 1/10th λ $\quad \lambda[cm] = \frac{15cm/nsec}{BW} = \frac{15cm/nsec}{0.35} RT = 43 \times RT[nsec]$

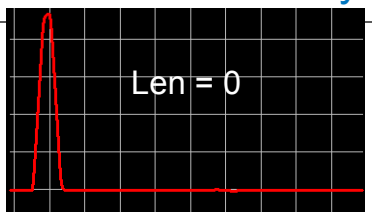
$$Len[cm] < \frac{1}{10} 43 \times RT[nsec] \sim 4 \times RT[nsec]$$

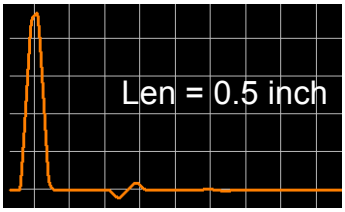
For RT = 0.3 nsec, Len < 1 cm ~ ½ inch

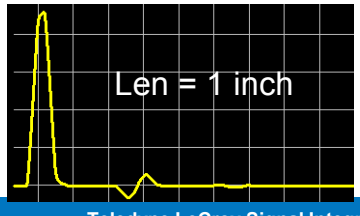
Impact from a Series Connector Discontinuity

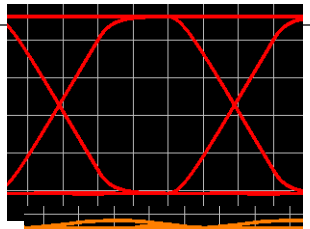


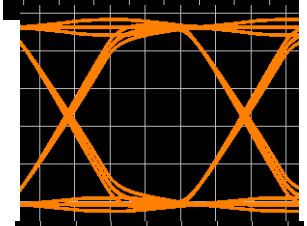
@ RX,
RT = 0.3 nsec
@ 2 Gbps

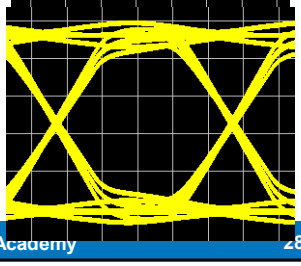








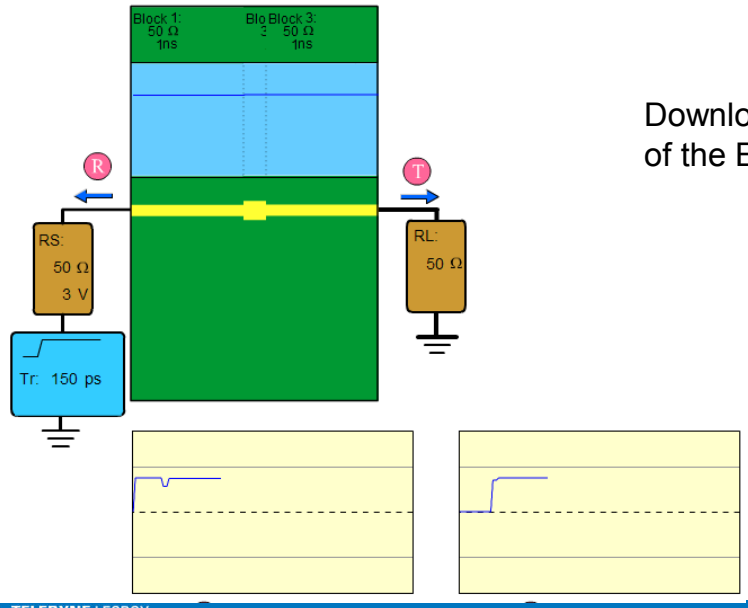




Connectors can be pretty transparent if kept short

Long connectors can pose problems

Explore Length-Rise Time Trade Offs With The Teledyne LeCroy Reflection app



Download this free app from section 3 of the EPSI online course

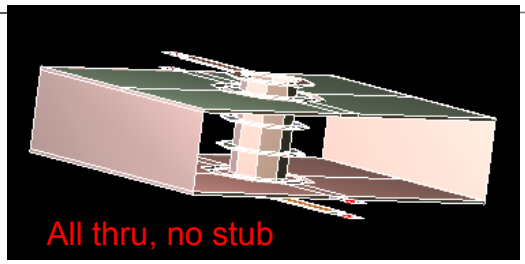
Lesson EPSI-04-70 Vias and stubs

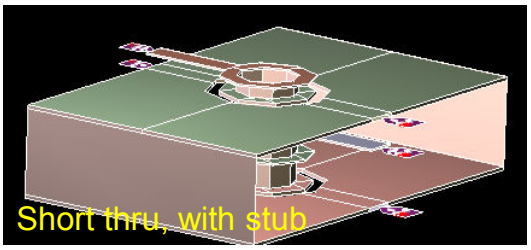
Course EPSI: Essential Principles of Signal Integrity

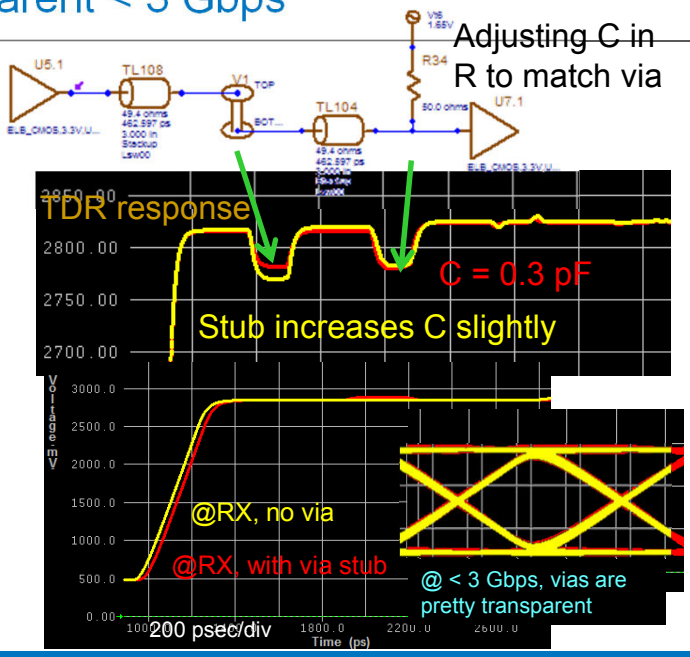
With Eric Bogatin,
Signal Integrity Evangelist, Teledyne LeCroy Front Range Signal Integrity Lab
Dean, Teledyne LeCroy Signal Integrity Academy
Adjunct Professor, University of Colorado, Boulder, ECEE

- EPSI-04-70: recorded live, Dec 1, 2013
  - Vias can be transparent if they are short enough
  - Optimizing the impedance of a via by tuning the clearance hole diameter
  - The quarter wave stub resonant frequency
  - Stub length as a limitation to the highest data rate in the channel

Vias Are Generally Transparent < 3 Gbps

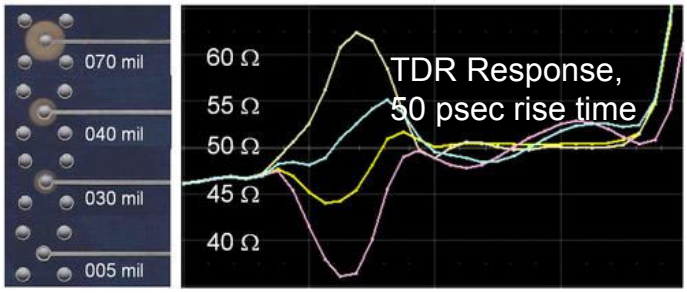


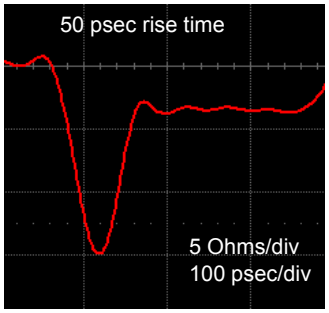




But if you want to worry about vias….
Optimize Via Impedance By Adjusting Clearance Hole Diameter

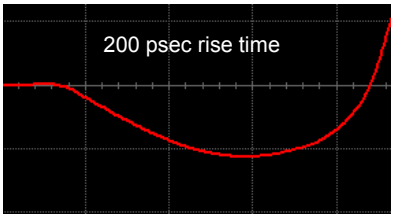
Different hole diameter





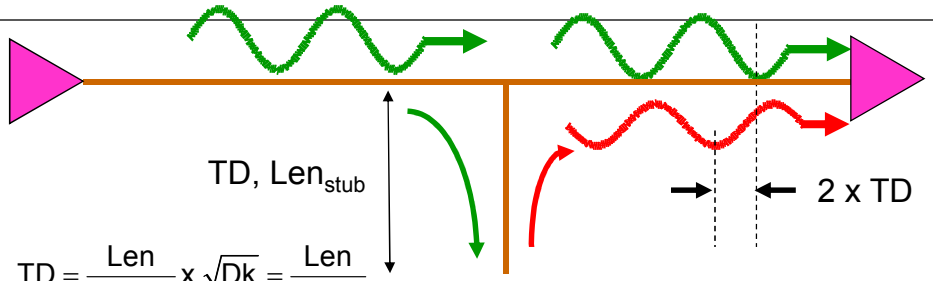
- Optimized clearance hole size depends on:
  - Capture pads
  - NFP
  - Barrel diameter
  - Number of layers in the board
  - Board stack up
  - Thickness of dielectric

@ RT > 200 psec, via is pretty transparent



Generally bigger impact from the via stub

The ¼ Wave Stub Resonance



Stubs from
- Routing stubs
- Package plating stubs
- Test lead stub
- Vias

$$TD = \frac{Len}{12\,^{in}/_{nsec}} \times \sqrt{Dk} = \frac{Len}{6\,^{in}/_{nsec}}$$

When 2 x TD = ½ cycle, minimum received signal
TD = ¼ cycle: the quarter wave resonance

$$TD = \frac{1}{4}\frac{1}{f_{res}}$$

$$f_{res}[GHz] = \frac{1}{4}\frac{1}{TD[nsec]} = \frac{1.5}{Len[inches]}$$

Example: Len = 0.5 inch, f_{res} = 3 GHz

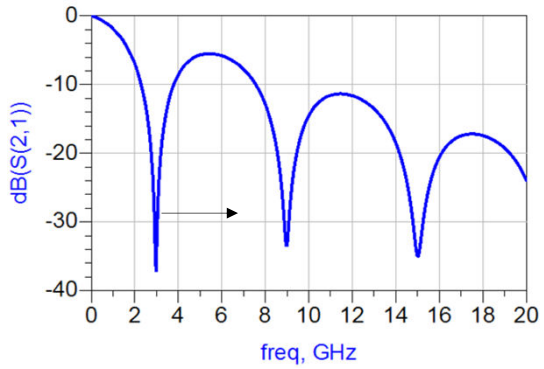
How Short Should Stubs Be? (worst case, low loss channel)

engineer f_{res} > 2 x BW of signal (@TX)

$$f_{res} = \frac{1.5}{Len} > 2 \times BW = 2 \times 5 \times \frac{1}{2}BR$$

$$\frac{1.5}{Len} > 10 \times \frac{1}{2}BR = 5 \times BR$$

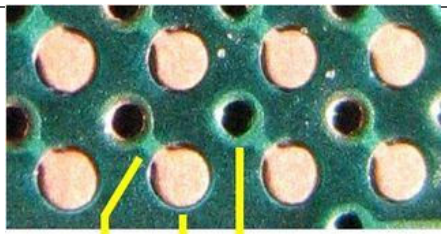
$$Len[inches] < \frac{1.5}{5 \times BR} = \frac{0.3}{BR[Gbps]}$$

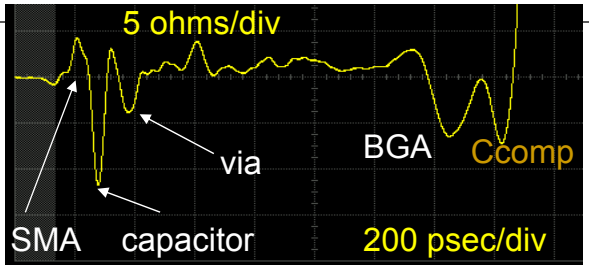


BR = 2.5 Gbps, Stub length < 0.12 inches
BR = 5 Gbps, Stub length < 0.06 inches
BR = 10 Gbps, Stub length < 0.03 inches

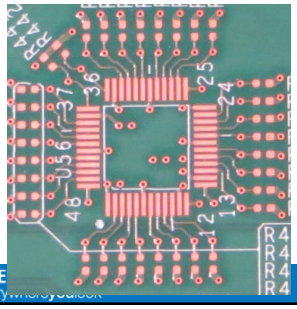
Routing stubs limit highest data rate a channel will support
ONLY point to point routing topology is possible for > 2 Gbps

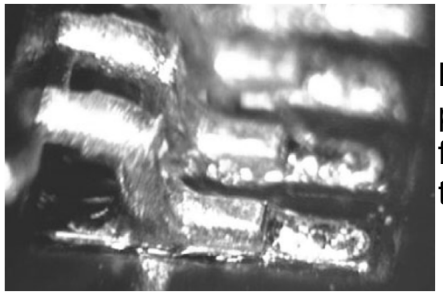
Impact from Package Attach Pad





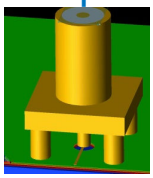
Measured TDR response looking into pkg

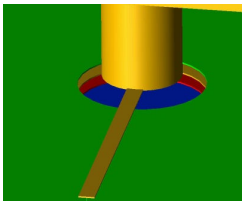




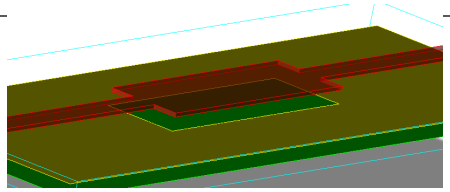
Biggest impact from a package typically is from mounting pads on the board: ~ 1-3 pF

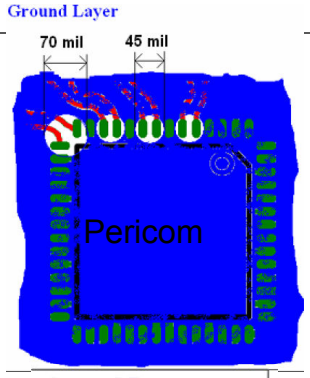
Add Relief Pads in Planes Under SMT Pads to Reduce Capacitance

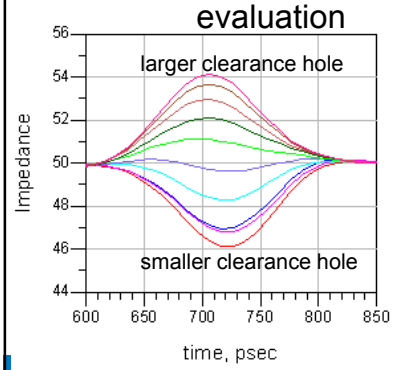


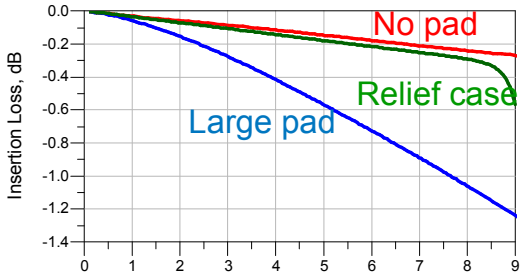


Performance evaluation









Adjust pad size to make pad disappear, or to reduce total input capacitance

Five Most Important Design Principles for Discontinuities

1. Try to simulate the reflection noise using simple transmission line models to get a quick, 1st order estimate of impact
2. If TD << RT, discontinuity may be transparent- don't worry about it! Move on to more important problems
3. Keep stub lengths short
4. Consider adding "relief anti-pad" under large surface pads
5. Avoid return path discontinuities (RPD)