## Lesson EPSI-03-01 Download the pdf file

# Course EPSI:
# Essential Principles of Signal Integrity

With Eric Bogatin,
Signal Integrity Evangelist, Teledyne LeCroy Front Range Signal Integrity Lab
Dean, Teledyne LeCroy Signal Integrity Academy
Adjunct Professor, University of Colorado, Boulder, ECEE

- EPSI-03-01: recorded live, Dec 1, 2013
  - The root cause of reflection noise and how to reduce it
  - Download a copy of the slides



## Lesson EPSI-03-10 How to Think About Reflections

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- EPSI-03-10: recorded live, Dec 1, 2013
  - Uniform lines and propagating signals
  - Reflection and transmission coefficients
  - The impact of reflections
  - It's all about what happens at one interface

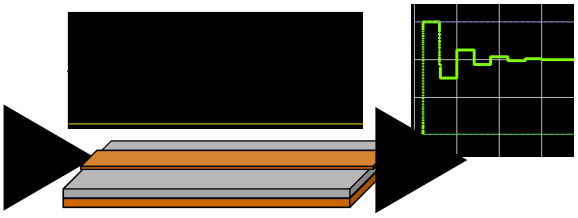
# EPSI: A 2-Day Workshop

- **Day 1**
  - EPSI 1 Transmission Lines
  - EPSI 2 Differential Pairs and Lossy Lines
  - Lunch
  - **EPSI 3 Reflections and Terminations**
  - EPSI 4 Routing Topologies and Discontinuities
- **Day 2**
  - EPSI 5 Eliminating Ground Bounce
  - EPSI 6 Navigating Return Path Discontinuities
  - Lunch
  - EPSI 7 NEXT and FEXT Features
  - EPSI 8 PDN and EMI Design



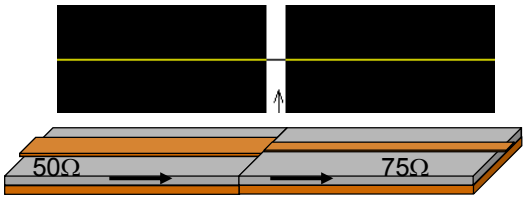
# Essential Principle# 5: Signals Will Reflect Whenever The Instantaneous Impedance Changes

If the instantaneous impedance is constant, the signal continues undistorted.



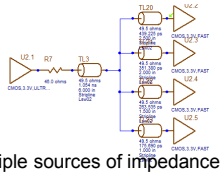
Ringing is caused by multiple reflections from impedance discontinuities at both ends of a line

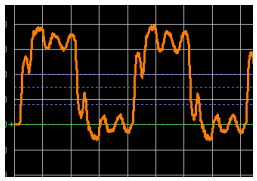
If the instantaneous impedance changes, some of the signal reflects.




$V_{incident}$ $V_{transmitted}$ $t = \frac{V_t}{V_i} = \frac{2 \times Z_2}{Z_2 + Z_1}$

$V_{reflected}$ $\rho = rho = \frac{V_r}{V_i} = \frac{Z_2 - Z_1}{Z_2 + Z_1}$





Multiple sources of impedance discontinuities will create reflections that can rattle around and can dramatically distort the signal

## Lesson EPSI-03-20 Voltage and Current Reflections

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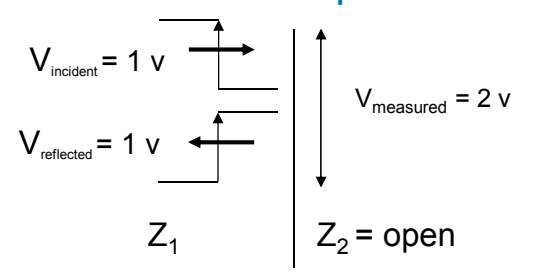
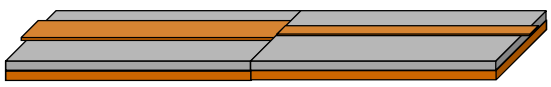
- EPSI-03-20: recorded live, Dec 1, 2013
  - Reflections from opens and shorts
  - What happens to the current in reflections
  - The bounce diagram and keeping track of reflections
  - Why simulation is essential

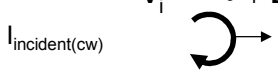


## Exercise The Essential Principles: Reflections at an Open or Short

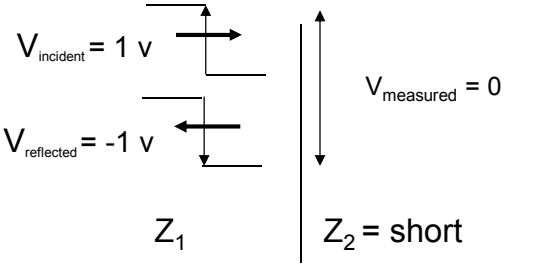


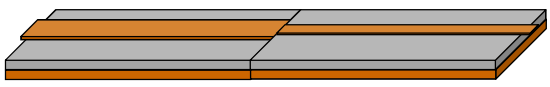



$$\rho = \text{rho} = \frac{V_r}{V_i} = \frac{\infty - Z_1}{\infty + Z_1} = 1$$

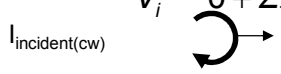




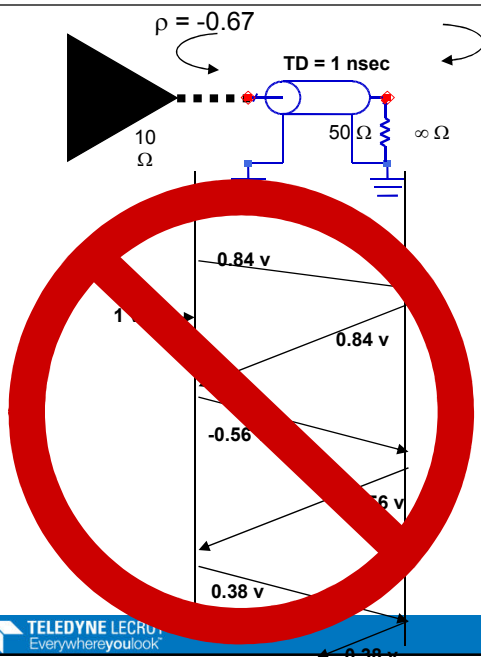


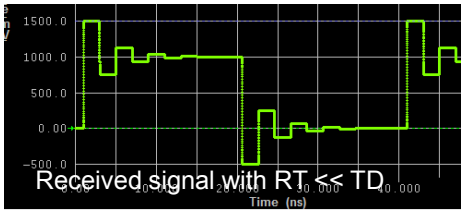



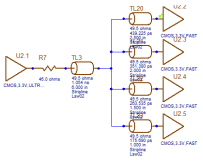
$$\rho = rho = \frac{V_r}{V_i} = \frac{0 - Z_1}{0 + Z_1} = -1$$

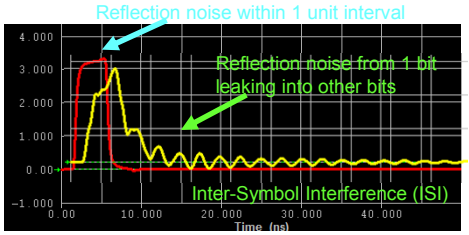



## Predicting Reflection Noise






**Single Bit Response (SBR)**

Circuit simulation is critical to evaluate acceptable designs:
SPICE, QUCS, HyperLynx…
*Rules of thumb, approximations are not good enough.*
ALL the details matter, some more than others



## Lesson EPSI-03-30 Practice safe simulation

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Adjunct Professor, University of Colorado, Boulder, ECEE

- EPSI-03-30: recorded live, Dec 1, 2013
  - Rule #9: How to practice safe simulation
  - A free simulation tool included in the downloaded .zip folder
  - Why it takes 2 reflections to cause problems
  - Impact on reflected and transmitted signal from all the parameters

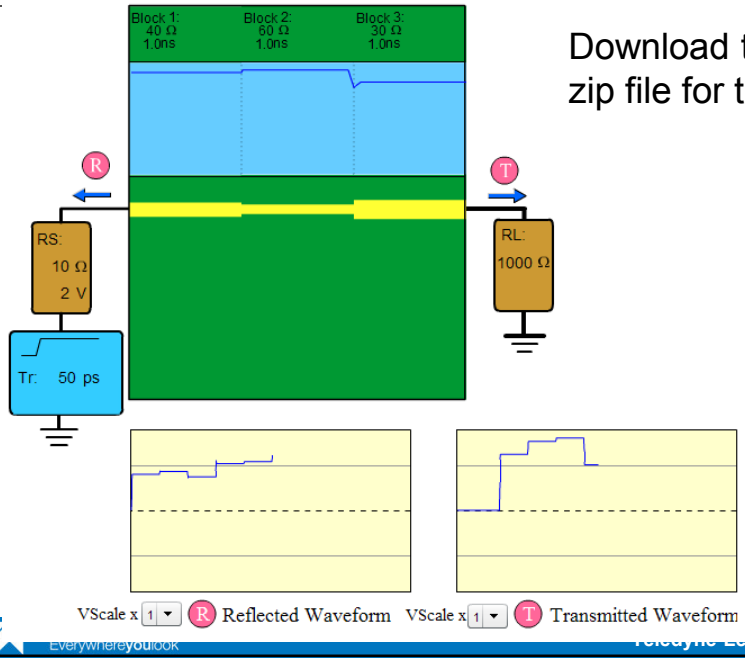
## Practice Safe Simulation

***Rule #9: Never do a measurement or simulation without first anticipating what you expect to see.***

- If you are wrong, there is a reason- either the set up is wrong or your intuition is wrong. Either way, by exploring the difference, you will learn something
- If you are right, you get a nice warm feeling that you understand what is going on.



## Dynamic Simulation of Reflected Signals




Download this free animation tool in the zip file for this lesson

## Lesson EPSI-03-40 Noise margins

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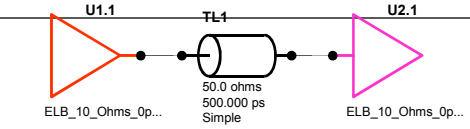
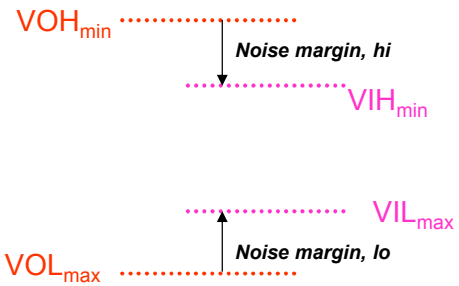
- EPSI-03-40: recorded live, Dec 1, 2013
  - The problem with reflections
  - Noise margins and timing jitter
  - Reflections and inter symbol interference (ISI)
  - Solving reflection problems



## Acceptable Performance: Noise Margins



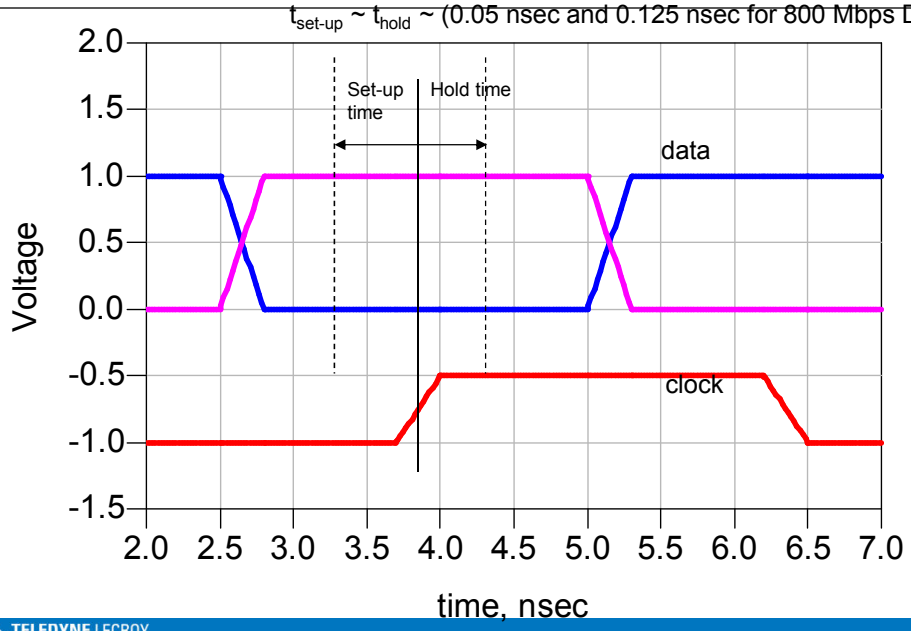

| | VOH | VIH | Margin | VIL | VOL | Margin |
|---|---|---|---|---|---|---|
| TTL [5volt] | 2.4V | 2.0V | 400mV | 0.8v | 0.5v | 300mV |
| FCT [5volt] | 2.5V | 2.0V | 500mV | 0.8v | 0.5v | 300mV |
| BTL [5 volt] | 2.1V | 1.62V | 480mV | 1.47v | 1.1v | 370mV |
| GTL [5 volt] | 1.5V | 1.05V | 450mV | 0.95v | 0.55v | 400mV |
| CMOS [5 volt] | 4.9V | 3.85V | 1050mV | 1.35v | 0.1 | 1340mV |
| LVTTL [3volt] | 2.4V | 2.0V | 400mV | 0.8v | 0.4v | 400mV |
| LVCMOS [3 volt] | 2.8V | 2.0V | 800mV | 0.8v | 0.2v | 600mV |
| CMOS [2.5V] | 2.0V | 1.7V | 300mV | 0.7v | 0.4v | 300mV |
| CMOS [1.8V] | 1.35V | 1.1V | 250mV | 0.66v | 0.45v | 210mV |

For 5 V CMOS, noise margin-hi/lo ~ 1/5 ~ 20%
For 2.5 V CMOS, noise margin-hi/lo ~ 0.3/2 ~ 15%
For 1.8 V CMOS, noise margin-hi/lo ~ 0.25/1.35 ~ 18%

*Typical noise margin for single-ended CMOS technology ~ 15% of signal swing*
*Noise budget allocation: ~ 1/3 to reflection noise, ~1/3 to xtk, ~1/3 to PDN noise*

## Acceptable Performance: Timing Margin for "Valid" Level

$t_{set\text{-}up}$ ~ $t_{hold}$ ~ (0.05 nsec and 0.125 nsec for 800 Mbps DDR2)




Data @RX must be "valid" within setup and hold interval

Clock to data skew, jitter, decrease timing margins on both sides

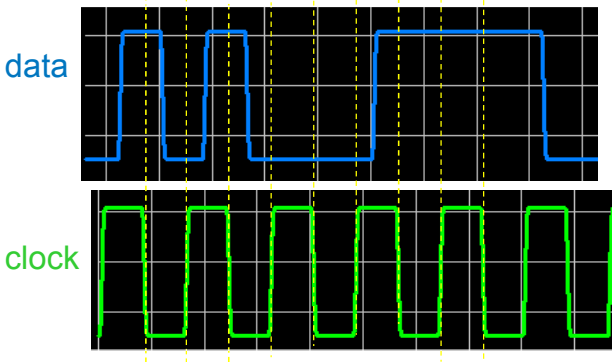
*At 1 Gbps, UI = 1 nsec, time when level needs to be valid: ~ 40% of UI*
*jitter can be ~30% on each edge*



## The Eye Diagram:

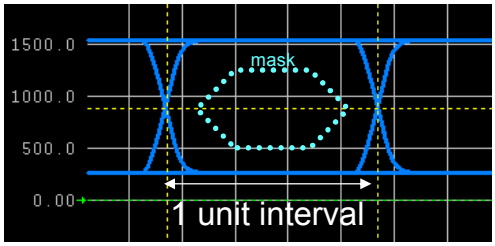
### The Most Important FINAL Metric of Performance

A Pseudo Random Bit Sequence (PRBS)
(all possible combinations of bit patterns)




A synchronous clock
2 bits per clock (double data rate)
Data read edge-triggered

Take every 2 bits,
Align synchronous with the clock
Superimpose: The Eye Diagram




If ALL RX voltage is outside the mask, bit error rate will be acceptable

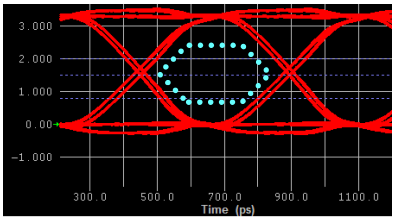
If any signal "violates" the mask, there may be a bit error

Vertical collapse: noise margin (noise)
Horizontal collapse: timing margin (jitter)

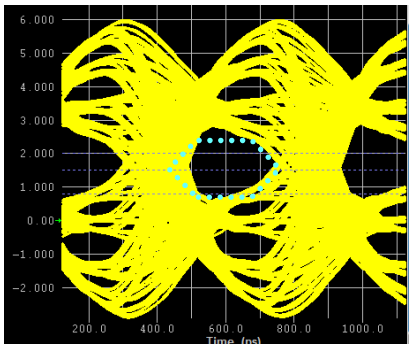
## The Problem: Mask Violations (collapse of the eye)

@ 2.5 Gbps

good




bad




- The process to "get it right the 1st time":
  - Identify the problem: collapse of the eye
  - Find the root cause: why do eyes go bad?
  - Turn root cause into practical design guidelines
  - Understand the "essential principles" of how physical design affects signal performance
  - Evaluate tradeoffs with analysis tools as early in the design process as possible



## Lesson EPSI-03-50 Four sources of reflections

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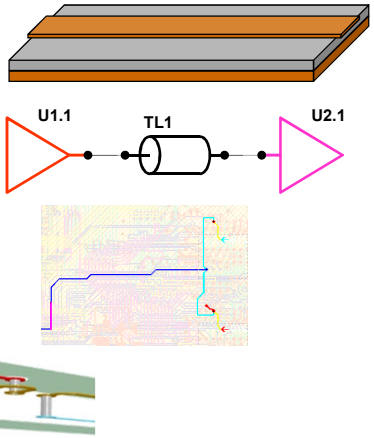
- EPSI-03-50: recorded live, Dec 1, 2013
  - Applying the Youngman Principle to reduce reflection noise
  - The four sources of reflection noise
  - Non-uniform lines, ends, routing topology, discontinuities
  - Uniform transmission lines and 2D field solvers

# Applying the Youngman Principle:
## Turn root cause into best design practices

- Reflections can cause signal distortion and collapse of the eye.
- If the root cause of reflections is changes in the instantaneous impedance, what general guideline do we follow to eliminate reflection noise?
  - Keep the instantaneous impedance the signal sees constant
- Four typical situations to engineer:

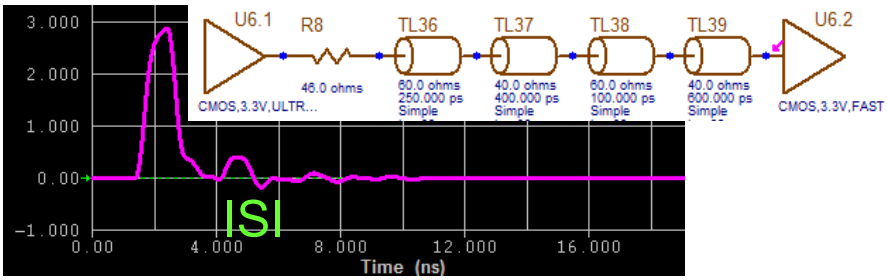
1. Problem: non-uniformity of the transmission lines
   - *Solution: use controlled impedance lines*
2. Problem: the ends of the lines
   - *Solution: use a termination strategy*
3. Problem: routing topology
   - *Solution: use a linear route, keep branches short*
4. Problem: discontinuities
   - *Solution: keep them short, match to line impedance*



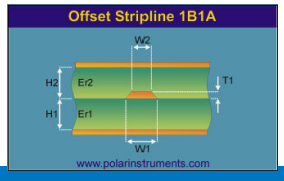



# Practical Design Guideline:
## 1. Use Controlled Impedance Lines

- Example: four different uniform segments: 40 Ω - 60 Ω




- Solution: Adjust cross section of each segment to hit target impedance (use 2D field solver)




## Lesson EPSI-03-60 Termination topologies

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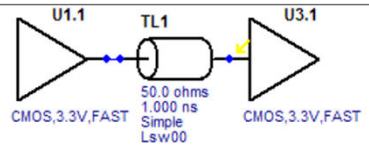
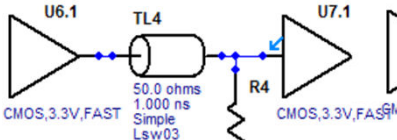
- EPSI-03-60: recorded live, Dec 1, 2013
  - Terminations to prevent reflections
  - Source series terminations
  - Far end termination
  - What's the problem with far end terminations



## Practical Design Guideline: Two General Termination Strategies

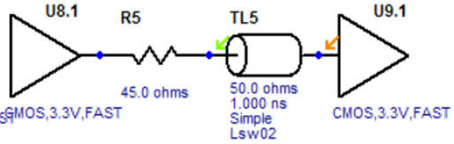



No termination



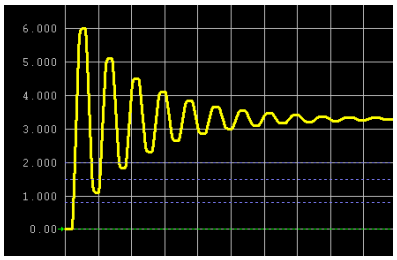

Far end parallel termination

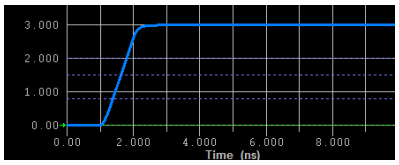
$R_{term}$ = Z0

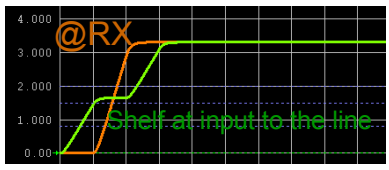


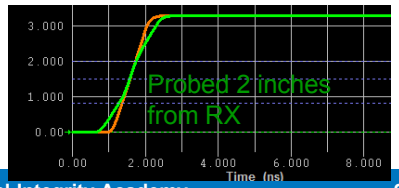

Source series termination

$R_{source}$ = Z0 - $Z_{driver}$



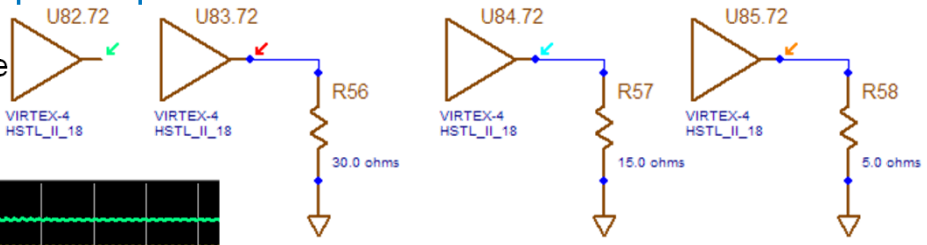



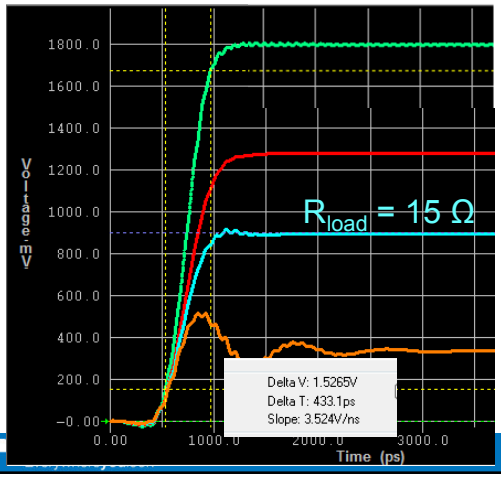



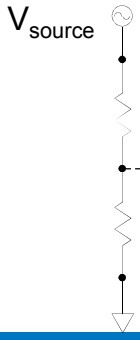

***For point to point, all have equivalent signal quality***

## Two Important Properties of EVERY Driver: Rise Time, Output Impedance

10-90 Rise Time
Output impedance



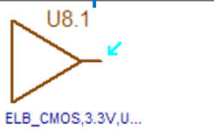



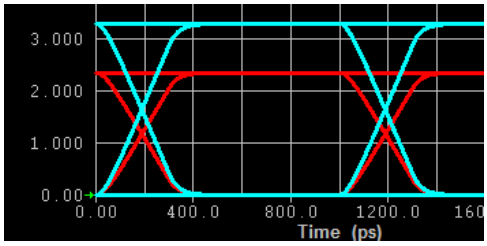

$$V_{out} = V_{source} \frac{R_{load}}{R_{source} + R_{load}}$$

When $V_{out}$ = ½ $V_{source}$,
$R_{source}$ = $R_{load}$

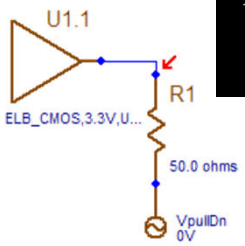


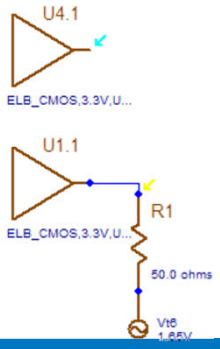
## Decision #1: Received Signal Swing Due to Finite Output Impedance

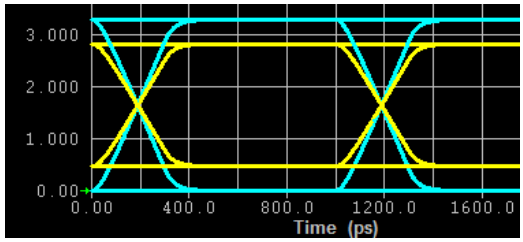



Losing voltage noise margin
Drop ~ output impedance of driver




How to modify far end termination to provide voltage offset?

## Lesson EPSI-03-70 Balancing Power and Signal Quality

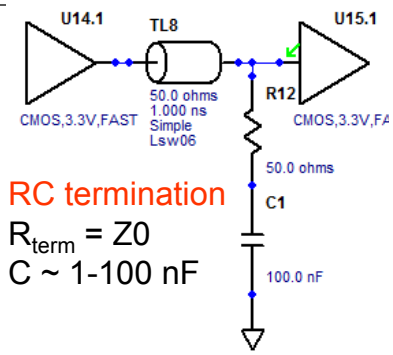
# Course EPSI: Essential Principles of Signal Integrity

With Eric Bogatin,
Signal Integrity Evangelist, Teledyne LeCroy Front Range Signal Integrity Lab
Dean, Teledyne LeCroy Signal Integrity Academy
Adjunct Professor, University of Colorado, Boulder, ECEE

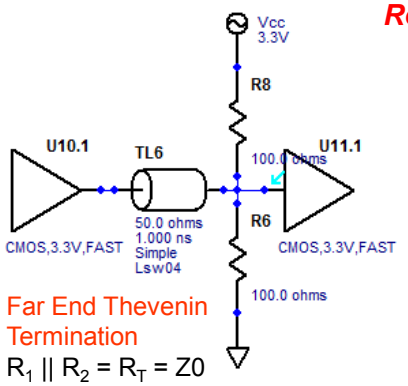
- EPSI-03-70: recorded live, Dec 1, 2013
  - RC, thevenin and Vtt termination
  - Estimating power dissipation in different terminations
  - Surprising differences in power dissipation
  - Limitations with RC terminations and why clocks are best



## Three Other Variations of Far End Termination

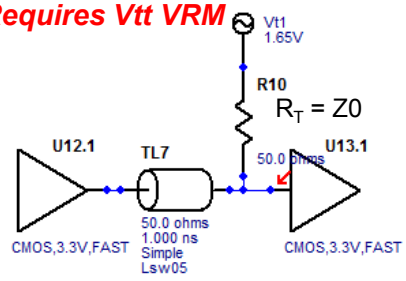



RC termination
$R_{term}$ = Z0
C ~ 1-100 nF

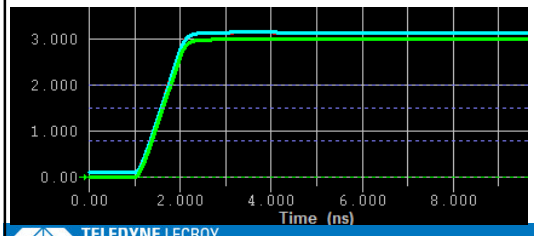



Far End Thevenin Termination
$R_1 \parallel R_2 = R_T$ = Z0

***Requires Vtt VRM***




Vtt Termination



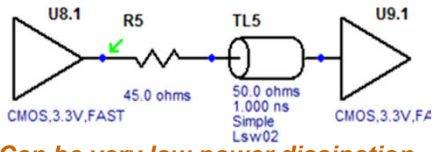

For point to point, all have equivalent signal quality.

Key feature of these approaches: centers signal about ½ Vcc

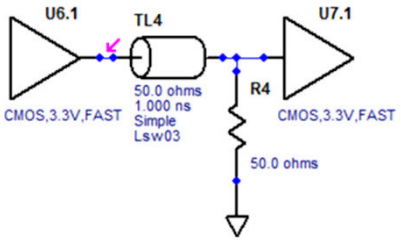
How do we decide which ones to use, when?

## Decision #2: Power Consumption

- Power is consumed in resistors: $\langle P \rangle = \frac{1}{2}\left(\frac{\Delta V_{lo}^{\ 2}}{R} + \frac{\Delta V_{hi}^{\ 2}}{R}\right)$ $\langle P \rangle = \frac{1}{2}\left(I_{lo}^{\ 2}R + I_{hi}^{\ 2}R\right)$




***Can be very low power dissipation. If you live for low power, source series termination should be your first choice***



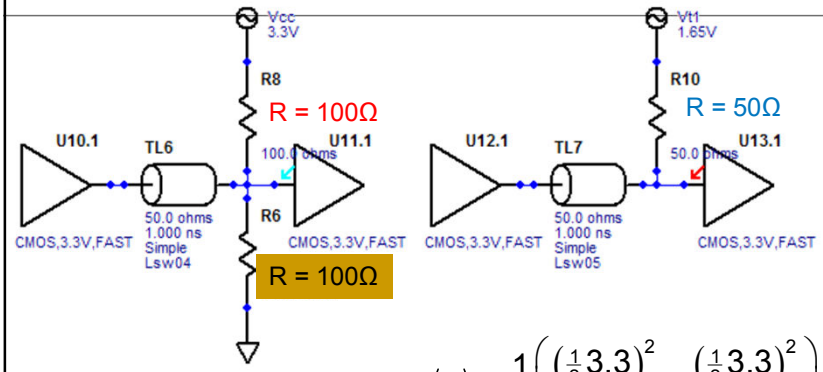


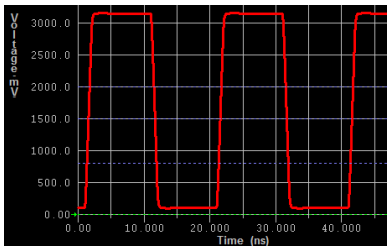
*Much less power if << 50% duty cycle, or >> 50% duty cycle and Vcc termination*

Power consumed by far end termination (50% duty cycle) = $\langle P \rangle = \frac{1}{2}\left(\frac{0^2}{50} + \frac{3.3^2}{50}\right) = 100\text{mW}$



## Power Consumed in Other Far End Terminations



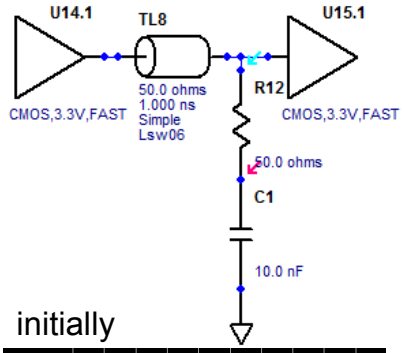

$\langle P \rangle = \frac{1}{2}\left(\frac{\Delta V_{lo}^{\ 2}}{R} + \frac{\Delta V_{hi}^{\ 2}}{R}\right)$

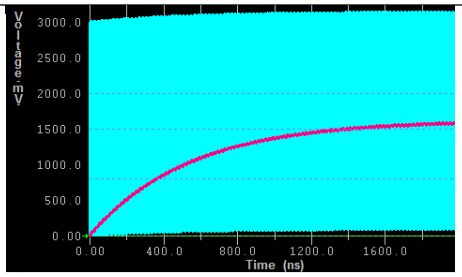
$\langle P \rangle = \frac{1}{2}\left(\frac{\left(\frac{1}{2}3.3\right)^2}{50} + \frac{\left(\frac{1}{2}3.3\right)^2}{50}\right) = 50\text{mW}$

$\langle P \rangle = \frac{1}{2}\left(\frac{3.3^2}{100} + \frac{3.3^2}{100}\right) = 100\text{mW}$

***Vtt termination consumes half the power as Thevenin far end!***
***(another reason it is preferred- what is the "cost"?)***

## Power Consumed in RC



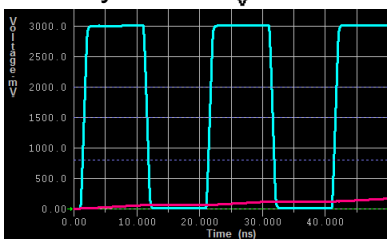




Voltage across capacitor "charges up"

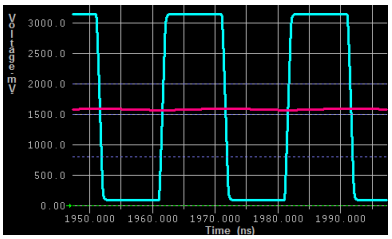
Signal not centered @RX initially

$$\langle P \rangle = \frac{1}{2}\left( \frac{\Delta V_{lo}^{\ 2}}{R} + \frac{\Delta V_{hi}^{\ 2}}{R} \right)$$

initially




A few time constants later ~ 50 x 10 nF ~ 1000 nsec




$$\langle P \rangle = \frac{1}{2}\left( \frac{\left(\frac{1}{2}3.3\right)^2}{50} + \frac{\left(\frac{1}{2}3.3\right)^2}{50} \right) = 50\text{mW}$$

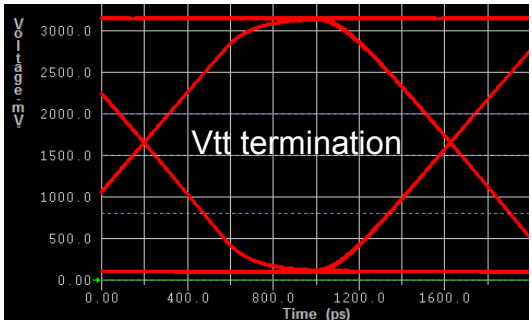
*Power consumed in RC termination is ½ as much as far-end single-resistor*

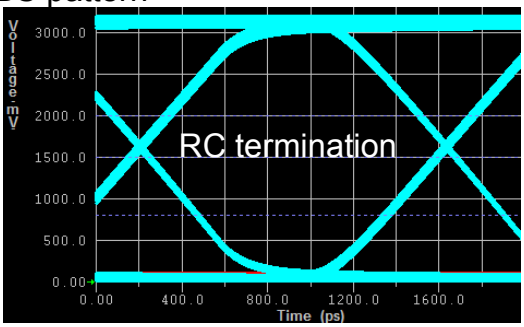


## Limitation with RC Termination

- Power dissipation advantage for 50% duty cycle
  - Less advantage with non 50% duty cycles
- Some data dependent jitter
  - Most suitable for clocks: with 50% duty cycle
  - Will have a turn on time for centered signal @RX
  - Might be ok for other data nets if jitter is acceptable (need to do PRBS simulation)

700 Mbps PRBS pattern



## Lesson EPSI-03-80 Flyby Termination

# Course EPSI: Essential Principles of Signal Integrity

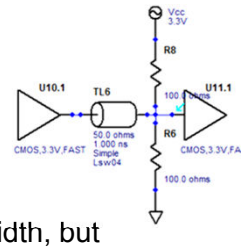
With Eric Bogatin,
Signal Integrity Evangelist, Teledyne LeCroy Front Range Signal Integrity Lab
Dean, Teledyne LeCroy Signal Integrity Academy
Adjunct Professor, University of Colorado, Boulder, ECEE

- EPSI-03-80: recorded live, Dec 1, 2013
  - Where to place the terminating resistor
  - How to minimize the termination stub
  - Flyby termination
  - Limitations with RC terminations and why clocks are best

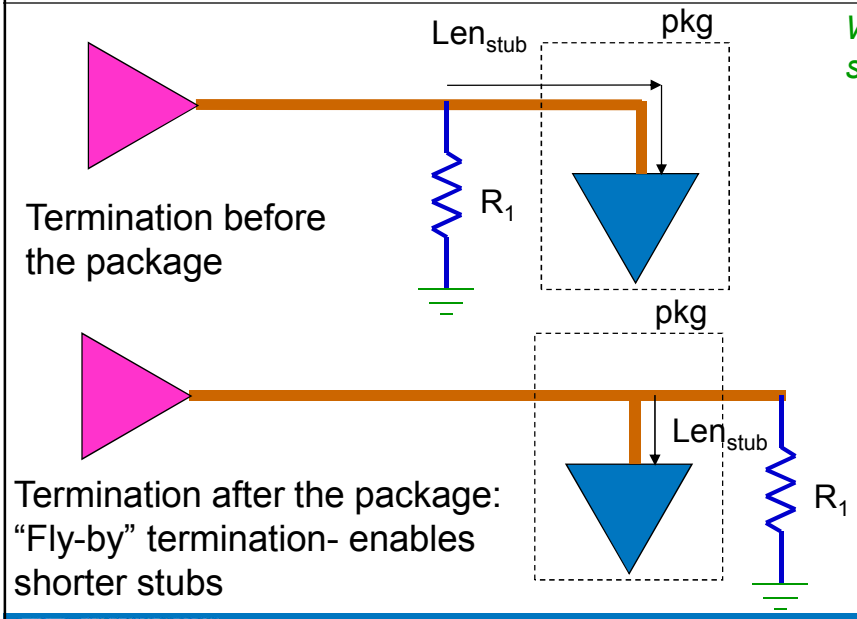


## Which Termination to Use?

- Often times many "correct" answers
- If power is most important
  - source series termination
- If a clock net, lowest power, and minimum complexity:
  - RC termination
- If low duty cycle control line, mostly lo or mostly hi, lowest power if:
  - Far end termination to Vss or Vcc
- For reduced ground bounce @termination:
  - Provide connection to each plane used in the return path
- Good balance between: lower power, higher noise margin, higher bandwidth, but higher cost:
  - Far end Vtt termination
- …but for the highest data rate:
  - It's the routing topology that sets the maximum supported data rate, not the termination strategy
  - You cannot "terminate away" reflections from poor routing topologies

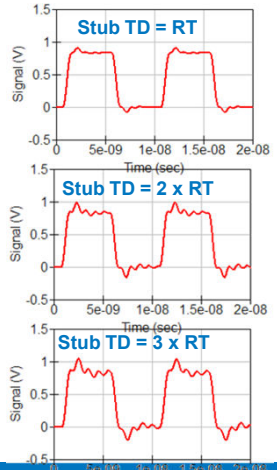


# Where Should the Far End Resistor Go? Does it Matter?



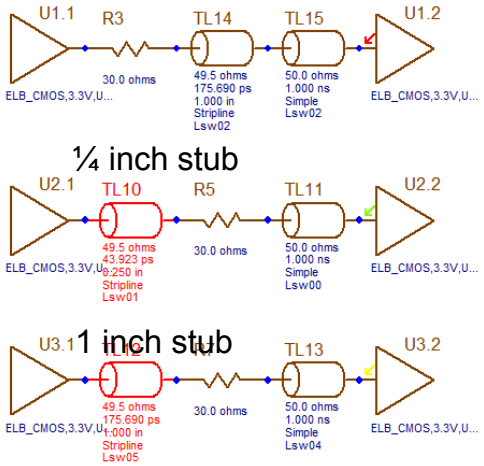

*Which topology has shorter stub and higher BW?*

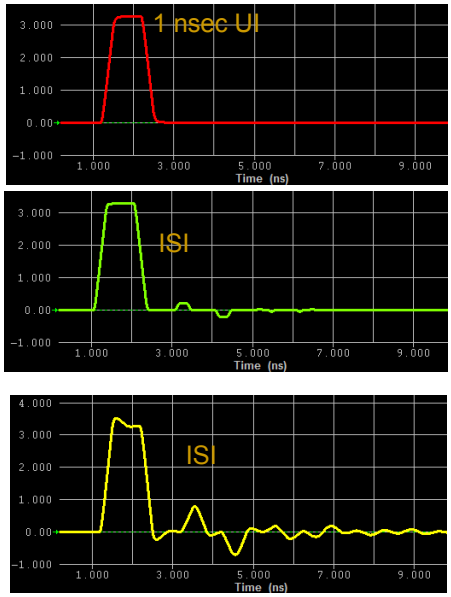
**Use the topology that enables the shortest termination stub length**






# Termination Stub in Source Series Termination

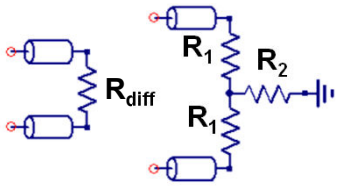



Place terminating resistor as close to Tx I/O pad as possible

## Terminating BOTH the Differential and Common Signals

Tee termination topology




**For differential signals**

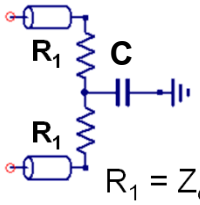
$Z_{diff} = R_{equiv} = 2\ R_1 = 2 \times Z_{odd}$ $\quad R_1 = Z_{odd}$

**Common signals:**

$Z_{comm} = R_{equiv} = ½\ R_1 + R_2 = ½\ Z_{even}$

$R_2 = ½\ (Z_{even} - Z_{odd})$

Typical implementation: RC termination



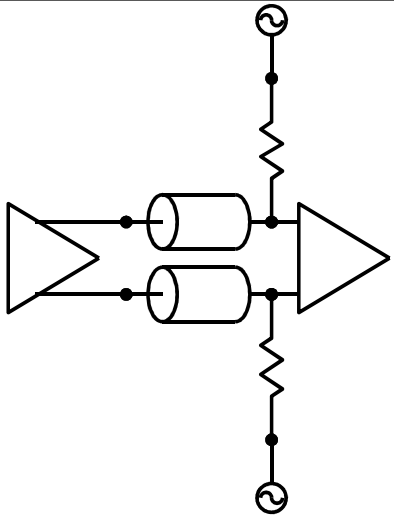

$R_1 = Z_{odd}$

$R_2 = ½\ (Z_{even} - Z_{odd}) \sim 0$

No DC power dissipation
Adds extra component to board- never ideal R, C
Difficult to do on die
C typically 1-100 nF



## Alternatively: Terminate as Single Ended Lines



Far end, Vtt termination of each line

Terminates both differential signal and common signal

Can be done on-die for shortest termination stub length




## Rule #9: Never do a measurement or simulation without first anticipating what you expect to see.

If you are wrong, there is a reason- either the set up is wrong or your intuition is wrong. Either way, by exploring the difference, you will learn something

If you are right, you get a nice warm feeling that you understand what is going on.