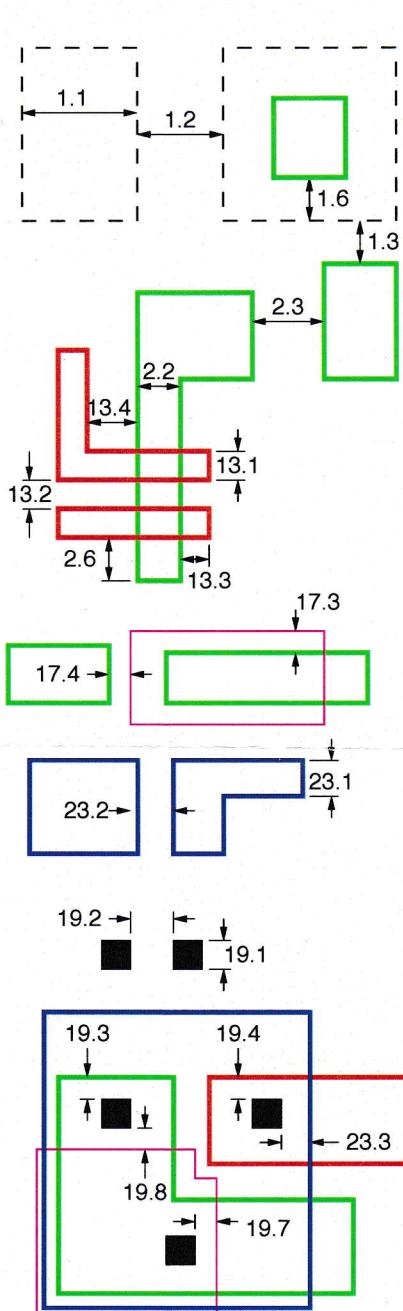


ELEC3221 Sample Design Rules

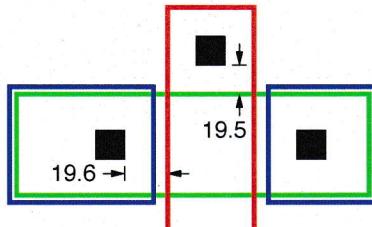
Suitable for ICD Exam Question Handout #2

Simplified Design Rules for a 0.4um CMOS process



Design Rule	Distance (microns)
N-well	
1.1 Minimum n-well width	2.4
1.2 Minimum n-well spacing	1.2
1.3 Minimum n-well spacing to active area	1.2
1.6 Minimum n-well enclosure of active area	1.2
Active Area	
2.2 Minimum active area width	0.6
2.3 Minimum active area spacing	0.8
2.6 Minimum source/drain length	0.6
Polysilicon	
13.1 Minimum polysilicon width	0.4
13.2 Minimum polysilicon spacing	0.6
13.3 Minimum polysilicon extension beyond gate	0.6
13.4 Minimum polysilicon spacing to active area	0.2
P implant	
17.3 Minimum p implant enclosure of active area	0.4
17.4 Minimum p implant spacing to active area	0.4
Metal 1	
23.1 Minimum metal 1 width	0.6
23.2 Minimum metal 1 spacing	0.6
Contact Window	
19.1 Minimum/maximum contact dimension	0.4
19.2 Minimum contact spacing	0.6
19.3 Minimum active area enclosure of contact	0.3
19.4 Minimum polysilicon enclosure of contact	0.3
19.7 Minimum p implant enclosure of contact	0.2
19.8 Minimum p implant spacing to contact	0.2
23.3 Minimum metal 1 enclosure of contact	0.2
19.5 Minimum polysilicon contact spacing to active area	0.4
19.6 Minimum active area contact spacing to polysilicon gate	0.4

* This is not a complete set of design rules but is sufficient for most simple cell designs *

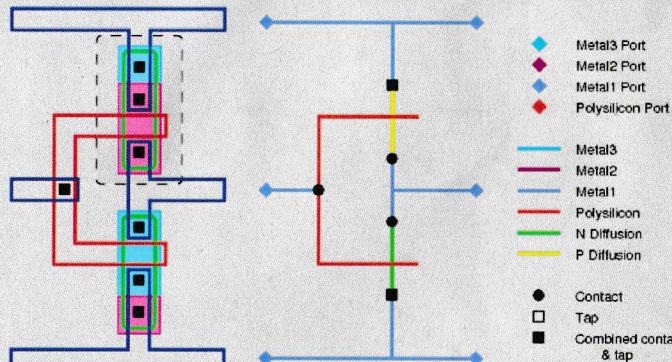


Selected Electrical Parameters

Ω/\square
Sheet resistance of Metal
Sheet resistance of Polysilicon – Low Ohmic (silicided)
– High Ohmic (unsilicided)
Sheet resistance of P Diffusion
Sheet resistance of N Diffusion

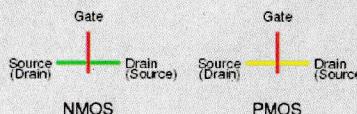
Drawing Stick Diagrams

- Mask Layout and Stick Diagram for a CMOS Inverter



- Transistors

A transistor exists where a polysilicon stick crosses either an N diffusion stick (NMOS transistor) or a P diffusion stick (PMOS transistor).

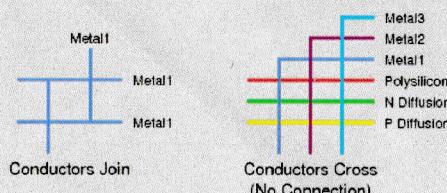


Note that there is no difference in the construction of a transistor source and a transistor drain. The source is determined as the source of conductors (electrons for NMOS / holes for PMOS) when current flows through the channel. In some pass transistor circuits, the source and drain may swap over during use.

- Implied Connections and Crossovers

Where two sticks of the same colour meet or cross there is always a connection.

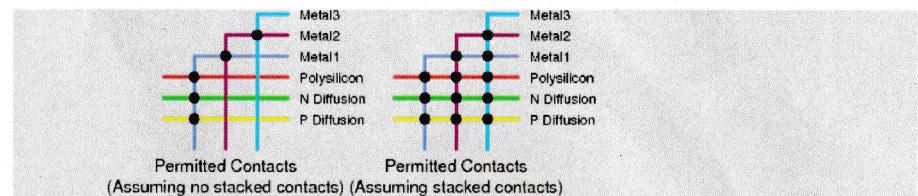
Where two sticks of different colours meet or cross there is no implied connection.



Note that N and P diffusions may not cross each other. Where poly crosses diffusion we have a transistor (see above).

- Contacts

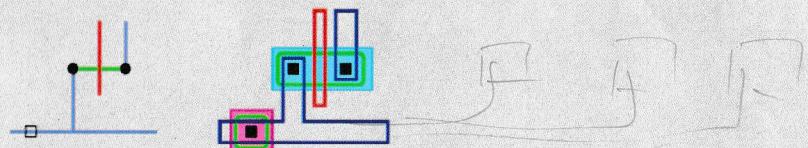
A connection may be explicitly defined using a filled black circle. In the general case a connection is permitted where the mask layers will be separated by just one layer of insulator (through which a "contact cut" may be defined). Thus P diffusion may connect to Metal1 but not directly to Metal2.



In a process where stacked contacts are permitted, we may draw a contact between non-adjacent conductors; e.g. between Poly and Metal3, in which case the connection to intermediate layers (Metal1 and Metal2) is implied.

- Taps

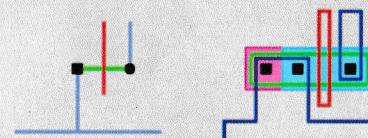
The tap represents a connection to something we can't see; either the N-Well (not shown on our stick diagram) or the wafer substrate. A tap is defined using an unfilled black square. Here there will be only one conductor crossing the square (Metal1 power or ground rail).



An N-Well Tap is inferred where the connection is from a power rail while a Substrate Tap is inferred where the connection is from a ground rail.

- Combined Contacts & Taps

We can often save space by using a combined contact and tap. Here the tap shares the same Active Area as the contact. A combined contact and tap is defined using a filled black square in place of the source contact (filled black circle).



A combined contact and tap can only be used where the end of a diffusion stick coincides with a contact to the power or ground rail.

- Stick Diagram Colour Code

P diffusion	: Yellow/Brown	Metal1 : Blue
N diffusion	: Green	Metal2 : Magenta/Purple
Polysilicon	: Red	Metal3 : Cyan/Turquoise
Contacts & Taps	: Black	

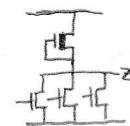
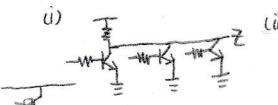
If you deviate from these colours you will need to include a key with your stick diagram.

ICD EXAM QUESTION HANDOUT #1

Q8/Q9 3.

- (a) For each of the following logic families draw a *transistor level circuit diagram* of a 3 input NOR gate and briefly describe its operation:

(i) Resistor Transistor Logic (RTL)



(ii) NMOS Logic

(iii)

Static CMOS Logic $\bar{Z} = \bar{A} + \bar{B} + \bar{C}$

$$\bar{Z} = \bar{A} + \bar{B} + \bar{C} = \bar{A} \cdot \bar{B} \cdot \bar{C}$$



What are the advantages of CMOS for VLSI design compared to the older RTL and NMOS technologies.

Fast, small, negligible power consumption

(9 marks)

10/11

1.

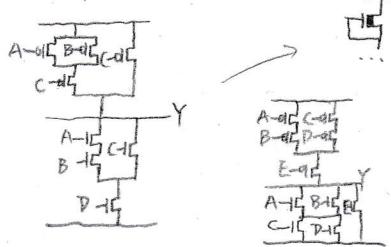
The following boolean expressions are to be implemented as standard cells on an integrated circuit:

$$Y = (\bar{A} + \bar{B}) \cdot \bar{C} + \bar{D}$$

$$Y = (\bar{A} \cdot \bar{B} + \bar{C} \cdot \bar{D}) \cdot E$$

$$\bar{Y} = (A + B) \cdot (C + D) + E$$

- (a) (i) For each of the boolean expressions derive a transistor level circuit diagram for its implementation as a static NMOS compound gate.



- (ii) For each of the boolean expressions derive a transistor level circuit diagram for its implementation as a static CMOS complementary compound gate.

- (iii) Discuss the relative merits of NMOS and CMOS technologies in the light of these circuit diagrams.

(16 marks)

Q9/10

1.

- (a) Which of the following Boolean functions may be implemented as single static CMOS complementary gate?

single static CMOS complementary
Do

$$Y = A \cdot B$$

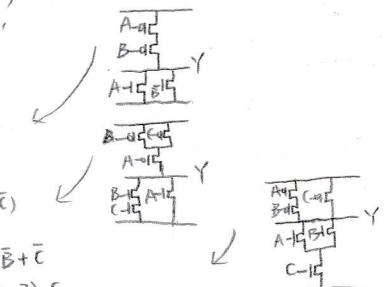
$$Y = A \oplus B = AB + \bar{A}\bar{B}$$

$$\checkmark Y = \bar{A} + B \quad \begin{cases} Y = \bar{A} \cdot \bar{B} \\ \bar{Y} = A + B \end{cases}$$

$$Y = \bar{A} \oplus B$$

$$\checkmark Y = \bar{A} + B \cdot C \quad \begin{cases} Y = \bar{A} \cdot (\bar{B} + \bar{C}) \\ \bar{Y} = A + BC \end{cases}$$

$$\checkmark Y = (\bar{A} + B) + \bar{C} \quad \begin{cases} Y = \bar{A} \cdot \bar{B} + \bar{C} \\ \bar{Y} = (A + B) \cdot C \end{cases}$$

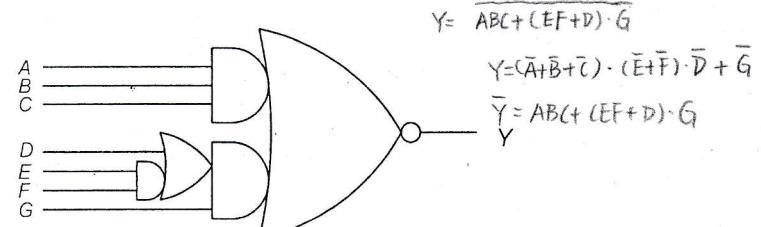
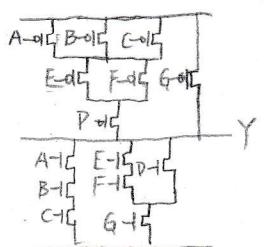


Where such an implementation is possible, provide a circuit diagram showing the transistor interconnections.

Define the set of Boolean functions which may be realized as single static CMOS complementary gates.

(12 marks)

- (b) The following compound gate is to be designed using CMOS technology:



- (i) Write a Boolean expression which defines the function of this gate and hence derive a suitable transistor level circuit diagram.

ICD Exam Question Handout #2

2011/2012 B1.

Figure B1 shows the mask level layout of a two-input CMOS gate.

- (a) The line between X and X' on figure B1 cuts through three transistors. Draw a cross-sectional diagram of the gate along this line and identify the doping regions according to their type (p or n) and their function (wafer substrate, well, tap or source/drain). (10 marks)
- (b) With reference to the masks in figure B1 and your cross sectional diagram, explain the term **self-aligned** as it applies to MOS transistor construction. (5 marks)

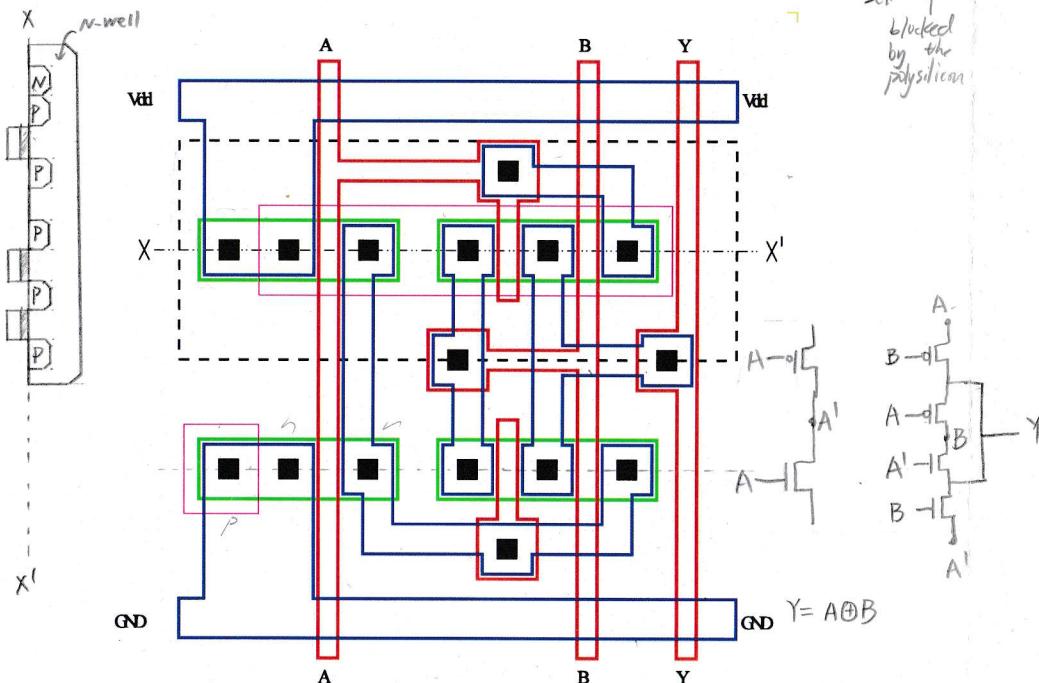
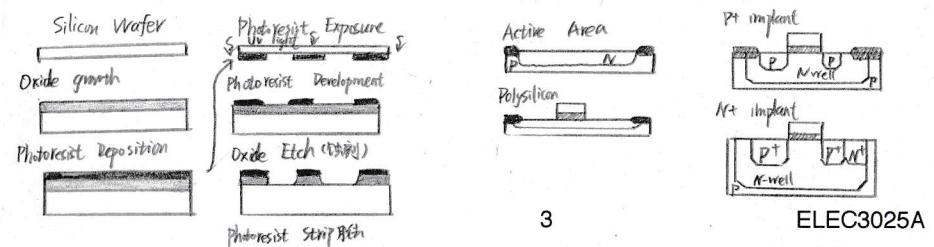
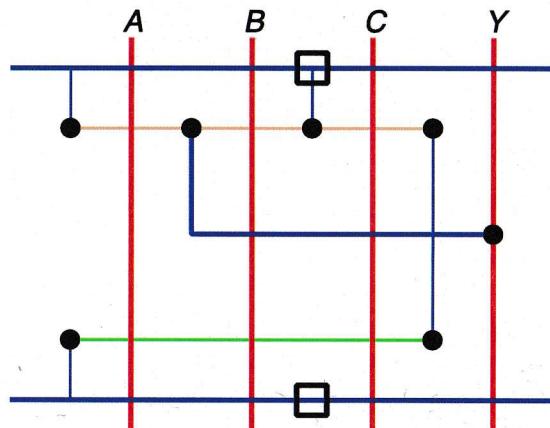


Figure B1: Mask layout of a two-input CMOS gate



- 2.
- (a) Briefly describe, with the aid of suitable diagrams, the stages involved in producing a PMOS transistor for a CMOS process. You should relate your answer to the masks listed in the sample design rules provided with this exam paper. (13 marks)

- (b) The figure below is a stick diagram for a 3 input NAND gate which is to be realized in $0.4\mu\text{m}$ CMOS (based on the sample design rules provided):



Sketch a complete mask level layout for this gate given the following transistor dimensions:

$$W_n = W_p = 1.0\mu\text{m}$$

$$L_n = L_p = 0.4\mu\text{m}$$

Your sketch need not be to scale.
From your sketch, derive the width of your NAND gate.
You should give your working and justify any assumptions that you make.

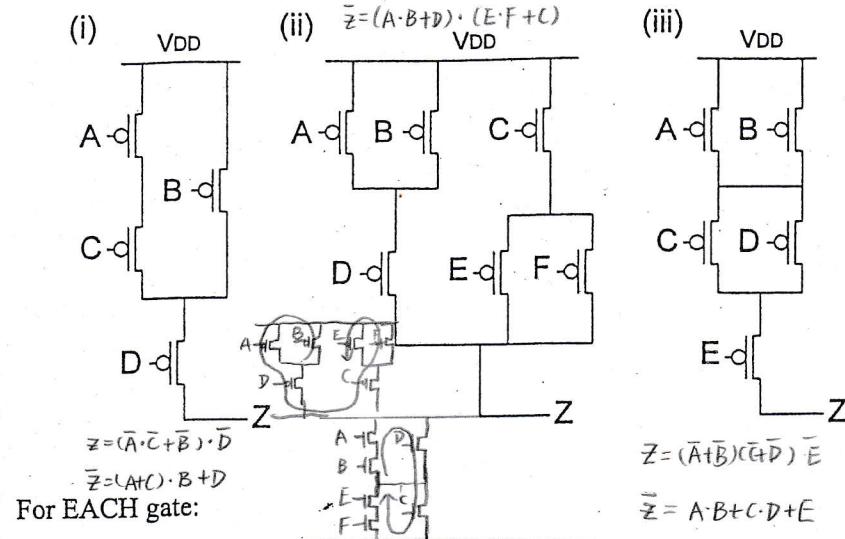
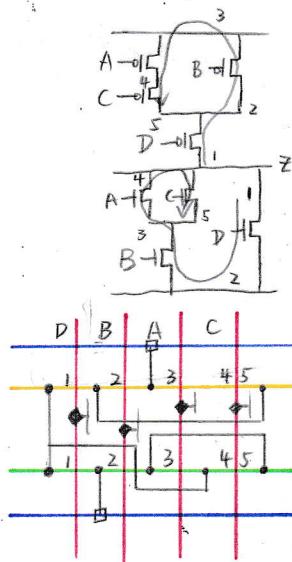
(20 marks)

TURN OVER

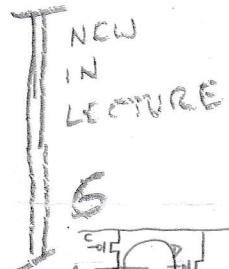
Q3/Q4

Q1

1. The Pull Up Networks (PUNs) for three static CMOS complementary gates are shown below:



- For EACH gate:
- (a) Derive a Boolean expression for the gate. (6 marks)
 - (b) Design a suitable Pull Down Network (PDN) to complete the gate. (6 marks)
 - (c) Find an Euler path for the gate if such a path exists.
Note that you may need to re-arrange the transistors within the schematic in order to find an Euler path. (10 marks)
 - (d) Derive a suitable stick diagram for efficient layout of the gate using a CMOS process supporting only one metal layer. (11 marks)



Q4/Q5

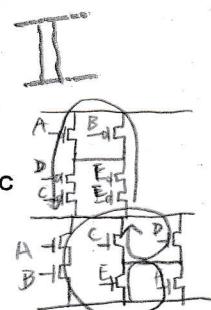
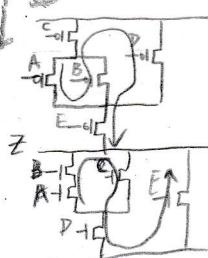
Q1

- (b) The following Boolean function is to be realized in static CMOS logic:

$$Y = (\bar{A} \cdot B + C) \cdot D + E = [\bar{A} + \bar{B}] \cdot \bar{C} \cdot \bar{D} \cdot \bar{E}$$

$$\bar{Y} = (A \cdot B + C) \cdot D + E$$

- (i) Derive a suitable transistor level circuit diagram for this gate.
- (ii) Derive a stick diagram for this gate, based on an investigation of possible Euler paths. (18 marks)



Q5/Q6

Q1

- (c) The following Boolean function is to be realized as a static CMOS complementary gate:

$$Y = (\bar{A} + \bar{B}) \cdot [\bar{C} \cdot \bar{D} + \bar{E} \cdot \bar{F}]$$

$$Y = \bar{A} \cdot B + (C + D) \cdot (E + F)$$

$$\bar{Y} = A \cdot B + C \cdot D + (E + F)$$

- (i) Derive a suitable transistor level circuit diagram for this gate.
- (ii) Derive a stick diagram for this gate, based on an investigation of possible Euler paths. Your design should be suitable for use as a standard cell for a CMOS process supporting two metal layers. (17 marks)



REQUIRES INFO
FROM LECTURE 7

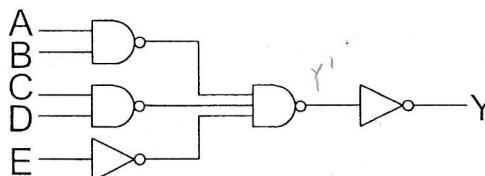
ϕ_8/ϕ_9

2

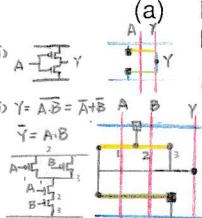
ELEC3025W1

1.

The following circuit is to be implemented in static CMOS logic



(a) Derive a stick diagram for the implementation of each of the following basic gates



$$\text{(i)} \quad \text{inverter}$$

$$\bar{Y} = A \cdot \bar{B}$$

$$\bar{Y} = A + B$$

$$\text{(ii)} \quad Y = \overline{A \cdot B} = \bar{A} + \bar{B}$$

$$Y = A \cdot B$$

$$\text{(iii)} \quad Y = \overline{A \cdot B \cdot C} = \bar{A} + \bar{B} + \bar{C}$$

$$\bar{Y} = A \cdot B \cdot C$$



$$\text{(i)} \quad \text{2 input NAND gate}$$

$$Y = \overline{A \cdot B}$$

$$\bar{Y} = A + B$$

$$\text{(ii)} \quad \text{3 input NAND gate}$$

$$Y = \overline{A \cdot B \cdot C}$$

$$\bar{Y} = A + B + C$$



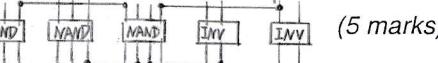
Your designs should be suitable for use as standard cells for a CMOS process which supports multiple metal layers (please state whether you design is aimed at a two metal layer process or a three metal layer process).

(9 marks)

(b) Explain the purpose of a *black box* or *abstract view* in the standard cell design process. Illustrate your answer with abstract views for each of the standard cells you have designed.

(5 marks)

(c) Derive a stick diagram for the full circuit above based on the abstract views you have drawn.



(5 marks)

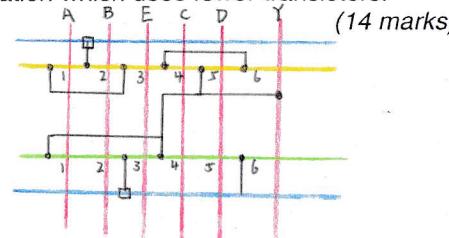
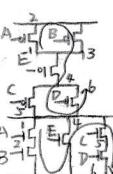
(d) Derive a boolean equation for Y in terms of A, B, C, D and E . Hence or otherwise derive a stick diagram for an alternative static CMOS implementation of this equation which uses fewer transistors.

$$Y = \overline{AB} \cdot \overline{CD} \cdot \overline{E}$$

$$= (\bar{A} + \bar{B}) \cdot (\bar{C} + \bar{D}) \cdot \bar{E}$$

$$\bar{Y} = \overline{\overline{AB} \cdot \overline{CD} \cdot \overline{E}}$$

$$= AB + CD + E$$



(14 marks)

5.

(a) (i) Derive a stick diagram for the layout of a 2-input AND gate based on static CMOS logic. The layout should be suitable for use as a standard cell for a CMOS process that supports just one metal layer.

$$Y = \overline{A \cdot B} = \bar{A} + \bar{B}$$

$$\bar{Y} = A \cdot B$$

(5 marks)

(ii) Redesign your gate for use as a standard cell for a CMOS process that supports two metal layers. What is the advantage of this approach over the one metal design?

(4 marks)

(iii) Redesign your gate for use as a standard cell for a CMOS process that supports three metal layers. What is the advantage of this approach over the two metal design?

(3 marks)

(iv) Draw *black box* or *abstract views* of each of these designs. What purpose do these views have in the standard cell design process?

(5 marks)

 ϕ_1/ϕ_2

5. (a) Produce a circuit schematic of an inverter gate using dynamic CMOS logic, and explain the gate operation.

(10 marks)

(b) Briefly discuss the two limitations of dynamic logic: charge leakage and charge sharing.

(6 marks)

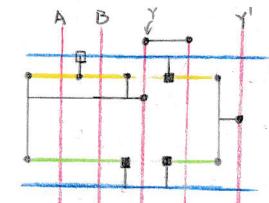
(c) Describe the standard cell approach to ASIC design and the restrictions it imposes on the design of individual gates. Illustrate your answer with a stick diagram for the dynamic inverter, suitable for implementation as a standard cell using a CMOS process with two metal layers.

(10 marks)

(d) Re-design the gate for a CMOS process with three metal layers.

Explain how the use of three metal layers can be exploited to reduce circuit area.

(7 marks)

 ϕ_7/ϕ_8

REVIEW
NOT YET
COMPLETED
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