CSCE 312 Lab manual

Lab-2 - Combinational logic design

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Chapter 3: Combinational logic design

In the last chapter we understood the usefulness of basic logic gates (example – TTL gates) in designing simple digital applications. In this chapter, we focus on designing the combinational digital circuits for similar applications. The idea is to learn how to apply Boolean logic theories in designing digital circuits to solve real-life problems.

1. Learning duration: 1 week. **Required Tools:** Logisim 3.8.0

2. Objective:

To learn -

Primary topics

1. How to design combinational digital circuits using logic gates.
2. What are the basic design considerations in designing combinational circuits?
3. How to identify and choose the required chips to implement the designed circuits.
4. How to test combinational circuits.
5. How to optimize the design using larger gates.

Secondary topics

6. To get familiar with TTL chips and their data sheets.
7. Develop an engineering understanding about which data sheet parameter to use.
8. Familiarity of a simple GUI based digital circuit design and simulation tool

3. Instructions:

The following instructions are good for next few chapters and labs –

1) You will use the freeware software tool named "**Logisim**" to design and verify the digital circuits.
2) This tool is available for download from https://github.com/logisim-evolution/logisim-evolution/releases.
   Documentation for Logisim is available on the same website. You should have already installed the tool during the first lab session. If you haven't, please do so currently. According to the devise you have, download the appropriate installer. You can also build the source code if you wish to do it.
   a) *Macbook - .dmg*
   b) *Linux - .deb*
   c) *Windows - .msi* (To figure out if your processor is x86 or arm : Link)
3) Use the Logisim tool to do all the problems of this chapter. You will have all the required gates, LED, 7 segment display, push button switch, memory, clock, sequence generator, etc. in the tool. Explore the tool by yourself to see what all circuit components are available and how to use them. If you get stuck using the software, contact your TA.

4) Use push button switches and attach them to the input lines whose logical states you want to change for testing. Logic states of the input lines can be changed simply by pushing the corresponding switches. Use LEDs to monitor the logic states of individual lines. A glowing LED indicates 1/true state.
5) As a good design practice, run parallel wires (called a bus) of all the input variables and their inverses (NOT of the variables) and then tap these to feed the input of the gates. It is possible to mark the wires, switches with names typed beside them.

4. Useful resources:

1. Chapter 1, 2 of Frank Vahid's "Digital Design" or the first few chapters of any digital circuit/design/architecture book by Morris Mano (available in TAMU library).

2. About TTL logic – http://en.wikipedia.org/wiki/Transistor-transistor_logic

3. About 74xx series logic family - http://en.wikipedia.org/wiki/7400_series

4. To obtain data sheets for the logic gates use – https://www.futurlec.com/IC7400Series.shtml

5. List of all 74xx series logic gates (this would be useful to identify which gates you would like to use) - http://en.wikipedia.org/wiki/List_of_7400_series_integrated_circuits or http://rabbit.eng.miami.edu/info/datasheets/

https://www.futurlec.com/IC74Series.shtml

6. You can also these resources or google for the required data sheet if you know the 74xx series chip name:

   a. http://rabbit.eng.miami.edu/info/datasheets/
   b. http://www.alldatasheet.com/

7. 7 segment display information (use pin diagram + truth table for Cathode) is available here - https://www.electronicshub.org/seven-segment-displays/

5. Exercises to do

Problem 1: (50 points)

Activities to do-

1. Using gates, draw and verify the digital circuit for the functions. Do not simplify/reduce the equations. Implement using gates as well as TTL ICs for both parts. Please provide a screenshot of your digital circuit in your lab report. Mention what are the names of the 74xx series logic gates that you use to do the above problem in real-life situations when using TTL ICs.

(30points in total, 15 for each)

a. F = abc + ab + bc + ca
b. G = a'b' + a'bc' + ab'c'

2. Calculate the delay performance (time delay between change of any input which leads to change of the output) of the two circuits (using gates only) designed above. Use respective data sheets for the required chips. **(10 points)**

3. Also, mention parameter(s) (Vcc, temperature, resistors, capacitance, tphl, tplh) you use to calculate the delay performance.

(10points)

Notes:

1. *Circuit delay is the delay of the longest path in the circuit from input to output. If your longest path had 3 gates, then the sum of the individual delays make up the delay of the circuit.*

2. *In the data sheet, the delays reported are for individual gates. It does not matter if the package has 4 gates in it or 6 gates in it- the delay reported in the datasheet is for one gate.*

Problem 2: (50 points)

New York's Metropolitan Transport Authority (MTA) operates the subway transport facility in New York. Each subway train consists of 9 subway cars all chained together and pulled by a motored subway car at the front end. (9 + 1 = 10 cars in total) To improve the security of passengers, MTA decided to install a switch inside every subway car. A passenger can press this emergency switch which is there in his/her car to signal the driver that an emergency has happened in his/her car. In response the driver will then dispatch security personnel to that car when the car stops at the next station. You are recruited by MTA to develop a digital system to achieve this. MTA's chief wants that when the emergency button is pressed in a particular car, that car's number should be displayed in the driver's dashboard. *If no button is pressed, the display remains off. Assume that no two cars have emergency at the same time.* You decided to use a **7 segment LED display**, an encoder and a decoder built by TTL chips, to design and implement this system. The functional diagram of the system is given below –

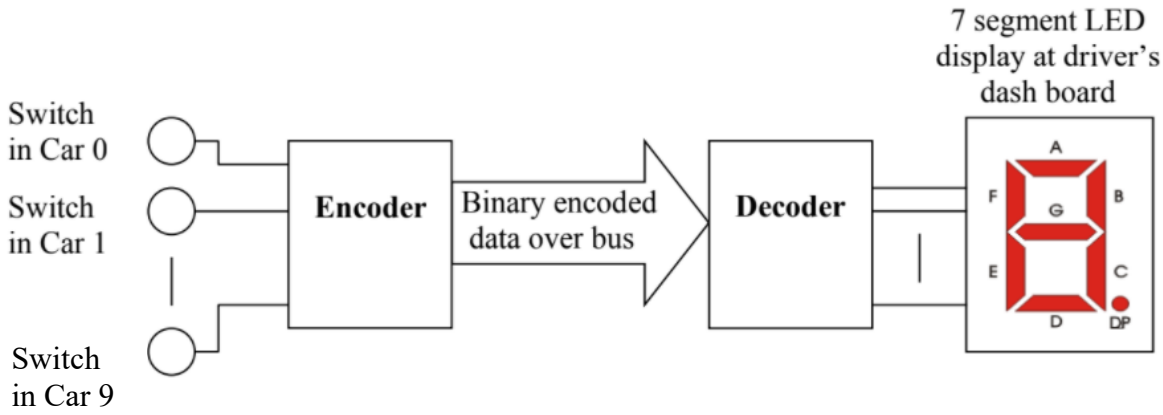

Fig. 1: The functional block level diagram of the proposed digital system

Activities to do-

1. Identify the following design parameters and mention them in your report –
    a. Number of switches/input bits that will be required
    b. Number of output bits used to light up the 7 segment display
    c. Number of the bits/wires required in the data bus.
    d. Size of the encoder.
    e. Size of decoder.
2. Read one of the 7 segment LED display data sheet, try to understand how to use it.
3. Design the encoder and decoder blocks with basic logic gates then incorporate the same into a complete digital system on Logisim.
4. Provide a screenshot of your design with a brief text explanation/description on how it will work in your lab report. Also, show a demo of your digital system to TA to get credit for this lab.

(50 points, 30 points for demo + 20 points for answer and in report explanation. However, if you don't show demo, you won't get credit for this lab)

Lab 2 Checklist

- ✓ Lab Report (with all the screenshots)
- ✓ All Logisim files created for Problem 1 (4 logic circuits)
- ✓ Logisim file created for Problem 2

Compress all these to create <LastName>_<UIN>.zip and submit it on canvas before deadline.