CSCE 312 Lab 3

Kevin Lei

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Problem 1

Here we implement a D flip-flop from scratch using only NAND gates. The D flip-flop uses two D latches, which are implemented as follows:

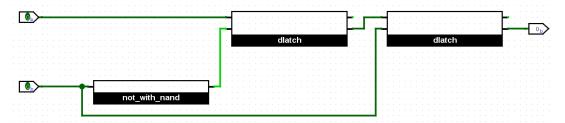


Figure 1: D Flip-Flop

The D latches are implemented as follows:

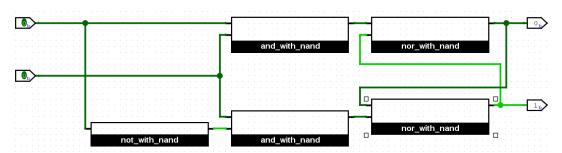


Figure 2: D Latch

The NOR, NOT, and AND gates are implemented as follows:



Figure 4: NOT Gate

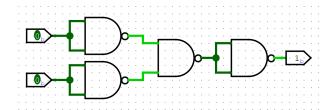


Figure 5: NOR Gate

Problem 2

Part A

Electromechanical switches can be described by their number of poles and throws. A pole is a common connection in a switch, and a throw is the number of positions the pole can connect to. Therefore, a single-pole, single-throw (SPST) switch has one pole and one throw, which means it is just a simple on-off switch that connects or disconnects a single circuit. The term NO means normally open, and it is used to describe the throw of a switch when it is not actuated (open means that the circuit is not connected).

Part B

L=0 b L=1	A:00	Ъ	S,	5,	n,	n,	l	
→ (A) 2p' (B)	C; (D	0	0	D	0	٥	0	l = S, ⊕ So
b' (1=0 (=1)b'	b:11	١	0	0	0	(٥	N= 6'5,'5+ 6'5, 5,'+ 65,5,'+ 65,5,
(0) 6 (2)		0	0	(1	٥	1	= P, (2', 20 + 2' 2, 2,) + P 2'(2°, + 2°)
6 Pb'		(0	(O	l	١	= b' (s, \theta s.) + b s,
		D	1	D	1	0	(N. = P
		ţ	[О	l	((
		D	(1	0	0	D	
		(1	1	(٥	

Figure 6: FSM, Truth Table, and boolean expressions for the circuit

Part C

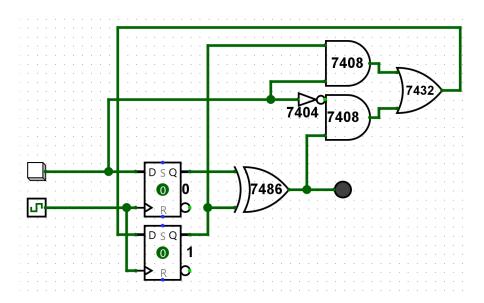


Figure 7: Overall circuit with 74xx series equivalents

Problem 3

Part A

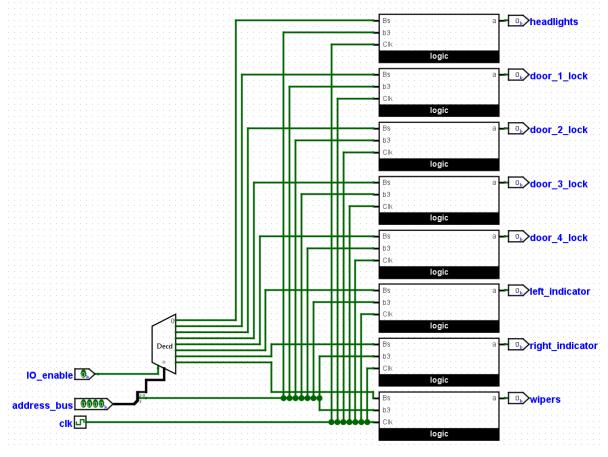


Figure 8: Overall design of the circuit

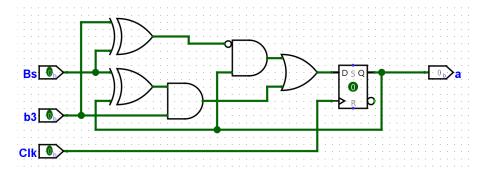


Figure 9: Logic implementation

Part B

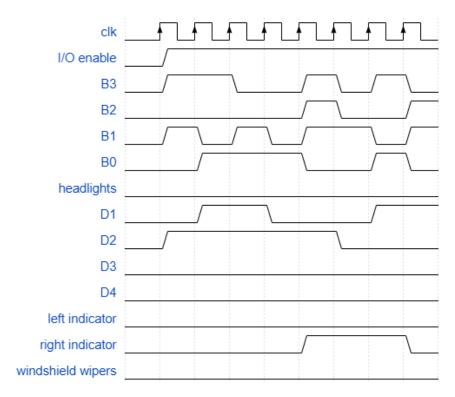


Figure 10: Timing diagram