CSCE 312 Lab 2

Kevin Lei

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1 Problem 1

1.1 Part 1

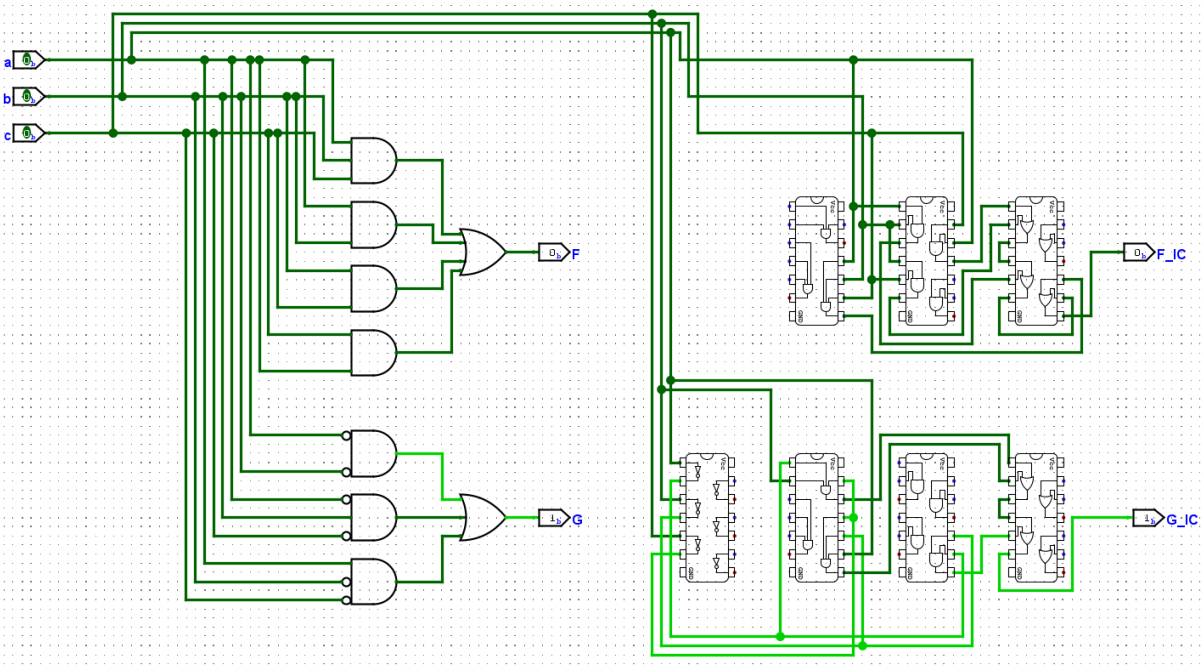

Figure 1: Implementations of boolean functions F and G using only logic gates and only 74xx series ICs.

ICs used in the implementation of boolean function F:

- 7408 quad 2-input AND gate
- 7411 triple 3-input AND gate
- 7432 quad 2-input OR gate

ICs used in the implementation of boolean function G:

- 7404 hex inverter
- 7408 quad 2-input AND gate
- 7411 triple 3-input AND gate
- 7432 quad 2-input OR gate

1.2 Part 2

For the pure logic gate implementations, we will assume a 22 nanosecond delay for each AND, OR, and NOT gate. The propagation delays for the 74xx series ICs are as follows:

- 7404: 22 ns
- 7408: 22 ns
- 7411: 22 ns
- 7432: 22 ns

Thus, the propagation delays for the implementations of F and G are as follows:

- F (logic gates): 22 ns + 22 ns = 44 ns
- G (logic gates): 22 ns + 22 ns + 22 ns = 66 ns
- F (74xx series ICs): 22 ns + 22 ns = 44 ns
- G (74xx series ICs): 22 ns + 22 ns + 22 ns = 66 ns

1.3 Part 3

Switching characteristics of 7404 hex inverter at Vcc = 5V and 25°C:

Symbol	Parameter	Conditions	Min	Typ	Max	Units
tplh	Propagation Delay Time LOW-to-HIGH Level Output	Cl=15pF Rl=400R			22	ns
tphl	Propagation Delay Time HIGH-to-LOW Level Output	Cl=15pF Rl=400R			15	ns

Switching characteristics of 7408 quad 2-input AND gate at Vcc = 5V and 25°C:

Symbol	Parameter	Conditions	Min	Typ	Max	Units
tplh	Propagation Delay Time LOW-to-HIGH Level Output	Cl=15pF Rl=400R			22	ns
tphl	Propagation Delay Time HIGH-to-LOW Level Output	Cl=15pF Rl=400R			15	ns

Switching characteristics of 7411 triple 3-input AND gate at Vcc = 5V and 25°C:

Symbol	Parameter	Conditions	Min	Typ	Max	Units
tplh	Propagation Delay Time LOW-to-HIGH Level Output	Cl=15pF Rl=400R			22	ns
tphl	Propagation Delay Time HIGH-to-LOW Level Output	Cl=15pF Rl=400R			15	ns

Switching characteristics of 7432 quad 2-input OR gate at Vcc = 5V and 25°C:

Symbol	Parameter	Conditions	Min	Typ	Max	Units
tplh	Propagation Delay Time LOW-to-HIGH Level Output	Cl=15pF Rl=400R			22	ns
tphl	Propagation Delay Time HIGH-to-LOW Level Output	Cl=15pF Rl=400R			15	ns

2 Problem 2

2.1 Part 1

a. The number of input bits is 10 since there are 10 cars with switches.

b. We will need 7 output bits for the 7-segment display (since each segment must be either on or off).

c. We will need a 4-bit data bus between the encoder and decoder, since $\lceil \log_2 10 \rceil = 4$.

d. We will need a 10 to 4 encoder.

e. We will need a 4 to 7 decoder.

2.2 Part 2

2.3 Part 3

2.4 Part 4