CSCE 312 Lab manual

Lab-3 - Sequential logic design

Instructor: Prof. Eun Jung Kim

Prepared by

Dr. Rabi Mahapatra.
Suneil Mohan & Amitava Biswas

Spring 2024

Department of Computer Science & Engineering
Texas A&M University

Chapter 4: Sequential logic design

In this chapter, we focus on the design of sequential digital circuits for real-life applications. Sequential circuits allow us to capture the notion of time, so that it is possible to store and track different states across time. Thus, sequential circuits can manifest higher level of machine intelligence and perform more complicated tasks than combinational circuits.

1. Learning duration: 2 weeks. **Required Tools:** Logisim 3.8.0

2. Objective:

To learn -

Primary topics

1. How to design sequential digital circuits using logic gates and standard components.
2. How to document the design and its operations for others to understand.
3. What are the basic design considerations for sequential circuits.
4. How to standardize designs to generate reusable circuit design patterns to benefit from standardization and reusability (concept of macro).
5. How to apply standard design patterns to organize basic IO and peripheral circuitry.

Secondary topics

6. Using the schematic design tool ("Logisim") to create reusable libraries of design patterns.
7. Familiarity with all the basic sequential circuit blocks.
8. How to interpret data sheets for industrial components as a part of the design activity.

3. Instructions: Use Logisim for your designs. Logisim should be available on the lab machines since you used it for the previous lab. If not, you can download a copy from the previously mentioned website.

4. Useful resources:

1. Chapter 1, 2, 3 of Frank Vahid's "Digital Design" or the first few chapters of any digital circuit/design/architecture book by Morris Mano (available in TAMU library).

Problem 1 ***(20 points)*****:** Implement a D-flip flop from scratch using **only NAND gates**.

a) First design the D-latch you wish to implement using only NAND gates.
b) Use two such latches and connect them using the master-servant logic and create the D-flip flop.
c) Add a screenshot of this logic in your report with all the subcircuits you might have used.
d) Show the demonstration for D-flip flop and D-latch (if you see "oscillation apparent" errors, it is fine).

Problem 2 ***(40 points)*****:** You performed well in your last design assignment at Ford Motor Company, so you still retain your job there. Today your manager asked you to design the switch which starts and stops the car's air conditioning system. The requirement is given as –

"….When the a/c button is pushed it should start the a/c, pushing this button for the second time should stop the a/c. The button also incorporates a built-in green LED which glows when the a/c is operating, and remains off otherwise. This switch signals the car's main control logic to turn on the relay which switches on the a/c compressor… "

You asked one of your senior colleagues to help you get started. He told you that this kind of button functionality is known as a "**toggle push button**". He also told you that as Ford is facing competition to cut costs, it would be better to use a "normally off (push-to-make) illuminated push button (SPST, NO)" to implement this toggle push button, which is cheaper and more reliable, rather than using a costly and less reliable mechanical toggle button.

Hint: Different types of switches are described in the below link – Switches

Activities to do-

a) What is the meaning of "SPST" and "NO" in the context of electro-mechanical switches? Mention in your report. *(5 points)*

b) Design a small digital circuit **using gates and memory elements (use the built in Flip Flops in Logisim with clocks)**, so that when this circuit is used with the chosen switch, it will make the circuit function as a toggle switch.

   Use the **button component in Logisim** for this question. (Input/Output > Button) The way the button switch operates in Logisim is that as long as you keep the button pressed, an LED or other output signal will stay ON. When you release the button, the LED or output signal goes OFF. Design a toggle switch such that when you press the button once, your LED turns ON and then remains ON (even after the button is released) until the button is pushed again. *(30 points)*

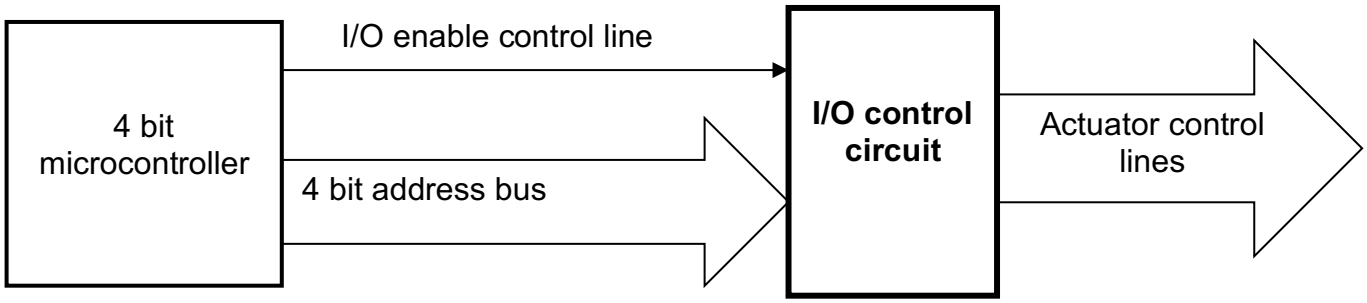
c) Using the text-insert feature in Logisim mention in the circuit the chip number(s) (from the 74XX family) that you would use for the circuit if you were to use TTL ICs. *(5 points)*

d) **Show a demo of your toggle switch to your TA and submit your Logisim file along with your lab report. Add a screenshot of this logic in your report as well.**

Problem 3 ***(40 points):*** Your manager at Ford has asked you to design a circuit to implement "addressable I/O" for a 4-bit microprocessor/microcontroller. This will be used to activate 8 actuators numbered from **000** to **111** (headlights, 4 individual door locks, left indicator, right indicator, and windshield wipers). This circuit will allow a CPU with a 4-bit address bus to activate actuators by writing suitable addresses on the address bus and activating/deactivating it **depending on the 4th bit of address**. He has provided the following text requirement to get you started –

"…The headlights are turned on by putting a binary equivalent of "**1000**" and enabling the I/O enable line. Similarly, an address value "**0010**" gets the 2nd door (Door 2) unlocked …"

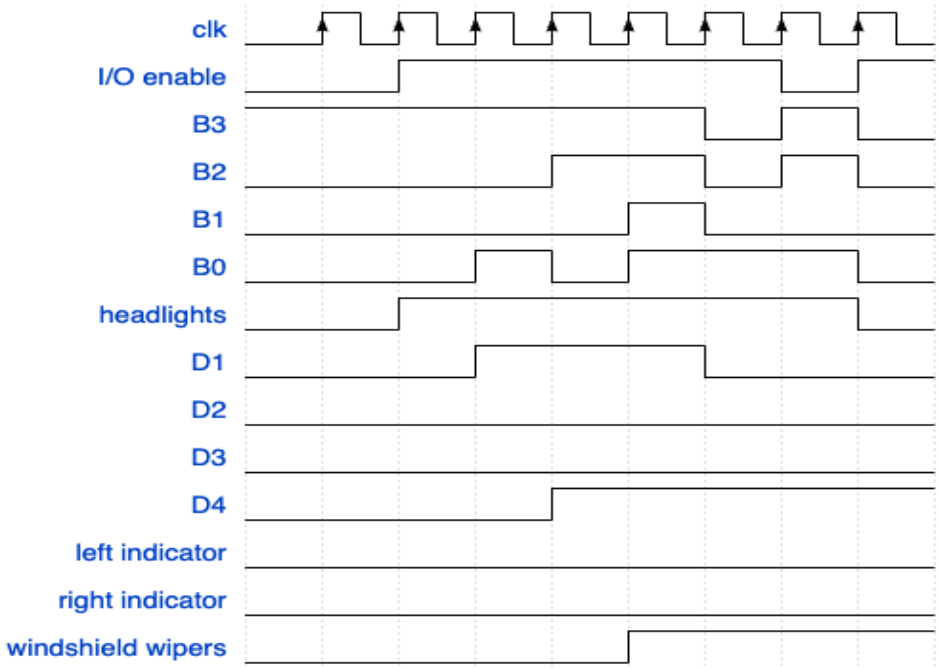
He has also sketched out the following system level diagram for you. He expects you to detail out the I/O control block and generate the required gate level circuitry for it in Logisim (**using the built in Flip Flops in Logisim)**.



Address bus lines				I/O Enable	Output actuator control lines								Comments
B3	B2	B1	B0		Headlights	D1	D2	D3	D4	Left Indicator	Right Indicator	Windshield wipers	
X	X	X	X	0	0	0	0	0	0	0	0	0	Nothing happens as I/O disabled
1	0	0	0	1	1	0	0	0	0	0	0	0	Headlights are ON
1	0	0	1	1	1	1	0	0	0	0	0	0	Door 1 locks
1	1	0	0	1	1	1	0	0	1	0	0	0	Door 4 locks
1	1	1	1	1	1	1	0	0	1	0	0	1	Wipers are ON
0	0	0	1	1	1	0	0	0	1	0	0	1	Door 1 unlocks
1	1	0	1	0	1	0	0	0	1	0	0	1	Nothing happens as I/O disabled
0	0	0	0	1	0	0	0	0	1	0	0	1	Headlights are OFF

When the I/O enable is ON, the three bits B2, B1 and B0 determine which actuator to select and the 4th bit, i.e. B3 determines whether the actuator should be activated (1) or deactivated (0). All the other actuators which are not selected retain their settings. When the I/O enable is OFF, no matter the value of the 4-bit address, the states of all the actuators remains constant.

To help you with the design, another one of your colleagues has provided you the following **timing diagram which corresponds to the previous table**–



Activities to do-

a) Design and verify the required circuit to implement the I/O control sub-system. *(30 points)*

b) **Create timing diagrams** showing the change of state of the various signal and control lines as implemented by your circuit. Show the clock and the set of pattern waveforms on B3-B0 and the control lines based on the following activities. (*10 points)*

(Assume I/O enable is set for the cases and at Clock cycle 0, all the lines are at state 0)

Clock cycle 1: B3-B0: value 1010
Clock cycle 2: B3-B0: value 1001
Clock cycle 3: B3-B0: value 0011
Clock cycle 4: B3-B0: value 0001
Clock cycle 5: B3-B0: value 1110
Clock cycle 6: B3-B0: value 0010
Clock cycle 7: B3-B0: value 1001
Clock cycle 8: B3-B0: value 0110

c) **Show a demo of your design to your TA and submit your Logisim file along with the lab report. Add a screenshot of this logic in your report as well.**

LAB 3 - Checklist:

- ✓ Problem 1 : Screenshot of D Flip Flop circuit and all subcircuits.
- ✓ Problem 1 : The Logisim file.

- ✓ Problem 2 : Answer to the question asked.
- ✓ Problem 2 : Diagram of Finite State Machine and Truth Table in report.
- ✓ Problem 2 : Screenshot of your logic (with screenshots of each subcircuit used)
- ✓ Problem 2 : Working Logisim file.

- ✓ Problem 3 : Timing Diagram.
- ✓ Problem 3 : Screenshot of your logic.
- ✓ Problem 3 : Working Logisim file.

Put all the Logisim files and your .pdf report in a folder, compress it and submit it on Canvas as "LastName_UIN.zip"