CSCE 312 Lab 2

Kevin Lei

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1 Problem 1

1.1 Part 1

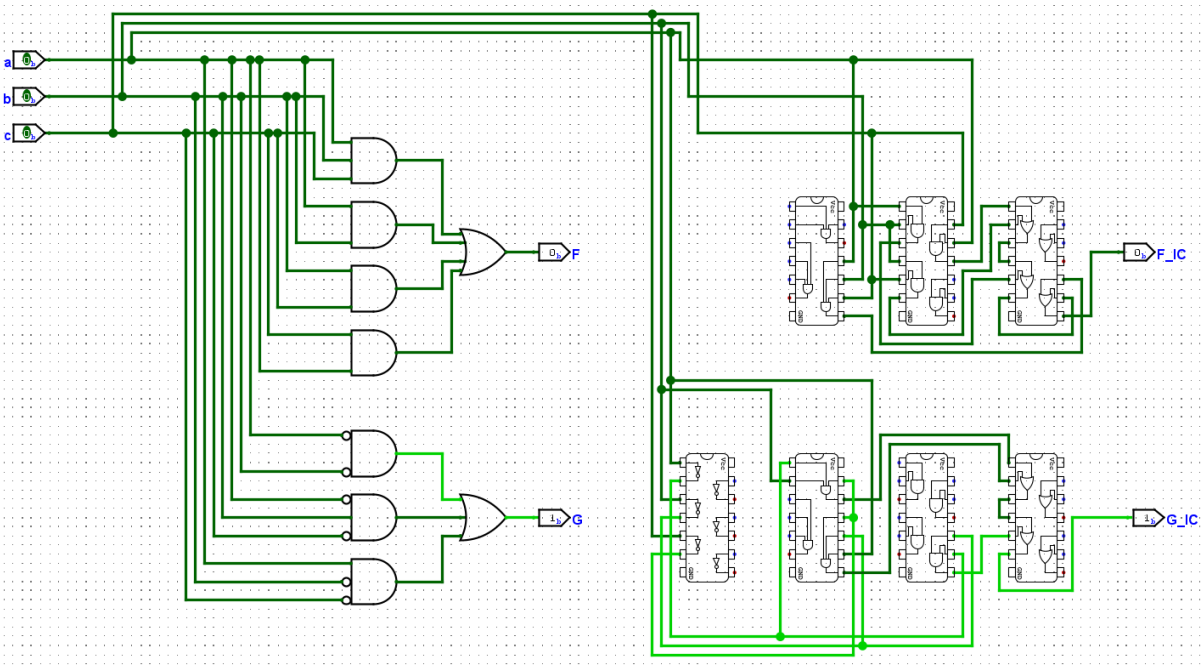

Figure 1: Implementations of boolean functions F and G using only logic gates and only 74xx series ICs.

ICs used in the implementation of boolean function F:

- 7408 quad 2-input AND gate
- 7411 triple 3-input AND gate
- 7432 quad 2-input OR gate

ICs used in the implementation of boolean function G:

- 7404 hex inverter
- 7408 quad 2-input AND gate
- 7411 triple 3-input AND gate
- 7432 quad 2-input OR gate

1.2 Part 2

For the pure logic gate implementations, we will assume a 22 nanosecond delay for each AND, OR, and NOT gate. The propagation delays for the 74xx series ICs are as follows:

- 7404: 22 ns
- 7408: 22 ns
- 7411: 22 ns
- 7432: 22 ns

Thus, the propagation delays for the implementations of F and G are as follows:

- F (logic gates): 22 ns + 22 ns = 44 ns
- G (logic gates): 22 ns + 22 ns + 22 ns = 66 ns
- F (74xx series ICs): 22 ns + 22 ns = 44 ns
- G (74xx series ICs): 22 ns + 22 ns + 22 ns = 66 ns

1.3 Part 3

Switching characteristics of 7404 hex inverter at Vcc = 5V and 25°C:

Symbol	Parameter	Conditions	Min	Typ	Max	Units
tplh	Propagation Delay Time LOW-to-HIGH Level Output	Cl=15pF Rl=400R			22	ns
tphl	Propagation Delay Time HIGH-to-LOW Level Output	Cl=15pF Rl=400R			15	ns

Switching characteristics of 7408 quad 2-input AND gate at Vcc = 5V and 25°C:

Symbol	Parameter	Conditions	Min	Typ	Max	Units
tplh	Propagation Delay Time LOW-to-HIGH Level Output	Cl=15pF Rl=400R			22	ns
tphl	Propagation Delay Time HIGH-to-LOW Level Output	Cl=15pF Rl=400R			15	ns

Switching characteristics of 7411 triple 3-input AND gate at Vcc = 5V and 25°C:

Symbol	Parameter	Conditions	Min	Typ	Max	Units
tplh	Propagation Delay Time LOW-to-HIGH Level Output	Cl=15pF Rl=400R			22	ns
tphl	Propagation Delay Time HIGH-to-LOW Level Output	Cl=15pF Rl=400R			15	ns

Switching characteristics of 7432 quad 2-input OR gate at Vcc = 5V and 25°C:

Symbol	Parameter	Conditions	Min	Typ	Max	Units
tplh	Propagation Delay Time LOW-to-HIGH Level Output	Cl=15pF Rl=400R			22	ns
tphl	Propagation Delay Time HIGH-to-LOW Level Output	Cl=15pF Rl=400R			15	ns

2 Problem 2

2.1 Part 1

a. The number of input bits is 10 since there are 10 cars with switches.

b. We will need 7 output bits for the 7-segment display (since each segment must be either on or off).

c. We will need a 4-bit data bus between the encoder and decoder, since $\lceil \log_2 10 \rceil = 4$.

d. We will need a 16:4 encoder. We will only need 10 of the 16 possible inputs.

e. We will need a 4:16 decoder. We will only need 7 of the 16 possible outputs.

2.2 Part 2

The 7-segment display is simply just a combination of 7 LEDs arranged in a pattern to display the numbers 0-9. Each LED has its own input, and the display is controlled by turning on the appropriate LEDs to form the desired number. There is also a decimal point LED, but it is not used in this lab. Although the logical inputs to the display take up 8 pins, there are typically two more pins for the common anode or cathode, depending on the type of 7-segment display used.

2.3 Part 3

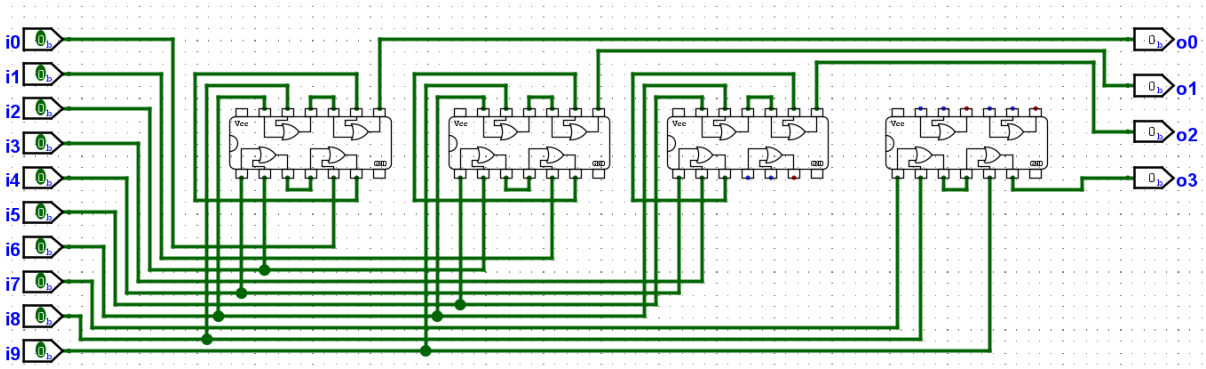

Figure 2: Encoder design

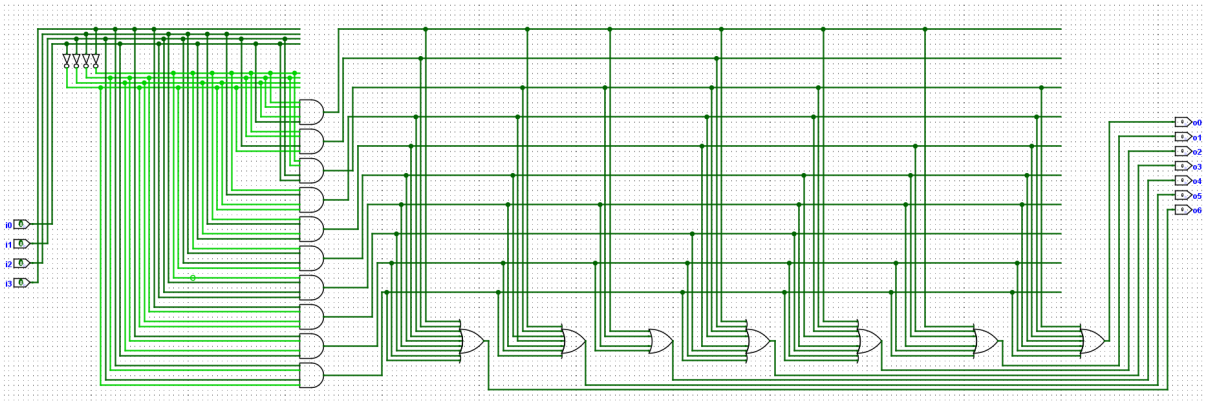

Figure 3: Decoder design

2.4 Part 4

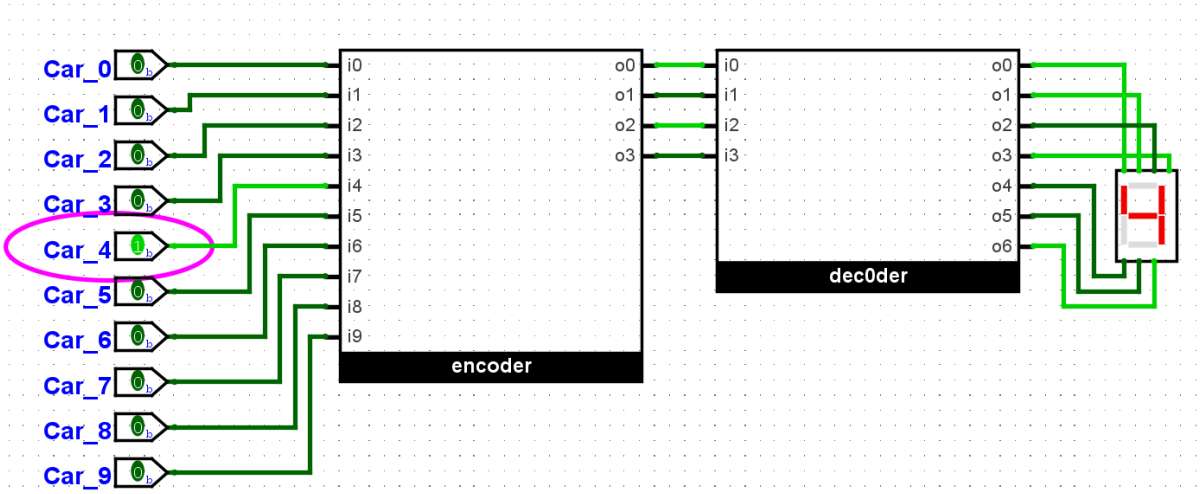

Figure 4: Overall circuit design

With the encoder and decoder abstracted away, the overall circuit design is relatively simple. The system works by having ten switches, each representing a car labeled from 0 to 9. It is assumed that no more than one switch will be on at a time. All ten switches are fed into the 16:4 encoder, which outputs a 4-bit binary number representing the car number. This 4-bit number is then fed into the 4:16 decoder, which outputs the 7-segment display signals for the corresponding number.