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5.10

5.10.1. P1=1.515 GHz; P2=1.11 GHz

5.10.2.

P1: 6.26ns and 9.48 cycles

For P1, at least one cycle is needed for all memory accesses. 70 ns access is needed for 8% of memory additionally to main memory. So 70/0.66 = 106.06cycles. Therefore, the Average Memory Access time is 1 + 0.08*106.06 = 9.48 cycles, or 6.26 ns.

P2: 5.11ns and 5.67 cycles

For P2, 70 ns is needed for a main memory. So 70/0.66 = 77.78cycles. Therefore, the Average Memory Access time is 1 + 0.06*77.78 = 5.67 cycles, or 5.1 ns.

5.10.3.

P1: 12.64 CPI and 8.34 ns per instruction.

P2: 7.36 CPI and 6.63 ns per instruction.

Explanation:

For P1, at least one cycle is needed for every instruction. 8% of all instructions miss the instruction cache and cause a 107-cycle delay. 36% of the instructions are data accesses. 8% of these 36% are cache misses, so it needs an additional 107 cycles.
1 + .08*107 + .36*.08*107 = 12.64

Each instruction takes 8.34 ns with a clock cycle of 0.66 ns.

For P2, 1 + 0.06*78 + 0.36*0.06*78 = 7.3648 ~= 7.36

Each instruction takes 6.63ns with a clock cycle of 0.9 ns.

Similarly, P2 has a CPI of 7.36 and an average of just 6.63ns/instruction

5.10.4.

5.62/0.66= 8.52 → round up to 9 → L2 access takes 9 cycles
At least 1 cycle is needed for all memory accesses. 8% of memory accesses miss in the L1 cache and make an L2 access, so it takes 9 cycles. 95% of all L2 access are misses and needs a 107 cycle memory lookup.

AMAT: 1 + .08[9 + 0.95*107] = 9.85 cycles

Hence, AMAT is worse with the L2 cache.

5.10.5.
AMAT + %memory * (AMAT-1).
→ CPI for P1 with an L2 cache =9.85 * 0.36*8.85 = 13.04

5.10.6.
Focusing on AMAT is sufficient as the clock cycle time and % of memory instructions are the same for both variants of P1.
AMAT with L2 < AMAT with L1 only
1 + 0.08(9 + m*107) < 9.56
So L2 miss rate needs to be smaller than 0.916

5.10.7
P1's average time per instruction can't be less than 6.63 ns.
Then, we need (CPI_P1 * 0.66) < 6.63.
Then, we need CPI_P1 < 10.05; CPI_P1 = AMAT_P1 + 0.36(AMAT_P1 – 1)
Then, we nedd AMAT_P1+ 0.36(AMAT_P1-1) < 10.05
If AMAT_P1< 7.65, it occurs

Then , solve 1+ 0.08[9+ m*107] < 7.65
We find m < 0.693
Therefore, the miss rate at most is 69.3%

5.16.
5.16.1.

			TLB		
Adrdress	Virtual page	TLB H/M	Valid	Tag	Physical Page
4669(0*123d)	1	TLB miss PT hit PF	1	b	12
			1	7	4
			1	3	6
			1 (last access 0)	1	13
2227 (0*08b3)	0	TLB miss PT hit	1 (last access 1)	0	5
			1	7	4
			1	3	6
			1 (last access 0)	1	13
13916(0*365c)	3	TLB miss PT hit	1 (last access 1)	0	5
			1	7	4
			1 (last access 2)	3	6
			1 (last access 0)	1	13
34587(0*871b)	8	TLB miss PT hit PF	1 (last access 1)	0	5
			1 (last access 3)	8	14
			1 (last access 2)	3	6
			1 (last access 0)	1	13
48870(0*bee6)	b	TLB miss PT hit	1 (last access 1)	0	5
			1 (last access 3)	8	14
			1 (last access 2)	3	6
			1 (last access 4)	b	12
12608(0*3140)	3	TLB miss PT hit	1 (last access 1)	0	5
			1 (last access 3)	8	14
			1 (last access 5)	3	6
			1 (last access 4)	b	12
49225(0*c040)	c	TLB miss PT hit PF	1 (last access 6)	c	15
			1 (last access 3)	8	14
			1 (last access 5)	3	6
			1 (last access 4)	b	12

5.16.2.

			TLB		
Adrdress	Virtual page	TLB H/M	Valid	Tag	Physical Page
4669(0*123d)	1	TLB miss PT hit	1	11	12
			1	7	4
			1	3	6
			1 (last access 0)	0	5
2227 (0*08b3)	0	TLB hit	1	11	12
			1	7	4
			1	3	6
			1 (last access 1)	0	5
13916(0*365c)	0	TLB hit PT hit	1	11	12
			1	7	4
			1	3	6
			1 (last access 2)	0	5
34587(0*871b)	2	TLB miss PT hit PF	1 (last access 3)	2	13
			1	7	4
			1	3	6
			2	0	5
48870(0*bee6)	2	TLB hit PT hit	1 (last access 4)	2	13
			1	7	4
			1	3	6
			1 (last access 2)	0	5
12608(0*3140)	0	TLB hit PT hit	1 (last access 4)	2	13
			1	7	4
			1	3	6
			5	0	5
49225(0*c040)	3	TLB miss PT hit PF	1 (last access 4)	2	13
			1	7	4
			1 (last access 6)	3	6
			1 (last access 5)	0	5

A larger page size lowers the TLB miss rate but increases fragmentation and reduces physical memory utilization.

5.16.3.

					TLB			
Adrdress	Virtual page	Tag	Index	TLB H/M	Valid	Tag	Physical Page	Index
4669(0*123d)	1	0	1	TLB miss PT hit PF	1	b	12	0
					1	7	4	1
					1	3	6	0
					1 (last access 0)	0	13	1
2227 (0*08b3)	0	0	0	TLB miss PT hit	1 (last access 1)	0	5	0
					1	7	4	1
					1	3	6	0
					1 (last access 0)	0	13	1
13916(0*365c)	3	1	1	TLB miss PT hit	1 (last access 1)	0	5	0
					1 (last access 2)	1	6	1
					1	3	6	0
					1 (last access 0)	1	13	1
34587(0*871b)	8	4	0	TLB miss PT hit PF	1 (last access 1)	0	5	0
					1 (last access 2)	1	6	1
					1 (last access 3)	4	14	0
					1 (last access 0)	1	13	1
48870(0*bee6)	b	5	1	TLB missPT hit	1 (last access 1)	0	5	0
					1 (last access 2)	1	6	1
					1 (last access 3)	4	14	0
					1 (last access 4)	5	12	1
12608(0*3140)	3	1	1	TLB hit PT hit	1 (last access 1)	0	5	0
					1 (last access 5)	1	6	1
					1 (last access 3)	4	14	0
					1 (last access 4)	5	12	1
49225(0*c040)	c	6	0	TLB miss PT hit PF	1 (last access 6)	6	15	0
					1 (last access 5)	1	6	1
					1 (last access 3)	4	14	0
					1 (last access 4)	5	12	1

5.16.4.

					TLB			
Adrdress	Virtual page	Tag	Index	TLB H/M	Valid	Tag	Physical Page	Index
4669(0*123d)	1	0	1	TLB miss PT hit PF	1	b	12	0
					1	0	13	1
					1	3	6	2
					0	4	9	3
2227 (0*08b3)	0	0	0	TLB miss PT hit	1	0	5	0
					1	0	13	1
					1	3	6	2
					0	4	9	3
13916(0*365c)	3	0	3	TLB miss PT hit	1	0	5	0
					1	0	13	1
					1	3	6	2
					1	0	6	3
34587(0*871b)	8	2	0	TLB miss PT hit PF	1	2	14	0
					1	0	13	1
					1	3	6	2
					1	0	6	3
48870(0*bee6)	b	2	3	TLB miss PT hit	1	2	14	0
					1	0	13	1
					1	3	6	2
					1	2	12	3
12608(0*3140)	3	0	3	TLB hit PT hit	1	2	14	0
					1	0	13	1
					1	3	6	2
					1	0	6	3
49225(0*c040)	c	3	0	TLB miss PT hit PF	1	3	15	0
					1	0	13	1
					1	3	6	2
					1	0	6	3

5.16.5.
Without a TLB, nearly every memory access would need two RAM accesses: one to the page table and followed by one to the requested data.

6.7.
6.7.1.

x	y	w	z
2	2	1	0
2	2	3	0
2	2	5	0
2	2	1	2
2	2	3	2
2	2	5	2
2	2	1	4
2	2	3	4
3	2	5	4

6.7.2.
We could create synchronization instructions after each operation thus all cores on all nodes receive the same value.

6.9.
6.9.1.

Core 1	Core 2
A3	B1,B4
A1,A2	B1,B4
A1,A4	B2
A1	B3

6.9.2.

Core 1	Core 2
A3	B1,B4
A1,A2	B1,B4
A1,A4	B2
A1	B3

6.9.3.

FU1	FU2
A1	A2
A1	
A1	
B1	B2
B1	
A3	
A4	
B2	
B4	

6.9.4.

FU1	FU2
A1	B1
A1	B1
A1	B2
A2	B3
A3	B4
A4	