An UHF RFID Tag Emulator for Precise Emulation of the Physical Layer

Michael Winkler [#1], Thomas Faseth [#], Holger Arthaber [#], Gottfried Magerl [#]

[#] *Institute of Electrodynamics, Microwave and Circuit Engineering, Vienna University of Technology*
Gusshausstrasse 25/354, 1040 Vienna, Austria
[1] michael.winkler@tuwien.ac.at

***Abstract*— In this paper the implementation of a configurable hardware for an UHF RF identification (RFID) tag emulator at 868 MHz is demonstrated. The tag emulator is used for reader performance verification under worst case conditions. The characteristics of a tag can precisely be emulated: reflection coefficient dependent on received signal strength, variation of the frequency, and timing jitter of the backscattered signal. The implemented tag emulator is segmented into an RF transceiver board and a baseband processing board with a powerful field programmable gate array (FPGA). Both boards are connected by optical links to not influence the electromagnetic field. The compact low power RF transceiver board is placed in the reader's electromagnetic field and is optically powered. The baseband processing board handles the signal processing for the implemented backscatter modulator and evaluates and monitors the signal strength and signal characteristics received by the reader. For being prepared to upcoming standards, an I/Q backscatter modulator with a variable modulation index is implemented. The higher protocol layers are processed by a microcomputer for rapid prototyping. In this paper the underlaying hardware, the synchronization algorithm for the optical links, and the modulator properties of the UHF RFID tag emulator are discussed.**

I. Introduction

UHF RFID technology is used in a lot of applications. The implementation in supply chain and warehouse management systems optimizes business scenarios and saves plenty of money [1][2]. RFID works reliably and is established in tolling and access systems. RFID reduces human errors in medical applications and lives can be saved. All components have to be tested intensively during research, engineering, and production to guarantee a working UHF RFID system. In order to determine system margins existing RFID installations have to be verified under worst case conditions. For these applications a tag emulator can be used. The implementation of a configurable hardware for an UHF RFID tag emulator at 868 MHz for different test applications is depicted in this paper. The concept and the implementation is presented in Sec. II. The synchronization algorithm for the data links is demonstrated in Sec. III. The implementation of the I/Q backscatter modulator is shown in Sec. IV.

II. The UHF RFID Tag Emulator Concept

A. Basic Requirements

Existing tag emulators measure the RF field strength of the downlink (reader to tag) signal at a single moment [3] and no detailed information about the signal characteristics is given. It is impossible to monitor the pulse shape and the modulation depth of the downlink signal. A tag varies its backlink frequency and the response time of the tag to reader commands jitters [4]. Additionally, the reflection coefficient of a tag depends on the received signal strength [5].

The tag emulator presented in [3] changes its reflection coefficient only between two states. The signal processing is done by a simple microcomputer. The tag's behavior can be emulated just on logical level but performance verification under worst case conditions is not possible. Complex signal processing is needed for correct emulation of the physical level. Upcoming new generations of readers for quadrature amplitude modulated (QAM) backscatter RFID signals cannot be tested by the emulator presented in [3].

It is essential that the characteristics of a tag can be precisely reproduced by the tag emulator not just on the logical level but also on the physical level. Adequate computing power is required resulting in high power consumption. A battery supply is impractical because of the rapid discharge of the battery. A power supply via copper cables would influence the field pattern. This can be avoided by using an optical power supply.

The tag emulator presented in this paper is partitioned into an RF transceiver board and a baseband processing board. The complex signal processing for the downlink and the uplink (tag to reader) signal is implemented on the baseband processing board where power consumption does not matter. The RF transceiver board is placed into the reader's field and is optically powered. Therefore, it has to be optimized for low power consumption and small area to avoid distortion of the field of the tag antenna. An antenna-coupled link between reader and tag emulator is useful because existing RFID installations can be evaluated. The RF transceiver board and the baseband processing board are connected by two optical links which do not influence the electromagnetic field [6].

A power detector with an appropriate dynamic range is needed for monitoring the received downlink signal over a wide distance between reader and tag. The downlink signal has to be sampled with a suitable analog to digital converter (ADC) bandwidth and resolution to evaluate signal characteristics like modulation depth, pulse shape, and pulse width. Important conclusions about the downlink budget can be drawn.

It is important that the reflection coefficient of the backscatter modulator is continuously changeable for evaluation of the

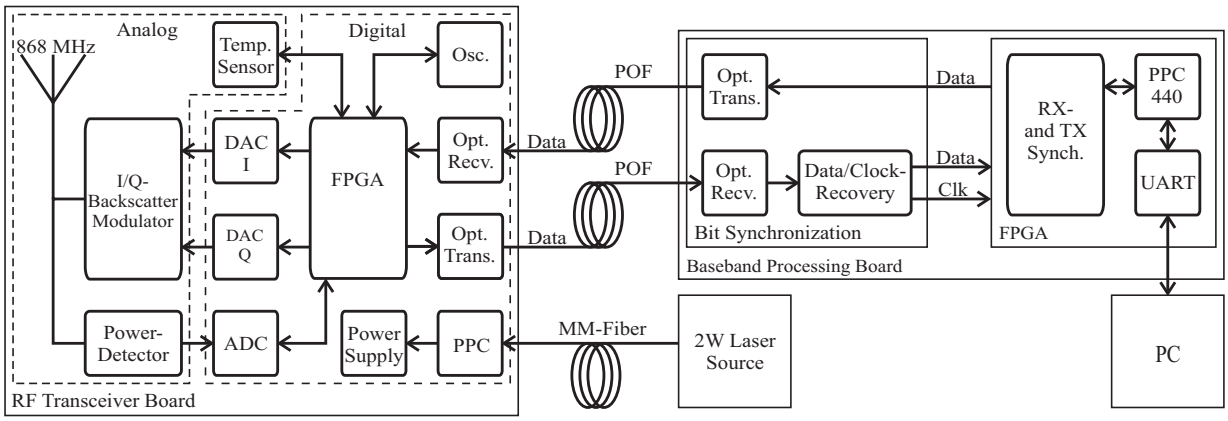

Fig. 1. Block diagram of the UHF RFID tag emulator.

reader's sensitivity and for performance optimization. In order to enable pulse shaping of the backscattered signal a sufficient digital to analog converter (DAC) resolution has to be considered.

Furthermore, the modulator needs to generate a reflection coefficient in the I/Q plane. On the one hand readers for upcoming QAM backscatter RFID signals can be tested by this hardware. On the other hand a power dependent reflection coefficient trajectory can also be emulated. Additionally, an I/Q backscatter modulator is used for emulating a moving tag by rotating the reflection coefficient's phase.

B. Technical Implementation

Fig. 1 shows the block diagram of the UHF RFID tag emulator. The two main components are the baseband processing and the RF transceiver board. The autonomous baseband processing board is a Xilinx ML507 Evaluation Platform with a Virtex5 FPGA where a Power PC 440 (PPC440) is included. Higher protocol layers can be elegantly implemented by the PPC440 in software. The tag emulator can be flexibly adapted for rapid prototyping and different test applications. Additionally, an interface to a PC is implemented. The RF transceiver board is placed into the reader's field like a common tag. The antenna is a dipole antenna with capacitive end loading which shortens the length of the dipole (Fig. 2 Analog). The antenna is designed for 868 MHz, the detuning effects by the digital part of the RF transceiver printed circuit board (PCB) (Fig. 2 Digital) and the heat sink is optimized in simulations.

A power detector with a dynamic range of –50 ... –5 dBm monitors the strength of the downlink signal received by the antenna. This power detector signal is sampled by a 10 Bit/3 MSps ADC. Downlink signals for existing standards, EPC Class-1 Gen-2 [4] for example, are sampled with an suitable bandwidth.

In order to evaluate the reader's sensitivity under worst case conditions and to enable pulse shaping of the uplink a backscatter modulator with continuously changeable reflection coefficient is implemented. An I/Q backscatter modulator (Sec. IV in detail), which is controlled by two 8 Bit/6 MSps DACs, is implemented for supporting upcoming standards and for the purpose of emulating a moving tag or an input power dependent reflection coefficient. Thus, sufficient bandwidth for existing [4] and upcoming standards is guaranteed.

Extensive baseband processing can be done by the baseband processing board. Important parameters of the downlink signal can be evaluated. The uncertainty of the backlink frequency and the timing jitter of the backscattered signal can be emulated with high resolution. Otherwise, the pulse shaping of backscattered signal can be studied.

The data transfer between the RF transceiver board and the baseband processing board is implemented by two unidirectional optical links with a data rate of 120 Mbit/s. The optical receiver and transmitter operates at a wavelength of 670 nm. Plastic optical fibers (POFs) were used in order to not influence the electromagnetic field [6]. An effective frame synchronization algorithm for the two data links is presented in Sec. III.

The power consumption of the operating RF transceiver board is about 450 mW. It is powered by a photonic power converter (PPC), cooled by a heat sink, which is driven by a 2 W 830 nm laser source. The PPC and the laser source are connected via a 62.5 μm multi mode (MM) fiber.

In Fig. 2 a prototype of the RF transceiver board is illustrated.

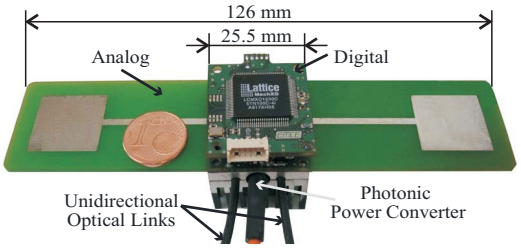

Fig. 2. A photograph of the prototype of the RF transceiver board.

The transceiver's RF components and a temperature sensor are implemented on the analog part of the PCB (Fig. 1 Analog). The temperature sensor's data can be used for correction of the influence of the temperature sensitive RF components. The remaining components including power supply, FPGA,

ADC et cetera are implemented on the digital part of the PCB (Fig. 1 Digital) which is stacked on the analog PCB. This modular design has got the important advantage of small area consumption compared to the wavelength. Moreover, a new antenna or modulator design does not influence the rest of the hardware.

III. A Robust Synchronization Algorithm

If independent clocks are used by the RF transceiver- and the baseband processing board for the frame synchronization of the optical links, frame sync in short, the complexity of the synchronization algorithm increases. The basic idea is that the FPGA of the RF transceiver board is the clock master and the whole synchronization is done by the baseband processing board. The FPGA on the transceiver board works exclusively with the bit clock and oversampling is avoided. No further synchronization logic is needed and power consumption is low. The baseband processing board derivates it's system clock from the 120 MBit/s RX frame by the data/clock recovery unit (Fig. 1). The frame sync of the two 8b10b encoded [7] optical

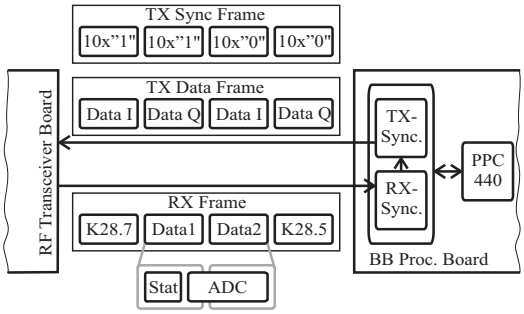

Fig. 3. Framing structure of the TX and RX data.

links is implemented in two steps. First, the bit synchronous system clock is used by the baseband processing board for byte- and frame sync by detecting the special characters K28.7 and K28.5 [7] in the RX frame (Fig. 3). Status bits from the RF transceiver board and RX ADC data are extracted by the hardware, after the baseband processing board is synchronous to the frame and no frame errors are detected.

Then, the TX synchronization unit is enabled in a second step (Fig. 3). The main unit here is a FPGA logic which is able to shift the TX frame in subsamples of the system clock. This mechanism is used for searching the sampling point of the first bit in the TX frame. This sampling point is further named the ideal sampling point T_{is} because if it is guaranteed that the FPGA samples the TX frame on the ideal sampling point, the RF transceiver board is bit– and frame sync simultaneously. The further processing logic saves rare logic and power because it is simple. The searching algorithm uses two status bits extracted from the RX frame. One status bit is the sampled first bit of the TX data which is echoed to the baseband processing board. If the TX data is not synchronized, no valid data is decoded by the FPGA on the RF transceiver board and an error flag is transmitted to the baseband processing board by the second status bit. The FPGA on the baseband processing board stops transmitting the TX data frame and starts transmitting the TX sync frame (Fig. 3) and searching the ideal sampling point T_{is}. For this

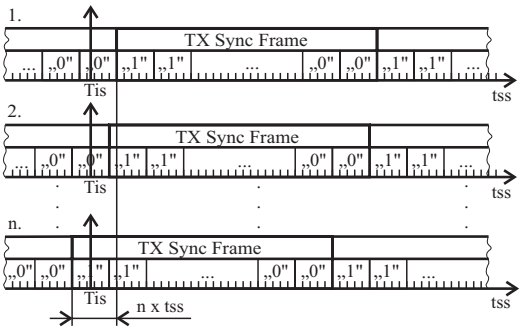

Fig. 4. Searching the ideal sampling point T_{is} by shifting the TX sync frame in steps of subsamples t_{ss} of the system clock.

reason, every starting frame is shifted stepwise by a subsample t_{ss} (Fig. 4). Simultaneously the sampled and echoed bit in the status data is observed. A detected rising edge indicates that the first bit of a TX sync frame is found at this point. Furthermore, the TX frame is shifted again by a half bit length to ensure that the bit is sampled in the middle. Thus, different delays of the TX signal caused by variable cable lengths are considered. The ideal sampling point is found and the FPGA on the baseband processing board starts transmitting data for the I/Q backscatter modulator again (Fig. 3).

IV. A Compact Low Power I/Q Backscatter Modulator

A. Theory of Operation

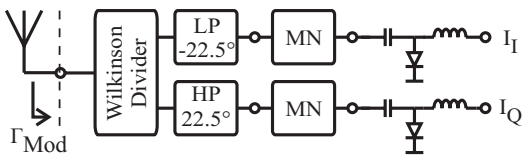

Fig. 5. A block diagram of the I/Q backscatter modulator.

The block diagram of the backscatter modulator is depicted in Fig. 5. In order to achieve I/Q modulation the input signal from the antenna is split by a Wilkinson divider. The isolation of the Wilkinson divider is needed for functionality. The low pass (LP) filter, the high pass (HP) filter, each implemented in T-structure, and the PIN-diodes permit a theoretical reflection coefficient $-1/2 < \Re(\Gamma_{\text{Mod}}) < 1/2$ and $-1/2 < \Im(\Gamma_{\text{Mod}}) < 1/2$ [8]. The structure with the two filters guarantees symmetrical paths on the prototype board, hence the alternative with a single $45°$ filter is avoided. The models for passive components in the filters were provided by Modelithics Inc. The control range of the reflection coefficient in practice is limited by the PIN-diodes which are controlled by the bias current I_I and I_Q. It is difficult to implement small/high resistance values with limited power consumption and circuitry. The parasitic diode capacitances lead to a reflection coefficient that is not

symmetric to the origin of the smith chart any more and additionally, the coordinate system is deformed. These effects are compensated by a matching network (MN), implemented by a parallel inductor.

B. Measurement Results

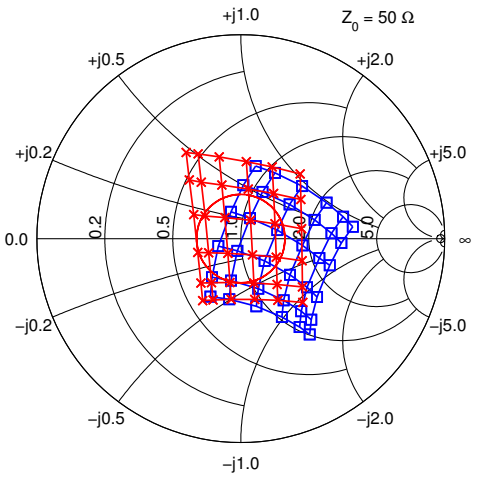

Fig. 6. Measurement results of the input reflection coefficient Γ_{Mod}. Crosses marks modulator with matching network. Squares marks modulator without matching network.

The main focus for the design of the I/Q backscatter modulator is low power and small area consumption. The power consumption of the modulator including the appropriate control circuitry (excluding the DACs and FPGA logic) is $P_{\text{Mod}} \approx 80mW$. The measurement results of the input reflection coefficient for two different modulator prototypes are depicted in Fig. 6. The reference plane is shown in Fig. 5. The squares illustrate the results of the modulator without a matching network. The influence of the parasitics of the diodes is obvious. The results of the modulator including a matching network are marked by crosses and are also shown in Fig. 6. The effects caused by the parasitic elements of the diodes are well compensated. The control range of the reflection coefficient is nearly symmetrical to the origin and the deformation is clearly reduced. The unbalance in the control range, especially for $\Re(\Gamma_{\text{Mod}}) < 0$, indicates that one path including splitter and filter has more insertion loss and/or different control behavior of the diodes. The phase shift of the filters is not exactly $22.5°$ and $-22.5°$. The axes of the coordinate system are not perfectly orthogonal which can be corrected by an additional calibration. The input reflection coefficient which can be achieved for any phase is $|\Gamma_{\text{Mod}}| \leq 0.22$ in maximum (marked by a circle in Fig. 6).

V. Conclusions

In this paper the implementation of a flexible hardware for an UHF RFID tag emulator for 868 MHz is demonstrated. The emulator is planned to be used for reader performance evaluation under worst case conditions. Hence, it is essential that the tag's behavior can be precisely emulated on the physical layer. The required extensively baseband processing results in high power consumption. The presented tag emulator is partitioned in a RF transceiver board and a baseband processing board. The implementation of the optical powered low power RF transceiver is very compact in order to not influence the electromagnetic field. The reader downlink signal is monitored by a power detector and sampled by an ADC with suitable bandwidth and resolution. In order to emulate a moving tag, QAM backscatter modulation, and a downlink signal strength dependent reflection coefficient an I/Q modulator is implemented which is controlled by two DACs with sufficient bandwidth and resolution for existing and upcoming UHF RFID standards. An input reflection coefficient of $|\Gamma_{\text{Mod}}| \leq 0.22$ was achieved for every phase.
The signal characteristics of the downlink signal can be evaluated by the baseband processing board which also handles the extensive signal processing for the modulator DACs. The frequency variation and the timing jitter of the backscatter signal can be emulated according to the standards. Higher protocol layers can be elegantly implemented in software by the PPC440 which allows rapid prototyping. The RF transceiver and the baseband processing board are connected via optical links in order to not influence the electromagnetic field. The synchronization algorithm is shown for both up- and downlink.

Acknowledgment

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