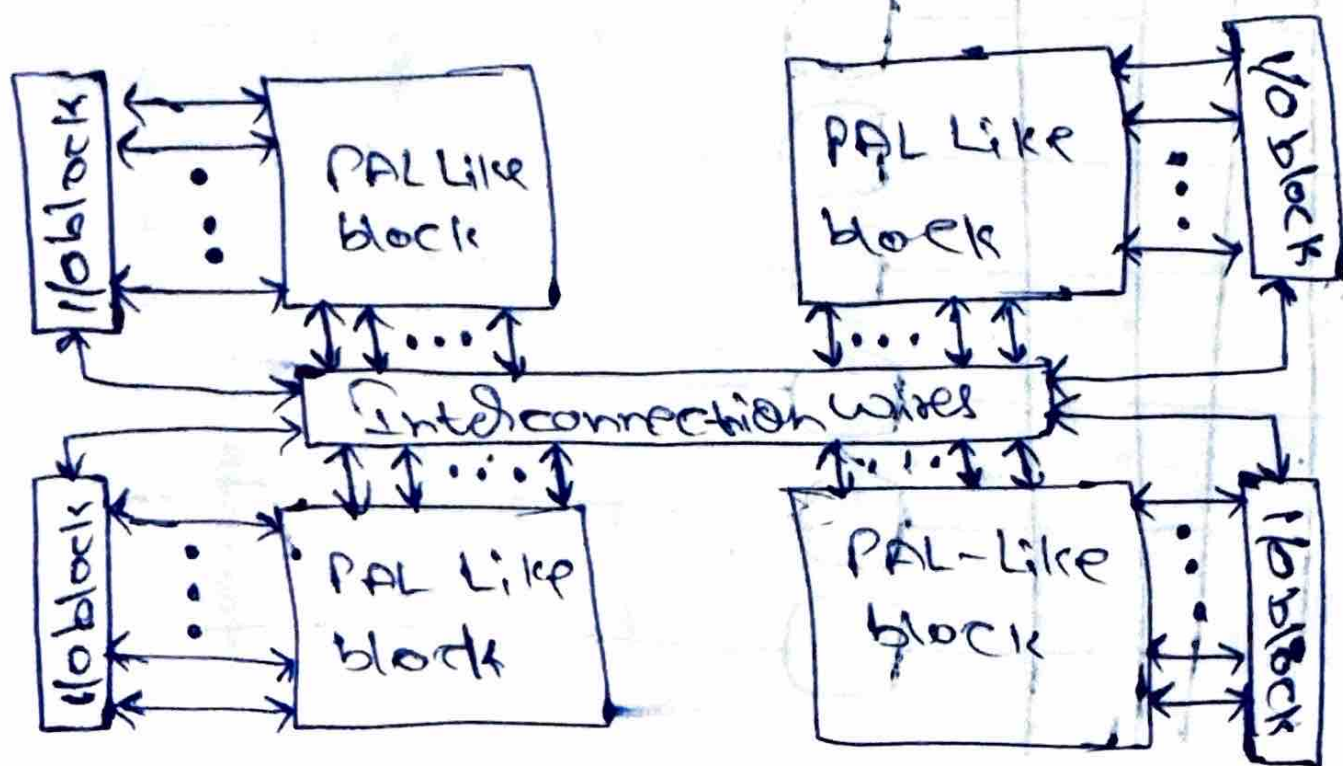


CPLD:

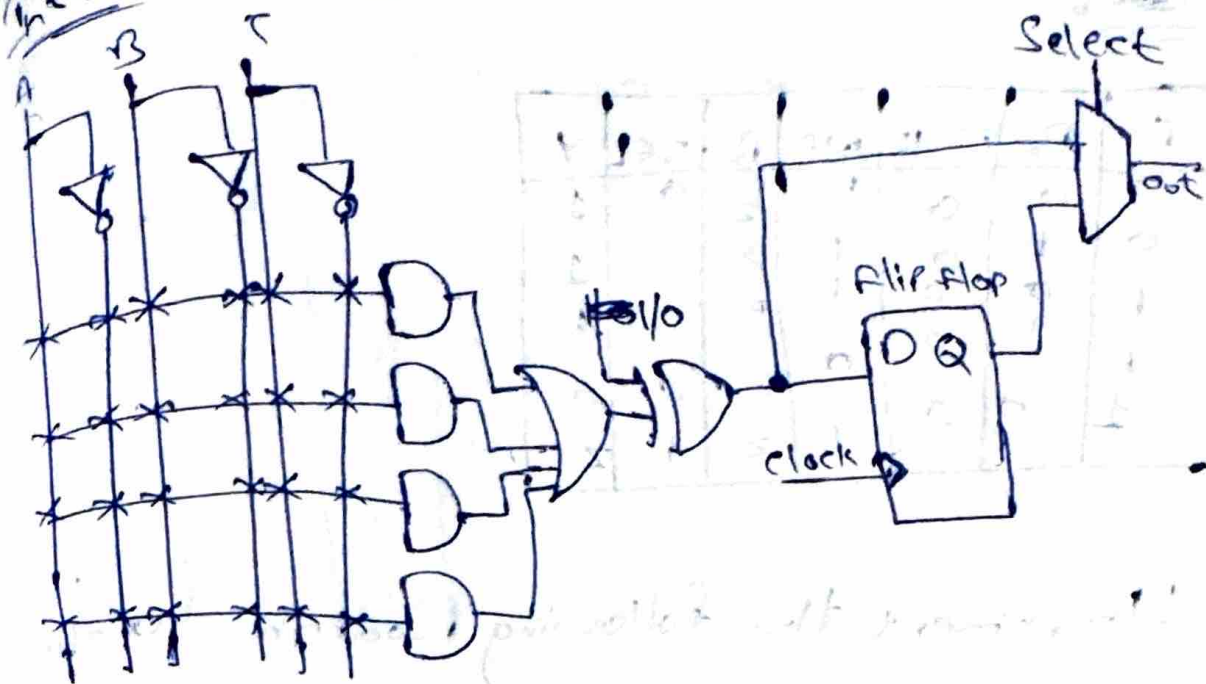
CPLD stands for Complex Programmable Logic Device.

Where we can integrated on multiple Programmable

ARCHITECTURE OF CPLD

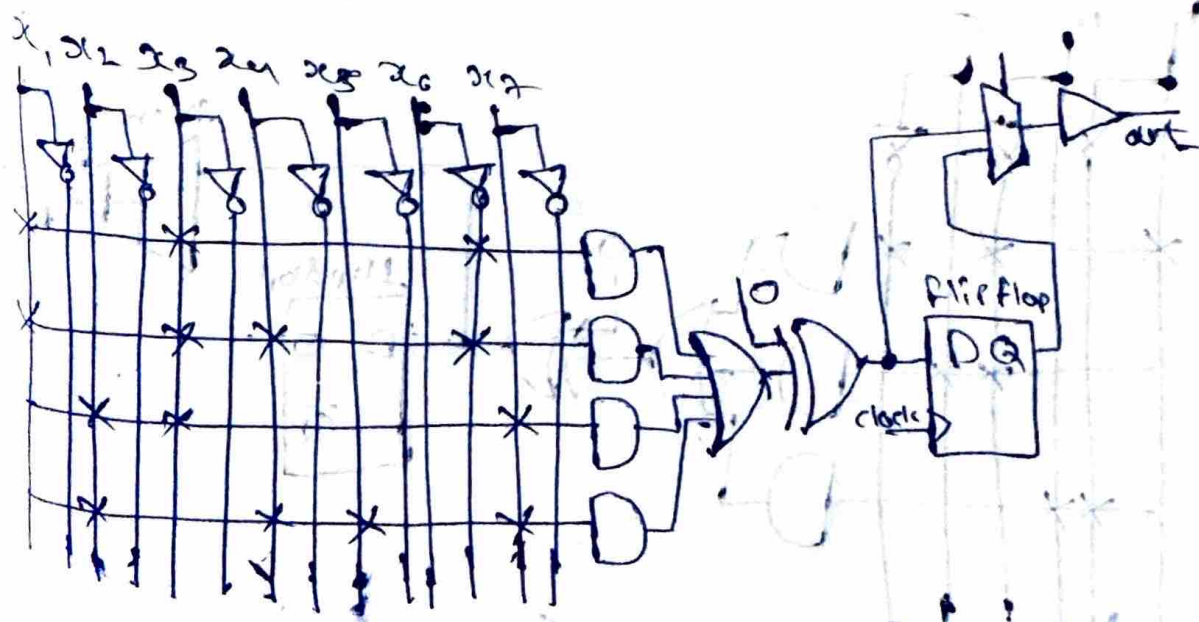


Internal Structure of CPLD



Implement the given function using the macrocell or CPLD.

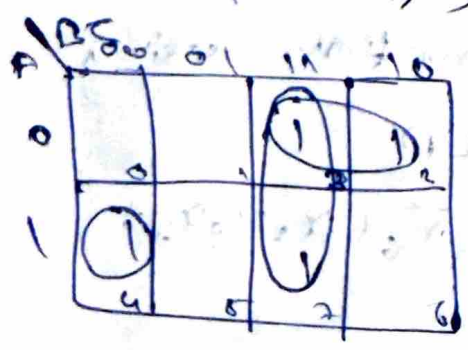
$$F = x_1 x_3 \bar{x}_6 + x_1 x_4 x_3 \bar{x}_6 + x_2 x_3 x_7 + x_2 x_4 x_5 x_7$$



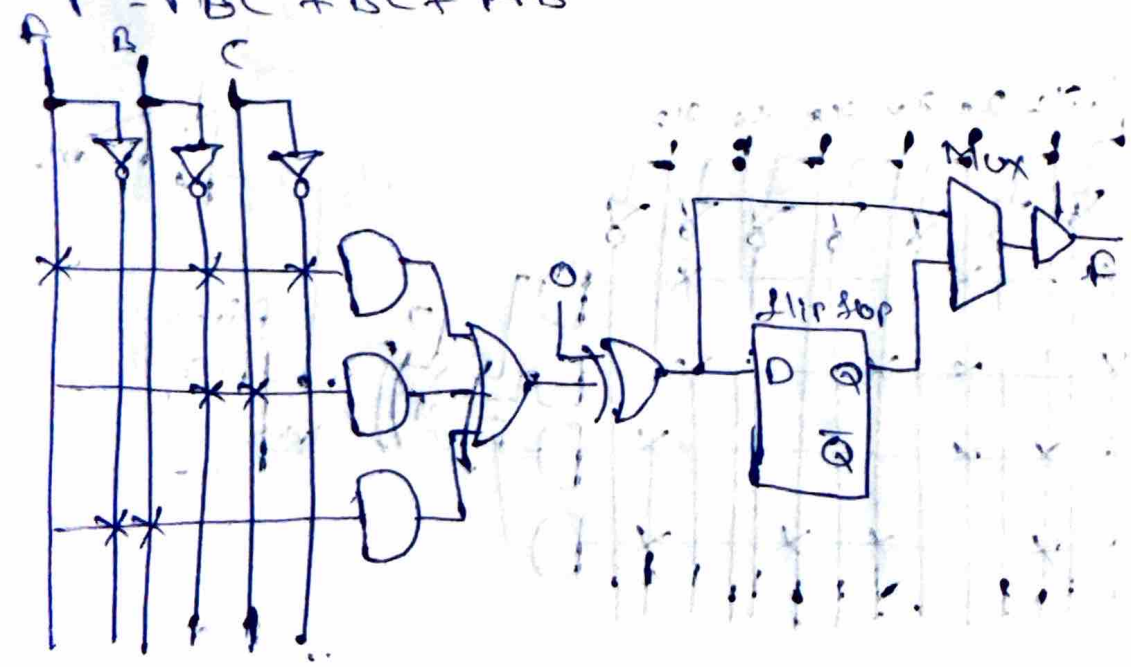
Q.:

A	B	ZLR	NR	R	SEL	Y
0	0	0	1	2	0	1
0	1	0	1	2	0	1
1	0	0	1	2	0	1
1	1	0	0	2	0	0
1	0	0	1	2	1	2

Implement the following Boolean function
 $F = \sum m(2, 3, 4, 7)$ using macro-cell



$$F = \overline{A}\overline{B}\overline{C} + BC + \overline{A}B$$

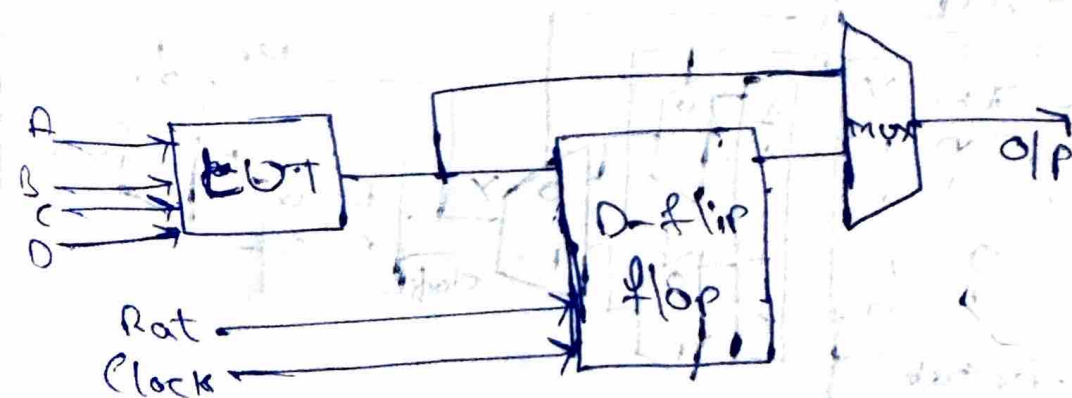


A	B	C	clk	RNR	R	SEL	o/p
0	0	0	0	0	z	0	0
0	0	1	0	0	z	0	0
0	1	0	0	1	z	0	1
0	1	1	0	1	z	0	1
1	0	0	0	1	z	0	1
1	0	1	0	0	z	0	0
1	1	0	0	0	z	0	0
1	1	1	0	1	z	0	1

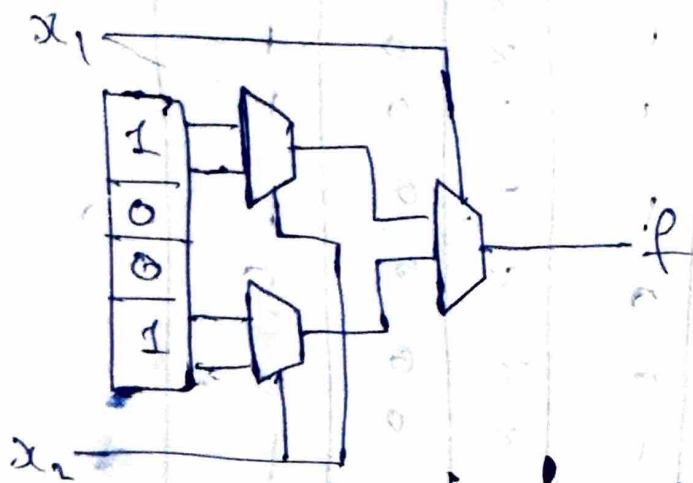
Applications of CPLD

- ① CPLD are ideal for high performance circuit control applications.

Configurable logic: Block (CLB) %



Look up table (LUT)



2ⁿ Single bit SRAM memory cells followed by a 2ⁿ-1

Implement the CLD for the given Boolean

$y = A \cdot B$ or $y(A, B) = \sum m(0, 1, 2)$

APGA: CLB

