FinFETs (Fin Field-Effect Transistors)

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Abstract— The evolution of semiconductor technology necessitates advancements beyond traditional planar transistors, which face limitations at nanometer-scale dimensions. FinFET (Fin Field-Effect Transistor) technology addresses these challenges with improved electrostatic control, reduced leakage currents, and enhanced performance at smaller geometries. This report provides an in-depth exploration of FinFETs, covering their motivation, historical development, and widespread commercial usage. It delves into the device's physical structure, fabrication processes, and characterization techniques. Additionally, the report discusses the advantages, limitations, and future directions of FinFET technology, highlighting its crucial role in modern electronics and potential for continued innovation.

Index Terms— FinFET, semiconductor technology, planar transistors, electrostatic control, leakage currents, device performance.

I. INTRODUCTION

In the semiconductor technology field which rapidly evolves, standard planar transistors encounter many compelling limitations. As the manufacturing process gets smaller and smaller, these limitations only grow. The need and the contunious efforts of the industry brought many improvements to performance, power consumption, and scalability. FinFET (Fin Field-Effect Transistor) technology cam ina s an advancement that adresses the issues with greater electrostatic control, less leakage currents, and exceptional performance is small sizes. In the end, FinFETs became another way of sustaining Moore's Law and meeting the demands of modern electronic devices that grow day-by-day.

A. Motivation

The motivation for adopting the FinFET technology is its ability to overcome short channel effects, leakage current issues that increase as the channel length shortens, and worsened performance. FinFETs, with their 3D structure, provides better control over the channel and greatly reducing the leakage current, thus further lowering the power cost of the transsistor. This better control over the channel translates to higher switching speeds and better overall performance for the FinFET technology making them important for next-gen microprocessors, mobile devices, and other high performance computing applications.

B. History

In 1995, as Moore's Law—predicting the doubling of transistors on a chip every two years—faced potential limits, the semiconductor industry was worried about the future of miniaturization. Chenming Hu, a professor at the University of California, Berkeley, responded to DARPA's call for innovative solutions. Hu conceptualized the FinFET (Fin Field-Effect Transistor), featuring a raised channel that allows the gate to wrap around it on three sides, enhancing control and reducing leakage. This breakthrough design helped extend Moore's Law beyond the sub-100 nanometer scale [1].

Hu's journey began in Taiwan, where his early interest in science led him to study electrical engineering. Influenced by the potential of semiconductors, he pursued graduate studies at Berkeley. His work on semiconductor reliability, particularly the hot-carrier-injection theory and the Berkeley Reliability Tool (BERT), became industry standards. By the mid-1990s, Hu's insights into 3D transistor structures became critical as traditional designs approached their limits.

Motivated by DARPA's initiative, Hu's team developed the FinFET, demonstrating its manufacturability and viability for sub-25 nm transistors. Despite initial skepticism, Intel's adoption of FinFETs in 2011 confirmed their significance. Hu's vision ensured the continuation of Moore's Law, fostering ongoing innovation in the semiconductor industry [1].

C. Common Usage

FinFET technology is now commonly used in various applications, due to its superior performance and energy efficiency:

- Microprocessors and CPUs: Essential for modern computing applications, FinFETs enhance performance and efficiency in PCs, servers, etc..
- Mobile Devices: FinFETs extend battery life and boost performance in smartphones, and other portable devices.
- GPUs (Graphic Processing Units): Due to the improved performance, FinFETs are prefered for graphical processes, AI, and machine learning purposes.

Corresponding author: All authors contributed equally.

- Consumer Electronics: From TVs to wearable devices, FinFETs are used in various consumer devices.

As we can see from the examples, FinFETs are commonly used in products that need high performance at a lower energy consumption rate. We can say that they can be used almost anywhere instead of regular transistors.

D. Commercialization

FinFETs are a special kind of transistor used in making computer chips. They are differentiated by their have a thin, vertical fin instead of being flat like conventional planar devices. This change aids in reduction of power loss, switching times and enhanced scalability. FinFETs became really popular in chip production around 2010 due to their performance benefits in small circuits with 14, 10 or 7nm process nodes [2].

II. DEVICE PHYSICS AND STRUCTURE

FinFETs are field-effect transistors. FinFETs are a transistor technology that further improves the performance limitations of MOSFETs. Especially the performance of low-sized MOSFET transistors decreases due to the leakage current below the threshold. These disadvantages are definitely not at an acceptable level at 10 to 20 nm sizes. To put it more generally, when MOSFET transistors are off (cut off), the current they flow increases considerably. At this point, FinFET technology comes into play. Figure 1 shows a Planar MOSFET.

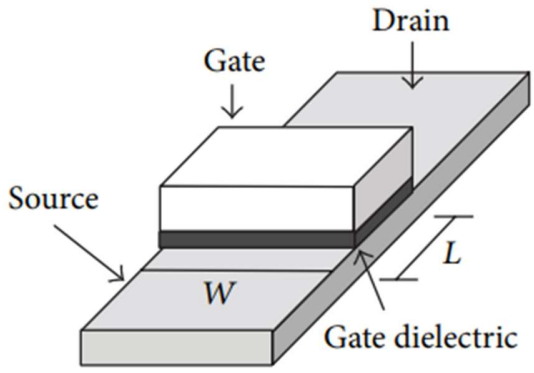

Fig. 1: Regular MOSFET [3]

FinFET differs from the structure of planar MOSFET in that it is not planar. So it has 3 dimensions. It is built on silicon substrate as seen in Figure 2. The structure seen in rectangular shape from the middle to the top is called FIN. This fin acts as a channel between the gate and source. In MOSFETs, the large distance between drain and source causes large dimensions. As the size decreases, the distance between the drain and source decreases and the short-channel effect comes into play, resulting in leakage currents. FinFETs have better short-channel effects than MOSFETs. The channel height H (fin) called fin in FinFET determines the width (w).

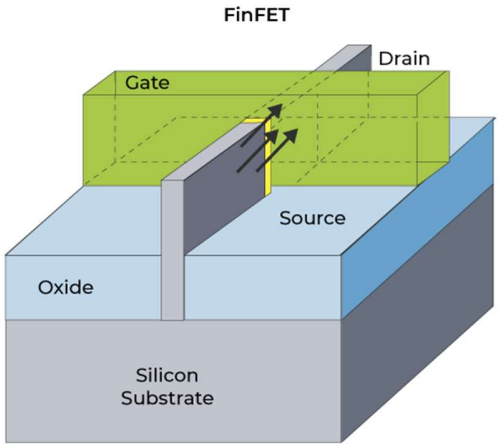

Fig. 2: Structures of FinFETs [4]

The height (H) of the FinFET seen in Figure 3 determines the behavior of the transistor. Although the length L in MOSFETs is the same as in FinFETs, W is very different. W is calculated as follows. W = 2Hfin + Tfin . Fin height determines current control, and width determines current carrying capacity. This shows that it is more controllable than Mosfet structures. Increasing height increases power consumption and provides better control. While increasing the width increases the current capacity, it consumes more energy. These two relationships must be well established during the production process steps. Thus, more stable designs are obtained. [3]

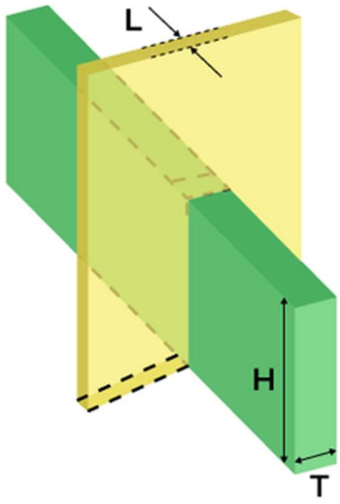

Fig. 3: FinFET, Fin and Gate Dimension [4]

- L = Gate Length
- T = Fin thickness
- H = Fin height

FinFETs can be examined under two main headings: gate numbers and substrate. Finfets with gates that are shortened in terms of the number of gates, both ends of the Gate are connected to each other. They have 3 doors and take up less space. It does not have threshold voltage control. FinFET structures with independent gates have 4 terminals, so the threshold voltage can be controlled. Gate ends are

not connected to each other. This structure 2 structure is shown in figure 4.

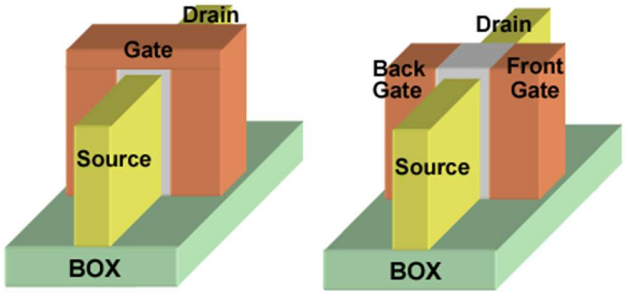

Fig. 4: Shorted and Independent Gate [5]

Finfets also vary depending on the Subsatrate type. It is known as Bulk FinFET and SOI FinFET. Bulk FinFET is similar to the bulk MOSFET structure in terms of substrate. Bulk FinFETs consume high power. SOI is more difficult to control than FinFET. Subthreshold voltage is not good compared to SOI. SOI FinFET, on the other hand, has a higher efficiency because it is a more controllable structure, but its production process is more complex. Figure 5 shows them more clearly.

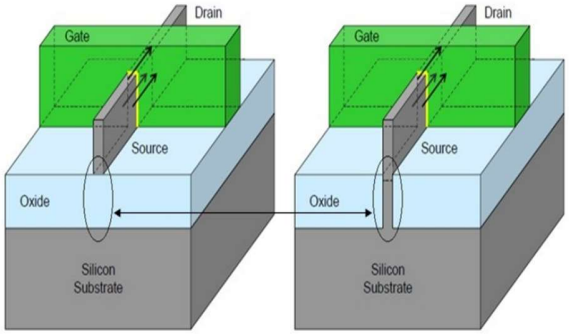

Fig. 5: Bulk FinFET and SOI FinFET [6]

These FinFET structures have become more efficient in terms of leakage currents in recent years. In terms of size, it takes up less space, making it highly preferable as it takes up less space and reduces energy efficiency and mass production costs.

III. DEVICE MICROFABRICATION PROCESS

As technology progresses, transistor sizes continue to diminish. This process, known as scaling, ensures the continuous advancement of the semiconductor industry. FinFETs, by offering new solutions when the limits of planar transistors are reached, contribute to the evolution of this process. While planar transistors encounter scaling challenges at 22 nm and smaller nodes, FinFETs demonstrate better performance. Despite offering better control through their 3D channel structure, they may require a more complex production process.
The manufacturing process can be explained in 7 steps:

A. Preparation of Wafer

The wafer is cleaned, and an oxide layer is applied to the surface. The basis of a FinFET is a slightly p-doped substrate with a hard mask on top, such as silicon nitride, and a patterned resist layer [N].

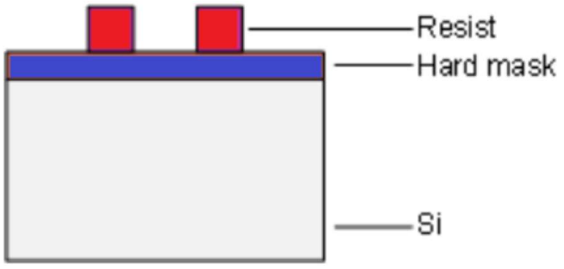

Fig. 6: Preparation of wafer [7]

B. Fin Etch

Fins are formed through a highly anisotropic etching process. This etching process must be time-based due to the wafer lacking a stop layer for the fins. In the 22 nm process, the width of the fins should ideally be 20 to 30 nm or higher.

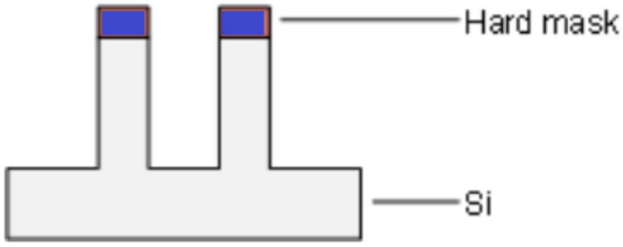

Fig. 6: Fin etching [7]

C. Deposition of Oxide

Materials layers such as gate dielectric, gate electrode, and source and drain regions are deposited onto the wafer. Techniques such as chemical vapor deposition or physical vapor deposition can be applied for this process.

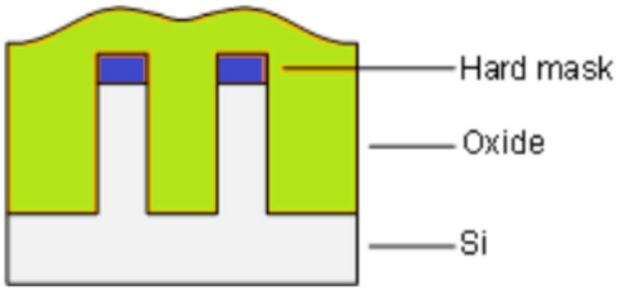

Fig. 7: Deposition of oxide [7]

D. Planarization

Primarily, it can be said that the initial raw wafers for fabrication of semiconductor device ideally need to be flat or planar. The planarization process is a technique, such as chemical mechanical polishing (CMP), that enhances the flatness of the semiconductor wafer.

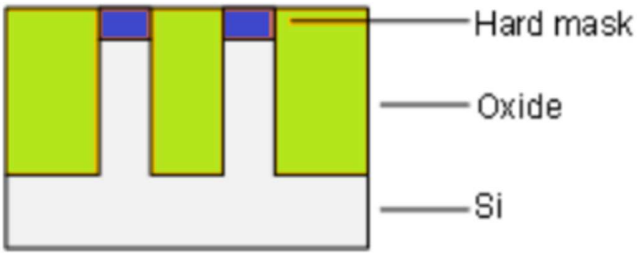

Fig. 8: Planarization [7]

E. Recess Etch

In the structure of the semiconductor, a recess is disposed in the first layer.

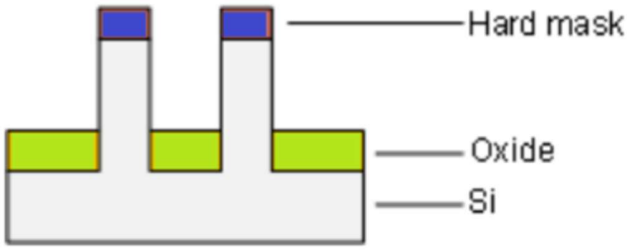

Fig. 9: Recess Etch [7]

F. Gate Oxide

The gate oxide is placed onto the fins after undergoing thermal oxidation. (Thus, the channel can be impressively separated from the gate electrode.) A dopant junction is established at the base of the fin through high-dose angled implantation, completing isolation as the fins stay connected underneath the oxide.

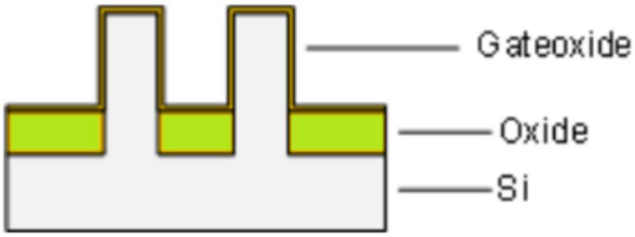

Fig. 10: Gate oxide [7]

G. Deposition of Gate

High level of n+-doped polysilicon layer is deposited above of the fins. Up to three gates, one on each side of each fin, and a third gate above wrapped around the channel. Gates should be wrapped around the channel considering the thickness of the gate oxide on top [7].

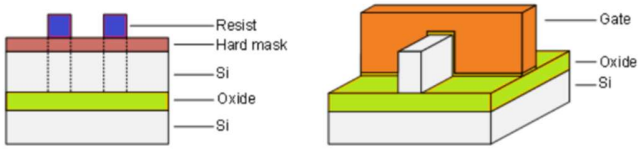

Fig. 11: Deposition of gate [7]

In Figure 12, an example FinFET and different cross-sections are depicted.

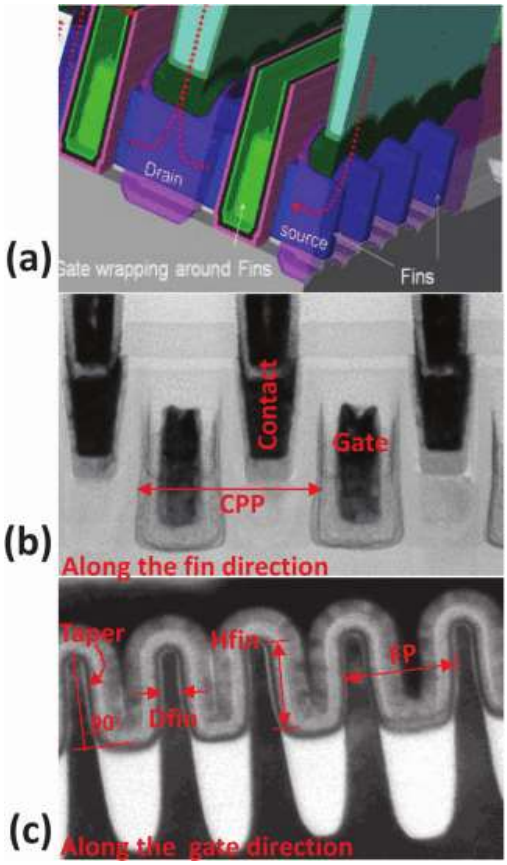

Fig. 12: (a) 3D view of finfet (b) cross-section along the fin (c) cross-section along the gate [8]

IV. WORKING PRINCIPLE DETAILS

FINFETs operate by using a fin-shaped channel as opposed to the planar channel seen in traditional MOSFETs. FinFETs have a vertically projecting fin-shaped channel that differs from the flat channel of planar transistors. With gate electrodes encircling the channel on three sides, the transistor's behavior can be more precisely controlled. A gate oxide layer, a gate electrode, and a gate insulator make up the gate structure.

In the channel region, an electric field is produced when a voltage is applied to the gate electrode. The current that flows across the channel is managed by this electric field. Better electrostatic control of the channel is made possible by the FINFET's unique design, which also lowers leakage current and enhances transistor performance overall. In this section, mathematical models and technologies of finfets will be discussed.

A. Mathematical/Theoretical Model

Model of Surface Potential:

DC bias facilities are used for field effect transistors (FETs). The area between the source and drain is called the channel or Si-body. The DC transition is controlled by the electrostatic potential in the channel. FinFET typically features storage of a three-dimensional surface. The following equation expresses the surface potential.

$$\frac{\delta^2\psi(x,y,z)}{\delta x^2}+\frac{\delta^2\psi(x,y,z)}{\delta y^2}+\frac{\delta^2\psi(x,y,z)}{\delta z^2}=\frac{qN_{\mathrm{ch}}}{\epsilon_{\mathrm{ch}}} \quad (1)$$

In this case, εch is the conductivity of the channel material and ψ is the surface potential, Nchis is known as the channel contribution. The following equation expresses the total surface potential.

$$\psi(x,y,z)=\psi_{sb}+E_{sb}\left(H_{fin}-x\right)+\frac{q}{2\varepsilon_{si}}N_A\left(H_{fin}-x\right)^2$$
$$+\sum_{r=1}^{\infty}\frac{1}{sin\,h(\gamma_r L_{eff})}[V_r'\sin h\,(\gamma_r y)+V_r\sin h\,(\gamma_r(L_{eff}-y))]$$
$$[\sin(\gamma_r x)+\frac{\varepsilon_{si}}{\varepsilon_{ox}}t_{oxf}\gamma_r\cos(\gamma_r x)]\sum_{s=1}^{\infty}P_{sr}[\sinh\{\chi_{sr}(T_{fin}-z)\}$$
$$+\sinh(X_{sr}z)]\frac{\sin(\alpha_s(y-L_{eff})}{\cos(\alpha_s L_{eff})}[\sin(\beta_r x)+\frac{\varepsilon_{si}}{\varepsilon_{ox}}t_{oxf}\beta_r\cos(\beta_r x)] \quad (2)$$

Threshold Voltage Model:

The threshold is the minimum voltage required for the MOSFET to turn on. It can be used to obtain equations similar to the following:

$$V_{TF}=V_{TF}^0-\Delta V_{TF}^1-\Delta V_{TF}^2 \quad (3)$$

an electrically regulated semiconductor device. In a FET, the electrostatic potential between the source and drain is produced by V^0_{TF}, ΔV^1_{TF} and ΔV^2_{TF}.

Drain Current Model:

The following equation can be used to express subthreshold current, or the tiny amount of drain current that can pass through the channel at a voltage below threshold, which is a crucial factor in assessing the performance of MOSFETs:

$$I_{\mathrm{DS}}=\frac{q\mu_n(kT/q)(n_i^2/N_a)[1-\exp(-V_{\mathrm{DS}}/(\mathrm{kT}/q))]}{\int_0^{\mathrm{L_{eff}}}(dy/\int_0^{H_{\mathrm{fin}}}\int_0^{W_{\mathrm{fin}}}\exp[q\psi(x,y,z)/\mathrm{kT}]\mathrm{dxdz})} \quad (4)$$

Transconductance:

The speed at which a transistor may activate when sweeping the gate voltage is determined by its conductance, which is directly correlated with gain. The increase in device sensitivity is caused by a larger transconductance value, which raises the drain current due to a change in surface charge. The highest transconductance gate voltage can be used to find a sensor's operation point. The majority of the examined devices exhibit maximal transconductances over 10 uS. The following formula can be used to define transconductance:

$$g_m=\frac{\mathrm{dI}_D}{\mathrm{dV_{GS}}} \quad (5)$$

- Drain Induced Barrier Lowering (DIBL):
  DIBL modifies the source-to-drain potential barrier, lowering the nanoscale MOS threshold voltage. As a result, lower gate voltages can be conducted by the device channel. The ratio of the threshold voltage recorded at the minimum value to the maximum priority of the drain current is used to compute the DIBL. A draininduced barrier lower is defined as a shift in threshold voltage (Vth) to alter in drain voltage (Vds).

$$\mathrm{DIBL}\,(\tfrac{\mathrm{mV}}{V})=\frac{\Delta V_{\mathrm{th}}}{\Delta V_{\mathrm{ds}}} \quad (6)$$

- Subthreshold Swing:
  The subthreshold swing, or drain current characteristics in the device's subthreshold region, can be used to assess the switching efficacy of low-power digital devices.
  Subthreshold swing is represented analytically by solving Poisson's equation in the channel region at cutline point x=Tf/2, y=Hfin.
  The swing expression below the threshold is:

$$S=[\frac{q}{2.3\mathrm{kT}}\frac{\partial\Psi(x,y,z)}{\partial V_{\mathrm{GS}}}]^{-1}$$
$$S=[\frac{q}{2.3\mathrm{kT}}(\frac{\partial\psi_{1D}}{\partial V_{\mathrm{GS}}}+\frac{\partial\psi_{2D}}{\partial V_{\mathrm{GS}}}|_{z=0}+\frac{\partial\psi_{2D}}{\partial V_{\mathrm{GS}}}|_{z=L_f}+\frac{\partial\psi_{3D}}{\partial V_{\mathrm{GS}}}|_{y=0}+\frac{\partial\psi_{3D}}{\partial V_{\mathrm{GS}}}|_{y=H_{\mathrm{ff}}})]^1 \quad (7)$$

Off Current:

Subthreshold Slope is directly related to off current (SS). It can be computed using the equation that follows:

$$I_{\mathrm{off}}=100\frac{W}{L}10^{-V_{\mathrm{Th}}/SSS} \quad (8)$$

Short Channel Effects in NC-FinFET:

In highly scaled FETs, negative capacitance is employed to offset short-channel effects [9]. The inverse subthreshold swing's critical short channel parameter can be expressed as:

$$\mathrm{SS} = 2.3\frac{K_B T}{q}\frac{\partial V_g}{\partial \psi_s} = 2.3\frac{K_B T}{q}\left(1+\frac{C_{\mathrm{dip}}}{C_{\mathrm{ox}}}\right) \quad (9)$$

B. Technology and Instruments

Similar transistors were created in 1990 and dubbed DELTA by Hisamoto and associates. SCEs dropped and channel control rose as a result of this arrangement. The three-gate architecture effectively reduces SCEs, as proved by Huang and colleagues' development of an 18 nm p-channel FinFET. by creating a 17 nm dual-port FinFET, Hisamoto et al. decreased SCEs. In order to scale current CMOS technology beyond the 50nm barrier, Huang and his colleagues discovered that sub-50nm dual-gate FinFETs exhibit exceptional short-channel performance. When Yu and his colleagues examined a dual-gate 10 nm FinFET, they discovered that the transistor's SCEs were substantially lower than those of traditional MOSFETs. The 40nm FinFET ash memory developed by Xuan and his colleagues featured lengthy storage times, good read and write speeds, and durability. By lowering the gate length to 5 nm, Yang and colleagues discovered decreased leakage current and gate latency in ultrascale nanowire FinFETs. Lederer and associates presented work on width to enhance FinFETs' AC performance.Kaneko and his colleagues minimized the barrier lowering and leakage current induced by drainage by using a ground plane. Nandi et al. discovered lower battery usage while examining the double-gate spacer layer's effect on power consumption. Following up on their investigation, Gaynor and colleagues demonstrated that the triangular n-shape might cut the leakage current of the device by as much as 70%. Narrower ns provide better protection against SCEs, according to Mohapatra and colleagues' analysis of the impact of n thickness and height on RF performance [10].

V. CHARACTERIZATION

A. Methods and Results

For analysis of FinFET devices threshold voltage approach [11] or a Keithley System 93 I-V setup operation under control of Metrics software [12] has been used. The former provides the different sections of operation with different solutions while the latter is practical experimentation and measurements.

The threshold voltage approach seperates the surface potential to three regions. These are the linear, saturation and cut-off regions.

In the linear region, for any given $V_g > V_t$, surface potential increases with V_{ds}. Drain-source current I_{ds} is approximated in [13, eq.(10)].

$$I_{ds} = 2\mu C_{ox}\frac{W}{L}\left(v_g - v_t - \frac{v_{ds}}{2}\right)v_{ds} \quad (10)$$

Where μ is the effective mobility in the channel impurity atoms, interface related imperfections, inversion region, C_{ox} is the oxide capacitance per unit area, W is the effective channel width, L is the effective channel length, V_t is threshold voltage, V_g is gate voltage and V_{ds} is drain to source voltage.

In the saturation region, I_{ds} is not related to V_{ds}. The value is approximated in [14, eq. (11)].

$$I_{ds} = \mu C_{ox}\frac{W}{L}\frac{\left(v_g - v_t\right)^2}{2m} \quad (11)$$

Where, $m = 1 + \frac{3T_{ox}}{X_d}$. X_d is the depletion region thickness and T_{ox} is the oxide thickness.

The cut-off region is where $V_g < V_t$, which collapses the channel, stopping any current flow. When V_g is lower than V_t, the drain current lowers exponentially. This current is referred to as sub-threshold current [11]. The sub-threshold current is approximated in [15, eq. (12)].

$$I_{dx} = \mu\frac{W}{L}kTn_i t_{si} e^{\frac{q(v_g-\Delta\phi)}{kT}}\left(1-e^{-\frac{qv_{dx}}{kT}}\right) \quad (12)$$

Where $\Delta\phi$ is the work function difference between the gate electrode and the almost intrinsic silicon body.

The output characteristics from the results obtained can be seen in [T, Fig.13]. This figure only includes the linear and saturation regions.

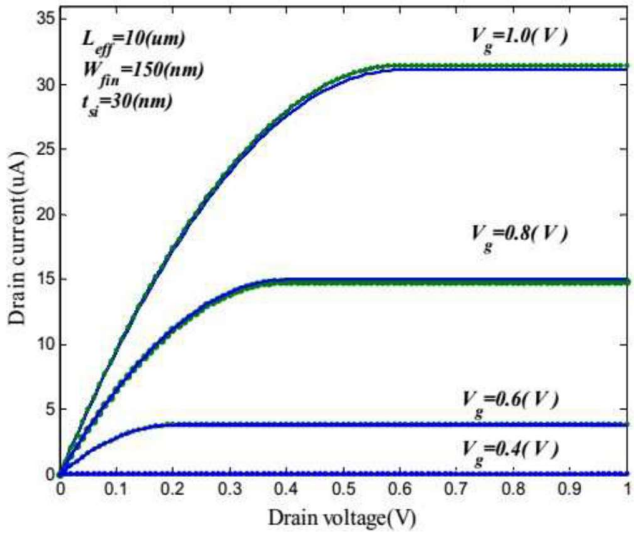

Fig. 13. Output characteristics of FinFET. Channel length is 10μm, the fin layer width is 150nm and the thickness is 30nm. The dotted line is from experiment data in [16] and the solid line is the theoretical data. [15]

The threshold voltage for a given FinFET can also be seen in [15, eq. (13)].

$$V_{th} = \phi + n\frac{kT}{q}\ln\left(\frac{2C_{ox}kT}{q^2 n_i t_{si}}\right) + \frac{h^2\pi^2}{2m_{dx}W_{si}^2} \quad (13)$$

Here, n denotes the number of channels.

The experimentation by Malinowski [12] was conducted on experimental devices with 2nm HfO_2 + 5 nm TiN gate stack.

Comparably very thin dielectric layered FinFET's were tested and both I_g and I_d measurements were obtained.

For low drain voltage the transfer and output characteristics of n-type and p-type FinFETs were measured. The measurements can be seen in [12, Figs.14-17]. Gate current is indicated to be a major parasitic effect [12] in the gate stack structure. The gate current I_g is exponentially dependent on gate voltage V_g. This indicates that it is related to the electric field and the inversion range. The figures can also show that n-type and p-type devices exhibited non-symmetrical threshold voltages. Doping errors and narrow channel (geometrical effect) effects can also be attributed to this change.

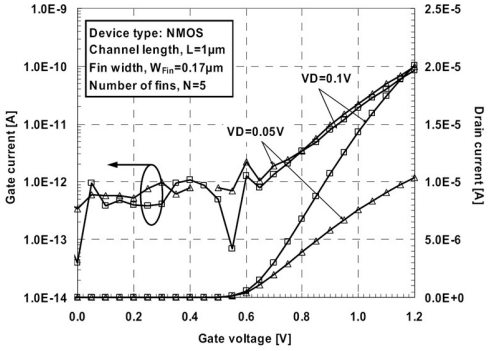

Fig. 14. Drain current and gate current in relation to gate voltage for a multifinger n-channel FinFET. [12]

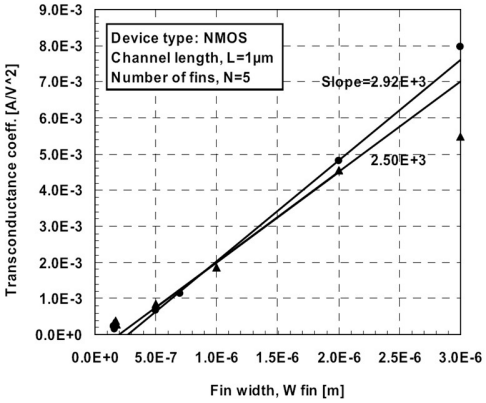

Fig. 15. Transconductance of n-channel FinFET with relation to fin width. Two identical sets of devices from two different chips were tested. [12]

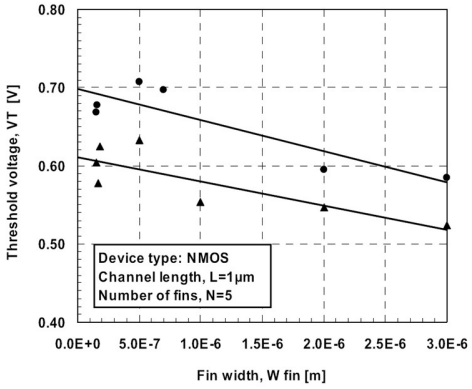

Fig. 16. n-channel FinFET threshhold voltage in relation to fin width. Two identical sets of devices from two different chips were tested. [12]

The most identifiable results of transconductance coefficient calculations are the dependence on fin width. The dependance is linear, however results also indicate that a difference between the projected and real fin width are different. These might come from errors in photolitography or etching processes. This difference is in the order of $0.2\mu m$.

From experimentation on two different devices, it can be seen that there is a certain dispersion of transconductance. Threshold voltage also shares this aspect and comparably narrower fins highlight this issue. The subthreshold slope and the mobility degradation factor vary significantly between devices. This variation can also be seen in wider finned FinFETs. Dispersion in the source/drain series resistance and/or the quality of the side fin walls and the line-edge roughness (LER) effect can be attributed to these issues [12].

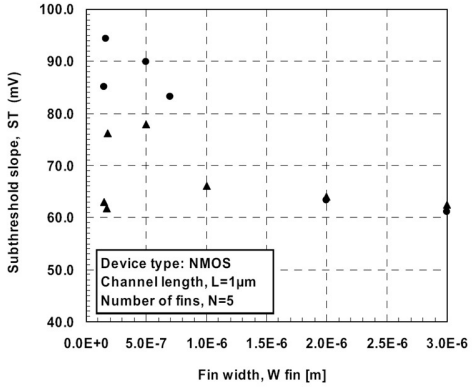

Fig. 17. n-channel FinFET subthreshold slope in relation to fin width. Two identical sets of devices from two different chips were tested. [12]

Gate current calculations by Malinowski [12] separate the gate current calculations into two parts. $J_{gate,top}$ and $J_{gate,side}$ can be expressed as the two major components. This calculation can be seen in [12, eq. (14)].

$$I_{gate} = W_{fin} \cdot L \cdot J_{gate,top} + 2 \cdot H_{fin} \cdot J_{gate,side} \tag{14}$$

This formula shows the linear correlation between I_{gate} and W_{fin}. The $J_{gate,top}$ component may be calculated as the slope of the regression line of $I_{gate} - W_{fin}$ plot, seen in [12, Fig 19]. The $J_{gate,side}$ component can be calculated point of intersecion of the regression line with the I_{gate} axis. The calculated R^2 value shows that I_{gate} and W_{fin} are linearly dependent and can be used to estimate gate current components.

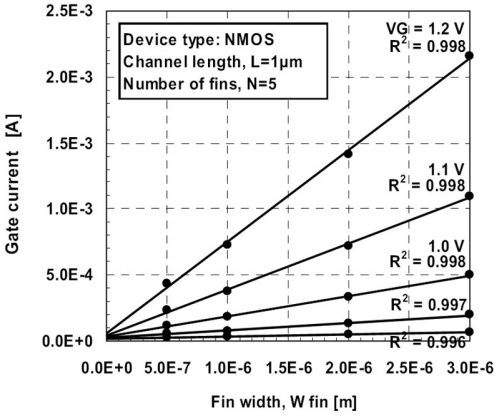

Fig. 19. n-channel FinFET dependance on fin width in relation to gate current. Different gate voltages were tested. This was done in the strong inversion range. [12]

The dependencies of the side gate current density $J_{gate,side}$ is notably weaker for electric field than the top component. This difference can be observed in [12, Fig. 20]. Fin narrowing also increases the side gate current, since less area is attributed in the fin to the top component, which is shown to increase current density in the sides.

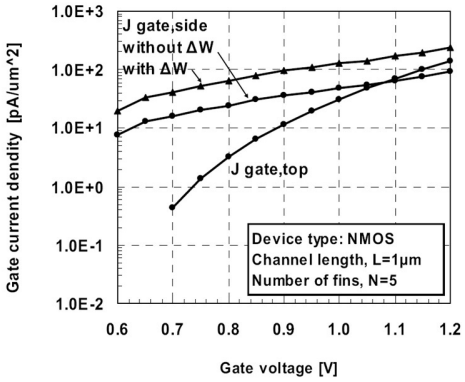

Fig. 20. Dependence of gate current densities $J_{gate,\,top}$ and $J_{gate,\,side}$ on gate voltage. The ΔW is the fin width variance in the tested devices. This value was shown to be in the order of 0.2µm. [12]

B. SEM Images

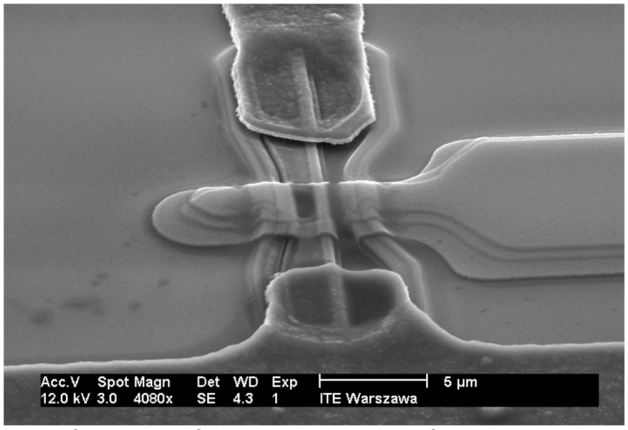

Fig. 21. SEM image of FinFET transistor made for testing purposes. It was fabricated in Institute of Technical Education (ITE) on silicon on insulator (SOI) wafer. Device was etched in HF to disclose the 300nm wide fin. [12]

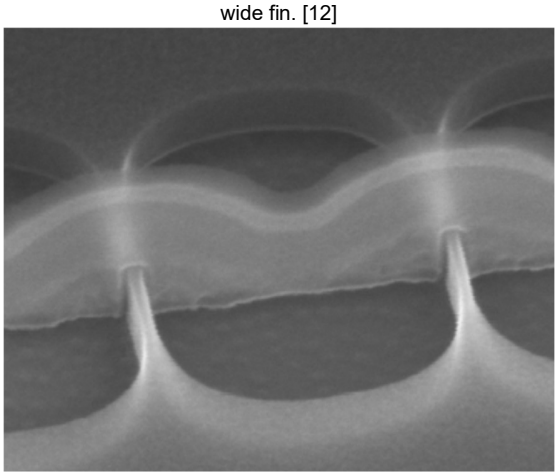

Fig. 22. SEM image of FinFET transistor after gate patterning. $Hf_xSi_{1-x}O$ deposition with Atomic Layer Deposition (ALD) was used to form the gate stacks. Stacks were then capped with 200nm of α-Si. The etching down to 100nm between gates of the Si makes gate etching easier. [17]

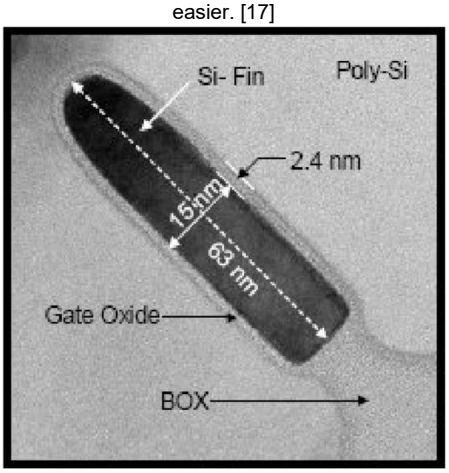

Fig. 23. SEM image of FinFET. [18]

VI. DISCUSSION & CONCLUSION

FinFET devices represent a significant advancement in semiconductor technology, offering several key advantages over traditional planar MOSFETs. These are improved control over leakage currents, enhanced electrostatic integrity, higher drive currents, and better scalability. As a result, FinFETs have become the cornerstone of modern integrated circuit (IC) design, enabling the continued miniaturization and performance improvements demanded by various applications, including mobile devices, data centers, and IoT devices.

Looking to the future, the trajectory of FinFET technology appears promising. Continued research and development efforts aim to further refine the fabrication processes, reduce manufacturing costs, and push the limits of device scaling. Progress in chemical and electronical components of the design and production processes can further improve the capabilities of FinFET devices.

Overall, FinFET technology is a vital component of the semiconductor industry for the foreseeable future.

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REFERENCES

[1] “How the Father of FinFETs Helped Save Moore’s Law,” *IEEE Spectrum*, Apr. 21, 2020. https://spectrum.ieee.org/how-the-father-of-finfets-helped-save-moores-law
[2] “What is a FinFET? – Benefits & How it Works | Synopsys,” *www.synopsys.com*. https://www.synopsys.com/glossary/what-is-a-finfet.html#:~:text=FinFETs%20are%20the%20basis%20for (accessed May 22, 2024).
[3] Bhattacharya, D. and Jha, N.K. (2014a) ‘FinFETs: From devices to architectures’, *Advances in Electronics*, 2014, pp. 3–3. doi:10.1155/2014/365689.
[4] GeeksforGeeks (2024) *FinFET*, *GeeksforGeeks*. Available at: https://www.geeksforgeeks.org/finfet/ (Accessed: 20 May 2024).
[5] Meng-Chou Chang, Kai-Lun He and Yu-Chieh Wang (2014) ‘Design of asymmetric TCAM (ternary content-addressable memory) cells using finfet’, *2014 IEEE 3rd Global Conference on Consumer Electronics (GCCE)*, pp. 359–359. doi:10.1109/gcce.2014.7031172.
[6] Deshmukh, R. *et al.* (2015) ‘Compairing FinFETs: Soi vs bulk: Process variability, process cost, and device performance’, *2015 International Conference on Computer, Communication and Control (IC4)* [Preprint]. doi:10.1109/ic4.2015.7375645.
[7] “FinFET Fabrication Process - Siliconvlsi,” *siliconvlsi.com*, Jan. 07, 2023. https://siliconvlsi.com/finfet-fabrication-process/ (accessed May 22, 2024)
[8] S. Banna, "Scaling challenges of FinFET technology at advanced nodes and its impact on SoC design (Invited)," *2015 IEEE Custom Integrated Circuits Conference (CICC)*, San Jose, CA, USA, 2015, pp. 1-8, doi: 10.1109/CICC.2015.7338378
[9] Alam, S.U. *et al.* (2022) ‘Mathematical modeling and performance evaluation of 3D ferroelectric negative capacitance FinFET’, *Modelling and Simulation in Engineering*, 2022, pp. 1–9. doi:10.1155/2022/8345513.
[10] U. F. Ahmed, "Mathematical Modeling Techniques for nm-FinFETs DC Characteristics," Ph.D. dissertation, Capital University, 2019.
[11] N. Patel and B. Soni, "A Research Paper On The Electrical And Physical Characteristics Of FinFET Using LTspice," 2023 IEEE 11th Region 10 Humanitarian Technology Conference (R10-HTC), Rajkot, India, 2023, pp. 207-212, doi: 10.1109/R10-HTC57504.2023.10461900.
[12] A. Malinowski et al., "Electrical characterization of FinFETS," 2008 15th International Conference on Mixed Design of Integrated Circuits and Systems, Poznan, Poland, 2008, pp. 65-69.
[13] Lee J-H, Park T-S, Yoon E, Park JJ (2003) Simulation study of a new body-tied FinFETs (Omega MSOFETs) using bulk Si wafers. In: Proceedings of Si nanoelectronics technical digest, pp 102–103.
[14] Choi Y-K, Lindert N, Xuan P, Tang S, Ha D, Anderson E, King T-J, Bokor J, Hu C (2001) Sub-20 nm CMOS FinFET technologies. In: IEDM technical digest, pp 421– 424.
[15] MOSFETs”, IEEE Trans. on Electron Devices letters, vol.25, no.2, Feb.2004.
[16] M. Zakir Hossain, Md.Alamgir Hossain et al., Electrical Characteristics Of Trigate Finfet, Global Journal of researches in engineering Electrical and Electronics engineering, Volume 11 Issue 7 Version 1.0 December 2011.
[17] M. J. Van Dal et al., “Material Aspects and Challenges for SOI FinFET Integration,”ECS Transactions, vol. 13, no. 1. The Electrochemical Society, pp. 223-234, Oct. 24, 2008. doi: 10.1149/1.2911503.
[18] http://toronto.ieee.org/r6/scv/eds/slides/20060221-Ivan-Pollentier-IMEC.pdf