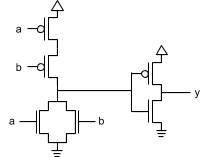
1) The circuit below implements which of the following?



a. NOT

b. CMOS

c. AND

d. OR

2) (a + a’) b = (1)b = b uses which two Boolean algebra properties?

a. Associative, Commutative

b. Complement (OR), Identity (AND)

c. Commutative, Identity (AND)

d. Complement (AND), Identity (OR)

3) Which of the following is a minterm for a function of variables d, g, and o?

a. g’o

b. dog’

c. g

d. do’(g + g’)

4) Which of the following is a sum-of-minterm representation of a(b + c')?

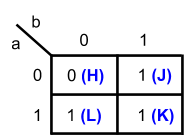
a. ab + ac’

b. abc + abc’ + ab’c’

c. abc + abc’ + ab’c’ + a’bc’

d. abc + abc’ + a’bc’

5) Which of the following results in the best simplification? Note: Each circle is denoted by parenthesis. (A, B) indicates that a circle includes cells A and B.



a. (J), (K), (L)

b. (J, K), (L)

c. (J), (K, L)

d. (J, K), (K, L)

6) Apply DeMorgan's Law to simplify y = (a + bc)'.

a. a'b'c'

b. a'b' + a'c'

c. a' + b' + c'

d. a' + b'c'

7) A two-input XNOR gate is equivalent to which equation?

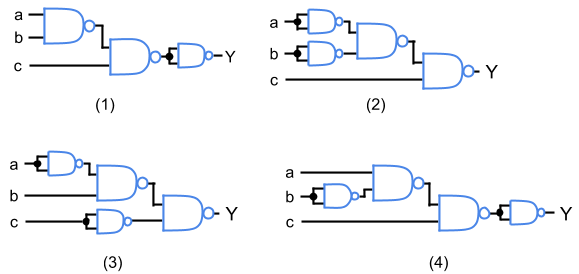
a. y = ab’

b. y = ab’ + a’b

c. y = a(b’ + b)

d. y = a’b’ + ab

8) This equation Y = (a' + b)c is implemented by which circuit?



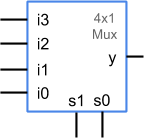
a. 1

b. 2

c. 3

d. 4

9) A 4x1mux is captured by which equation?



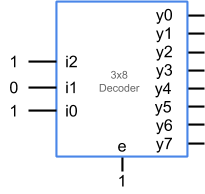
a. y = s0’i0 + s0i1 + s1'i2 + s1'i3

b. y = s1's0’i0 + s1's0i1 + s1s0'i2 + s1s0i3

c. y = (s1 + s0)(i3i2i1i0)

d. y = i3 + i2 + i1 + i0

10) What does the following circuit output?



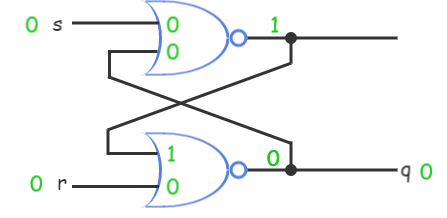
a. 00000000

b. 00001000

c. 10100000

d. 111110111

11) For the given SR-latch, if S is set to 1 and R remains 0, q will \_\_\_.



a. oscillate

b. become 0

c. become 1

d. become 10

12) If e = 1 for a D latch, what is the value of the output q?

a. The previously-stored bit

b. 0

c. 1

d. q = d

13) A 2-bit register has data inputs d1, d0, clock input clk, and outputs q1, q0. Data inputs d1d0 is 01 and output q1q0 is 00. What does q1q0 become after the clk rises?

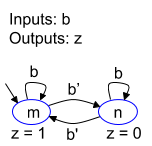
a. 00

b. 01

c. 10

d. 11

14) The given FSM has input b, output z, and starts in state m. What is the FSM's resulting output and state if on the clock’s rising edge b is 0?



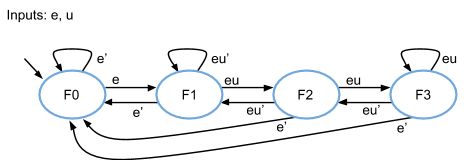
a. z = 0, state = m

b. z = 1, state = m

c. z = 0, state = n

d. z = 1, state = n

15) State F3 transitions to state \_\_\_\_\_ when enable (e) is 0.



a. F0

b. F1

c. F2

d. F3

16) How many bits does the state register of an FSM with 7 states require?

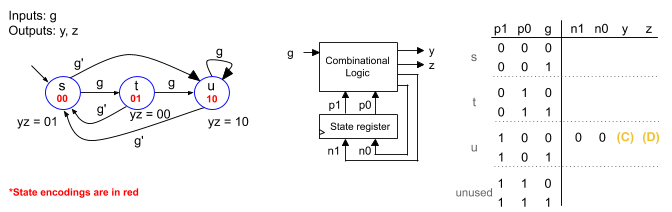
a. 1

b. 2

c. 3

d. 4

17) Table entries (C) and (D) correspond to what values?



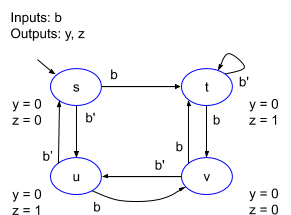
a. C = 0, D = 0

b. C = 0, D = 1

c. C = 1, D = 0

d. C = 1, D = 1

18) Which states are equivalent?



a. s, v

b. u, v

c. t, v

d. t, u

19) An FSM's initial state s is encoded as 000, so the FSM's circuitry sets the state register's clear input to 1 for a few microseconds upon startup. Which is a typical method?

a. The initial state should have the action "clear = 1".

b. The initial state should have the action "clear = 0".

c. The initial state should have a transition back to itself.

d. Special circuitry sets the register's clear signal to 1 upon startup.

20) What is the clock frequency given a critical path of 10 ns?

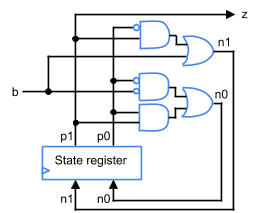
a. 1 MHz

b. 10 MHz

c. 100 MHz

d. 1000 MHz

21) What is the equation for n0?



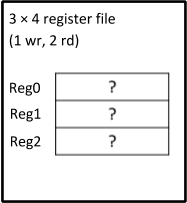
a. p1'p0' + p1p0

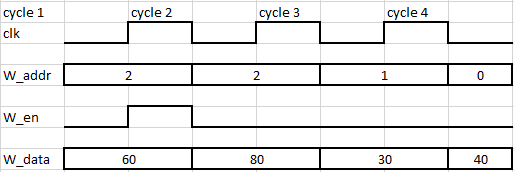
b. p1p0' + p0’b’ + p1p0

c. p0b + p1p0

d. p0’b’ + p1p0

22) Consider a 3 × 4 register file. What is the value of Reg 2 at cycle 2 and at cycle 3?





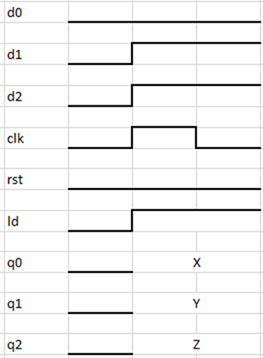
a. 60 and 80

b. 60 and 60

c. 40 and 30

d. 40 and 80

23) For the given timing diagram of a 3-bit load register, what is the value of q0q1q2 when a rising clock occurs?



a. X = 0, Y = 1, and Z = 1

b. X = 1, Y = 0, and Z = 0

c. X = 0, Y = 0, and Z = 0

d. X = 1, Y = 1, and Z = 1

24) What is the function of a 2-bit multi-function register when ld = 1, clr = 1, inv = 1, s1 = 0, and s0 = 0?

|  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- |
| ld | clr | inv | s1 | s0 | Register function |
| 0 | 0 | 0 | 0 | 0 | Maintain |
| 0 | 0 | 1 | (F) |  | Invert bits |
| 0 | 1 | 0 | (G) |  | Clear |
| 0 | 1 | 1 | 0 | 0 | (Maintain) |
| 1 | 0 | 0 | (H) |  | Load |
| 1 | 0 | 1 | 0 | 0 | (Maintain) |
| 1 | 1 | 0 | 0 | 0 | (Maintain) |
| 1 | 1 | 1 | 0 | 0 | (Maintain) |

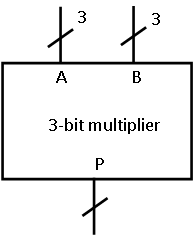
a. Load bits

b. Invert bits

c. Maintain bits

d. Clear bits

25) Determine the number of transistors used to compute all partial products for the given 3-bit multiplier if a2a1a0 = 101 and b2b1b0 = 011.



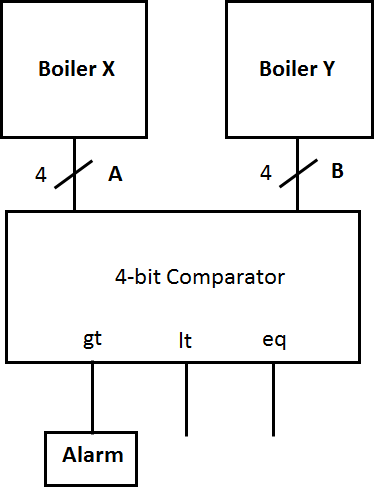
a. 36 transistors

b. 3 transistors

c. 9 transistors

d. 63 transistors

26) A 4-bit comparator’s inputs A and B are connected to two boilers X and Y through an analog-to-digital converter device. This device converts analog temperatures to binary bits. The comparator compares the temperatures and raises an alarm if the temperature of X is greater than that of Y. Identify the combination of inputs from the truth table for which the alarm is triggered.



|  |  |
| --- | --- |
| A | B |
| 0001 | 0100 |
| 0101 | 0100 |
| 1000 | 0010 |
| 0010 | 0110 |
| 0110 | 1001 |

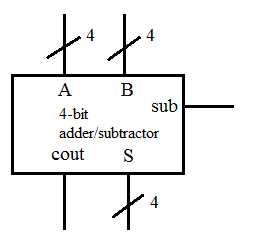
a. A = 0001, B = 0100

b. A = 0101, B = 0100

c. A = 0110, B = 1001

d. A = 0010, B = 0110

27) A 4-bit adder/subtractor has inputs A = 0100, and B = 0010. What value of sub outputs sum S = 0110 and cout = 0000?



a. 0

b. 1

c. 0000

d. 1111

28) What is the sum yielded by a two-digit binary number and the two’s complement of the same number?

a. 1

b. 10

c. 100

d. 1000

29) Identify the ALU operation from the given table if A = 0001, B = 0000, and S = 0010.

|  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- |
| Control inputs |  |  | ALU operation | Mux configuration |  |  |
| v | w | x |  | A | B | cin |
| 0 | 0 | 0 | S = A + B | A | B | 0 |
| 0 | 0 | 1 | S = A – B | A | B’ | 1 |
| 0 | 1 | 0 | S = A + 1 | A | 0 | 1 |
| 0 | 1 | 1 | S = 0 | 0 | 0 | 0 |
| 1 | 0 | 0 | S = A AND B | AB | 0 | 0 |
| 1 | 0 | 1 | S = A OR B | A OR B | 0 | 0 |
| 1 | 1 | 0 | S = A XOR B | A XOR B | 0 | 0 |
| 1 | 1 | 1 | S = NOT A | A’ | 0 | 0 |

a. S = A AND B

b. S = A + 1

c. S = A OR B

d. S = A + B

30) Consider a barrel shifter with eight shift control inputs. How many 1-bit shifters are required to design the mentioned barrel shifter?

a. Eight 1-bit barrel shifters

b. Sixteen 1-bit barrel shifters

c. Sixty-four 1-bit barrel shifters

d. Two hundred fifty-six 1-bit barrel shifters

31) For an 8-bit up-counter, the binary data 00000111 is loaded into the counter’s register. What would happen when the load input of the counter is enabled and cnt is 1?

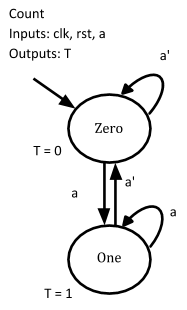
a. The counter starts counting from 00000111

b. The counter starts counting from 00000110

c. The counter starts counting from 00001000

d. The counter starts counting from 00001111

32) What is AAA in the Verilog code snippet that describes the given FSM?



// Count FSM   
AAA  
 // Initial state  
 C\_State = C\_Zero;  
 end  
 else begin  
 // State transitions  
 end  
 …  
 end

a. AAA =

always @ (posedge clk) begin  
 if (rst) begin

b. AAA =

always @ (rst) begin  
 if (posedge clk) begin

c. AAA =

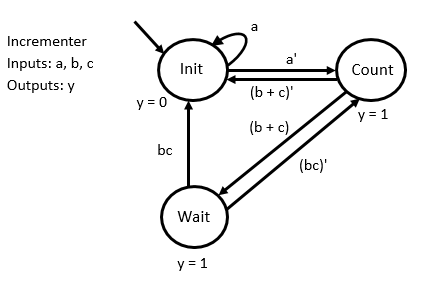
always @ (rst) begin  
 if (C\_State) begin

d. AAA =

always @ (posedge clk) begin  
 if (C\_State) begin

33) Identify XXX in the Verilog code snippet that uses the correct logical operator for the given FSM.

I\_Init: begin  
 XXX  
 I\_State = I\_Count;  
 end  
…  
end



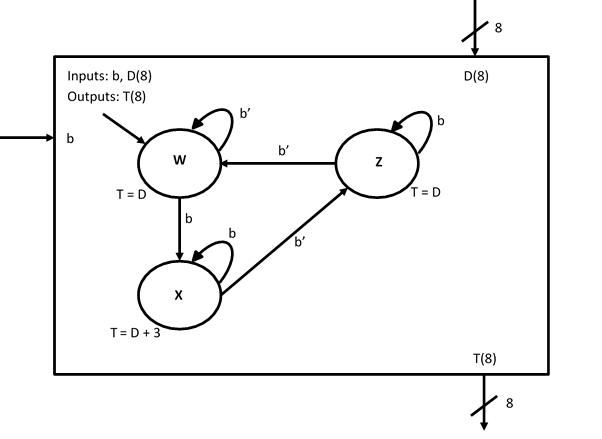
a. if (a') begin

b. if (!a) begin

c. if (~a) begin

d. if (not a) begin

34) In the given extended FSM, the value of D is 00000011 and the present state is W. If b is 1 for the first rising clock cycle and then 0 for the next rising clock cycle, what is the output T?



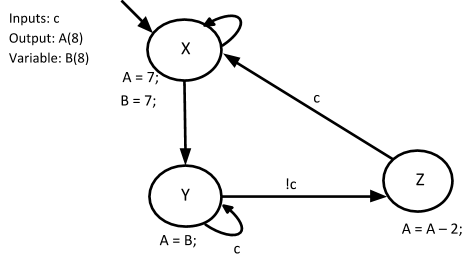
a. 00000000

b. 00000011

c. 00000110

d. 00110011

35) Which of the following statements is true of the given HLSM?



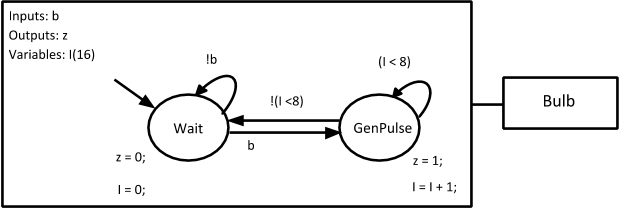
a. If the present state is Y and c is 1, then the next state is Z and A becomes 7 when the clock rises

b. If the present state is Z and c is 0, then the next state is X

c. If the present state is Y and c is 0, then the next state is Z and A becomes 5 when the clock rises

d. If the present state is X and c is 1, then the next state is Z

36) The HLSM describes the loop behavior of a pulse generator. The output z is connected to the bulb and the pulse generated switches on the bulb. For how many clock cycles is z set to 1?



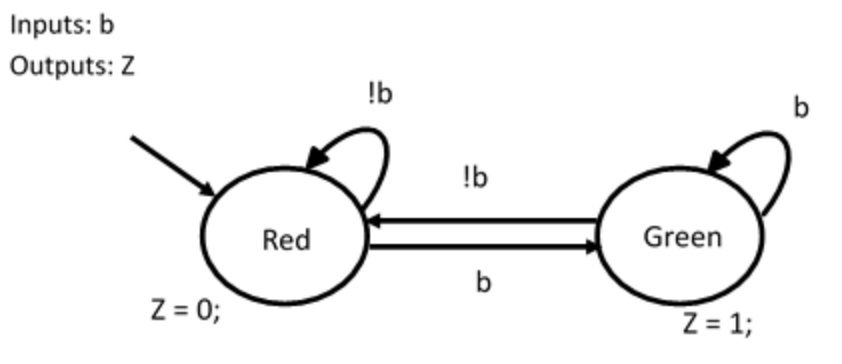
a. 2 clock cycles

b. 4 clock cycle

c. 8 clock cycles

d. 16 clock cycles

37) Consider the given light controller HLSM. Which of the following is true of the given HLSM?



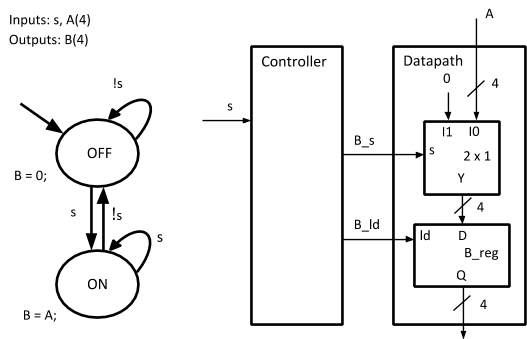
a. When b = 1, the present state is Red

b. When b = 1, Z = 1

c. When b = 0, Z = 1

d. When b = 0, the present state is Green

38) For the given diagram, identify the action in ON state.



a. B\_s = 0 and B\_ld = 1

b. B\_s = 0 and B\_ld = 0

c. B\_s = 1 and B\_ld = 0

d. B\_s = 1 and B\_ld = 1

39) Which of the following statements explains the difference between SRAM and DRAM?

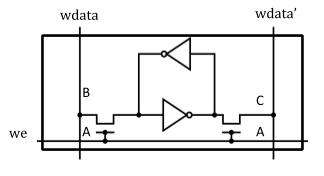
a. SRAM is typically used for on-chip cache, DRAM is typically used for larger off-chip main memory

b. SRAM is slower than DRAM

c. SRAM is typically used for larger off-chip main memory, DRAM is typically used for on-chip cache

d. SRAM is denser and cheaper than a DRAM

40) Which of the following statements holds true for the given SRAM cell?



a. If we = 1 and wdata = 1, then 1 is written to the left side of the inverter loop. Thus, wdata’ = 0

b. If we = 0 and wdata = 1, then 0 is written to the left side of the inverter loop. Thus, wdata’ = 1

c. If wdata’ = 1 and we = 1, then the output of the inverter loop on the other side is 1

d. If wdata’ = 1 and we = 0, then the output of the inverter loop on the other side is 1

41) A user buys a ROM in an unprogrammed state. The user then programs the ROM by blowing the fuse. Identify the type of ROM described here.

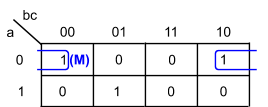
a. EPROM

b. OTP ROM

c. EEPROM

d. Mask-programmed ROM

42) Circle (M) corresponds to what simplified term?



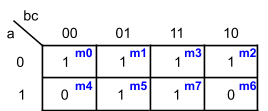
a. a’b’c’

b. a’bc’

c. a’c’

d. a’b’

43) Which of the following results in the best simplification? Note: Each circle is denoted by parenthesis. (A, B) indicates that a circle includes cells A and B.



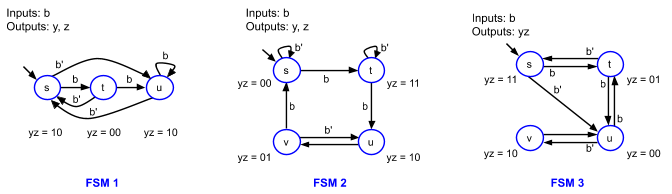
a. (m0, m1), (m3, m2), (m5, m7)

b. (m0, m2), (m1, m3, m5, m7)

c. (m0, m1, m3, m2), (m5, m7)

d. (m0, m1, m3, m2), (m1, m3, m5, m7)

44) Which of the FSMs can be encoded using output encoding?



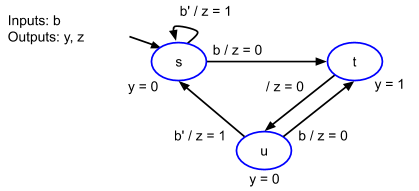
a. FSM 1

b. FSM 1, FSM 2

c. FSM 2, FSM 3

d. FSM 1, FSM 2, FSM 3

45) Before the first rising clock, so in the initial state, what is z?



a. 0

b. 1

c. 01

d. Need b’s present value to determine z’s value.

46) Eight 1 KB memory chips (10 address inputs) named C0, C1, ..., C7 (top to bottom) are composed into an 8 KB memory (13 address inputs). Which of the following sentences is true in this case?

a. For address 1010000000111, chip C7 is activated

b. For address 0110110000000, chip C0 is activated

c. For address 1010000000111, chip C5 is activated

d. For address 0110110000011, chip C2 is activated

47) Which of the following statements is true for yield?

a. Larger chips have higher yield

b. Smaller chips have lower yield

c. Many smaller chips are preferred over having fewer larger chips

d. Fewer large chips are preferred over having many smaller chips

48) Which of the following statements is true of Verilog?

a. Verilog is an HDL that originated in 1985 at a company called Gateway Design Automation

b. Verilog is an HDL that was first published in 1987 as an IEEE standard

c. Verilog was developed at the behest of the U.S. Dept. of Defense

d. Verilog's syntax is borrowed largely from Ada, an earlier DoD language for software programming

49) Identify the example that represents the accurate conversion of a Boolean expression to Verilog.

a. x = a'bc' is converted to x = a & b & c

b. x = a + b + c’ is converted to x = a | b | c

c. x = (pq) (rs) + a is converted to x = (p & q) (r & s) + a

d. x = (pq) + (rs) + a’ is converted to x = (p & q) | (r & s) | ~a

50) Which of the following statements is not true of identifiers?

a. An identifier is a designer-defined name used for items such as modules, inputs, and outputs

b. Identifiers are case sensitive

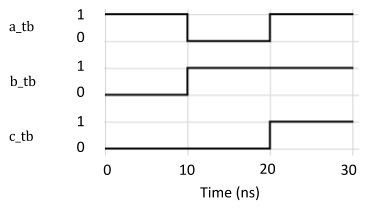
c. An identifier must start with a letter or underscore, followed by any number of letters

d. Identifiers are case insensitive

51) The given testbench code generates the timing waveform shown in the figure. Identify the correct snippet that must be placed instead of ZZZ to obtain the given waveform.

`timescale 1 ns/ 1 ns  
module Lightcontroller (a, b, c);  
 input a, b;   
 output reg c;  
  
  
 always @ (a, b) begin  
 c = a & b;  
 end  
endmodule

module Testbench ();  
 reg a\_tb, b\_tb;  
 wire c\_tb;  
 Lightcontroller Lightcontroller\_tb (a\_tb, b\_tb, c\_tb);  
  
  
 Initial begin  
 a\_tb = 1;  
 b\_tb = 0;  
 ZZZ  
 #10 a\_tb = 1;  
 end  
  
  
endmodule



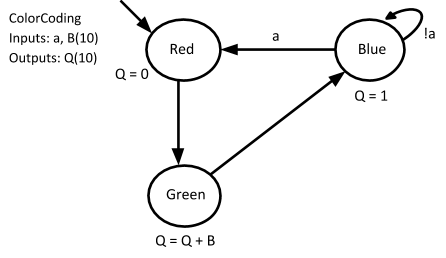
a. #10 a\_tb = 0;  
b\_tb = 1;

b. #20 a\_tb = 1;  
b\_tb = 1;

c. #10 a\_tb = 0;  
#20 a\_tb = 1;

d. #10 a\_tb = 0;  
#10 a\_tb = 1;

52) Identify the Verilog description’s input and output declaration for the given HLSM.



a. module ColorCoding\_HLSM (clk, rst, a, B, Q);   
 input clk, rst;  
 input a;  
 input [9:0] B;  
 output reg [9:0]Q;  
 …  
endmodule

b. module ColorCoding\_HLSM (clk, rst, a, B, Q);   
 input clk, rst;  
 input a;  
 input [0:9] B;  
 output reg [0:9]Q;  
…  
endmodule

c. module ColorCoding\_HLSM (Q, B, a, clk, rst);   
 input [10:0] B, a, clk, rst;  
 output reg [10:0] Q;  
…  
endmodule

d. module ColorCoding\_HLSM (Q, B, a, clk, rst);   
 input [0:10] B, a, clk, rst;  
 output reg [0:10] Q;  
…  
endmodule

53) Which of the following statements is true of testbench?

a. A testbench consists of one main element named a module

b. A testbench provides a sequence of input values to test a module

c. A testbench is a module with inputs and outputs

d. A testbench creates an instance of a module named with the extension “#tb”

54) How many bits are required for a one-hot encoding of an eight-state FSM?

a. 1 bit per FSM input

b. 1 bit per FSM output

c. 3

d. 8

55) Which equation is NOT in sum-of-product form?

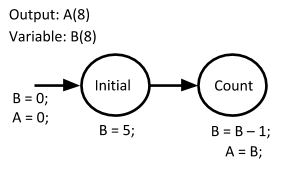
a. a + c

b. ab’c + ac’ + bc

c. (a + b)(b' + c)

d. a

56) For the HLSM, what is the value of variable A when the state “Count” has been entered for the first time?



a. When the value of B is the highest, 1 is added to B on the next clock cycle

b. The value of A is 5 when the state Count has been entered for the first time

c. The value of A is 4 when the state Count has been entered for the first time

d. When the value of A is 0, there is a transition from Count to Initial state

57) An FSM implemented as a circuit experiences a non-ideal delay between \_\_\_\_\_.

a. rising clock edges and the next state's output value changes.

b. controller value and output value changes.

c. rising clock edges and the input.

d. input and controller value changes.

58) A 4-bit carry-ripple adder has inputs A = 1000, B = 1100, and cin = 1. Identify the sum, S, and the carry output, cout, of the adder circuit.

a. S is 0101 and cout is 1.

b. S is 0101 and cout is 0.

c. S is 0100 and cout is 0.

d. S is 0100 and cout is 1.

59) Which statement is INCORRECT?

a. No less than one outgoing transition should have a true condition at any given time.

b. No more than one condition for an outgoing transition should be true.

c. No less than one condition for an outgoing transition should be true.

d. Exactly one outgoing transition should have a true condition at any given time.

60) A light y should illuminate when neither room b is occupied nor room c is occupied. The functionality can be captured as y = (b + c)'. Which of the following is equivalent?

a. The light should illuminate when room b is not occupied or room c is not occupied.

b. The light should illuminate when room b is not occupied and room c is not occupied.

c. The light should illuminate when room b is occupied and room c is occupied.

d. The light should illuminate when room b is occupied or room c is occupied.