ENGG 125.03 Laboratory Activity 3: Decoder

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***Abstract*—The laboratory activity is about decoders and simulating a 3-to-8, specifically a 74xx138 IC, in Quartus. A decoder is a combinational logic circuit that converts coded inputs into coded outputs. It can convert n coded inputs to a maximum of 2^n coded outputs. Although only the 3-to-8 decoder was done in the experiment, there are also other types of decoders such as 2-to-4 and 4-to-16. The decoder was simulated using conditional statements. The inputs, outputs, and enablers were included in the code.**

Keywords - Decoder, Quartus, Verilog

I. Computations/Solutions

A decoder converts coded inputs into coded outputs. Because of this, the different outputs of the inputs will be shown in this part.

Since the 74xx138 3-to-8 decoder uses an enable, the only way that the decoder will work is for these enablers to be on. There are three enabler inputs, namely G2B', G2A', and G1. The only way for the decoder to be on is for the values to be 1, 0, and 0 respectively. If the enablers are not on, then the value of the output will simply be 00000000.

If the enablers are on, these are the values that a 3-bit input will decode to.

000 = 10000000
001 = 01000000
010 = 00100000
011 = 00010000
100 = 00001000
101 = 00000100
110 = 00000010
111 = 00000001

II. HDL Code

This section shows and explains the code made for the activity.

```
module decoder(En, I, O);
    input wire[2:0] En;
    input wire[2:0] I;
    output wire[7:0] O;

    assign O = (En==3'b100) ?
~(8'b0000_0001 << I) : 8'b0000_0000;

endmodule
```

Fig. 1. Code for the 3-to-8 Decoder

A ternary operator was used to simplify the if else statement. The condition for the statement is the value for the enable. If the condition returns true, then a left shift is done on 00000001. The amount of shifting done depends on the input. If the condition returns false, then the value of the output is simply 00000000.

III. Output Circuit

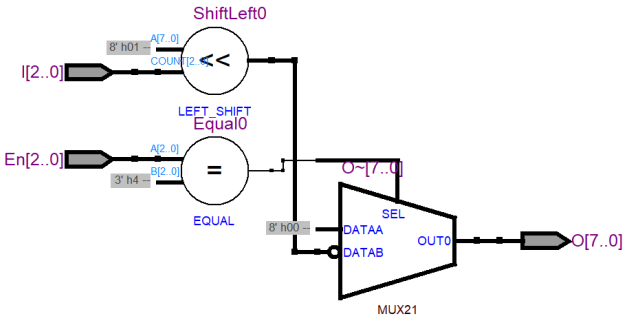

Fig. 2. Circuit for the ALU

A shift left operator is seen in the circuit and is used on the inputs. For the enablers, the equal operator is used. Ultimately, they end up in a multiplexer.

IV. Screenshot(s) of Simulations and VWF file

The screenshots of the simulations are presented below.

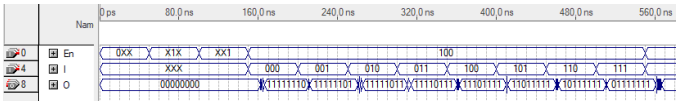

Fig. 3. Simulation for the Decoder

As seen in the screenshot, all the answers in the simulation are the same with the equivalents in the calculations part. However, some glitches can be seen in the simulation. This is because the simulation needs to transition bits. Although there are glitches, they last extremely short so they are almost insignificant.