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Tutorial Sheet1 (Computer Architecture, UEC-510)

1. Differentiate between Von-Neumann Model andHarvard architecture.
   Sol. Done in class
2. Highlight the main differences between CISC and RISC architectures and Draw the data flow for MUL M1, M2.Where M1 and M2 are memory locations(for both the cases).

Sol. These are flow charts of steps for execution

3. A program runs in 10 seconds on computer X with 2 GHz clock. What is the number of CPU cycles on computer X? We want to design computer Y to run same program in 6 second. But computer Y requires 10% more cycles to execute program. What is the clock rate for computer?
   Sol. use CPU time equation here
4. Suppose we have two implementations of the same ISA (instruction set architecture). For a given program
   Machine A has a clock cycle time of 250 ps and a CPI of 2.0
   Machine B has a clock cycle time of 500 ps and a CPI of 1.2
   Which machine is faster for this program, and by how much?
   Sol. use CPU time equation here
5. A compiler designer is trying to decide between two code sequences for a particular machine. Based on the hardware implementation, there are three different classes of instructions: class A, class B, and class C, and they require one, two, and three cycles per instruction, respectively. The first code sequence has 5 instructions: 2 of A, 1 of B, and 2 of C The second sequence has 6 instructions: 4 of A, 1 of B, and 1 of C Compute the CPU cycles for each sequence. Which sequence is faster? What is the CPI for each sequence?

$$\text{CPU clock cycles} = \sum_{i=1}^{n} \text{CPI}_i \times \text{IC}_i$$

Sol:

$$\text{CPI} = \frac{\sum_{i=1}^{n} \text{CPI}_i \times \text{IC}_i}{\text{Instruction count}} = \sum_{i=1}^{n} \text{CPI}_i \times \left(\frac{\text{IC}_i}{\text{Instruction count}} \right)$$