UEC 510: COMPUTER ARCHITECURE

L	T	P	Cr
3	1	0	3.5

Course Objectives: To introduce the concept of parallelism followed in the modern RISC based computers by introducing the basic RISC based DLX architecture. To make the students understand and implement various performance enhancement methods like memory optimization, Multiprocessor configurations, Pipelining and interfacing of I/O structures using interrupts and to enhance the student's ability to evaluate performance of these machines by using evaluation methods like CPU time Equation, MIPS rating and Amdahl's law.

Fundamentals of Computer Design: Historical Perspective, Computer Types, Von-Neuman Architecture, Harvard Architecture Functional Units, Basic Operational Concepts, Bus Structures, Performance metrics, CISC and RISC architectures, Control Unit, Hardwired and micro-programmed Control unit.

Instruction Set Principles: Classification of Instruction set architectures, Memory Addressing, Operations in the instruction set, Type and Size of operands, Encoding an Instruction set, Program Execution, Role of registers, Evaluation stacks and data buffers, The role of compilers, The DLX Architecture, Addressing modes of DLX architecture, Instruction format, DLX operations, Effectiveness of DLX.

Pipelining and Parallelism: Idea of pipelining, The basic pipeline for DLX, Pipeline Hazards, Data hazards, Control Hazards, Design issues of Pipeline Implementation, Multicycle operations, The MIPS pipeline, Instruction level parallelism, Pipeline Scheduling and Loop Unrolling, Data, Branch Prediction, Name and Control Dependences, Overcoming data hazards with dynamic scheduling, Superscalar DLX Architecture, The VLIW Approach.

Memory Hierarchy Design: Introduction, Cache memory, Cache Organization, Write Policies, Reducing Cache Misses, Cache Associatively Techniques, Reducing Cache Miss Penalty, Reducing Hit Time, Main Memory Technology, Fast Address Translation, Translation Lookaside buffer Virtual memory, Crosscutting issues in the design of Memory Hierarchies.

Multiprocessors: Characteristics of Multiprocessor Architectures, Centralized Shared Memory Architectures, Distributed Shared Memory Architectures, Synchronization, Models of Memory Consistency.

Input/ Output Organization and Buses: Accessing I/O Devices, Interrupts, Handling Multiple Devices, Controlling device Requests, Exceptions, Direct Memory Access, Bus arbitration policies, Synchronous and Asynchronous buses, Parallel port, Serial port, Standard I/O interfaces, Peripheral Component Interconnect (PCI) bus and its architecture, SCSI Bus, Universal Synchronous Bus (USB) Interface.

Course Learning Outcomes (CLO S): The students will be able to:

1. Understand and analyze a RISC based processor.
2. Understand the concept of parallelism and pipelining.

3. Evaluate the performance of a RISC based machine with an enhancement applied and make a decision about applicability of that respective enhancement as a design engineer.
4. Understand the memory hierarchy design and optimise the same for best results.Understand how input/output devices can be interfaced to a processor in serial or parallel with their priority of access defined.

Text Books:

1. *Hennessy, J. L., Patterson, D. A., Computer Architecture: A Quantitative Approach, Elsevier (2009) 4th ed.*
2. *Hamacher, V., Carl, Vranesic, Z.G. and Zaky, S.G., Computer Organization, McGraw-Hill (2002) 2nd ed.*

Reference Books:

1. *Murdocca, M. J. and Heuring, V.P., Principles of Computer Architecture, Prentice Hall (1999) 3rd ed.*
2. *Stephen, A.S., Halstead, R. H., Computation Structure, MIT Press (1999) 2nd ed.*

Evaluation Scheme:

S.No.	Evaluation Elements	Weightage (%)
1	MST	30
2	EST	45
3	Sessional (May include Assignments/Projects/Tutorials/Quizes/Lab Evaluations)	25