UEC612: DIGITAL SYSTEM DESIGN

L	T	P	Cr
3	1	2	4.5

Course Objectives: To familiarize the student with the analysis, design and evaluation of digital systems of medium complexity that are based on SSI, MSI and Programmable logic devices. Also, to familiarize the students with the issues in the design of iterative networks, timing analysis of synchronous and asynchronous systems.

Binary Codes: Review of special binary codes, Error detection and correction codes.

Combinational Circuits: Q. M. Method, Variable Map Method, Ripple carry adder, BCD adder, High speed adder, Subtractor, Code conversion, Magnitude comparators, Applications of Encoders, Decoders, MUX, DEMUX, Implementations using ROM, PLA, PAL. Standard ICs and their applications.Using combinational modules to design digital systems, Iterative networks.

Sequential Circuits: Various types of latches and flip-flops and their conversions, Universal Shift Registers, Counters – Ring, Johnson, Design of Counters, Timing issues, Setup and hold times, operating frequency limitations, Static Timing Analysis, Standard ICs for their applications, Finite State Machines – Moore and Mealy, Design of Synchronous and Asynchronous sequential circuits, Races and hazards, hazard free design.

Logic Circuits: DTL, TTL, MOS, CMOS logic families their comparison, Detailed study of TTL & CMOS logic families and their characteristics i.e. Fan-in, Fan-out, Unit load, Propagation delay, Power dissipation, Current & voltage parameters, Tristate Logic, Interfacing of TTL & CMOS logic families, reading and analyzing Datasheets, Performance estimation of digital systems.

Familiarity with Standards IEEE 91a-1991 and IEEE 91-1984.

Laboratory Work: *To study standard ICs and their usage, To study latches and Flip-flops, Design of registers and asynchronous/synchronous up/down counters, Variable modulus counters, Design of Finite State Machines, Study of timing waveforms, Usage of IC tester.*

Course Learning Outcomes: The student will be able to:

1. Perform Logic Minimization for single/multiple output function(s).
2. Generate multiple digital solutions to a verbally described problem.
3. Evaluate the performance of a given Digital circuit/system.
4. Draw the timing diagrams for the identified signals in a digital circuit.
5. Assess the performance of a given digital circuit with Mealy and Moore configurations.
6. Perform static timing analysis of the digital circuits/systems.
7. Compare the performance of a given digital circuits/systems with respect to their speed, power consumption, number of ICs, and cost.

Text Books:

1. *Fletcher, W.I., Engineering Approach to Digital Design, Prentice Hall of India (2007) 4th ed.*
2. *Wakerly, J.F., Digital Design Principles and Practices, Prentice Hall of India (2013) 5thed.*

Reference Books:

1. *Givone D. D., Digital Principles and Design, Tata McGraw Hill (2007) 2nd ed.*
2. *Tocci, R.J., Digital Systems: Principles and Applications, Prentice-Hall (2006) 10th ed.*
3. *Mano, M.M. and Clitti M. D., Digital Design, Prentice Hall (2001) 3rd ed.*

Evaluation Scheme:

S.No.	Evaluation Elements	Weightage (%)
1	MST	25
2	EST	35
3	Sessional (May include Assignments/Projects/Tutorials/ Quizes/Lab Evaluations)	40