

Question 1

Instruction	Clock Cycles																	
	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18
LD R1, 0(R2)	IF	ID	EX	M	W													
DADDI R1, R1, #1																		
SD 0(R2), R1																		
DADDI R2, R2, #4																		
DSUB R4, R3, R2																		
BENZ R4, Loop																		

Complete the above timing sequence.

A. Assume no forwarding unit

Instruction	Clock Cycles																	
	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18
LD R1, 0(R2)	IF	ID	EX	M	W													
DADDI R1, R1, #1		IF	ST	ST	ID	EX	M	W										
SD 0(R2), R1					IF	ST	ST	ID	EX	M	W							
DADDI R2, R2, #4								IF	ID	EX	M	W						
DSUB R4, R3, R2									IF	ST	ST	ID	EX	M	W			
BENZ R4, Loop												IF	ST	ST	ID	EX	M	W

B. assume forwarding unit

Instruction	Clock Cycles																	
	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18
LD R1, 0(R2)	IF	ID	EX	M	W													
DADDI R1, R1, #1		IF	ST	ID	EX	M	W											
SD 0(R2), R1				IF	ID	EX	M	W										
DADDI R2, R2, #4					IF	ID	EX	M	W									
DSUB R4, R3, R2						IF	ID	EX	M	W								
BENZ R4, Loop							IF	ID	EX	M	W							

Question 2

Suppose that in 1000 memory references there are 40 misses in the first-level cache and 20 misses in the second-level cache.

Assume the miss penalty from the L2 cache to memory is 200 clock cycles, the hit time of the L2 cache is 10 clock cycles, the hit time of L1 is 1 clock cycle. What is the average memory access time.

AMAT = hit time L1 + Miss rate L1 x miss penalty L1

Miss penalty L1 = hit time L2 + miss rate L2 + miss penalty L2

Hit time L1 = 1

Miss rate L1 = 40/1000

Miss penalty L1 = 10 + (20/40) x 200 = 110 // local miss rate of 20/40 (50%)

AMAT = 1 + .04 x 500 = 5.4

Question 3

Performance Evaluation

You are investigating the possible benefits of a way-predicting level 1 cache. Assume that the 32 KB two-way set-associative single-banked level 1 data cache is currently the cycle time limiter. It takes one cycle to hit this cache.

As an alternate cache organization you are considering a way-predicted cache modeled as a 16 KB direct-mapped cache with 85% prediction accuracy. Unless stated otherwise, assume a mispredicted way access that hits in the cache takes one more cycle.

What is the average memory access time of the current cache versus the way-predicted cache?

Given:

Miss rate for 2 way LRU is 0.0056

Miss rate for Direct-mapped is 0.015

Miss penalty is 20 cycles for both types

Hit time= Hit Rate* Hit Cycles

Current cache:

Average memory access time (AMAT) = hit time + miss rate

Hit time = $(1 - 0.0056) * 1 = 0.9944$

Miss rate = $0.0056 * 20 = 0.112$

AMAT = 1.1064

Way-predicted cache

AMAT = $(1 - \text{miss rate})[\text{Pred \%} \times 1 + (1 - \text{pred \%}) \times 2] + (\text{miss rate} \times \text{miss penalty})$

AMAT = $(1 - 0.015)[.85 \times 1 + (1 - .85) \times 2] + (0.015 \times 20)$

AMAT = 1.43275

The current cache system is better as it has a lower average memory access time than the way-predicted cache. This is mostly due to the much higher miss rate for the direct-mapped cache.