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| Santa Clara University |
| Implementation of AWGN |
| Using the Box-Muller Method |
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| This paper discusses some of the trials and tribulations in building a “hardware” version of an Additive White Gaussian Noise (AWGN) generator. I begin by discussing complications in System Generator and then go into some of the algorithms used in my Matlab simulation. I then show the results of this implementation. Due to an extension of the due date I was also able to write Verilog files that compiled in Modelsim, but could not simulate them in Vivado due to technical difficulties and lack of knowledge of this toolset. |

# Introduction

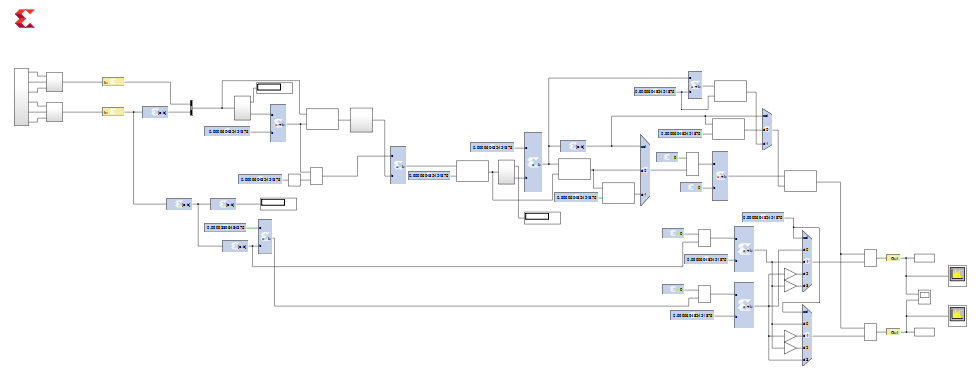
Additive White Gaussian Noise (AWGN) is invaluable to signal processing. Not only can it be used to knock down spurious signals from constructive interference in FPGA signals, but it is at the core of LPC Speech Coding reproduction. With that said, it is necessary to ensure that this noise is as random as possible, so that a “full” reproduction of speech can be obtained and constructive interference can be mitigated. With the computational demand of many random generating algorithms, implementation of these designs can be utilized on chipsets to speed them up. These ideas are outlined in [1] more fully. In our project, we were to implement this design and create the RTL’s for it. Although I was able to get a simulation in Matlab created, due to my limited knowledge of Vivado and lack of time after failing with System Generator, my hardware construction was an impossibility. Hopefully, by seeing what road blocks I was up against and how I overcame most of the obstacles I overcame, it will be noticeable the efforts I put into this endeavor and the knowledge I gained.

# Initial Design Attempt Using System Generator

When I started this project, my natural intuition was to use a program that I knew had a better likelihood of accelerated prototyping from design to hardware implementation. That is why I chose to work with System Generator and the Vivado Suite. System Generator uses a set of modularized blocks much like Simulink, but designed for straight implementation into simulated design and quick synthesis on an FPGA. My approach was to get a full simulation created of the System Generator design and then synthesis would be no more than creating the RTLs for a particular chipset and then synthesizing it to an FPGA board. Although this sounds straight forward, System Generators error messages aren’t exactly great indicators of the problem, and having no more than perhaps 100 hours of practice using System Generator from my ELEN226, FPGA design class, I was by no means an expert. Therefore, after dozens of hours troubleshooting and even going to the extent of a teleconference with the Professor, I decided it was in my best interest to throw in the proverbial towel for this design. The following sections illustrate some of the design and errors that I received.

## System Generator Design

Below you can see the entire implementation of System Generator:



Although this design did not implement all the correct cordics and was by no means free of errors, getting even a more simple simulation performed was a difficult task. Below are a few of the methods I tried to use just for the Tausworthe URNG that ended in failure:

### S-Function Module:

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| --- | --- |
| S-Function | S-Function Error |

### Black Box Module:

|  |  |
| --- | --- |
| Black Box Error – Could not find file (file highlighted on left) | Black Box Error– unable to initialize module |

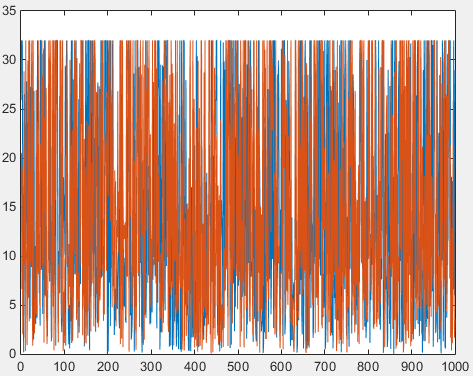
Without being able to create the Tausworthe UNRG or simulate due to an assortment of errors in my model, I decided to stop while I was behind. Therefore, I started to code using Matlab.

# Later Design Attempt Using Matlab

Although I was behind the curve with only a week to go, I felt more natural in the simplistic Matlab coding environment. Even though it was going to take learning more code and longer searches on the internet to get a feel for the fixted point implementation within Matlab, this methodology allowed for a more “divide and conquer” approach by allowing more coder friendly troubleshooting techniques (not all variable needed to be tied off as they did in System Generator). So with that said, all I needed to do was follow a bit stream through all the methods of the paper [1]. Using Figure 6 as a model and Figure 2 to get the necessary bit lengths, I was able to get a working model within roughly 20 hours of coding. The reason it wasn’t quicker, was because I needed to become familiar with the fixed point representation of the code. By using “fi”, I was able to make quick work of Figure 6 with the properly quantized values throughout the process using Figure 2. This was no easy task though; I was required to make sure no bit overflow occurred in the process, and I am not fully convinced I was able to accomplish this. I also used programming techniques rather than all inclusive hardware design implementations. This means that creation of the RTL file would not be possible until these design bugs were fixed. Although the Leading Zero Detector (LZD) hardware design was provided in the paper [1], my implementation of it was not without bugs, and this late in the game, I needed to get something working or I would feel that I accomplished nothing for the amount of time I spent on this. Thus, I just walked through the array looking for the first one and returned the array value.

# Results

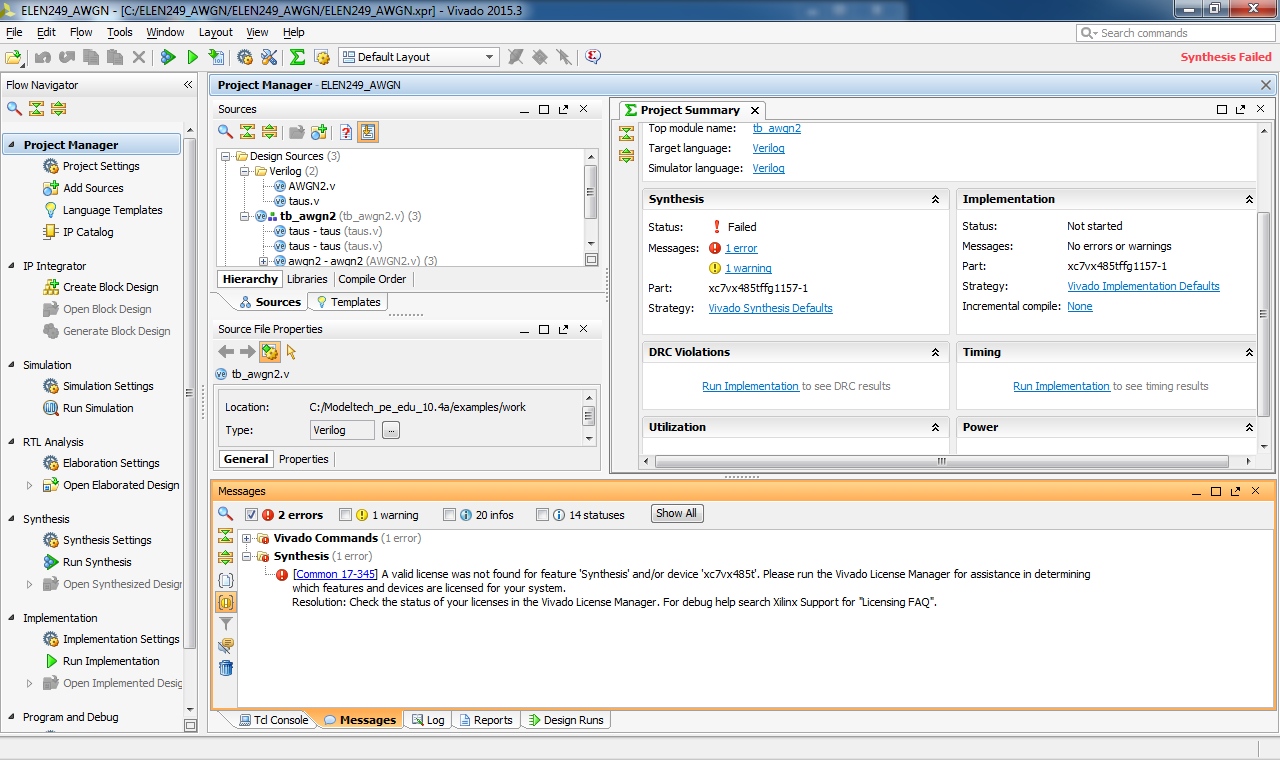
Due to the inability to simulate my System Generator version of this design, I was unable to get any results to see if my design was viable; but, as for my Matlab code, I was able to get results close to Figure 12 of the paper[1].



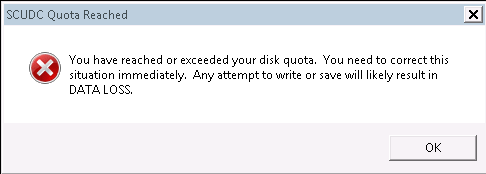
As you can see from the plot. It appears that there is some overflow from the truncation of the tops of these signals. I notice this earlier in the code and was able to alleviate it by using more bits during calculations and then shifting it to fit within the recommended bit length, but with the outputs being set at 16 bits with 11 fractional bits, the prior calculation must have overflowed rather than truncated / rounded. This is another issue I would have worked on given the time.

# Attempt to Create an RTL

Without the hardware to utilize for this project, not that I had the know-how to get it done, I decided pretty late in the project timeframe to try to create RTLs for this design. With only a week left, I started learning the Verilog programming language. I had many hurdles, considering this is not like its conventional programming language counterparts; it contains syntax more like that found in electrical technician vocabulary with its “wire” for intermediate variables that connect one operation or variable to another, “reg” for data that might be held in a register, and “parameter” that holds perhaps constants. There was also a need to “assign” all or most variables that needed to be declared, rather than just using a “=” or “<=”, not that I know the difference between the two, because both seemed to work. There was also a need to synchronize and maintain timing, that I probably lacked the knowledge to do effectively. All-in-all, I was able to compile the files I needed and pull them into Vivado. Unfortunately, with a day left, I had licensing issues that couldn’t be resolved (see below):



And when I went to use the school remote access to try their version of Vivado, my account went to the maximum allowable storage usage:

  
With these defeats and knowing that I wouldn’t be able to affectively get a behavioral model done in the last few hours, I am consciously throwing in the towel. I have learned a lot from this project, perhaps more than any other student in our class, and although I was unable to get a working prototype created, I have had great growth in this area of the industry. I now know the tools that would get me to the place I would like to be for the next time I tackle any hardware FPGA designs. If I had known about these tools when we started this project, perhaps I would have completed, but my hours of watching YouTube videos were ineffective, since I was watching the wrong videos. Now I know that Vivado is the main resource for digital design, while simulations can be carried out using the Modelsim simulation engine. I also realize that there are a myriad of templates within Vivado that could potentially assist a budding engineer with little digital design programming time under his belt. I think that this knowledge that I learned towards the end of this project was invaluable.

# Conclusion

Due to the time constraints and the difficulty of the project, I am quite pleased with the results I achieved despite the inability to implement this design in hardware. I had some major hurdles in this project, not being from this discipline of studies and not having my hands into some research of this type. My over-optimism with thinking that I could simulate and synthesize in the System Generator / Vivado environment left me with little time to regroup, but with only four days to redesign this implementation, I was able to get this code working, cordics and all. Then getting an extension I was able to start programming of Verilog module scripting; unfortunately, I didn’t consult with the professor in time to realize that there was a plethora of intuitive design tool right from within the Vivado toolset. Knowing this gives a budding electrical engineer hope for future implementations of digital designs. If I had to do it all over again, I would definitely start with simple coding and if time permitted, I would go to Simulink / System Generator implementation or directly to Vivado. Although I didn’t get the required RTLs that my PhD candidate peers did, I would say that I achieved a lot for being one of only two Master’s students in this class. I was quite happy with the results, but wish I had more time to follow this through to completion.

# References

1. Dong-U Lee, John D. Willasenor, Wayne Luk, and Philip H. W. Leong, “A Hardware Gaussian Noise Generator Using the Box-Muller Method and Its Error Analysis”, “http://ieeexplore.ieee.org/xpl/login.jsp?reload=true&tp=&arnumber=162895”, IEEE.