Project 2 Report
5/8/2021
By: Krishna Menon and Arman Hoque

Processor 470:

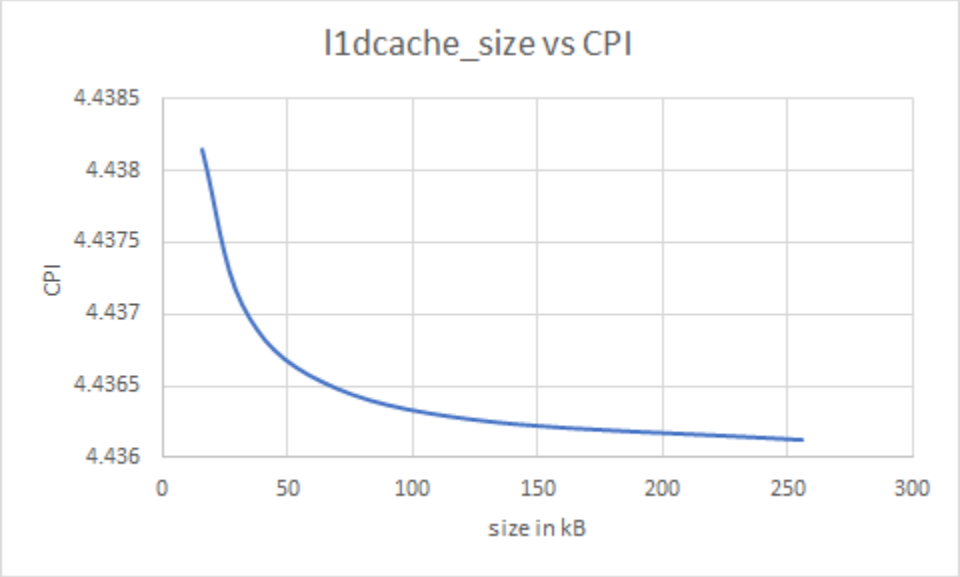

Figure 1.1 : L1D Cache vs CPI

In figure 1.1 we can see that as the L1D cache size increases the CPI decreases requiring less latency.

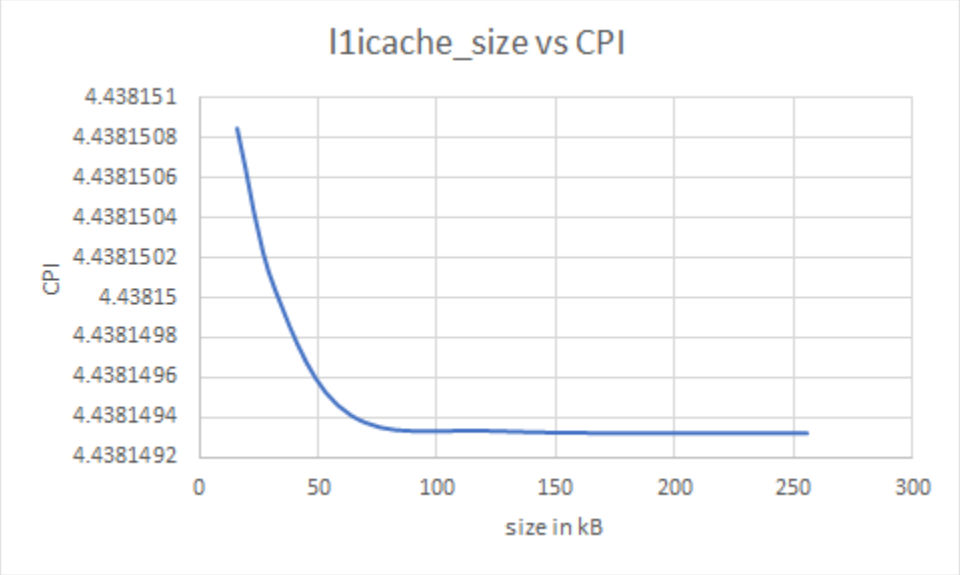

Figure 1.2 : L1I Cache vs CPI

In figure 1.2 we can see that as the L1I cache size increases the CPI decreases requiring less latency.

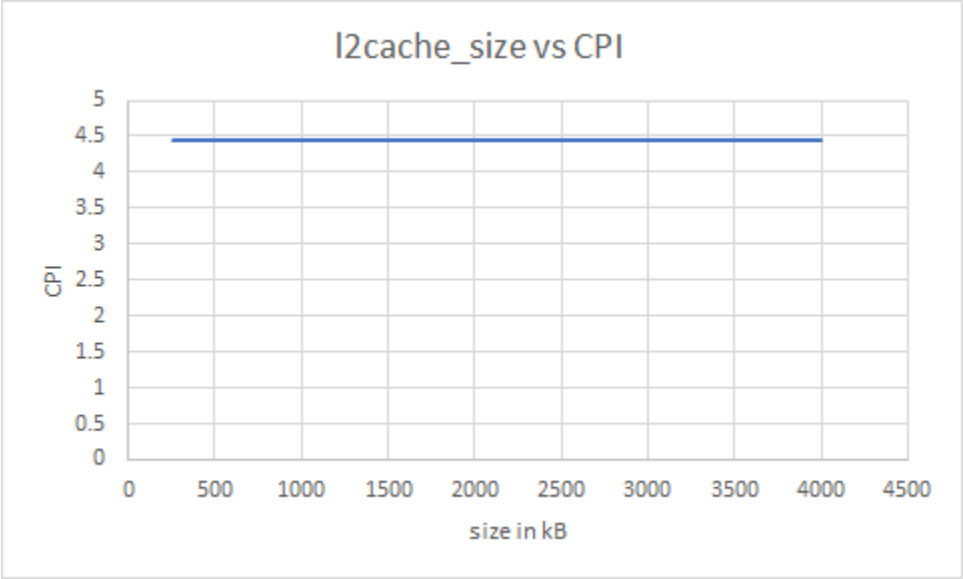

Figure 1.3 : L2 Cache vs CPI

In figure 1.3 we can see that as the L2 cache size increases the CPI remains the same meaning there is no change in the latency whatsoever.

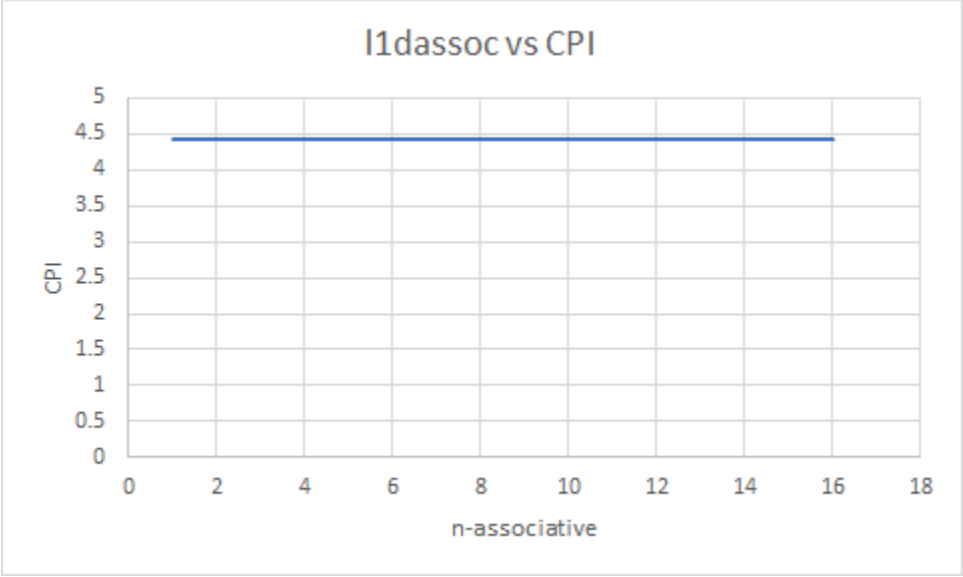

Figure 1.4 : L1D Assoc vs CPI

In figure 1.4 we can see that as the L1D Associative cache size increases the CPI stays the same.

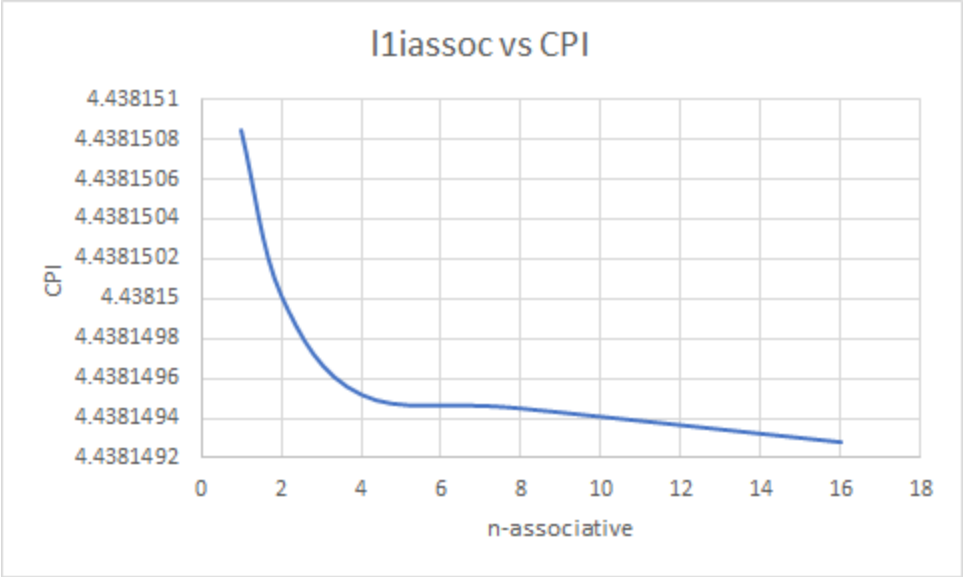

Figure 1.5 : L1I Assoc vs CPI

In figure 1.5 we can see that as the L1I Associative cache size increases the CPI decreases exponentially meaning a significant increase in performance.

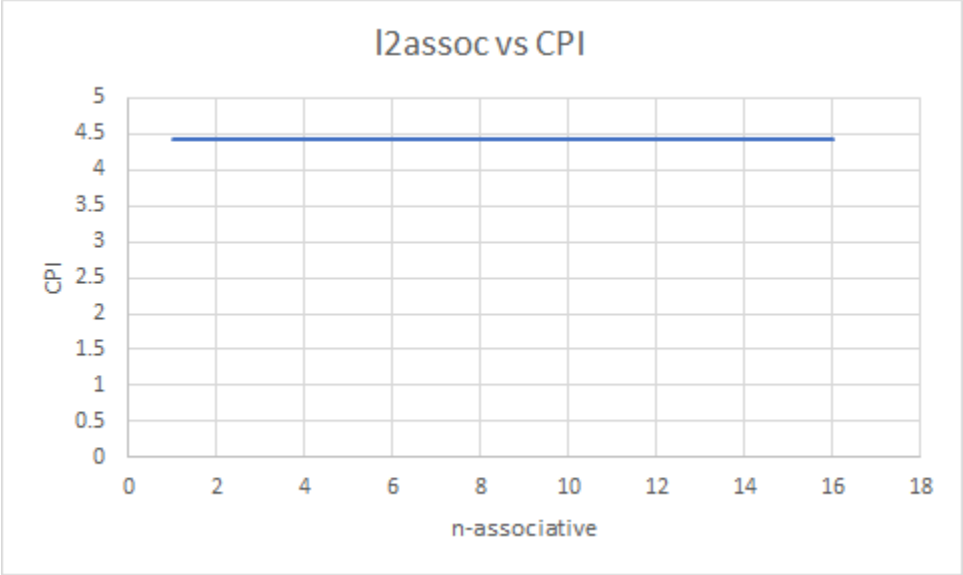

Figure 1.6 : L2 Assoc vs CPI

In figure 1.6 we can see that as the L2 Associative cache size increases the CPI stays the same implying that there is no change in performance.

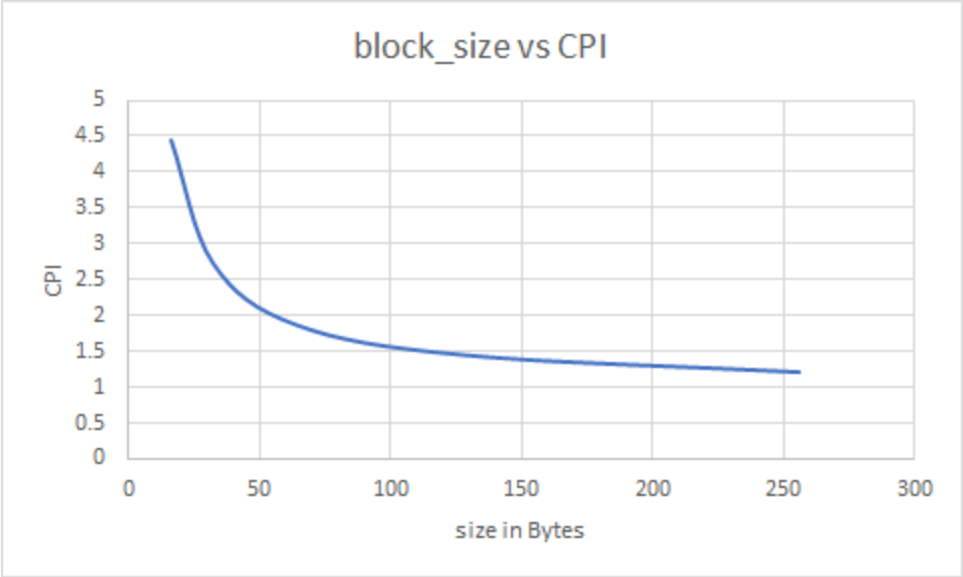

Figure 1.7 : L1D Assoc vs CPI

In figure 1.7 we can see that as the Block size increases the CPI decreases exponentially meaning a significant increase in performance.

Processor 458:

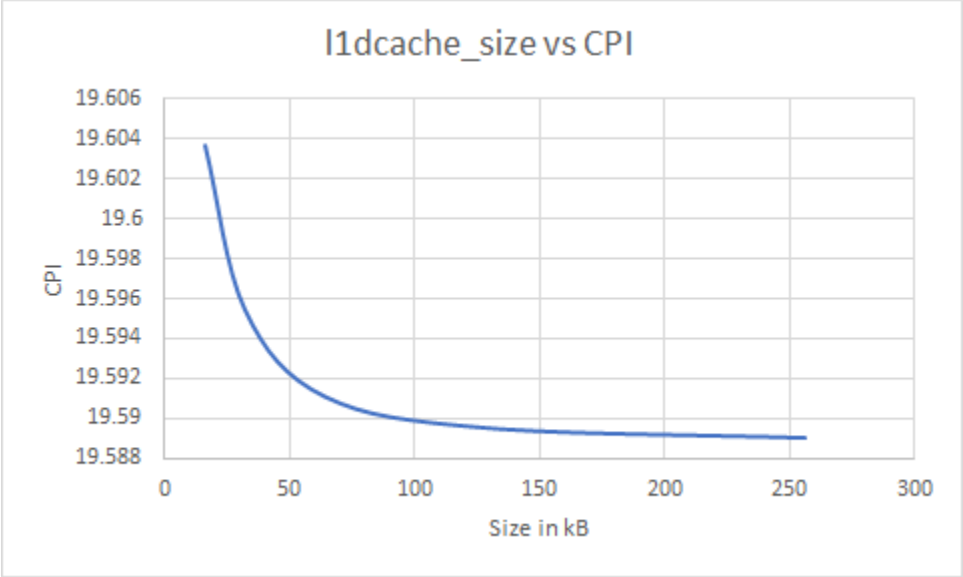

Figure 2.1 : L1D Cache vs CPI

In figure 2.1 we can see that as the L1D cache size increases the CPI decreases requiring less latency.

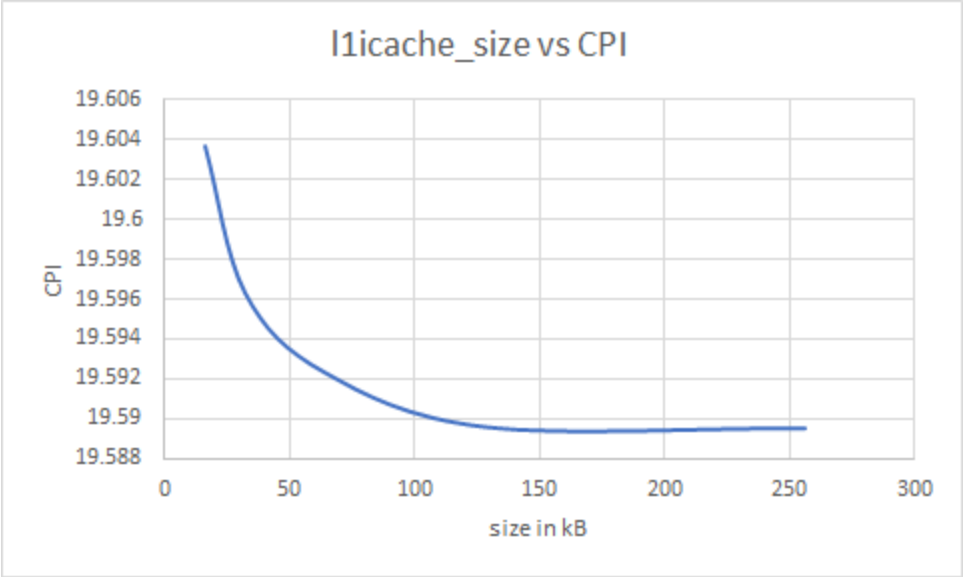

Figure 2.2 : L1I Cache vs CPI

In figure 2.2 we can see that as the L1I cache size increases the CPI decreases significantly requiring less latency.

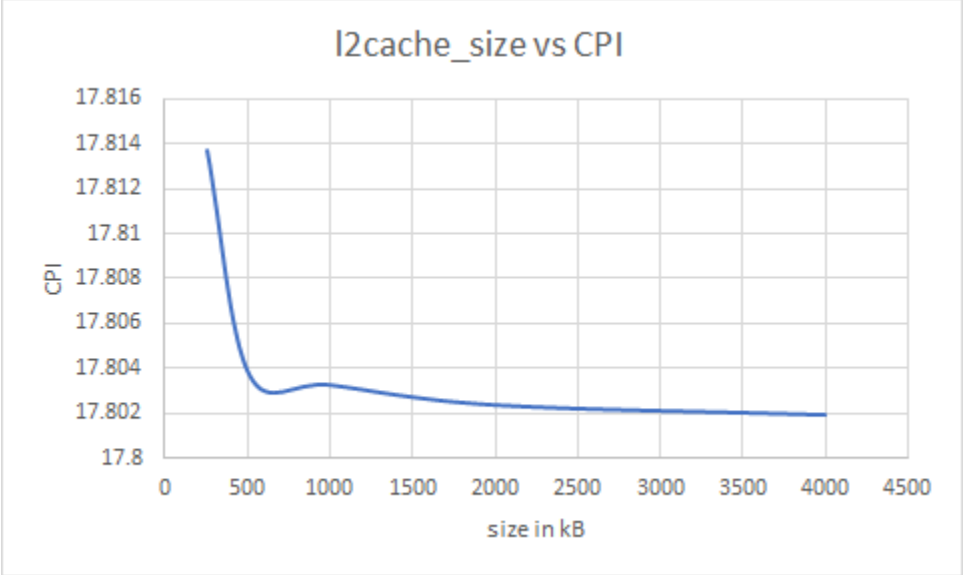

Figure 2.3: L2 Cache vs CPI

In figure 2.3 we can see that as the L2 cache size increases the CPI decreases significantly requiring less latency.

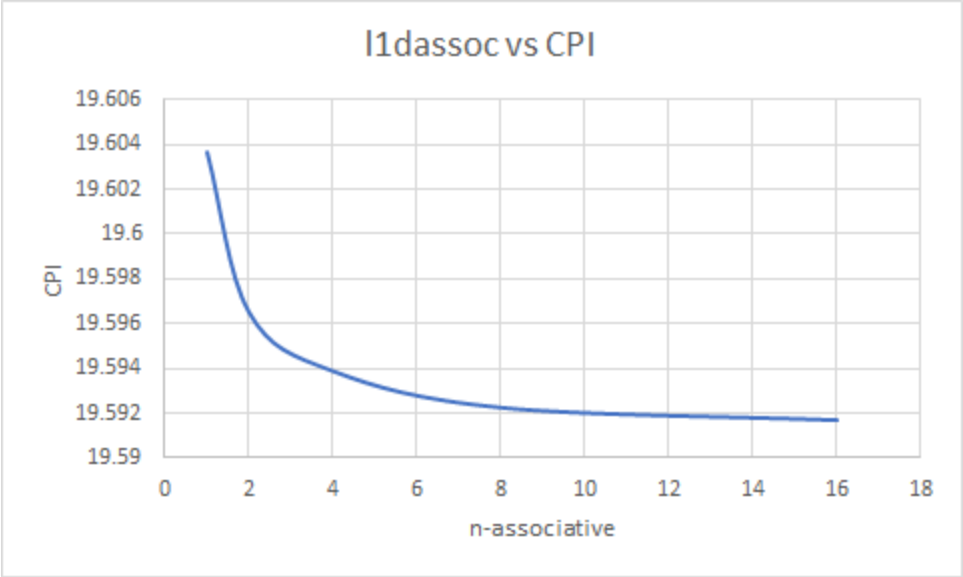

Figure 2.4 : L1D Assoc vs CPI

In figure 2.4 we can see that as the L2 cache size increases the CPI decreases significantly requiring less latency.

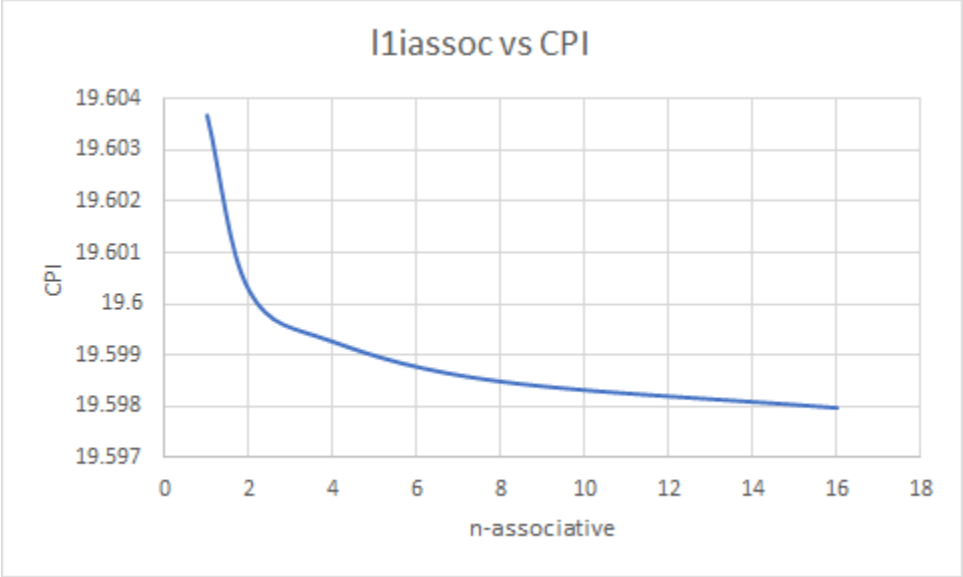

Figure 2.5 : L1I Assoc vs CPI

In figure 2.5 we can see that as the L2 cache size increases the CPI decreases significantly requiring less latency.

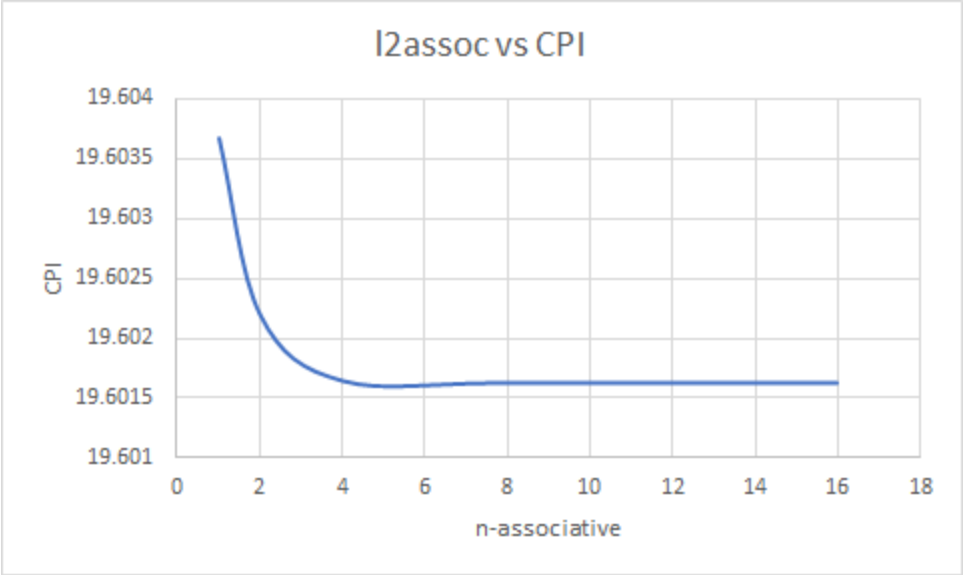

Figure 2.6 : L2 Assoc vs CPI

In figure 2.6 we can see that as the L2 Assoc size increases the CPI decreases significantly requiring less latency.

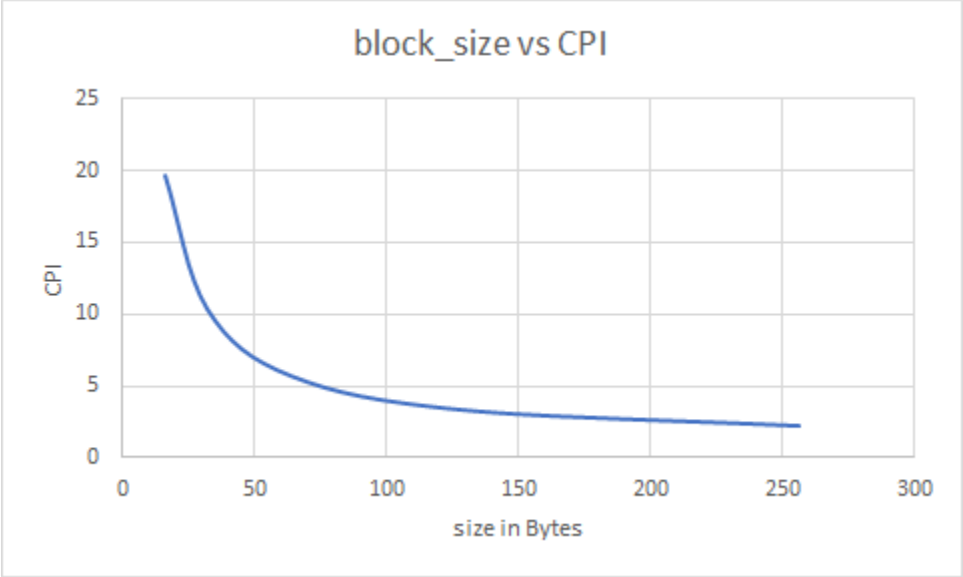

Figure 2.7: Block Size vs CPI

In figure 2.7 we can see that as the Block size increases the CPI decreases significantly requiring less latency.

Processor 429:

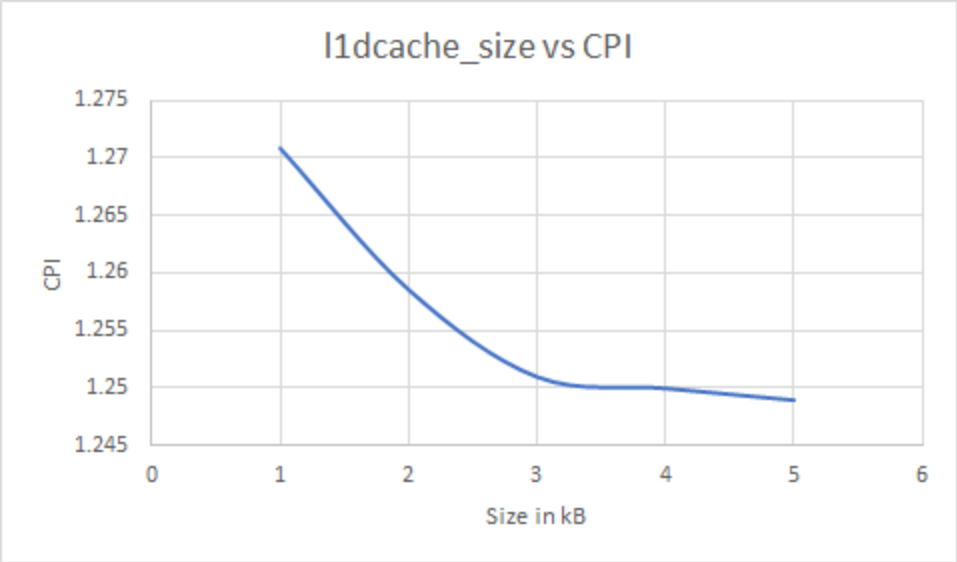

Figure 3.1: LD Cache vs CPI

In figure 3.1 we can see that as the LD Cache size increases the CPI decreases significantly requiring less latency.

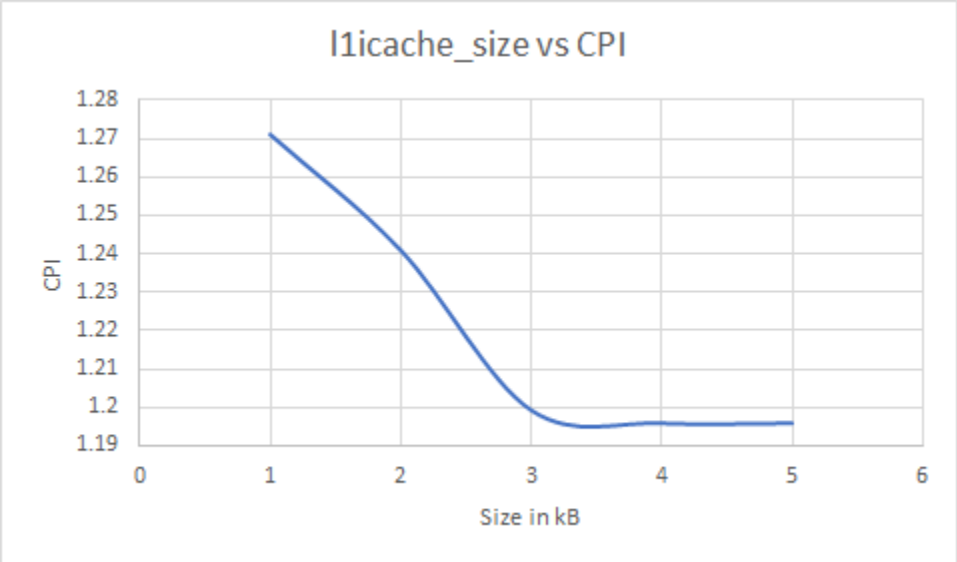

Figure 3.2: LI Cache vs CPI

In figure 3.2 we can see that as the LI Cache size increases the CPI decreases significantly requiring less latency.

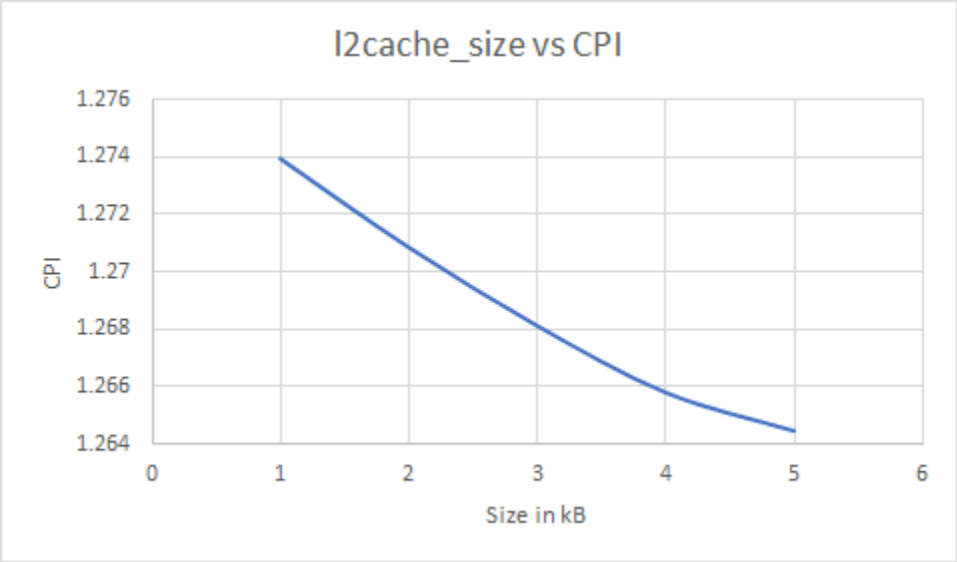

Figure 3.3: L2 Cache vs CPI

In figure 3.3 we can see that as the L2 Cache size increases the CPI decreases significantly requiring less latency.

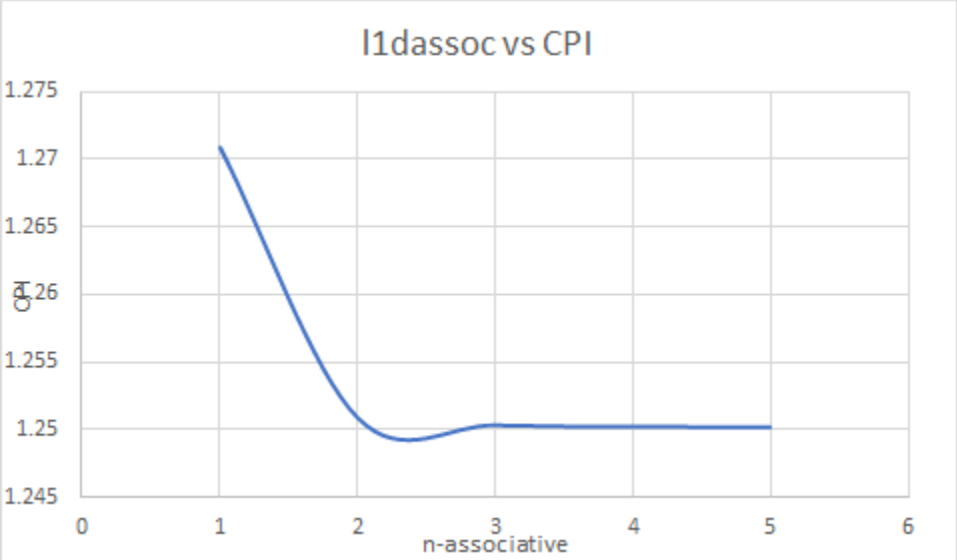

Figure 3.4: LD Assoc vs CPI

In figure 3.4 we can see that as the LD Assoc size increases the CPI decreases significantly requiring less latency.

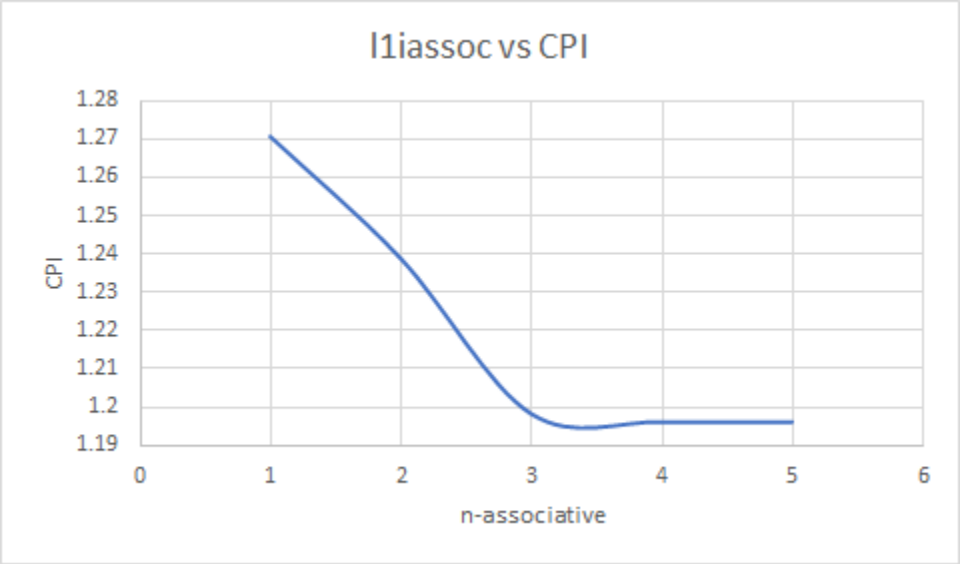

Figure 3.5: LI Assoc vs CPI

In figure 3.5 we can see that as the LI Assoc size increases the CPI decreases significantly requiring less latency.

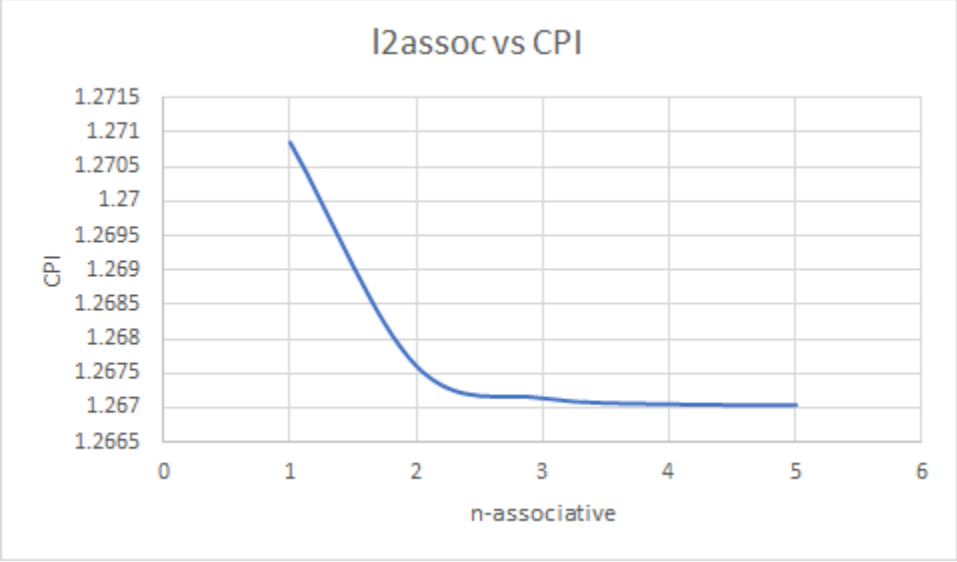

Figure 3.6: L2 Assoc vs CPI

In figure 3.6 we can see that as the L2 Assoc size increases the CPI decreases significantly requiring less latency.

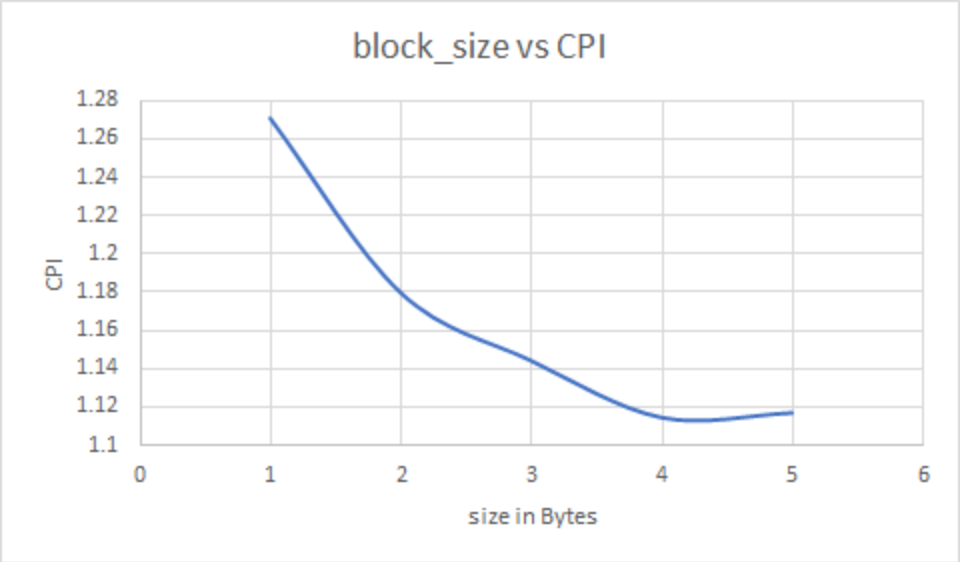

Figure 3.7: Block Size vs CPI

In figure 3.7 we can see that as the Block size increases the CPI decreases significantly requiring less latency.

Processor 401:

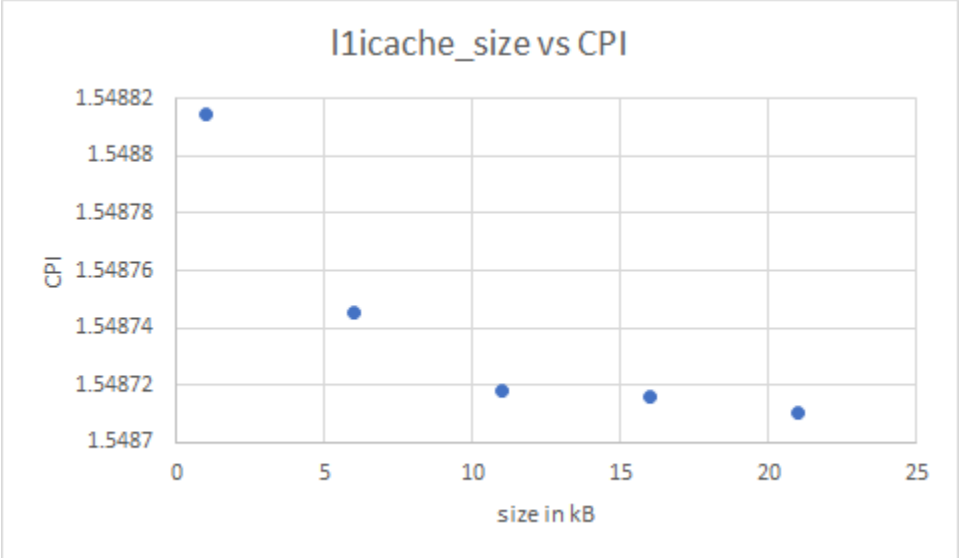

Figure 4.1: LI Cache vs CPI

In figure 4.1 we can see that as the LI Cache size increases the CPI decreases significantly requiring less latency.

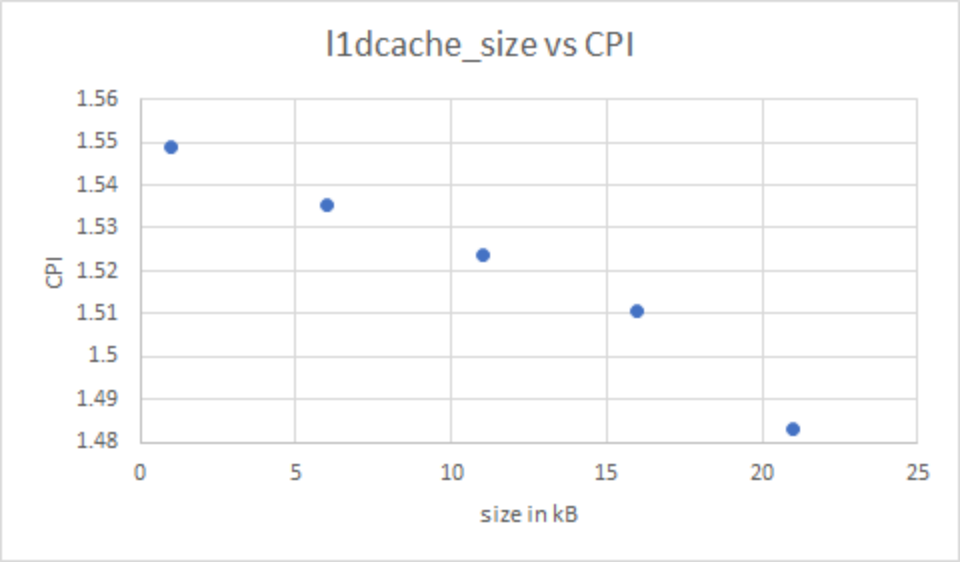

Figure 4.2: LD Cache vs CPI

In figure 4.2 we can see that as the LD Cache size increases the CPI decreases significantly requiring less latency.

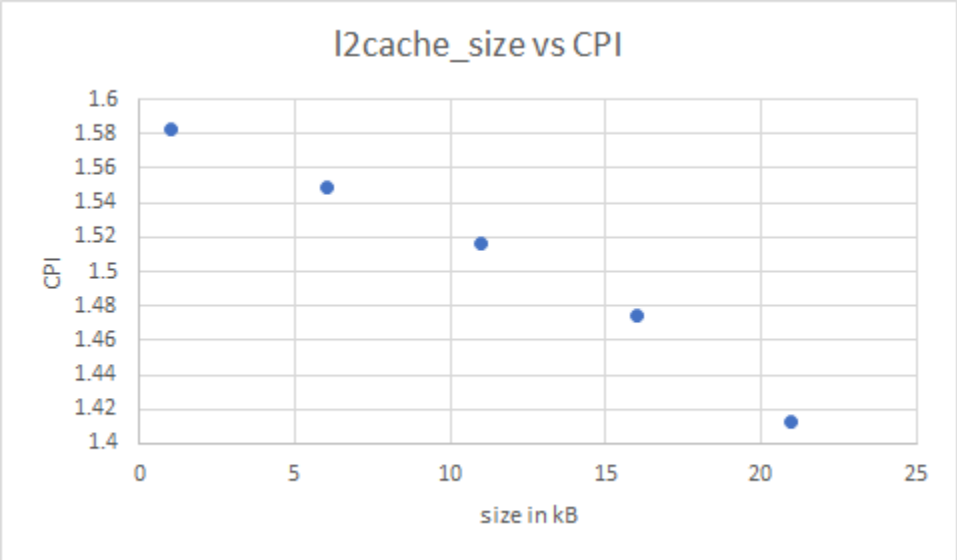

Figure 4.3: L2 Cache vs CPI

In figure 4.3 we can see that as the L2 Cache size increases the CPI decreases significantly requiring less latency.

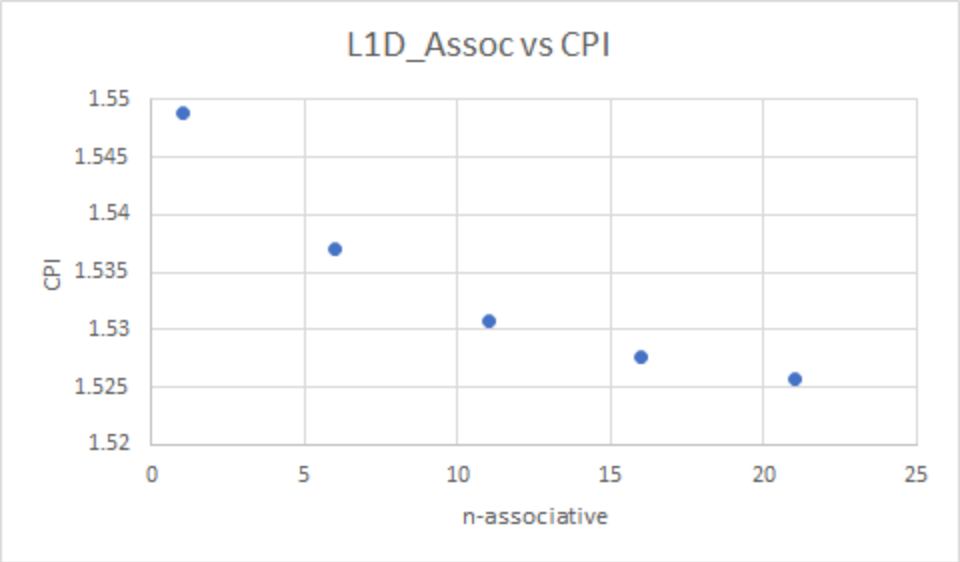

Figure 4.4: LD Assoc vs CPI

In figure 4.4 we can see that as the LD Assoc size increases the CPI decreases requiring less latency.

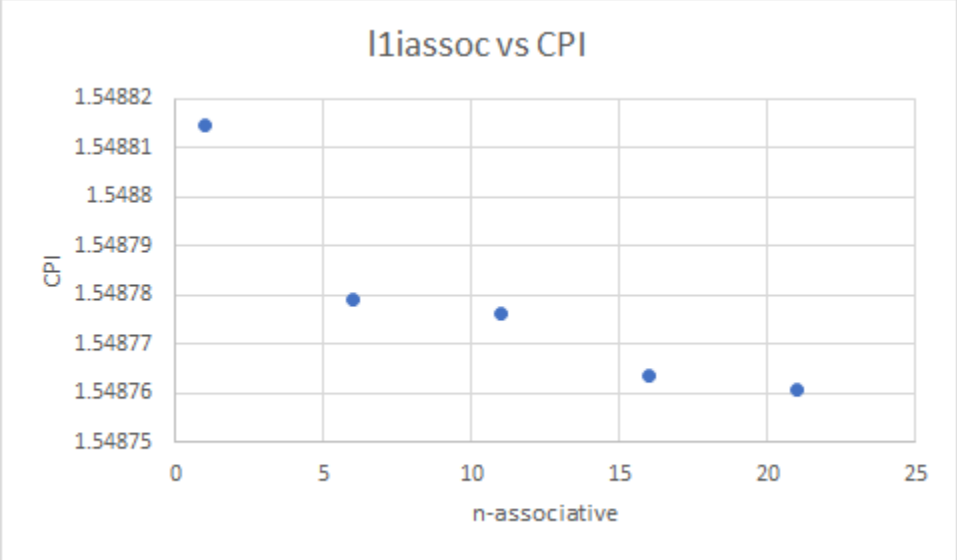

Figure 4.5: LI Assoc vs CPI

In figure 4.5 we can see that as the LI Assoc size increases the CPI decreases requiring less latency.

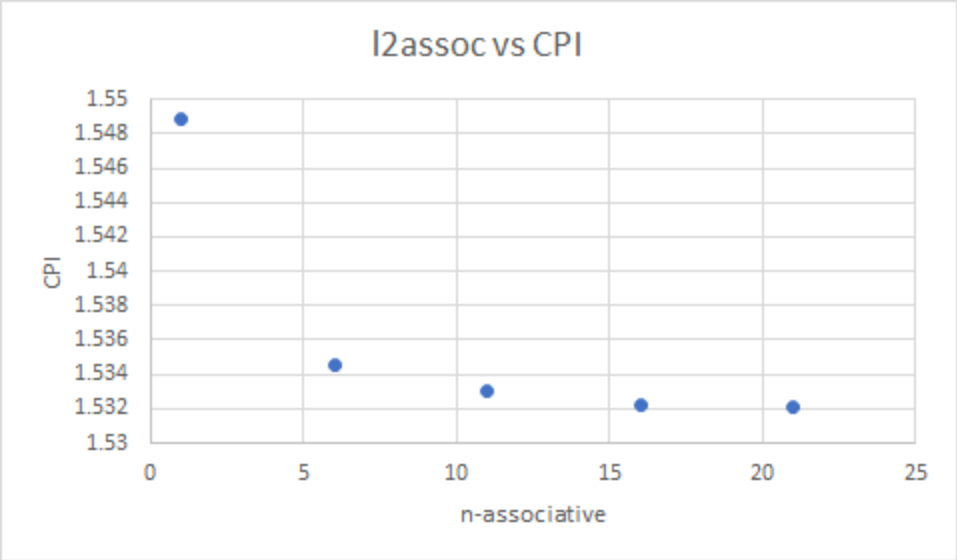

Figure 4.6: L2 Assoc vs CPI

In figure 4.6 we can see that as the L2 Assoc size increases the CPI decreases dramatically requiring less latency.

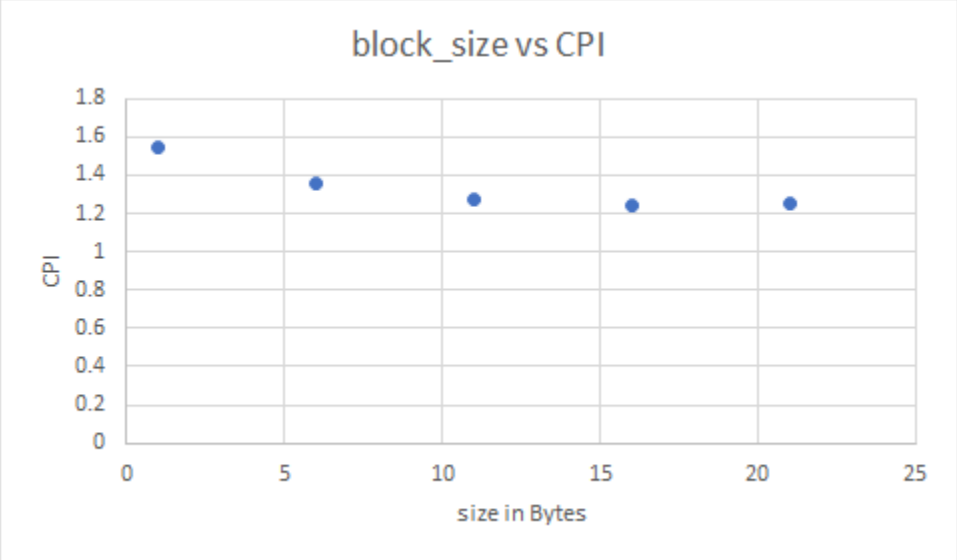

Figure 4.7: Block Size vs CPI

In figure 4.7 we can see that as the Block size increases the CPI decreases dramatically requiring less latency.

Processor 456:

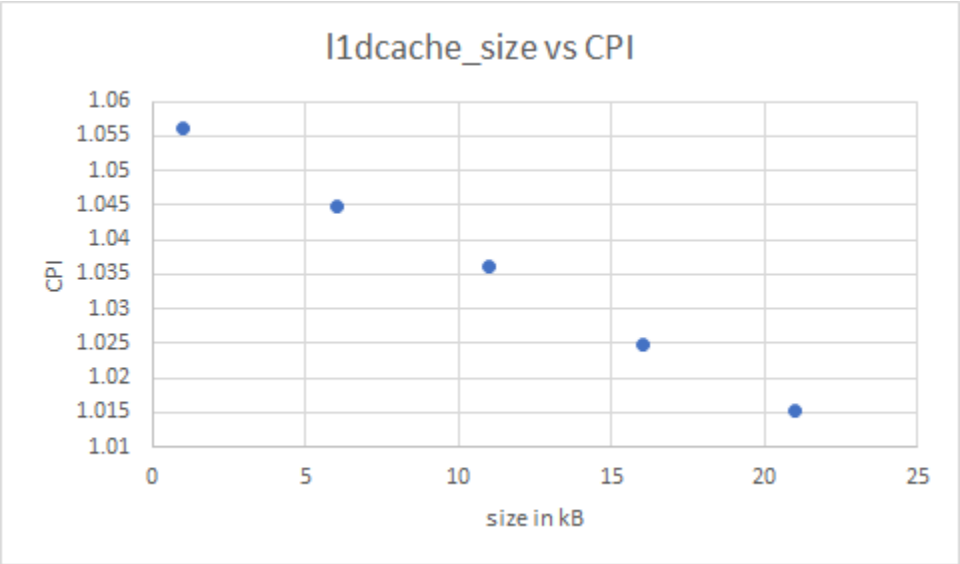

Figure 5.1: LD Cache vs CPI

In figure 5.1 we can see that as the LD Cache size increases the CPI decreases requiring less latency.

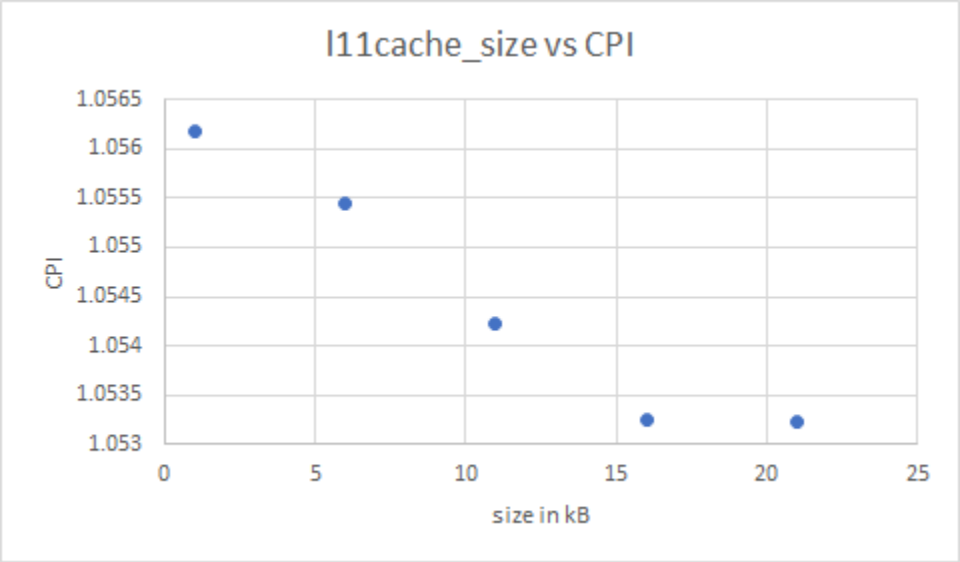

Figure 5.2: LI Cache vs CPI

In figure 5.2 we can see that as the LI Cache size increases the CPI decreases requiring less latency.

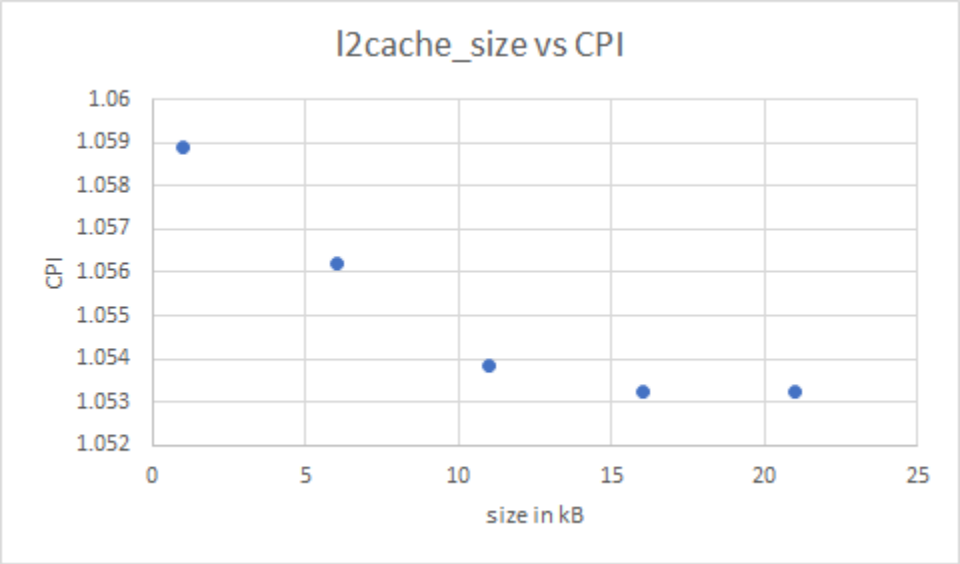

Figure 5.3: L2 Cache vs CPI

In figure 5.3 we can see that as the L2 Cache size increases the CPI decreases requiring less latency.

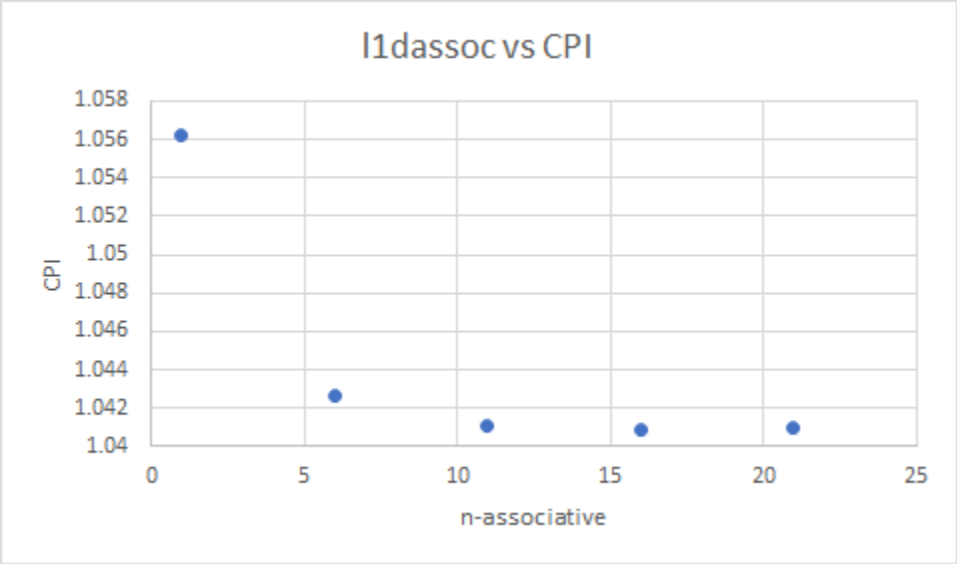

Figure 5.4: LD Assoc vs CPI

In figure 5.4 we can see that as the LD Assoc size increases the CPI decreases dramatically requiring less latency.

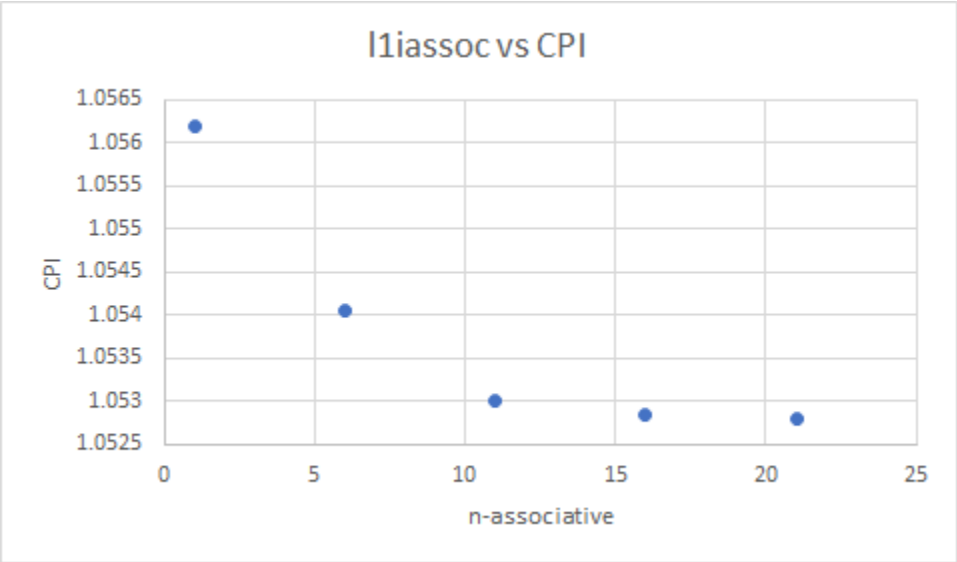

Figure 5.5: LI Assoc vs CPI

In figure 5.5 we can see that as the LI Assoc size increases the CPI decreases dramatically requiring less latency.

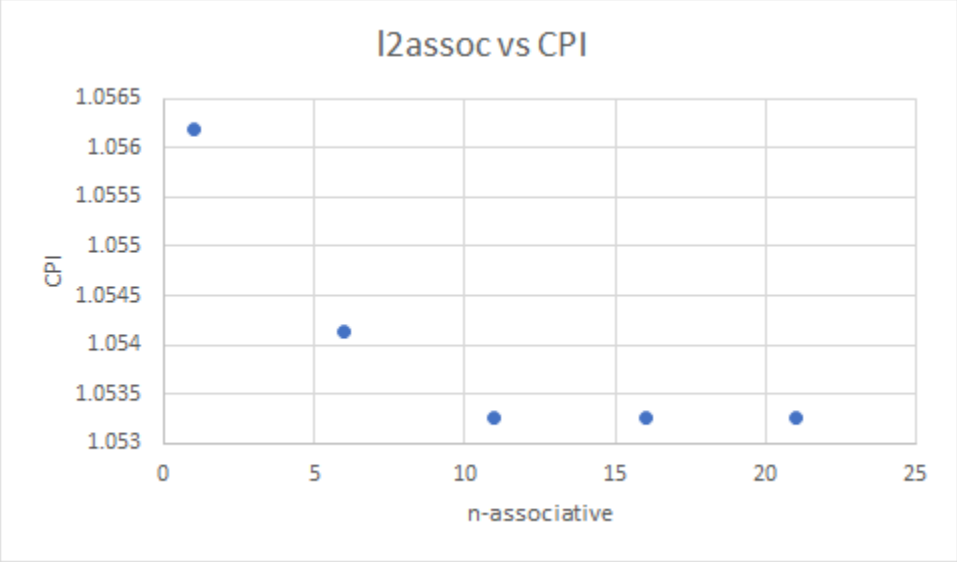

Figure 5.6: L2 Assoc vs CPI

In figure 5.6 we can see that as the L2 Assoc size increases the CPI decreases dramatically requiring less latency.

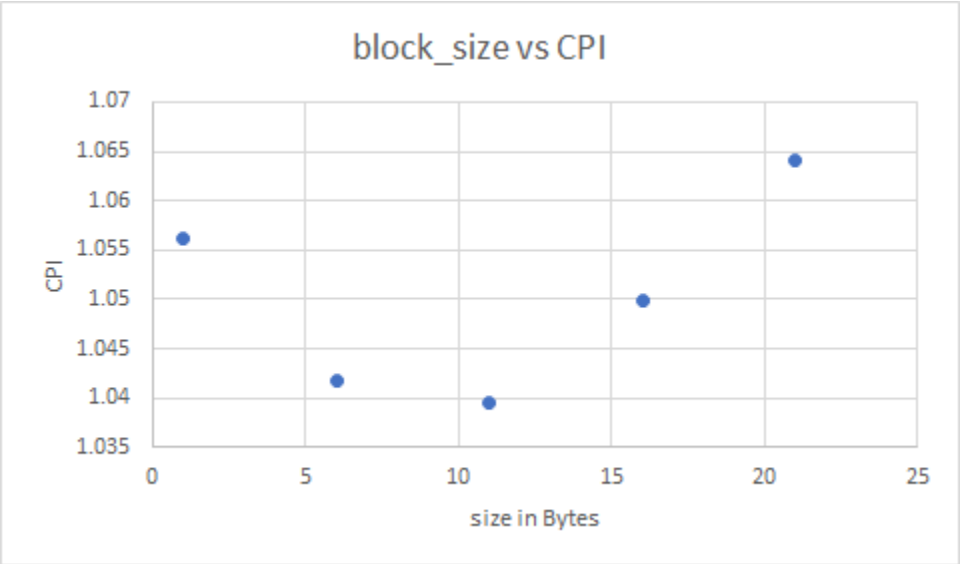

Figure 5.7: Block Size vs CPI

In figure 5.7 we can see that as the Block size increases the CPI decreases dramatically at first then peaks requiring less latency at first but inversely causing negative impact as block size gets bigger.