Embedded Systems Architecture

Session #3

Instruction Sets

- Processor Basics
- ARM Processor
- PICmicro mid-range family
- TI C55x Digital Signal Processor

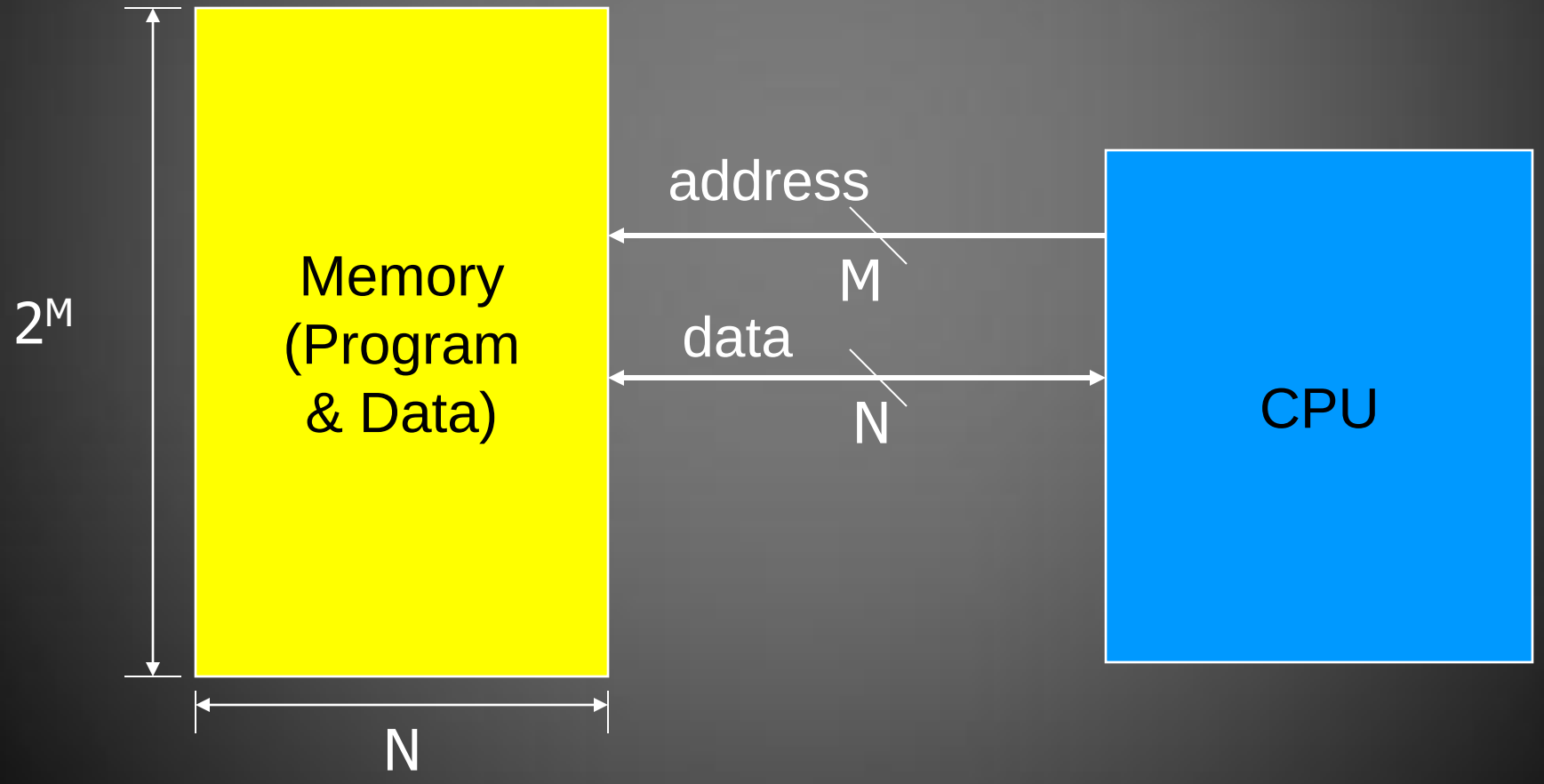
Processor Basics

- Memory Architectures
- Endianess
- Addressing Modes
- Instruction Execution
- Instruction Execution Pipelining
- Register Sets

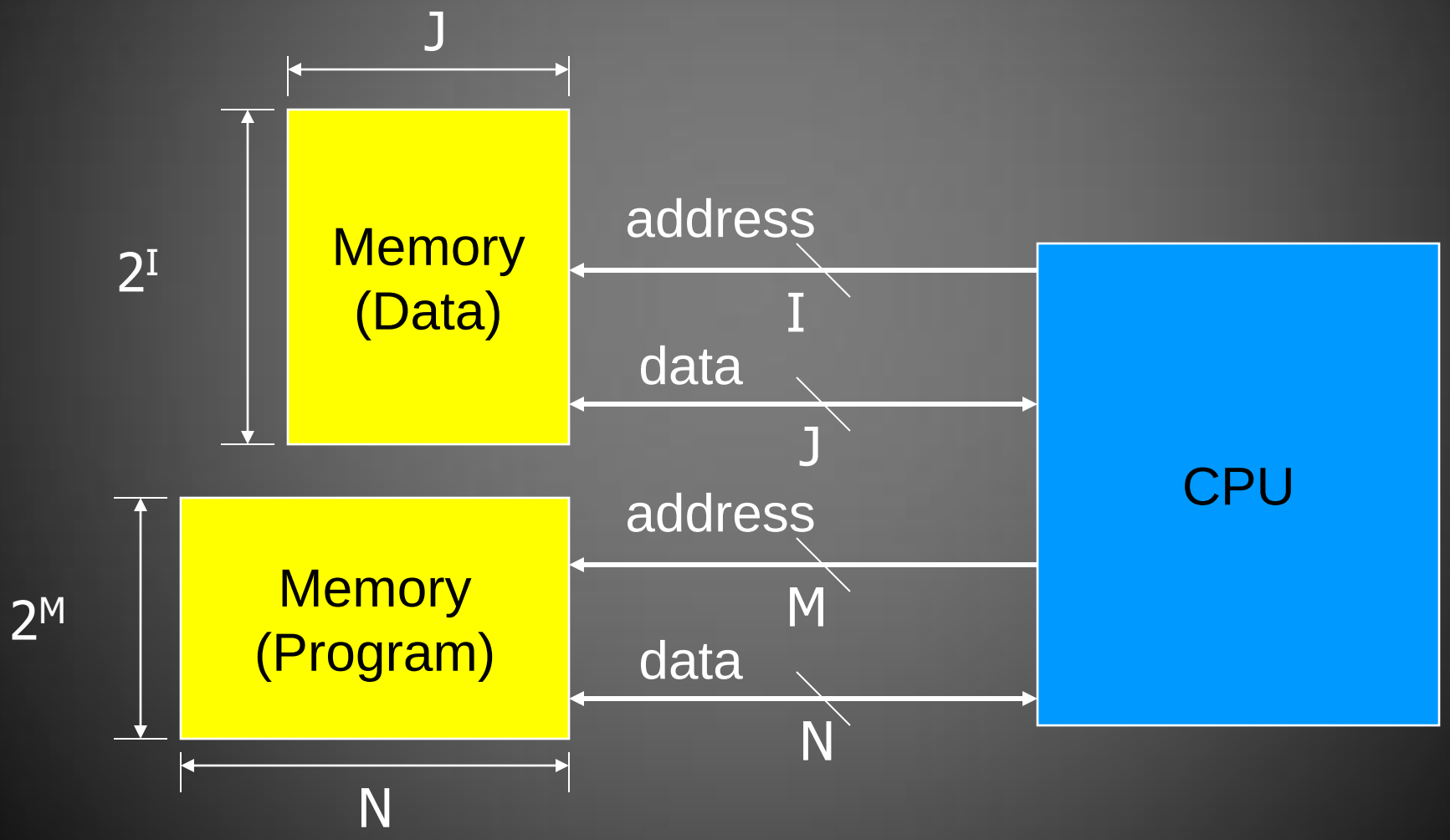
Memory Architectures

- von Neumann architecture
- Harvard architecture

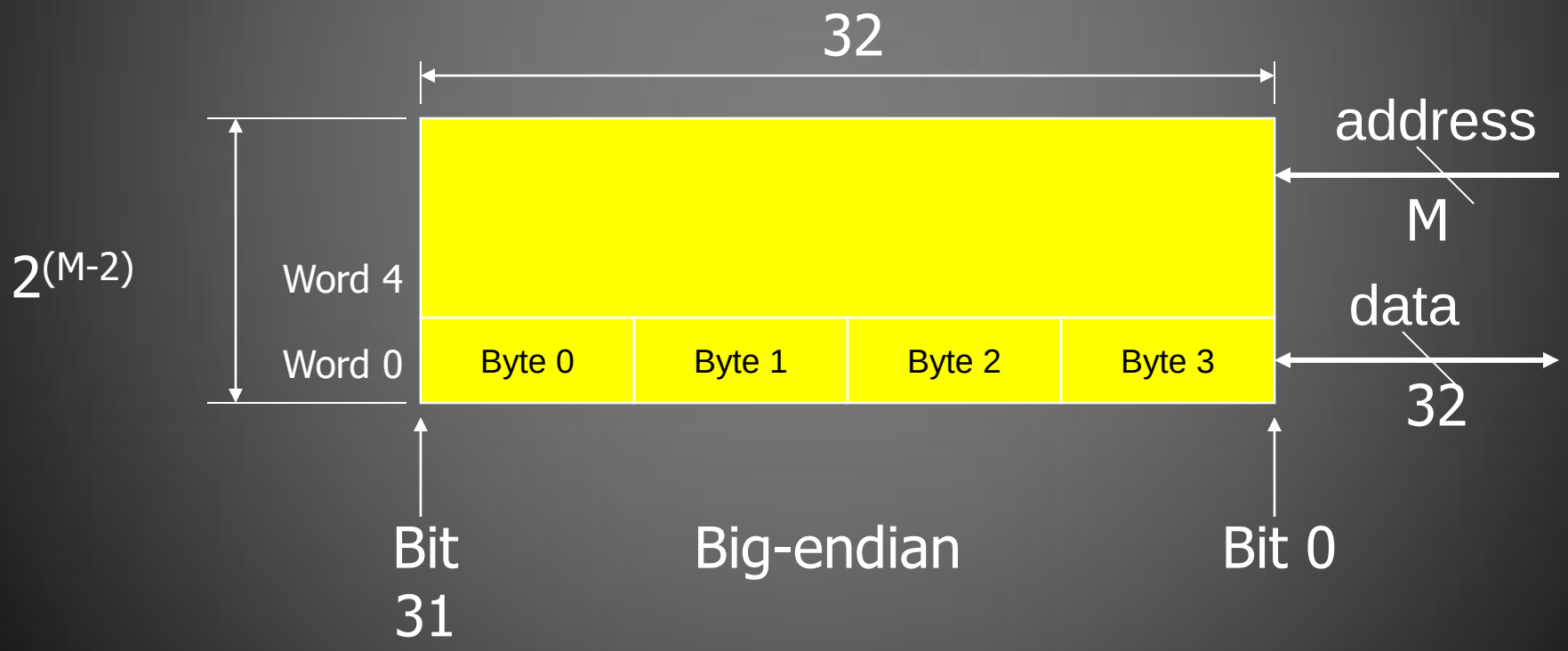
Von Neumann architecture



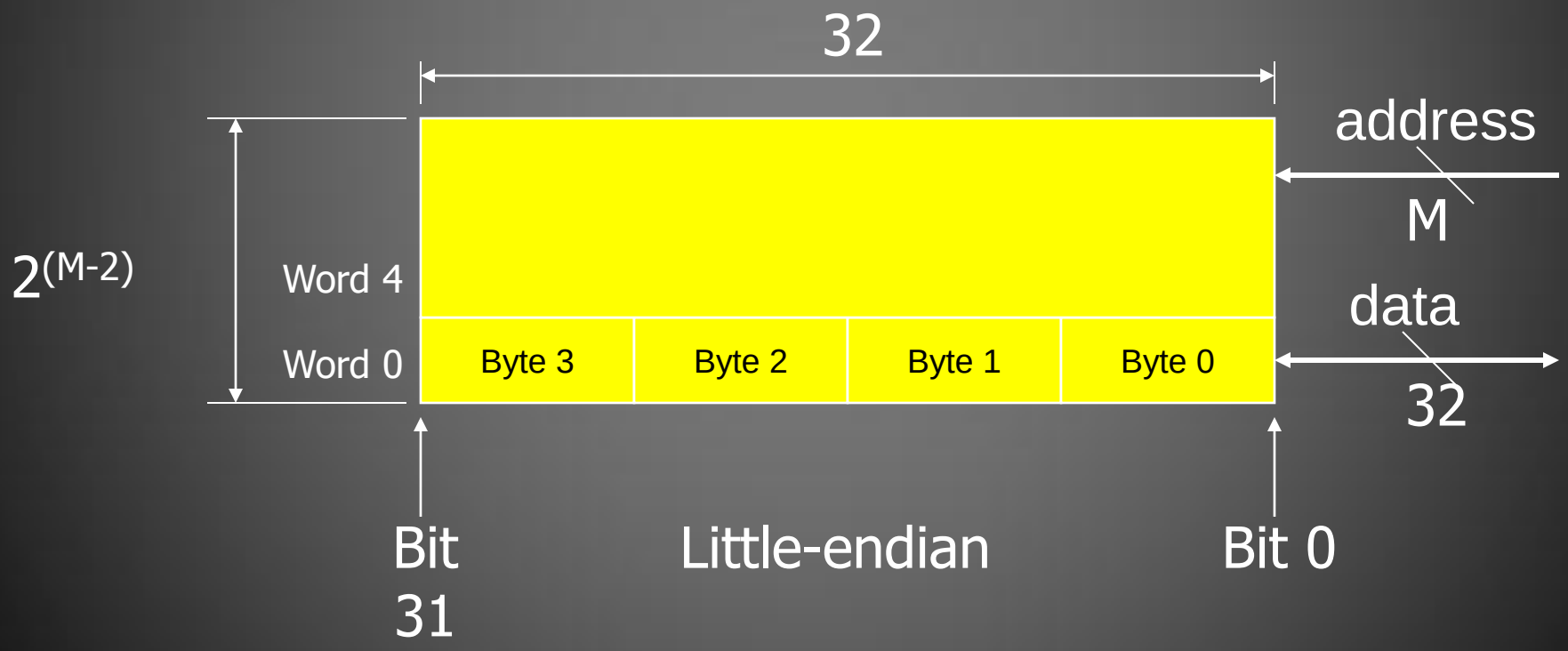
Harvard architecture



Endianess


32
address
M
$2^{(M-2)}$
Word 4
Word 0
Byte 0
Byte 1
Byte 2
Byte 3
data
32
Bit 31
Big-endian
Bit 0

Endianess (continued)



Addressing modes

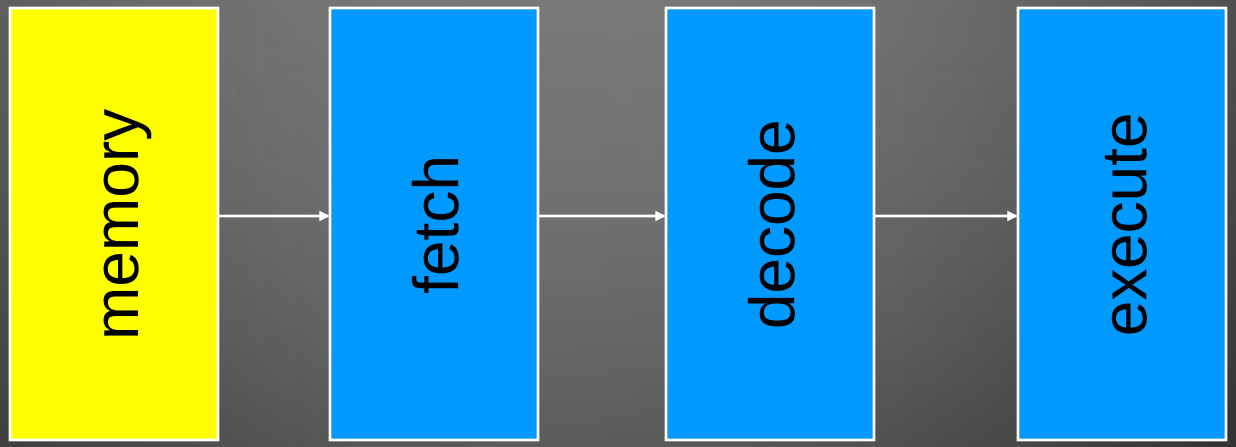
- Absolute
- Immediate
- Program relative
- Register direct
- Register indirect

Instruction Execution

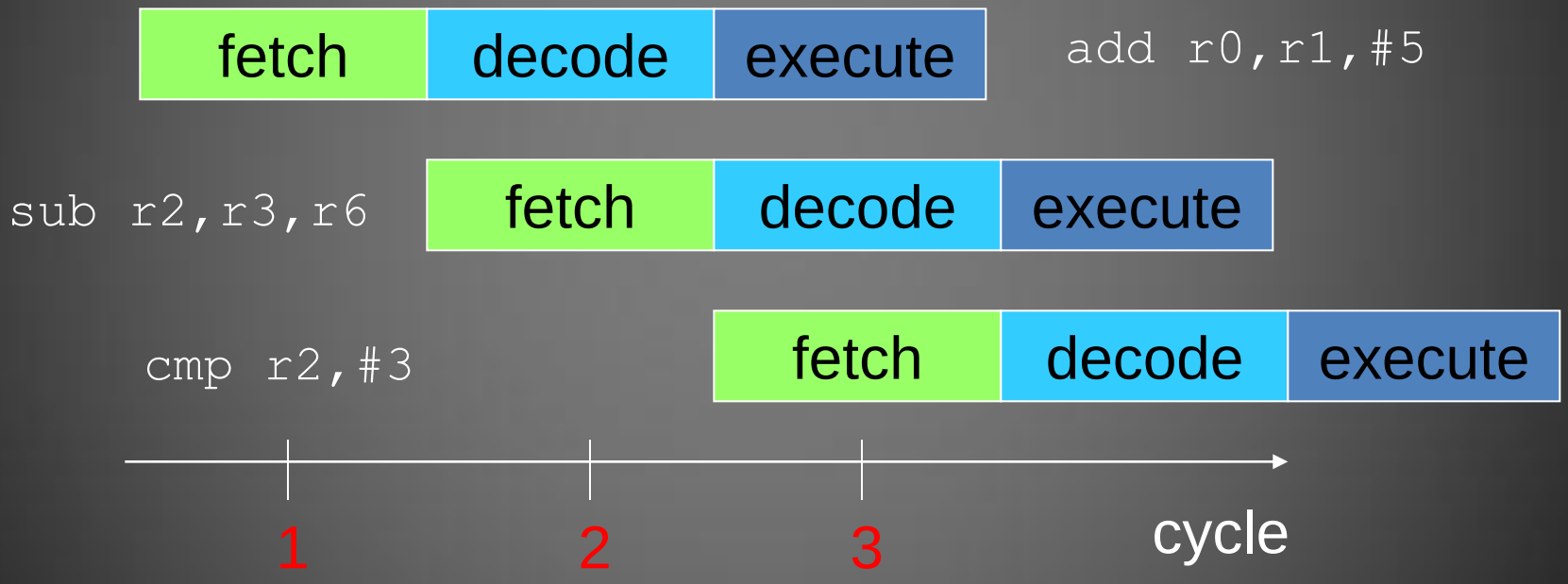
- Multiple cycle, single operation
  - CISC
- Single cycle, single operation
  - RISC, DSP
- Single cycle, multiple operation
  - RISC, DSP, VLIW, SIMD
- The line between RISC and CISC is not so well defined these days.

Instruction Execution Pipelining

- Execute several instructions simultaneously but at different stages.
- Simple three-stage pipeline:



Execution Pipelining



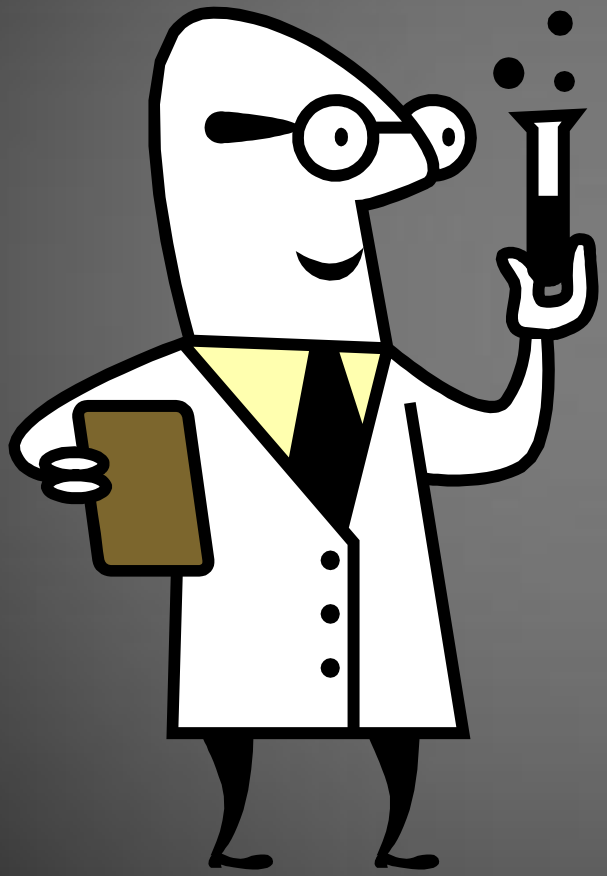
Register Sets

- Directly accessible
- Indirectly accessible
- Specific purpose
- General purpose
- Redundant register sets

Three Processor Architectures

- ARM Processor
- PICmicro mid-range family
- TI C55x Digital Signal Processor

Lab Session #3



- Control Flow Diagrams

Last Week

- Data Flow Diagrams
  - Graphical Elements
    - Process
    - Data Flow
    - Data Store
    - Terminator
  - Process Specification (PSPEC)
  - DFD Hierarchy
  - Data Context Diagram

This Week

- Data vs. Control
- Control Flow Diagrams
- Data Conditions

Data vs. Control

- *Data* signals may be either discrete or continuous valued.
- *Control* signals *must be* discrete valued.

Control Flow Diagrams (CFD)

- Control Flow
- Control Store
- Control Specification (CSPEC)
- Control Context Diagram (CCD)

Control Flow

- Definition
  - A control flow is a pipeline through which control information of known composition flows.
- Symbol
  - A named unidirectional or bidirectional *dashed* vector.
- Naming Convention
  - No verbs, only nouns and adjectives.

Control Store

- Definition
  - A store is simply control information retained for later use.
- Symbol
  - Parallel lines with the name of the stored control information.
- Naming same as control flow.

Control Specification (CSPEC)

- Definition
  - A CSPEC describes how the outputs are generated from the inputs. *(Just like a PSPEC)*
- Symbol
  - Shown as a single vertical line or bar.
- Naming Convention
  - Possesses the same name and number as it's CFD.

Control Context Diagram (CCD)

- Top level CFD with a single process for the system itself and terminators indicating system boundaries.

Data Conditions

- The output of a PSPEC *may* contain one or more control flows.

Data Conditions Example

- Compare PSPEC
  - If A>B then Comparison=GREATER_THAN
  - Elsif A=B then Comparison=EQUAL
  - Else Comparison=LESS_THAN