Embedded Systems Architecture

Session #6

Moore's Law

- "The number of transistors on an integrated circuit doubles every 24 months."

Small Scale Integration (SSI)

- Fixed logic (7400, 5400 series families)
  - AND, OR, INV logic gates
  - Flip-flops
- Memory devices

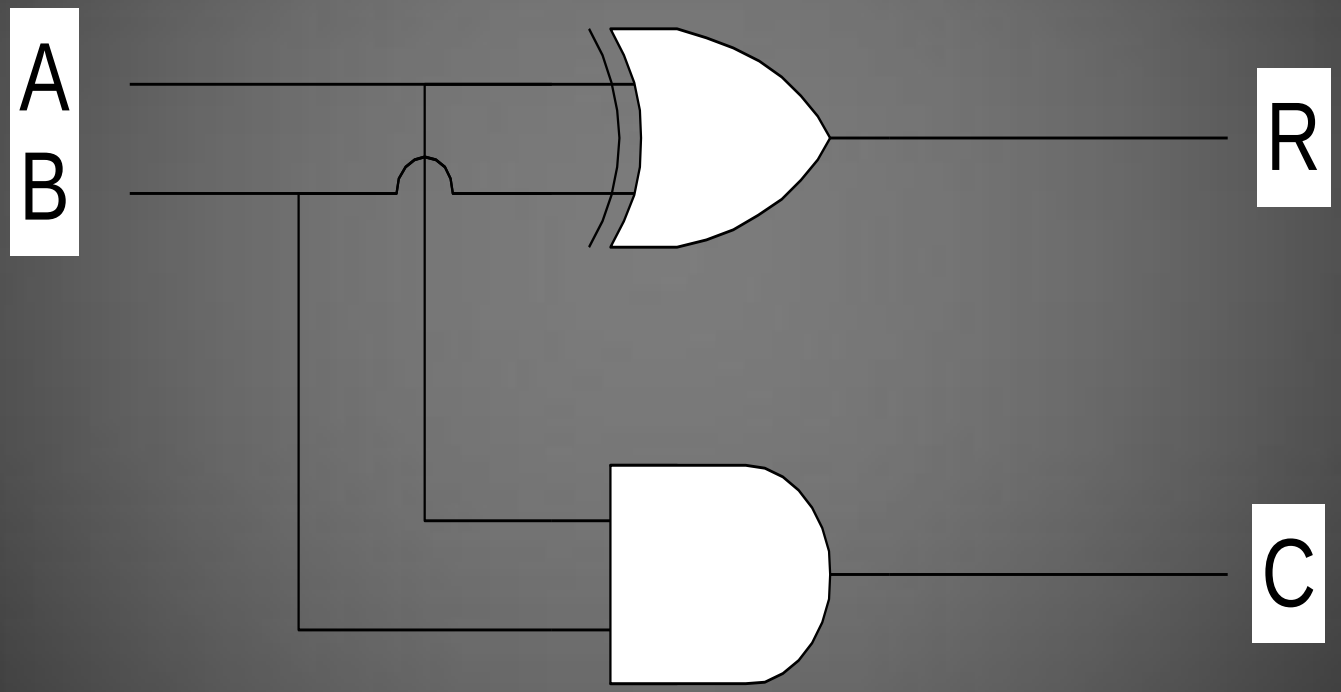
Truth Table

- A tabular method for describing the response of digital outputs to digital inputs.
- Strictly combinatorial (no internal memory).

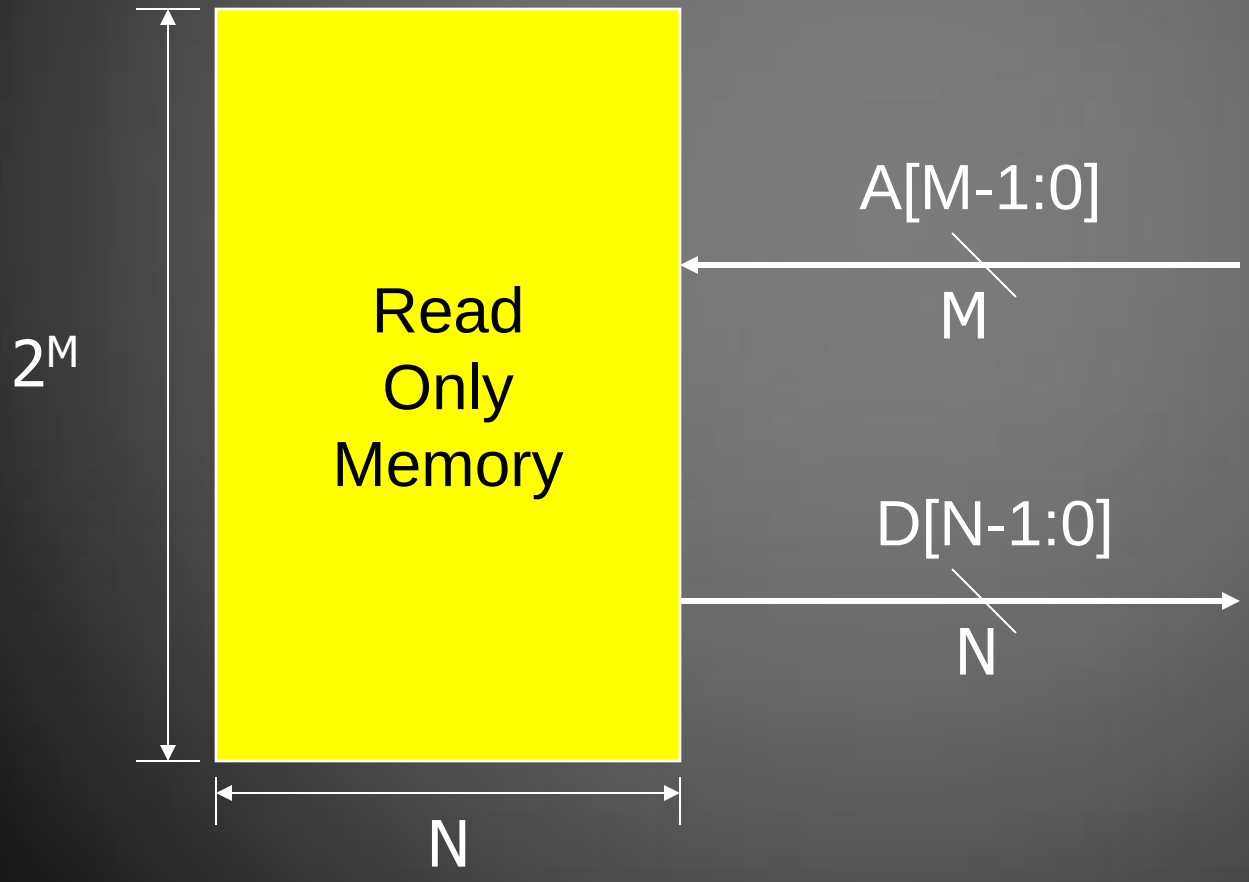
Truth Table Example

A	B	R	C
0	0	0	0
0	1	1	0
1	0	1	0
1	1	0	1

Truth Table Logic



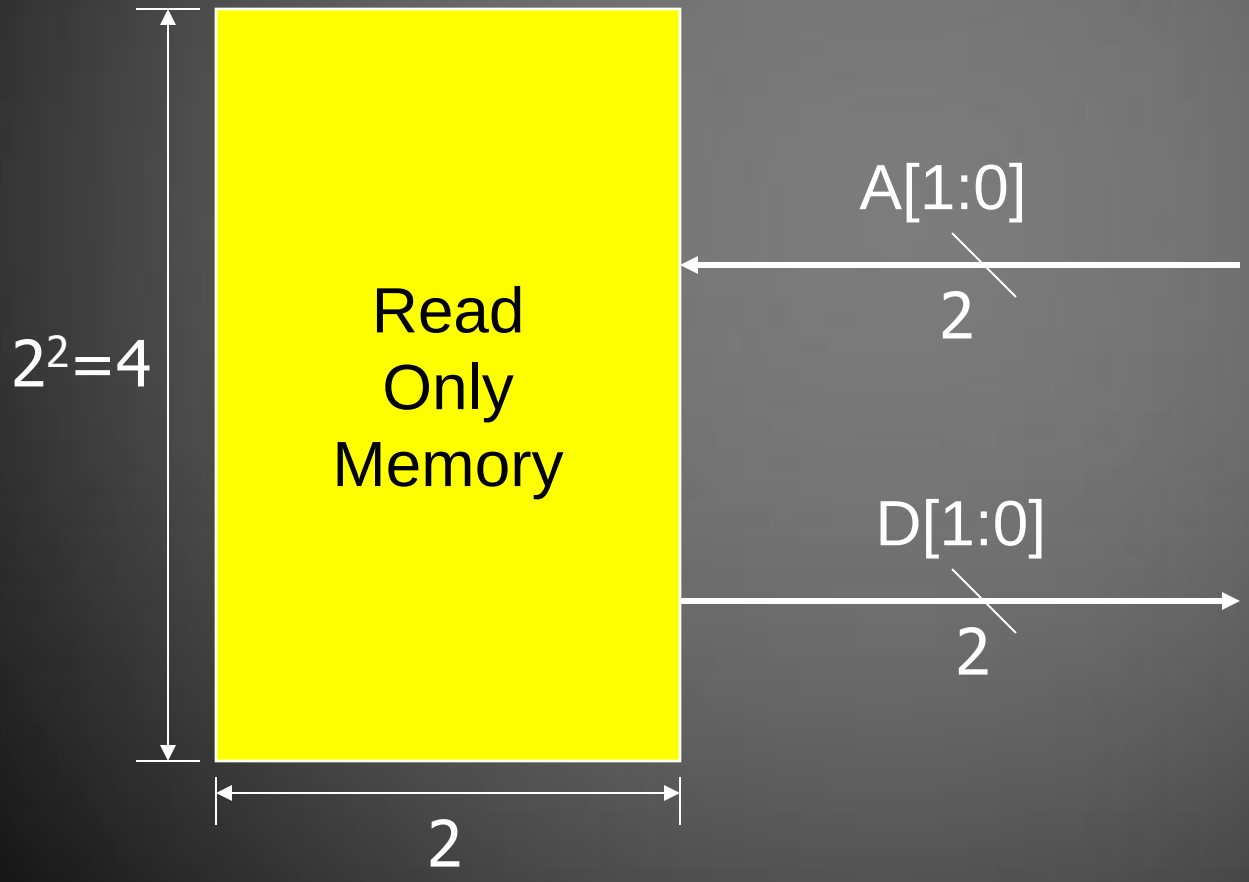
Lookup Table



Lookup Table Example

A1(A)	A0(B)	D1(R)	D0(C)
0	0	0	0
0	1	1	0
1	0	1	0
1	1	0	1

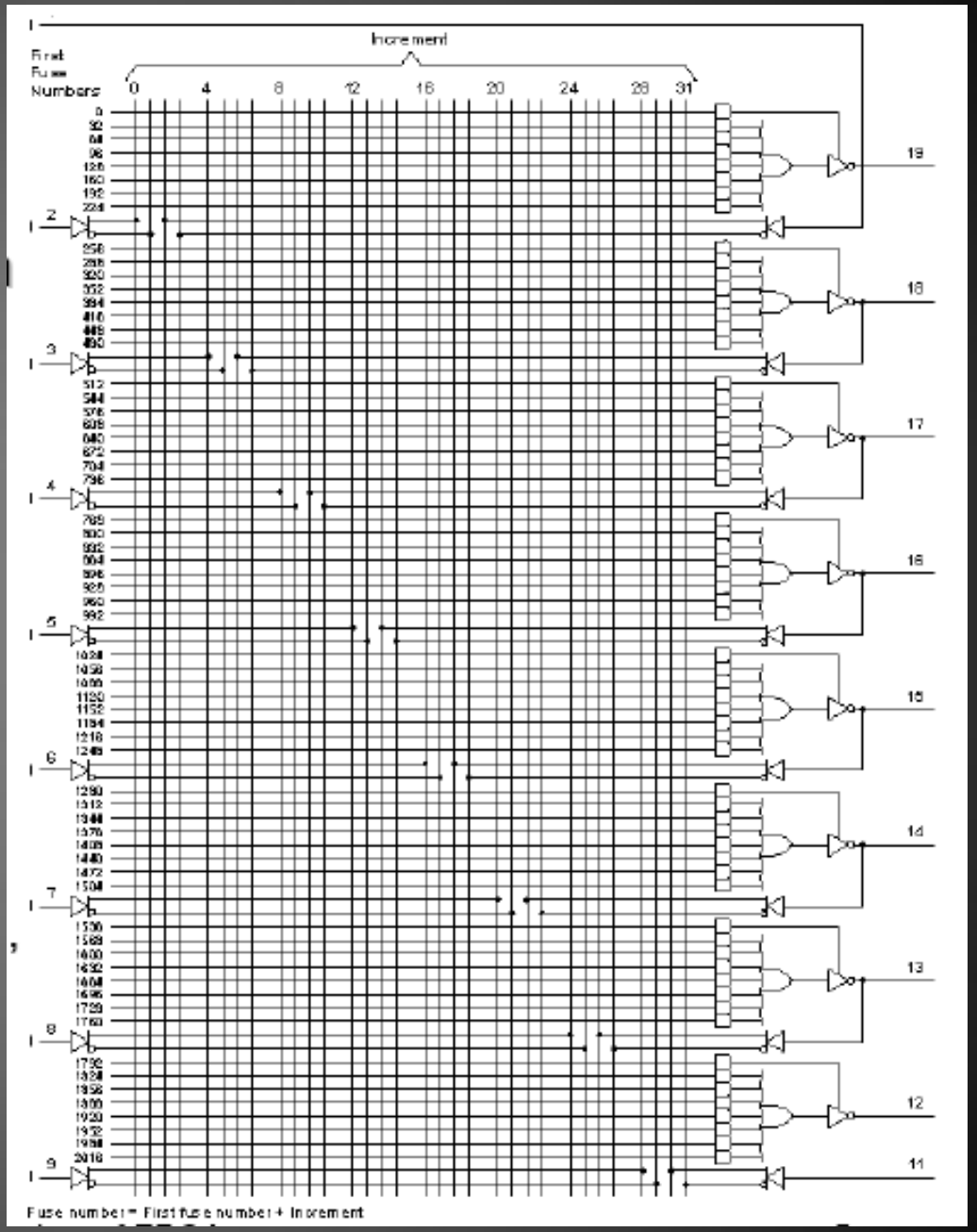
Lookup Table



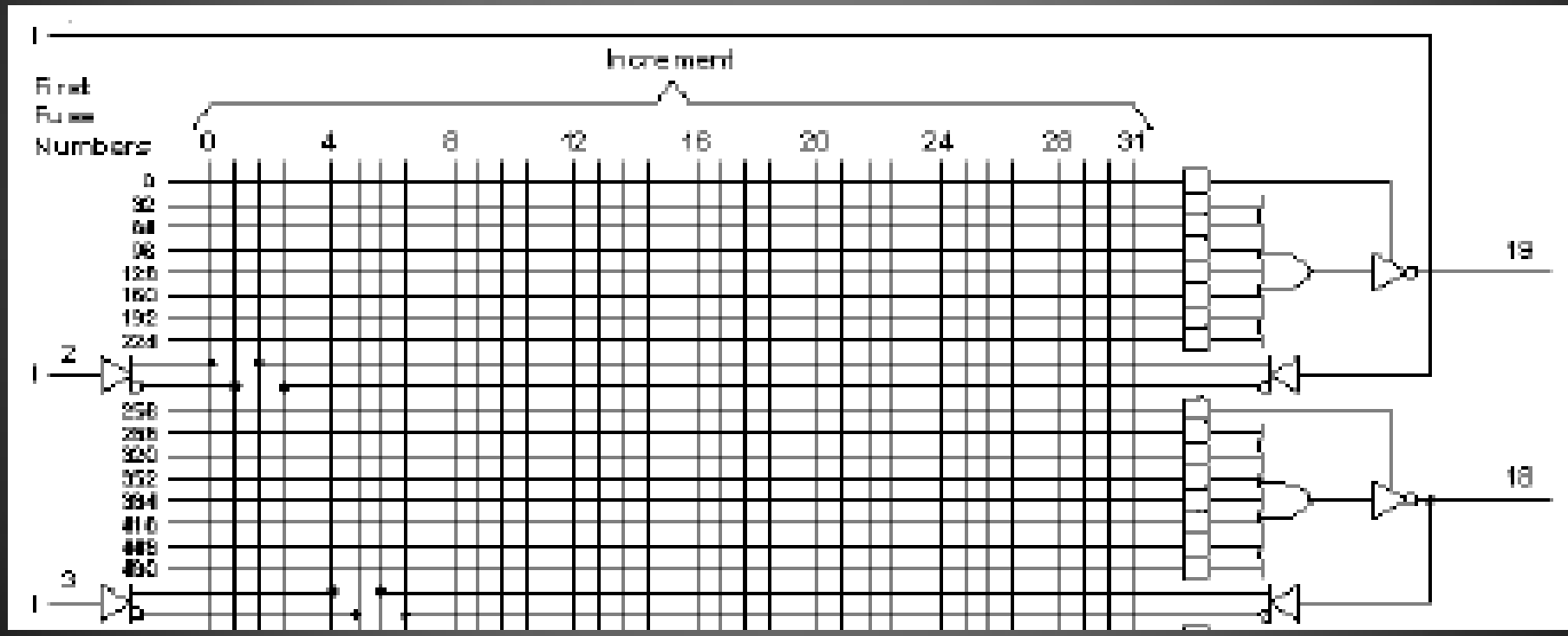
Programmable Logic Device (PLD)

- Programmable Array Logic (PAL)
- Complex PLD (CPLD)
- Field-programmable gate array (FPGA)

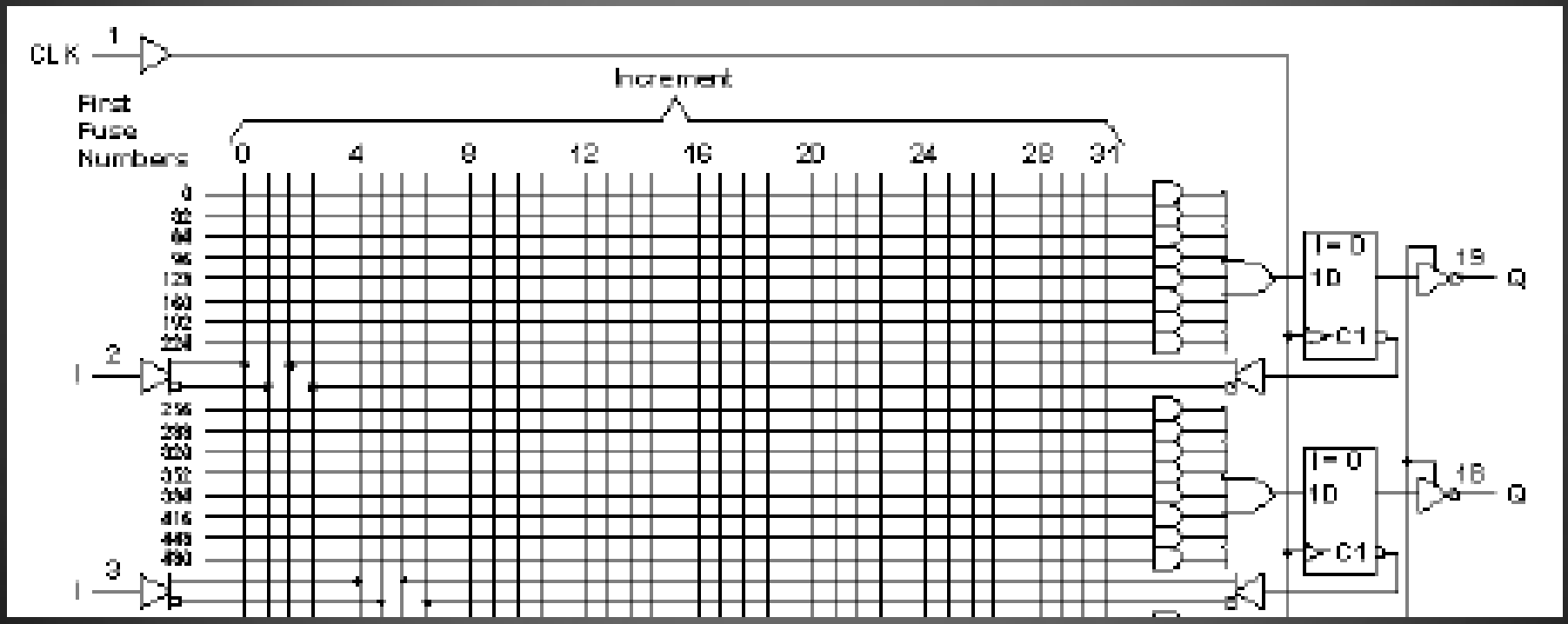
16L8 PAL


Increment
First Fuse Numbers
0
4
8
12
16
20
24
28
31
19
18
17
16
15
14
13
12
11
Fuse number = First fuse number + Increment

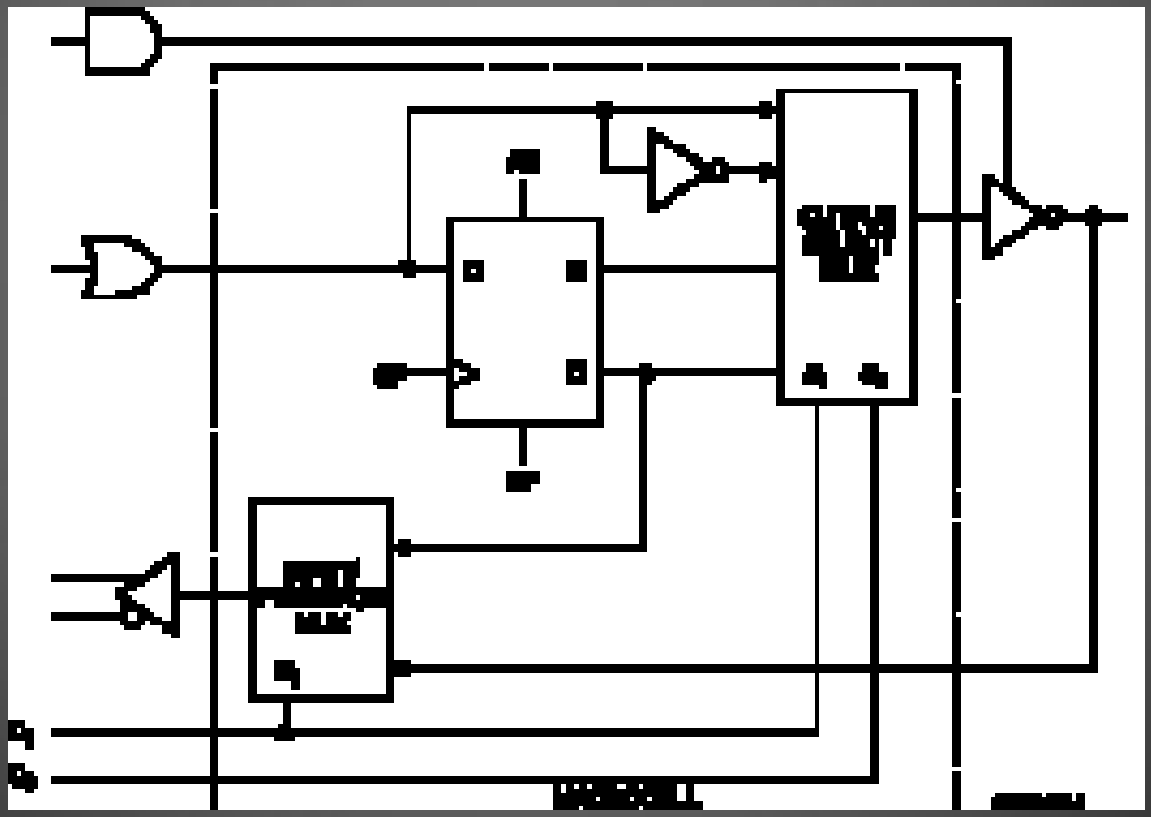
16L8 PAL



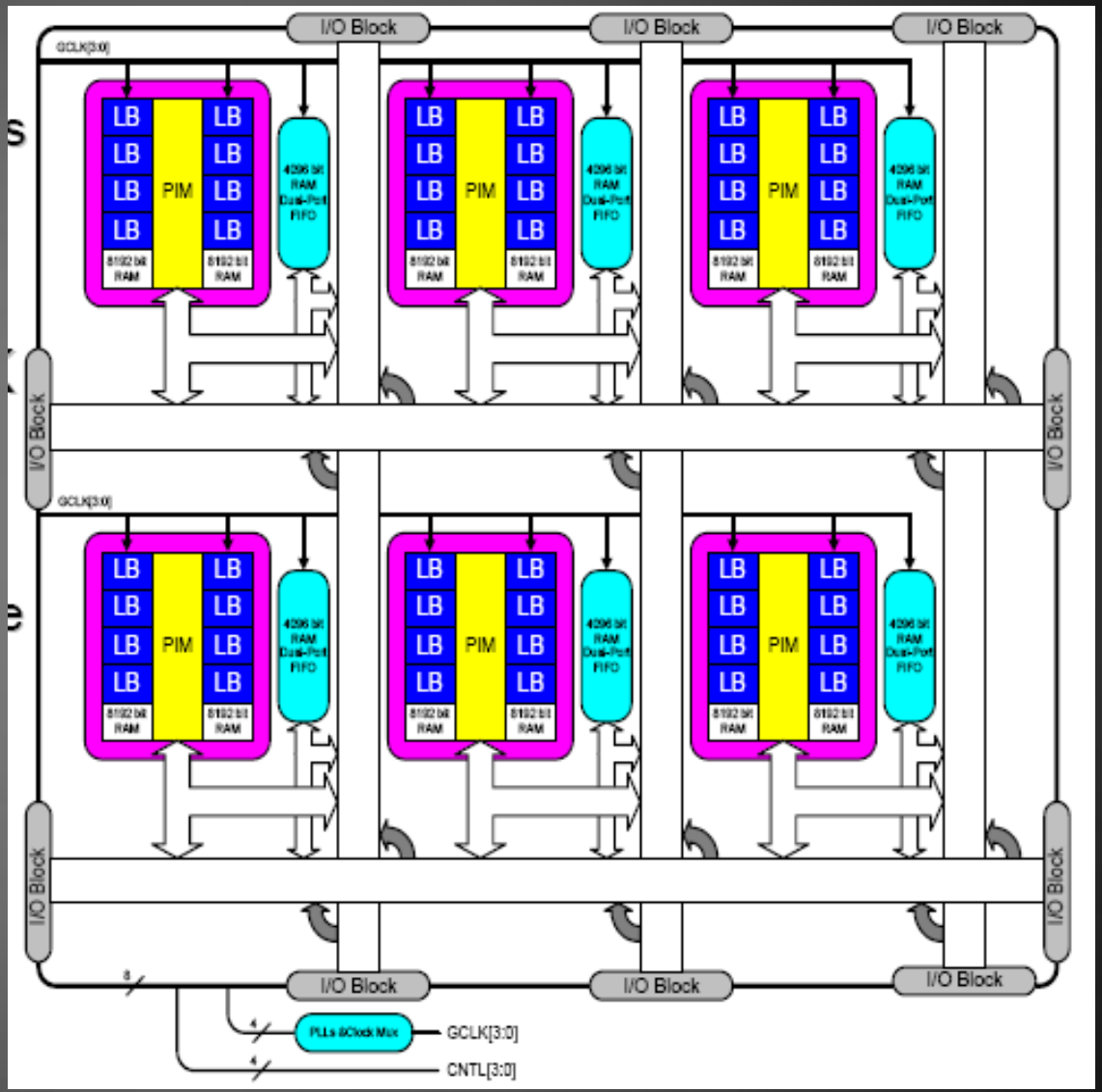
16R8 PAL


CLK
1
Increment
First
Fuse
Numbers
0
4
8
12
16
20
24
28
31
2
3
I = D
1D
C1
19
Q
I = D
1D
C1
18
Q

22V10 Macro Cell

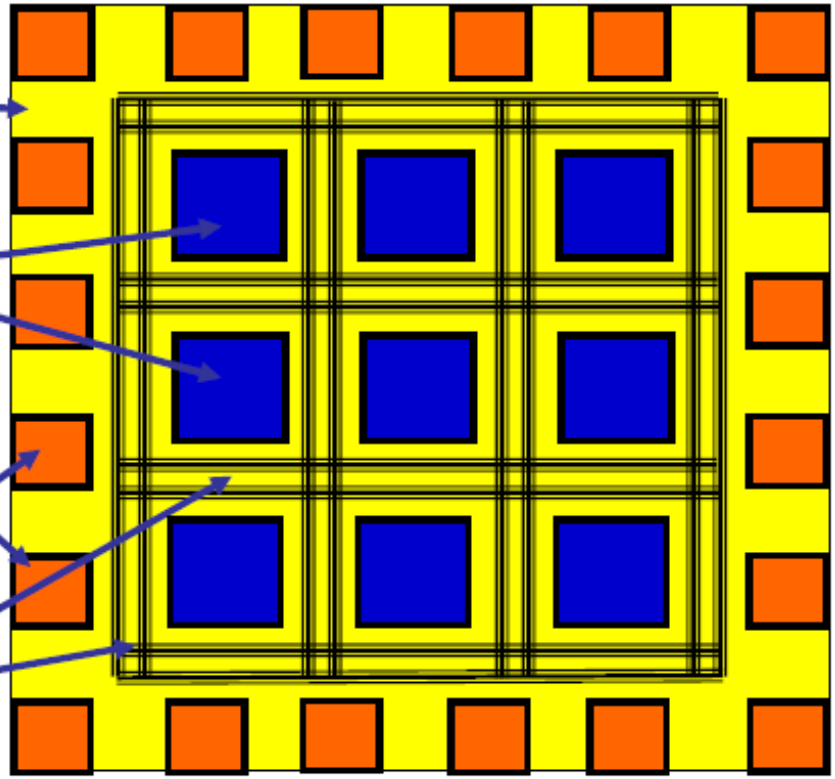


CPLD


I/O Block
I/O Block
I/O Block
GCLK[3:0]
LB
PIM
4096 bit RAM Dual-Port FIFO
8192 bit RAM
I/O Block
I/O Block
I/O Block
I/O Block
I/O Block
I/O Block
I/O Block
PLLs &Clock Mux
GCLK[3:0]
CNTL[3:0]

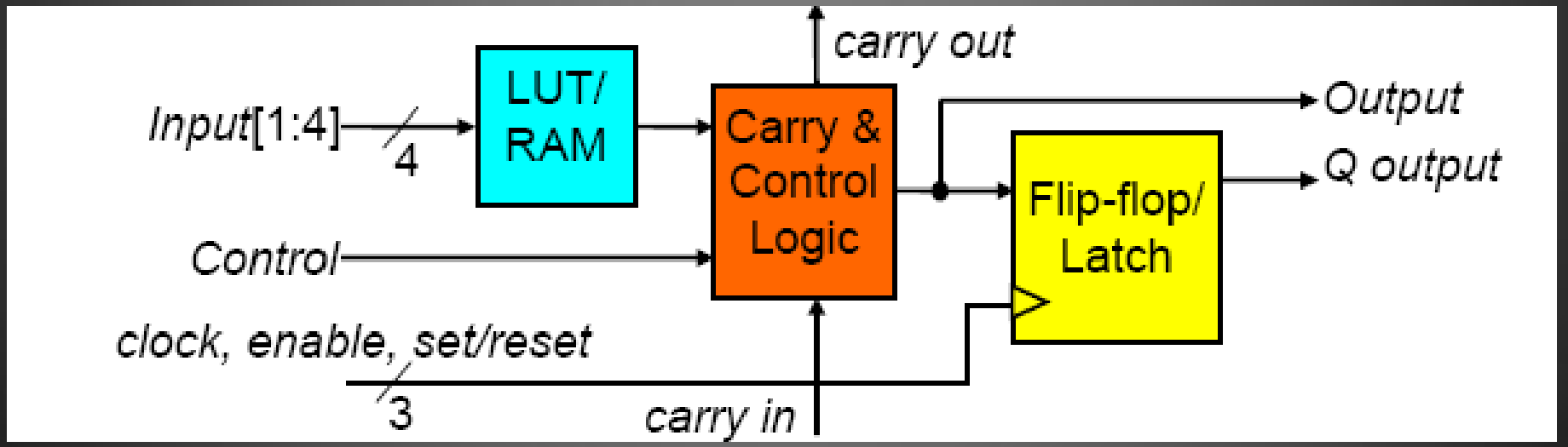
FPGA

- Configuration Memory
- Programmable Logic Blocks (PLBs)
- Programmable Input/Output Cells
- Programmable Interconnect



Typical Complexity = 5 million – 1 billion transistors

Programmable Logic Block



SoC (System on Chip)

- SoC Definition
- SoC Choice Considerations
- SoC Fabrication
- Hardcore vs. Softcore
- SoC Processors

SoC Definition

- Integration of processor, memory, bus, DMA, and peripherals into a single IC chip.

SoC Choice Considerations

- Advantages
  - Physically smaller.
  - Less cost at higher volumes.
  - Greater speed.
  - Greater reliability.
- Disadvantages
  - Greater development time.

SoC Fabrication

- Application-specific integrated circuit (ASIC)
  - Full-custom
  - Standard cell
  - Structured
- FPGA (PSoC)

Hardcore vs. Softcore

- This is a FPGA specific issue.
- A hardcore resource like a processor, multiplier, block RAM, or I/O peripheral consists of silicon real estate dedicated towards that particular function.
- A softcore resource is implemented using the normal gate array logic resources.

SoC Processors

- ARM
- PowerPC
- MicroBlaze / PicoBlaze
- Nios II
- OpenRISC
- SPARC
  - Leon (Leox)
  - OpenSPARC
  - UltraSPARC T1

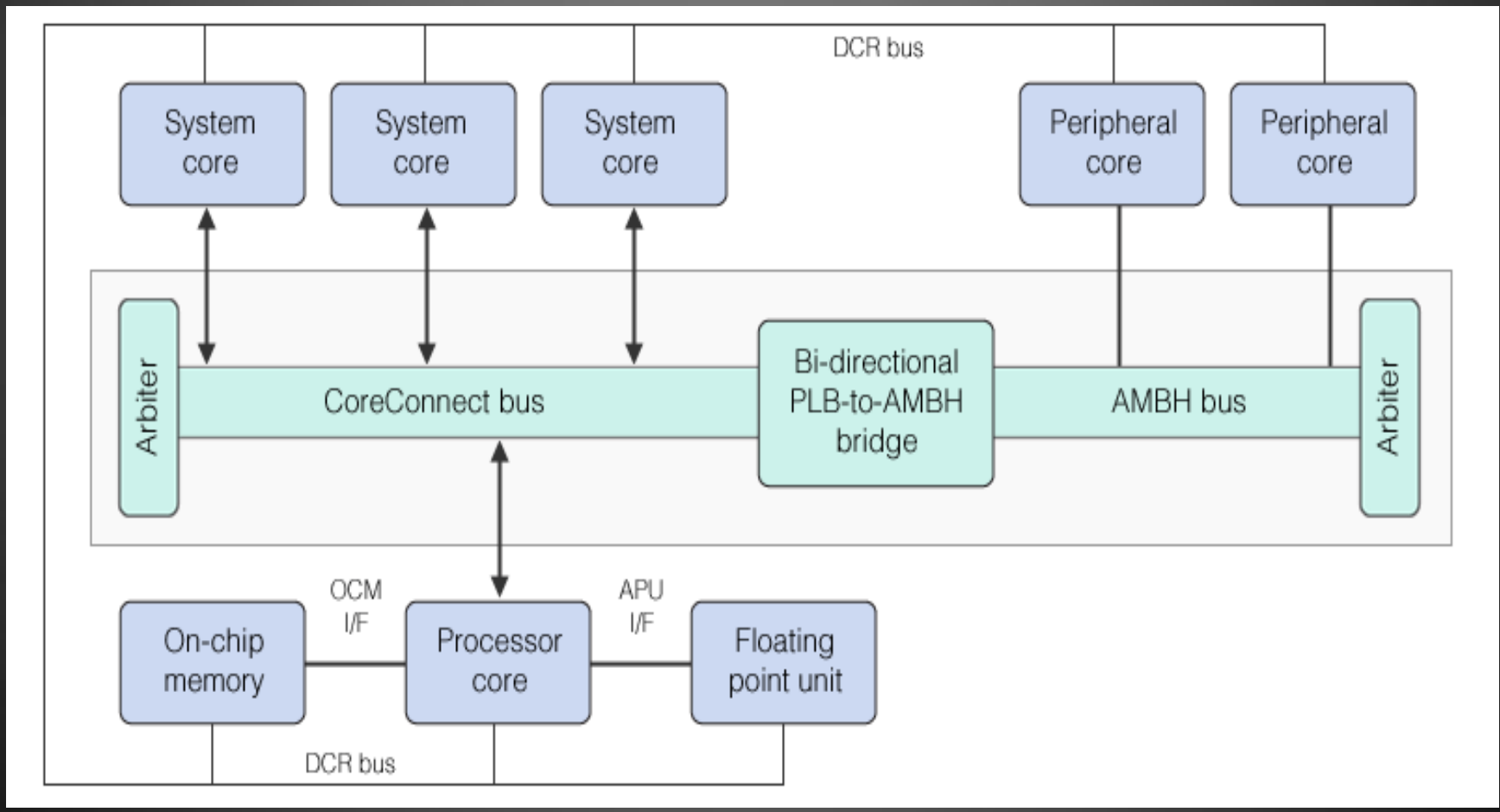
SoC (Continued)

- SoC Buses
- SoC Peripherals
- SoC Operating Systems

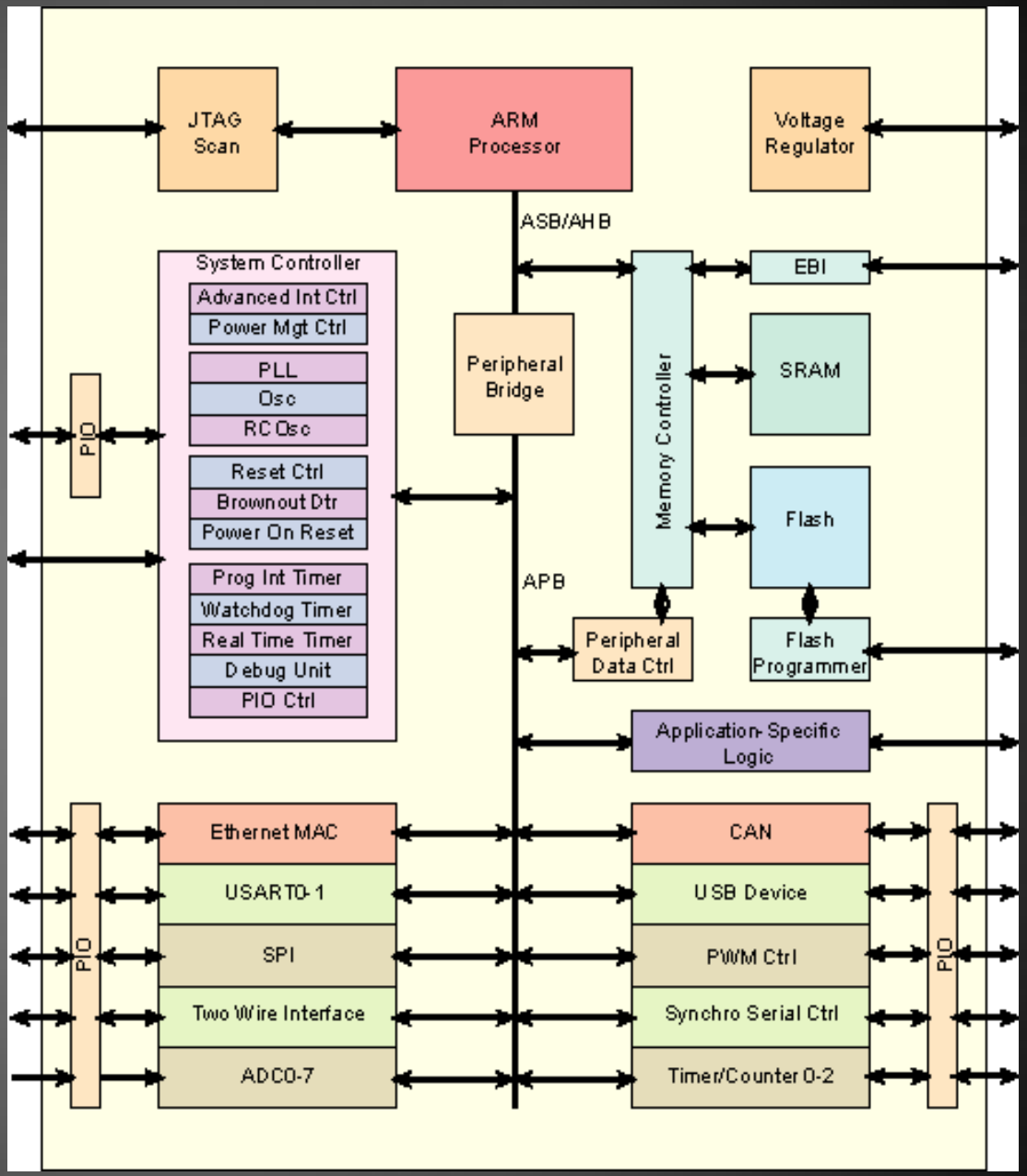
SoC Buses

- CoreConnect
- Wishbone
- AMBA
- Avalon
- OCP-IP

CoreConnect



AMBA


JTAG Scan
ARM Processor
Voltage Regulator
ASB/AHB
System Controller
Advanced Int Ctrl
Power Mgt Ctrl
PLL
Osc
RC Osc
Reset Ctrl
Brownout Dtr
Power On Reset
Prog Int Timer
Watchdog Timer
Real Time Timer
Debug Unit
PIO Ctrl
PIO
Peripheral Bridge
EBI
Memory Controller
SRAM
Flash
APB
Peripheral Data Ctrl
Flash Programmer
Application-Specific Logic
Ethernet MAC
USART0-1
SPI
Two Wire Interface
ADC0-7
CAN
USB Device
PWM Ctrl
Synchro Serial Ctrl
Timer/Counter 0-2
PIO

SoC Peripherals

- Analog interface converters
- Ethernet controllers
- UARTs
- PS2 keyboard & mouse interfaces
- VGA

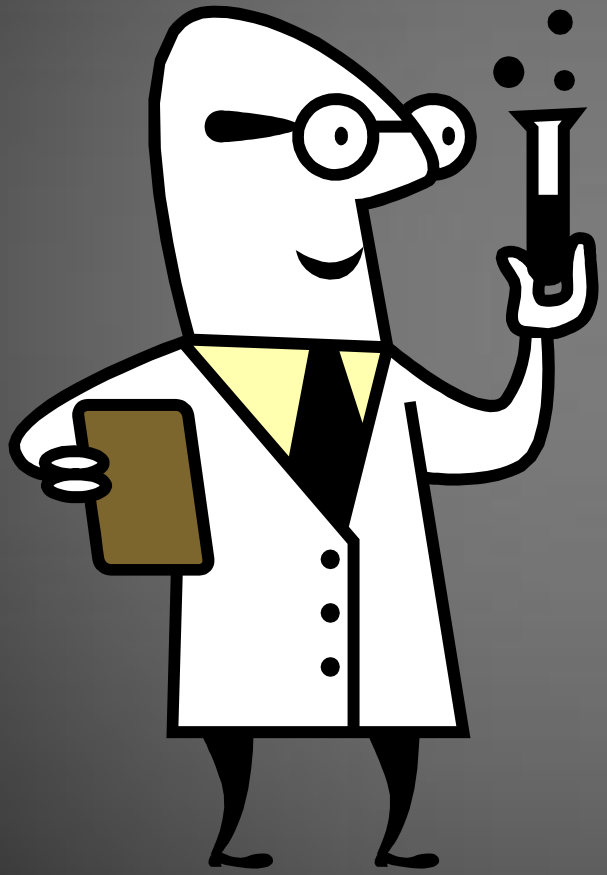
SoC Operating Systems

- FreeRTOS
- eCos
- uClinux
- µC/OS-II
- Xilkernal

Other Online SoC Resources

- Open Collector
- Design and Reuse
- OpenCores

Lab Session #6



- Architecture Model #1

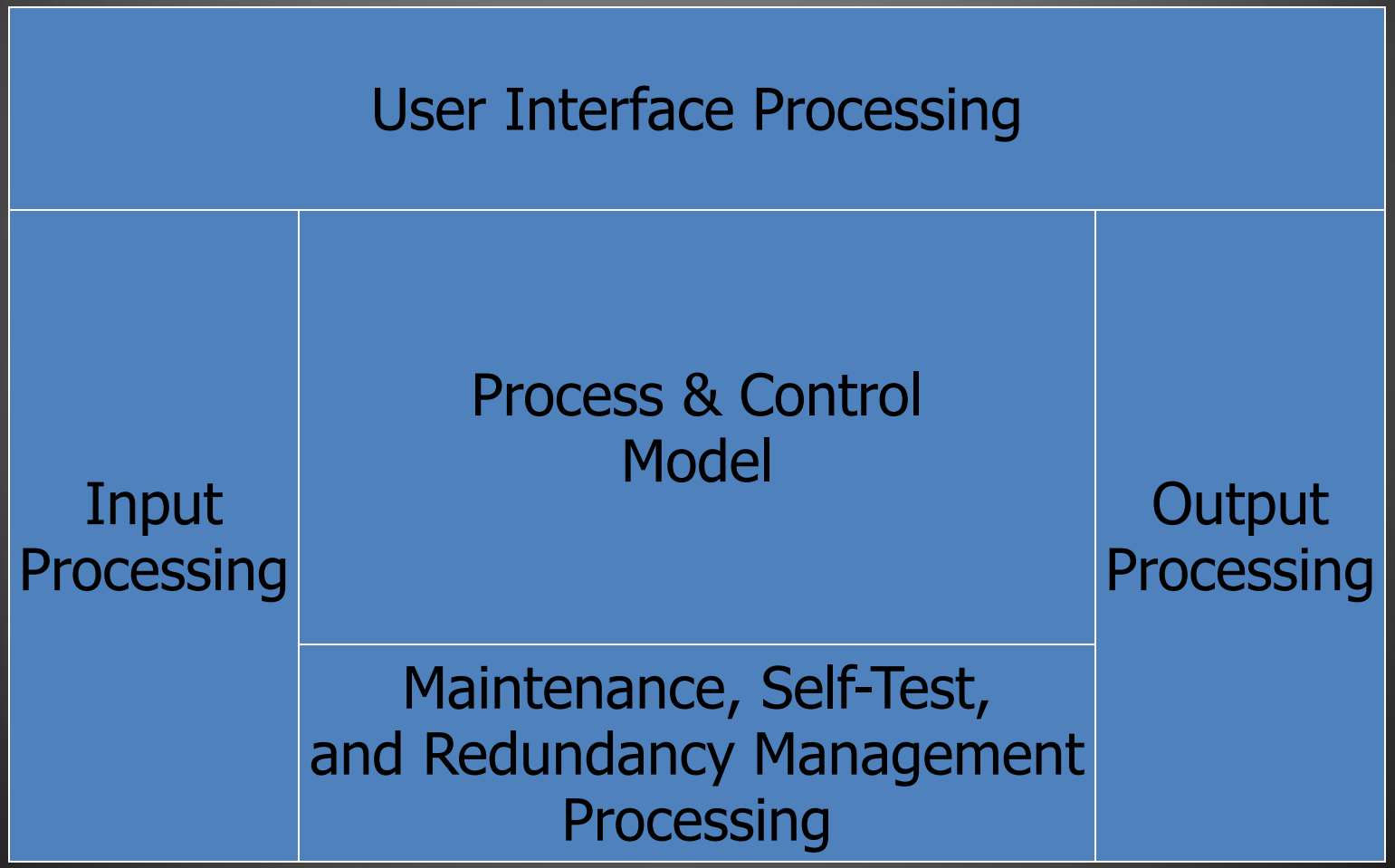
Architecture Model

- Architecture template
- Symbols
  - Architecture module
  - Information flow vector
  - Information flow channel

Architecture Template

- Adds 4 perspectives to the requirements model:
  - Input processing.
  - Output processing.
  - User interface processing.
  - Maintenance or self-test processing.

Architecture Template



Architecture Module Symbol

- Contains allocation of requirements processes, flows, & stores to a physical module.
- Symbol: a rectangle with rounded corners.
- Naming convention: noun with no verbs.

Information Flow Vector Symbol

- Represents all the flows between architecture modules.
- Symbol: same as that of control and data flows.

Information Flow Channel Symbol

- Shows the physical means by which information flows between architecture modules.
- Symbol should be indicative of physical channel.
- Naming convention is the same that of information flow vector.