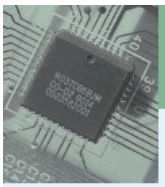

Nonvolatile MRAM is ready for prime time

Devices unique features can provide interesting market opportunities

BY TOM LEE
Freescale Semiconductor
Austin, TX
http://www.freescale.com

The first commercial memory chip to use the magnetic random-access memory (MRAM) technology in a 4-Mbit chip was announced this summer. This memory technology, which uses magnetic moments to store the bit state, has been talked about for years, but is finally a reality. MRAM is nonvolatile memory that features unlimited endurance. MRAM has unique features that can open up interesting product opportunities for a range of devices.

MRAM features

The recently announced 4-Mbit MRAM chip is arranged in a 256-K x 16-bit configuration with an asynchronous design that uses standard chip enable, write enable, and output enable pins. Separate byte enable pins allow flexibility to read and write data as 8 or 16 bits. MRAM is inherently a nonvolatile memory with a minimum data retention of 10 years.

The MRAM chip has infinite write-cycling capability. Empirical studies have shown the bit cells to endure over 58 trillion write and read cycles under the worst case operating conditions. No endurance failures have been recorded with the chip's bit cell to date, and the bit cycling study is ongoing.

The device is fabricated using the 0.18-µm process technology with a total of five layers of interconnect and runs on a 3.3-V supply. It has write and read access times of 35 ns with fully static operation. Active read and write current values are 55 and 105 mA, and typical standby current is 9 mA.

This first MRAM device is available in a 44-pin TSOP type-II package with RoHS compliance. It is configured with an industry-standard center power and ground SRAM pinout so it can be used in existing hardware (see *Fig. 1*).

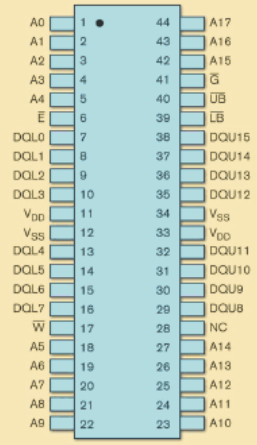

Fig. 1. The MR2A16A MRAM package has an SRAM-like footprint.

MRAM bit cell operation

The chip has toggle bit cells that contain one transistor and one magnetic tunnel junction. The magnetic tunnel junction or MTJ is at the heart of the MRAM bit cell. It is comprised of a very thin aluminum oxide dielectric layer placed between two magnetic layers. Each of the magnetic layers has a magnetic polarity associated with it. The top magnetic layer is called the free layer because it has the freedom to flip polarities and the bottom magnetic layer is called the fixed layer.

It is the polarity of the free layer that determines whether a bit is programmed to a "0" state or a "1" state. When the polarities of the free layer and the fixed layer are aligned, the resistance through the MTJ stack is low (see *Fig. 2*) and when they are opposite the resistance through the MTJ stack is high (see *Fig. 3*). This low and high resistance through the MTJ stack determines whether a bit cell is read as a "0" or a "1."

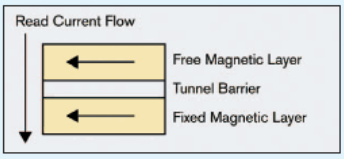

Fig. 2. When the polarities of the free layer and fixed layer are aligned, the resistance through the MTJ stack is low.

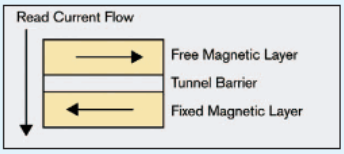

Fig. 3. When the polarities of the free layer and fixed layer are opposed, the resistance through the MTJ stack is high.

During the programming operation, the polarity of the free layer is set via copper interconnects running in perpendicular directions above and below the MTJ. A dose of current through the perpendicular interconnects creates a magnetic field that toggles the polarity of the free

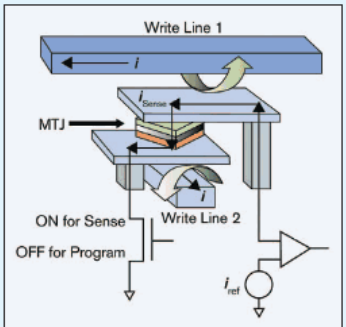

Fig. 4. Current through the perpendicular interconnects of the bit cell creates a magnetic field that toggles the polarity of the free layer.

Overview of Memory Technologies

Parameter	SRAM	DRAM	Flash	FRAM	MRAM
Read speed	Fastest	Fast	Fast	Fast	Fast
Write speed	Fastest	Fast	Slow	Medium	Fast
Cell density	Low	High	High	Medium	Medium/high
Nonvolatility	No	No	Yes	Yes	Yes
Endurance	Unlimited	Unlimited	Limited	Limited	Unlimited
Cell leakage	Low/high	High	Low	Low	Low

layer (see *Fig. 4*).

One major drawback that had to be overcome before productizing MRAM as a reliable memory was the single-line bit disturb rate of conventional MRAM. When the target bit is being programmed, the free layer in an untargeted bit could be programmed inadvertently by the field from a single write line.

Researchers have overcome this issue by creating a toggle bit cell that rotates the magnetic moment in the same direction each time the state of the bit is flipped. A staggered pulse of current on write line 1 and write line 2 rotates the polarity without disturbing bits along the same row or column as the target bit.

To further isolate untargeted bits from being disturbed, MRAM researchers have surrounded the copper interconnects with a layer of cladding on three sides of the copper. This cladding directs and focuses the strength of the magnetic field toward the target bit cell. This allows the target bits to be programmed using a much lower current and isolates neighboring bits from the magnetic field that would normally induce a disturb.

MRAM advantages

MRAM has many distinct advantages over other types of memories (see *Table 1*).

Flash technology uses a charge stored on a piece of floating polysilicon (floating gate) laid over a gate oxide. The programming of a flash bit cell requires a high-voltage field that accelerates electrons fast enough so that the electrons can overcome the energy barrier of the oxide between the silicon and the floating gate. This causes the electrons to punch through the oxide and charge the floating gate, which alters the threshold voltage of the bit cell transistor.

Repeated transfers of electrons through the oxide causes a gradual wear out of the oxide material so that the flash memory is limited to 10 K to 1 M write cycles before the bit is no longer functional. During programming, flash requires a high voltage to draw the electrons through the oxide material, while MRAM uses current to create a magnetic field to program the free layer. Flash also typically performs a program or erase operation on a large block of the memory array. MRAM can perform writes on individual addresses.

SRAM requires power to retain its memory contents, and as technology continues to shrink the cells the smaller geometry tends to leak more, increasing power dissipation. While MRAM takes a fair amount of supply current, it can be completely shut down when not in read/write operation.

Battery-backed SRAM has a built-in battery. The write-read speed of the MRAM is faster and elimination of the battery improves reliability and eliminates environmental issues associated with battery disposal.

An EEPROM (electrically erasable programmable read only memory) has much slower programming speeds as compared to MRAM with limited write cycling capability.

NVSRAM uses a combination of SRAM and EEPROM with a large external capacitor used to hold power on the device while the data transfer takes place during a power-down. However, this transfer of data to the EEPROM is very slow, and MRAM has the benefit of faster writes so that the data can be written during the normal operation of the system, while a minimum amount of data transfer is necessary during a power loss. And, MRAM does not need the large external capacitor.

Ferroelectric RAM (FRAM) is non-volatile, but typically the array sizes are small—4 Kbit to 1 Mbit. The array sizes are small because FRAM technology has limited scalability. MRAM does not run into the same limitations and can be programmed faster than FRAM. Some FRAMs have limited cycling capability of about 10 billion cycles and some FRAMs require a refresh of the memory after a read because the operation destroys the contents of the bit cell being read.

Dynamic RAM (DRAM) is volatile and requires frequent refresh of the memory for data retention.

MRAM applications

The next stage for MRAM will be its use in automotive applications. Automobile crash recorders using the MRAM will be able to gather and store more data during the course of an accident.

Many automotive applications use sensors that write data continuously to memory, as do odometers, tire pressure logs, and ABS systems. With frequent writes, you can easily exceed the write-erase capabilities of flash, so the unlimited write cycling capability of MRAM is a big advantage.

There are some interests in MRAM for use in military applications where many systems rely on battery-backed SRAM. MRAM is a more reliable alternative, and Honeywell has licensed the technology from Freescale Semiconductor for military and aerospace applications.

MRAM has the potential to replace the RAM + flash memories in embedded microcontrollers, being able to replace both with a single-memory architecture.

Once MRAM is capable of replacing computer system RAM and hard drives, we will be able to have systems that can boot up instantaneously and resume operation from where they left off. These exceptional features of MRAM can open up interesting market opportunities. ■