# Embedded Systems Architecture

Session #5

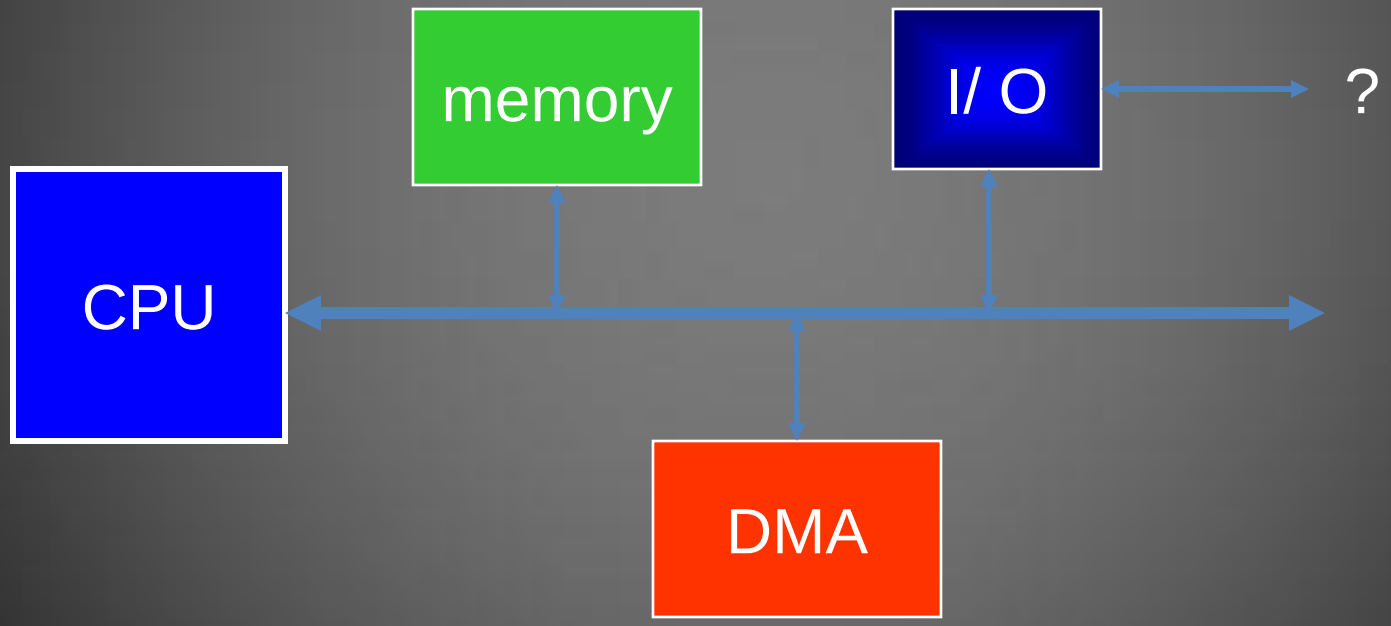
# The Embedded Computing Platform

- CPU Bus Structures
- Memory Devices
- Direct Memory Access (DMA)
- I/O Devices
- Designing with Microprocessors
- Development and Debugging
- Manufacturing Testing

# CPU Bus Structures

- Consist of a Data bus, an Address bus, Control signals, and Status signals.
- Control signals include READ, WRITE, CLOCK, Interrupts, et cetera.
- Status signals (if any) in READY, Data Acknowledge, Interrupt Acknowledge, et cetera.
- May be sole master or multi-master.

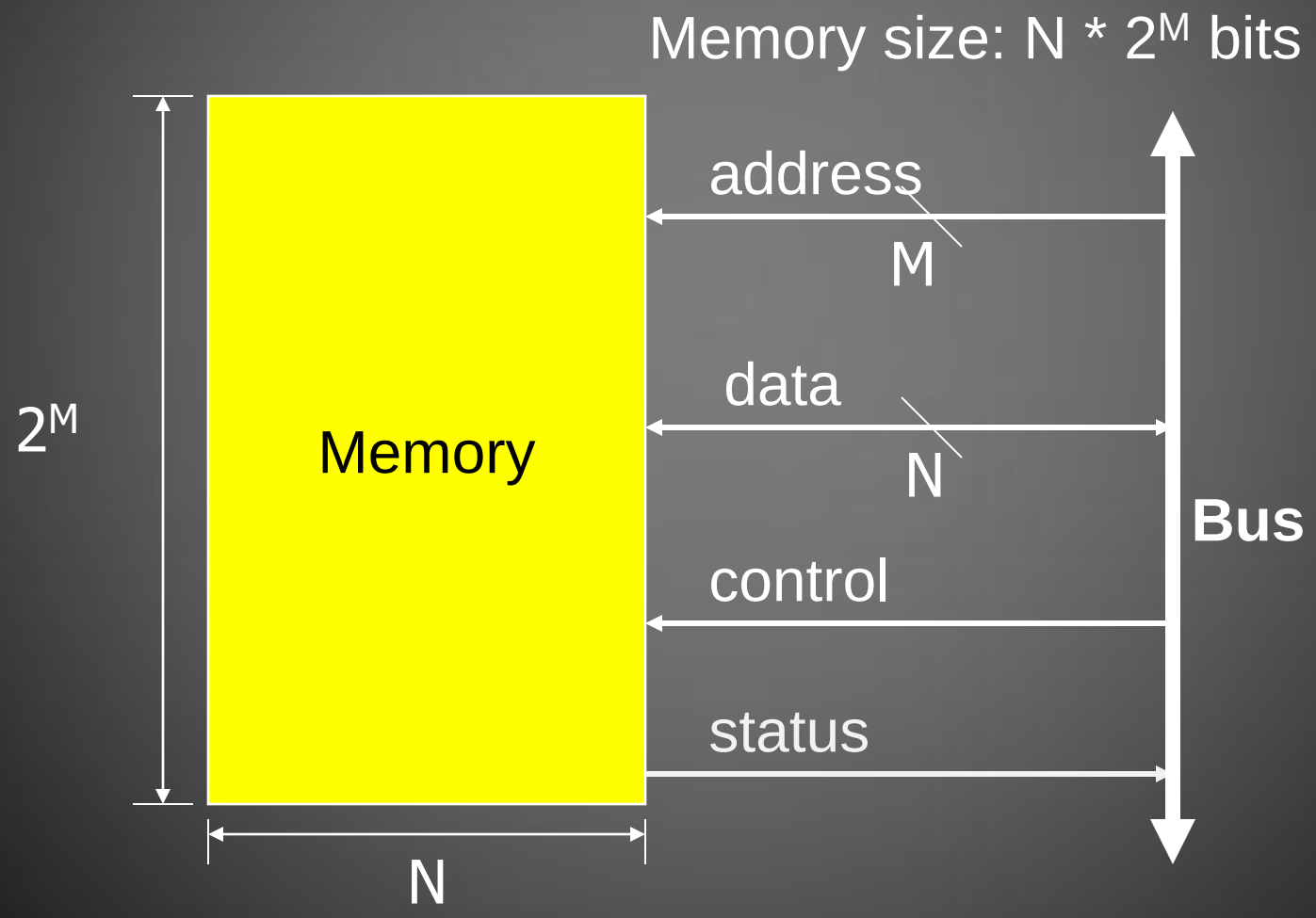
# CPU Bus Structure Example



# Memory Devices

- Organization
- Read-Only Memories (ROMs)
- Random-Access Memories (RAMS)

# Memory Device Organization



# Read-only memories (ROMs)

- Non-volatile
- Mask ROMS
- One-Time-Programmable (OTP) ROMs
- Erasable ROMs
- Flash memory

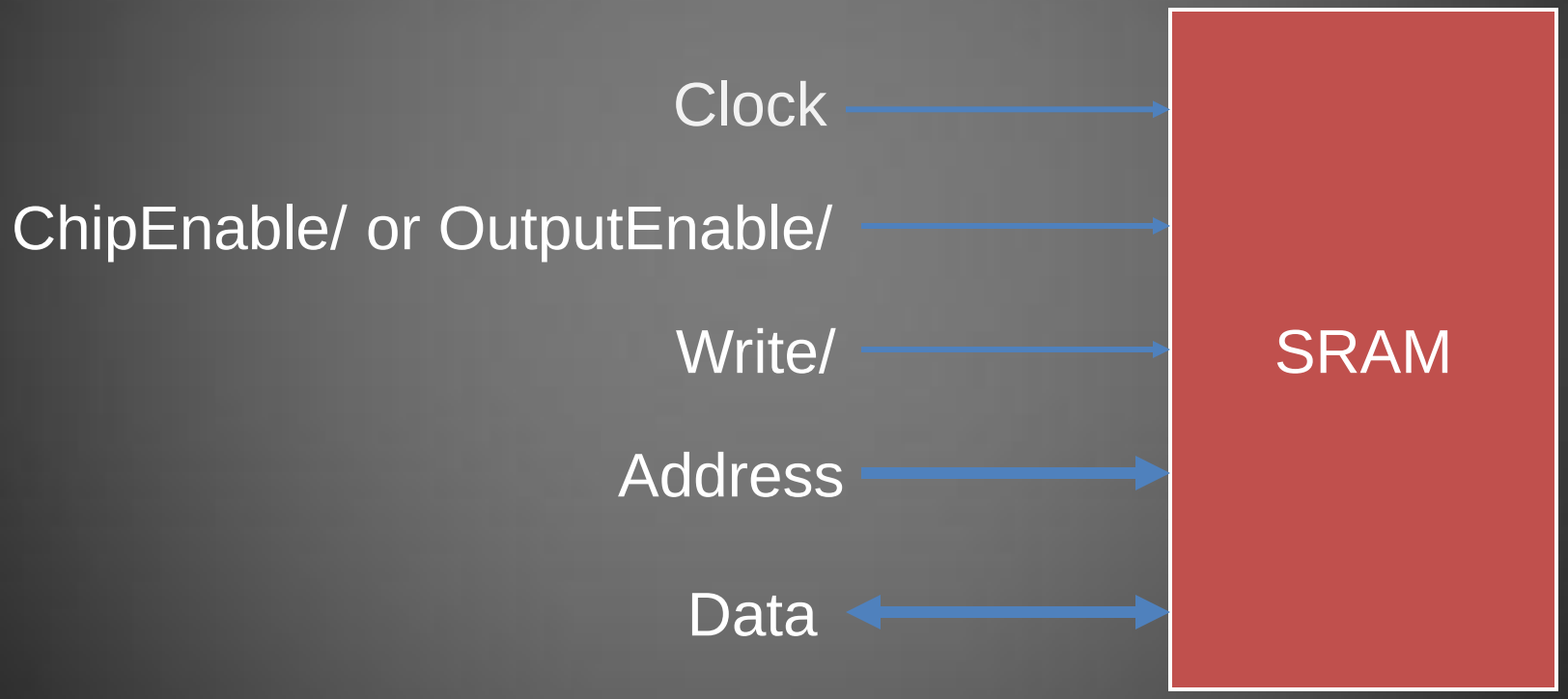
# Flash Memory

- Block erase and write.
- NAND
  - Greater endurance (1,000,000 cycles for NAND vs. 100,000 cycles for NOR).
  - Block read access.
  - Faster write.
- NOR
  - Random access read.

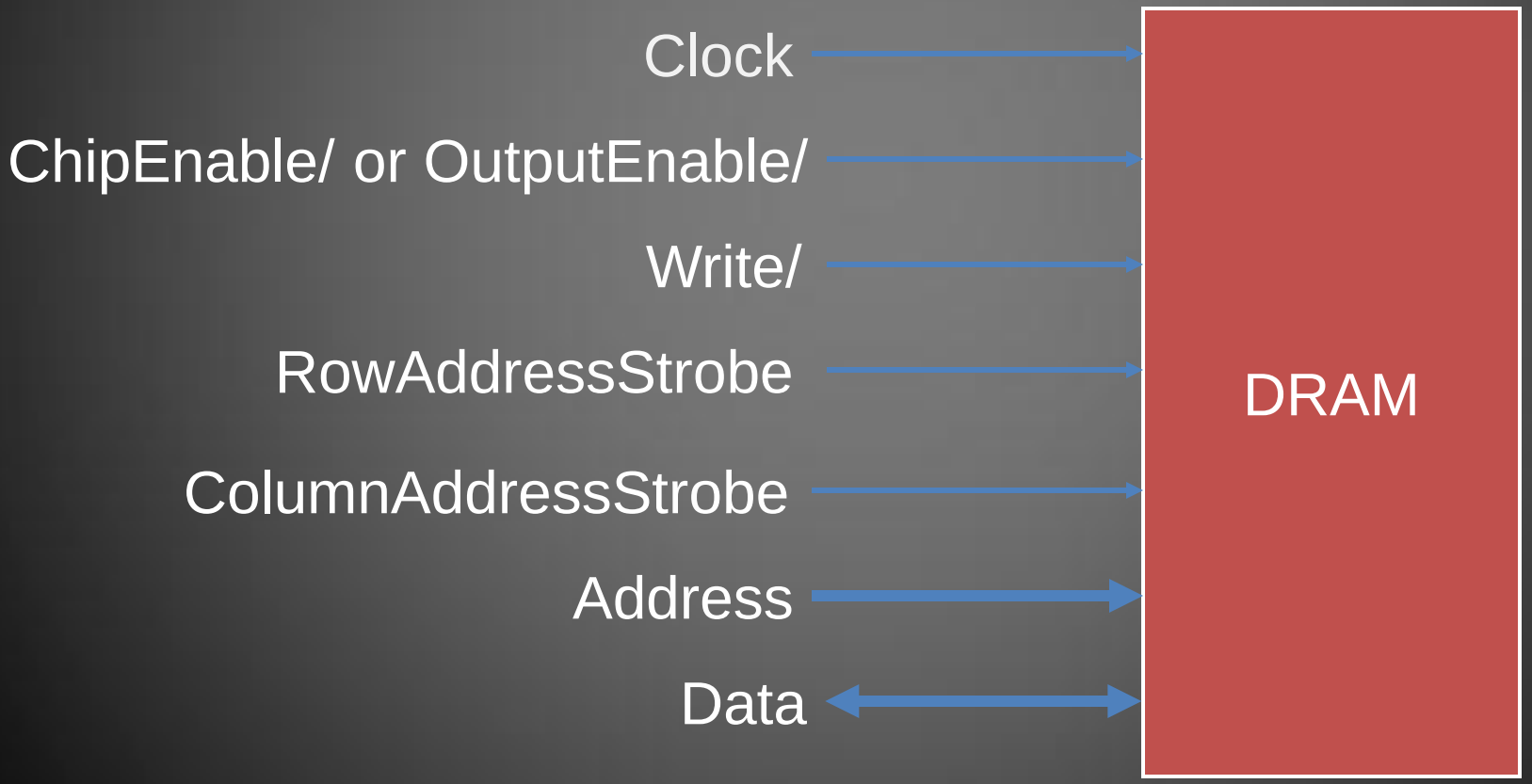
# Random access memories (RAMS)

- Volatile (typically)
- Static RAMs
  - Asynchronous
  - Synchronous Burst
- Dynamic RAMs
  - Asynchronous
  - Synchronous
  - Double Data Rate (DDR)

# Static RAMs (SRAMs)



# Dynamic RAMs (DRAMs)



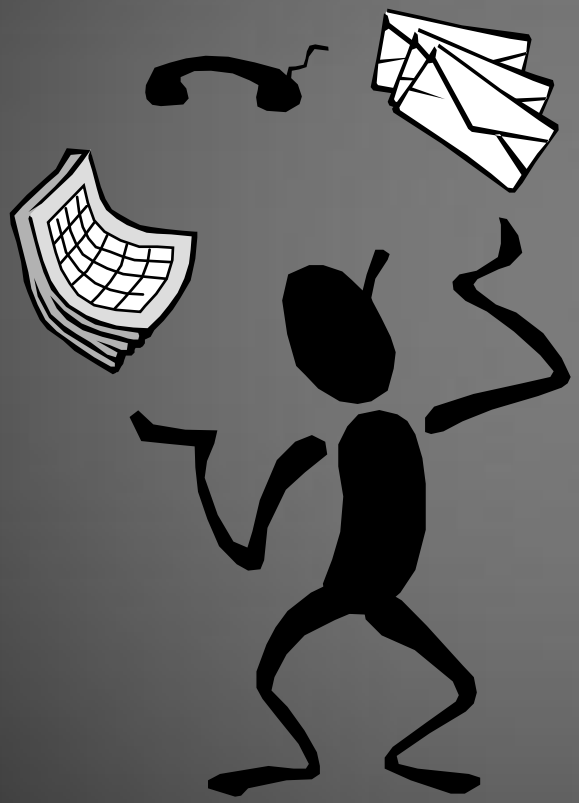
# Direct Memory Access (DMA)

- Temporary Bus master.
- Transfers data between or amongst I/O and memory.
- Must be initialized by CPU.
- Transfer can be initiated by CPU or I/O.
- Can interrupt CPU upon completion.

# I/O Devices

- Timers & Counters
- Communications
- Analog Interface
- Mechanical Interface
- Switches & Keyboards
- Displays

# Designing with Microprocessors



- In designing an embedded system architecture, we must *juggle* the requirements with different elements of hardware and software technology.

# Designing with Microprocessors

- System Architecture
  - Software Partition
  - Hardware Partition
- Platform issues
  - Processor choice
  - Bus choice:
    - ISA
    - Peripheral Component Interconnect (PCI)
    - PCI Express (PCIe)
    - VMEbus
    - PC/104

# Development

- Development Environments
  - Custom collection of development tools.
  - Integrated Development Environments (IDEs).
- Host and target
  - Same.
  - Same CPU but different target hardware.
  - Totally different from each other.

# Debugging

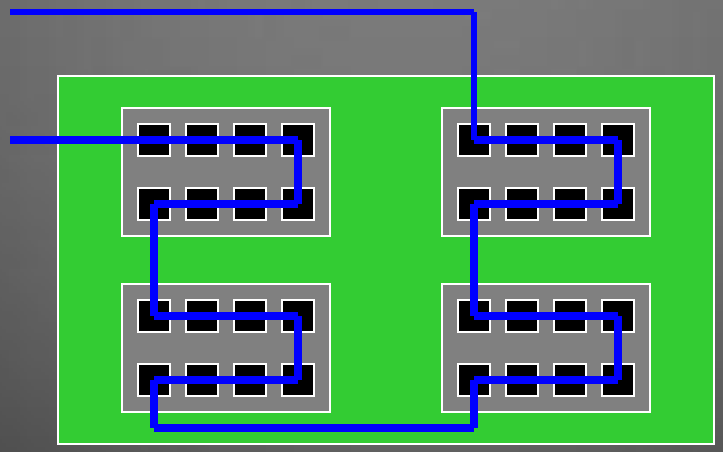
- Target contains own facilities.
  - Display & keyboard.
  - Non-volatile storage for diagnostic messages.
- Target contains hooks.
  - DAC ports for display of internal data.
  - JTAG port for ICE.
  - Logical analyzer connection port.
- Target is simulated.

# Manufacturing Testing

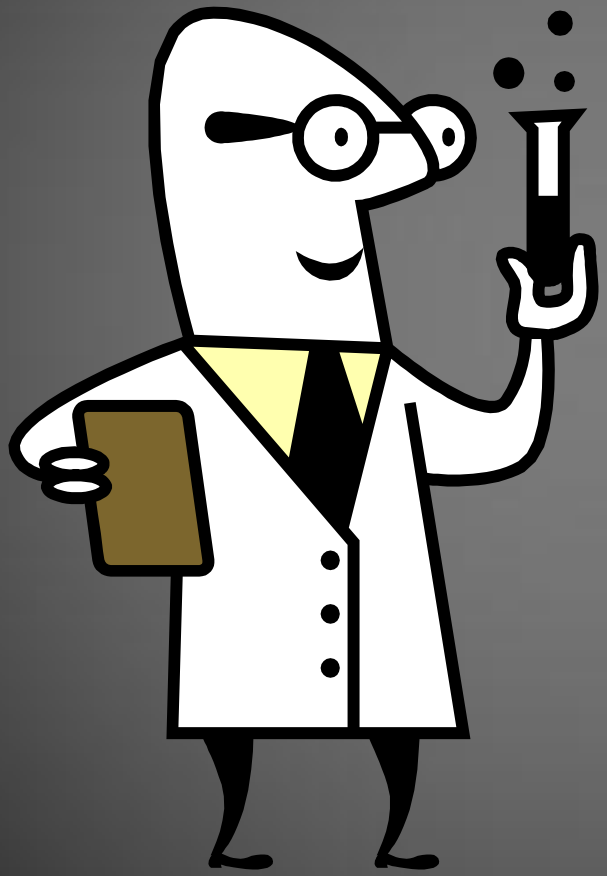
- Built-In-Test (BIT) facilities.
  - Self test software.
  - Sanity checking hardware.
- JTAG boundary scan.
- Anything that might be used for development debugging could also be used for manufacturing test.

# JTAG Boundary Scan

- Serial interface standard which allows for reading or controlling any pin within the scan chain.



# Lab Session #5



- *My Design Project Requirements Model*

# *My Design Project Requirements Model*