ARM Processor

Architecture

ARM architecture

- ARM stands for Advanced RISC Machines.
- ARM IP (Intellectual Property) cores and architectures developed and licensed by ARM Ltd.
- Both von Neumann (ARM7) and Harvard (ARM9) architectures.
- “2,500 ARM devices per second.”

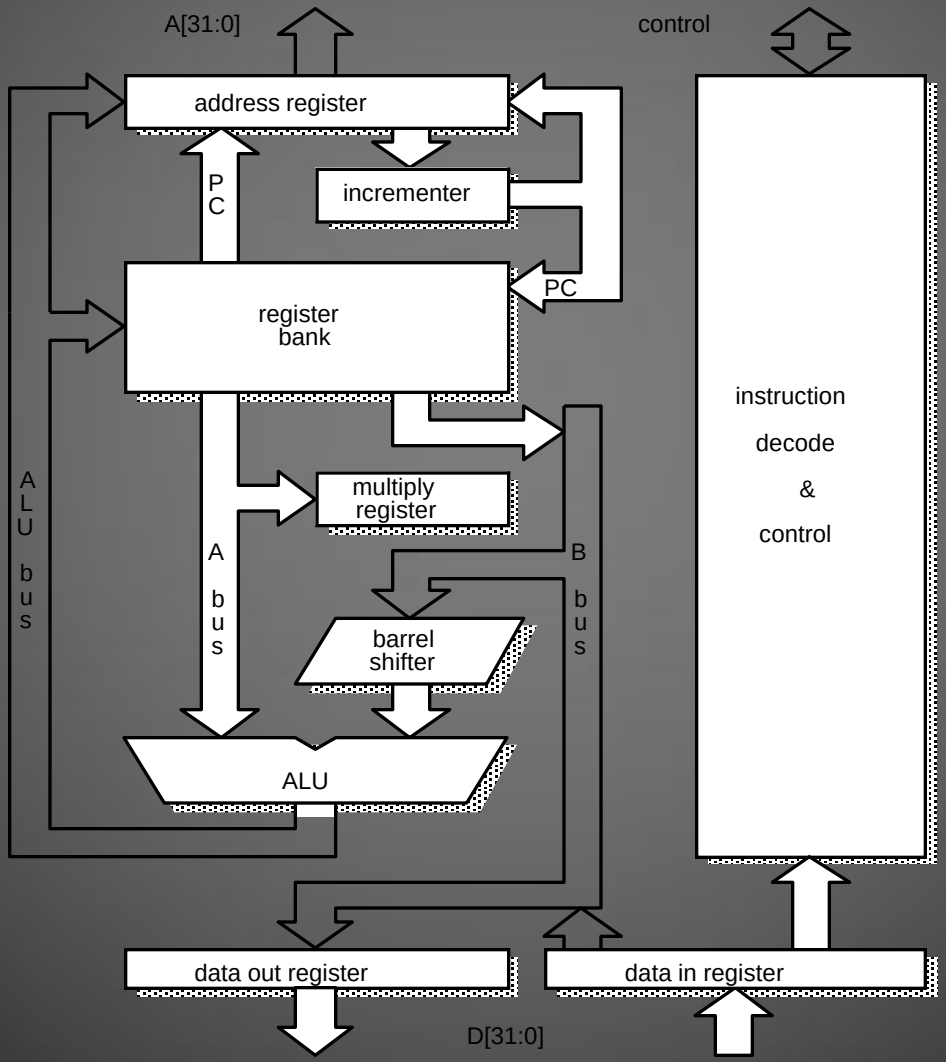
ARM7 Processor

- 32-bit fixed point RISC processor.
- von Neumann memory architecture.
- Three-stage instruction execution pipeline.
- ARM (32-bit) & Thumb (16-bit) instruction sets.
- Code is forward-compatible to ARM9, ARM9E and ARM10 processors.

ARM7 Processor (continued)

- Load-store memory operations.
- 32-bit word size.
- Address is 8-bit byte oriented.
- Endianess configurable at boot up.
- Each instruction can be conditionally executed.

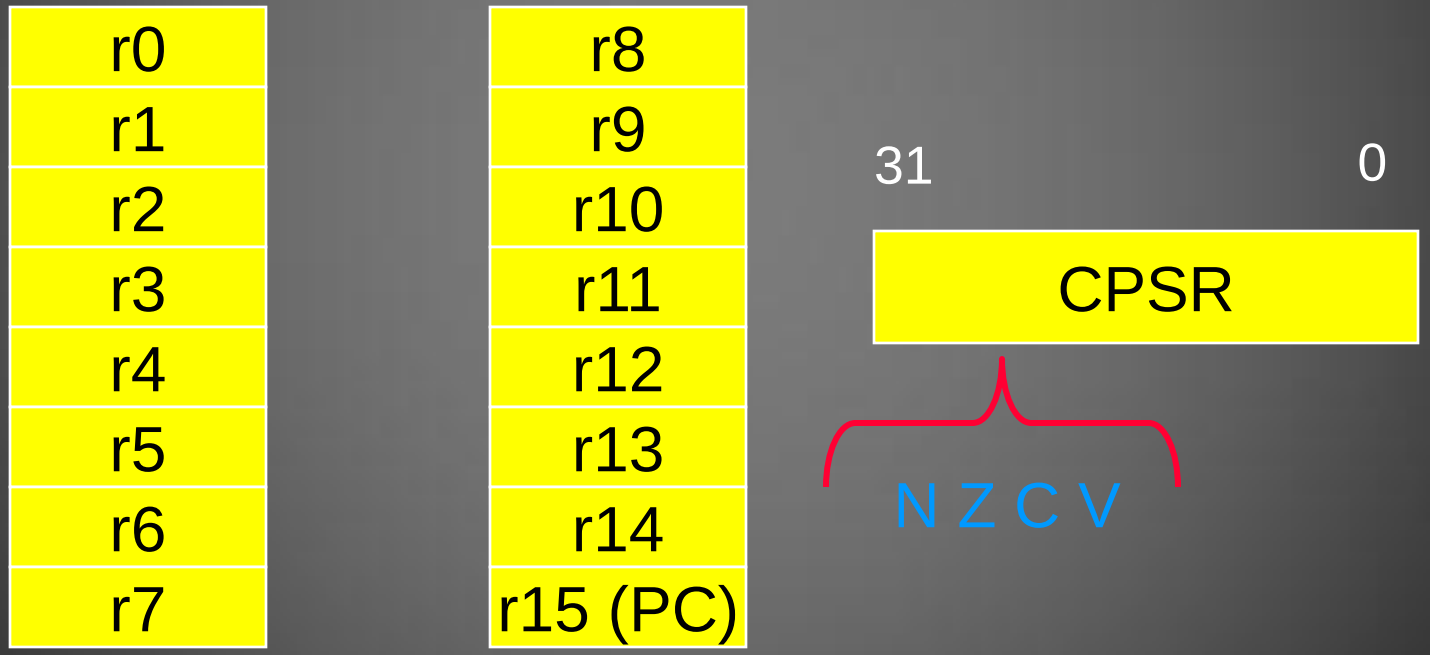
ARM7 Block Diagram



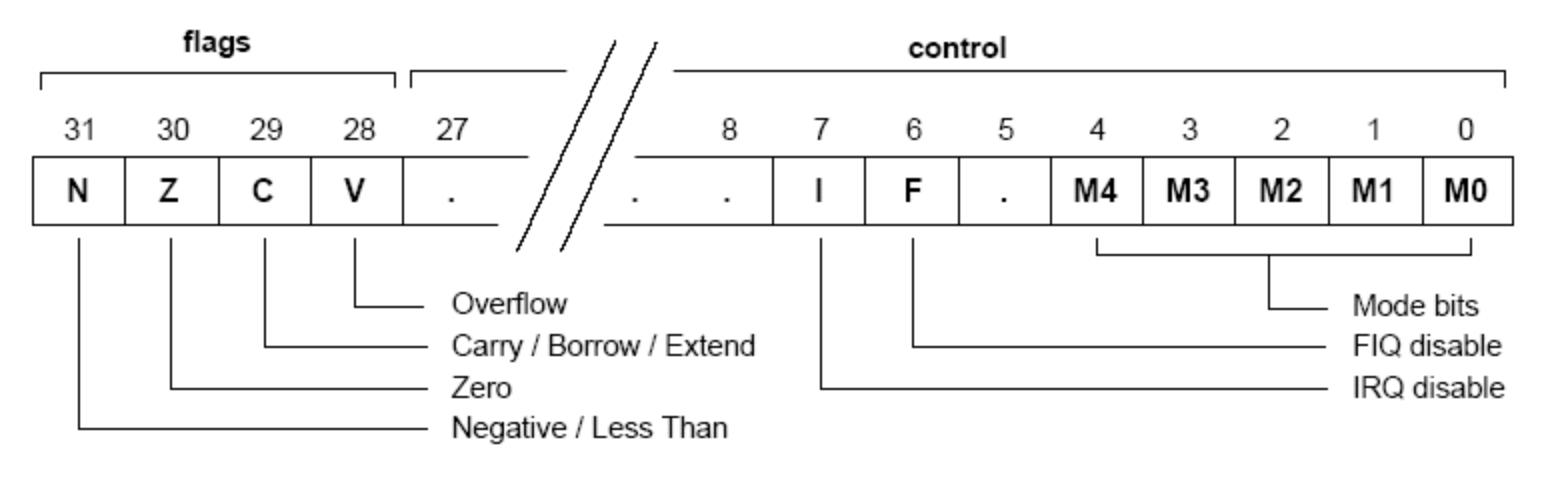
ARM7 Register Set

- 16 general purpose registers (r0 - r15).
- r15 is also the Program Counter (PC).
- r14 is used as the subroutine link register and receives a copy of r15 when a Branch and Link instruction is executed.
- Redundant register sets used for context switching between various modes.

ARM7 Register Set



ARM7 Current Program Status Register (CPSR)



ARM7 Current Program Status Register (CPSR)

- CPSR flag bits affected by arithmetic and logical instruction operations.
  - N-bit: set when result is negative or less than.
  - Z-bit: set when result is zero.
  - C-bit: set when there is a carry or borrow or extend.
  - V-bit: set when there is an overflow.

ARM7 Current Program Status Register (CPSR)

- The CPSR also contains mode bits and interrupt control bits.

M[4:0]	Mode	Accessible register set	
10000	User	PC, R14..R0	CPSR
10001	FIQ	PC, R14_fiq..R8_fiq, R7..R0	CPSR, SPSR_fiq
10010	IRQ	PC, R14_irq..R13_irq, R12..R0	CPSR, SPSR_irq
10011	Supervisor	PC, R14_svc..R13_svc, R12..R0	CPSR, SPSR_svc
10111	Abort	PC, R14_abt..R13_abt, R12..R0	CPSR, SPSR_abt
11011	Undefined	PC, R14_und..R13_und, R12..R0	CPSR, SPSR_und

ARM7 Addressing Modes

- Immediate
- Register direct
- Register indirect with pre or post increment or decrement or offset
- Auto indexing.