

## Answer1

a.  $CPI = 1 \times 50\% + 2 \times 20\% + 8 \times 20\% + 20 \times 10\% = 4.5$

b.  $MIPS = 50 \div 4.5 = 11.1$      $Time = \frac{4.5 \times 400000}{50 \times 10^6} = 3.6 \times 10^{-2}s$

c. easy to implement,  
the cycle time is associated to the longest instruction,  
signal asynchrony.

d.  $CPU_A \text{ instr count} = 25 \times 2 + 75 \times 1 = 125$   
 $CPU_B \text{ instr count} = 25 \times 2 + 50 \times 1 = 100$

### Case 1

$$\begin{array}{ll} CPU_A \text{ rate} = 1.5m & CPU_B \text{ rate} = m \\ CPU_A \text{ time} = \frac{125}{1.5m} & CPU_B \text{ time} = \frac{100}{m} \\ CPU_A \text{ is faster} \end{array}$$

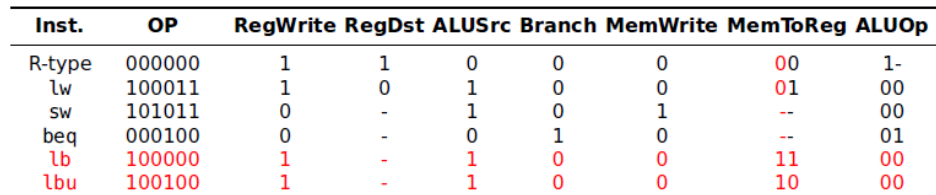
### Case 2

$$\begin{array}{ll} CPU_A \text{ rate} = 1.2m & CPU_B \text{ rate} = m \\ CPU_A \text{ time} = \frac{125}{1.2m} & CPU_B \text{ time} = \frac{100}{m} \\ CPU_B \text{ is faster} \end{array}$$

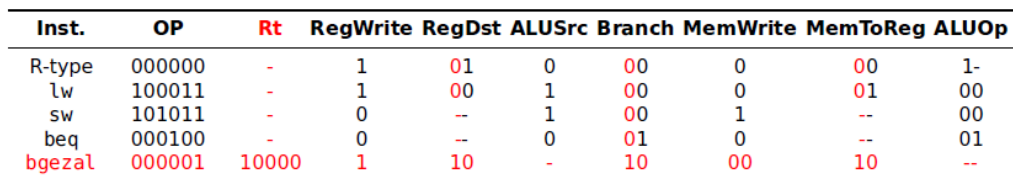
## Answer2

- a. No, because the value in r5 register hasn't been written back, thus leading to **data hazard**.
- b. Yes, because there are **two multiply units** thus avoiding structure hazard.
- c. It will cause **data hazard, control hazard**.
- d. Using hardware implemented with algorithm like **scoreboard** and **tomasulo**.  
Using **stall** and **forwarding** to avoid hazards.

a.



b.



### Answer4

a

- 1) **7**
- 2) **8**
- 3) No. The predicted PC can't be calculated until the fetch stage is finished for the jmp instruction.

**b**

[1]

```
icode:ifun←"M"_"1" [PC]
rA:rB←"M"_"1" [PC+1]
valC←"M"_"4" [PC+2]
valP←PC+6
```

[2]

```
valA ← R[rA]
valB ← R[rB]
```

[3]

```
valM ← "M" _ "4" [valE]
"M" _ "4" [valE] ← valA
```

[4]

**R[rA] ← valM**

C

[1] <b>M</b>	[2] <b>E</b>	[3] <b>E</b>	[4] <b>--</b>
[5] <b>done</b>	[6] <b>E</b>	[7] <b>W</b>	[8] <b>M</b>
[9] <b>11</b>	[10] <b>--</b>	[11] <b>0x44F</b>	
[12] <b>W</b>	[13] <b>D</b>	[14] <b>M</b>	
[15] <b>6</b>	[16] <b>0x44F</b>		

d

18

[illegible]