Extensible Homebrew Computer System Architecture Whitepaper

Detailed System Manual

2024. 1. 18.

Revision

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Before You Read This Document…

This document is detailed system manual of the homebrew computer powered by Motorola MC68030 Microprocessor. Its coverage is from low-level hardware structures and electrical characteristics to firmware operation calls to create your own bootloader and operating system or port existing applications or operating systems to this architecture.

Due to the educational purpose of this system architecture, you can freely create, modify, and delete any contents of it without almost every limitation. To read detailed information, see the license text inside of a box in the previous page.

Contacts

You can visit <https://github.com/kms1212/68k30-hbc> to create an issue to this repository.

Related Documents

More detailed informations of each components/standard used in this architecture may be needed to comprehend their operation, referencing documents in following table is recommended.

|  |  |
| --- | --- |
| Title | Contents |
| MC68030 User’s Manual | Detailed description of MC68030 Microprocessor |
| MC68882 User’s Manual | Detailed description of MC68882 Floating-point coprocessor |
| FLEX® 6000 PLD Family Datasheet | Electrical characteristics, device architecture, timing parameters, etc. of Altera® FLEX® 6000 FPGA Family |
| MAX® 7000 PLD Family Datasheet | Electrical characteristics, device architecture, ISP programming methods, timing parameters, etc. of Altera® MAX® 7000 CPLD Family |
| Altera® Configuration Handbook | Configuration methods for Altera® FPGA Families. |
| JEDEC Standard No.21-C Page 4.4.2 | Description of JEDEC 72-pin SIMM Memory module standard. |
| 030HBC Software Development Supplement Manual | Considerations and detailed information regarding software (Bootloader/OS/Application) development (TBD) |
| 030HBC System Bus Controller Operation Datasheet | Detailed description of operation principle of the SBC implemented on FPGA (TBD) |
| 030HBC Cached DRAM Controller Operation Datasheet | Detailed description of operation principle of the CDC implemented on FPGA (TBD) |
| TBD |  |

Most of these documents will be archived into a single site soon.

Note that this list of related documents can be updated without noticing.

Notational Conventions

The following tables of notational conventions affects all descriptions throughout this document.

|  |  |
| --- | --- |
| Term / Convention | Description |
| *Arithmetic Operations* (such as “+”, “−“, “×”, “÷”) | Every arithmetic operation must be spaced with single whitespace to left and right. |
| *Logical Operations* (such as “|”, “&”, “!”, “**xor**”) | Similar to above. In addition, every multi-character operation such as “**xor**” and “**nand**” must be bold-faced and can be either uppercase or lowercase. |
| *Enumeration Signs* (such as “,”) | A sign has to be placed right after a previous content (no whitespaces are allowed), and trailing single whitespace must be added. |
| *Braces and square brackets* | A single whitespace must be added to each leading and trailing side of the content(s) inside. |
| 0x*value* | Hexadecimal value. Every Alphabetical representation above decimal range (from A to F) can be either uppercase or lowercase.  Any characters except from 0 to 9, from a to f, and from A to F are not allowed. |
| 0b*value* | Binary value. Any characters except 0 and 1 are not allowed. |
| “*value*” | String value. Represents the value inside double quotes. |
| [ item1, item2, item3, … ] | Array value. Represents the array of the values inside square brackets enumerated by “,”. |
| { *address* } | Address value. A binary, decimal, or hexadecimal values are allowed inside braces. |
| *value*(*bit*) | A value of data where the *bit*th position of *value* counted from LSB. Multiple bits are selectable to specify the range using the term described below. |
| <*start*:*end*> | Represents the range of the position of bits. The ordering of bits is counted from LSB to LSB. |
| { *value1* | *value2* | *…* } | Enumeration value. One of these values enumerated by “|” can be selected. |
| #{ *address* } | Referenced value. Represents the value referenced by the given address. |
| Boldface Text | Indicates that the text is critical to the contents of the context. It also indicates that the text is locally defined vocabulary. |
| Italic Text | Indicates that the text can be replaced into corresponding value. Simply, it is a placeholder. |
| Boldface Italic Text | A reference to a chapter, section, table or image. |
| Monospaced Text | Indicates that the text is code example, filename, file path, or any value that needs to be aligned by monospaced font. |
| Boldface Monospaced Text | Similar as above, but the role of boldface text is added. |
| → | Represents a flow of the data. The left side can be a data and the right side can be an address or a register. |
| ⇒ | Represents a transition and modification of the data. |
|  |  |
|  |  |
|  |  |
|  |  |

Notes and Warnings

Warning

Contents described inside this box are warnings about the factors which can cause misoperation of the system.

Note

Contents described inside this box can be an useful trick and shortcut to utilize this documentation.

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# Overview

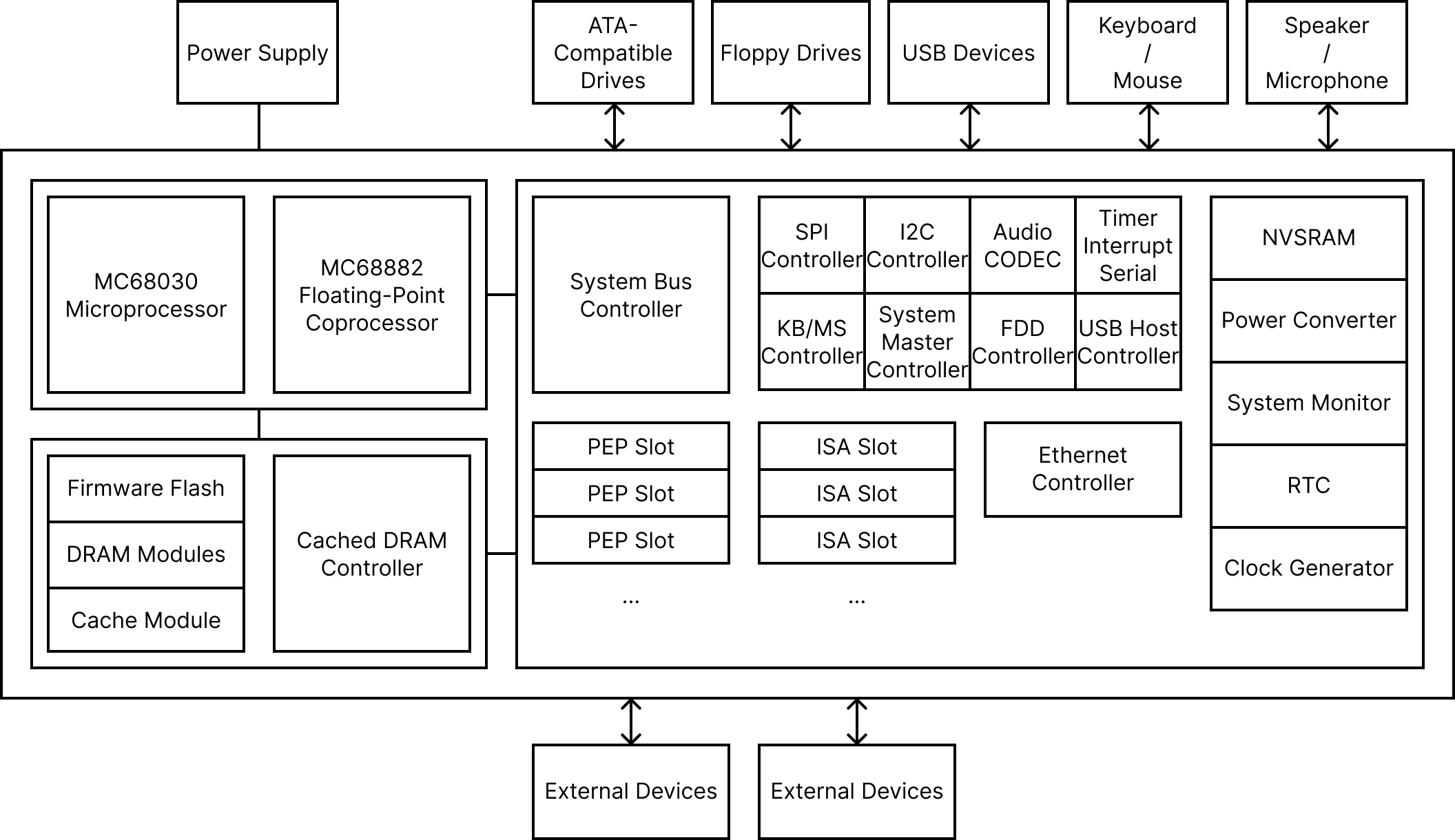


Figure 1 System Block Diagram

Contents in this chapter roughly explains about the entire architecture of the `030 Extensible Homebrew Computer. The architecture of this system is designed to provide flexible operations, rich system functions, and large expansion capabilities.

## Features

The features and characteristics of the `030 Extensible Homebrew Computer (hereafter ‘030EHBC’) are listed as follows:

* Powered by a Motorola MC68030 microprocessor and a MC68882 coprocessor
  + 32-bit microprocessor up to 50 MHz of operation clock
  + Integrated 256-byte data cache and 256-byte instruction cache
  + Paged Memory-Management Unit (MMU) integrated for memory protection
  + 7 levels of interrupt autovector
  + A MC68882 floating-point coprocessor which accelerates real-number arithmetic is installable
* Configurable processor frequency up to 50MHz and two fixed clocks at 24MHz and at 14.61818MHz
* Four 72-pin SIMMs for DRAM capacity up to 64MiB
* Cache support with the SRAM capacity up to 4MiB of data space and 512kiB of tag space.
* The Cached DRAM Controller and the System Bus Controller implemented on FPGA:
  + The Cached DRAM Controller, CDC is a DRAM controller with a cache support. It also works as a 8-channel DMA controller.
  + The System Bus Controller, SBC is a multifunctional bus controller which supports PEP, ISA, OPB, and  
    PATA.
* Synchronous local bus transfer support by system controllers (CDC and SBC) in order to achieve fast operation cycles
* 8 DMA channels with detailed signal customizations
* Full support of IRQ signals driven by ISA bus devices
* 4 programmable timers
* Rich capabilities of peripheral buses and external devices:
  + Peripheral Expansion Port, PEP: 32-bit high-speed bus with multiplexed address and data
  + Industry Standard Architecture, ISA: 8-bit or 16-bit ISA bus for IBM PC compatibility
  + On-board Peripheral Bus, OPB: Simple 8-bit or 16-bit bus for integrated system peripherals
  + Parallel AT-Attachment, PATA: ACS-4 compatible 16-bit bus for storage devices
  + Inter-Integrated Circuit, I2C (IIC): Serial bus for system management and device recognization
  + Serial Peripheral Interface, SPI: Serial bus for NVSRAM connection
  + 1 floppy drive interface
  + 1 USB host interface
  + PS/2 keyboard and mouse interface
  + 1 RS232 serial port
  + 1 10Base-T 10Mbps ethernet port
  + Speaker/Microphone/Line-in audio jack
* 5 expansion bus device connectors:
  + 3 sets of DIN-41612 3x32 and 3x10 connector for each PEP device
  + 2 sets of a 36-pin and 62-pin card-edge socket for each ISA device
* Real-time clock and NVSRAM
* Coin cell battery backup for a RTC and a NVSRAM
* Two 4MiB flash memories storing firmware code and data
* A dual-channel step-down buck converter providing adjustable voltage supplies to processors and system controllers.
* A power monitor supervising voltage and current of each power supply rails
* A System Master Controller implemented on ATMega32 controls switches, a buzzer, reset signals, etc.
* A 24-pin ATX power supply connector for power inputs

## System Performance

Default

Bold

Italic

Bold Italic

Monospaced

Bold Monospaced

|  |  |
| --- | --- |
| Field | Description |
| Data | Data |
| Data | Data |
| Data | Data |
| Data | Data |

Table 1‑1 Descriptor Table

|  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| Offset | 0 | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 | A | B | C | D | E | F |
| 0000h |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| 0010h |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| 0020h |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| 0030h |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| 0040h |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| 0050h |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| 0060h |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |

Table 1‑2 Hex Space Table

Code

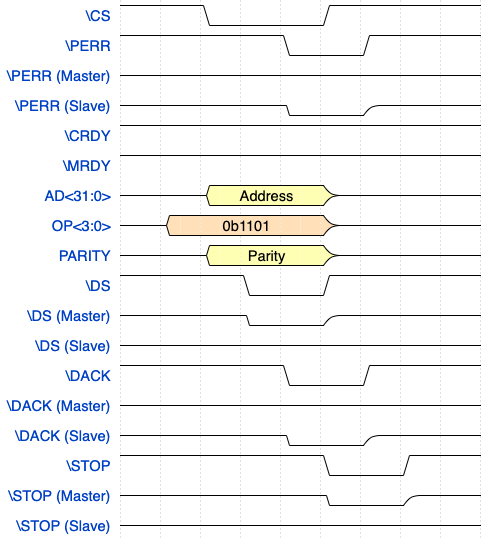


Figure 1‑2 Image Fil

Footnote[[1]](#footnote-1)

* Item1
* Item2
* Item3
* Item4
* Item5
* Item6
* Item7
* Item8
* Item9
* Item10
  + Subitem1
  + Subitem2
  + Subitem3

Note

Note Content

1. Item1
2. Item2
3. Item3
4. Item4
5. Item5
6. Item6
7. Item7
   1. Subitem1
   2. Subitem2
   3. Subitem3

Warning

Warning Content

System Block Diagram

# Processor & Coprocessor

## The Main Processor

## The Coprocessor

# Memory Subsystem

## Types of System Memories

|  |  |  |
| --- | --- | --- |
| Type | Form | Description |
| DRAM | 72-pin SIMM | Primary memory of this system. The DRAM address space is linearly accessible from the bottom of the memory map of the processor local bus when the CDC has been configured correctly after finishing its initialization process. |
| Cache | 80-pin SIMM | It is level-2 cache memory between integrated level-1 cache and DRAM. This space of memory is not accessible via dedicated address space but an access to the DRAM space. |
| NVSRAM | 1x IC | This space of memory is accessible via SPI bus. Contents in this space are non-volatile, unless the battery backup is unavailable for some reason. |
| Flash | 2x IC | The non-volatile memory space for storing firmware binaries. It is only accessible at the supervisor address space. After the initialization process of the CDC, this memory space is allocated at the bottom of the address space of the processor local bus. This space can be hidden by modifying the value of the corresponding register of CDC. |

## Processor Local Bus Memory Map

### Memory Map of the Supervisor Address Space

|  |  |  |
| --- | --- | --- |
| Base | Size | Description |
| 0xFF000000 | 16MiB | Used or Reserved MMIO Space |
| 0x???00000 |  | Unavailable Area |
| 0x00100000 | *DRAM Size* – 1MiB | DRAM Space After the First 1MiB Space |
| 0x00000000 | 1MiB | Firmware Flash Memory Space or DRAM Space |

### Memory Map of the User Address Space

|  |  |  |
| --- | --- | --- |
| Base | Size | Description |
| 0x00000000 | *DRAM Size* | DRAM Space |

## Dynamic RAM Modules

## Cache SRAM Module

## Memory-Mapped I/O

## Direct Memory Access

# System Controllers

# System Bus

## Local Bus

## PEP Bus

## ISA Bus

## OPB

## ATA Bus

# Peripheral Expansion Port

This chapter illustrates the detailed description of PEP(Peripheral Expansion Port) bus which includes the electrical characteristics, connector pinout, port wiring diagram, signal protocol, etc. The PEP is a 32-bit wide bidirectional half-duplex parallel bus which enables the interconnection between a dedicated bus controller and expansion cards in order to extend the system capability of the 030EHBC.

Due to the simplicity of signal protocol of the PEP bus, it is easy to implement and debug the operation of the port. And the synchronous operation of the protocol and the high-speed bus synchronization clock can increase the overall system performance.

## Overview

The function summary of the PEP is defined as follows:

* 32-bit width multiplexed address/data bus
* Synchronized bus operations
* High-speed 24MHz bus synchronization clock
* Flexible wait-state insertion up to (TBD) cycles from the device
* Addressed and unaddressed operation support with or without sequential multi-word I/O
* Dedicated nEN(active low) signal per device which indicates that the device is selected
* Binary-encoded operation selection signals which selects the actual operation of each data transaction cycle
* Dedicated device configuration bus cycle
* Additional (but mandatory) I2C bus directly connected to I2C EEPROM storing the device information

## Electrical Characteristics

### Operating Conditions

|  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- |
| Symbol | Description | Min | Typical | Max | Units |
| +12V | +12V supply voltage relative to **GND** | 11.5 | 12 | 12.5 | V |
| +5V | +5V supply voltage relative to **GND** |  | 5 |  | V |
| +3.3V | +3.3V supply voltage relative to **GND** |  | 3.3 |  | V |
| +5VSB | +5V standby supply voltage relative to **GND** |  | 5 |  | V |
| -5V | -5V optional supply voltage relative to **GND** |  | -5 |  | V |
| -12V | -12V supply voltage relative to **GND** |  | -12 |  | V |

### DC Characteristics

|  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- |
| Symbol | Description | Min | Typical | Max | Units |
| VML | Low-level Voltage of Bus Master Output | 0 |  | 0.8 | V |
| VMH | High-level Voltage of Bus Master Output | 2 | +5V | **+5V** + 0.2 | V |
| VDL | Low-level Voltage of Bus Device Output | 0 |  | 0.8 | V |
| VDH | High-level Voltage of Bus Device Output | 2 |  | +5V | V |

## Signal descriptions and Pinouts

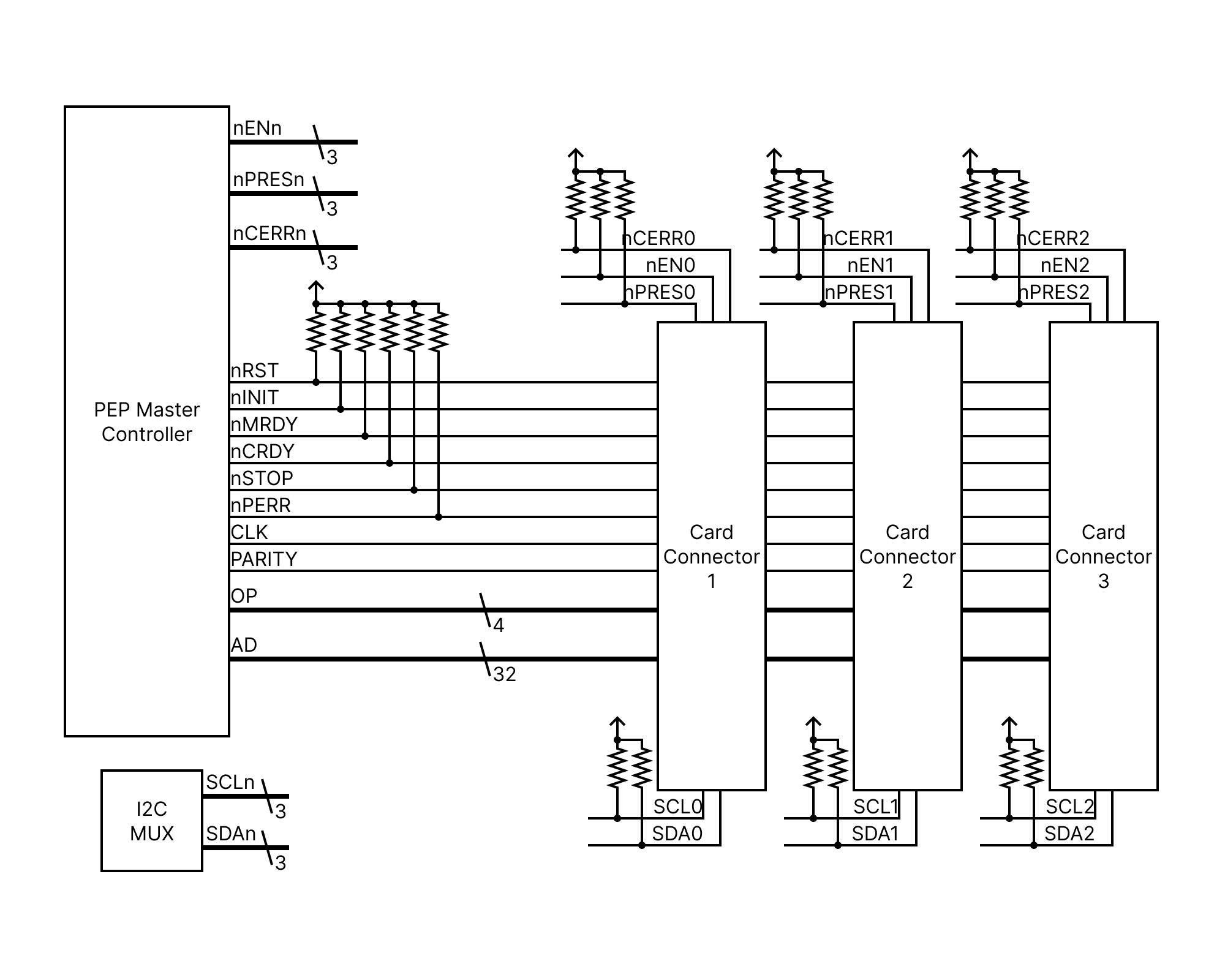
|  |  |  |  |
| --- | --- | --- | --- |
| Row | Col. A | Col. B | Col. C |
| 1 | GND | GND | GND |
| 2 | +12V | +12V | +12V |
| 3 | +12V | +12V | +12V |
| 4 | +5VSB | -12V | -5V |
| 5 | +5V | GND | +5V |
| 6 | +5V | nPRES | +5V |
| 7 | +5V | +5V | +5V |
| 8 | +3.3V | +3.3V | +3.3V |
| 9 | +3.3V | +3.3V | +3.3V |
| 10 | GND | GND | GND |

|  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- |
| Row | Col. A | Col. B | Col. C | Row | Col. A | Col. B | Col. C |
| 1 | GND | GND | GND | 17 | AD28 | GND | AD29 |
| 2 | nPRES | GND | nEN | 18 | AD26 | GND | AD27 |
| 3 | CLK | GND | nRST | 19 | AD24 | GND | AD25 |
| 4 | N/C | GND | SCL | 20 | AD22 | GND | AD23 |
| 5 | N/C | GND | SDA | 21 | AD20 | GND | AD21 |
| 6 | N/C | GND | N/C | 22 | AD18 | GND | AD19 |
| 7 | N/C | GND | N/C | 23 | AD16 | GND | AD17 |
| 8 | N/C | GND | N/C | 24 | AD14 | GND | AD15 |
| 9 | N/C | GND | N/C | 25 | AD12 | GND | AD13 |
| 10 | nMRDY | GND | nIRQ | 26 | AD10 | GND | AD11 |
| 11 | nCRDY | GND | nCERR | 27 | AD8 | GND | AD9 |
| 12 | OP3 | GND | nPERR | 28 | AD6 | GND | AD7 |
| 13 | OP2 | GND | nSTOP | 29 | AD4 | GND | AD5 |
| 14 | OP1 | GND | nINIT | 30 | AD2 | GND | AD3 |
| 15 | OP0 | GND | PARITY | 31 | AD0 | GND | AD1 |
| 16 | AD30 | GND | AD31 | 32 | GND | GND | GND |

|  |  |
| --- | --- |
| Signal Type | Description |
| T/S | Bidirectional tri-state signal |
| O/D | Open-drain signal (a pull-up resistor is required) |
| Reserved | Reserved pin. Do not connect to any other power or signal traces. |

|  |  |  |  |
| --- | --- | --- | --- |
| Signal | Description | I/O | Type |
| CLK | 24MHz bus synchronization clock. Every PEP signals except nRST, nPRES, nINIT, nIRQ, and signals for the I2C bus are sampled on the rising and failing edge of this signal. | I |  |
| nEN | Indicates that the device is selected and OP<3:0> signals are valid. | I |  |
| nRST | Reset signal for the device. The device is not available in any condition when this signal is asserted. | I | O/D |
| nPRES | Device presence signals. One is in the **PDAT** connector and the other is in the **PPWR** connector. One or more of these signals should be tied directly into GND to indicate that the device is present. | O | O/D |
| nINIT | Indicates that one or more PEP device is on the initialization sequence. | O | O/D |
| SCL | Serial clock signal for the additional I2C bus. **SCL** and **SDA** are not affected by the level of any other signals. | I | O/D |
| SDA | Serial data signal for the additional I2C bus. **SCL** and **SDA** are not affected by the level of any other signals. | I/O | O/D |
| nMRDY | Indicates that the PEP master controller ready for the transaction of data. This signal is driven high when the controller is on the initialization sequence or busy. | I |  |
| nCRDY | Indicates that the PEP device is ready for the transaction of data. Wait states are inserted by driving it low. This signal does not affect the availability of the I2C bus. | O | O/D |
| OP<3:0> | Signals for recognizing data transaction operation type at the beginning of the transaction. After one clock, **OP<3:0>** indicate the size of the transaction and the direction of the **AD<31:0>**. | I |  |
| nSTOP | Transaction termination request signal from device. | O | O/D |
| AD<31:0> | Multiplexed address/data signals. These signals contain a 32-bit address during address transaction cycle(s), or contain variable bytes of data during data transaction cycle(s). | I/O | T/S |
| PARITY | Even parity bit across AD<31:0> and OP<3:0>. **nPERR** signal is asserted at next falling edge of the **CLK** when this signal is invalid. | I/O | T/S |
| nIRQ | Optional interrupt request signal. Driving it low initiates the interrupt acknowledge routine. This signal is negated when the routine is finished. | O | O/D |
| nPERR | Indicates that the **PARITY** signal is invalid and the current transaction should be retried or terminated. | O | O/D |
| nCERR | Optional device error indicator signal. When this signal is asserted, the system can initiate error correction routine, reset, or disable corresponding device. | O | O/D |
| N/C | Not used currently and reserved for future use. Do not connect to any signal or power supply rail. | - | Reserved |

## Example Signal Connection Block Diagram



# On-board Peripheral Bus

# Onboard Peripherals

# Bootstrap Firmware

# Mass Storage Interfaces

# Power Supply

# System Initialization

# Debugging Interfaces

###### Brief Description of Cached DRAM Controller

* 1. Appendix Heading 2
     1. Appendix Heading 3

Appendix Heading 4

###### Brief Description of System Bus Controller

1. Footnote content [↑](#footnote-ref-1)