East West University

Course title: Digital Logic Design
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Section: 4

Mini project

Metrorail fare counting

Submitted To:

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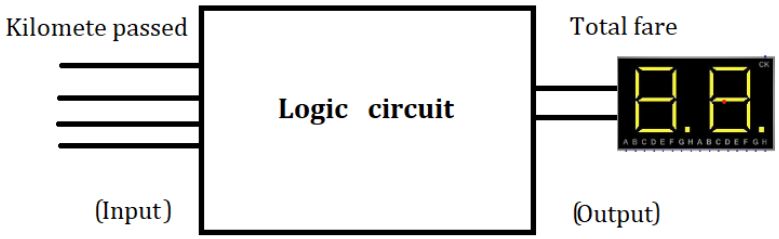
Project Name: Metrorail fare counting

Description:

Our project is of Metrorail fare counting. Where, we are estimating the fare of passengers by the length of their travelling in the Metrorail in kilometers. We are counting it in a simple manner just to show the implementation. We fixed 1 Km for 5Tk. We are doing it for 1 to 15 kilometers. Because we have the input of 4bits(A,B,C,D). We have shown this using the seven segment display so that we can get a decimal result to understand the output quickly.



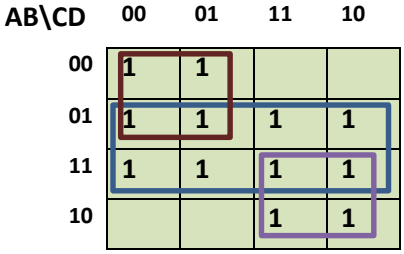
Calculations:

Length (Km)	Fare per Kilometer(TK)	Total fare (TK)
1	5	5
2	5	10
3	5	15
4	5	20
5	5	25
6	5	30
7	5	35
8	5	40
9	5	45
10	5	50
11	5	55
12	5	60
13	5	65
14	5	70
15	5	75

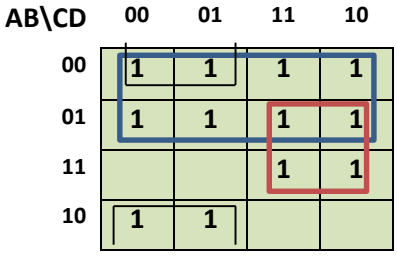
Truth table:

Input				Output													
A	B	C	D	a1	b1	c1	d1	e1	f1	g1	a2	b2	c2	d2	e2	f2	g2	TK
0	0	0	0	1	1	1	1	1	1	0	1	1	1	1	1	1	0	0
0	0	0	1	1	1	1	1	1	1	0	1	0	1	1	0	1	1	5
0	0	1	0	0	1	1	0	0	0	0	1	1	1	1	1	1	0	10
0	0	1	1	0	1	1	0	0	0	0	1	0	1	1	0	1	1	15
0	1	0	0	1	1	0	1	1	0	1	1	1	1	1	1	1	0	20
0	1	0	1	1	1	0	1	1	0	1	1	0	1	1	0	1	1	25
0	1	1	0	1	1	1	1	0	0	1	1	1	1	1	1	1	0	30
0	1	1	1	1	1	1	1	0	0	1	1	0	1	1	0	1	1	35
1	0	0	0	0	1	1	0	0	1	1	1	1	1	1	1	1	0	40
1	0	0	1	0	1	1	0	0	1	1	1	0	1	1	0	1	1	45
1	0	1	0	1	0	1	1	0	1	1	1	1	1	1	1	1	0	50
1	0	1	1	1	0	1	1	0	1	1	1	0	1	1	0	1	1	55
1	1	0	0	1	0	1	1	1	1	1	1	1	1	1	1	1	1	60
1	1	0	1	1	0	1	1	1	1	1	1	0	1	1	0	1	1	65
1	1	1	0	1	1	1	0	0	0	0	1	1	1	1	1	1	0	70
1	1	1	1	1	1	1	0	0	0	0	1	0	1	1	0	1	1	75

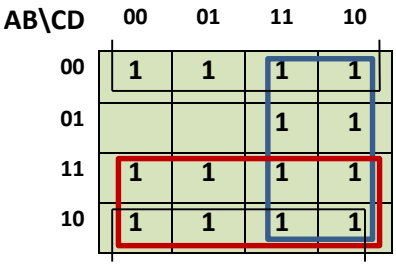
K maps:



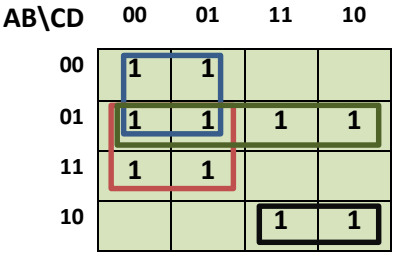
a1 = B + A'C' + AC



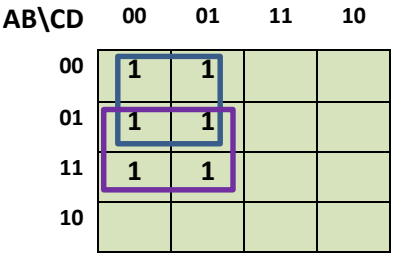
b1 = A' + B'C' +BC



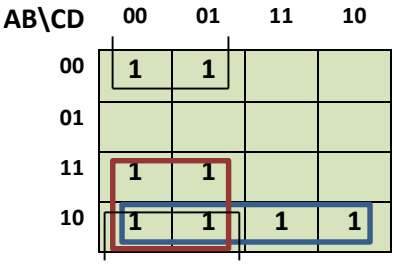
c1 = C + A + B'



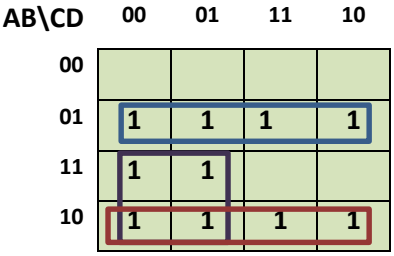
d1 = A'B + A'C' + BC' + AB'C



e1 = A'C' + BC'



f1 = AB' + AC' + B'C'



g1 = A'B + AB' +AC'

AB\CD	00	01	11	10
00	1	1	1	1
01	1	1	1	1
11	1	1	1	1
10	1	1	1	1

a2=c2=d2=f2=1

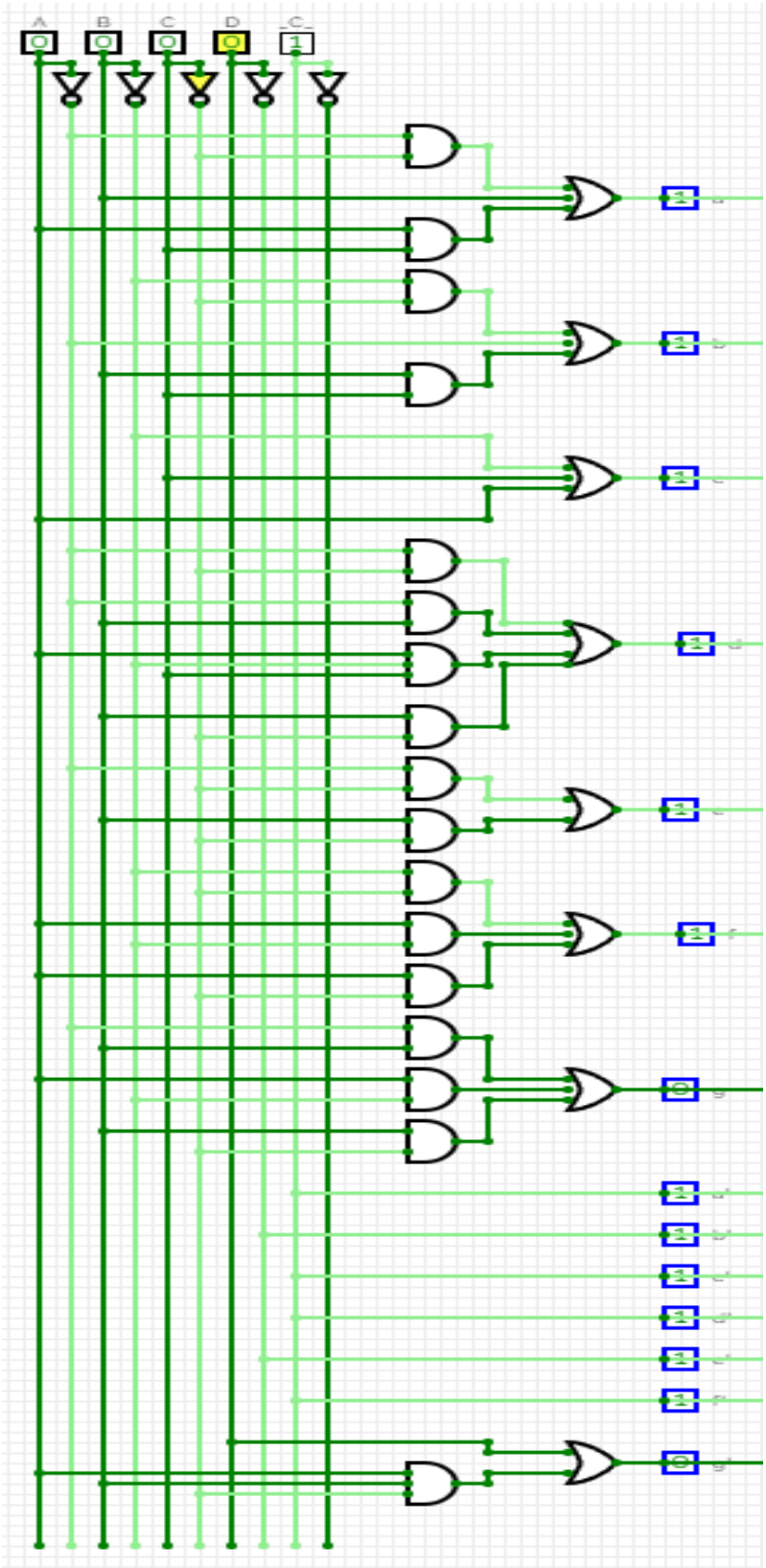
AB\CD	00	01	11	10
00	1			1
01	1			1
11	1			1
10	1			1

b2 = e2 = D’

AB\CD	00	01	11	10
00		1	1	
01		1	1	
11	1	1	1	
10		1	1	

g2 = ABC’ + D

Circuit Diagram:

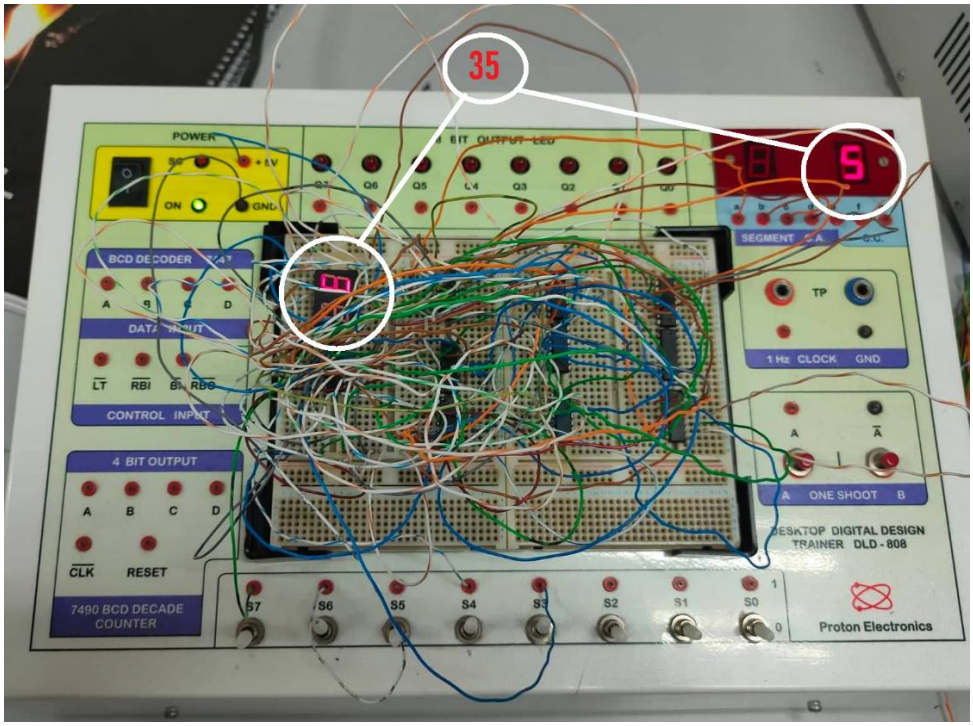


Project implement and output:

Here we are using 5 AND ICs(7408), 4 OR ICs(7432) and 1 NOT IC(7404) for implementing the project. Also we have used trainer board's in-built seven segment display and a seven segment IC.

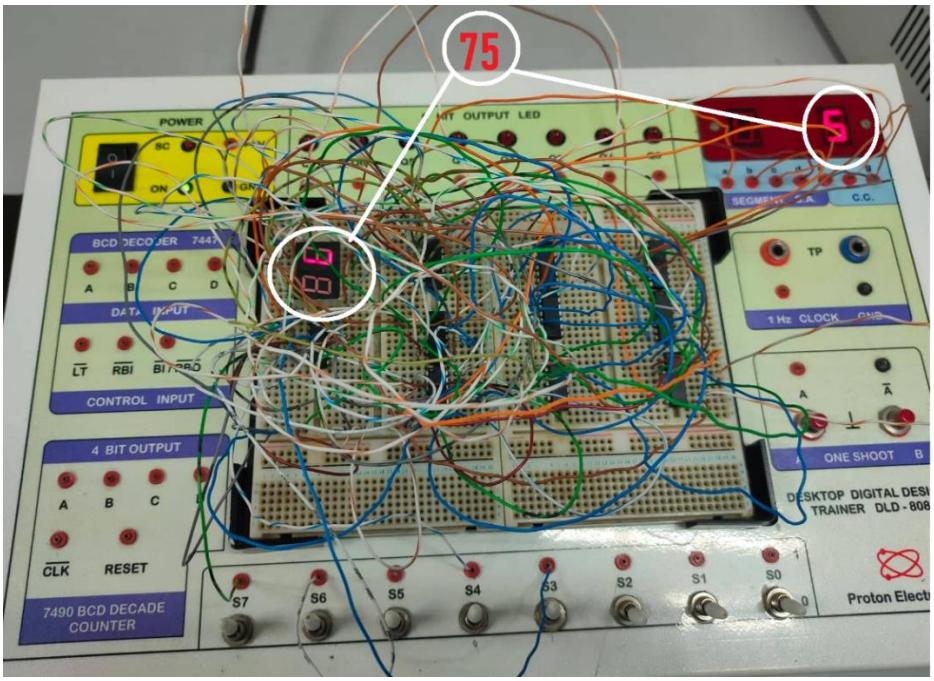
Here, for some technical issue in lab tools, we could not able to show 2 digits together in seven segment display. However we have shown the unit digits in the main seven segment of the trainer board and the tens digits in the seven segment IC.

Here input S7 is A, S6 is B, S4 is C and S3 is D. S5 is not any input



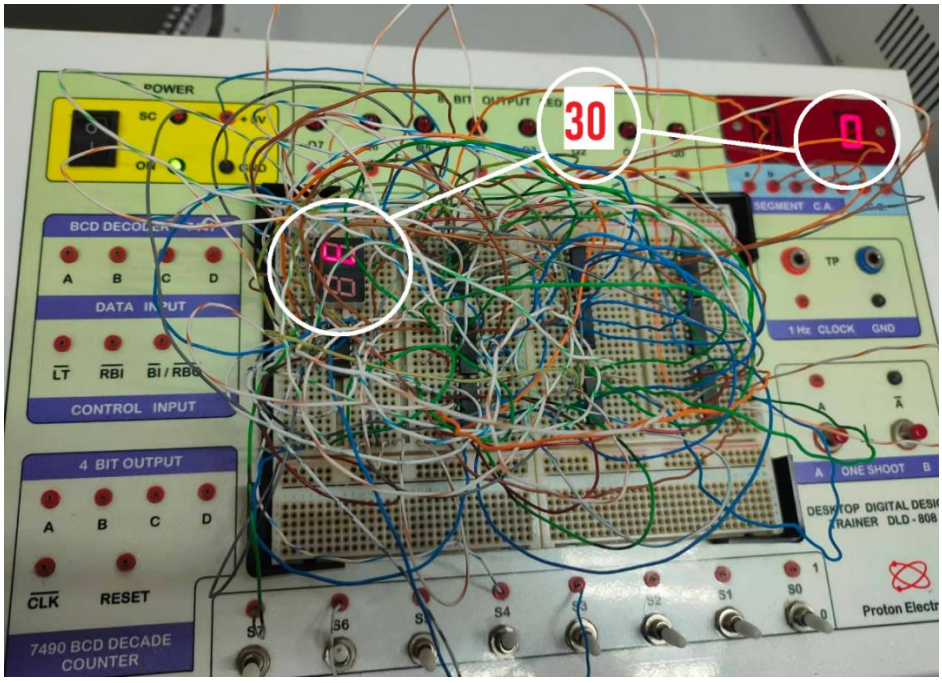
Input: 7Km (0111)

Output: 35



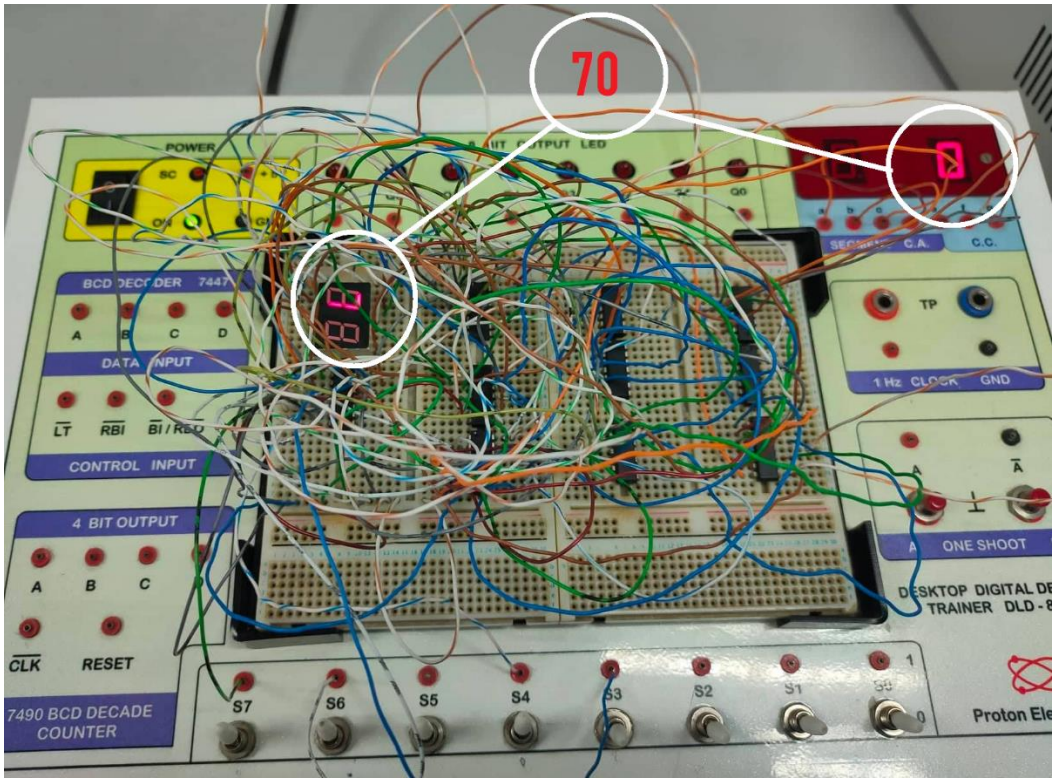
Input: 15Km (1111)

Output: 75



Input: 6Km (0110)

Output: 30

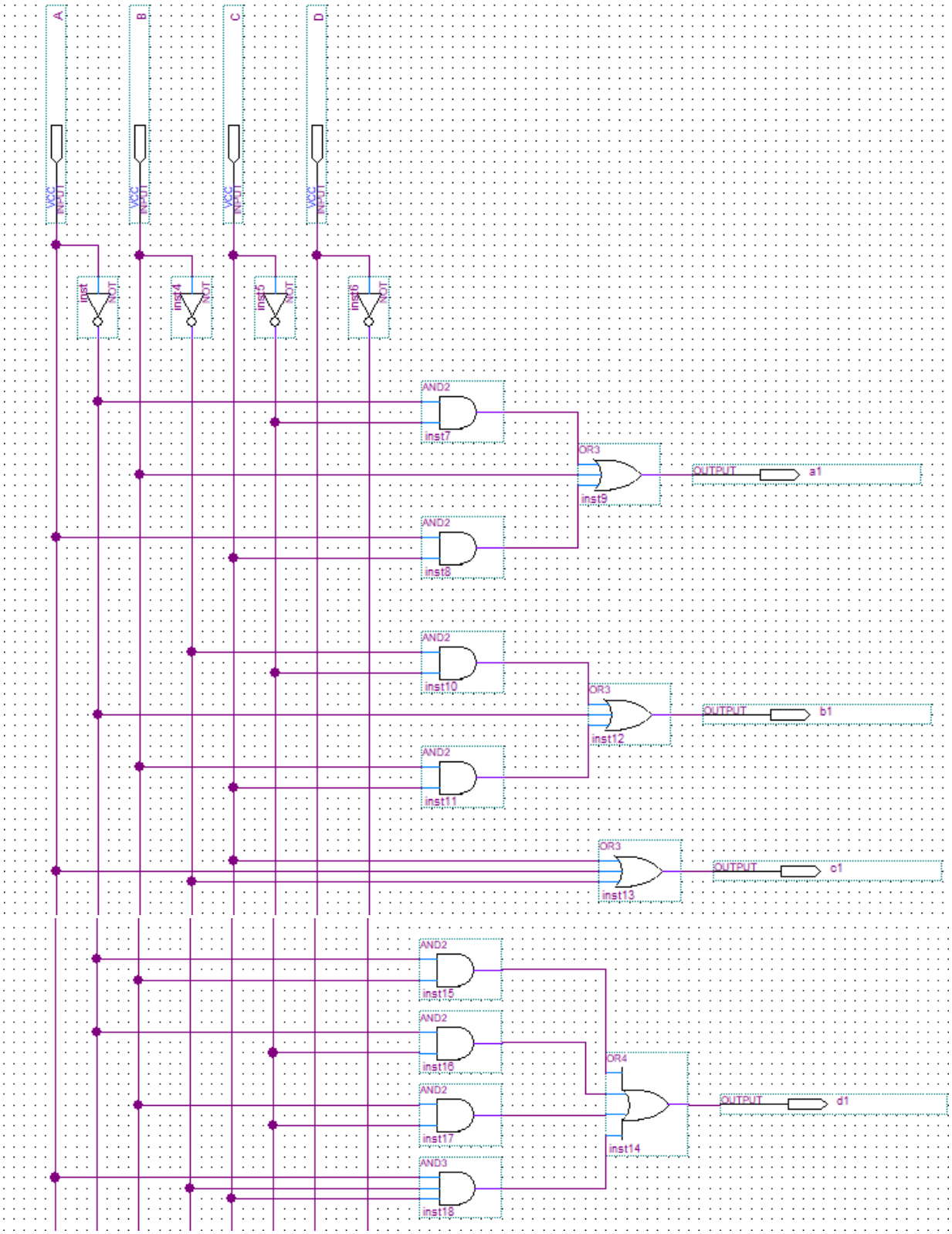


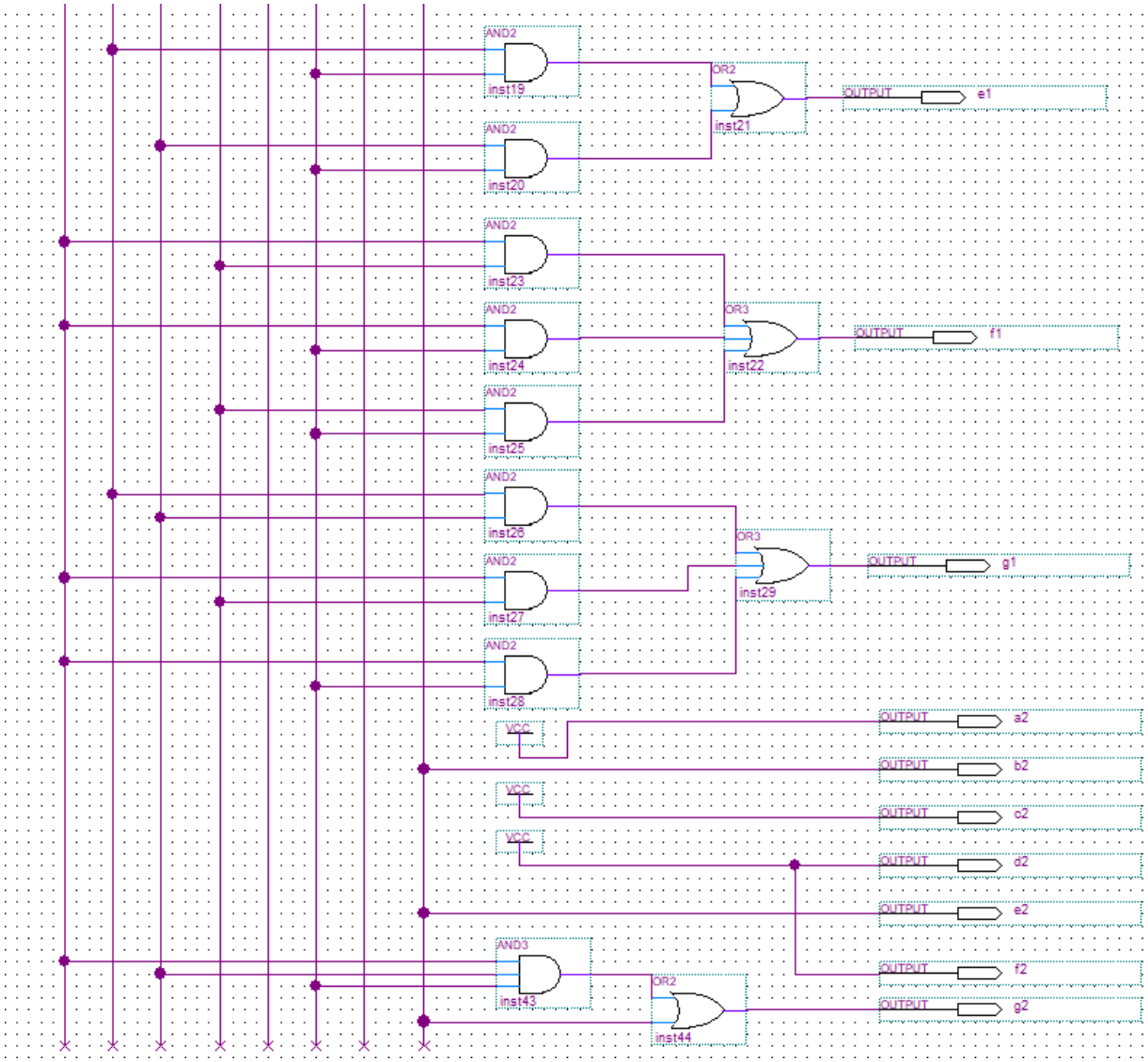
Input: 14Km (1110)

Output: 70

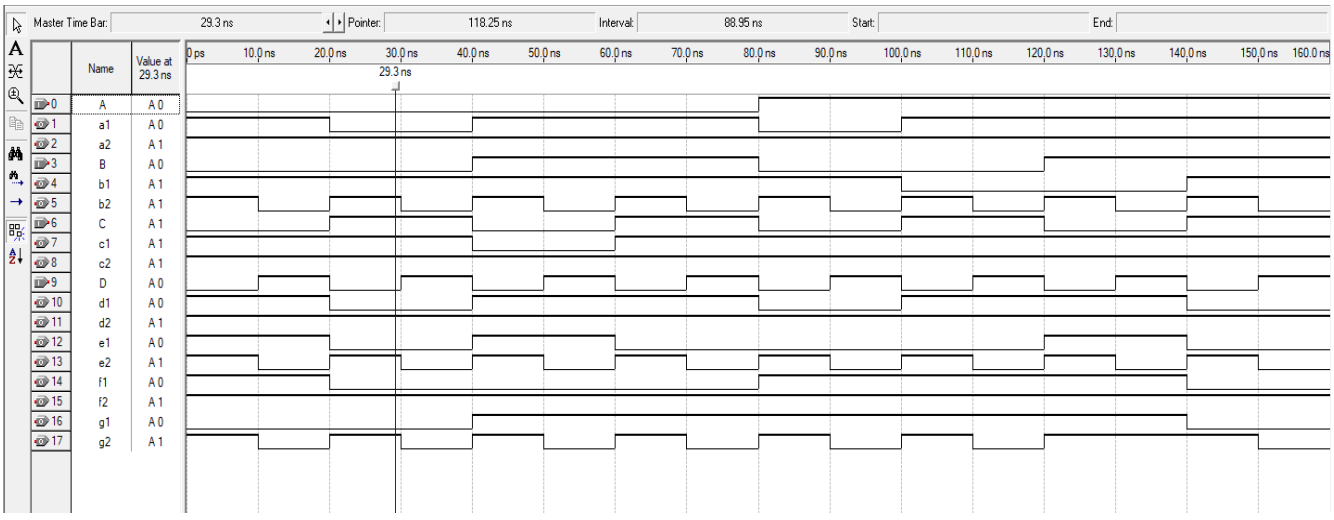
Here we have shown some of the pictures of the results which we have clicked after the implementation the project practically in our lab. We have shown here for the length of 6km, 7km, 14km and 15 km where we get the results as 30, 35, 70 and 75. Which passengers have to pay in Tk.

Simulation:

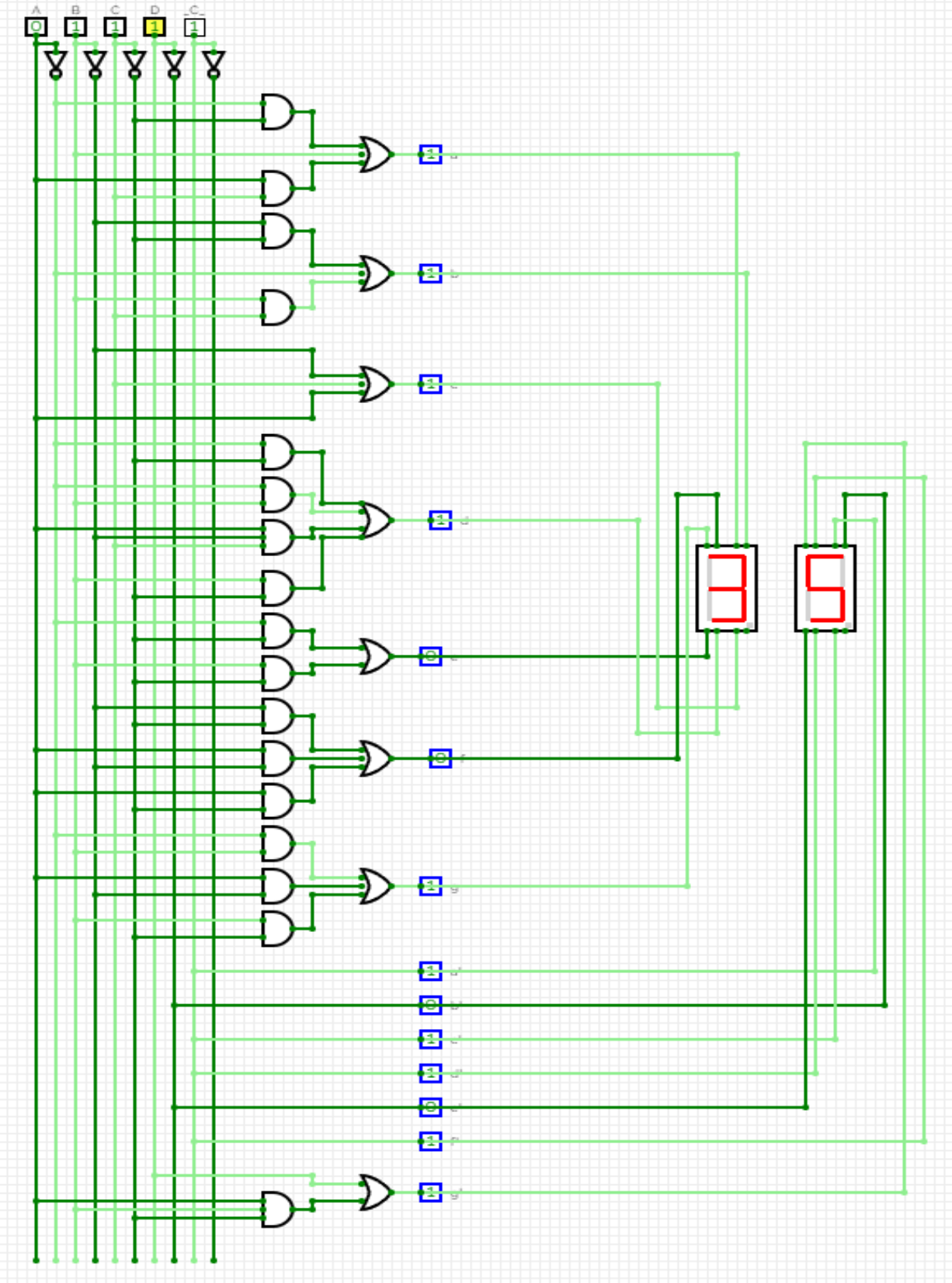

A
B
C
D
VCC
INPUT
inst
inst4
inst5
inst6
NOT
AND2
inst7
inst8
inst10
inst11
AND3
inst18
OR3
inst9
inst12
inst13
OR4
inst14
inst15
inst16
inst17
OUTPUT
a1
b1
c1
d1


AND2
inst19
OR2
inst21
OUTPUT
e1
AND2
inst20
AND2
inst23
AND2
inst24
OR3
inst22
OUTPUT
f1
AND2
inst25
AND2
inst26
OR3
inst29
OUTPUT
g1
AND2
inst27
AND2
inst28
VCC
OUTPUT
a2
VCC
OUTPUT
b2
VCC
OUTPUT
c2
OUTPUT
d2
OUTPUT
e2
AND3
inst43
OR2
inst44
OUTPUT
f2
OUTPUT
g2

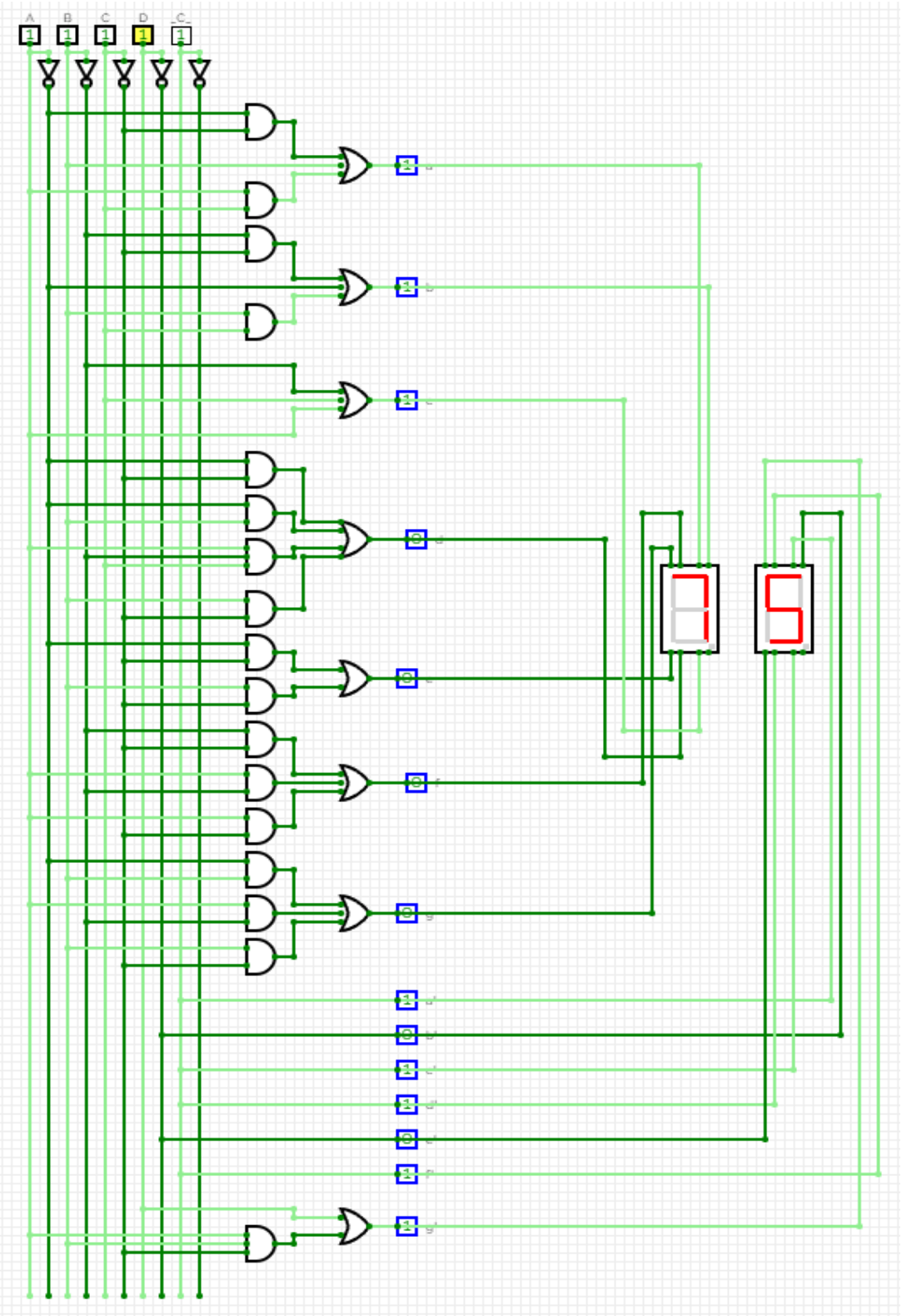
Waveform:


Master Time Bar:
29.3 ns
Pointer:
118.25 ns
Interval:
88.95 ns
Start:
End:
Name
Value at 29.3 ns
0 ps
10.0 ns
20.0 ns
30.0 ns
40.0 ns
50.0 ns
60.0 ns
70.0 ns
80.0 ns
90.0 ns
100.0 ns
110.0 ns
120.0 ns
130.0 ns
140.0 ns
150.0 ns
160.0 ns
29.3 ns
0 A 0
1 a1 A 0
2 a2 A 1
3 B A 0
4 b1 A 1
5 b2 A 1
6 C A 1
7 c1 A 1
8 c2 A 1
9 D A 0
10 d1 A 0
11 d2 A 1
12 e1 A 0
13 e2 A 1
14 f1 A 0
15 f2 A 1
16 g1 A 0
17 g2 A 1

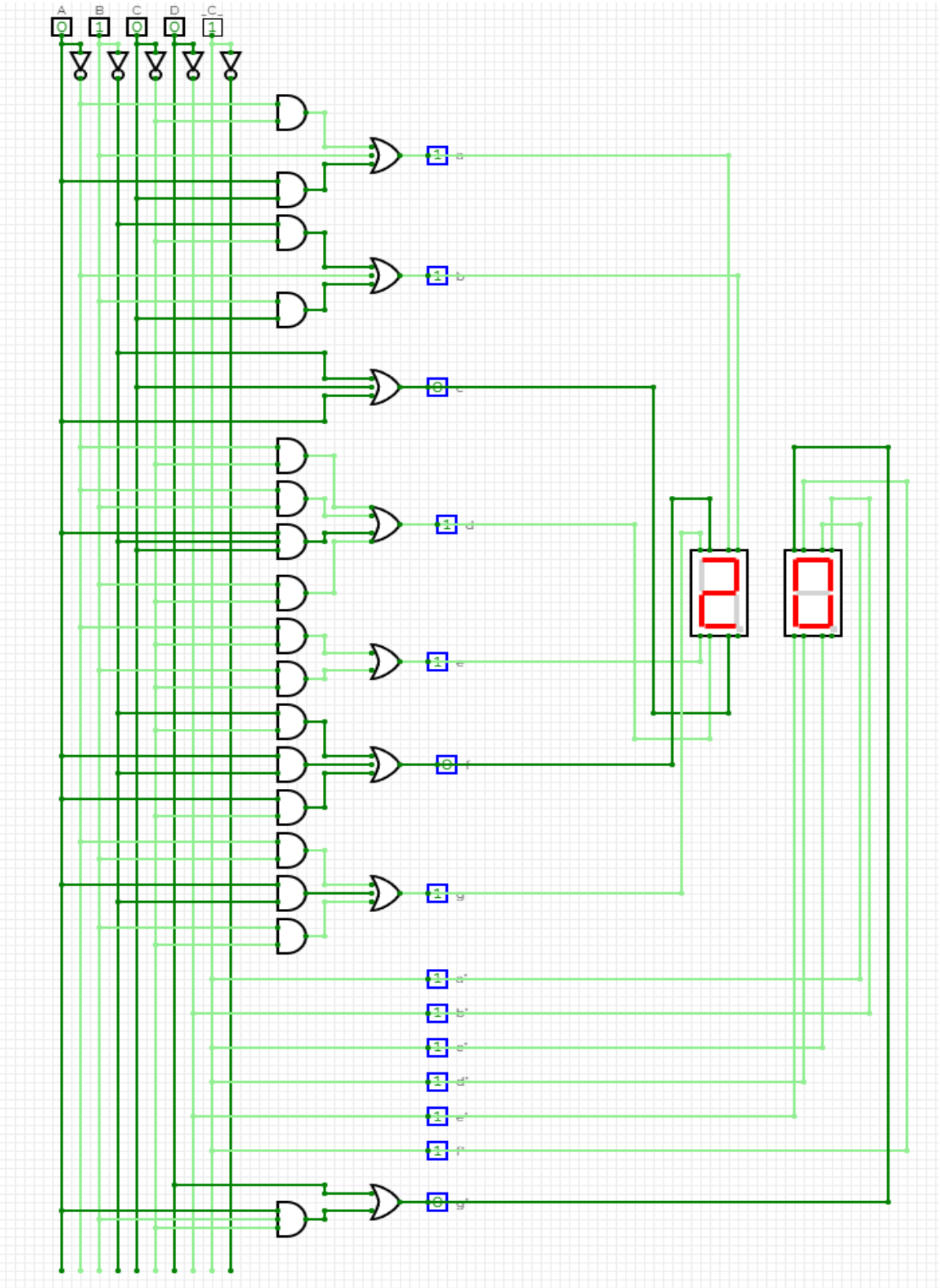
Simulation with 7 segment display: When input is 0111 (7KM), output is 35



When input is 1111 (15KM), output is 75



When input is 0100 (4KM), output is 20



Verilog code:

```
1  module project(input A,B,C,D,
2                 output a1,b1,c1,d1,e1,f1,g1,a2,b2,c2,d2,e2,f2,g2);
3  assign a1= B | ~A & ~C | A & C;
4  assign b1= ~A | ~B & ~C | B & C;
5  assign c1= C | A | ~B';
6  assign d1= ~A & B | ~A & ~C | B & ~C | A & ~B &C;
7  assign e1= ~A & ~C  | B & ~C;
8  assign f1= A & ~B | A & ~C | ~B & ~C;
9  assign g1= ~A & B | A & ~B | A & ~C;
10 assign a2= 1;
11 assign b2= ~D;
12 assign c2= 1;
13 assign d2= 1;
14 assign e2= ~D;
15 assign f2= 1;
16 assign g2= A & B & ~C | D;
17 endmodule
18
```

Discussion:

We get successful in our project after implementing it as per our plan. We have learnt a lot of things and clear our concepts a bit more by doing the project. While implementing the logic circuit we face faced some of the difficulties as we have lots of connections. Also we face difficulties in connecting our seven segment display. As, we have no previous knowledge about implementing it. So, we self-studied to know the connections and then we able to connect that properly. However it was a little bit challenging to give all the connections of wires in one beard board properly. By doing this project we can enlarge our thinking and vision ability. Which can help us to do more and more projects like this, with the help our own thoughts.