

Data Book

AU6333
USB2.0 SD/MMC/MS
Single/Dual LUN
Card Reader Controller
Technical Reference Manual

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| ILINIACTIVA SNACITICATION | This data book contains target specifications for product development. |
|---------------------------|--|
| Preliminary specification | This data book contains preliminary data; supplementary data may be published later. |
| Product specification | This data book contains final product specifications. |

Revision History

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| Sep 2005 | 1.02W | Moved "3.0 Power Switch Feature" to "5.6 Power Switch Feature" |
| Jan 2006 | 1.03W | Add "Support SD 2.0 specification" feature |
| Aug 2006 | 1.04W | Update new address of Los Angeles Office |



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Contact Information:

Web site: http://www.alcormicro.com/

Taiwan

Alcor Micro Corp. 4F, No 200 Kang Chien Rd., Nei Hu, Taipei, Taiwan, R.O.C.

Phone: 886-2-8751-1984 Fax: 886-2-2659-7723

China ShenZhen Office

Rm.2407-08 ,Industrial Bank Building No.4013, Shennan Road ,ShenZhen,China.

518026

Phone: (0755) 8366-9039 Fax: (0755) 8366-9101

Santa Clara Office

2901 Tasman Drive, Suite 206 Santa Clara, CA 95054 USA

Phone: (408) 845-9300 Fax: (408) 845-9086

Los Angeles Office

9070 Rancho Park Court Rancho Cucamonga, CA 91730 USA

Phone: (909) 483-9900 Fax: (909) 944-0464



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1.0 Introduction

1.1 Description

AU6333 is an USB2.0 high-speed transmission controller, which is designed as a bridge between USB and SD/MS compatible flash card interface, such as SD, HS-SD, MMC, HS-MMC, RS-MMC, MMCmicro, MS, MS Pro and MS Duo...etc. AU6333 can read digital contents stored on memory card designed to cover a wide area of applications such as digital cameras, PDAs, MP3 players and smart phones...etc. With the AU6333, users can transfer digital data between flash memory card and PC or other electronic devices.

AU6333 inherits the high-performance and cost-efficiency character from Alcor's products, included power switch integration, dynamic icon utility support, and DMA engine integration.

1.2 Features

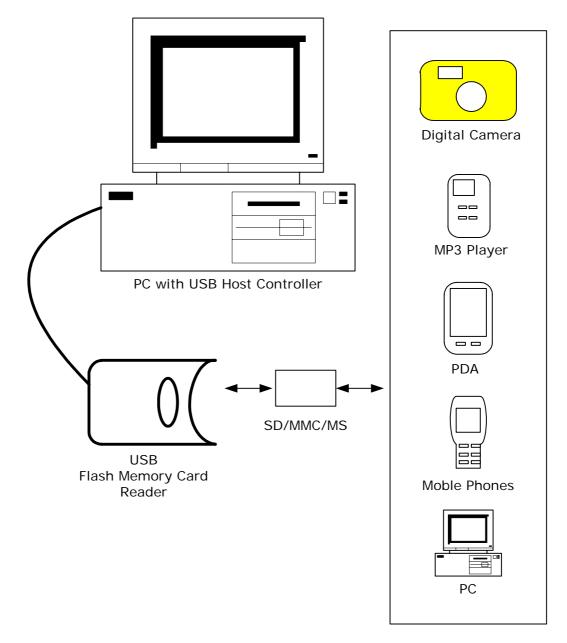
- Support USB V2.0 specification and USB Device Class Definition for Mass Storage, Bulk-Transport V1.0
- Support SD/MMC/MS compatible flash card
- Support the latest flash card specification: SD1.1 (HS-SD), MMC4.0 (8-bit), MSPro parallel mode (4-bit)
- Support SD 2.0 specification
- Alcor DMA engine integrated for performance enhancement
- Work with default driver from Windows ME/2000/XP and Mac OS X; Windows 98/2000(SP1/SP2) and Mac OS 9 are supported by vendor driver from Alcor.
- Ping-pong FIFO implementation for concurrent bus operation
- Support multiple sectors transfer optimize performance
- Support slot-to-slot read/write operation (Dual LUN)
- Support Dynamic Icon Utility
- Support LED for bus operating indication
- Power switch integrated to reduce production BOM cost
- Built in 2.5V regulator



2.0 Application Block Diagram

Following is the application diagram of a typical card reader product with AU6333. By connecting the card reader to a desktop or notebook PC through USB bus, AU6333 is implemented as a bus-powered, high speed USB card reader, which can be used as a bridge for data transfer between Desktop PC and Notebook PC.

2.1 Block Diagram





3.0 Pin Assignment

The AU6333 is packed in 48pin-LQFP-form factor. The following figure shows signal name for each pin and the table in the following page describes each pin in detail.

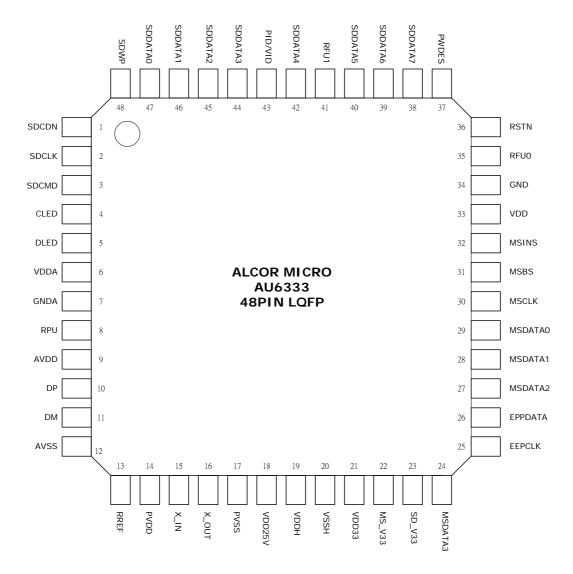


Figure 3.1 Pin Assignment Diagram



Table 3.1 Pin Descriptions

| Pin # | Pin Name | 1/0 | Description |
|-------|----------|-----|---|
| 1 | SDCDN | ı | SD card detect; |
| | SDCDIN | ı | ("0":Detected; "1":unDetected[Default]) |
| 2 | SDCLK | 0 | SD CLK |
| 3 | SDCMD | 1/0 | SD CMD |
| 4 | CLED | 0 | Card activity LED |
| 5 | DLED | 0 | Device LED |
| 6 | VDDA | I | 2.5V Analog power |
| 7 | GNDA | I | Analog GND |
| 8 | RPU | ı | Connect 1.5K pull up resistor to 3.3V VDD |
| 9 | AVDD | I | 3.3V Analog power |
| 10 | DP | 1/0 | DP |
| 11 | DM | 1/0 | DM |
| 12 | AVSS | I | Analog GND |
| 13 | RREF | I | Connect 1K resistor to AVSS for impedance match |
| 14 | PVDD | I | OSC power 3.3V |
| 15 | X_IN | I | 12MHz crystal input |
| 16 | X_OUT | 0 | 12MHz crystal output |
| 17 | PVSS | I | OSC GND |
| 18 | VDD25V | 0 | 2.5V output connect to core power VDD |
| 19 | VDDH | I | I/O power 3.3V |
| 20 | VSSH | I | I/O GND |
| 21 | VDD33 | I | 3.3V for card power |
| 22 | MS_V33 | 0 | 3.3V for MS card |
| 23 | SD_V33 | 0 | 3.3V for SD card |
| 24 | MSDATA3 | 1/0 | MS data3 |
| 25 | EEPCLK | 0 | EEPROM CLK |
| 26 | EPPDATA | 1/0 | EEPROM Data |
| 27 | MSDATA2 | 1/0 | MS data2 |
| 28 | MSDATA1 | 1/0 | MS data1 |
| 29 | MSDATA0 | 1/0 | MS data0 |
| 30 | MSCLK | 0 | MS CLK |
| 31 | MSBS | 0 | MS BS |
| 32 | MSINS | I | MS INS |
| 33 | VDD | I | Core power 2.5V |
| 34 | GND | I | Core GND |
| 35 | RFU0 | I | Always pull low |
| 36 | RSTN | I | Chip reset, pull up with RC. |
| 37 | PWDES | I | Operating power in confiscation Descriptor; ("0": 100mA[Default]; "1": 250mA) |



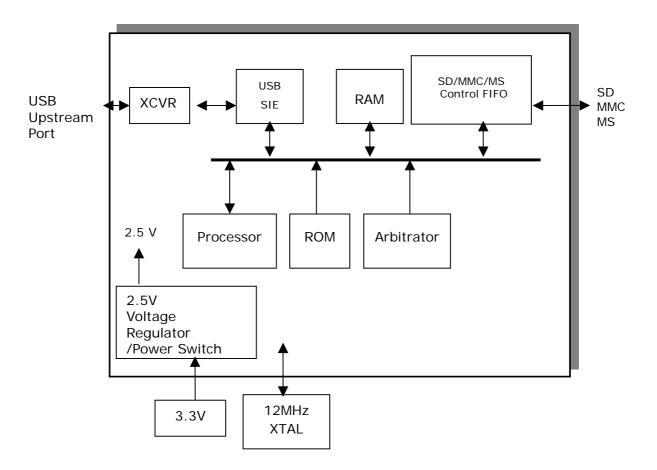
| Pin # | Pin Name | 1/0 | Description |
|-------|----------|-----|--|
| 38 | SDDATA7 | 1/0 | SD data7 |
| 39 | SDDATA6 | 1/0 | SD data6 |
| 40 | SDDATA5 | 1/0 | SD data5 |
| 41 | RFU1 | I | Always pull low |
| 42 | SDDATA4 | 1/0 | SD data4 |
| 43 | PID/VID | I | LUN Mode Selection ("0": 2-LUN; "1": 1-LUN) |
| 44 | SDDATA3 | 1/0 | SD data3 |
| 45 | SDDATA2 | 1/0 | SD data2 |
| 46 | SDDATA1 | 1/0 | SD data1 |
| 47 | SDDATA0 | 1/0 | SD data0 |
| 48 | SDWP | I | SD write protect |



4.0 System Architecture and Reference Design

4.1 AU6333 Block Diagram

Figure 4.1 AU6333 Block Diagram





5.0 Electrical Characteristics

5.1 Absolute Maximum Ratings

Table 5.1 Absolute Maximum Ratings

| SYMBOL | BOL PARAMETER RATING | | UNITS |
|------------------|----------------------|------------------------------|-------|
| V _{CC} | Power Supply | -0.3 to V _{CC} +0.3 | V |
| V _{IN} | Input Voltage | -0.3 to 3.6 | V |
| V _{OUT} | Output Voltage | -0.3 to V _{CC} +0.3 | V |
| T _{STG} | Storage Temperature | -40 to 150 | °C |

5.2 Recommended Operating Conditions

Table 5.2 Recommended Operating Conditions

| SYMBOL | PARAMETER | MIN | TYP | MAX | UNITS |
|------------------|-----------------------|------|-----|------|-------|
| V _{CC} | Power Supply | 3.0 | 3.3 | 3.6 | V |
| V_{DD} | Digital Supply | 2.25 | 2.5 | 2.75 | V |
| V _{IN} | Input Voltage | 0 | 3.3 | 5.2 | V |
| T _{OPR} | Operating Temperature | 0 | | 85 | °C |

5.3 Leakage Current and Capacitance

Table 5.3 General DC Characteristics

| SYMBOL | PARAMETER | CONDITIONS | MIN | TYP | MAX | UNITS |
|------------------|-----------------------------------|----------------------------|-----|-----|-----|-------|
| I _{IN} | Input current | no pull-up or pull-down | -10 | ±1 | 10 | μА |
| I _{OZ} | Tri-state leakage current | | -10 | ±1 | 10 | μА |
| C _{IN} | Input capacitance | Pad Limit | | 2.8 | | ρF |
| Соит | Output capacitance | Pad Limit | | 2.8 | | ρF |
| C _{BID} | Bi-directional buffer capacitance | Pad Limit | | 2.8 | | ρF |



5.4 DC Electrical Characteristics of 3.3V I/O Cells

Table 5.4 DC Electrical Characteristics of 3.3V I/O Cells

| SYMBOL | PARAMETER | CONDITIONS | | UNIT | | |
|-----------------|----------------------------------|---------------------------|-----|------|-----|---------|
| STIVIBUL | | CONDITIONS | MIN | TYP | MAX | UNIT |
| V _{CC} | Power supply | 3.3V I/O | 3.0 | 3.3 | 3.6 | V |
| V _{il} | Input low voltage | LVTTL | | | 0.8 | V |
| V_{ih} | Input high voltage | LVIIL | 2.0 | | | V |
| V _{ol} | Output low voltage | I _{ol} =2~16mA | | | 0.4 | V |
| V _{oh} | Output high voltage | I _{oh} =2~16mA | 2.4 | | | V |
| R _{pu} | Input pull-up resistance | PU=high, PD=low | 40 | 75 | 190 | ΚΩ |
| R _{pd} | Input pull-down resistance | PU=low, PD=high | 40 | 75 | 190 | ΚΩ |
| I _{in} | Input leakage current | $V_{in} = V_{CC}$ or 0 | -10 | ±1 | 10 | μ A |
| l _{oz} | Tri-state output leakage current | | -10 | ±1 | 10 | μ A |



5.5 USB Transceiver Characteristics

Table 5.5 Electrical characteristics

| | Table old Electrical characteristics | | | | | | |
|-----------------------|--------------------------------------|---|------|------|------|------|--|
| Symbol | Parameter | Conditions | Min. | Тур. | Max. | Unit | |
| AVCC | Analog supply Voltage | | 3.0 | 3.3 | 3.6 | V | |
| VCC | Digital supply Voltage | | 2.25 | 2.5 | 2.75 | V | |
| I _{CC} | Operating supply current | High speed operating at 480 MHz | | | 73 | mA | |
| I _{CC(susp)} | Suspend supply current | In suspend mode, current with 1.5kΩ pull-up resistor on pin RPU disconnected | | | 120 | μΑ | |

Table 5.6 Static characteristic: Digital pin

| Symbol | Parameter | Conditions | Min. | Тур. | Max. | Unit | |
|-----------------|---------------------------|------------|---------|------|------|------|--|
| Input levels | | | | | | | |
| V _{IL} | Low-level input voltage | | | | 0.8 | V | |
| V _{IH} | High-level input voltage | | 2.0 | | | V | |
| Output levels | | | | | | | |
| V _{OL} | Low-level output voltage | | | | 0.2 | V | |
| V _{OH} | High-level output voltage | | VCC-0.2 | | | V | |

AVCC=3.0V~3.6V; VCC=2.25V~2.75V; Temp=0 $^{\circ}$ C~85 $^{\circ}$ C



Table 5.7 Static characteristic : Analog I/O pins (DP/DM)

| | Table 5.7 Static chara | acteristic . Analog 17 | O pins | וט /פט | | | |
|--------------------------------------|--|---|--------|--------|------|------|--|
| Symbol | Parameter | Conditions | Min. | Тур. | Max. | Unit | |
| | USB | 2.0 Transceiver (HS) | | | | | |
| | Input Lev | vels (differential receiv | ver) | | | | |
| V _{HSDIFF} | High speed differential input sensitivity | V _{I (DP)} -V _{I (DM)} measured at the connection as application circuit | 300 | | | mV | |
| V _{HSCM} | High speed data signaling common mode voltage range | | -50 | | 500 | mV | |
| V _{HSSQ} | High speed squelch detection threshold | Squelch detected | | | 100 | mV | |
| VHSSQ | | No squelch detected | 150 | | | mV | |
| V _{HSDSC} | High speed disconnection | Disconnection detected | 625 | | | mV | |
| ▼ HSDSC | detection threshold | Disconnection not detected | | | 525 | mV | |
| | | Output Levels | | | 1 | | |
| V _{HSOI} | High speed idle level output voltage(differential) | | -10 | | 10 | mV | |
| V _{HSOL} | High speed low level output voltage(differential) | | -10 | | 10 | mV | |
| V _{HSOH} | High speed high level output voltage(differential) | | -360 | | 400 | mV | |
| V _{CHIRPJ} | Chirp-J output voltage (differential) | | 700 | | 1100 | mV | |
| V _{CHIRPK} | Chirp-K output voltage (differential) | | -900 | | -500 | mV | |
| | | Resistance | | | | | |
| $R_{ m DRV}$ | Driver output impedance | Equivalent resistance used as internal chip only | 3 | 6 | 9 | Ω | |
| NDRV | | Overall resistance including external resistor | 40.5 | 45 | 49.5 | \$ 2 | |
| | Γ | Termination | | | 1 | 1 | |
| V_{TERM} | Termination voltage for pull-up resistor on pin RPU | | 3.0 | | 3.6 | V | |
| | USB1 | .1 Transceiver (FS/LS |) | | | | |
| Input Levels (differential receiver) | | | | | | | |
| V _{DI} | Differential input sensitivity | $ V_{I(DP)} - V_{I(DM)} $ | 0.2 | | | V | |
| V _{CM} | Differential common mode voltage | | 0.8 | | 2.5 | V | |
| | Input Leve | els (single-ended recei | vers) | | | | |



| V _{SE} | Single ended receiver threshold | | 0.8 | | 2.0 | V | |
|-----------------|---------------------------------|--|-----|--|-----|---|--|
| Output levels | | | | | | | |
| V _{OL} | Low-level output voltage | | 0 | | 0.3 | V | |
| V _{OH} | High-level output voltage | | 2.8 | | 3.6 | V | |

AVCC=3.0V~3.6V; VCC=2.25V~2.75V; Temp=0 $^{\circ}$ C~85 $^{\circ}$ C

Table 5.8 Dynamic characteristic : Analog I/O pins (DP/DM)

| Table 5.8 Dynamic characteristic : Analog 1/O pins (DP/DM) | | | | | | | | |
|--|---|---|------|------|------|------|--|--|
| Symbol | Parameter | Conditions | Min. | Тур. | Max. | Unit | | |
| Driver Characteristics | | | | | | | | |
| High-Speed Mode | | | | | | | | |
| t _{HSR} | High-speed differential rise time | | 500 | | | ps | | |
| t _{HSF} | High-speed differential fall time | | 500 | | | ps | | |
| | | Full-Speed Mode | | | | | | |
| t _{FR} | Rise time | CL=50pF; 10 to 90% of V _{OH} -V _{OL} ; | 4 | | 20 | ns | | |
| t _{FF} | Fall time | CL=50pF; 90 to 10% of $ V_{OH}-V_{OL} $; | 4 | | 20 | ns | | |
| t _{FRMA} | Differential rise/fall time matching (t _{FR} / t _{FF}) | Excluding the first transition from idle mode | 90 | | 110 | % | | |
| V_{CRS} | Output signal crossover voltage | Excluding the first transition from idle mode | 1.3 | | 2.0 | V | | |
| | Low-Speed Mode | | | | | | | |
| t _{LR} | Rise time | CL=200pF-600pF; 10 to 90% of V _{OH} -V _{OL} ; | 75 | | 300 | ns | | |
| t _{LF} | Fall time | CL=200pF-600pF; 90 to 10% of V _{OH} -V _{OL} ; | 75 | | 300 | ns | | |
| t _{LRMA} | Differential rise/fall time matching (t _{LR} / t _{LF}) | Excluding the first transition from idle mode | 80 | | 125 | % | | |
| V_{CRS} | Output signal crossover voltage | Excluding the first transition from idle mode | 1.3 | | 2.0 | V | | |
| V_{OH} | High-level output voltage | | 2.8 | | 3.6 | V | | |

5.6 Power Switch Feature

AU6333 integrates a 3.3V to 2.5V voltage regulator and power switch to replace all MOS chips for flash card power supply.

Card Power Output Current Range

■ For SD/MMC

◆ MAX: 200mA

■ For MS

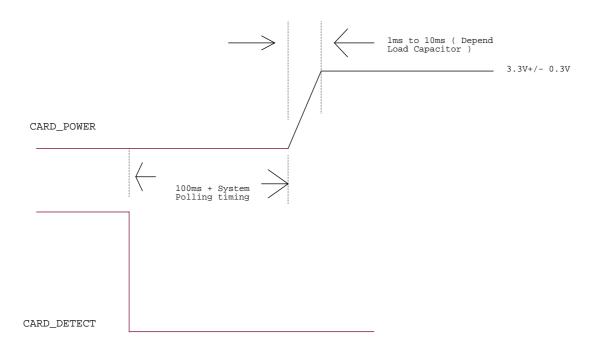
MAX: 100mA

Card power output voltage range

♦ SD/MMC/MS: 3.3V±0.3V

■ AU6333 will turn off all of Card Power in suspend mode

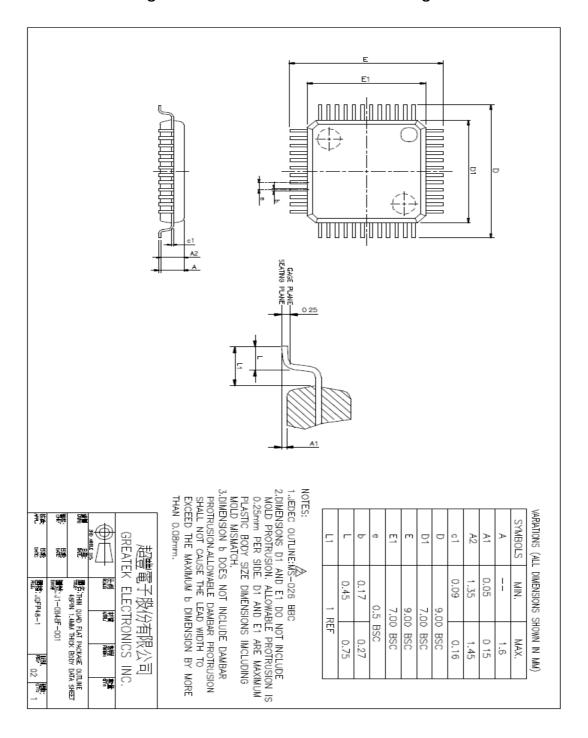
Figure 5.1 Card Detect Power-on Timing





6.0 Mechanical Information

Figure 6.1 Mechanical Information Diagram







7.0 Abbreviations

This chapter lists and defines terms and abbreviations used throughout this specification.

SIE Serial Interface Engine

SD Secure DigitalMMC Multimedia CardMS Memory Stick Card

UTMI USB Transceiver Macrocell Interface

[MEMO]

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Alcor Micro, Corp. designs, develops and markets highly integrated and advanced peripheral semiconductor, and software driver solutions for the personal computer and consumer electronics markets worldwide. We specialize in USB solutions and focus on emerging technology such as USB and IEEE 1394. The company offers a range of semiconductors including controllers for USB hub, integrated keyboard/USB hub and USB Flash memory card reader...etc. Alcor Micro, Corp. is based in Taipei, Taiwan, with sales offices in Taipei, Japan, Korea and California.

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