

Timing diagram showing the relationship between the clock (clk), input (in), and outputs (out1, out2, out3) over a 120 ns period. The clock (clk) is a periodic square wave. The input (in) is a single pulse at 10 ns. The outputs (out1, out2, out3) represent the 3-bit counter state, with out1 being the least significant bit and out3 the most significant bit. The counter increments on each rising edge of clk, triggered by the in pulse.

Signal	0-10 ns	10-20 ns	20-30 ns	30-40 ns	40-50 ns	50-60 ns	60-70 ns	70-80 ns	80-90 ns	90-100 ns	100-110 ns	110-120 ns
clk	Low	High	Low	High	Low	High	Low	High	Low	High	Low	High
in	Low	High	Low	Low	Low	Low	Low	Low	Low	Low	Low	Low
out1	0	0	1	1	0	0	1	1	0	0	1	1
out2	0	0	0	1	1	0	0	1	1	0	0	1
out3	0	0	0	0	1	1	0	0	1	1	0	0