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Digital



16/07/2012

Digital System

- Boolean Expressions, Laws, K-maps
variable Entout map minimization ($V \oplus M$ - minimization).
- Multiplexers, De-mux, Encoder, Decoder
- Hazards: S-a-0, S-a-1, path
for connecting test vectors
- flip-flop...Types, Interconnection
Counters and sequence detectors

switching theory and automation \Rightarrow Z-kobagi
 Digital Electronics - R.P. Jain
 * Digital Electronics - Malvino Leach

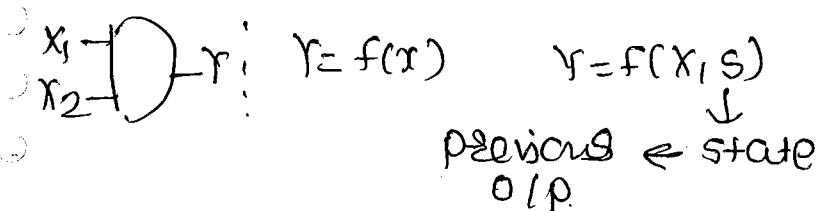
Digital Systems

Combinational
function

sequential
function

Multi-ip
single ip

multi-ip
multi-ip,



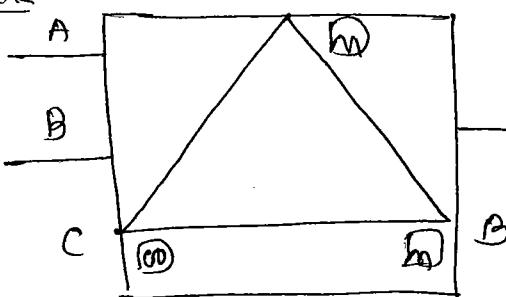
selection by Elimination

Physical problem \rightarrow Boolean Exp. \rightarrow Computing m/c
 \rightarrow Boolean gates' \rightarrow Boolean Result \rightarrow Actuator
 Selection

Track simulation

clock = anti-clock

0 1



$f(A, B, C) = 1$ iff
only two vehicles
meet together.

Same velocity

A	B	C	F
0	0	0	0 ← No two vehicles will meet.
0	0	1	1 ← BC → min-term
0	1	0	1 ← AB .
0	1	1	1 AB
1	0	0	1 AC
1	0	1	1 BC
1	1	0	1 AC
1	1	1	0 ← moving anti-clockwise (all vehicles)

product of
input
variables
(::1),

$$f(A, B, C) = \overbrace{A'B'C + A'BC' + ABC}^{\text{SOP}} + AB'C' + A'BC + ABC$$

$$= \Sigma(1, 2, 3, 4, 5, 6).$$

max-term



sum of i/p
variables (::0).



$(A + B + C)$



$$f(A, B, C) = (A + B + C) (A' + B' + C')$$

POS

$$\underline{\underline{\Sigma \pi(0, 7)}}.$$

Ques. What will be minterms of fun. $f(p,q,r) = pqr + \bar{p}qr$

$$+ p \overline{R}$$

- (a) $m_2 + m_4 + M_6 + m_7$

(b) $M_0 + M_1 + m_3 + m_5$

(c) $M_0 + m_1 + m_6 + m_7$

(d) $m_2 + m_3 + m_4 + m_5$

$$\underline{\leq (2, 4, 6, 7)}$$

maxterms

$$\frac{m_0 m_1 m_3 m_5}{\pi(0,1,3,5)}$$

" If oil is having more min-teens the
pos oil sop "

AB	f_1	f_2	B
00	0	0	1
01	1	0	0
10	1	0	1
11	1	1	1

↓ ↓ ↓

$A+B$	$A \cdot B$	$(A+B')$
(POS)	(SOP)	(POS)

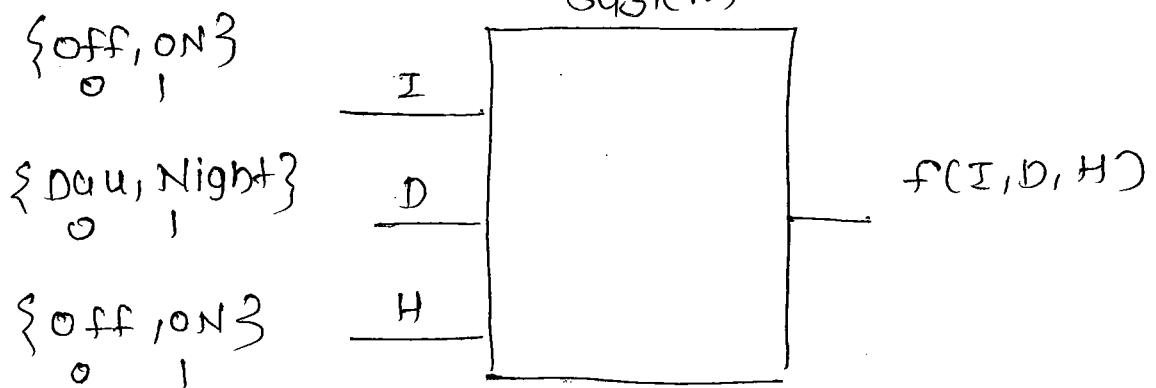
JES

\oplus $f(A, B)$ denotes 'OR' operation

$$A + \theta \equiv A'B + AB' + A\bar{B}$$

$$\underline{\text{SOP}} \rightarrow \overline{AB} = (A+B) \cdot (A+B') \cdot (\overline{A}+B) \quad \leftarrow \underline{\text{POS}}$$

Headlight switching system



I	D	H	$f(I, D, H)$
0	0	0	0
0	0	1	1
0	1	0	0
0	1	1	1
1	0	0	0
1	0	1	0
1	1	0	1
1	1	1	0

$$f(I, D, H) = I'D'H + I'DH + ID'H + IDH$$

SOP $\Leftrightarrow \{1, 3, 5, 6\}$

$$f(I, D, H) = (I+D+H) \cdot (I+D+H') \cdot (I'+D+H) \cdot (I'+D+H')$$

POS _{Position} $= \pi(0, 2, 4, 7)$

What are the max-terms in the given expression.

$$f(A, B, C) = A' + BC$$

(pos)

a) 3, 5, 6

b) 4, 5, 6

c) 5, 6, 7

d) 3, 4, 6, 7

$$\underline{x+yz = (x+y)(x+z)}$$

$$= \underline{(A'+B)} \underline{(A'+C)}$$

A B C

1 0 \emptyset

* 4, 5

A B C

1 \emptyset 0

1 0 0

1 1 0

6, 4

4, 5, 6

Que. Consider a 3-ip, 3-op function where the ips are A, B, C and ops are P, Q, R. The relation between ip and op is given as -

$D_0 = (D_i + 3) \bmod 8$. where D_i and D_0 represent decimal values of binary ip's and binary op's resp.

Ex. A B C D_i D₀ P Q R

0 1 0 $\Rightarrow 2 \Rightarrow 5$ 1 0 1

midterm

which of follow. exp. gives R(A, B, C)

a) $\Sigma(0, 2, 4, 6)$ c) $\Sigma(0, 1, 4, 7)$

b) $\Sigma(1, 3, 5, 7)$ d) $\Sigma(0, 2, 4, 5)$.

With respect to the O/P's of above, identify the correct statement.

(a) Except for the O/P ② other functional means few min-terms each P

(b) Only OR contains equal no. of min-terms & max-terms

(c) All the O/P's are having equal no. of min-terms and max-terms

(d) None of the O/P's contain 4 min-terms.

$$D_i = (D_i + 3) \bmod 8$$

↑

k-times rotated version.

O/P is equal to O/P

3 (k) variable will have 8 no. of min-terms.

4 _____ 16 _____ .

(Ques) The characteristics of boolean expression is.

1) every boolean expression must contain atleast one function

(2) Complemented function

Duality

The Duality is used for indirect proof of (ex p) function.

→ It is used for converting the realization from one logic system to another logic system

→ The dual funⁿ is obtained by complementing and
operations to OR and vice versa

0 is obtained

0 is replaced with 1 and 1 with 0.

$$X+1=1;$$

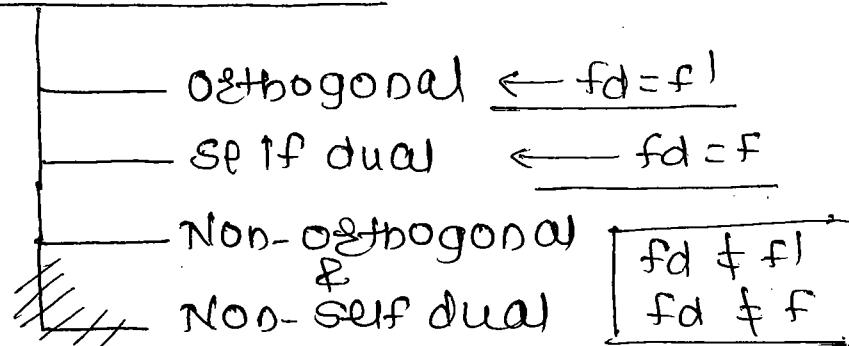
$$X \cdot 0=0;$$

Ques. Obtain the dual function for the following →

$$\underline{f(A,B,C) = A'(B+C) + A(B'C')}$$

$$\rightarrow \underline{f_d(A,B,C) = (A'+BC) \cdot (A+B'C')}$$

→ Based on the relation between the funⁿ and its dual the boolean function is classified as,



e.g. obtain the dual for $f(A,B) = A'B + AB'$

$$\rightarrow \underline{f_d(A,B) = (A'+B) \cdot (A+B')}$$

$$\frac{\Pi(1,2)}{\Sigma(1,2)}$$

$$\underline{f_d = f'}$$

min-term of one funⁿ =

max term then

complement of funⁿ.

Even i/p EX-OR and EX-NOR are having orthogonal relation. $\therefore f_d = f_1$.

$$f(A, B, C) = A \oplus B \oplus C$$

$$= \Sigma(1, 2, 4, 7)$$

(SOP) $= \underbrace{A'B'C + A'B'C' + AB'C'}_{\text{001}} + \underbrace{ABC}_{\text{000}}$

$\begin{array}{c} 001 \\ 010 \\ 100 \\ 111 \end{array}$ } odd no. of 1's as i/p's.

$$f_d(A, B, C) = \overline{(A' + B' + C)} \cdot \overline{(A' + B + C')} \cdot \overline{(A + B' + C')} \cdot \overline{(A + B + C)}$$

$$\therefore = \Pi(6, 5, 3, 0)$$

$$= \underline{\underline{\Pi(0, 3, 5, 6)}}$$

$$\underline{\underline{\Sigma(1, 2, 4, 7)}}$$

for odd no. of i/p's EX-OR and EX-NOR are having equality relation hence, odd i/p EX-OR is self dual function.

$$A \oplus B \oplus C = A \odot B \odot C \leftarrow \text{odd i/p.}$$

Ques. What is the dual of $f(A, B) \in \underline{A' + B}$.

$$\rightarrow f_d(A, B) = A'B$$

$$\underline{\Sigma(0)}$$

$$\underline{\Sigma(1) = \Pi(0, 2, 3)}$$

$$\downarrow \underline{\underline{\Pi(2) = \Sigma(0, 1, 3)}}$$

NON-ortho.
NON-self

- * The number of minterms must be equal to number of maxterms
- and the condition

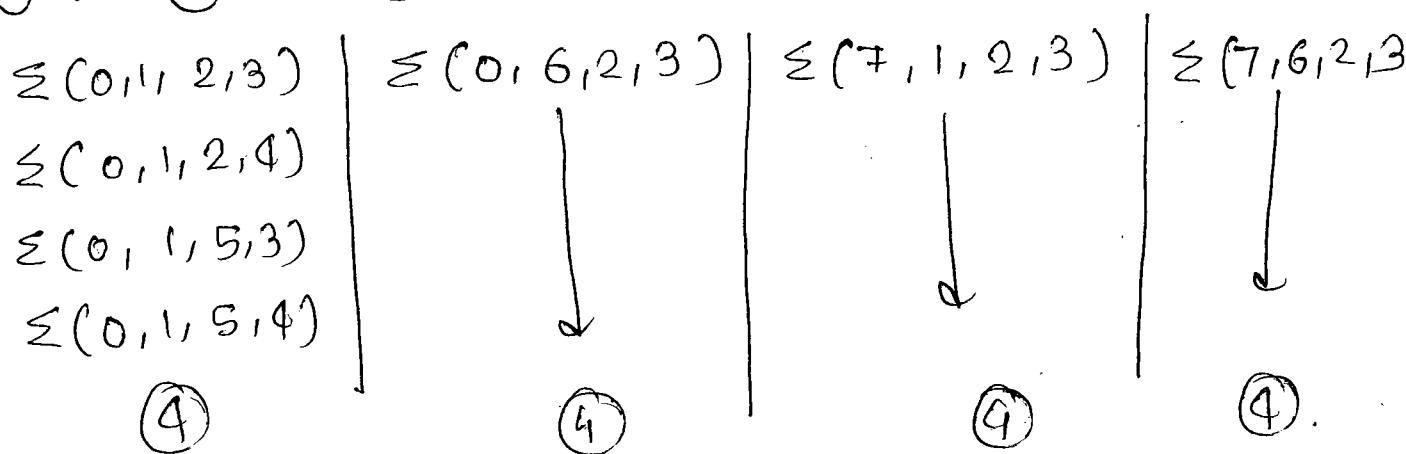
$$f(x_1, x_2, \dots, x_n) \neq f(x_1^1, x_2^1, \dots, x_n^1)$$

(0,7) (1,6) (2,5), (3,4)

$$f(ABC) = (0,2,1,6)$$

- How many self dual functions are possible with 3 boolean variables.

③ 3 ④ 8 ⑤ 16 ⑥ 64.



groups
 $= 2$ $= 2^4 = \underline{\underline{16}}$

NOTE: with 4 variable $\rightarrow 2^8 = 256$

No. of dual functions

n variable $\rightarrow 2^{n-1}$

n variable $\rightarrow 2^n$ combinations

$\frac{2^n}{2} \text{ groups.} = 2^{n-1}$

* The complementation is done similarly to that of dual only exception is even variables also replaced with their complementation.

$$\text{AND} \rightleftharpoons \text{OR}, \quad 0 \rightleftharpoons 1,$$

variable \rightleftharpoons complemented variable.

$$f(A, B, C) = A' + BC' + AC$$

$$f_d(A, B, C) = A \cdot (B + C') \cdot (A + C)$$

$$f_c(A, B, C) = A \cdot (B' + C) \cdot (A' + C')$$

i.e. $f'(A, B, C) = f_d(A', B', C')$
OR

$$f_d(A, B, C) = f'(A', B', C')$$

Ques. How many boolean functions are possible with n boolean variables such that.

$$f(x_1, x_2, \dots, x_n) = f'(x_1', x_2', \dots, x_n')$$

- (a) n (b) 2^n (c) 2^{2^n} (d) $2^{2^{n-1}}$



$$f(x_1, x_2, x_3, \dots, x_n) = f'(x_1', x_2', \dots, x_n')$$

$$= f_d(x_1, x_2, \dots, x_n)$$

$$\boxed{2^{2^{n-1}}}$$

{self dual function}

NOTE: If the condition is not given then the ans

$$\underline{\underline{= 2^n}}$$

Ques How many boolean functions are possible with 3 boolean variables such that the o/p containing either 4 minterms or 6 minterms.

→ 3 variables $\rightarrow 2^3$ combinations = 8

$$\therefore 8C_4 + 8C_6 = \frac{8*7*6*5}{4*3*2} + 8C_6 = 70 + 28 = \underline{\underline{98}}$$

$$8C_0 + 8C_1 + 8C_2 + 8C_3 + 8C_4 + 8C_5 + 8C_6 + 8C_7 + 8C_8 = 2^8$$

$$\underline{\underline{2^2 = 2^3 = 256}}$$

$$\text{atmost 3 minterms} = 8C_0 + 8C_1 + 8C_2 + 8C_3$$

$$\text{exactly 4 minterms} = 8C_4$$

∴ with 3 variables

$$\boxed{2^n C_0 + 2^n C_1 + \dots + 2^n C_{2^n} = 2^{2^n}}$$

Ques A boolean funcⁿ is said to be TALE if it contains equal no. of minterms and maxterms how many TALE funⁿs are possible with n boolean variables.

$$\boxed{2^n C_{2^{n-1}}}$$

e.g. 3 variables

$$\boxed{8C_4}$$

MIXED LOGIC FUNCTIONS

- $n \rightarrow$ No. of variables
- $2 \rightarrow$ Nature of variables
- $2 \rightarrow$ (Boolean functions)
- Nature of function

Ques. How many boolean functions are possible with 2, Ternary variables.

$$\rightarrow 2^3 = 2^2 = 512$$

$n^n \rightarrow$ no. of n-ary fun^{ns} possible with n variables with n-valued algebra.

BOOLEAN LAWS

The boolean laws are used for minimization of a function, the minimized funⁿ does not change the func. functionality but reduces h/w.

The sop is said to be minimized if it reduces the no. of terms and no. of literals in each term.

1) Identity Law \Rightarrow

" Identical operation on identical variable give unique result ",

$$f: X + X + X + X = X \quad (\text{here } + \text{ follows law})$$

$$f_d: X \cdot X \cdot X \cdot X = X \quad (\cdot \text{ (and) also follows identity law})$$

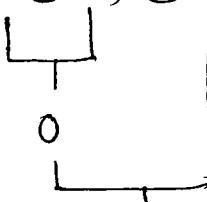
* NAND does not obey identity law

NOR also does not follows id. law (coz NOR is dual of NAND)

$$\begin{array}{l} \text{NAND} = \overline{\square} \\ \text{NOR} = \overline{\vee} \end{array}$$

Ques. check whether XOR follows identity law or not.

$$(\dots (((x \oplus x) \oplus x) \oplus x) \dots) = \underline{x}$$

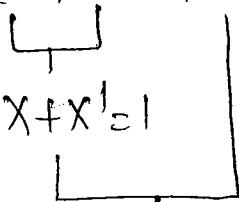

 x
 $x' + x \cdot x'$
 $= x$.

NOTE: XOR as well as XNOR does not follow identity law.

Q. A new boolean operation \$ is defined as
 $A \$ B = A + B'$. does \$ follows identity law?



$$(\dots (((x \$ x) \$ x) \$ x) \dots) = \checkmark$$


 $x + x' = 1$
 $1 + x' = 1$

follows Identity law
indeed, even

AB' also follows
identity law

2) Commutative law \rightarrow "order of inputs does not (position) change functionality"

$$f: \underline{A+B=B+A}$$

$$f_d: \underline{AB=BA}$$

"All symmetric functions satisfies commutative law"

a) NAND, NOR, X-OR, X-NOR are symmetric functions.

\hookrightarrow boolean fun. is said to be symmetric if \rightarrow

i) It is not getting changed on permutation of I/P.

e.g. $f(A,B,C) = \underline{AB+BC+CA}$ } follows
 $f(B,A,C) = \underline{BA+AC+CB}$ } commutative law.

$$\begin{aligned} f(A,B,C) &= (A' B C + B' C A) \\ &= (A' + BC)(B' + CA)(C' + AB) \end{aligned}$$

2) A boolean fun. said to be symmetric if it contains all possible terms for each a-number &.

a number of a term is the total number of ones in its binary pattern.

e.g. A number of 8 (1000_2) is 1.

A number of 7 (111_2) is 3.

(check whether the following fun. is symm. or not?)

$$f(A,B,C) = \Sigma (3,5,6,7)$$

$$\text{a_num of 3} = (011) = 2$$

$$5 = (101) = 2$$

$$6 = (110) = 2$$

$$7 = (111) = 3$$

total terms with a-num 3 must be

$$\underline{\underline{= nC_3 = 3C_3 = 1}}$$

→ function with 4 variables 2 must be

$$= \underline{3C_2 = 3}.$$

Ques. check whether the follo. funⁿ satisfies commutative law or not.

$$f(A, B, C, D) = \sum(0, 1, 2, 4, 8, 15)$$
$$\begin{array}{cccccc} \downarrow & \downarrow & \downarrow & \downarrow & \downarrow \\ 0 & 1 & 1 & 1 & 1 & 4 \end{array}$$

$$f_C_0 = 1 \leftarrow q_num = 6$$

$$f_C_1 = 4 \leftarrow q_num = 11$$

$$f_C_4 = 1 \leftarrow q_num = 4$$

} this is symmetric
 $\underline{\underline{= S_{0,1,4}(A,B,C,D)}}$

$$S_2(A, B, C, D) = \sum(3, 5, 6, 9, 10, 12)$$
$$\begin{array}{cccccc} \downarrow & \downarrow & \downarrow & \downarrow & \downarrow & \downarrow \\ 0011 & 0101 & 0110 & 1001 & 1010 & 1100 \end{array}$$

$$(f_2 = 6)$$

$$= AB'CD + A'BC'D + A'B'C'D + AD'C'D + AB'C'D + ABC$$

Ques. check whether the follo. funⁿ is symm. or not if not what will be the min no. of terms are to be added

$$f(A, B, C, D) = \sum(0, 1, 2, 7, 8, 13, 15)$$
$$\begin{array}{cccccc} \downarrow & \downarrow & \downarrow & \downarrow & \downarrow & \downarrow \\ 0 & 1 & 1 & 0 & 1 & 3 \end{array}$$

$\underline{\underline{+ \sum(4, 11, 14)}}$
terms to be added

$$f_C_0 = 1$$

$f_C_1 = 4$ ← terms but here are only 3 terms

∴ hence it is not symm.

3) Associative laws "order of operation is not going to change functionality."

$$f: (A+B)+C = A+(B+C)$$

$$fd: \underline{(AB) \cdot C = A \cdot (BC)}$$

$$A \uparrow (B \uparrow C) = (A \uparrow B) \uparrow C$$

↓ ↓
 $(B'+C')$ $(A'+B')$
 ↓ ↓
 $A' + B \cdot C$ \neq $AB + C'$

23/07/2012

* NAND and NOR does not follow associative law.

Ans. Commutative, associative but not distributive

a) OR b) AND c) NOR d) X-NOR
dual → both can't be ans.

$$\text{e.g. } A \oplus (B \oplus C) = (A \oplus B) \oplus C.$$

$$A=0$$

$$\text{LHS} = B \oplus C$$

$$\text{RHS} = B \oplus C$$

$$A=1$$

$$\text{LHS} = (B \oplus C)' = \underline{(B \oplus C)} = B'C' + BC$$

$$\text{RHS} = (B' \oplus C) = (B')'C + (B')C'$$

$$= BC + B'C' = \underline{B \oplus C}$$

$$x \oplus y = x'y + xy'$$

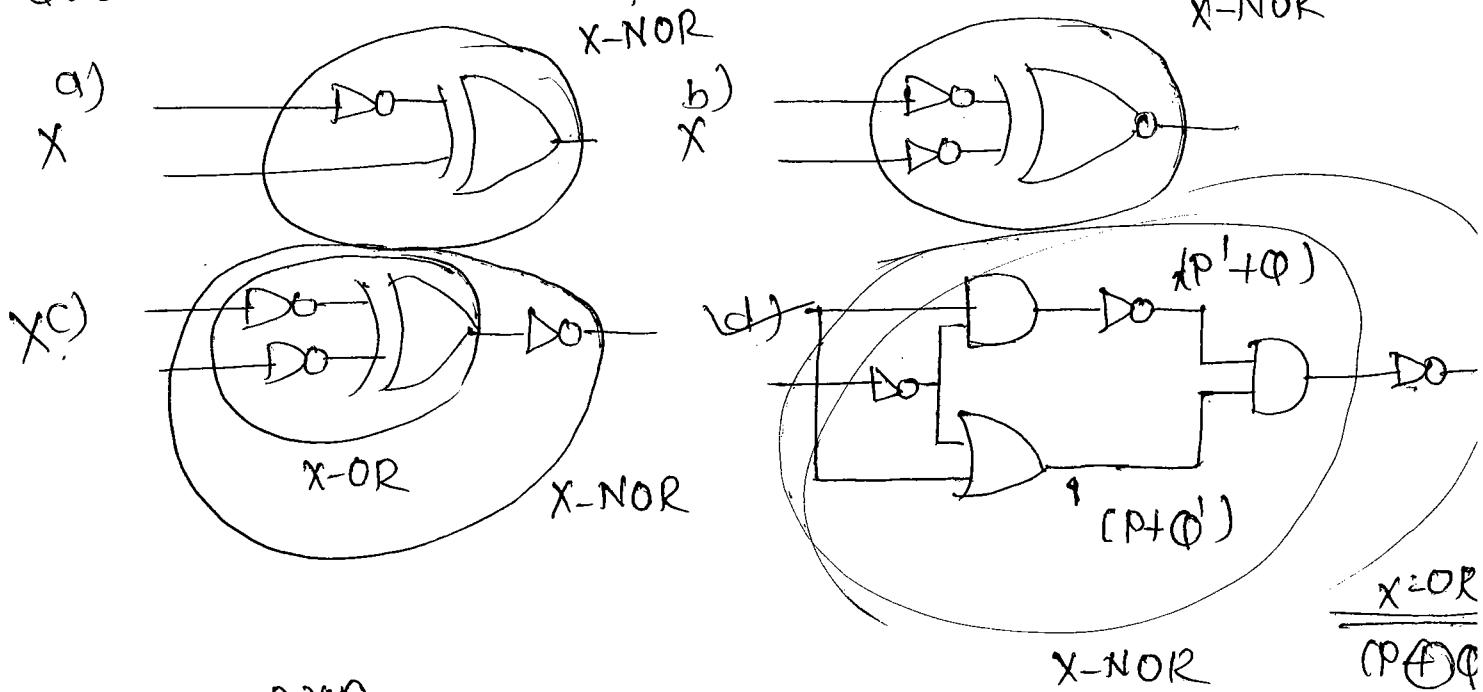
⇒ X-OR as well as X-NOR follows associative law.

$$\begin{aligned} 0 \oplus p &= p; \quad 1 \oplus p = p' \\ p' \oplus q &= p \ominus q = p \oplus q' \\ p' \oplus q' &= p \oplus q. \end{aligned}$$

$$\begin{aligned} p' \oplus q' &= (p')' q' + p'(q')' \\ &= p q' + p' q \\ &= \underline{\underline{p \oplus q}}. \end{aligned}$$

$$\begin{aligned} 1 \odot p &= p; \quad 0 \odot p = p' \\ p' \odot q &= p \oplus q = p \odot q' \\ p' \odot q' &= p \odot q. \end{aligned}$$

Ques. Which is NOT a 2 input X-NOR operr.



$$Z = A * B$$

$$\text{Ques. i)} B = Z * A$$

$$\text{ii)} A = Z * B$$

$$\text{iii)} (Z * A * B) = 1$$

✓a) i & ii

✗b) i, ii, iii

✗c) ii & iii

✗d) i & ii

$* \equiv \text{XOR}$

$$\rightarrow \underline{x \oplus x = x'x + xx' = 0} \quad \text{--- (I)}$$

$$x \oplus x' = x'x' + x \cdot (x')!$$

$$= \underline{x' + x = 1} \quad \text{--- (II)}$$

$$x \oplus x' = x + x'$$

$$* = \oplus$$

$$\begin{aligned} i) &= \exists * A \\ &= A * B * A = \boxed{A * A} * B \\ &\qquad\qquad\qquad \boxed{B} \end{aligned}$$

\therefore Statement (i)
is valid.

$$\begin{aligned} ii) &= \exists * B = A * \boxed{B * B} \\ &\qquad\qquad\qquad \boxed{A} \end{aligned}$$

\therefore Statement (ii)
is valid.

$$\begin{aligned} iii) &= \exists * A * B = A * B * A * B \\ &= \boxed{0 * 0} \\ &\qquad\qquad\qquad \boxed{0 \neq 1} \end{aligned}$$

\therefore Statement (iii)
is not valid.

$$\text{Ques. } 2 = A * B = A' B + A B'$$

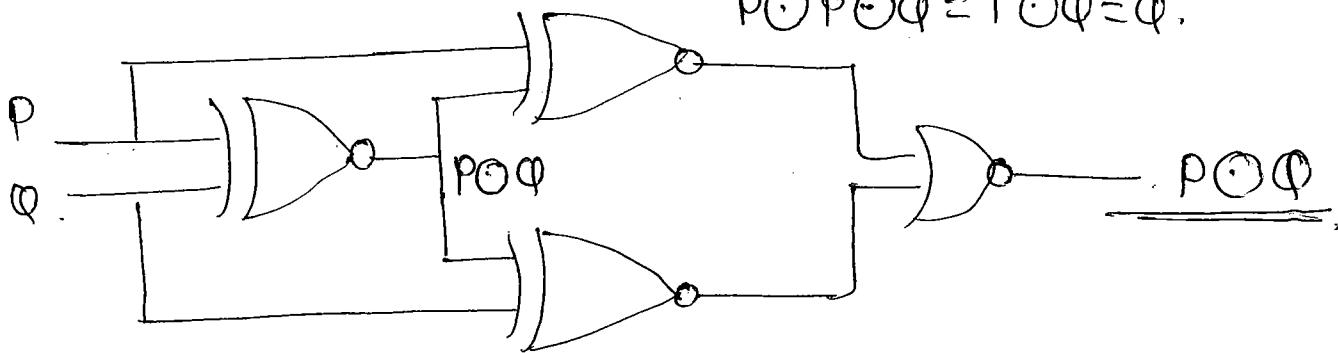
$$\rightarrow \exists * A * 2' * B + \exists * A * B + 2 = 1.$$

$$\begin{aligned} &= \underbrace{\exists * \exists *}_{0} \underbrace{\exists * \exists'}_{1} * \underbrace{A * A}_{0} * \underbrace{B * B}_{0} \end{aligned}$$

$$= \boxed{1} \quad \checkmark$$

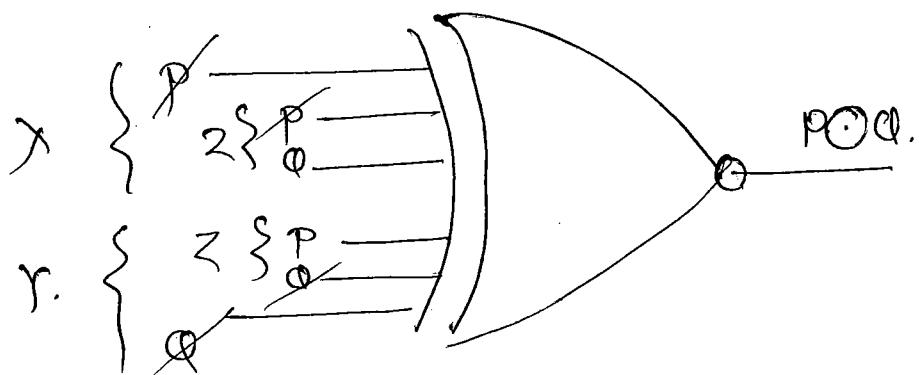
Ques. what is the expression given by following realization?

$$P \oplus P \ominus Q = 1 \ominus Q = Q.$$



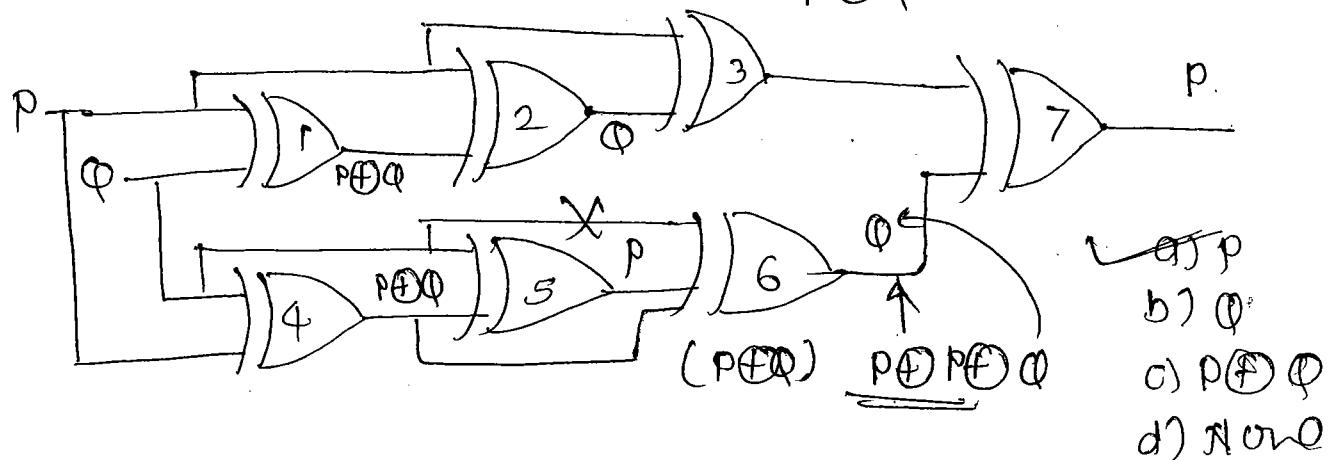
$$Q \ominus P \ominus Q = 1 \ominus P = P$$

- a) NAND b) NOR c) X-OR d) X-NOR



Ques. what is the funⁿ represented by following realization.

$$P \oplus Q$$



- a) $\oplus p$
b) $\ominus p$
c) $P \oplus Q$
d) None

4) Distributive law \rightarrow This law is excessively used
in the minimization.

$$f: A+BC = (A+B) \cdot (A+C)$$

OR distributed on AND.

$$f_d: A \cdot (B+C) = AB + AC$$

Distributive law is available in two forms \rightarrow

i) Combining law -

$$f: A \cdot B + A \cdot B' = A$$

$$f_d: (A+B) \cdot (A+B') = A$$

ii) Absorption law -

$$f: A + AB = A$$

$$f_d: A \cdot (A+B) = A$$

Ques. What is the SOP for the following expression.

- $(P+\bar{Q}+\bar{R})(P+\bar{Q}+R)(P+Q+\bar{R})$.
- a) $\bar{P}\bar{Q}+\bar{R}$ c) $\bar{P}Q+R$
 b) $P+\bar{Q}R$ ~~d) $P+\bar{Q}\bar{R}$~~

$$\boxed{\begin{aligned} & (x+y)(x+z) \cdot (x+w) = x + \cancel{x(y)} \quad y \neq w \\ & \end{aligned}}$$

$$= P + \underline{(\bar{Q}+R)(\bar{Q}+R)(Q+\bar{R})}.$$

$$= P + \left(\cancel{\bar{Q}} (Q+\bar{R}) \right)$$

$$= P + \bar{Q} \cdot \bar{R}$$

Ques. If the follo. funⁿ is minimized, it is free from which variable/variables.

$$(\omega' + x'y' + y\omega + x'y\omega)(\omega' + x' + y')(\omega'y + \omega')$$

- \Rightarrow a) w b) x, y, w ~~c) x, y, z~~ d) w, y, z .

$$\begin{array}{c}
 (\omega' + x'y' + yw + x'y\omega) (\omega' + x' + y') \boxed{(\omega'y + \omega')} \\
 \downarrow \quad \downarrow \quad \downarrow \\
 \omega' \left(\frac{\omega' + x' + y'}{\omega' + y'} \right) \rightarrow \left(\frac{\omega' + x' + y'}{\omega' + y'} \right) \\
 \hline
 A(A+B) \\
 \downarrow \\
 \boxed{\omega' (\omega' + x' + y')} \\
 \hline
 \therefore \frac{A \cdot (A+B)}{\omega' + x' + y'} \\
 \downarrow \\
 \underline{\omega'}
 \end{array}$$

Q16. What will be the minimal expression represented by following.

$$A + \overline{AB} + \overline{A}\overline{B}C + \overline{A}\overline{B}\overline{C}D$$

- a) 1 b) A+B+C d) A+C+D ~~e) A+B+C+D.~~

$$A + \bar{A}X = (A + \bar{A}) \cdot (A + X)$$

$$\cancel{\omega' + x'y} = \omega' + x'y \quad (\cancel{C + \bar{C}D} = C + D)$$

$$\cancel{x' + y} = x' + y$$

$$A + \cancel{AB} + \cancel{ABC} + \cancel{BCD} = A + B + C + D$$

$$PQ + (P' + Q')\omega y z = PQ + \underline{\omega y z} \quad (\because P\bar{Q} = (P' + Q'))$$

De Morgan Laws →

Used to converting universal
realization into basic realization and basic
realiz'n into univ. realiz'n

$$\textcircled{1} \quad \overline{AB} = \overline{A} + \overline{B}$$

$$\textcircled{2} \quad (\overline{A+B}) = \overline{A} \cdot \overline{B}$$

AND-OR realiz'n is replaced with NAND-NAND
realiz'n

$$\boxed{\text{AND-OR} \Leftrightarrow \text{NAND-NAND}}$$

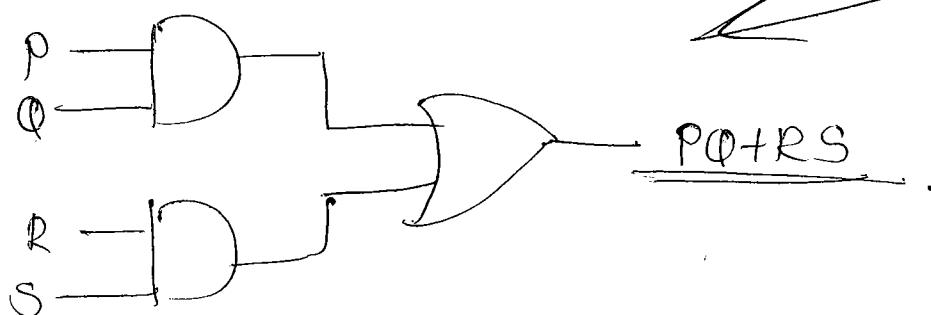
NAND-NAND is suitable for SOP.

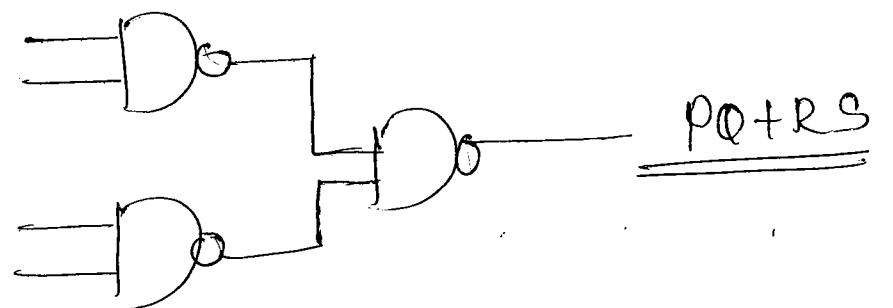
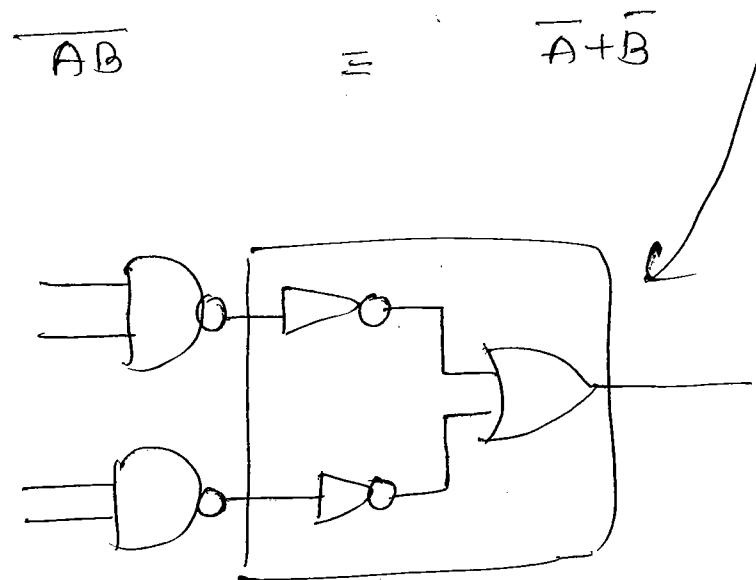
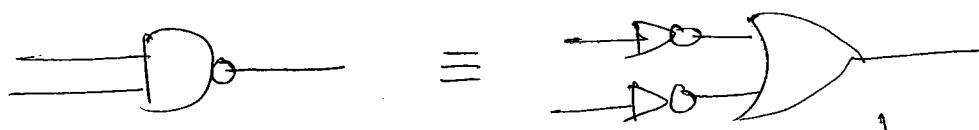
$$\boxed{\text{OR-AND} \Leftrightarrow \text{NOR-NOR}}$$

NOR-NOR

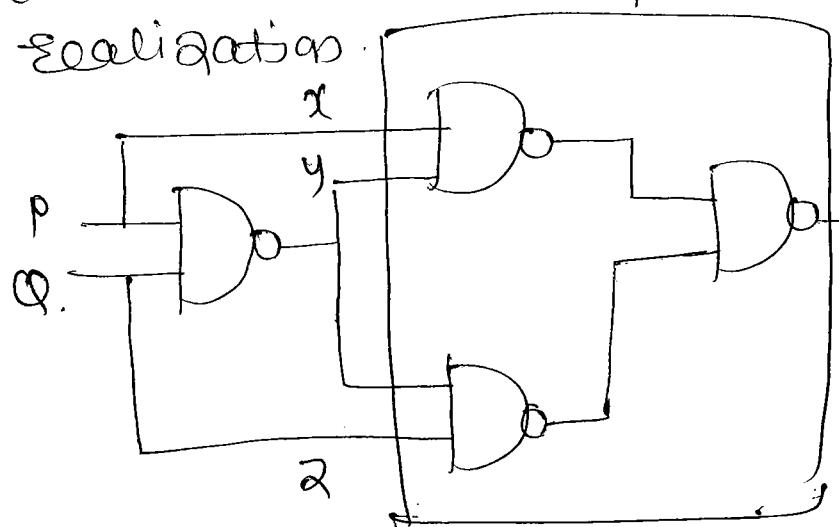
AND → OR

↓ pos





Ques. What is the func? represented by following realization.



$$\bar{x}\bar{y} + \bar{y}\bar{z}$$

a) NAND

b) NOR

~~c) X-OR~~

d) X-NOR

$$= \bar{x}y + y\bar{z}$$

$$= P(P' + Q') + (P + Q')Q$$

$$= P\bar{Q}' + P'\bar{Q} = P \oplus Q$$

NAND-NAND

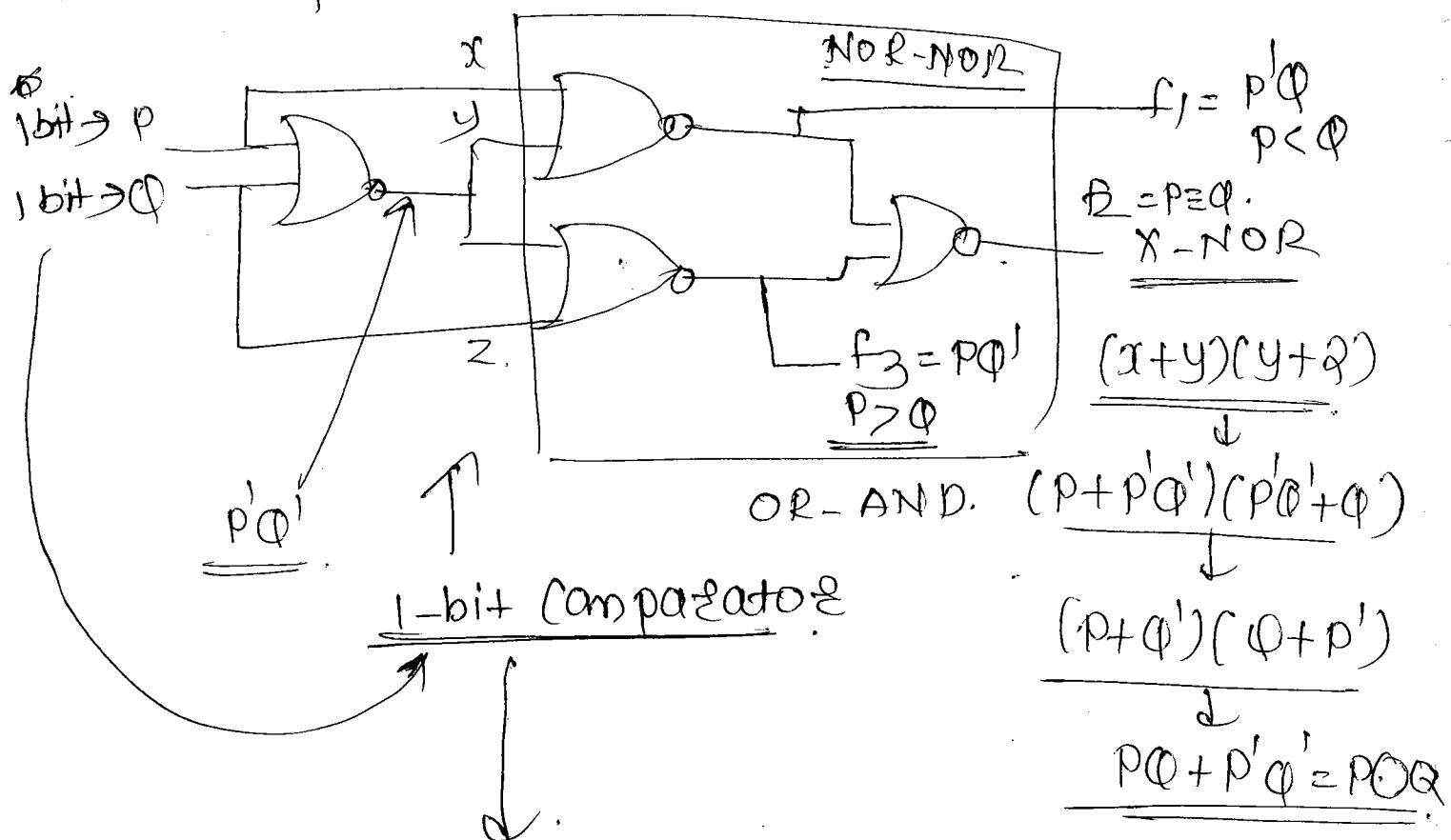
↓

AND-OR

4 NAND
gates are
needed.

* Min. no. of two i/p NOR gates req. to implement.

$$X-NOR = 4.$$

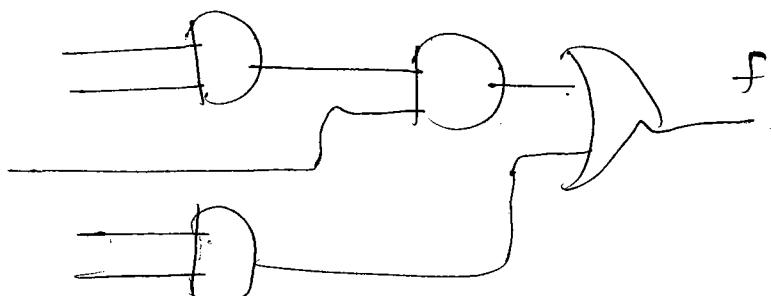


A	B	f ₁	f ₂	f ₃
0	0	0	1	0
0	1	1	0	0
1	0	0	0	1
1	1	0	1	0

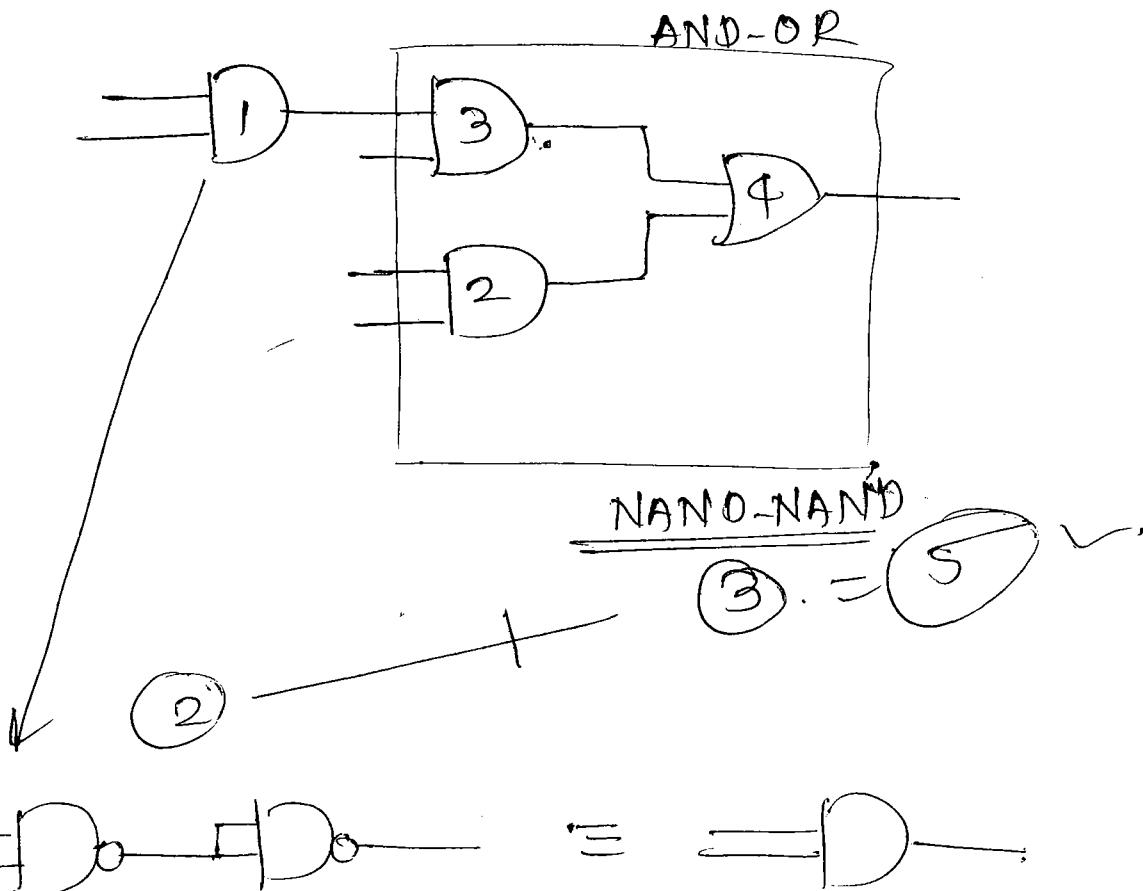
When f₁ is high
it is forcing
f₂ & f₃ = low.

Ques →

What will be the min. no. of 2 i/p-NAND gates req. to realize the following fun?



- (A) 5
- (B) 5
- (C) 6
- (D) 7



Ques. what will be the min. no. of 2-input NOR gates are reqd. for exp. 2.

$$f(A, B, C) = A + BC$$

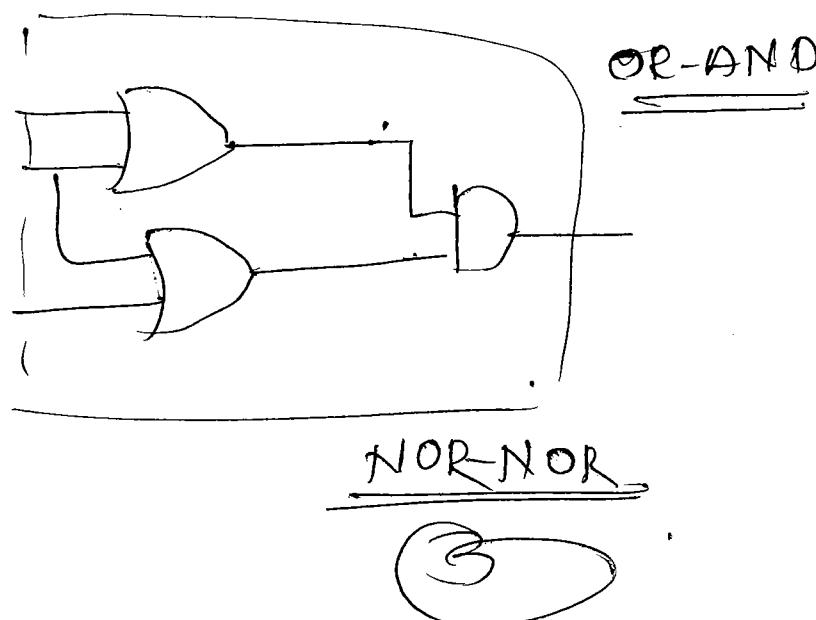
$$\rightarrow = \underline{(A+B)} \cdot \underline{(A+C)}$$

a) 2

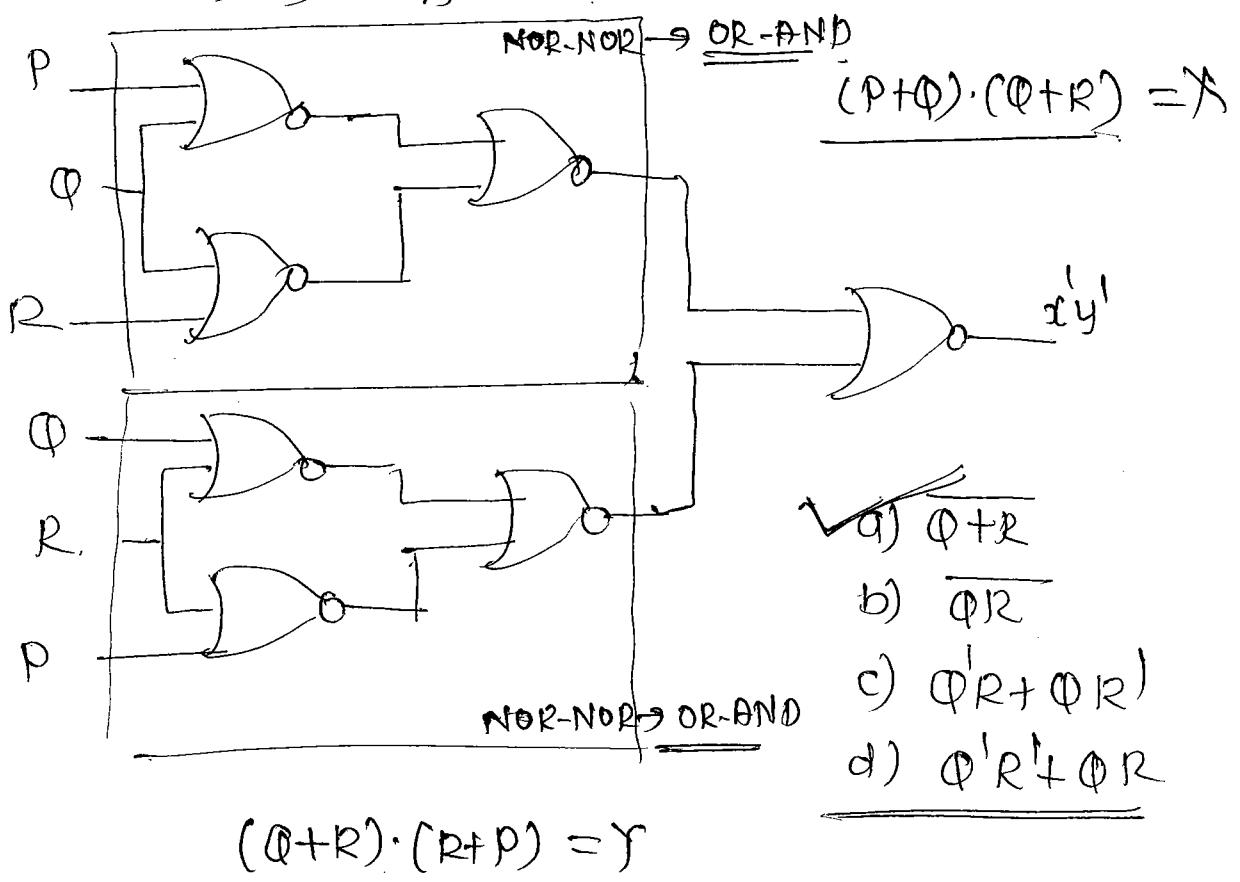
~~b) 3~~

c) 4

d) 5.



Ques. what is the expression represented by following NOR gate combination.



$$X' = P'Q' + Q'R'$$

$$Y' = Q'R' + R'P'$$

$$\begin{aligned} X'Y' &= (A+B)(A+C) \\ &= A + AC \\ &= (Q'R' + P'Q' \cdot R'P') \end{aligned}$$

$$= (\underline{Q'R'} + \underline{P'Q'R'})$$

$$A + AB$$

↓

$$Q'R'$$

$$\underline{\underline{Q+R}}$$

Compensation Thm

this theorem is aimed to identify and remove the redundant term.

The removal of redundant term is not changing the functionality but reducing the b/w.

$$AP_1 + A'P_2 + \boxed{P_1P_2} \text{ redundant}$$

$$\underline{= AP_1 + A'P_2}$$

$$\text{if } P_1P_2 = 0 \quad \underline{\text{LHS} = \text{RHS}}$$

$$\text{if } P_1P_2 = 1 \Rightarrow P_1 = P_2 = 1$$

$$\underline{\text{LHS} = A + A' + 1}$$

$$\underline{\text{RHS} = A + A' = 1}$$

$$\underline{\text{LHS} = \text{RHS}}$$

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$$f: AP_1 + A'P_2 + P_1P_2 = AP_1 + A'P_2$$

$$fd: (A+P_1) \cdot (A'+P_2) \cdot (P_1+P_2) = (A+P_1)(A'+P_2).$$

Redundant

Ques.

$$(x'y'z)(y'xz)(z'xy)$$

- (a) $xyz + x'y'z'$
- (b) $(x+y+z)(x'+y'+z')$
- (c) $\overline{xyz} + \overline{x'y'z'}$
- (d) None

$$\Rightarrow (x+y)(x'+z)(y'+x)(y'+z)(z'+x)(z'+y)$$

Compensation w.r.t x.

↓

$$\frac{(x+y')(x'+\underline{z}) \cancel{(y'+z)} (x+z') (x'+\underline{y}) \cancel{(z'+y)}}{(x+y')(x'+z) (x+z') (x'+y)}$$

\uparrow redundant.

\uparrow Redundant.

$$\frac{(x+y')(x+z') (x'+y) (x'+z)}{\downarrow \qquad \qquad \downarrow}$$

$$\frac{(x+y'z') + (x'yz)}{\downarrow}$$

$$\underline{(xz+xy'z')}$$

Limitation of boolean theorems →

Even though the boolean th^m supports the minimization, it is difficult to know which boolean law is to be used when. If the substitution is not proper the expression may result expanded form instead of minimized.

It is not sure that the result \textcircled{H} is in the minimal most form (redundant) or,

the result can be further minimized (redundant). These problems are solved using K-maps.

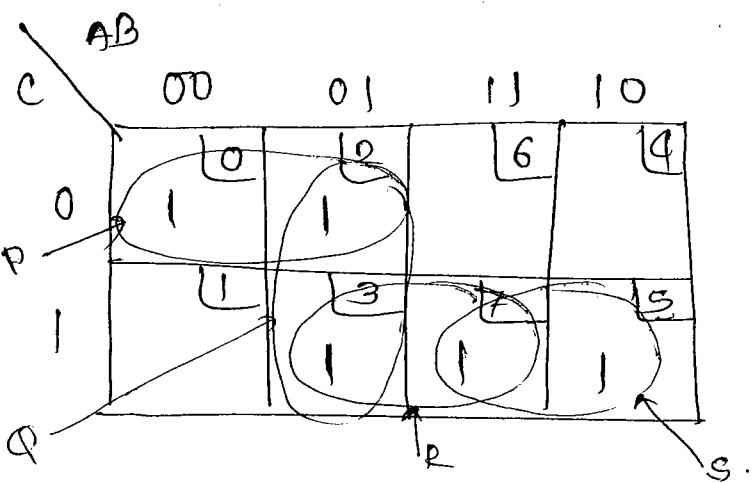
K-map \rightarrow Karnaugh maps.

- i) The K-map is a pictorial description of Truth table.
- ii) It provides systematic way of minimization of SOP or POS
- iii) n-variable map contains 2^N cells, each of which is addressed by Gray code.
- iv) The adjacent minterms or maxterms result prime implicant (pair, Quad, Octet).
- v) The prime implicant cannot be the subset of another. It becomes essential if it exclusively covers at least one minterm or maxterm.
- vi) The minimal expression is also called as minimal cover.

$$\text{minimal cover} = \boxed{\begin{array}{l} \text{All essential} \\ \text{prime implicants} \end{array}} + \begin{array}{l} \text{prime implicant} \\ \text{needed to cover} \\ \text{remaining minterms} \end{array}$$

- vii) If the no. of variables are 6 or 7 identification of prime implicants is difficult and hence, minimization is also difficult.

The variable entant map (VEM) can be used as an alternative.



$$f(A,B,C) = \Sigma(0,2,3,5,7)$$

A	B	C	f
0	0	0	1
0	0	1	0
0	1	0	1
0	1	1	1
1	0	0	0
1	0	1	1
1	1	0	0
1	1	1	1

PIM \rightarrow n product of unchanged input
denotes variables \in $\{0,1\}$

- How many PIMs ? ④ (P,Q,R,S) pairs.
- _____ ESPIMs ? ② (P,S).
- _____ Redundant PIMs ? ③ (Q,R)
- _____ minimal Expressions ? ② .
- _____ Liteseqs ? ⑥

* 0 has been exclusively covered by only P.
 Thus, P is ESPIMs.

* but Q and R are covering more \rightarrow (Redundant.)
 * 5 \rightarrow . thus S is ESPIMs.

minimal Expressions \rightarrow $P \rightarrow 0,2$. } ④.
 covered by. $S \rightarrow 5,7$

8 is not covered.

so, choose any one from Q and R.

\therefore (1) st minimal cover = $\frac{P+S+Q}{P+S+R} \rightarrow \underline{\{0,2\} \{5,7\} \{2\}}$

(2) nd _____ = $P+S+R$

indeed $P+S+Q+R$ covers all (m) exp. but does not satisfy minimality.

P' 's & s. prime Imp $\rightarrow A'C' (\because B$ is getting changed)

Q' 's $\rightarrow A'B (\because C$ is getting changed)

R' 's $\rightarrow BC$

S' 's $\rightarrow AC$

\therefore ESSPIM = $A'C', AC$

Redundant = $A'B + BC$

\therefore minimal exp. = $A'C' + AC$

$$\begin{array}{c} \underline{A'C' + AC + A'B} \\ \underline{A'C' + AC + BC} \end{array}$$

minimal
Literals \rightarrow $\underset{\text{is SOP}}{\underset{\downarrow}{(A'C')^2 + (AC)^2 + (A'B)^2}} = 6$

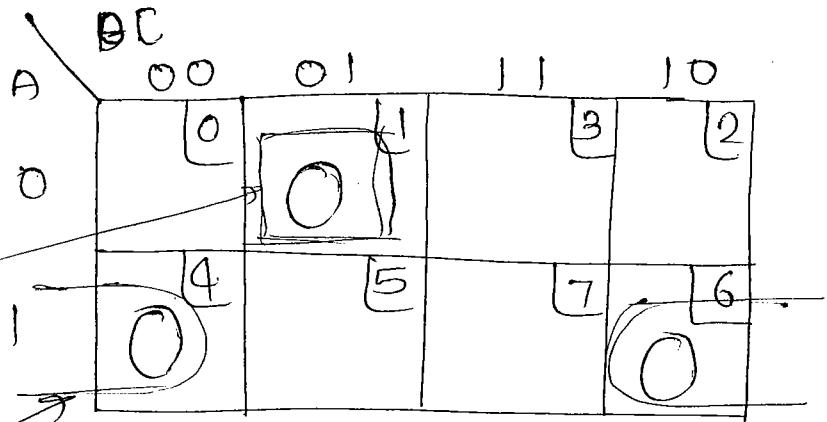
but

$\underset{\text{OR}}{(A'C')^2 + (AC)^2 + (BC)^2} = 6$

otherwise

$A'(C' + B) + AC = 5$

Ques. minimize the above \rightarrow follo. I pos minim'



$$f(A, B, C) = \overline{AB}C + AB\bar{C} + A\bar{B}\bar{C}$$

PIMs \rightarrow ②

EssPIMs \rightarrow ②

Redundant \rightarrow 0

minimal exp. \rightarrow ① \rightarrow POS = $X \cdot Y = \underline{(A+B+C')(A'+C)}$

Literals \rightarrow ⑤.

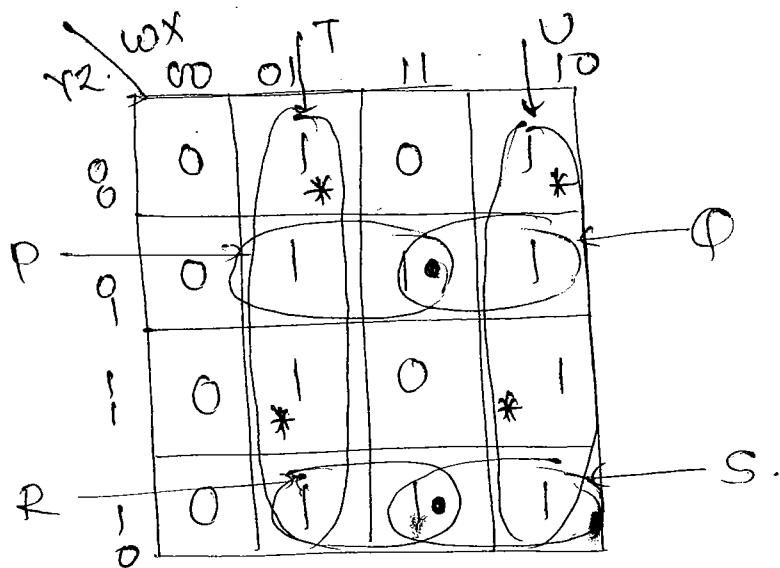
for POS sum of PIM is \rightarrow sum of unchanged input variables ($\because 0$)

for X \rightarrow $A+B+C'$

for Y \rightarrow $A'+C$.

Ques. how many minimal expressions represented by following K-map?





- (a) 1
- (b) 2
- (c) 4
- (d) 6.

PIMs \Rightarrow 6 ($2Q, 4P$)

SSPIMs \Rightarrow 2 ($T \& U$)

Redundant \Rightarrow 4 (P, Q, R, S)

minimal SOP \Rightarrow ④

Literals \Rightarrow ~~10~~ ⑩

$$T+U+\underbrace{Q}_{m_x} + \underbrace{S}_{m_y} \Rightarrow \begin{array}{l} T+U+P+R \\ T+U+P+S \\ T+U+Q+R \\ T+U+Q+S \end{array} \quad \left. \begin{array}{l} T+U+P+R \\ T+U+P+S \\ T+U+Q+R \\ T+U+Q+S \end{array} \right\} ④$$

$$\begin{aligned} &\Rightarrow \omega'x + \omega x' + xy'q + x'yq' \\ &\Rightarrow \omega'x + \omega x' + xy'q + \omega yq' \\ &\Rightarrow \omega'x + \omega x' + \omega qy' + x'yq' \\ &\Rightarrow \omega'x + \omega x' + \omega qy' + \omega yq' \end{aligned}$$

Ques. above what is the relation b/w no of literals in SOP and POS.

- SOP contains \downarrow extra literal than POS.

- ① SOP $\xrightarrow{\quad}$ POS
 ② SOP contains 2 extra letter than POS
 ③ POS $\xrightarrow{\quad}$ SOP
 ✓ ④ both with have same.

In POS for above \Rightarrow

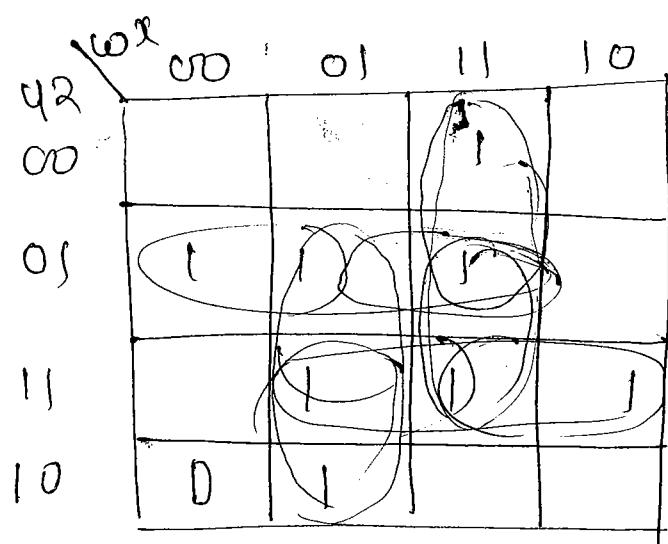
- PIMs \rightarrow ③.
 ESS PIMs \rightarrow ③
 Redundant \rightarrow ⑤.

(Quad) * (single term) & (single)

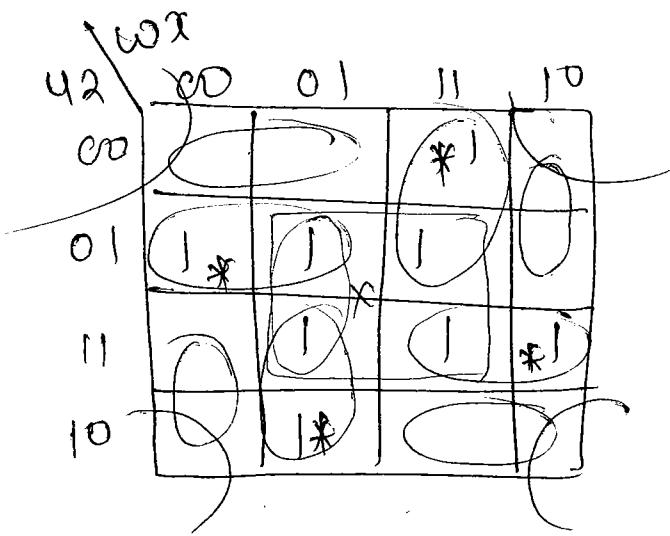
$$② \cdot ④ \cdot ④ = ⑩.$$

$$(w+x)(w'+x'+y+q)(w'+x'+y'+q') \Rightarrow POS.$$

Ques. Which of the following is not a prime impl. w.r.t to the given K-map.



- a) $w'y'q$
 b) $yz'xz$
 c) wyz
 d) $w'xz$.



$$w'x_2 \in x_2$$

Ques. Identify incorrect statement wrt to above.

~~x~~ a) The no. of literals in SOP is equal to no. of literals in POS. ($12=12$)

~~x~~ b) The dual of SOP gives POS

~~x~~ c) both SOP & POS contain 5 PRIM.

~~(x)~~ d) The minimal funⁿ is independent of one variable. (incorrect)

not independent of any variable. (all are diff.)

$$\text{PRIM} \Rightarrow 5$$

SOP

$$w'y'z + wxy' + w'xy + wyz$$

$$\text{fd: } \Rightarrow (w+y+z) \cdot (w+x+y')$$

$$(w'+x+y) \cdot (w+y+z)$$

POS

$$(w+y+z) \cdot (w+x+y')$$

$$(w'+x+y) \cdot (w'+y+z)$$

=

Que. In a hypothetical k-map essential PIM case all the minterms except 2. Each of the left over minterm is covered by 3 diff. redundant PIM. What will be the no. of minimal expr. represented by this map.

- (a) 3 (b) 8 ~~(c)~~ 9 (d) 12.

→

$$\text{All ESPIIM} + \left\{ \begin{matrix} P \\ 02 \\ Q \\ 02 \\ R \end{matrix} \right\} + \left\{ \begin{matrix} S \\ 02 \\ T \\ 02 \end{matrix} \right\}$$

$$\text{All ESPIIM} + mx + my$$

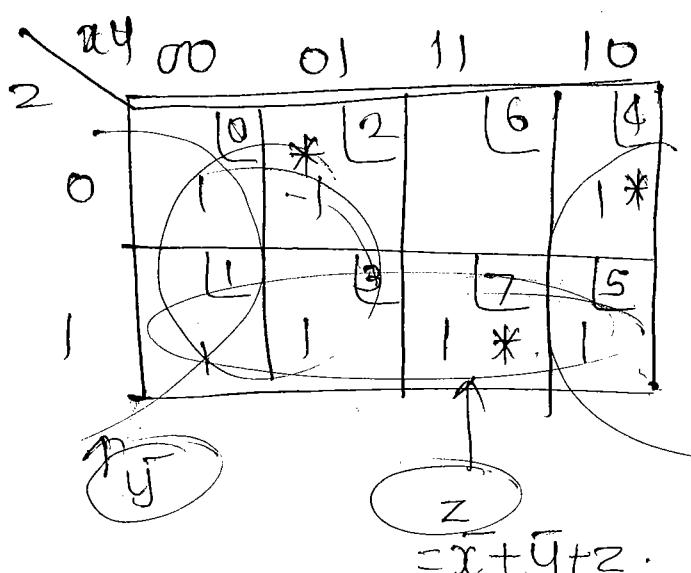
Que. Let $f(x,y,z) = \overline{x} + \overline{y}x + xz$, which one of the following is valid.

a) $\overline{y}x$ is prime impl.

x. b) xz is minterm. → not minterm (since y is not

c) xz is implicant | xz is a coll'n these
of minterms.

Let \overline{y} is PIM.



$$100 \rightarrow x\bar{y}\bar{z} = 4.$$

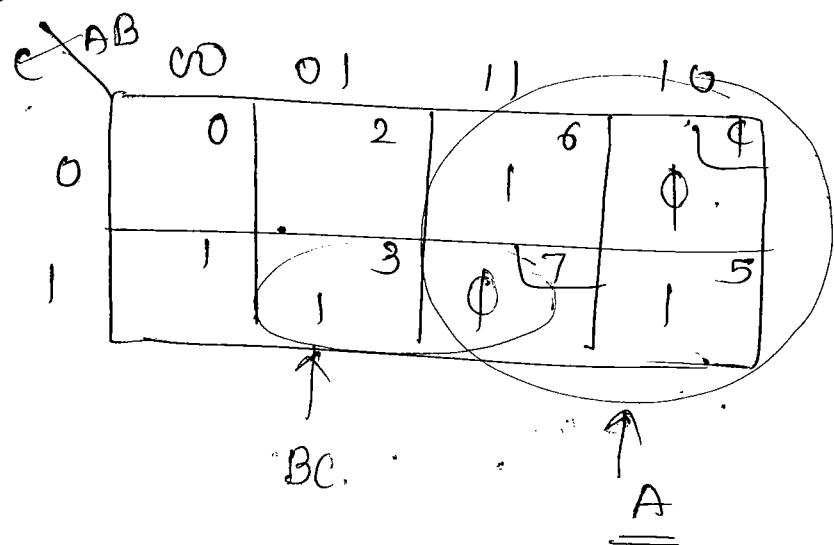
$$= x + \bar{y} + z.$$

Ques. Consider a 3-variable function $f(A, B, C) = \sum (3, 5, 6)$
 It is minimized as $\bar{A} + BC$. Identify the valid statement from below.

- a) The minimization is using 2 seven, 7 as don't care
- b) minimization using 2, 4 as don't care
- c) _____ 4, 7 _____
- d) _____ 2, 4, 7 _____

$$\Rightarrow f = \underline{\bar{A}} + BC$$

(two vars are eliminated
 thus 4 minterms.)



Ques. If P, Q, R represent don't care, what will be their values if the function denoted by the map is minimized.

Ⓐ $\frac{P \quad Q \quad R}{0, 1, 1}$

Ⓑ $1, 1, 1$

Ⓒ $1, 0, 0$

Ⓓ $0, 0, 0$

U_2	00	01	11	10
00	0	0	P	0
01	0	0	1	J
11	1	J	1	J
10	0	R	0	0

" use only minterms and construct the pim "

P, Q, R are useless

they don't support SOP

\therefore treated at 0's.

They are minimizing

POS not SOP

$$SOP \Rightarrow w_2 + y_2.$$

$$POS \Rightarrow \varphi(w+y)$$

Ques.

ab	00	01	11	10
cd	1	1	1	
00	1			
01	x	p		
11	x	q		
10	1	1		x

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a) $\bar{b}\bar{d} + \underline{\bar{a}\bar{d}}$

X b) $\bar{a}\bar{b} + \bar{b}\bar{d} + \bar{a}\bar{b}\bar{d}$

X c) $\bar{b}\bar{d} + \bar{a}\bar{b}\bar{d}$

X d) $\bar{a}\bar{b} + \bar{b}\bar{d} + \underline{\bar{a}\bar{d}}$.

$P=Q=0 ; R=1$

wx

42.	00	01	11	10	φ	is free from
00	1	0 0	1	1	1	one variable (<u>w</u>)
01	0	1 1	1	0	1	b) Two variables
11	1	0 0	1	1	1	c) Three variables
10	1	1 1	1	1	1	d) depend on all

p

→ we should go to pos

→ $f: (x' + y + z)(x + y + z') (x' + y' + z')$ → missing ' w '

↑ ↑ ↑
P Q R

⇒ f' : is also free from \hat{w}'

⇒ f_d : is also free from ' w '

$f(w, x, y, z) = \sum (0, 4, 5, 7, 8, 9, 10, 15)$ is NOT equivalent.

(X) a) $x'y'z' + wx'y + wy'z$ ✓

b) $x'y'z' + w'xy' + wy'z + xz$ X

c) both a & b X

d) Neither a nor b. X

xz

wx

42.	00	01	11	10	φ	$w'y'z'$
00	1	1	4	12	1	$wx'y'$
01	1	1	5	13	1	$xz + w'y'z' +$
11	3	1	7	15	11	$wx'y'$
10	2	6	14	10	1	

* Applications of k-map \rightarrow

- ① consider a new boolean operation $\$$ which is defined as $A \$ B = \overline{A} + B$. f_1, f_2 happens to be three variables functions denoted by the following maps. How many literals are there in the sop of $f_1 \$ f_2$.

PQ	00	01	11	10	
R	0	1	0	0	1
R	1	1	1	0	1

(f1)

PQ	00	01	11	10
R	0	0	1	0
R	1	0	1	0

(f2)

$$\Rightarrow A \$ B = 0 \text{ iff } \underline{A=1 \& B=0} \text{ else,}$$

$$= 1 \text{ else}$$

PQ	00	01	11	10	
R	0	0 ⁰	1 * ¹	1 ¹	0 ⁰
R	1	1 * ¹	0 ⁰	1 * ¹	0 ⁰

$f_1 \$ f_2 \Rightarrow 7$ literals

$$\underline{\text{sop}} \Rightarrow QR' + P\bar{Q} + P'\bar{Q}'R.$$

Ques. Consider the following funⁿs f_1 & f_2 . Obtain the minimal exp. for $f_1 + f_2$, $f_1 \cdot f_2$.

$$f_1(w, x, y, z) = \sum(2, 4, 6, 8, 14) + \sum_{\emptyset}(\underline{2}, \underline{3}, \underline{7}, \underline{13}, \underline{15})$$

$$f_2(w, x, y, z) = \sum(0, \underline{2}, 4, 6, \underline{7}, \underline{15}) + \sum_{\emptyset}(\underline{1}, \underline{3}, \underline{10}, \underline{14})$$

$$\Rightarrow f_1 + f_2 = \sum(0, 2, 4, 6, 7, 8, 14, 15) + \sum_{\emptyset}(1, \underline{5}, \underline{10}, \underline{3}, \underline{13})$$

$$f_1 \cdot f_2 = \sum(0, 4, 6) + \sum_{\emptyset}(14, 12, \underline{7}, \underline{15})$$

or $\Phi = \Phi^{\text{don't care}}$

The term 'x' is the don't care for all the operation iff.

$x \in (\text{maxterm})$ of one funⁿ and

$x \in (\text{don't care list})$.

maxterms of $f_1 = \cancel{\sum(0, 9, 10, 11, 12)}$

maxterms of $f_2 = \cancel{\sum(3, 8, 9, 11, 12, 13)}$

wx	yz	00	01	11	10	w1
00	1	1	1	1	1	
01	1	1	1	1	1	
11	1	1	1	1	1	
10	1	1	1	1	1	

$$\underline{xy} + x'z' + w'$$

1. $\Phi = \Phi$. The term x is the don't care for AND operation iff
 $x \in (\text{minterm})$ of the one funcn &
 $x \in (\text{don't care})$

$$f_1, f_2 = \sum_{\Phi} (0, 4, 6) + \sum_{\Phi} (14, 2, 7, 15) = \text{compl}$$

Ques. Consider follo. three 3 variables funcn share the four pms P, Q, R, S (all of them are paired).

$$f_1(A, B, C) = \sum (0, 1, 3)$$

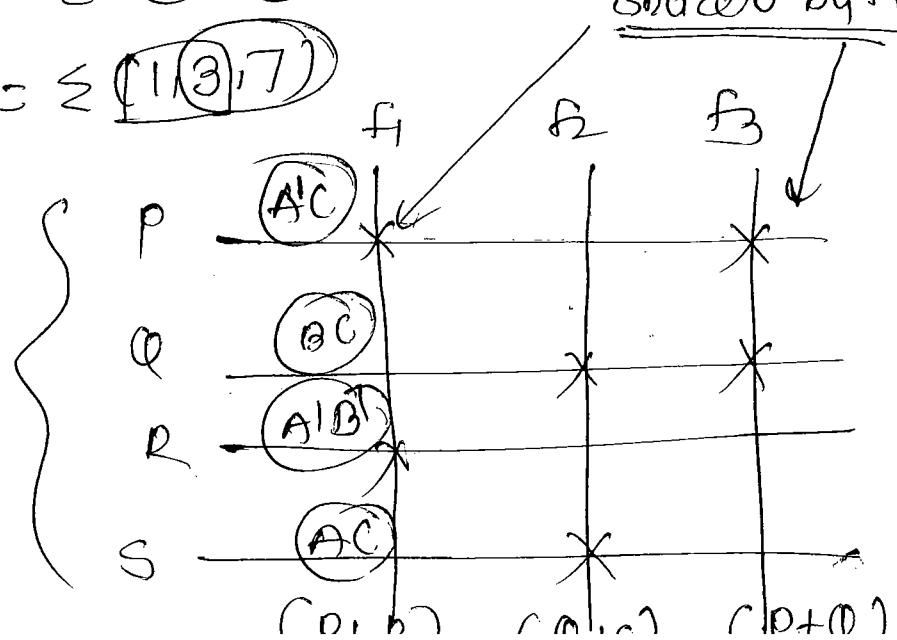
$$f_2(A, B, C) = \sum (3, 5, 7)$$

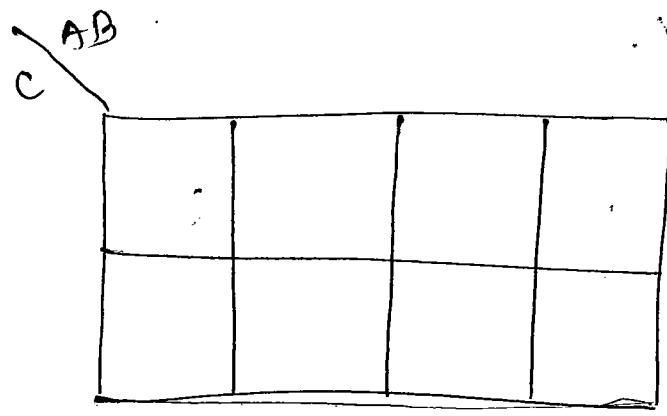
$$f_3(A, B, C) = \sum (1, 3, 7)$$

shared by f_1, f_3 .



pairs





$$P = \frac{1}{2} ABC^T + \frac{3}{2} A'BC$$

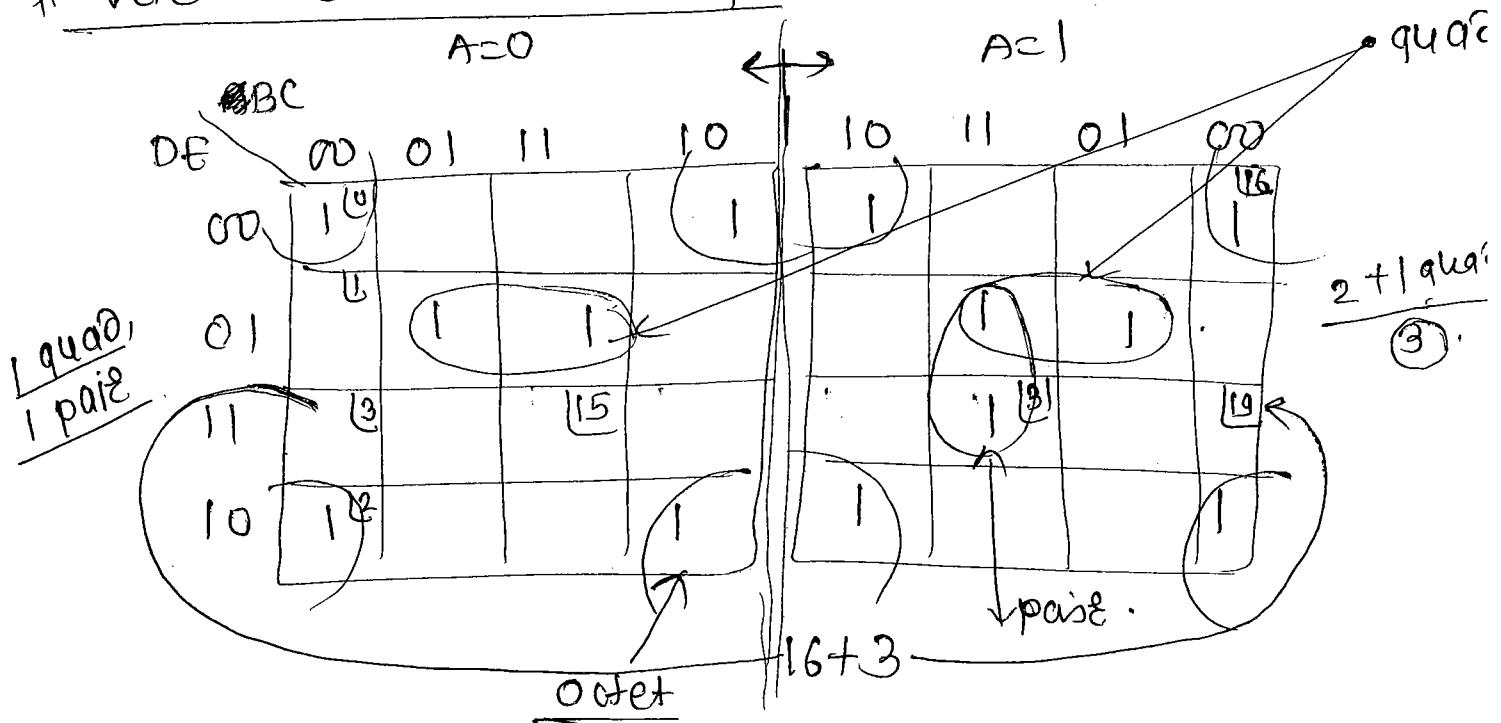
$$P = A'B'C + A'BC = \underline{A'C}$$

$$Q = \frac{1}{2} A'BC' + \frac{3}{2} A'B'C = \underline{BC}$$

$$R = \underline{A'B'} = A'B'C' + A'B'C$$

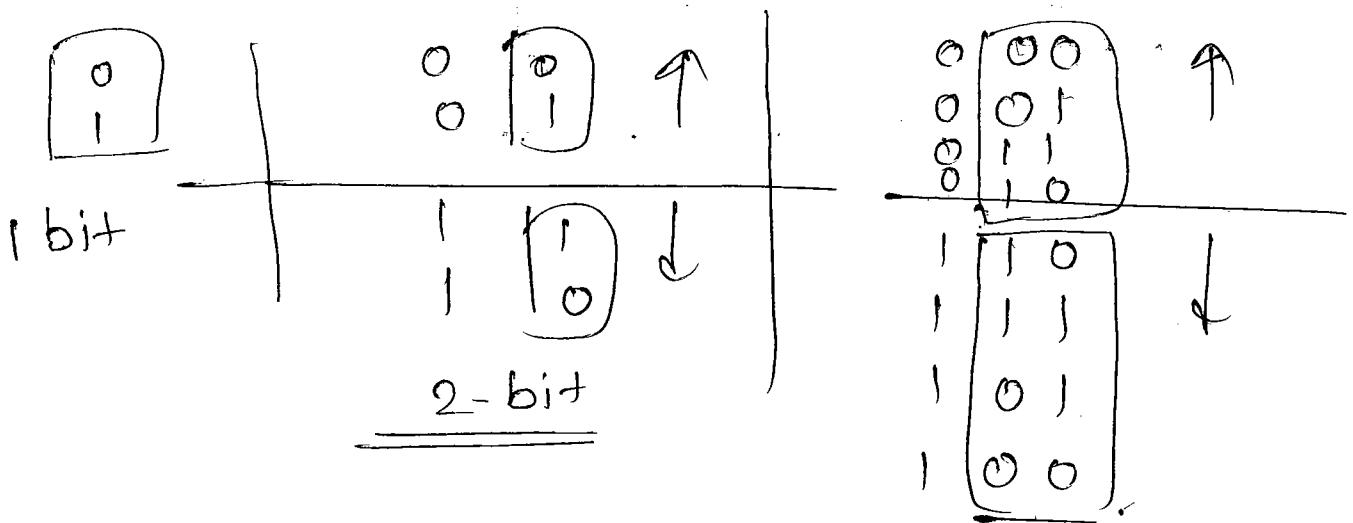
$$S = AB'C + ABC = \underline{AC}$$

* Variable Content Map \rightarrow



Gray Addresses: Unit distance,

cyclic, self - reflective



3-bit

Gray-code

(self-complementary)

$$f(A, B, C, D, E) = \underset{\text{octet}}{C'E'} + \underset{\text{quad}}{CD'E} + \underset{\text{pair}}{ABC'E}$$

④ The VEM is capable of representing higher variable function with lesser variable map. Since contents of the cells can be variables, the map is termed as VEM.

		AB	00	01	11	10
		C	0	D	D	I
A	B	0	0	0	I	I
		1	Φ	0	D	D

VEM $f(A, B, C, D)$

$$\underline{= AC' + C'D + AB'}$$

minimizing pos \rightarrow

- f) make all the variables in the cell as zero obtain sop
- 2) a) set one variable as high and compute sop expression by making previous 1's as don't care
 b) multiply the above sop with concerned variable
- 3) Repeat the step 2 until all the variables in the cell have been covered

Step 1 \rightarrow

		00	01	11	10
		0	0	1	1
		1	φ	0	0
A	B				
C					

$$\underline{\text{sop: } AC'}$$

Step 2a \rightarrow

		00	01	11	10
		0	1	1	0
		1	φ	0	0
A	B				
C					

$$\underline{\text{sop = } C'}$$

Step 2b \rightarrow DC'.

Step 3 \rightarrow

		00	01	11	10
		0	1	0	0
		1	φ	0	1
A	B				
C					

$$2a) A$$

$$2b) A \cdot D'$$

Ques. what will be expression represented by following VGM.

AB		00	01	11	10
C		0	1	D	0
A	B	0	1	D'	D
0	0	1	1	0	0
1	0	1	D'	D	0

$$f(A, B, C, D) = \underline{A'C'} + \underline{A'B'} + \underline{ABD} + \underline{A'D'}$$



AB

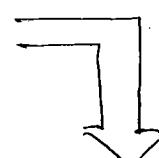
AB		00	01	11	10
C		0	1	D	0
A	B	0	1	D'	D
0	0	1	1	0	0
1	0	1	0	0	0

$$\dot{A}C' + A'B'$$

One consider the follo. 3 variable funⁿ

$f(A, B, C) = \sum(0, 1, 2, 3, 7)$ is denotes by vsm
with the cell contents P, Q, R, S. what will be
their values.

	0	1
0	P (0)	Q (2)
1	R (1)	S (3)



$\Rightarrow P A' B' + Q \cdot A B' @ R \cdot A' B + S \cdot A B$

make pass 1
and perform

Compare

$$f(A, B, C) = [A' B' C'] + [A' B' C] + [A' B C'] + [A' B C] + [A B C]$$

$$\underline{P = C' + C = 1}$$

$$P \cdot A' B' + Q \cdot A B'$$

$$\underline{Q = 0}$$

$$\underline{R = C' + C = 1}$$

$$R \cdot A' B + S \cdot A B$$

$$\underline{S = C}$$

	A	0	1
B	0	1	0
1	1	0	C

$$f(A, B, C) = A' + B C$$

$$ABC \quad ABC \rightarrow \emptyset \cup \{3, 7\}$$

$$0 \emptyset \emptyset \quad \{0, 1, 2, 3\}$$

$$= \{0, 1, 2, 3, 7\}$$

verified

Ques.

		0	1
0	$A \oplus B$	0	
1	1	\overline{AB}	

(func. val. func? presented
in 2 val. map.)

$$\underline{f(A, B, C, D)} = \underline{\frac{d \cdot D}{\text{Step 1}}} + C!(A \oplus B) + D \cdot \overline{AB}.$$

$$= C!D + C!(A'B + AB') + D(A' + B')$$

29 \rightarrow

	1	0
	ϕ	0

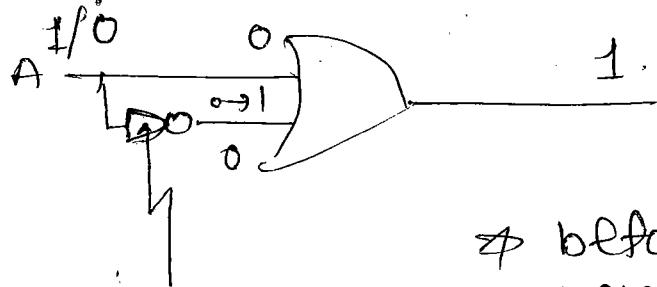
 $C!(A \oplus B)$

0	0
ϕ	1

$D \cdot \overline{AB}$

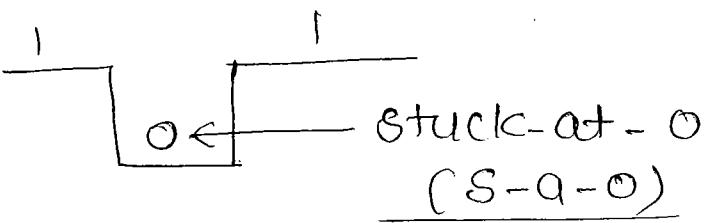
Hazards \rightarrow

$$\underline{A + A' = 1}.$$



\Rightarrow before 5 ns = 0
After 5 ns = 1

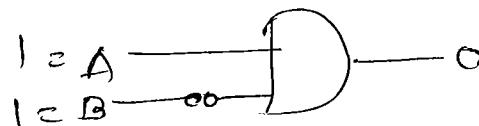
propagation delay $T_{pd} = 5 \text{ ns}$
delay \rightarrow



unequal delays in inputs

$$\underline{A \cdot A' = 0 \quad \{S-A-1\}}$$

- The unclocked delays of the I/O's result temporary hazards.
- The open circuit or short circuit of the terminals result permanent hazards.



- for the same applications between the temporary hazards and permanent hazards are allowed. • In the fault analysis, the test vector is computed to check whether the path is faulty or fault free.
- the test vector is the subset of I/O combinations influencing the concerned path.
- The path sensitization provides test vector.

27/07/2012



Digital Logic

8/11/2012

Hazards → dealing with permanent hazards →

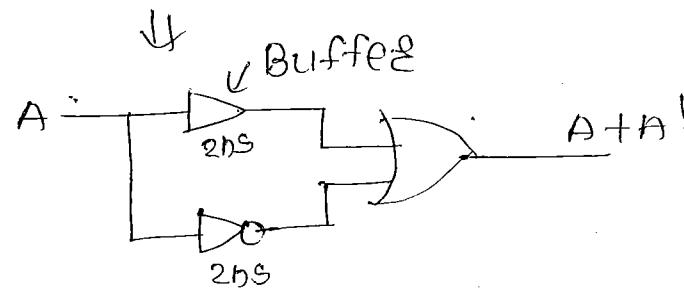
Path Sensitization Technique → ↪

$$f(A, B) = A$$

1. Inactivate all other paths except the tested one.
2. Apply the opposite logic value at tested place with respect to suspected fault.
3. All input combinations satisfying the above form test vector.

Hazards →

- * Temporary →
- Redundancy → add redundant term
 - External delay " so that all i/p's arrive at the same time."



* delay of buffer = delay of inverter

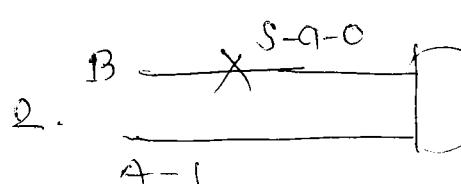
* permanent →

Test vector - subset of i/p combinations which can be used to test whether the path is faulty or fault free.

path sens. Tech →

$$\begin{aligned} 1. \quad f(A, B) &= AB \\ &= 1 \cdot B \end{aligned}$$

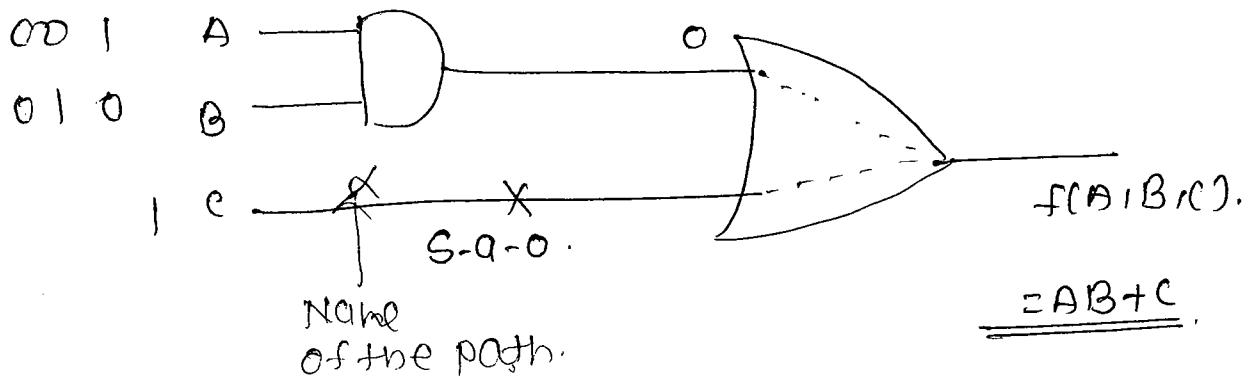
} AND | NAND $\Rightarrow 1$
OR | NOR $\Rightarrow 0$.



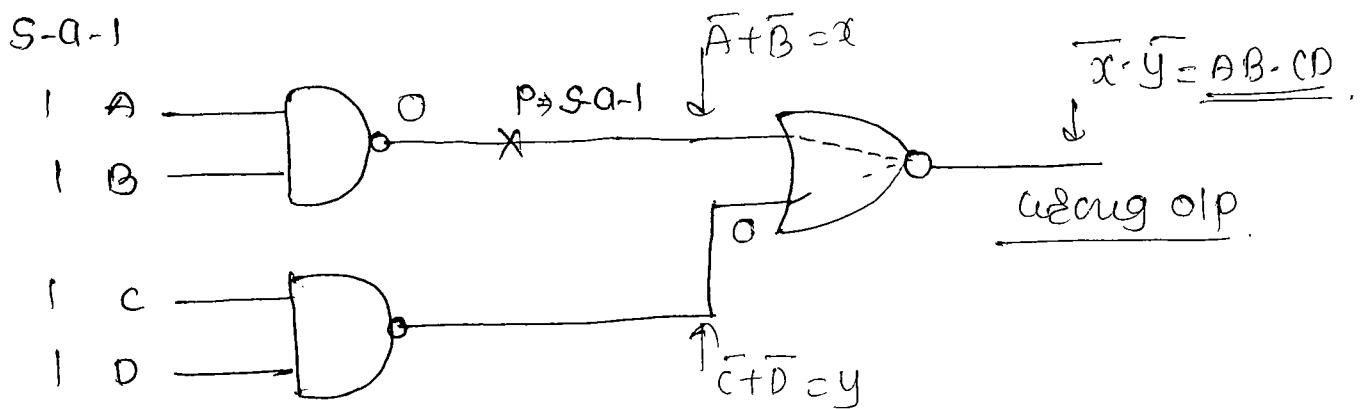
$$f(A, B) = B = 1$$

Test vector set = $\{001, 011, 101\}$
 \Downarrow
 $= \{1, 3, 5\}$.

If we are getting wrong value then there is a problem with it.

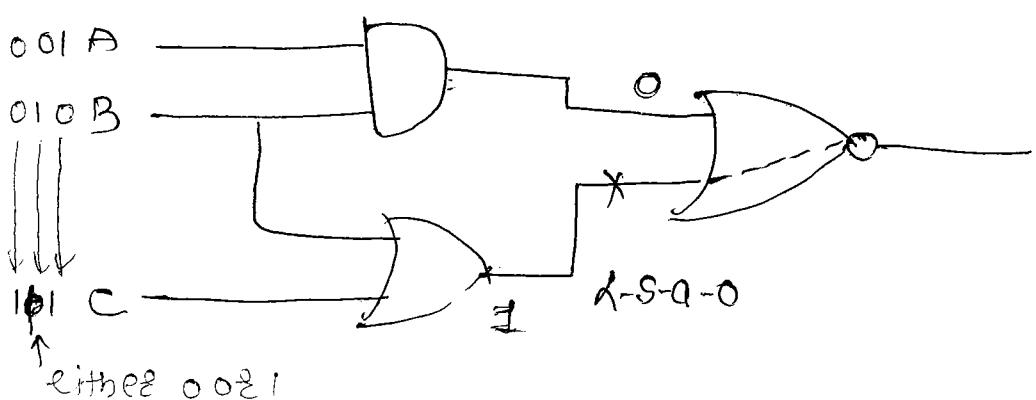


Ques.1) Construct a test vector for path P (stuck at 1)



Test vector = $\{ABCD\}$
 $= \{15\}$.

Ques.2) Con - for $\alpha - \underline{S-a-0}$.

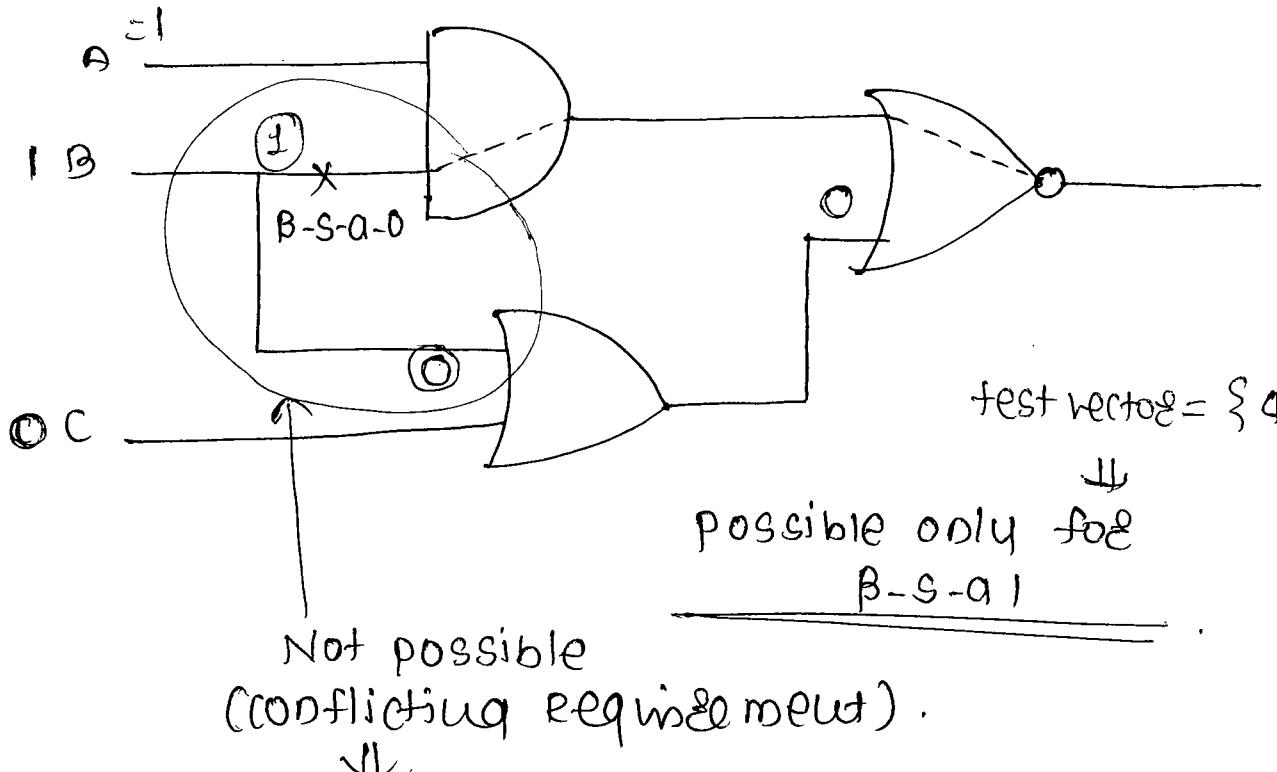


$$\frac{\{001, 101, \underbrace{010}, \underbrace{011}\}}{\phi}.$$

2384

{ 1, 5, 2, 3 }

(Qe.3) β -S-a-O



Limitation of path sensitization tech →

It is not possible to construct the test vector in the presence of conflicting requirements on any i/p.

Fe_2O_3

Combinational Circuits (MSI)

* MUX (many-to-one) Data selector	8x1	{ 8-i/p 1-o/p }
De. MUX (one-to-many) Data distributor	1x4	{ 1-i/p, 4-o/p 2-select }
* Decoder (lessless decomposition)	Address selection	3x8 { 3-i/p, 8-o/p }
Encoder (lossless compression)	Decimal to Binary conversion (Priority Interrupt servicing)	{ 4x2 { 4-i/p, 2-o/p } }

$$N \times 1 \rightarrow [\text{select line} = \log_2 N]$$

MUX \rightarrow [functionally complete operation suitable for SOP].

gate Count of IC

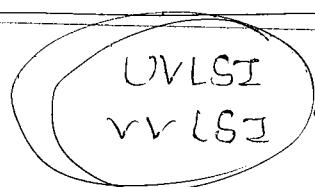


$< 10 \rightarrow \text{SSI}$ (small scale integration)

> 10
 $< 100 \rightarrow \text{MSI} \rightarrow$ major devices (adders, multipliers)

> 100
 $< 1000 \rightarrow \text{LSI}$ (mem. gadgets)

$> 1000 \rightarrow \text{VLSI.} \Leftarrow$ microprocessors

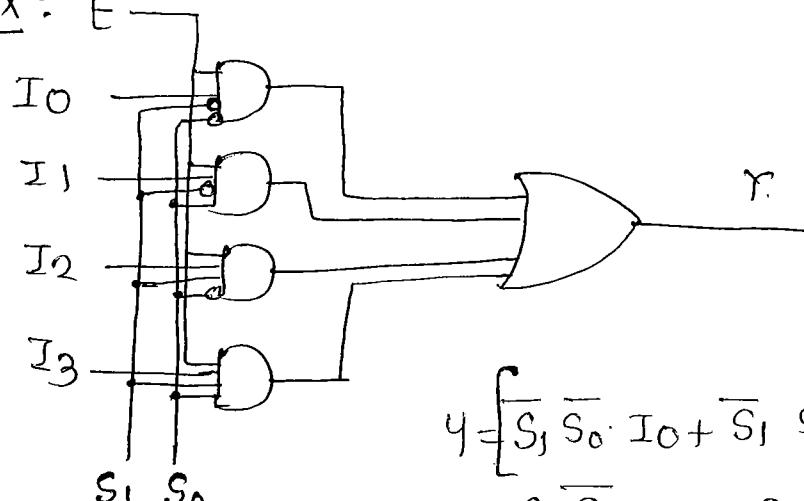


\Leftarrow design people.

- * Multiplexer is a functionally complete operation and used to realize boolean function.
- \rightarrow The internal structure of mux is (AND-OR) combination suitable for SOP.

- In the expansion of multiplexer, multiple levels of basic mux is used.
- The characteristic expression of mux is (to) the function of i/p's and select line.

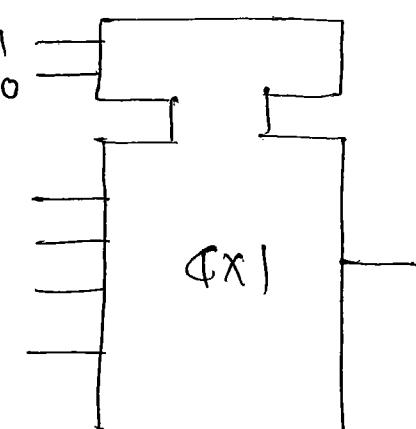
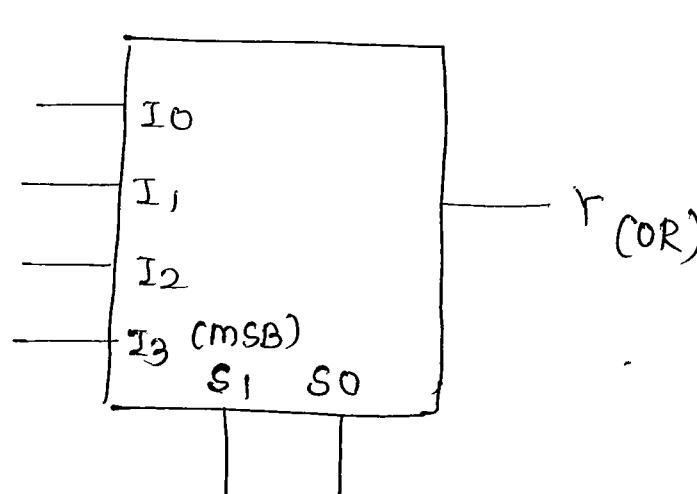
4x1 MUX:



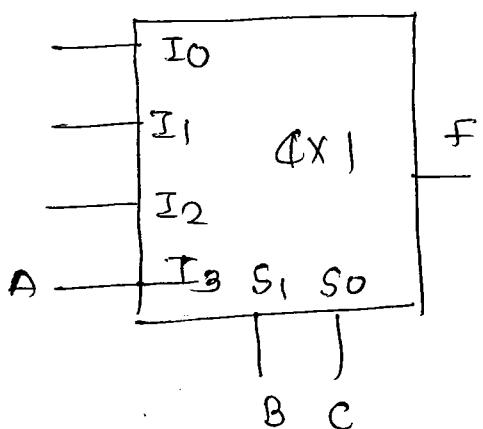
E	S ₁ , S ₀	Y
1	0 0	I ₀
1	0 1	I ₁
1	1 0	I ₂
1	1 1	I ₃
0	0 0	0

$$Y = \overline{S_1} \cdot \overline{S_0} \cdot I_0 + \overline{S_1} \cdot S_0 \cdot I_1 + \\ \underline{\underline{S_1} \cdot \overline{S_0} \cdot I_2 + S_1 \cdot S_0 \cdot I_3} + E \cdot 0$$

* there is no mux action when E=0.



Ques.1) Identify the correct statement w.r.t. the JIP's



- a) f is free from 1 variable
- b) f is dependent of 2 variables
- c) f is independent of all var.
- d) f is dependent of all var

$$f = \overline{B}\overline{C} \cdot A + \overline{B}C \cdot A + B\overline{C} \cdot A + BC \cdot A$$

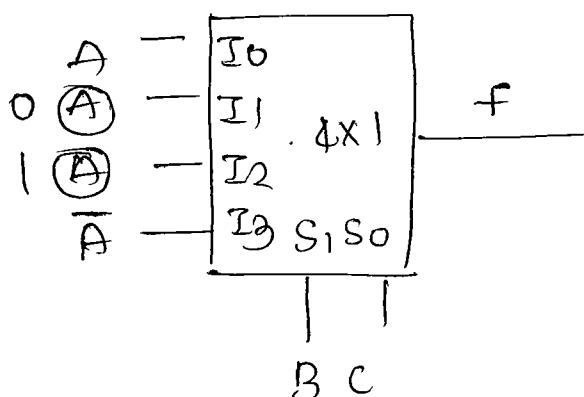
$$(\overline{S_1} \overline{S_0} \cdot I_0 + \overline{S_1} S_0 \cdot I_1 + S_1 \overline{S_0} \cdot I_2 + S_1 S_0 \cdot I_3)$$

$$f = A \left[\frac{\overline{B}\overline{C} + \overline{B}C}{\overline{B}} + \frac{B\overline{C} + BC}{B} \right]$$

$$\boxed{f = A}$$

$\therefore f(A, B, C) = A$ (independent of B & C)

Ques.2) what is the fun. represented by follo. mux
(min terms)



$$= A\overline{B}\overline{C} + \overline{A}B\overline{C} + \overline{A}\overline{B}C$$

$$\Rightarrow f = \overline{B}\overline{C}A + B\overline{C} + BC \cdot \overline{A}$$

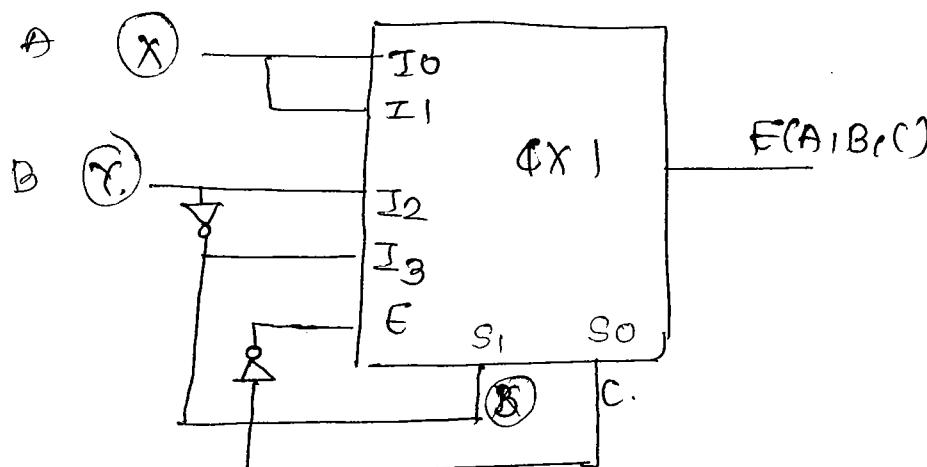
$$f(A, B, C) = \sum(4, 2, 6, 3)$$

$$= \sum(2, 3, 4, 6)$$

(OR)

$$= \overline{\sum}(0, 1, 5, 7)$$

Ques) find funⁿ represented by follo. mon.



~~a) ABC~~

X b) $A + B + C$

X c) $(\bar{A}B + A\bar{B})C$

X d) None



$$S_1 = \bar{B}, \quad S_0 = C,$$

$$E = \bar{C}$$

$$\underline{I_0 = A = I_1}, \quad \underline{I_2 = B}, \quad \underline{I_3 = \bar{B}}$$

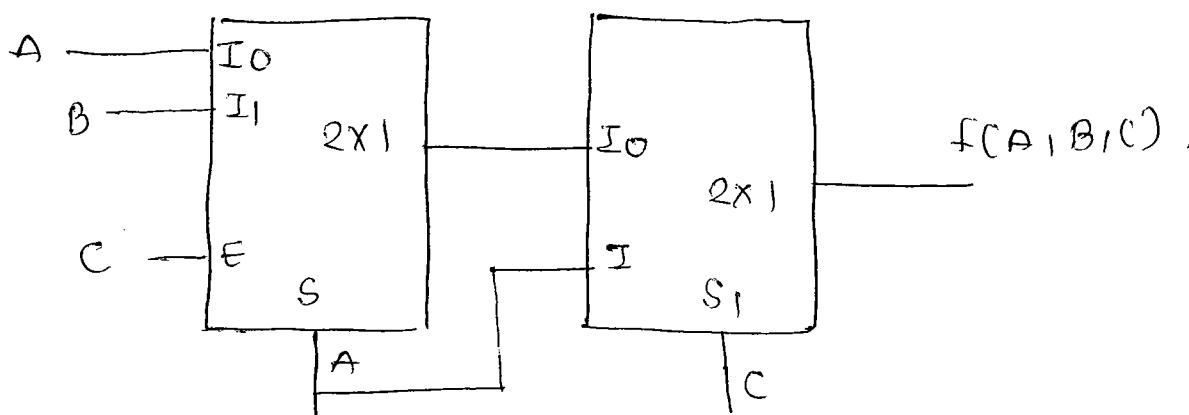
$$= E \left[\bar{S}_1 \bar{S}_0 I_0 + \bar{S}_1 S_0 I_1 + S_1 \bar{S}_0 I_2 + S_1 S_0 I_3 \right]$$

$$= \bar{C} \left[\cancel{\bar{B}\bar{C}A} + \cancel{BCA} + \cancel{\bar{B}\bar{C}B} + \cancel{\bar{B}CB} \right]$$

$$= \cancel{C} \cancel{C} \cancel{C} BA$$

$$= \underline{\underline{ABC}}$$

Ques) find the expression represented by follo. mon



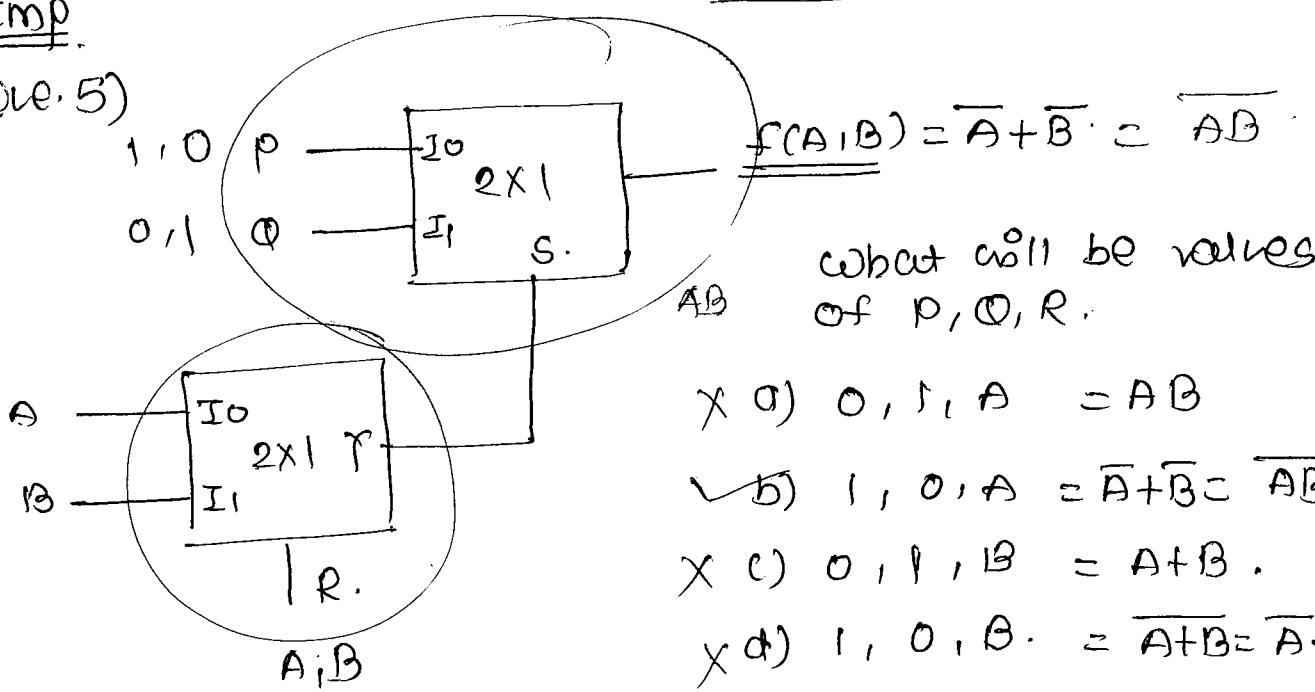
$$\underline{E(\bar{S}I_0 + SI_1)} \leftarrow \text{for } 1^{\text{st}} \text{ mux}$$

if P $\underline{\underline{ABC}}$ } for
if P $\underline{\underline{A}}$ } 2^{\text{nd}} \text{ mux} \quad \underline{\bar{S}I_0 + SI_1}

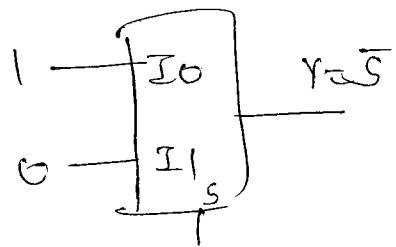
$$\begin{array}{c} C \cdot ABC + C \cdot A \\ \hline ABC + AC \\ \hline AC \end{array}$$

Imp.

Ques. 5)

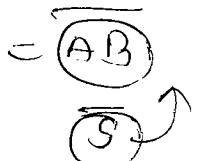


1st
mux



$$\underline{\bar{S}I_0 + SI_1}$$

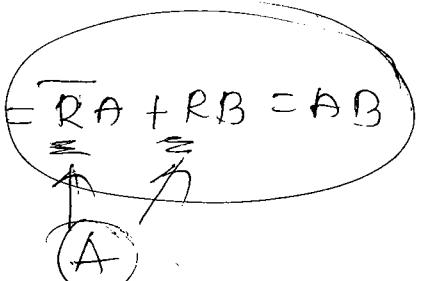
$$f(A, B) = \overline{A} + \overline{B}$$



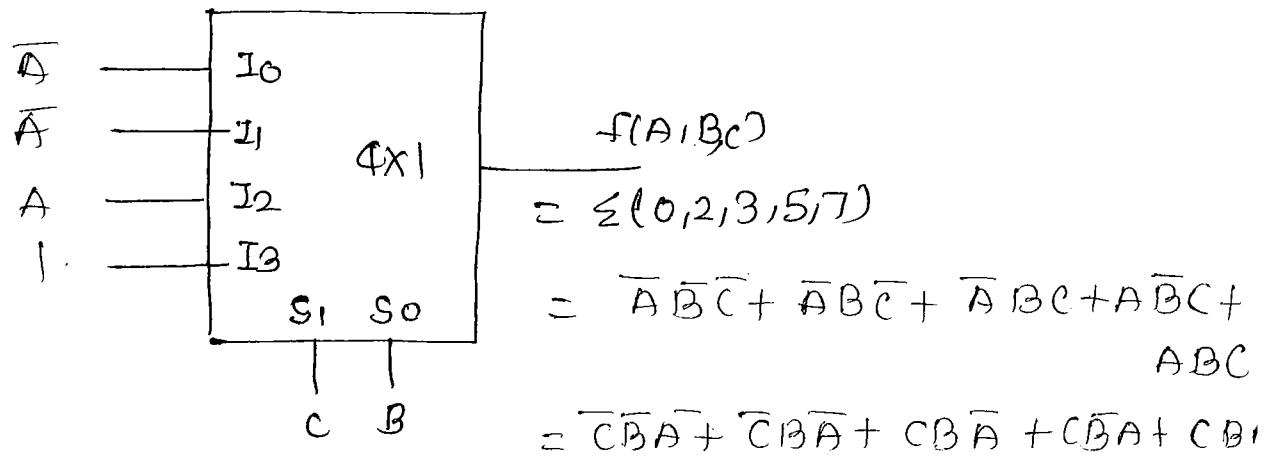
2nd
mux

should be 1, 0

$$\underline{\bar{S}_0 I_0 + S_1 I_1} = \overline{RA} + RB = AB$$



Ques. 6) Consider the follo. funⁿ $f(A, B, C) = \Sigma (0, 2, 3, 5, 7)$,
is to be realized by follo. mux. what will be the
connections for the ilp

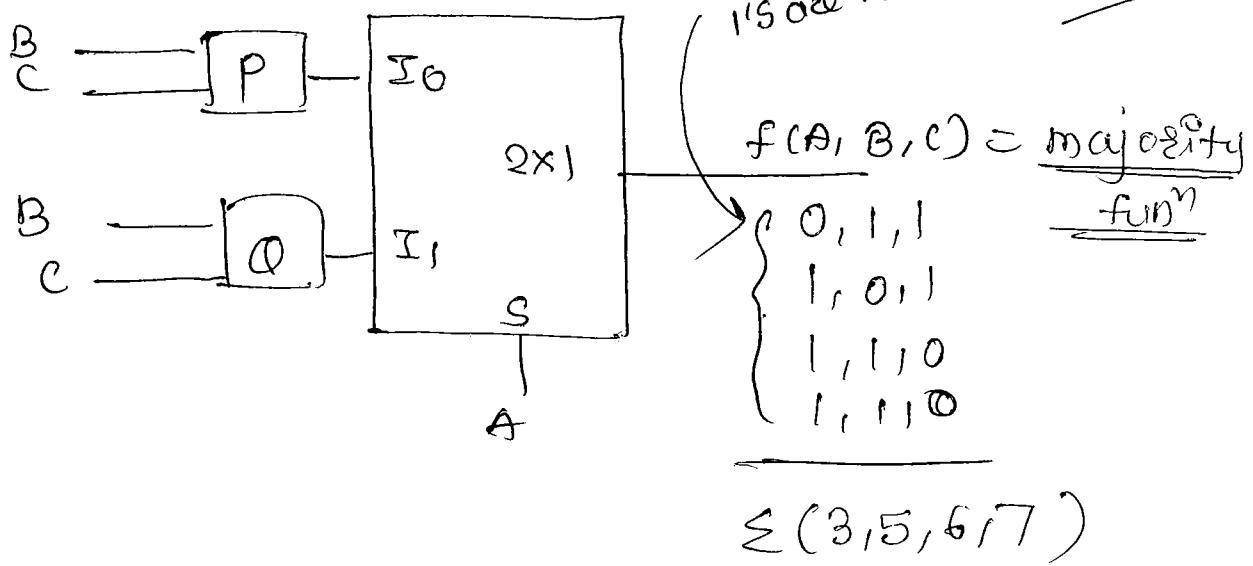


$$= \overline{S_1} \overline{S_0} I_0 + \overline{S_1} S_0 I_1 + S_1 \overline{S_0} I_2 + S_1 S_0 I_3$$

$$= \underline{\overline{C} \overline{B} I_0} + \underline{\overline{C} B I_1} + \underline{C \overline{B} I_2} + \underline{C B I_3}$$

$$\underline{I_0 = \overline{A}}, \underline{I_1 = \overline{A}}, \underline{I_2 = A}, \underline{I_3 = \overline{A}/A} = \underline{\overline{A} + A} = 1$$

Ques. 7) A 3-variable majority funⁿ is to be represented by follo. mux. what will be the express. denoted by P, Q.



- X a) EX-OR , $\frac{P}{Q}$
 X b) EX-NOR , EX-OR
 X c) OR , AND
 d) AND , OR.

AND.

$$\underline{\underline{\overline{A}P + A \cdot Q}}.$$

$$\begin{aligned} P &= \text{AND opes}^N \\ &= BC \end{aligned}$$

$$\underline{\Sigma(3,5,6,7)} = \underline{\underline{\overline{A}BC + \overline{ABC} + AB\overline{C} + ABC}}$$



$$A \cdot Q$$

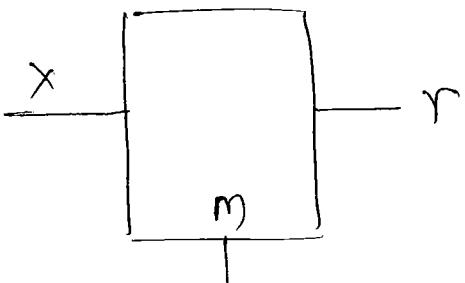
$$\therefore Q = \frac{\overline{B}C + \overline{B}\overline{C} + BC}{\overline{B}C + B}$$

$$\underline{\underline{B+C}}$$

OR

Applications of mux \rightarrow

03/08/2012



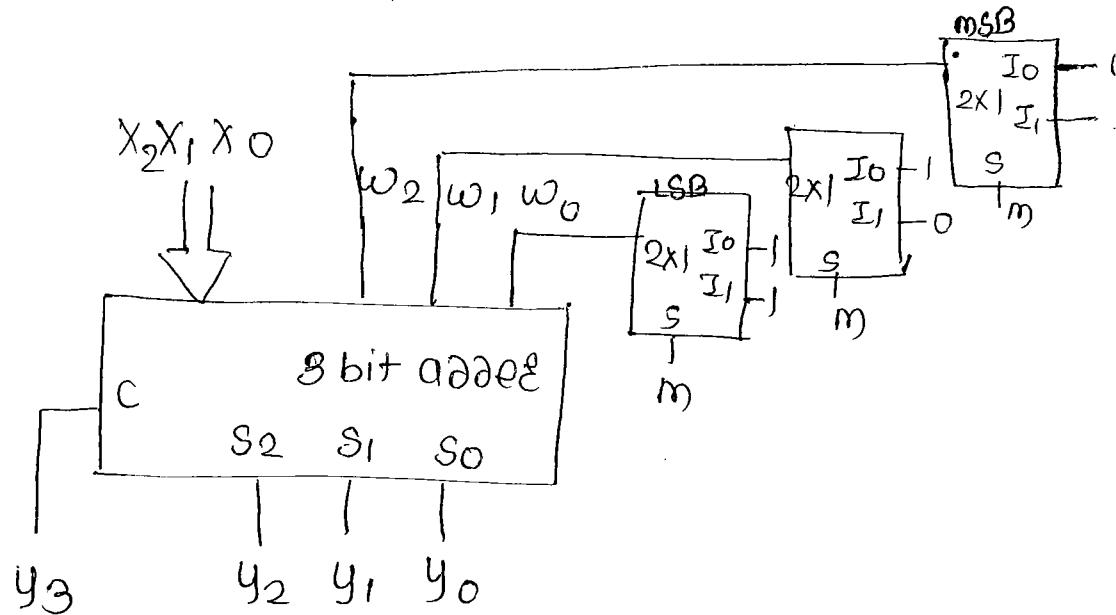
\Rightarrow Binary to $x_5 - 3$ if $m=0$

\Rightarrow $x_5 - 3$ to B if $m=1$.

$$Y = x_5 + 3 \quad \text{if } m=0$$

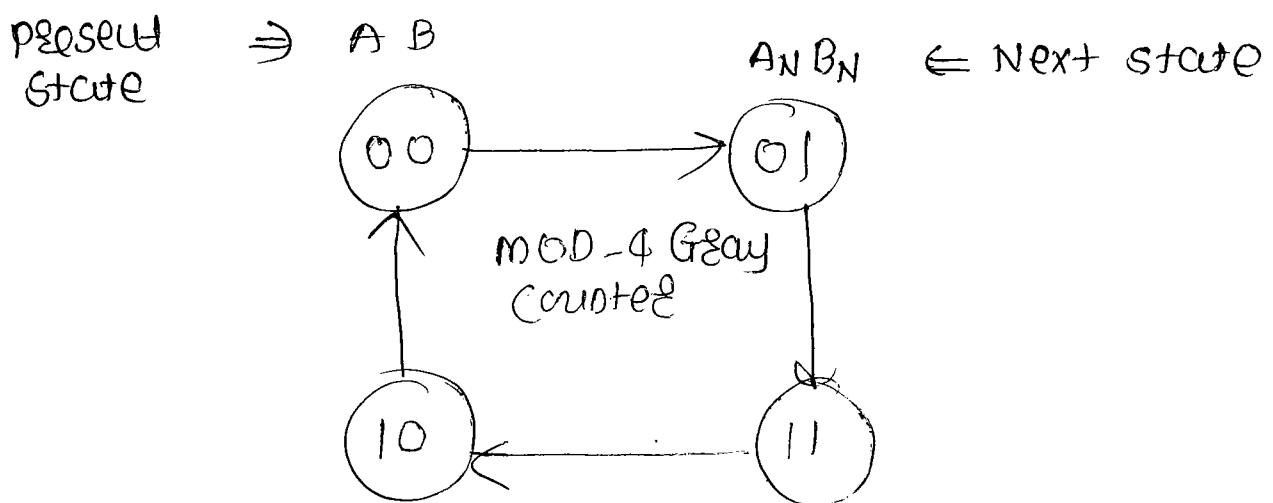
$$Y = x_5 - 3 \quad \text{if } m=1$$

$$Y_3 Y_2 Y_1 Y_0 = \begin{array}{c|c} X_2 X_1 X_0 & X_2 X_1 X_0 \\ \hline 0 & 1 & 1 & 1 & 0 & 1 & 1 & 1 \\ m=0 & & & & m=1 & & & \end{array} \leftarrow \text{2's complement of } B.$$

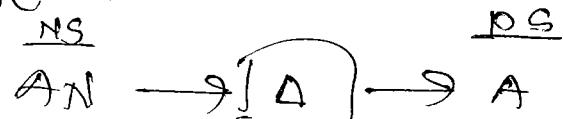


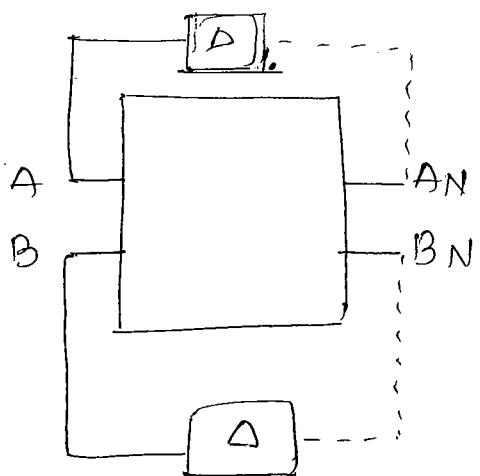
* Multiplexers for Realizing sequential circuits

The multiplexers along with D-flip-flops are used for realizing seq. ccts.



Q Every next state after some delay becomes present state \Rightarrow





A B		AN	BN
PS	NS		
0 0	0 1		
0 1	1 1		
1 0	0 0		
1 1	1 0		

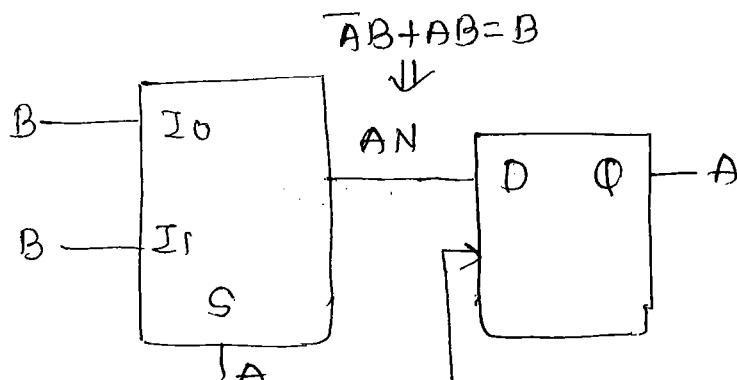
$$\underline{AN = \overline{AB} + AB} \quad \leftarrow \text{minterm expression}$$

$$\underline{AN = B} \quad \textcircled{I} \quad \leftarrow (\text{next state expression})$$

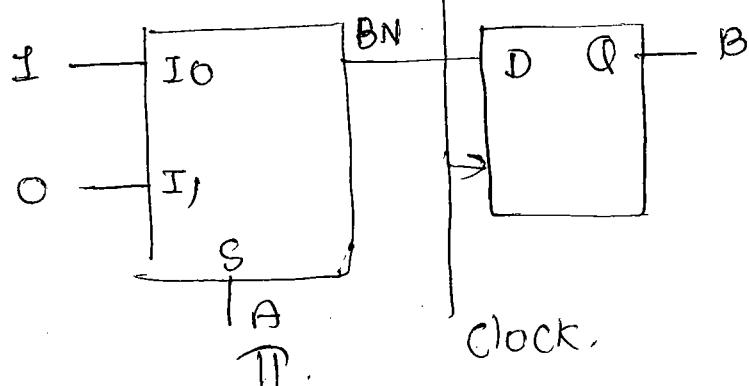
$$BN = \overline{AB} + \overline{A}B$$

$$\underline{BN = \overline{A}} \quad \textcircled{II}$$

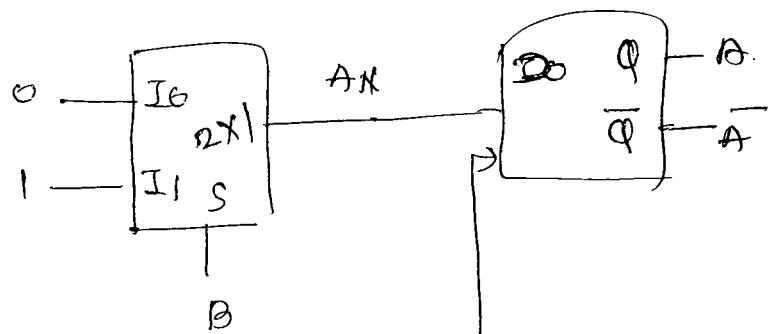
TWO MUX ARE REQUIRED TO
IMPLEMENT \textcircled{I} & \textcircled{II} .



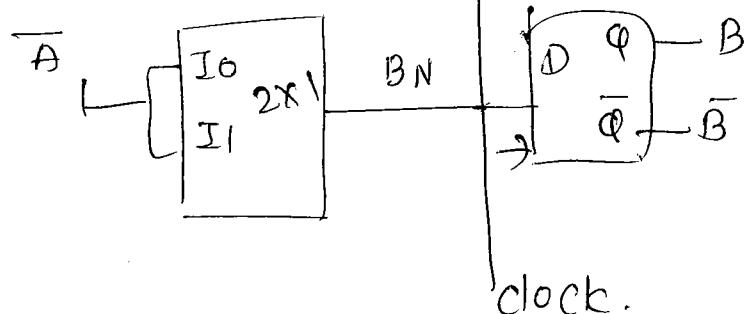
mod-4 gray
synchronized
counter.



$$\overline{A} \cdot 1 + A \cdot 0 = \overline{A}$$



mod-8 gear
counter



2bit \rightarrow 2 D flip
flop

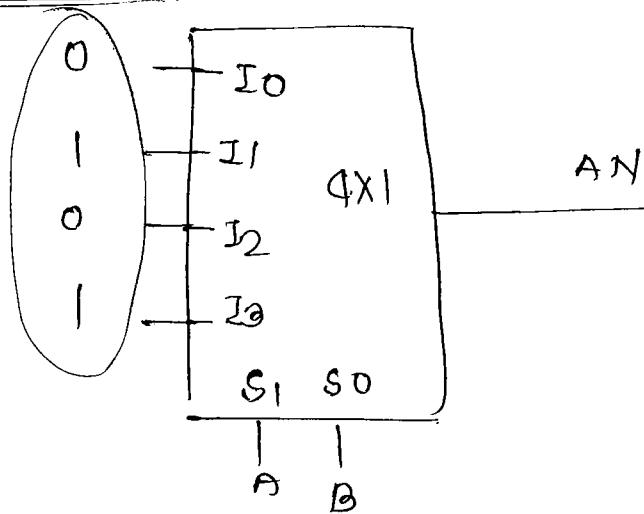
for 3 bit

counter \rightarrow

3 D flip flop
are req.



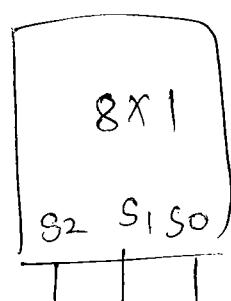
AN column



3 var. funⁿ



8x1



2 select lines ($2-1$)

$2^{3-1} \times 1$ MUX

$n-1$ select line MUX

$2^{n-1} \times 1$ MUX

If none of var. in the complemented form
then size of MUX = $2^n \times 1$

If complemented = $2^{n-1} \times 1$

Expansion of MUX's \Rightarrow

The higher capacity MUX is constructed with combinations of lower capacity MUX's which are arranged in multiple levels.

$$2 \times 1 \Leftarrow \text{Basic size} \Rightarrow N \times 1$$

$$8 \times 1 \Leftarrow \text{Target size} \Rightarrow M \times 1 (M > N)$$

$$K = 3 \Leftarrow \text{Number of levels, } k \Rightarrow \log_N M$$

$$\begin{matrix} i \\ \rightarrow \\ 1 & 2 & 3 \end{matrix} \quad \begin{matrix} 8 \\ 8/2 \\ 8/2^2 \\ 8/2^3 \end{matrix} \Leftarrow \text{Number of multiplexers} \Rightarrow (M/N)^i = x_i$$

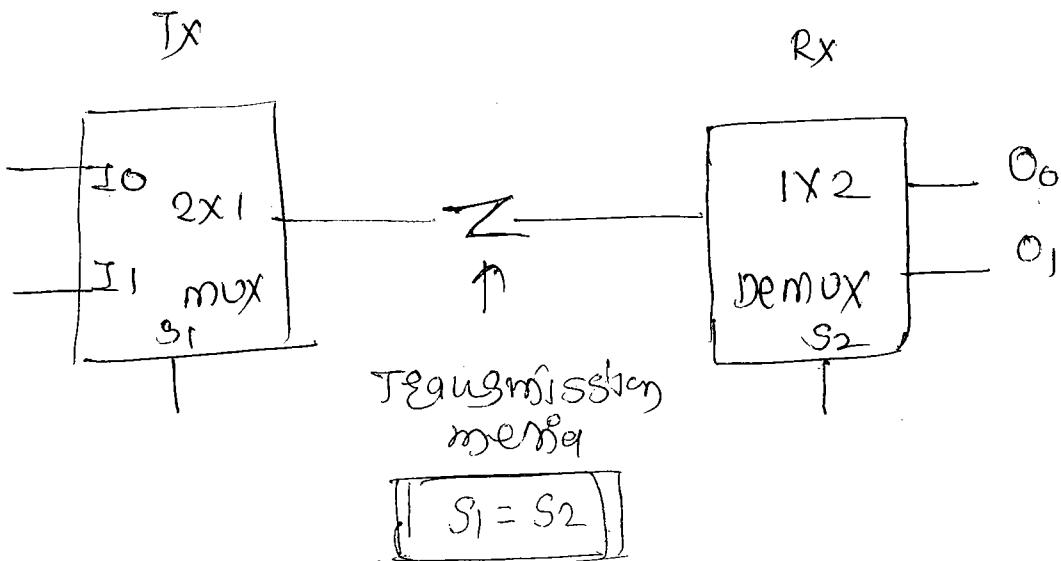
$$4 + 2 + 1 = 7 \Leftarrow \text{total no. of MUX's} \Rightarrow \sum_{i=1}^k x_i$$

$$2^3 \times 1 = 8 \times 1 \Leftarrow \text{max. expandable capacity with } k\text{-levels.} \Rightarrow N^K \times 1$$

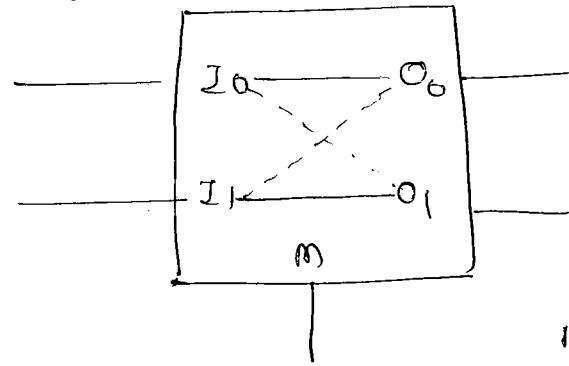
De-multiplexer \Rightarrow (Demux)

- The Demux is placed at the receiving end and it will get back desired IP from multiplexed signal.

- In the absence of multiplexed signal, the Demux is not having any significance, with slight modification. It can be used as decoder.

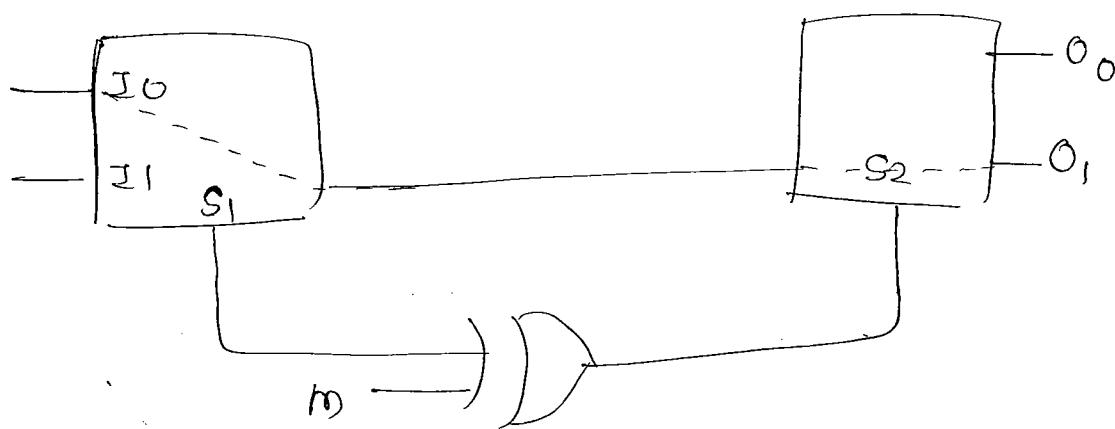


Intelligent switch



$m=0$ Straight connection

$m=1$ Crossed connection



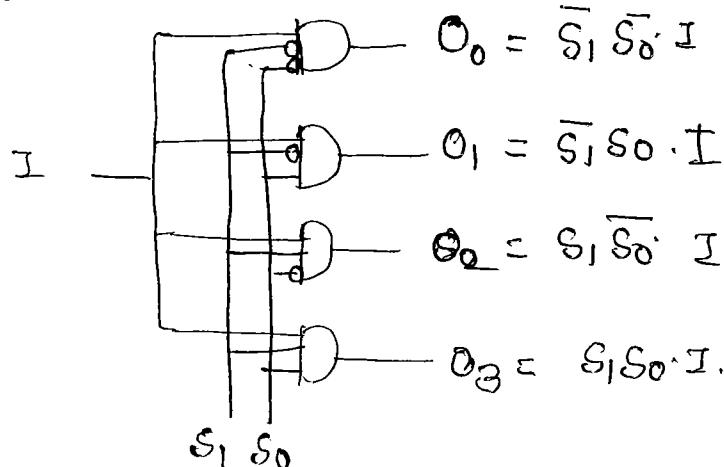
$$\text{if } m=0 \quad S_2 = m \oplus S_1$$

$$m=1 \quad S_2 = \bar{S}_1$$

- By slightly changing mux b/w, Demux is dense.

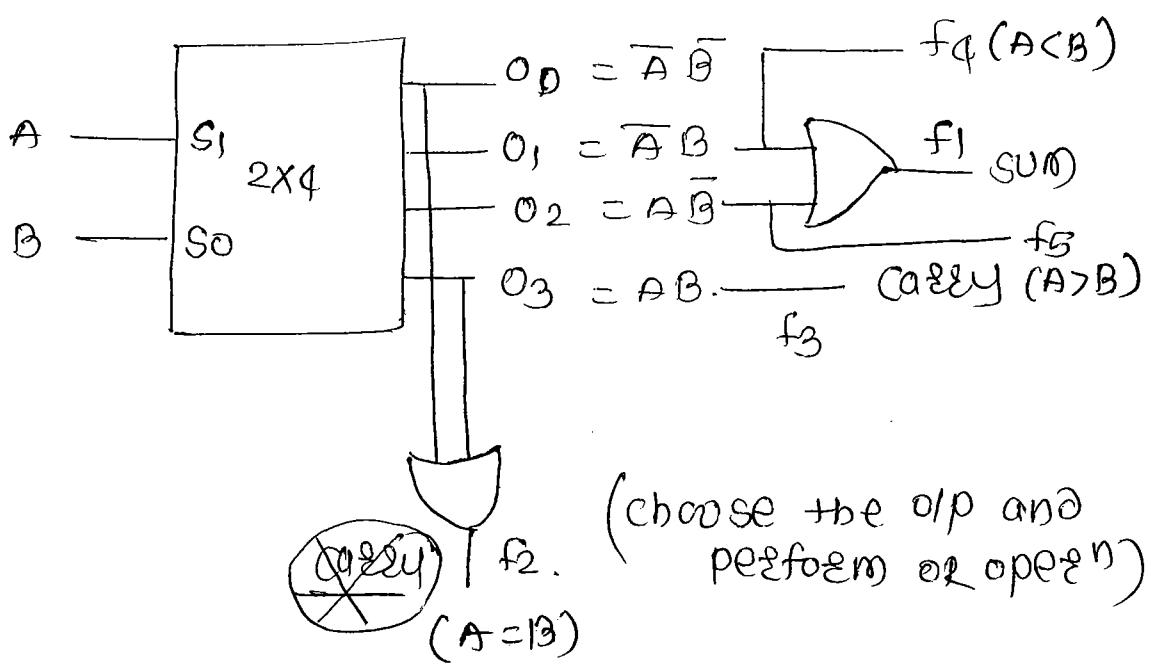
changes -

- i) Join all i/p's of mux and detach the final OR gate

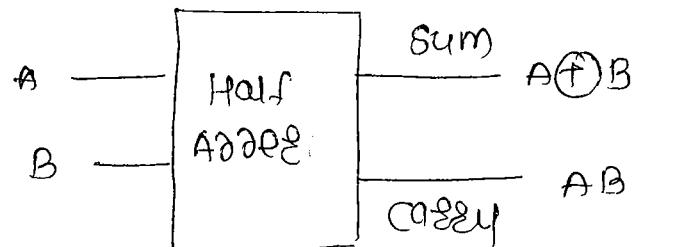


$S_1 S_0$	00	01	02	03
00	I	0	0	0
01	0	I	0	0
10	0	0	I	0
11	0	0	0	I

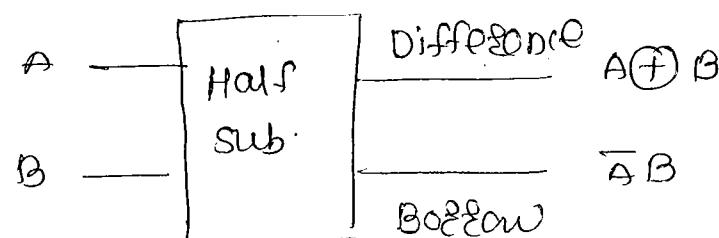
→ Demux is converted as a decoder by inactivating its enable and converting select lines as input lines.
 ↓ → hence, 1x4 mux can also be used as 2x4 decoder.
 (make $I=1$)



- single decoder can be used to realise multiple functions.
 (for every funcⁿ external OR-gate is needed)
- single decoder can be used as half adder/subtractor.



$$\begin{array}{c} \text{Sum} \\ \uparrow \\ HA \end{array} \quad \begin{array}{c} \text{carry} \\ \uparrow \\ f_1, f_3 \end{array}$$

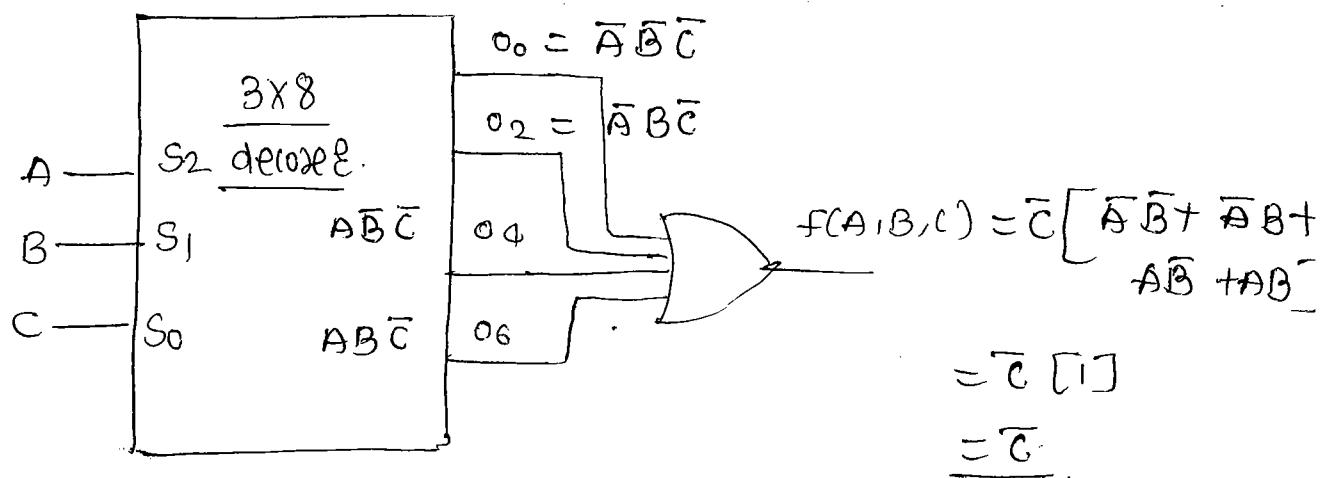


$$\begin{array}{c} \text{diff.} \\ \uparrow \\ HS \end{array} \quad \begin{array}{c} \text{borrow} \\ \uparrow \\ f_1, f_4 \end{array}$$

1-bit Comparator \Rightarrow $\frac{f_2, f_4, f_5}{\uparrow \uparrow \uparrow}$

Equal less greater
than than
(EQ). (LT) (GT)

Ques. Consider the following decoder which is realizing three variable function $f(A, B, C)$. Identify the correct stmt among the following.



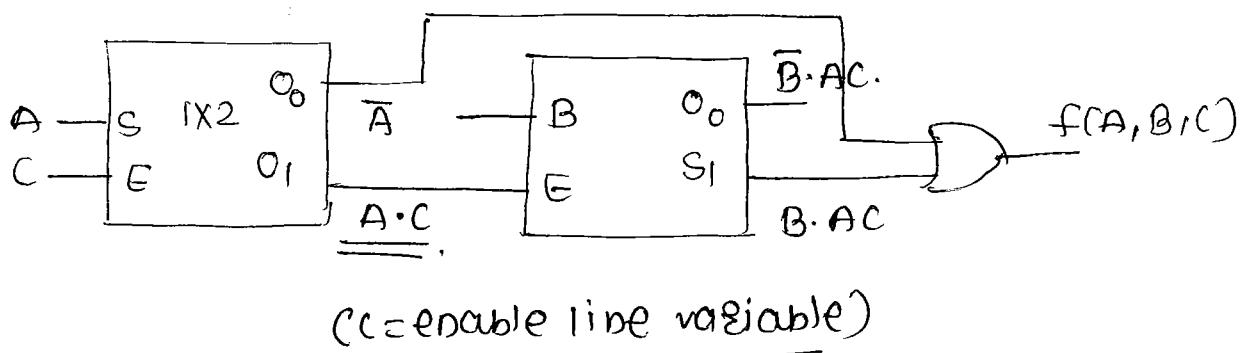
a) f is free from 1 var.

b) 2 -

c) All - (If all 8 op's are connected)

d) f depends on all var.

Que. What is the funⁿ represented by follo. decoders.



$$f(A, B, C) = \bar{A}C + ABC$$

$$= C [\bar{A} + AB]$$

$$= \underline{\bar{A}C + BC}$$

$$\Sigma = (1, 3, 7) \quad 0 \notin$$

$$\Pi (0, 2, 4, 5, 6)$$

2 to 5.30 Eng.
6 to 8.30 Eng
202

04/08/2012

* Binary to decimal Decoding *

(A, B, C, D)

(0 to 9)

Que. If the design does not reject the false data expression for output. 8

- (a) $A\bar{C}$ (b) $A\bar{B}\bar{C}\bar{D}$ (c) $A\bar{C} + AB$ (d) $A\bar{C} + \bar{A}B$

$$= \Sigma(8) + \underset{\Phi}{\Sigma}(10 \text{ to } 15)$$

= $\Sigma(8) \dots$ with false
data rejctn

$A\bar{B}\bar{C}\bar{D}$

false
data

ABCD	O ₀	O ₁	...	O ₈	O ₉
0000	1	0	...	0	0
0001	0	1	...	0	0
0010	0	0	1	0	0
0011	0	0	0	1	0
0100	0	0	0	0	1
0101	0	0	0	0	0
0110	0	0	0	0	0
0111	0	0	0	0	0
1000	0	0	0	0	0
1001	0	0	0	0	0
1010	0	0	0	0	0
1011	0	0	0	0	0
1100	0	0	0	0	0
1101	0	0	0	0	0
1110	0	0	0	0	0
1111	0	0	0	0	0

AB		00	01	11	10
CD					
00				∅	12
01				∅	13
11				∅	14
10				∅	15
					16
					17
					18

without false data
rejection = \bar{AD}

Expression for 'g' = $A\bar{B}\bar{C}D$ --- with false data reject
= AD ----- without _____.

Que.

Consider binary to ⑧ 5 4 2 1 BCD converter with the inputs are A,B,C,D and outputs are P,Q,R,S. what will be the expression for R

8 4 2 1				5 4 2 1				2 4 2 1			
A	B	C	D	P	Q	R	S	P	Q	R	S
'0'	0	0	0	0	0	0	0	0	0	0	0
'1'	0	0	0	1	0	0	0	1	0	0	0
'2'	0	0	1	0	0	0	1	0	0	1	0
'3'	0	0	1	1	0	0	1	1	0	0	1
'4'	0	1	0	0	0	1	0	0	0	1	0
'5'	0	1	0	1	1	0	0	0	1	0	1
'6'	0	1	1	0	1	0	0	1	1	0	0
'7'	0	1	1	1	0	0	1	0	1	1	0
'8'	1	0	0	0	1	0	1	1	1	1	0
'9'	1	0	0	1	1	0	0	1	1	1	1

5 4 2 1
 $\emptyset 0 0 0$
 $\underline{1 0 0 1}$

2 4 2 1
 $\emptyset 0 0 0$
 $\underline{1 0 0 1}$

5. 0 0 0 0
 $\emptyset 0 0 0$
 $\underline{1 0 1 1}$

$\underline{31}$

10 to 15
 \uparrow
don't care cases.

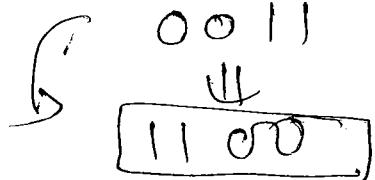
$$R(A, B, C, D) = \sum_{\text{10 to 15}}(2, 3, 7, 8) + \sum_{\text{9}}(1)$$

* 9's complement of Number A \Rightarrow $9 - A$

9's

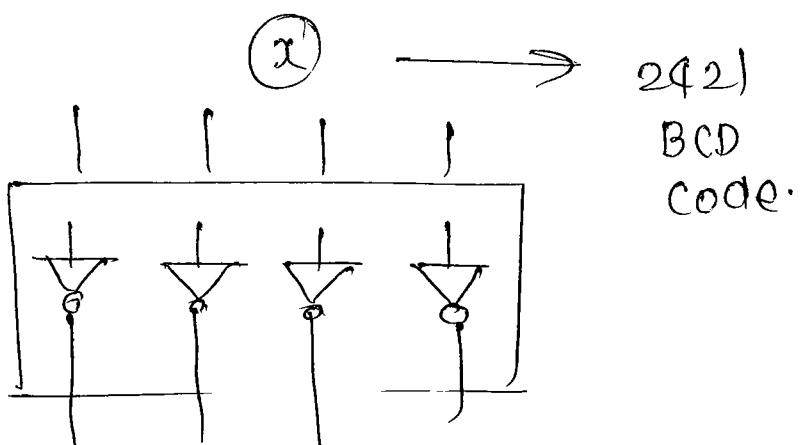
$$8 \Rightarrow 9 - 8 = 6$$

Take 2421 code of 3.



(flip all bits) \Rightarrow invert them

Ques.



④ \Rightarrow y is 9's complement of x

what is 2421 of x & y?

43
- 21

22

78
- 21

57

q's complement of 21
(carry is to be considered)

43
- 21

22

79
- 21

58

10's complement of 21
(carry is ignored)
- It is faster.

2's complement is eqv. to
10's complement

1's complement is eqv. to
9's complement

∴ 2's complement is fasted.

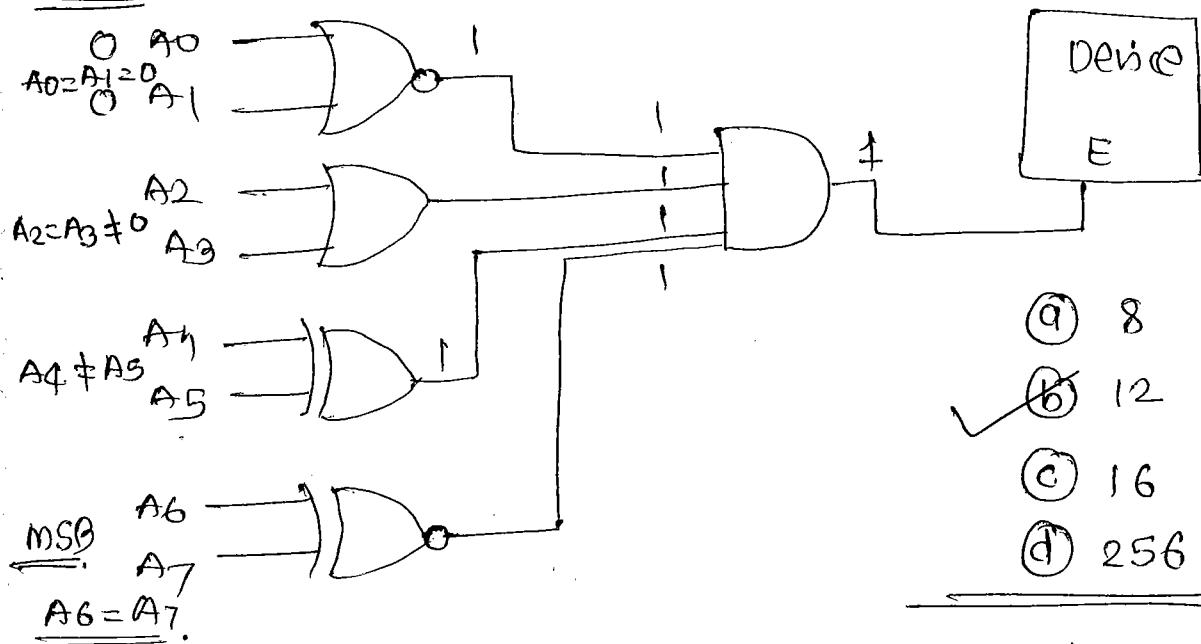
NOTE-

(Complementing
bits of no = 9's comp)

The XS-3 code also exhibit this property \rightarrow only
but XS-3 code is not a weighted code.

(not 8421, 9421, 2424)

Ques.

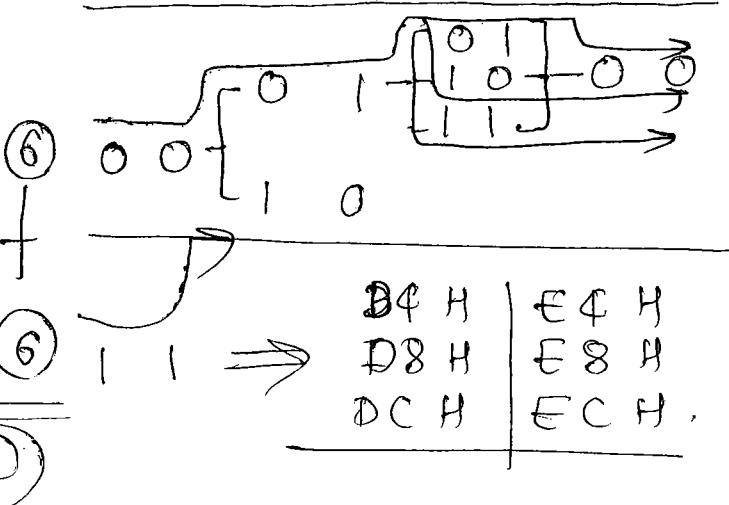


when does the device will be activated?

00010100
00011000 } ③
00011100 }
00100100 } ③
00101000 }
00101100 }

↓
24 H
28 H
2C H.

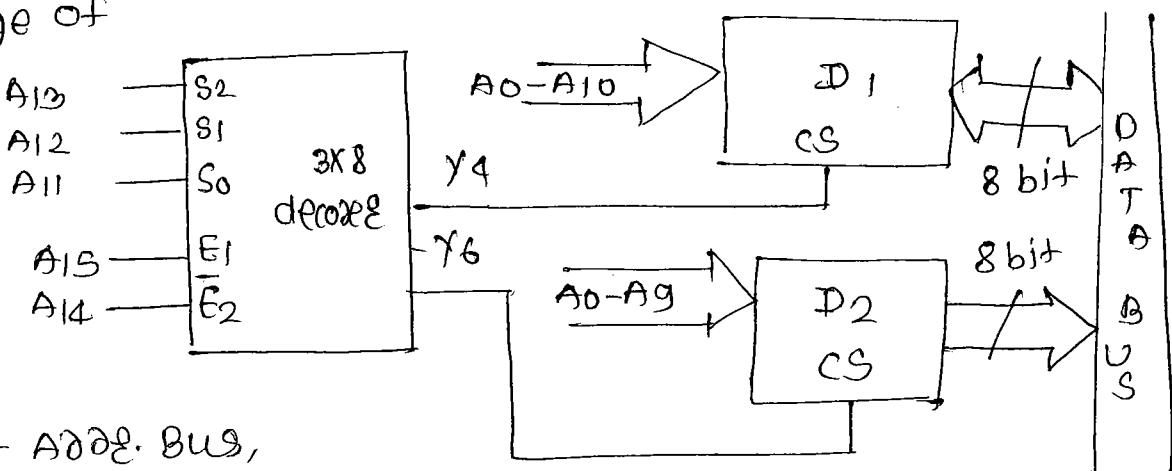
A₇ A₆ A₅ A₄ A₃ A₂ A₁ A₀



Q1. Consider the following interfacing and obtain address range of device 1 and device 2.

Average range of

D.R.D.2



16-bit Address Bus,

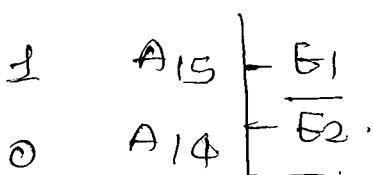
8 bit data bus

(RAM) D₁ $\Rightarrow \frac{2^{11}}{8 \text{ bits}} = 2 \text{ KB}$ $\left(\frac{2^{11} \times 8 \text{ bits}}{8 \text{ bits}} \right)$ (both read and write operation)

(ROM) D₂ \Rightarrow 1 kB $\xrightarrow{\text{Only read opes}} \text{(only read opes)}$

to select drive D1 \Rightarrow A13 A12 A11 } possible
 \leftarrow 1 0 0
D2 \Rightarrow 1 1 0 } only cover it is decoze

→ Thus, we have to enable lines.



$O_1 \Rightarrow A000H \Rightarrow$ starting Address
 $A7FFH \Rightarrow$ ending Address

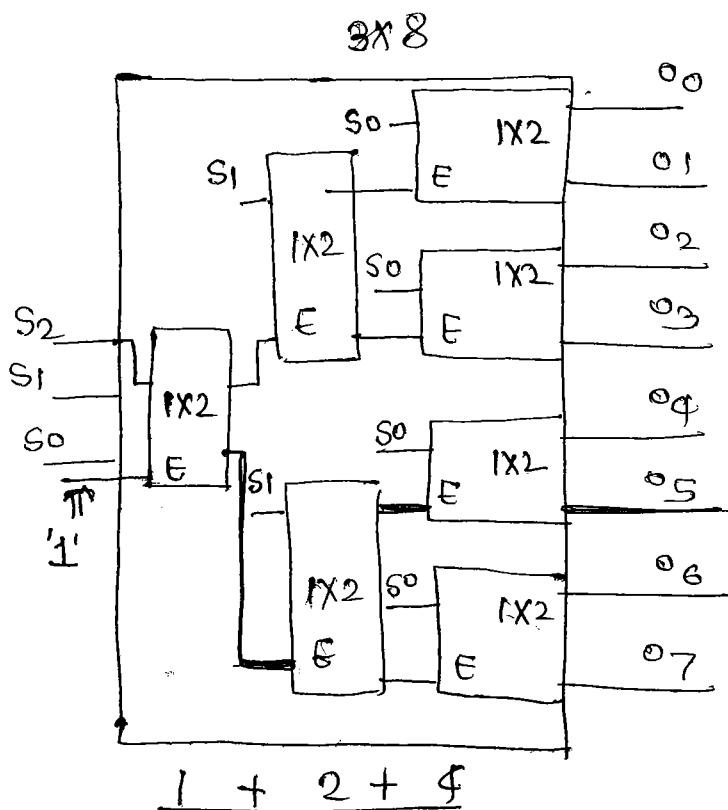
$O_2 \Rightarrow A10=0 \quad A10=1$
 $B000H : B3FFH \Rightarrow$ starting Address
 $A10=1 \Rightarrow B400H : B7FFH \Rightarrow$ ending Address

Shadow Addressing.

(At a given instant it is 1KB but in future 1KB can be added/capacity can be increased)

* Expansion of Decoders *

The capacity of decoders can be expanded by using smaller capacity decoders in multiple levels. The 1st level decoder will provide enable signals to the given; IX2, Target: 3x8.



If $S_2 = 1$
 $S_1 = 0$
 $S_0 = 1$
 $E = 1$

O_5 is selected

- MSB bit \Rightarrow 1st level
- LSB bit \Rightarrow last level.

levels: 1st 2nd 3rd

Target $\rightarrow M \times N (N = 2^M) \rightarrow 3 \times 8$

Basic $\rightarrow P \times Q (Q = 2^P) \{ \text{PCM} \} \rightarrow 1 \times 2$

levels - k $\rightarrow M/p \otimes \log_Q N \rightarrow 3$

Number of decoders

in i-th level $\rightarrow \frac{N}{Q^{(i+k+1)}} = x_i$

$$\begin{array}{c} i \mapsto 1 \quad 2 \quad 3 \\ 8/2^3 \quad 8/2^2 \quad 8/2^1 \end{array}$$

Total decoders $\rightarrow \sum x_i \rightarrow 7 (1+2+4)$

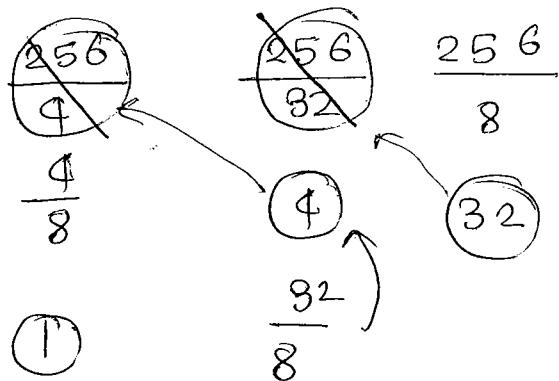
maximum capacity
with k-levels. $\rightarrow (P * k) \times Q^k \rightarrow (1 * 3) \times 2^3 = 3 \times 8$

Ques. How many 8x8 decoders are required to construct 8x256 decoder.

8x256

3x8

$$k = 8/3 = \underline{\underline{3}}$$



$$\text{max. capacity} = 3 \times 3 \times 8^3$$

$$= \underline{\underline{9 \times 512}}$$

$$8 \times 256$$

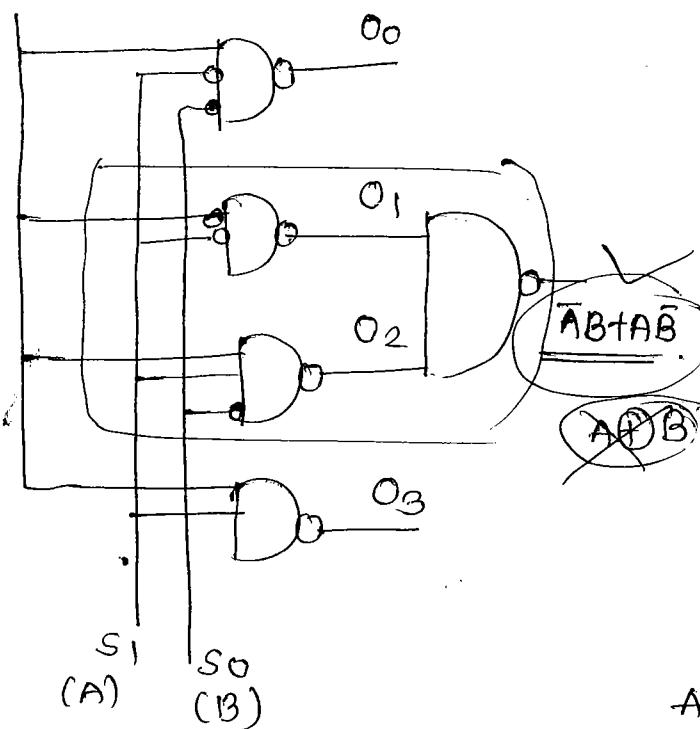
100% utilization \leftarrow utilization
 \downarrow 50% less

$$86 \rightarrow 3 \times 8$$

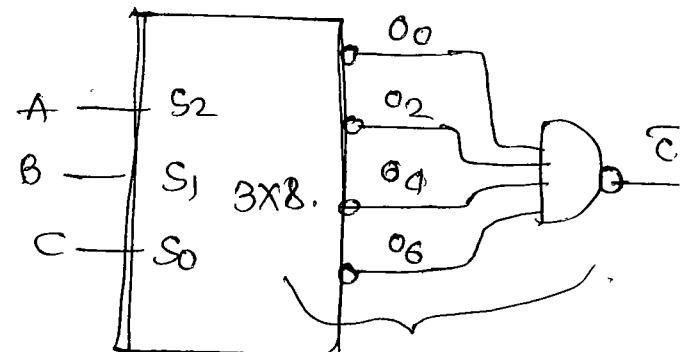
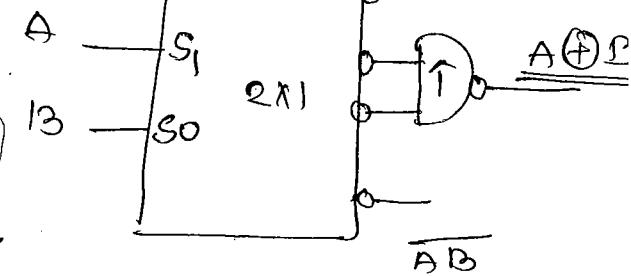
$$1 \rightarrow 2 \times 4$$

NOTE - If the decoders are using NAND gates internally it is termed as active low decoder. The selected output is at logic '0' and others are at logic '1'. To realize a function using active decoder, appropriate outputs are selected and the NAND operations are performed.

$I=1$



Active low decoder



$$\Sigma (0, 2, 4, 6)$$

Free from
A & B

Encoder

05/08/2012

- Convert decimal to binary Ex: 4x2
- Rule of Encoding: Highest suffix input is encoded with highest binary value.
- Non-priority encoders does not allow simultaneous input activation and consume more hardware.
- Priority encoders require less hardware but exposed to stagnation for low priority input.

Rule of assigning priority: Highest suffix input is given with highest priority.

PIC → Priority Interrupt Controller

Priority Encoder

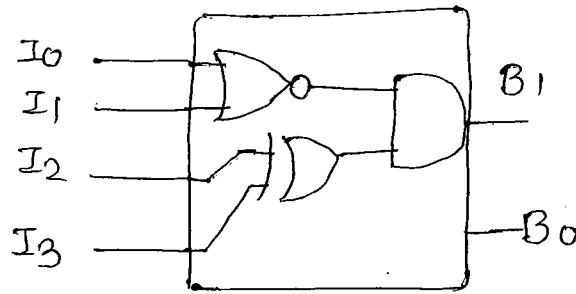
I ₀	I ₁	I ₂	I ₃	B ₁	B ₀	I ₀	I ₁	I ₂	I ₃	B ₁	B ₀
1	0	0	0	0	0	1	0	0	0	0	0
0	1	0	0	0	1	0	1	0	0	0	1
0	0	1	0	1	0	0	0	1	0	1	0
0	0	0	1	1	1	0	0	0	1	1	1

Non-Priority Encoder →

$$\begin{aligned}
 B_1(I_0, I_1, I_2, I_3) &= \overline{I_0} \overline{I_1} I_2 \overline{I_3} + \overline{I_0} I_1 \overline{I_2} I_3 \\
 &= I_0' I_1' (I_2 \oplus I_3) \\
 &= (\overline{I_0 + I_1}) (I_2 \oplus I_3)
 \end{aligned}$$

$$B_0(I_0, I_1, I_2, I_3) = \overline{I_0' I_1 I_2 I_3} + \overline{I_0' I_1' I_2' I_3}$$

$$= \overline{I_0 + I_2 \cdot (I_1 \oplus I_3)}$$

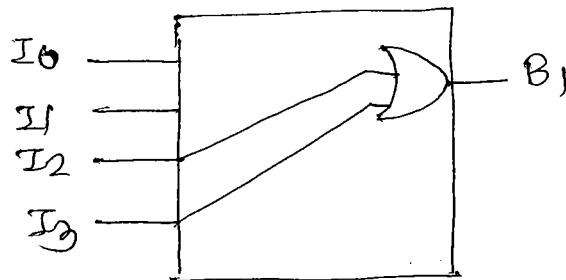


\leftarrow simultaneous activations are not allowed.

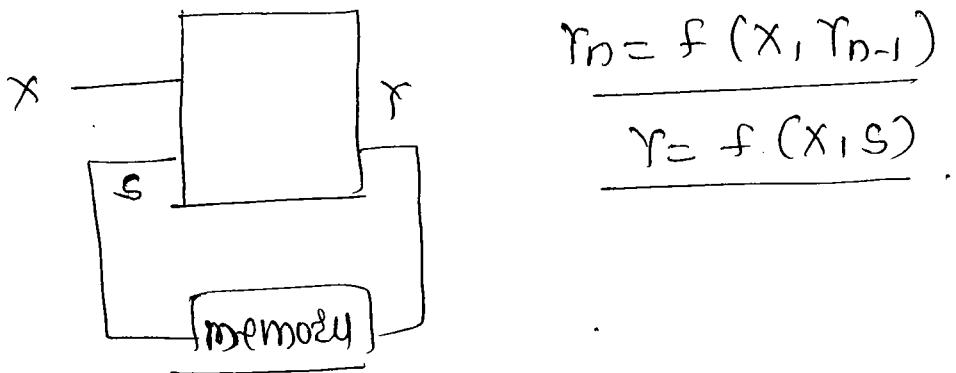
Priority Encoder -

$$B_1(I_0, I_1, I_2, I_3) = I_2 I_3' + I_3 = \underline{(I_2 + I_3)}$$

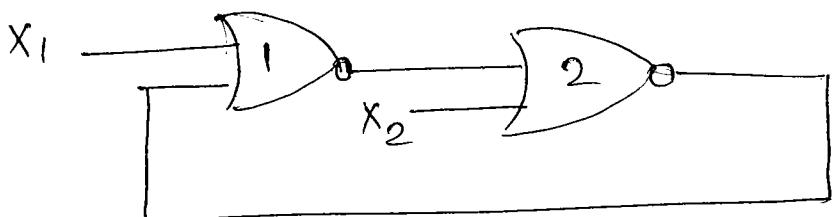
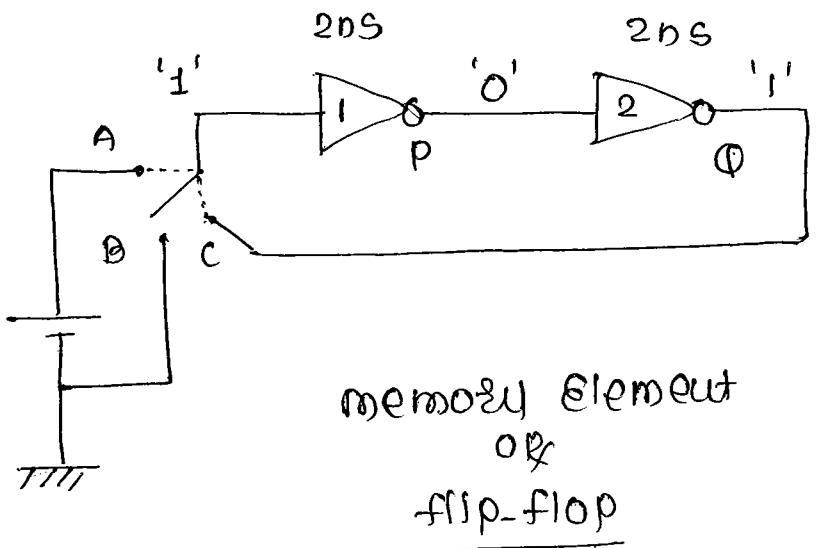
$$B_0(I_0, I_1, I_2, I_3) = \underline{\underline{I_1 I_2 + I_3}}$$



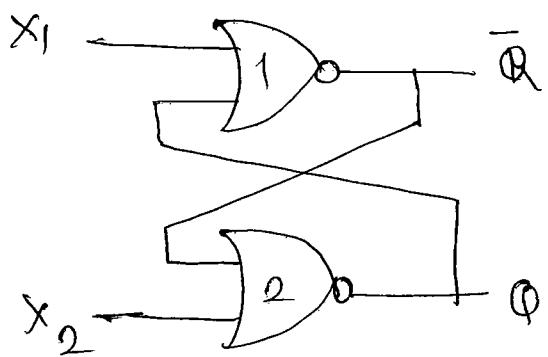
Sequential Circuits



$$\frac{Y_n = f(X, Y_{n-1})}{Y = f(X, S)}$$

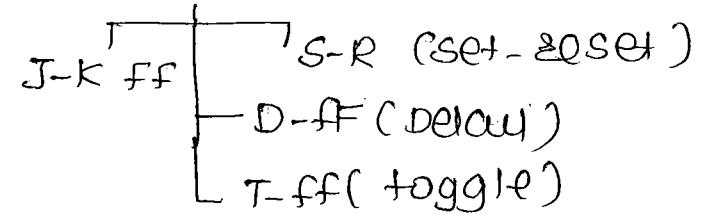


NOR- flip flop

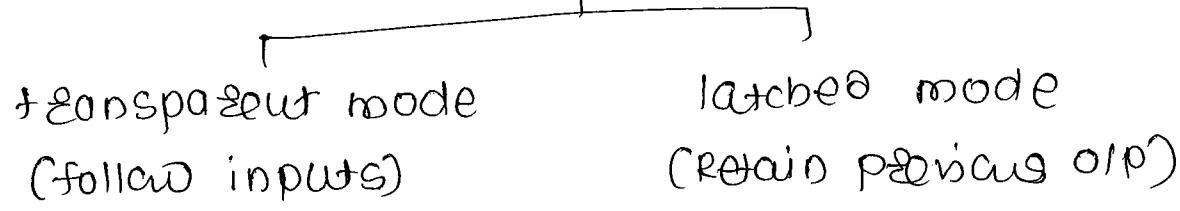


- The flip-flop is the basic memory element which is capable of 1-bit storage.
- The flip-flop contains 2-stable states. (1 for logic 1 and another for logic 0) hence it is called as 'bistable multivibrator'
- The flip-flop contains 2-complementary op's. It will have valid operation only when op's are having complementary relation
- The flip-flops can be classified

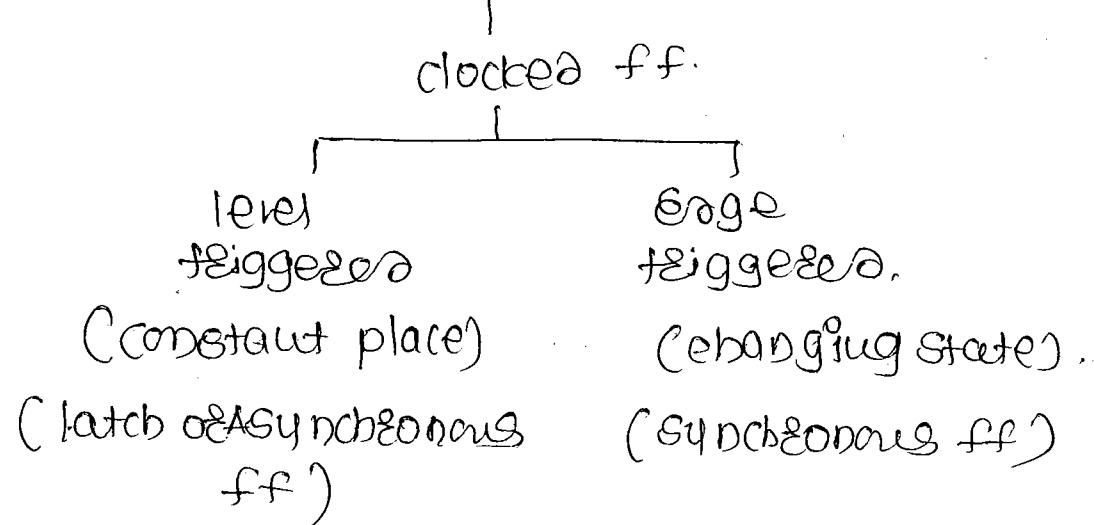
- i) based on the construction (NOR, NAND flip flop)
- ii) based on the function they perform

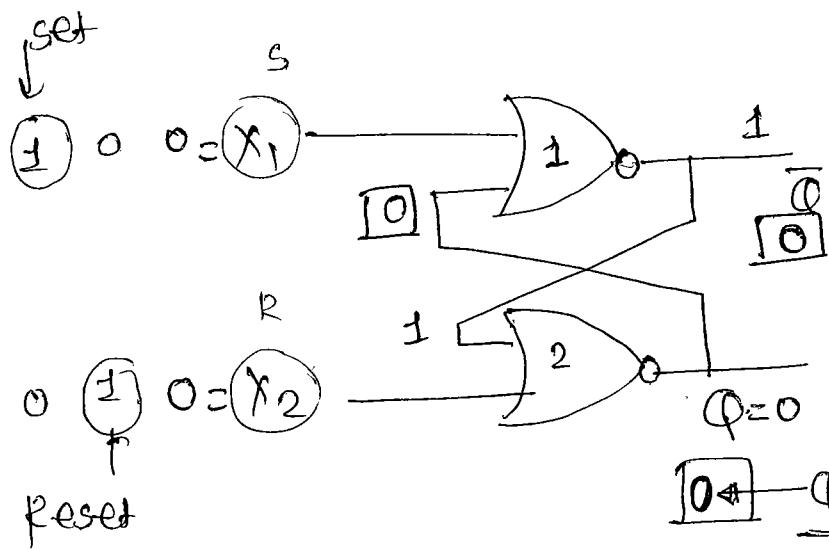


- iii) based on operating mode



- iv) based on synchronization-





		NOR
A	B	
1	0	0
0	1	0
0	0	1

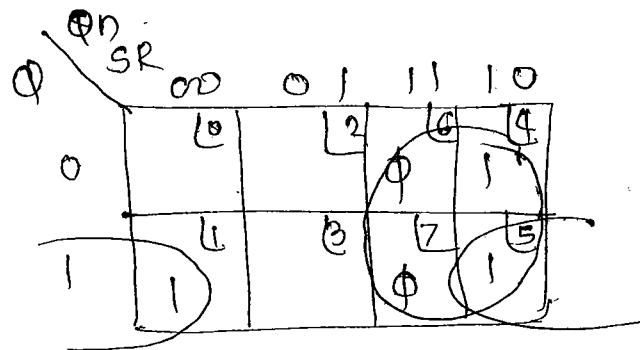
set \downarrow Reset line \downarrow

X_1	X_2	Q	Q_n	
0	0	0(A)	0	$Q_n = Q$.
0	0	1(B)	1	
0	1	0(A)	0	$Q_n = 0$
0	1	1(B)	0	
1	0	0(A)	1	$Q_n = 1$
1	0	1(B)	1	
1	1	0(A)	0	Invalid
1	1	1(B)	0	

* Every flip-flop is having characteristic expression, state diagram and excitation table.

→ The char. expression is the expressⁿ for next state.

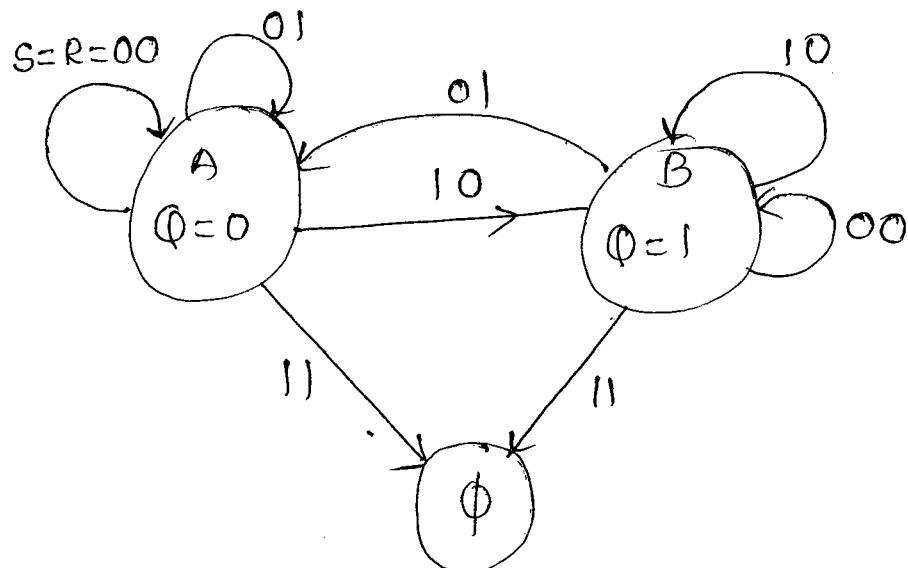
$$Q_n(S, R, Q) = \sum(1, 4, 5) + \sum_{\emptyset}(6, 7)$$



$$\underline{S + \bar{R} Q}$$

Q_n (char. expression of S-R flip-flop) = $S + \bar{R} Q$, when
 $S=R \neq 1$

State Diagram \Rightarrow



Excitation table \Rightarrow

The ex. table indicates the desired inputs for getting equivalent change at output

$Q \rightarrow Q_n$		S	R
(A)	0 0	0	ϕ .
	0 1	1	0
	1 0	0	1
	1 1	ϕ	0.

A new FF. X, Y is having the following behaviour

X, Y	Y	Q_n
00		1
01		0
10		0
11		0

Construct the state table

state diag

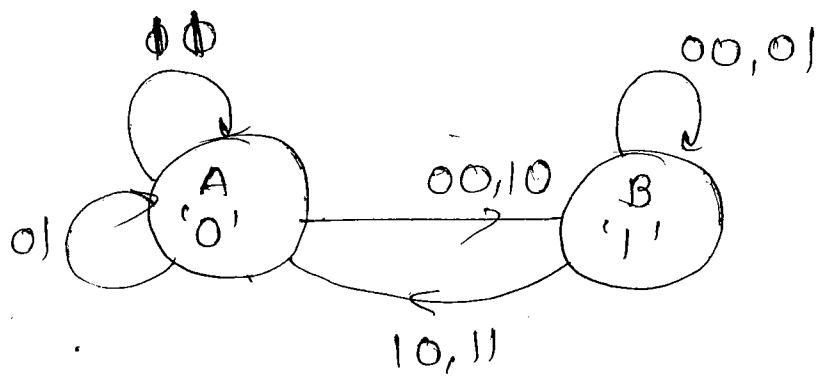
char. exp

excitation table. for

this new ff.

$$Q_n(X, Y, \emptyset) = \overline{X}Q + \overline{Y}Q$$

X	Y	Q	Q_n
0	0	0	1
0	0	1	1
0	1	0	0
0	1	1	1
1	0	0	1
1	0	1	0
1	1	0	0
1	1	1	0

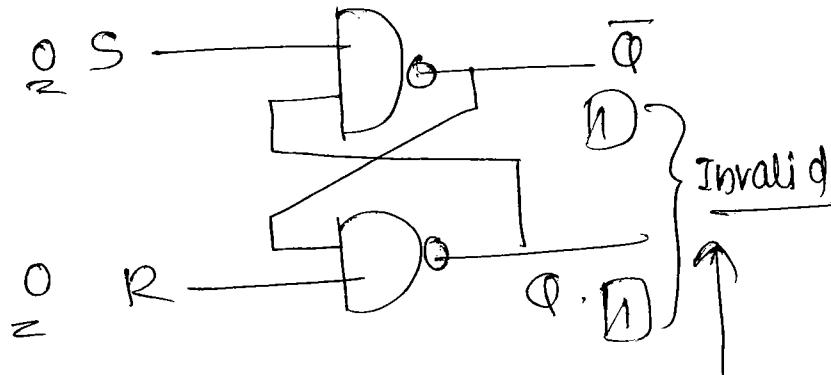


$Q \rightarrow Q_n$	X	Y
00	∅	↑
01	∅	0
10	1	∅
11	0	∅

NAND-FF \Rightarrow

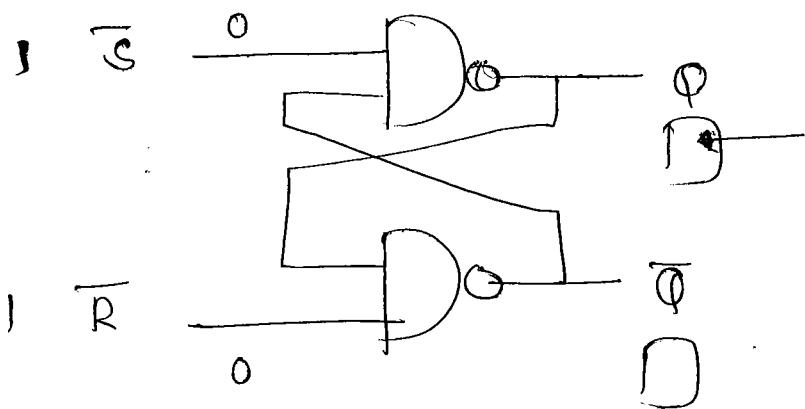
The SR NAND FF will behave as SR NOR FF provides $S \neq R$. If $S=R$, the NAND behaviour and NOR behaviour are opposite.

ff	S	R	Q_n
	00	01	10
NOR	0	0	1
NAND	Invalid	1	0



A	B	NAND
0	0	1
0	1	1
1	1	0

does not follow the
Complementary selection



$$SR\text{ NAND} \equiv SR\text{ NOR}$$

06/08/2012

- * FF classification based on the function →
 - JK-FF is behave as S-R and allowed $J=K=1$ ($J=S$, $K=R$)
 - If $J=K=1$ the flip flop complement (Toggle) its output.
 - JK-ff can be used as
 - D ff ($J \neq K$)
 - T ff ($J \equiv K$)
 - T-ff act as MOD-2 counter
 - D-FF is the basic ff in shift Registers and shift counters
 - T-ff is the basic ff in ring counters.

(Completely specified)

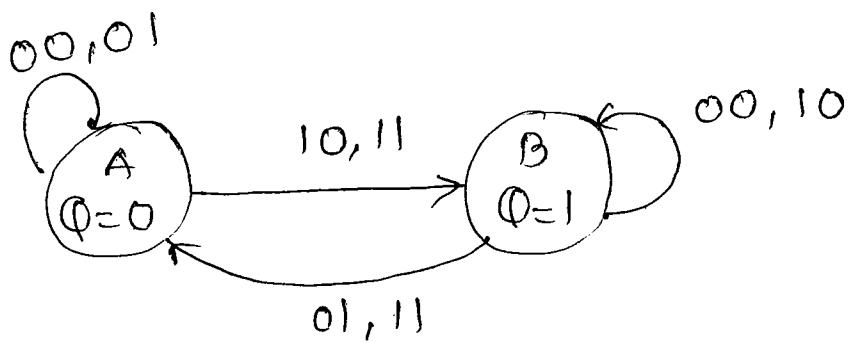
J	K	Q	Q_n
T-ff	0	0	0
	0	0	1
D-ff	0	1	0
	0	1	0
	1	0	1
	1	0	1
T-ff	1	1	1
	1	1	0

$$Q_n = Q$$

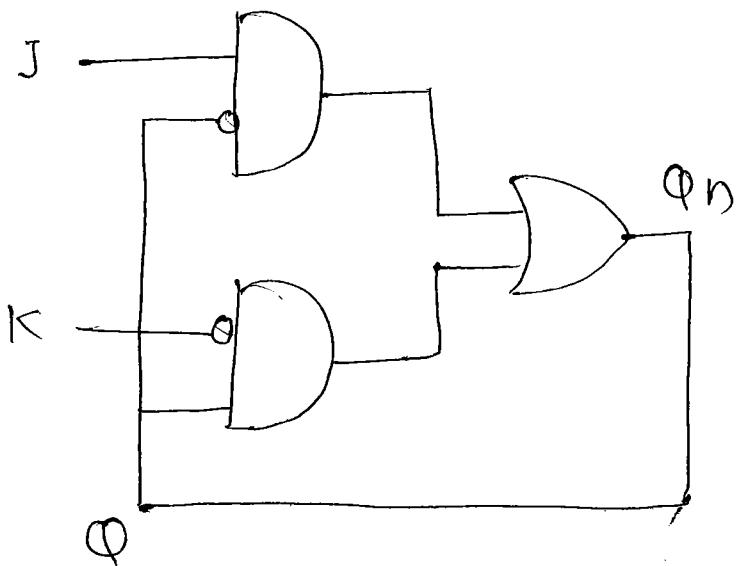
$$\Phi_D(J, K, Q) = \Sigma(1, 4, 5, 6)$$

while SR-ff
incompletely specified

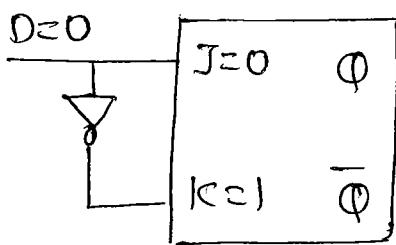
$$= J\bar{Q} + \bar{K}Q$$



$Q \rightarrow Q_n$	J	K
0 0	0	0
0 1	1	0
1 0	0	1
1 1	0	0

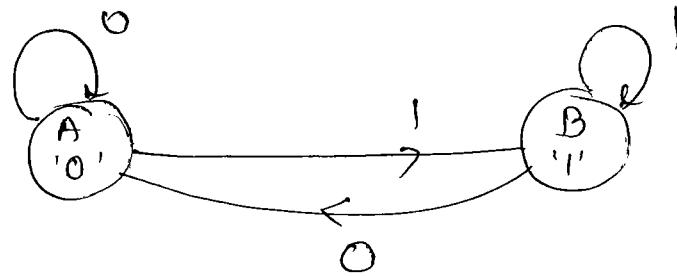
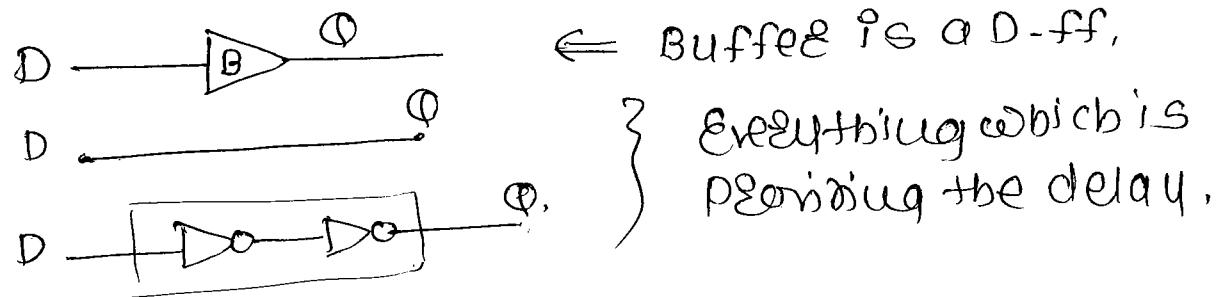


D-ff ($J \neq K$)



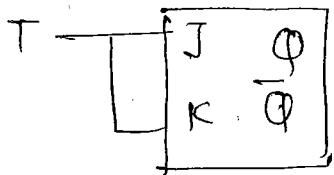
D	Q	Q_n
0 (0)	0	$Q_n = 0 = D\bar{Q} + DQ = D$
0 (1)	0	
1 (0)	1	$Q_n = 1 = D$
1 (1)	1	

"D-ff is a true combinational gate"
 current o/p depends on only current i/p.



The excitation statement of the D-flipflop
 whatever Q_n is required it must be applied at
 D-i/p [$D = Q_n$]

T-FF \rightarrow (J=K)

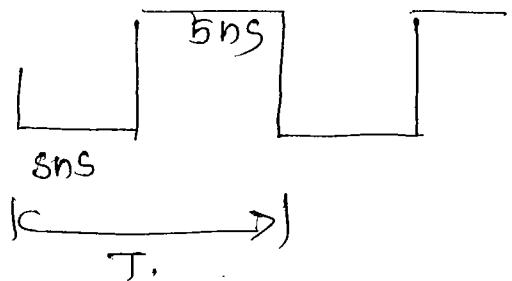
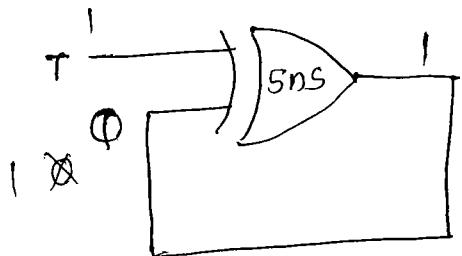


T	Q	Q_D
0	0	0
0	1	1
1	0	1
1	1	0

$Q_D = \bar{Q}$

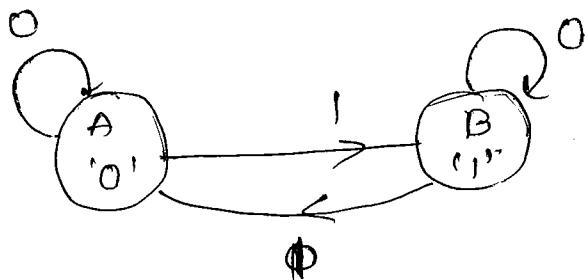
$$Q_D(T, Q) = \overline{T}Q + T\overline{Q}$$

$$= \underline{\underline{T \oplus Q}}$$



$$f = \frac{1}{T}$$

\Rightarrow delay will be doubled, freq. is half, thus called as mod-2 counter.



Excitation statement \rightarrow

If $\Delta Q \neq 0$, T must be ± 1

change is there either 0 to 1 or 1 to 0

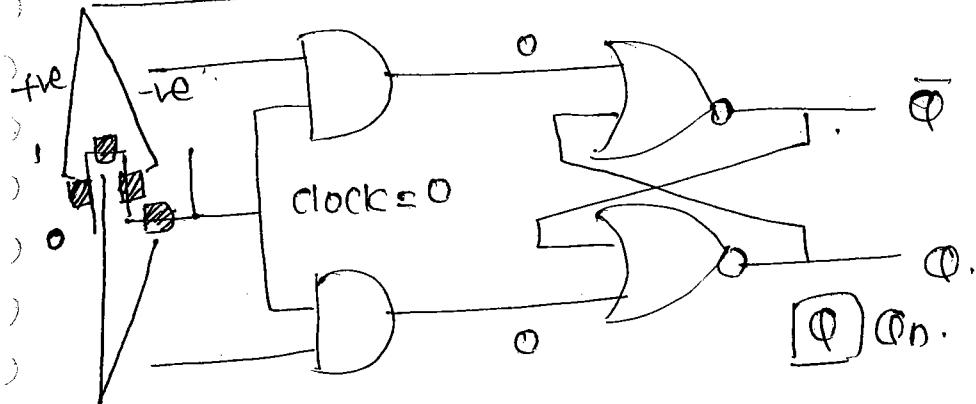
Clocked ff -

In the clocked ff, the change in the state is synchronized with external signal Clock. If clock is not active, the ff will retain its previous output.

Based on the instance of the clock, the clocked ff can be level triggered or edge triggered.

If clock is active, the operating mode is called transparent mode. Now the ff is operating in latched mode.

Edge triggered



Level triggered.

(+ve, -ve)

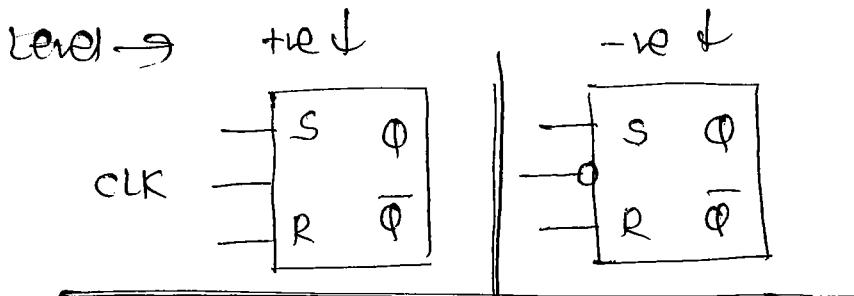


(triggering at
constant place).

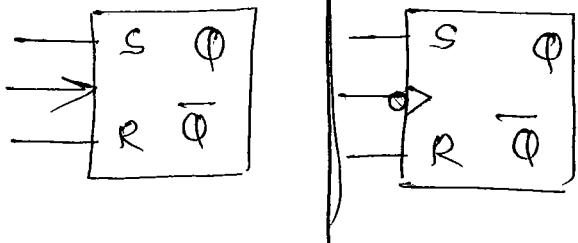
* Edge triggering is preferred to level triggering because it is less sensitive to the noise.

CLK	S	R	Qn
0	φ	φ	φ

t _{ve}	clk			Q _n
	S	R		
↑	0	0	φ	} transparent mode
↑	0	1	0	
↑	1	0	1	
↑	1	1	Invalid	
0/w.	φ	φ	φ (Latched mode)	

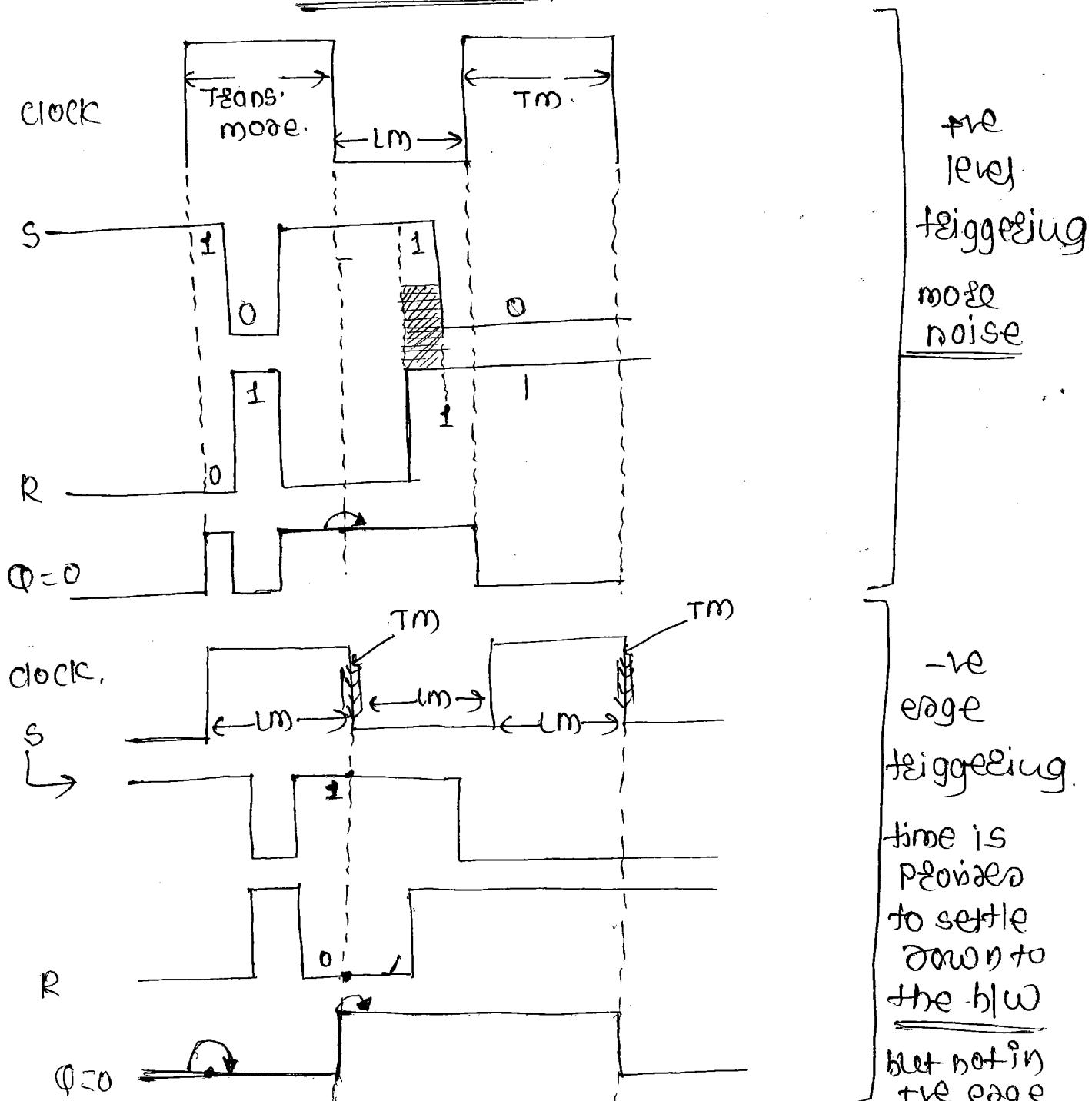


edge



↗ -ve edge triggering

+ve level trigger:



+ve
level
triggering
mode
noise

-ve
edge
triggering.

time is
provided
to settle
down to
the h/w

but not in
the edge

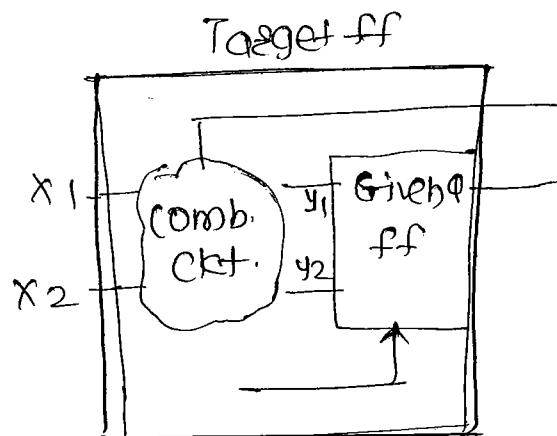
ff. interconnection procedure

The ff interconnection allows the connection of one ff into another, here the source ff is made to simulate the behaviour of NOR-gate target.

Step 1) - Obtain the truth table of target ff

Step 2) - Replace the next state using the excitation table of given ff.

Step 3) - Get the expressions for the i/p's of given ff and realize them.



$$Y_i = f(x_1, x_2, \Phi)$$

NOTE: If the given ff is J-K flip-flop direct connection can be made

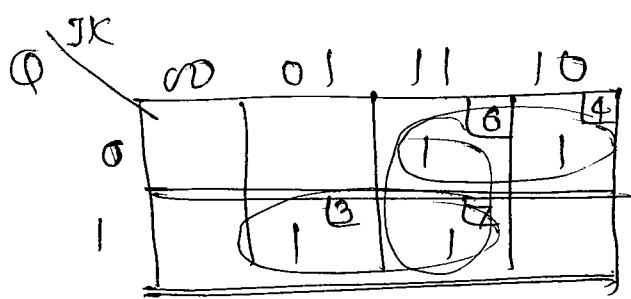
*** Connect the T-ff into J-K ff \Rightarrow

J	K	Φ	Q_n	T
0	0	0	0	0
0	0	1	1	0
0	1	0	0	0
0	1	1	0	1
1	0	0	↑	1
1	0	1	1	0
1	1	0	↑	1
1	1	1	0	1

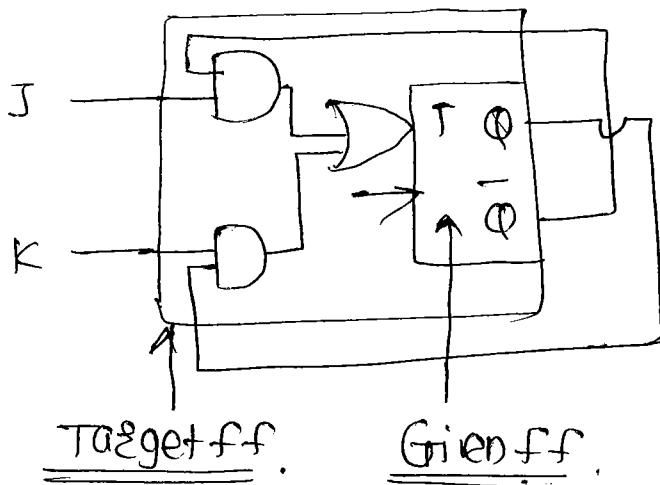
② excitation stat of T-ff.

if $\Delta\Phi \neq 0$
T must b 1

③ $T(J, K, \Phi) = \Sigma(3, 4, 6, 7)$



$$T = \bar{J}Q + KQ$$

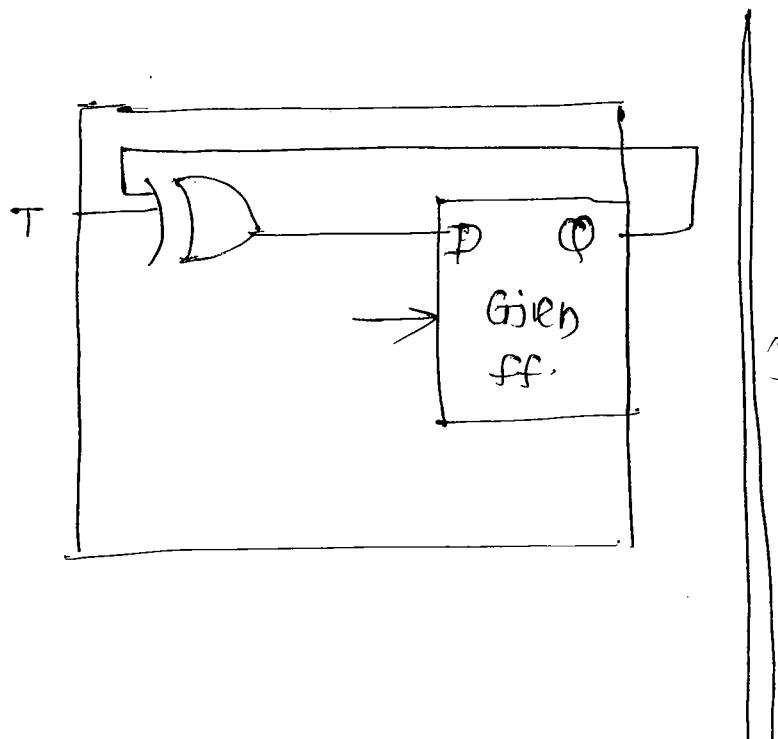


i.e. connect the D-ff into T-ff. \Rightarrow

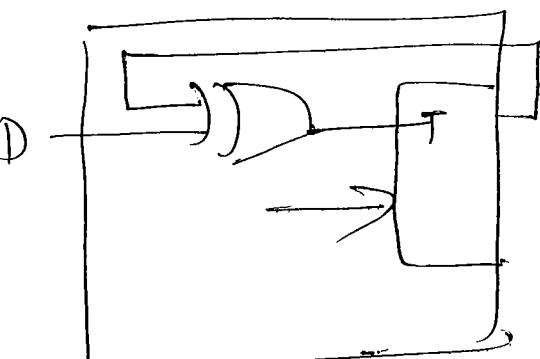
T	Q	Qn	D
0	0	0	0
0	1	1	1
1	0	1	1
1	1	0	0

$$\textcircled{2} \quad D = Qn$$

$$\begin{aligned} \textcircled{3} \quad D(T, Q) &= \bar{T}Q + T\bar{Q} \\ &= T \oplus Q. \end{aligned}$$

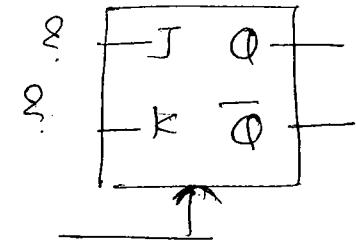
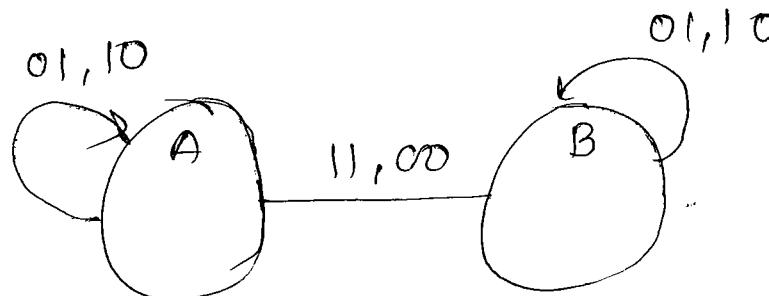


Connect T-ff \rightarrow D-ff



2004
 Ques. Consider a Mealy X-Y whose state diagram is given below. Realize this Mealy using JK.

X-Y:



X	Y	Qn
0	0	Q
0	1	Q
1	0	Q
1	1	Q

J K

- (a) $\bar{X}Y + X\bar{Y}$, $\bar{X}\bar{Y} + XY$
- (b) $\bar{X}\bar{Y} + XY$, $\bar{X}Y + X\bar{Y}$
- (c) $\bar{X}\bar{Y} + XY$, $XY + \bar{X}\bar{Y}$
- (d) $\bar{X}Y + X\bar{Y}$, $\bar{X}Y + X\bar{Y}$

X	Y	Q	Qn	J	K
0	0	0	1	1	0
0	0	1	0	0	1
0	1	0	0	0	0
0	1	1	1	0	0
1	0	0	0	0	0
1	0	1	1	0	0
1	1	0	1	1	0
1	1	1	0	0	1

$Q \rightarrow Q_n$	J	K
$0 \rightarrow 0$	0	0
$0 \rightarrow 1$	1	0
$1 \rightarrow 0$	0	1
$1 \rightarrow 1$	0	0

$$J(X, Y, Q) = \sum (0, 6) + \sum_{\phi} (1, 3, 5, 7)$$

$$K(X, Y, Q) = \sum (1, 7) + \sum_{\phi} (0, 2, 4, 6)$$

209 @

6-8.30	OS
9-1	Eng

$$\begin{array}{l} J = \overline{X}\bar{Y} + X\bar{Y} \\ K = \overline{X}Y + XY \end{array}$$

Shortcut ⇒

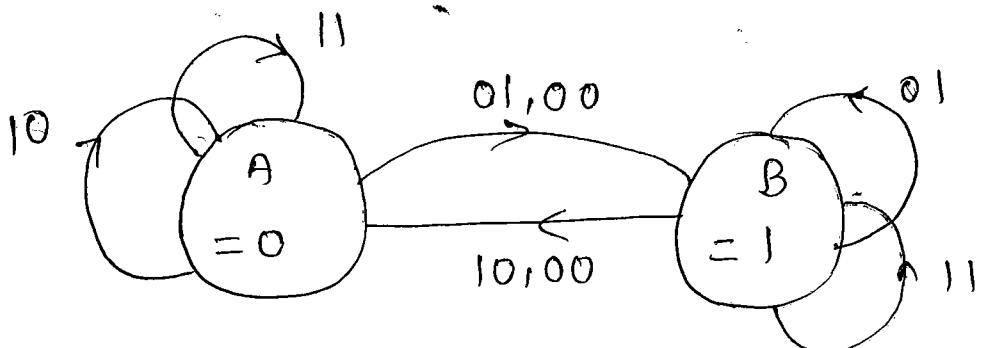
X	Y	Q_n	J	K
0	0	0	1	1
0	1	0	0	0
1	0	0	0	0
1	1	1	1	1

$\left. \begin{array}{l} J=K \\ \text{expression} \end{array} \right\}$

$$\underline{J = \overline{X}\bar{Y} + X\bar{Y} = K}$$

XY:

08/08/2012



If it is realized by
JK-FF expression for J & K.

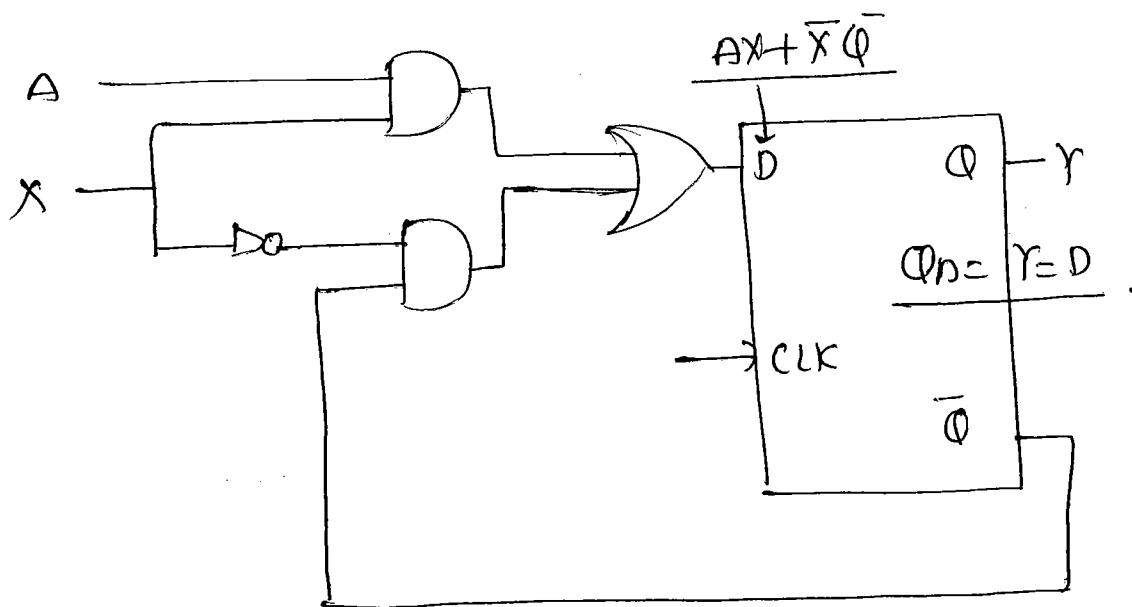
X	Y	Q_n	J	K
0	0	0	1	1
0	1	1	1	0
1	0	0	0	1
1	1	0	0	0

$$J = \overline{X}\bar{Y} + X\bar{Y}$$

$$\underline{J = \bar{X}}$$

$$K = \overline{X}\bar{Y} + X\bar{Y}$$

$$\underline{K = \bar{Y}}.$$



Let $X = 101100$

$A = A_1 A_2 A_3 A_4 A_5 A_6$ what is Y .

$$Q_n = Y = D = AX + \bar{X}Q$$

$$Y = A \quad \text{if } X=1$$

$$= \bar{Q} \quad \text{if } X=0.$$

$$\boxed{Y = A_4}$$

CLK	1	2	3	4	5	6
X	1	0	1	1	0	0
A	A_1	A_2	A_3	A_4	A_5	A_6
Y	A_1	\bar{A}_1	A_3	A_4	\bar{A}_4	<u>A_4</u>

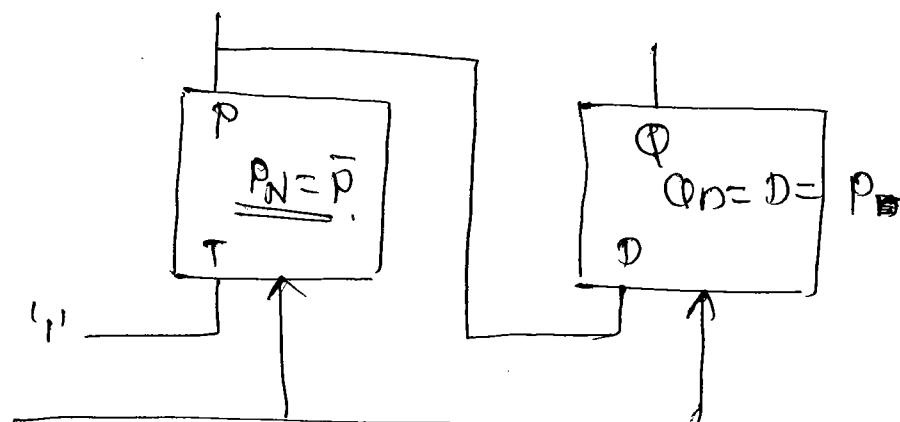
Ques. Consider the following sequential circuit in which initial values of P, Q are 0's. What will be their values after 3 clock cycles.

a) 01

~~b) 10~~

c) 11

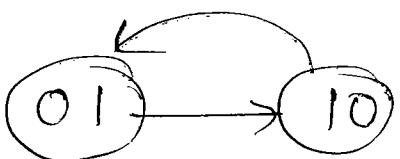
d) 00



PS	NS
P Q	P _N Q _n
00	1 0
→ 01	1 0
1 0	0 1
1 1	0 1

$$P_N = \bar{P}$$

$$Q_N = P$$



COUNTERS

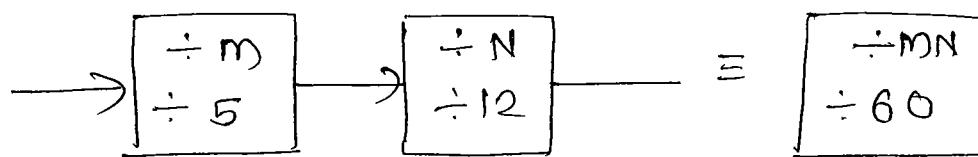
2/4 marks

- The counters are used to provide accurate, timing / control signals
- The synchronous counters gives the fast response and they are suitable for RT. Application
- In the, Synchronous Counter → All the flipflop are operated with the same clock
- In Asynchronous Counter, the O/P of one flipflop drives the clock of another.
- Asynchronous counters are simple to implement
- Most of the IC counters belongs to Asynchronous.
- A mod-5 counter contains 5-states in the counting path.
It divides the clock frequency by a factor five.

→ Hence, it is also called as divided by 5-counted.

$$f_{\text{counted}} = \frac{f_{\text{clk}}}{5}$$

→ When the two counters of the modulus m & n are cascaded the resultant counter will have MN modules (used in RT clock applⁿ)



→ The counters are used to generate the sequences, the repetitive length of sequence is equal to the modulus.

e.g. A mod-6 counter is used to generate, the following sequence.

101100 101100 1011...

mod-6 counter ⇒ for sequence geneⁿ

0111110

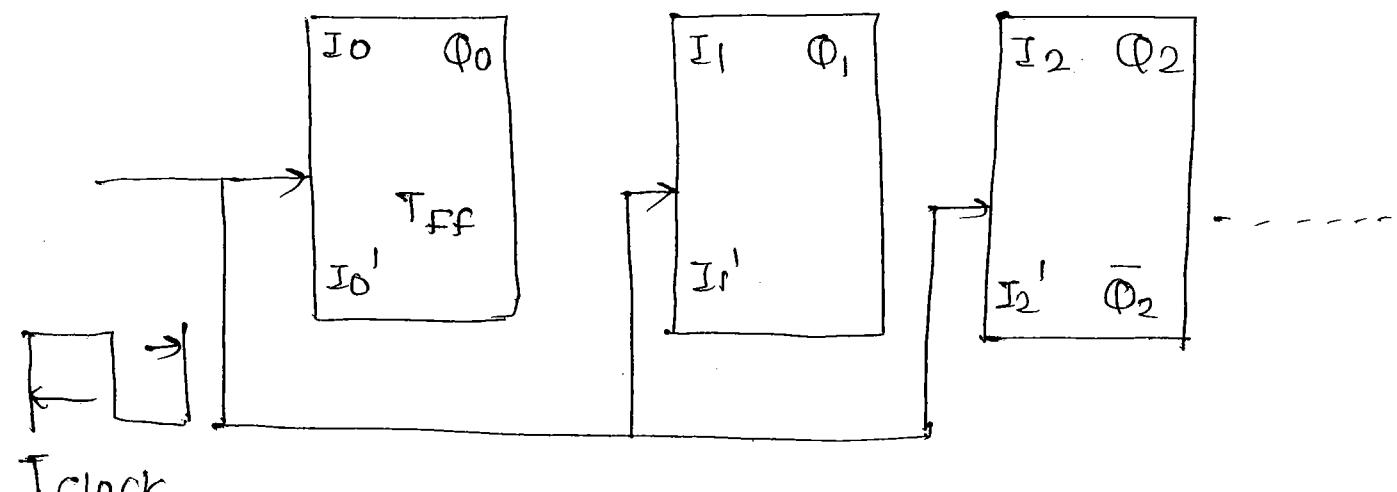
mod-8 ⇒ in data communication.

→ A counter is said to be self-starting if it performs the counting irrespective of initial state.

→ A counter is said to be free-running if it visits all possible states in counting path.

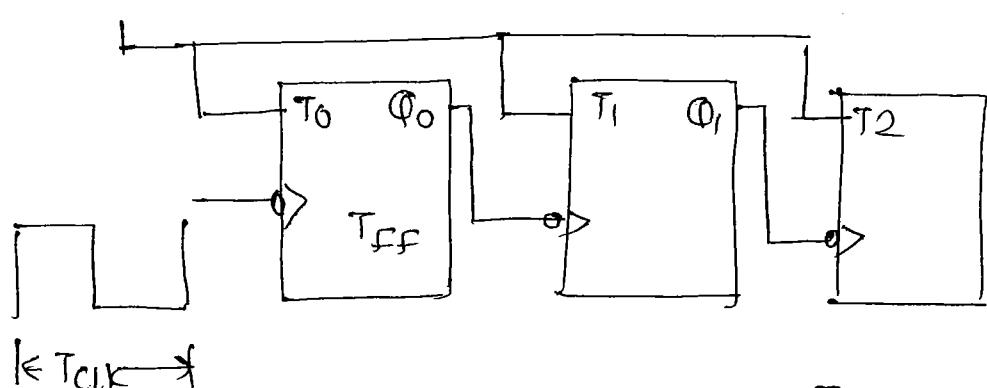
- Every free-running counter is self-starting but not every every vice-versa.
- The shift counter is the modified version of synchronous counter.
- The basic ff in shift counter is **D-ff**.
Further simplification, the shift counter will result in Ring counter, Johnson counter (Twisted Ring).
- The ring counter is used to provide Round-Robin scheduling.
- The specific instance of the ring counter can be treated as DECODER.
- The Johnson counter generates Gray counting.
- The n-bit Johnson counter provides $2^n - \text{gray}$ counting.
 $\text{mod}(2^n)$.

Synchronous Counter (more design complexity)



$$T_{clock} \geq [T_{ff} + T_{comb}] \leftarrow \text{propagation delay.}$$

$T_{pd.}$



Asynchronous

~~gated counter~~

$$\frac{T_{CLK} \geq N * T_{FF} + T_{Comb}}{N \rightarrow \text{No. of flip-flops.}}$$

* In synchronous counter \Rightarrow

- more design complexity,

$$I_i = f(Q_0, Q_1, Q_2, \dots, Q_{n-1}) \quad 0 \leq i \leq n-1.$$

$$I_0 = f(Q_0, Q_1, Q_2, \dots, Q_{n-1}) \quad \leftarrow \text{only initial } \begin{matrix} \text{ff} \\ \text{flip} \end{matrix}$$

Shift
counter
(D-ff)

$$I_i = Q_{i-1}$$

$$\text{ie. } I_1 = Q_0, I_2 = Q_1, \dots, i \leq 1 \leq n-1.$$

$$\underline{Q_n = D}$$

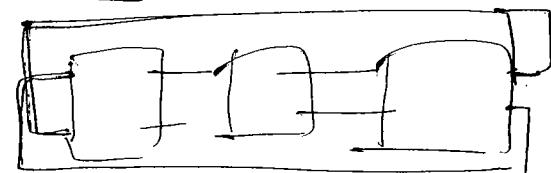
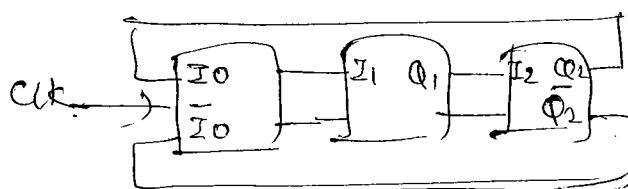
$$\underline{I_0 = f(Q_{n-1})}$$

$$\underline{I_0 = Q_{n-1} \text{ or } I_0 = \overline{Q_{n-1}}}$$

\downarrow
(RING counter)

\downarrow
(JOHNSON counter)

\downarrow
twisted counter



No. of fflops $\Rightarrow 2^n$ modulus.

Due to reduction in formula.
Reduction in modulus

RING COUNTER $\Rightarrow n$ fflops $\Rightarrow n$ modulus



n fflops $\Rightarrow 2n$ modulus. \Leftarrow Johnson

3 \longrightarrow 6 modulus

\uparrow
 $\text{mod}(6)$ gray counting

synchronous

Costliest counter.

Synchronous Counter \Rightarrow Design proc-

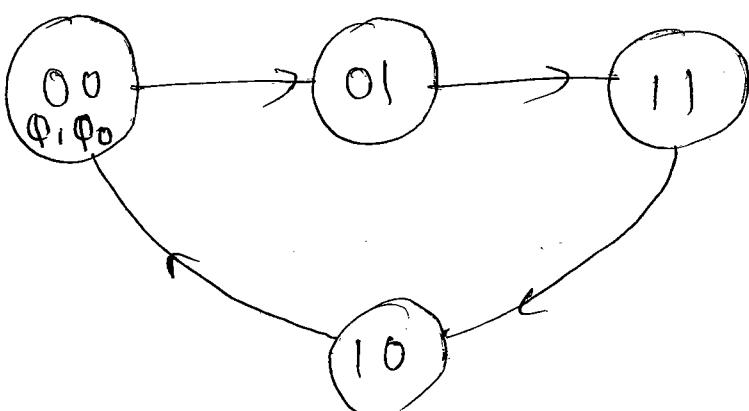
Step-1) Get the state diagram and obtain state table for the concerned counter

2) Identify the no. and type of flip-flops

3) Replace the concerned next state using excitation table of associate ff.

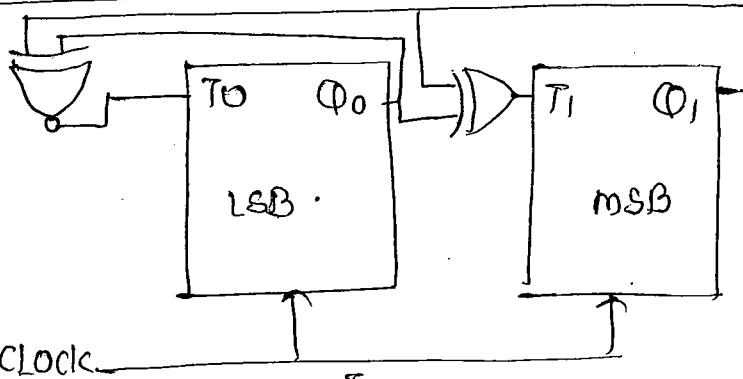
4) Get the expression for the f/f's and realize them.

* mod-4 gray counter $\Rightarrow n(\cdot 4)$ states = $\log_2 n$ ff's,

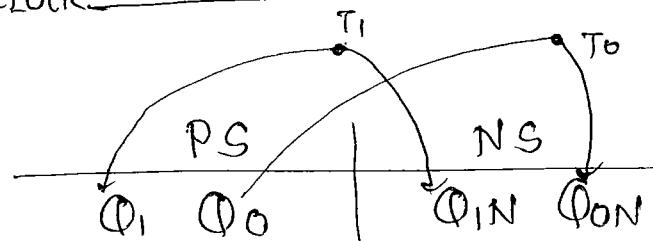


state diag

$Q, T\text{-ff} \rightarrow$



$\Delta\Phi \neq 0$
 $T=1$



← obtain from state diagram.

$\Delta Q=0 \rightarrow$	$0 \quad 0$	$0 \quad 1$	$1 \quad 0$	$1 \quad 1$
$\Delta\Phi \neq 0 \quad \{$	$0 \quad 1$	$1 \quad 0$	$0 \quad 1$	$1 \quad 0$
$\Delta Q=0$	$1 \quad 1$	$0 \quad 0$	$1 \quad 1$	$0 \quad 0$

State table

$$T_1(Q_1, Q_0) = \overline{Q}_1 Q_0 + Q_1 \overline{Q}_0 = Q_1 \oplus Q_0$$

$$T_0(Q_1, Q_0) = \overline{Q}_1 \overline{Q}_0 + Q_1 Q_0 = Q_1 \odot Q_0$$

Que. In the above problem, If D-ff's are to be used what will be the expression for D₀ & D₁.

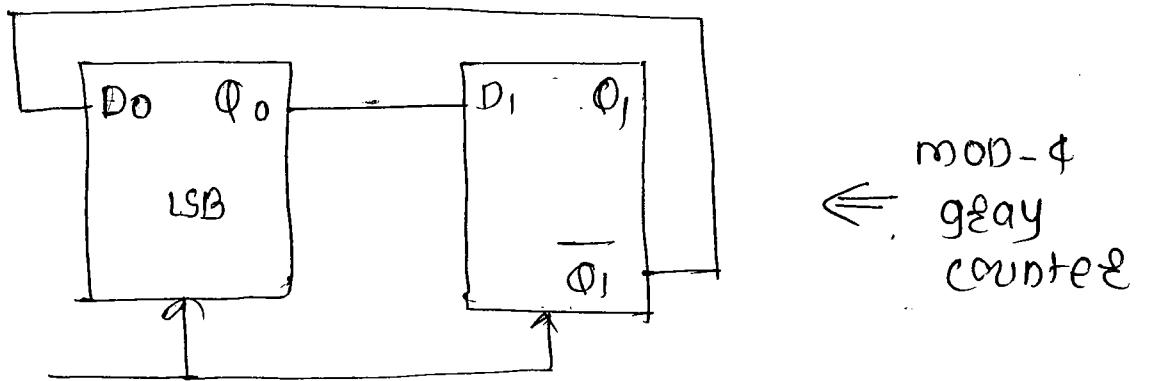
$$D_0 = Q_{0N}(Q_1, Q_0) = \overline{Q}_1 \overline{Q}_0 + \overline{Q}_1 Q_0$$

$$\boxed{D_0 = Q_{0N}}$$

$$\boxed{D_1 = Q_{1N}}$$

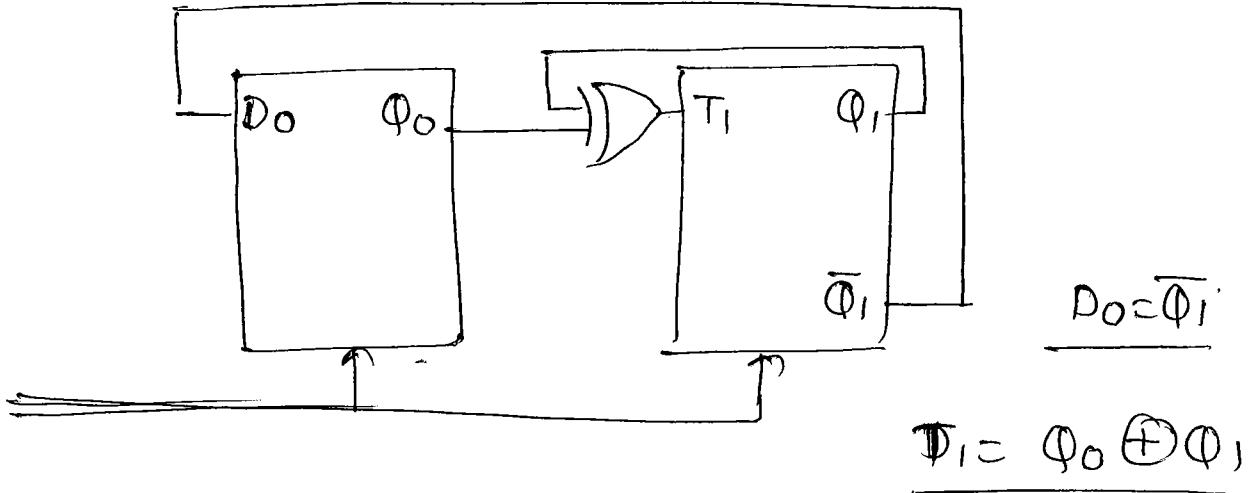
$$D_1 = Q_{1N}(Q_1, Q_0) = \overline{Q}_1 Q_0 + Q_1 \overline{Q}_0 = \overline{Q}_1 \oplus Q_0$$

$= \overline{Q}_1 \oplus Q_0$

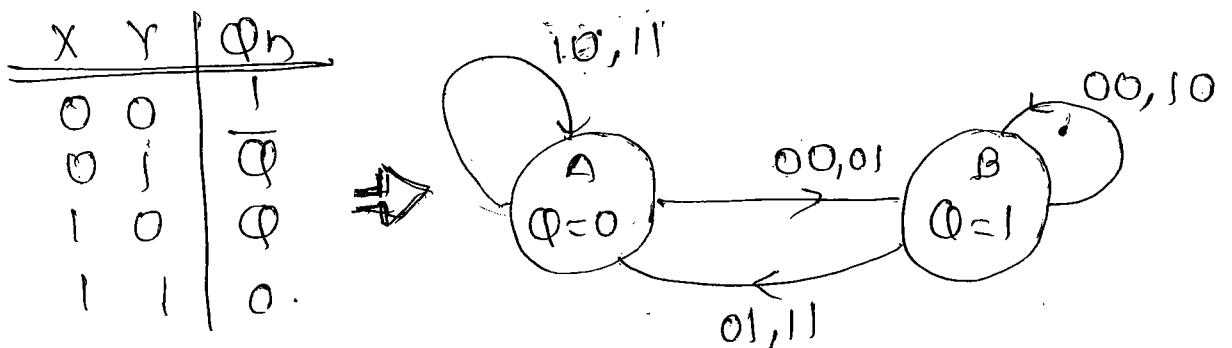


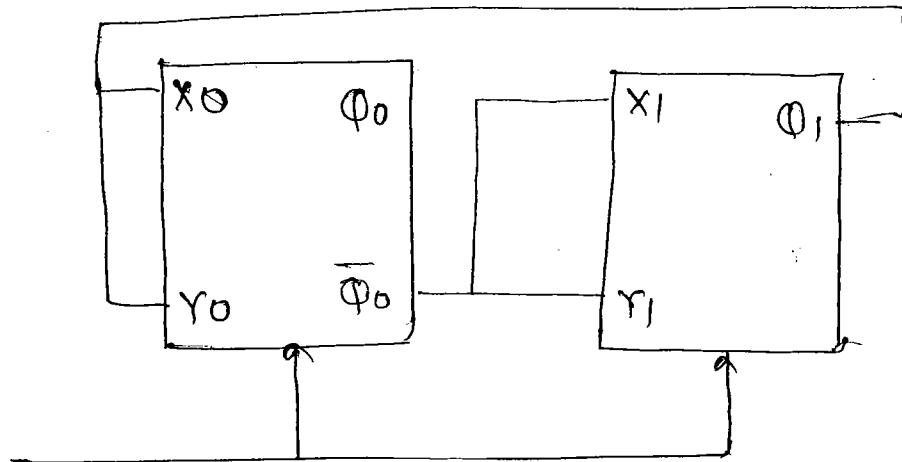
Johnson Counter \Rightarrow

Ques. The above counter is to be realized so that,
MSB must be given by T -flip-flop & $LSB \rightarrow D$ flip-flop.



Ques for the above problem, it is required to use XY-ff's, the behavior is given below.





$$x_i = f(\phi_1, \phi_0) = Y_i$$

ϕ_1	ϕ_0	ϕ_{in}	ϕ_{out}	x_i, Y_i	x_0, Y_0	Y_1
0	0	0	1	1, $\phi \Rightarrow$	0, $\phi^{(0,1)}$	00
0	1	1	1	0, ϕ	0, 0	01
1	0	0	0	$\phi, 1 \Rightarrow$	1, $\phi^{(0,1)}$	11
1	1	1	0	$\phi, 0$	1, 1	10

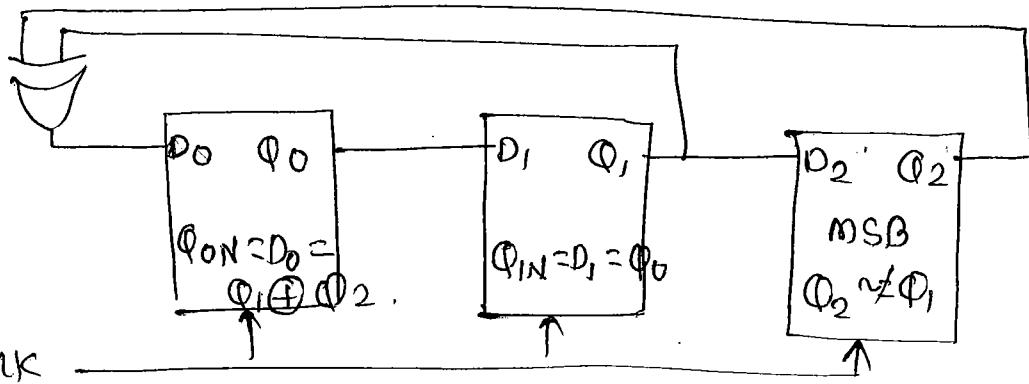
1 bit change
 1 bit use
 10, $\rho \Rightarrow$
 two bit change.

$$\begin{aligned} x_1 &= \overline{\phi_1} \overline{\phi_0} + \phi_1 \overline{\phi_0} = \overline{\phi_0} \\ Y_1 &= \phi_1 \overline{\phi_0} + \overline{\phi_1} \overline{\phi_0} = \overline{\phi_0} \end{aligned} \quad \left. \right\} = \underline{\overline{\phi_0}}$$

$$x_0 = \overline{\phi_1} \overline{\phi_0} + \phi_1 \phi_0 = \phi_1$$

$$Y_0 = \phi_1 \underline{\phi_0} + \overline{\phi_1} \underline{\phi_0} = \circled{(\phi_0)} \phi_1$$

$$\therefore \underline{x_0} = \underline{Y_0} = \underline{\phi_1}$$

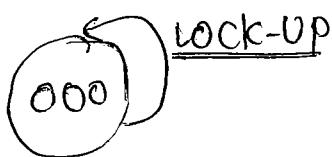


- 1) If initial state Q₂Q₁Q₀ is 101 that will be the state of above sequential mc after 5 clocks $\underline{001}$.
- 2) what is the counting sequence $\rightarrow S_0 \rightarrow S_7 \rightarrow S_6 + S_4 \rightarrow S_1 \rightarrow S_2$
- 3) Is the counter is self starting or free running
- 4) what is the max. useable clock frequencies if ff delay is 15 ns and exor delay is 5 ns.

\rightarrow

	$\overset{\text{PS}}{\curvearrowleft}$			Q _{2N}	Q _{1N}	Q _{0N}
	Q ₂	Q ₁	Q ₀			
S ₀	0	0	0	0	0	0
S ₁	0	0	1	0	1	0
S ₂	0	1	0	1	0	1
S ₃	0	1	1	1	1	1
$\xrightarrow{\text{initial state}}$ S ₄	1	0	0	0	0	0
S ₅	1	0	1	0	1	0
S ₆	1	1	0	1	0	1
S ₇	1	1	1	1	1	1

Counting sequence diagram showing the state transitions from S₀ to S₇. The states are represented by binary numbers: 000, 011, 111, 110, 101, 010, 001, and 100. Transitions are indicated by arrows labeled 'PL' (parallel load).



* mod7 counter can be enable, so it is not a self starting counter, initial state is zero & cannot give mod7 counter.

\rightarrow At the end of 20 ns all the flipflops get the valid input.

$$T_{clock} \geq T_{ff} + T_{com}$$

↓

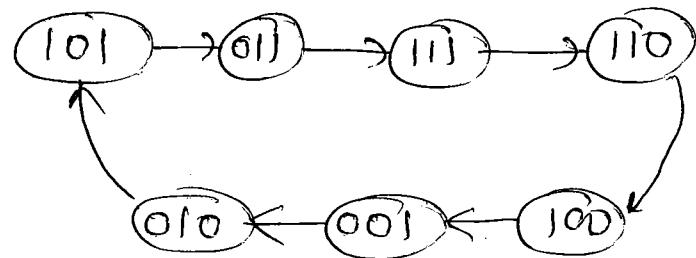
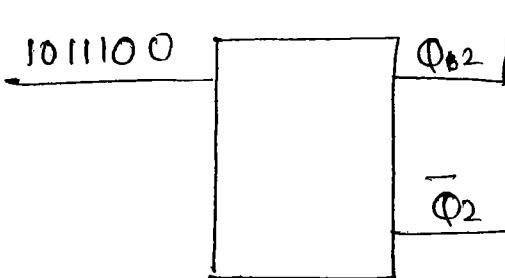
$T_{clock\ min} = T_{pd}$

$T_{pd} \Rightarrow$ Propogating delay.

$$f_{clock\ max.} = \frac{1}{T_{clock\ min}} = \frac{1}{20\ ns/cycle} = \frac{1}{20 \times 10^{-9}\ sec}$$

$$= \frac{10^9}{20} \text{ Hz} = \underline{\underline{50\ MHz}}$$

* If output is taken Q_1, Q_2 what is sequence generated.



* How many sequences can be generated from above problem.

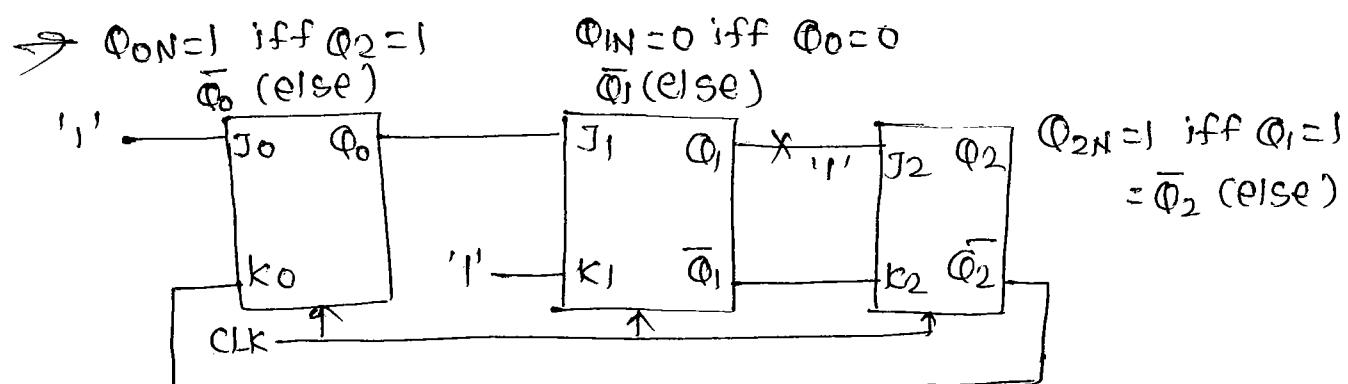
$$\rightarrow = 6 \text{ independent} \\ = 2 \times 3 \text{ (no. of flipflop)} = 2 \times 3 = \underline{\underline{6}}$$

* In the above counter, it is designed to have 6 modulus counter frequency what is the clock frequency which can produce this

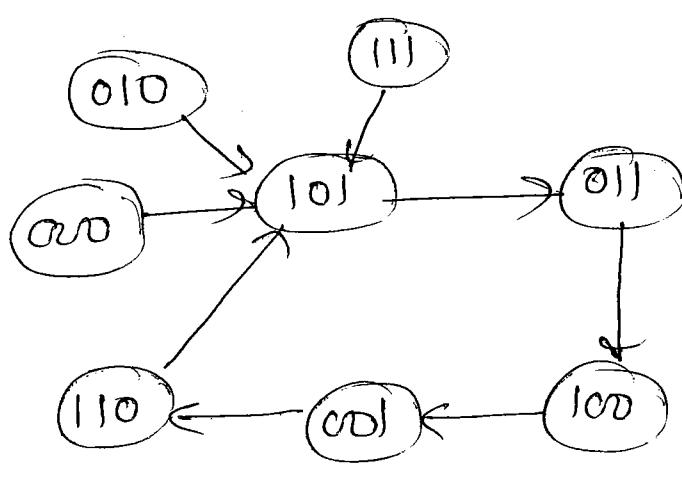
$$\rightarrow f_{counter} = \frac{f_{clk}}{\text{modulus of Counter}}$$

$$6\text{ M} = \frac{f_{clk}}{7}$$

Ques. Consider the following synchronous counter when P1 will get back initial state.



PS			NS		
Q_2	Q_1	Q_0	Q_{2N}	Q_{IN}	Q_{0N}
0	0	0	1	0	1
0	0	1	1	1	0
0	1	0	1	0	1
0	1	1	1	0	0
1	0	0	0	0	1
1	0	1	0	1	1
1	1	0	1	0	1
1	1	1	1	0	1



\Rightarrow self starting counter.

* What is the max. delay for setting the people counting?

\Rightarrow The max. delay needed for people counting is equal to 1 clock.

Ques. Consider the following counter configuration with all bits set initially.

\Rightarrow i) what will be the total no. of distinct states represented by the counter.

- a) 3 b) 4 c) 5 d) 6.

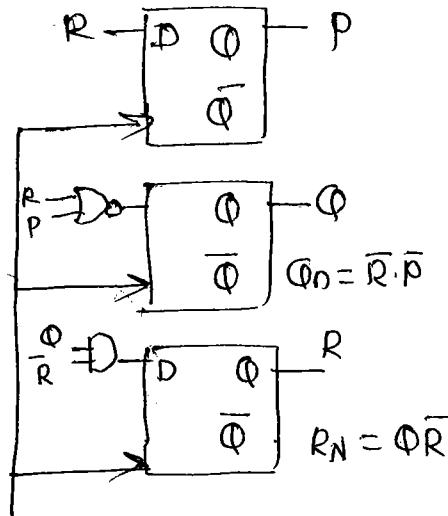
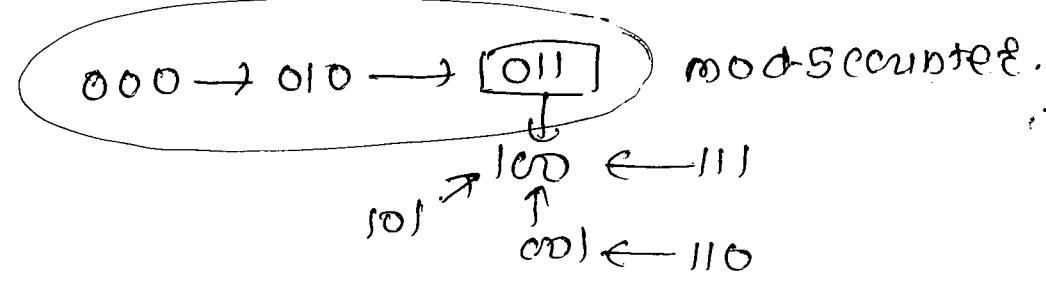
ii) If initial state is 010 what will be the state of the counter after the clock '8'

a) 000

b) 001

c) 010

d) 011

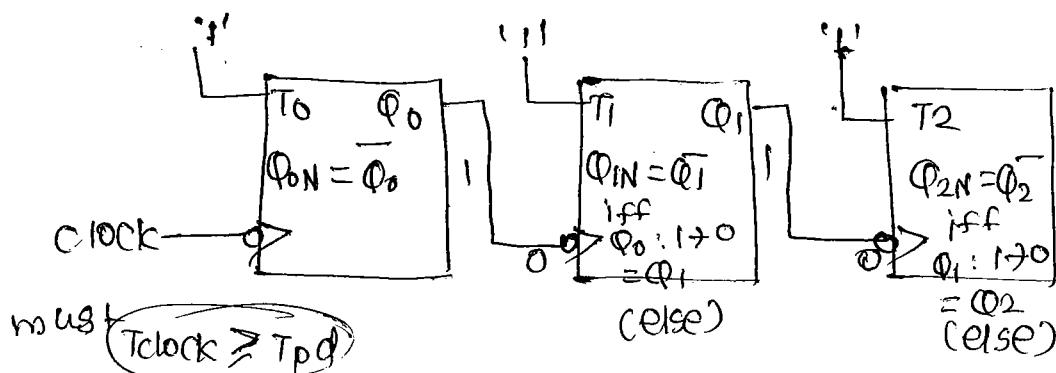


PS			NS		
P	Q	R	P _N	Q _N	R _N
0	0	0	0	1	0
0	0	1	1	0	0
0	1	0	0	1	1
0	1	1	1	0	0
1	0	0	0	0	0
1	0	1	1	0	0
1	1	0	0	0	1
1	1	1	1	0	0

⇒ self starting counter.

* Asynchronous Counter *

- Asynchronous Counter uses T-ff in toggle mode as the o/p of 1 ff gives the clock to the next ff. The clock will pass as ripple from the ff to another. Hence the Asynchronous Counter is called as ROLLER Counter.
- Due to the simple design complexity, they are preferred in IC fabrication. The natural counting is binary up counting. The up and down counter are used for incrementation and decrementation either involve a timer.

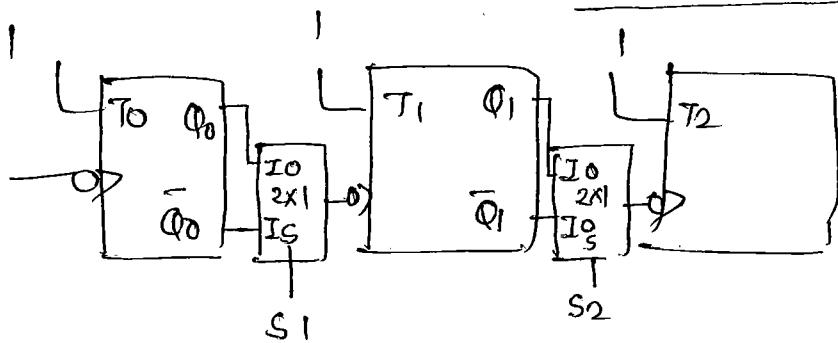


$$T_{pd} = N * T_{ff} + T_{comb}$$

PS			NS		
Φ_2	Φ_1	Φ_0	Φ_{2N}	Φ_{1N}	Φ_{0N}
0	0	0	0	0	1
0	0	1	0	1	0
0	1	0	0	1	1
0	1	1	1	0	0
1	0	0	1	0	1
1	0	1	1	1	0
1	1	0	1	1	1
1	1	1	0	0	0

$000 \rightarrow 001 \rightarrow 010 \rightarrow 011 \rightarrow 100$
 ↓ Bi-directional counting.
 $111 \leftarrow 110 \leftarrow 101 \leftarrow$

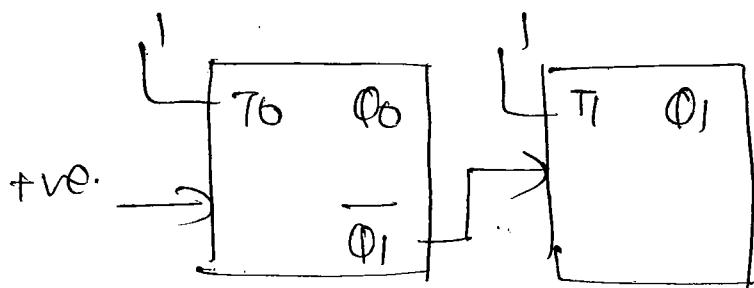
→ If place of negative edge if positive edge is used
 then it will perform binary down counting



$S_1 = S_2 = 0 \Rightarrow$ UP
 $S_1 = S_2 = 1 \Rightarrow$ DOWN
Controlled Up-Down Counter

CLK	CLK feedback	Natural counting
-ve	time	up
+ve	complement	up

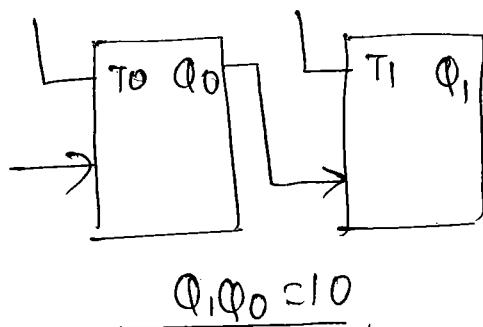
Ques. what will be the state of counter after two clock pulse with initial state 00



$$\Rightarrow 00 \rightarrow 01 \rightarrow \underline{10} \rightarrow 10$$

- a) 00
- b) 10
- c) 01
- d) 11

* Restricted modulus Asynchronous Counter & Digital - 1910812012



$10 \rightarrow 01 \rightarrow 00 \rightarrow 11$

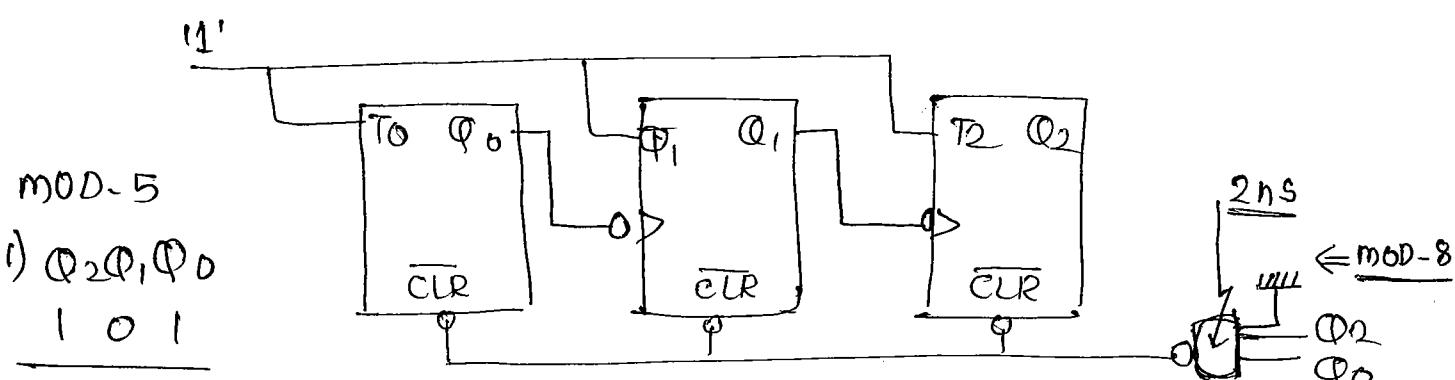
\Rightarrow self running / free running

mod-K, $K < 2^N$ (N --- Number of ff)

mod-5

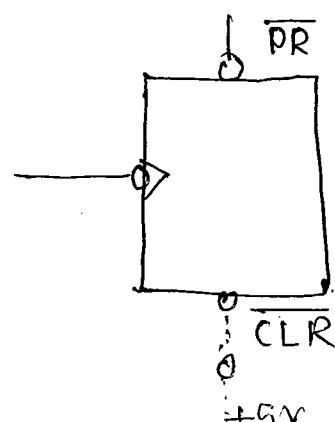
Design POC.

- 1) choose the suitable binary upcounter and initialize with it zeros
- 2) To restrict the modulus to K, get the binary pattern for and take those ff. O/p's which are 1 for that binary pattern.
- 3) Connect them to NAND gate. The O/p of the NAND gate is given to the clear i/p of all the ff's.



Nature \Rightarrow

Low active



connecting both PR & CLR to ground level (0) is not applicable

At least one of them should be '1'

Initial state in p&v. case is

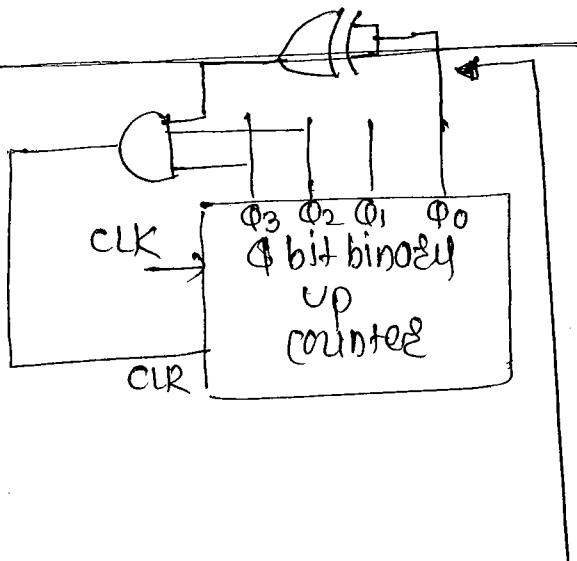
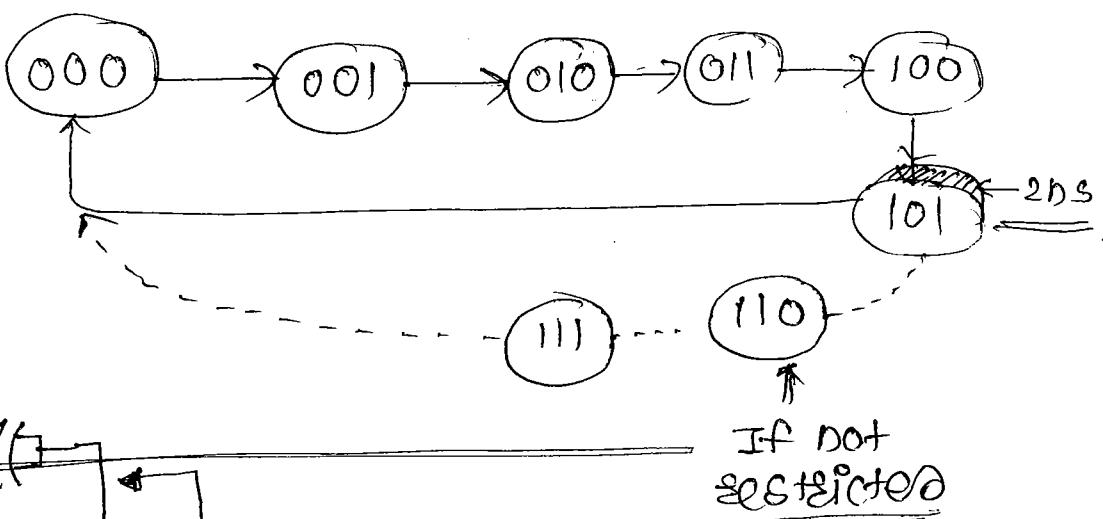
$Q_2\ Q_1\ Q_0$

0 0 0

Binary up

Complete duration
states = 5

Res. MOD 5. counter



\leftarrow MOD-12 counter.

$Q_3\ Q_2\ Q_1\ Q_0 \rightarrow$ connect with AND
 \downarrow
MOD-15 counter

This extension to above prob.
gives. MOD-16 Counter \leftarrow 2 4

Ques. - It is required to design MOD-29 counter. The 5 FF's A,B,C,D,E are used (A is MSB, E is LSB). What are the inputs to NAND gate for controlling low-active clear signal.

- a) ABE
- b) ACE
- c) ADE
- d) ACDE

$$16 + 4 + 2 + 1 = 23$$

16	8	4	2	1
1	0	1	1	1
<u>A B C D E</u>				

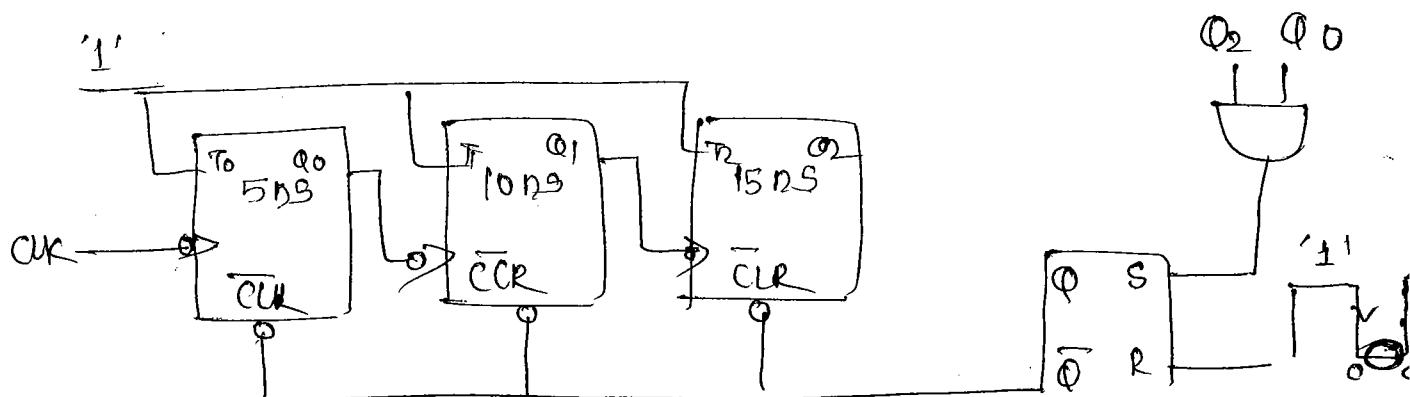
* The problem with NAND feedback *

If the FF's are not having uniform delay, there is a possibility of entering into a wrong state and performing wrong counting.

Ex. delay is max \rightarrow more time to respond.

Unequal delay \rightarrow insufficient duration of active clear signal

"The uneven delays result in insufficient duration of active clear signals. This problem is resolved using latch feedback. The clear signal is initiated by FF Q1's while it is terminated by external clock".



The presence of the latch extends active clear signal duration so that all FF's clear themselves. By adjusting external clock frequency, the duration of the clear signal can be controlled.

* SHIFT Registers → (SHR)

These are useful for performing arithmetic operation, the left shift operation result multiplication by 2 and right shift will perform division by 2.

- The registers are classified based on the direction of shift and also based on how the register is loaded and how the contents are read, the basic ff with shift reg. is D-flip-flop.

<u>used</u> <u>In Receiving end</u>	<u>n-bit SHR</u>		
	loading	reading	
S I S O	n	n-1	2n-1
S I P O	n	0	n } Data communication
P I S O	1	n-1	n }
P I P O	1	0	1 ← seq. only one clock fastest
<u>used</u> <u>In Transmitter end</u>			use PIP mode reads faster

A 82-bit shift reg. is operated with 1MHz clock and it is using PISO mode. How much time is req. for loading and reading the contents



1 ns for every clock

∴ 82 for 82 clocks

a) 1 us

b) 81 us

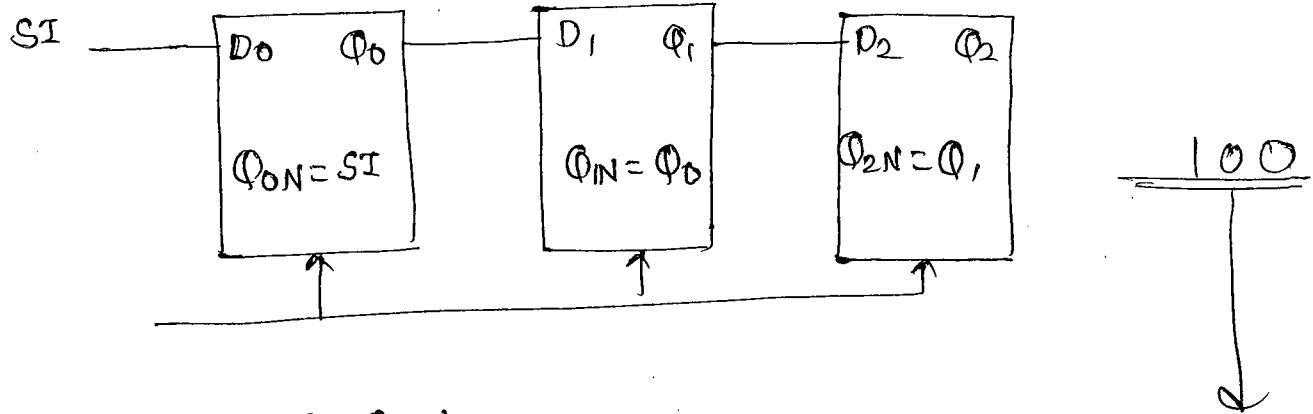
~~c) 82 us~~

d) 63 us

In PIP mode → 1 us

In SISO → 63 us

(Serial Isp)



Φ_k	Φ_2	Φ_1	Φ_0	Φ_{2N}	Φ_{IN}	Φ_{ON}
1	φ	φ	φ	1	φ	φ
2	φ	φ	1	0	φ	1
3	φ	1	0	0	1	0
4	1	0	0	φ	0	0
5	0	0	φ	φ	0	φ

$\Phi_2, \Phi_1, \Phi_0 \leftarrow SI$
Left shift

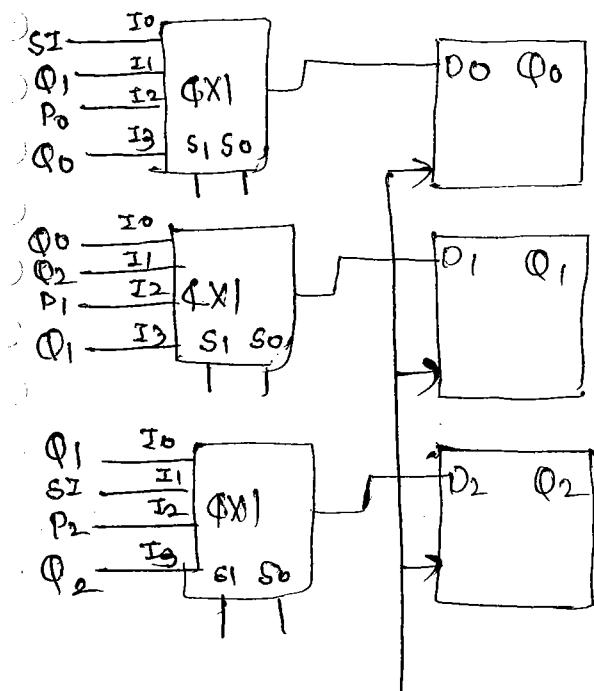
$$\Phi_2 = 1, \Phi_1 = 0, \Phi_0 = 0$$

→ 8 bit SHR taken 3-clocks to reach the desired state.
5-bit SHR → 5 clocks.

clk cycles(s) = Loading + Reading

SISO
 $2n-1 \Rightarrow 2(3)-1 = 5$
SIPo = 5

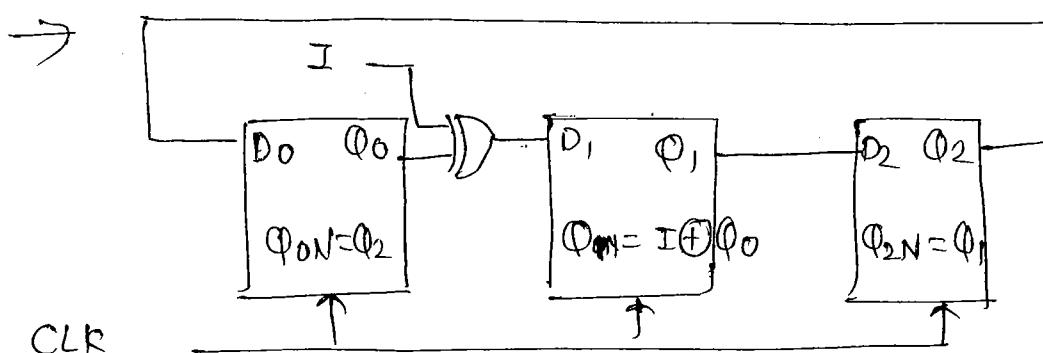
Universal SHR → It is capable of performing serial loading (left shift & right shift), parallel loading and latching.



<u>SISO</u>	function.	$D_2 D_1 D_0$
0 0	left shift	$Q_1 Q_0 S$
0 1	right shift	$SI \Phi_2 C$
1 0	parallel loading	$P_2 P_1 F$
1 1	latching	$\Phi_2 \Phi_1 G$

- $\Phi X 1$ map is taken coz we need 4 bit DFF

Consider the following SR flip-flop which is initialized as 101. The SI-I is applied with 11001. What will be the state of the register at the end of 5-clock pulses.



$$Q_2 Q_1 Q_0 = 101$$

XOR operation

LMP

CLK	PS			I	NS		
	Q ₂	Q ₁	Q ₀		Q _{2N}	Q _{1N}	Q _{0N}
1	1	0	1	1	0	0	1
2	0	0	1	1	0	0	0
3	0	0	0	0	0	0	0
4	0	0	0	0	0	0	0
5	0	0	0	1	0	1	0

In above P&D,

It is req. to have 100 at the end of 2nd clock
what will be initial state and what will be IP's

clk	PS			I	NS		
	Q ₂	Q ₁	Q ₀		Q _{2N}	Q _{1N}	Q _{0N}
1	1	0	0	1	0	1	1
2	0	1	1	0	1	0	0

Ans \Rightarrow

$$\begin{array}{c} \text{IP} = 01 \quad \boxed{101} \\ \text{OR} \end{array}$$

$$\text{and } \text{IP} \Rightarrow \underline{\underline{11}}$$

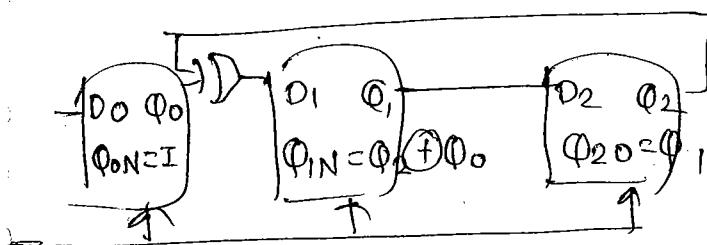
Above seq. having $IS = 000$ what will be state of seq. at the end of 9 clock cycles, so that the I/p-I is applied as [100H 00000]

a) 000

b) 001

c) 010

d) 101

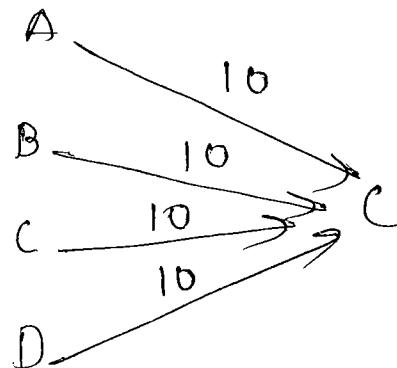


Consider the follo. seq. m/c. It is seq. to have the state as 'C' what will be min. no. of i/p bits ensure this.

PS	NS, Z $x=1$	$x=0$
A	B, 0	A, 0
B	B, 0	C, 1
C	B, 1	C, 0
D	C, 1	D, 0

- ✓ a) 10
 b) 01
 x c) 101 } asked.
 x d) 0110 } min. so
 neglect.

respecting to initial state, if i/p is 10, the m/c is landing in 'C' state



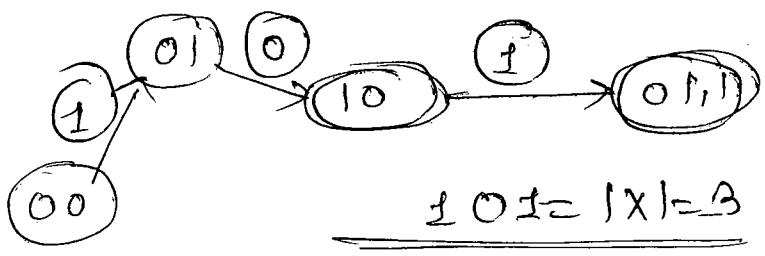
Given the state table of fsm with 2-states A & B, 1 i/p and 1 o/p.

- a) 6
 b) 5
 c) 4
 d) 3

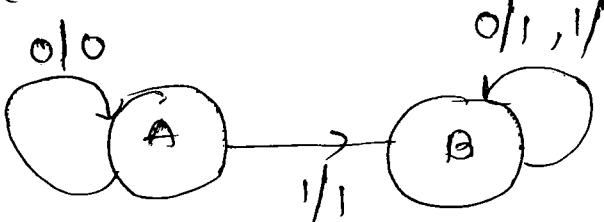
PS A B	NS, Z	
	$x=0$	$x=1$
0 0	00, 1	01, 0
0 1	10, 0	00, 1
1 0	01, 0	01, 1
1 1	10, 0	00, 1

$$A=B=0$$

what is the minimum length of input taken the machine $A=0, B=1, Z=1$



Ques. Consider the following seq. m/c. If the 1st bit i.e. is received is LSB. what is the funⁿ of the sequential m/c.



- (x) serial 1's comple.
- (x) serial incrementing
- 2's comple.
- (d) None.

$x : 1 \ 0 \ 0 \ 1 \ \downarrow$

B B B D A

$r : 0 \ 1 \ 1 \ 1$

$$\begin{array}{r}
 1001 \rightarrow 0110 \\
 + 1 \\
 \hline
 0111
 \end{array}$$

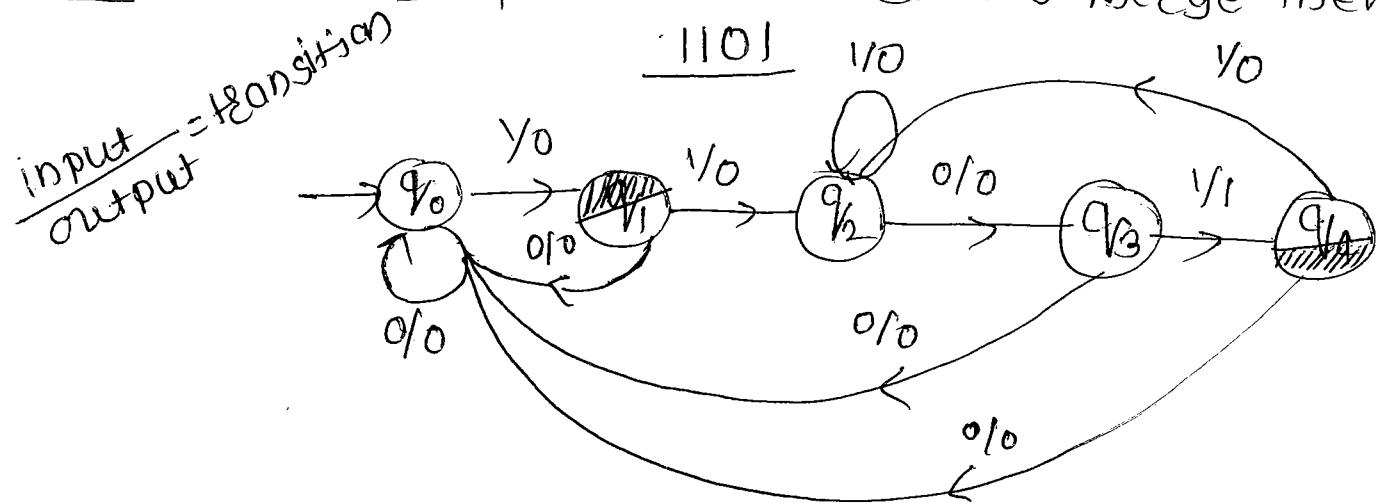
Sequence Detectors

Dig - 28/08/2012

- Sequence detectors are placed at receiving end to detect the presence of valid (the sequence detector) or invalid sequence (no sequence detector)
- Detection can use overlapping / Non-overlapping inputs
- No sequence detector detects a sequence of length N with less than N -states.
- On current state and current input, the next state can be.
 - i) initial state
(In case detection can not progress)
 - ii) That state which leads quick detection.

Seq. Det? pce.

- Step 1 - Construct the state diagram for the skeleton path
- Step 2 - Define the binary transition for each state
- Step 3 - Identify equivalent states and merge them



$$\Phi \text{ No. of states} = 4 = \text{length of } (1101) \quad \star$$

$q_{N, Z}$

p_s	$x=0$	$x=1$
q_1	$q_0, 0$	$q_2, 0$
q_4	$q_0, 0$	$q_2, 0$

$$\therefore \underline{q_1 = q_4} \quad \therefore \{q_0, q_1, q_2, q_3\}$$

Compatibility chart \rightarrow

p_s	$x=0$	$x=1$
q_0	$q_0, 0$	$q_1, 0$
q_1	$q_0, 0$	$q_2, 0$
q_2	$q_3, 0$	$q_2, 0$
q_3	$q_0, 0$	$q_4, 1$
q_4	$q_0, 0$	$q_2, 0$

q_1	q_1	q_2	
q_2	q_0, q_3	q_0, q_3	
q_3	q_1, q_2	q_0, q_3	X
q_4	q_1, q_2	\checkmark	q_0, q_3
	q_0	q_1	q_2
			q_3



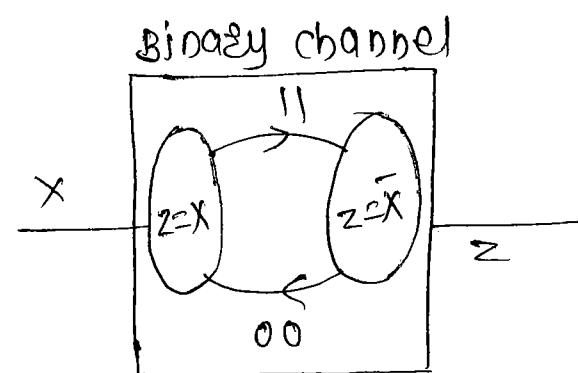
$$q_0 q_1 \rightarrow q_1 q_2 \rightarrow q_0 q_3 \rightarrow X$$

$-X \leftarrow X \leftarrow$

2 ff's are
equivalent to
expressed.

$$\Rightarrow \underline{\{q_0, q_1, q_2, q_3\}}$$

Consider a binary channel which has one i/p and one o/p. Initially the copy of i/p is presented at o/p. This will continue until the channel receives two consecutive 1's from then onwards complemented i/p is presented at o/p. The complement? continue until the channel receive 2 consecutive zero's from then onwards it repeats the behavior what will be the min. no. of states in this binary channel?



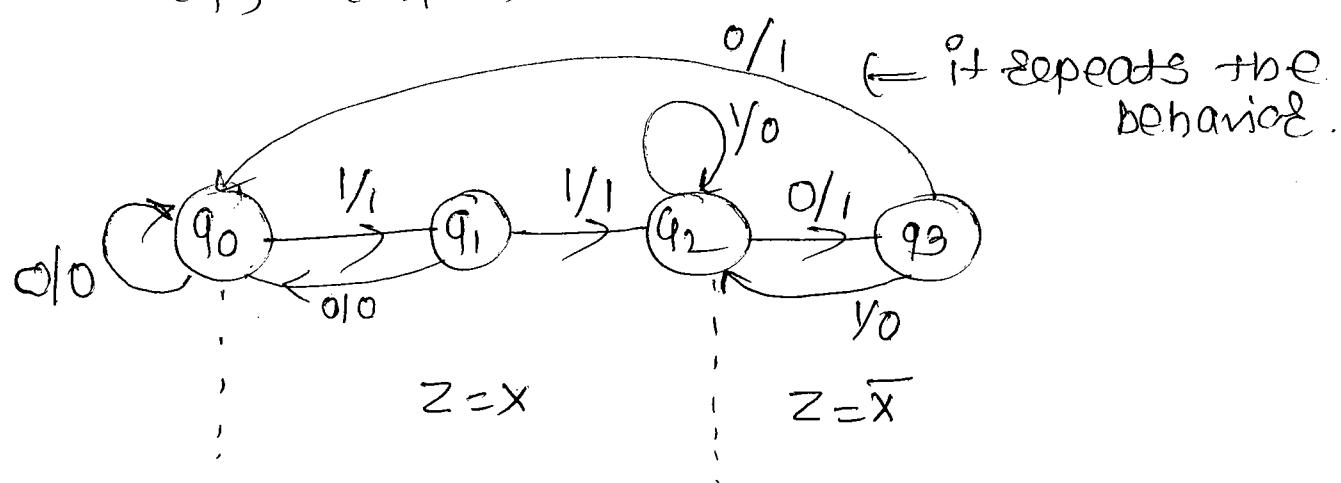
$$X @ 3 \quad \checkmark \text{ } 6 \\ X @ 5 \quad X @ 6.$$

$$\underline{1100} \Leftarrow 14$$

so, Ans will not be less than 4

$$X: 1011|10001 \\ Z: 1011|0\bar{0}\bar{0}01 \\ \begin{matrix} \uparrow & \uparrow \\ Z=X & Z=\bar{X} \end{matrix} \quad Z=X$$

copy complementation

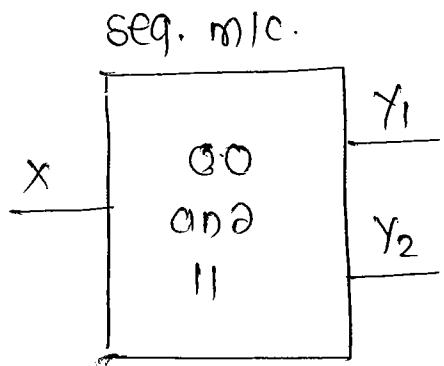


Consider a sequential m/c which has one ip and 2 o/p's. Initially the o/p y_1, y_2 are 0's, they will remain in the same state until one of the following event occurs.

- i) $z_k = Nk+2$ then k^{th} and subsequent ips the o/p $y_1, y_2 = 01$.
- ii) $Nk = z_k + 2$ then k^{th} and subsequent ips the o/p $y_1, y_2 = 10$

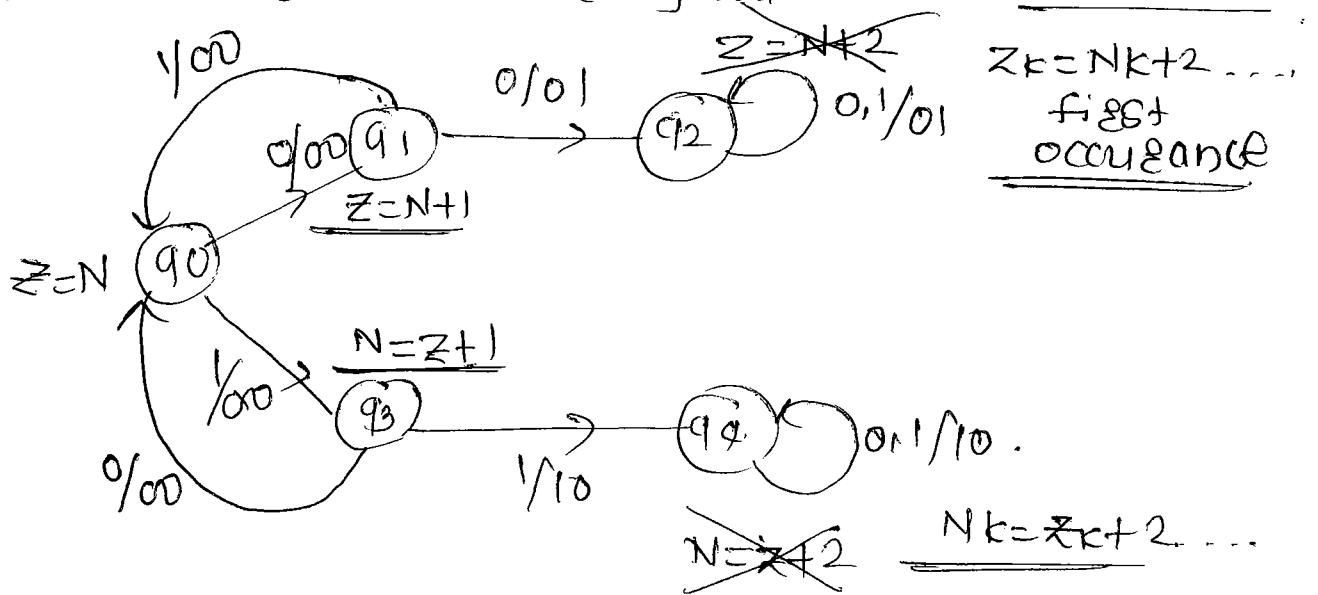
the z_k and Nk represent, No. of zeros and No. of 1's in first k bits. (if $x=101 \Rightarrow k=3, Nk=2, z_k=1$)
Count will be the min. no. states in this seq. m/c.

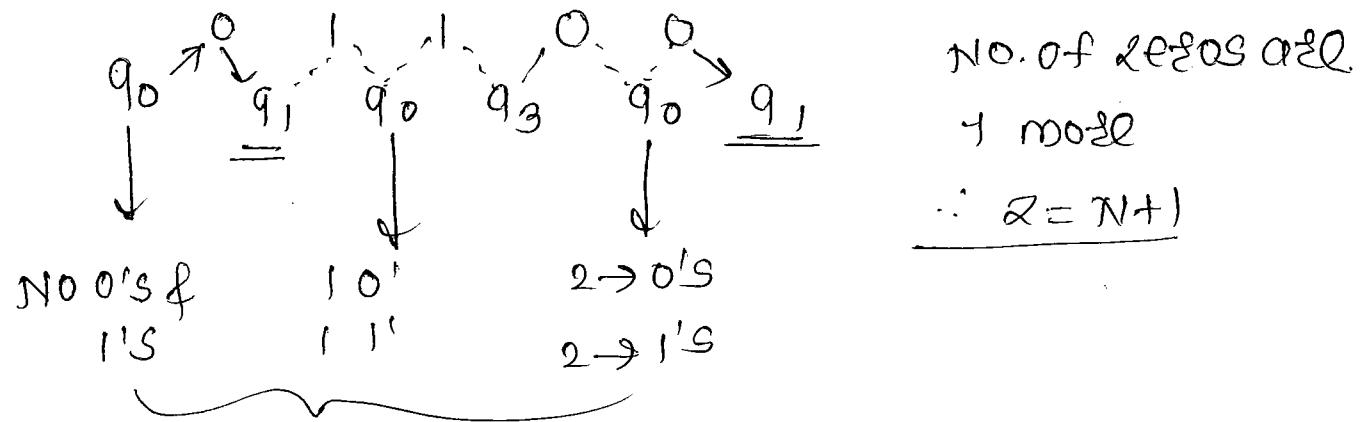
- Ⓐ 3 Ⓑ 4 Ⓒ 5 Ⓓ 6.



to satisfy event i)
min. value of $Nk=0$
and $z_k=2$
hence, first 2 bits
must be zeros.

Similarly, to satisfy the event ii) min. value of $z_k=0$
and hence $Nk=2$, 1st 2 bits must be 1's
Hence, this m/c has to recognise either 00 or 11





q_0 representing equal nos. of 0's & 1's

No state is meagable due to outputs all differing.

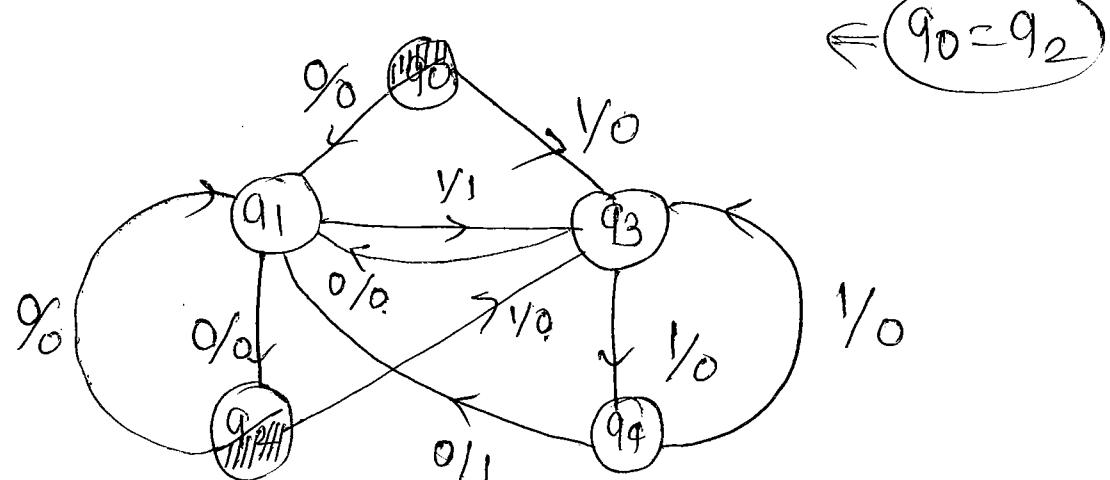
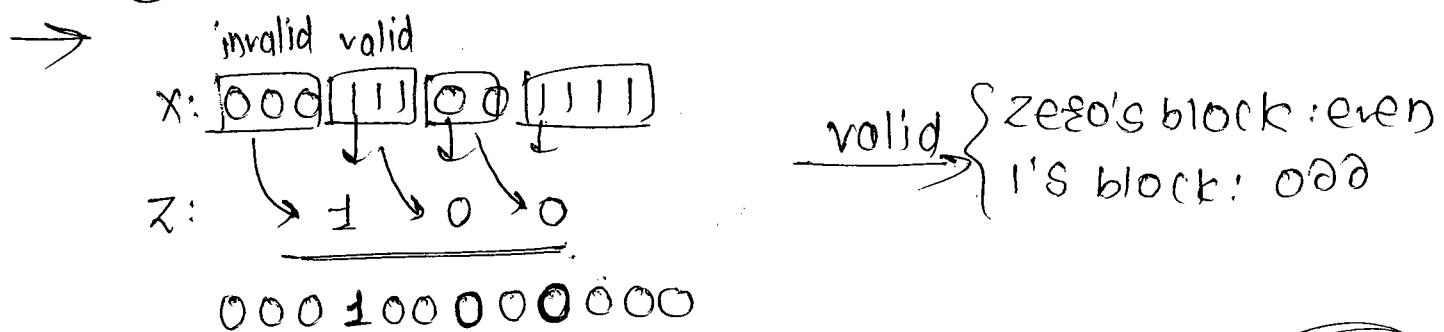
Que. Consider a seq. m/c. which has 1 ip and 1 o/p. for the valid operation no. of zeros received must be even and no. of 1's received must be odd. On any violation the o/p is set to 1 on the 1st bit of opposite block. What will be the min. no. of states in this seq. m/c.

(A) 3

~~(B)~~ 4

(C) 5

X(D) 6.



X: 0 1 0 1 0 1 0 1 0 1 0

Z: 1 0 1 0 1 0 1 0

what will min. no. of steps in excess-3 BCD detector.

- Ⓐ 8 9 10 16 ✓

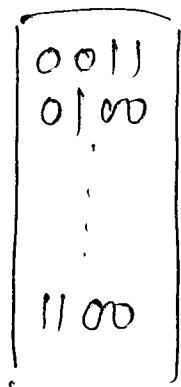
$$ADS \geq 10$$

0000
0001
0010
1101
1110
1111

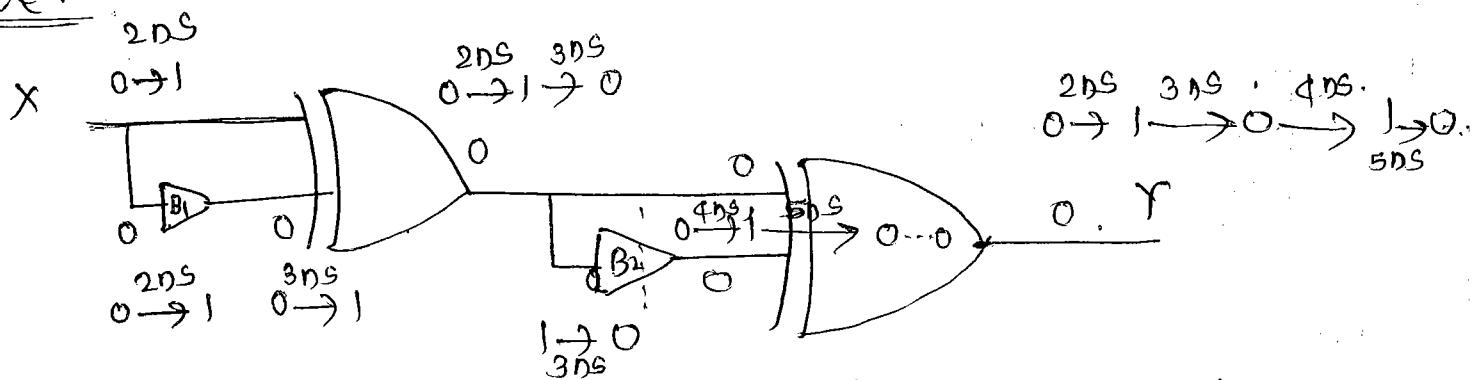
out of 16 → 6 are invalid

$\Rightarrow \frac{10}{16}$

valid
EX-3 BCD
seg.



Ques.



Except Buffers B₁ and B₂. No gate and NO connecting lead has delay, B₁ = 1 ns, B₂ = 2 ns delay
Initially all i/p's and o/p's are zero.

How many changes does Y takes due to X

- Ⓐ 3 ✓ ④
Ⓒ 5 Ⓞ 6

