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Post results on bSpace by 5:00 pm, 04/12/2013

EECS 141: CLASS PROJECT — PHASE 1 REPORT

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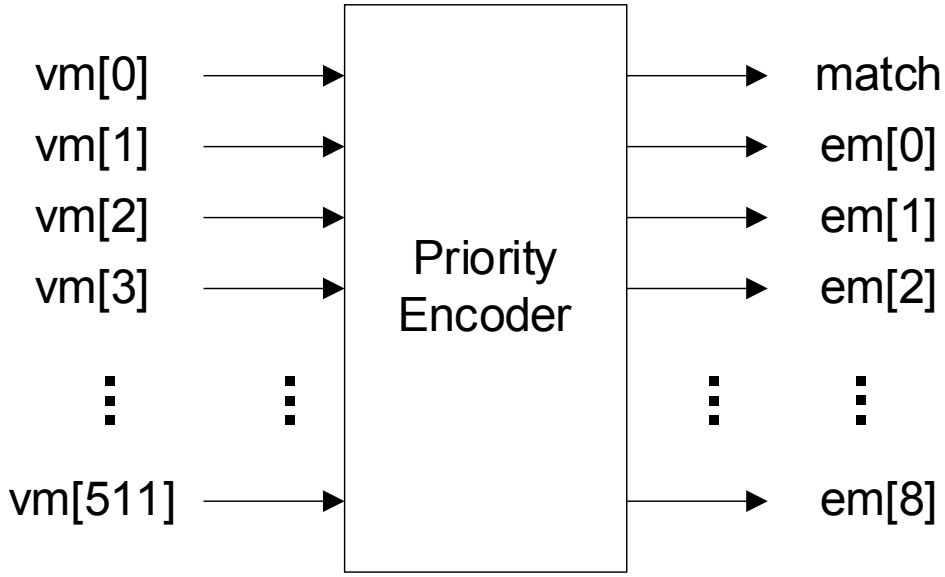
MAIN RESULTS:

Optimization Metric: *Power/ Energy.*

Parameters	**Values**	**Units**
Calculated Worst-Case Delay	0.55	*ns*
Simulated Worst-Case Delay	1.02	*ns*
Calculated Energy Consumption	498.70	*fJ*
Simulated Energy Consumption	347.34	*fJ*
Total Estimated Area	46,376	um^2



I. Executive Summary

We design our 512-input priority encoder with low-energy operation as the highest goal in mind. In order to come up with the schematic, we have decided to use static CMOS as our logic gates for two reasons. We want the supply voltage to be as low as possible because it is one major element that contributes to power dissipation. Therefore, the first reason for using static CMOS is that it does not use clocks like dynamic gates, which have to recharge capacitors every clock cycle and hence leads to high power dissipation. The second reason for using static CMOS is that we want to divide evenly the power dissipation for pull-down network and pull-up network so that there is often fixed power dissipation regardless of low-to-high or high-to-low situation.

Another key element for low-energy optimization in our design is capacitors. Because the total capacitance directly affects the power dissipation, we want to keep it as low as possible. Therefore, we keep all the capacitors as much low as allowed instead of sizing them as usual. This is the tradeoff between energy and delay. In this situation, we neglect delay by sizing all gates to be equivalent with a unit inverter as long as the total delay is below 40ns and rise and fall time is below 1ns.

Another design optimization we have done is to favor NAND and NOR gates in our design. Moreover, NAND4 and NOR4 are favored if possible. The reason is because NAND and NOR gates are simpler compared to AND, OR, XOR, which yield shorter paths and less capacitance. This could help us lower power dissipation.

In order to design and draw our schematic, we follow our guidelines as specified above and try to keep the schematic as modular as possible. We start with the smallest module, which is the 8:3 priority encoder (8 inputs, 3 outputs, 1 matching output) [Figure II.1]. We use 9 of these priority encoders, and 3 multiplexors [Figure II.2] for the next 64 inputs to yield 6 outputs and 1 matching output. Similarly, we use 8 of 64:6 priority encoders, 1 8:3 priority encoder, and 6 multiplexors for the next 512 inputs to yield 9 outputs and 1 matching output [Figure II.3].

Finally, we reduce the supply voltage V_{DD} down to 0.7 to have the lowest power dissipation while satisfying the design constraints.

Note that in this report, we use power dissipation and energy consumption interchangeably since they both denote the same optimization metric in our design.

II. Logic and Transistor Diagrams

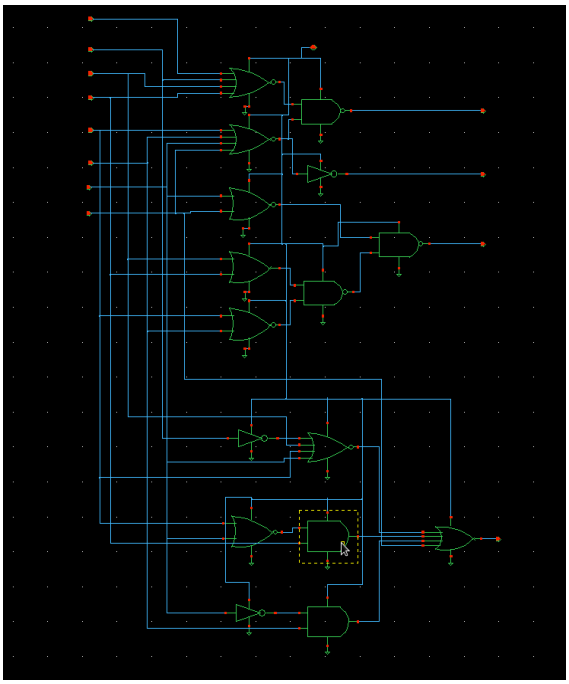


Figure II.1: 8:3 priority encoder

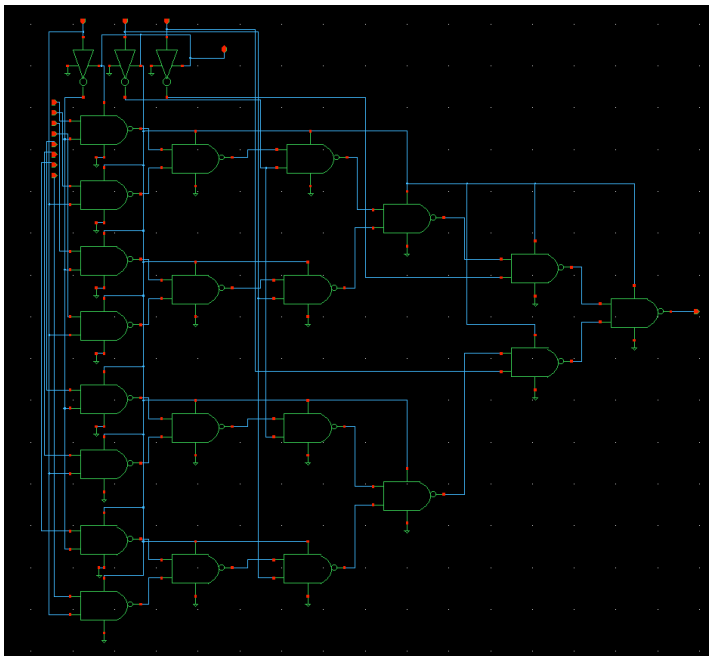


Figure II.2: Multiplexor 8:1

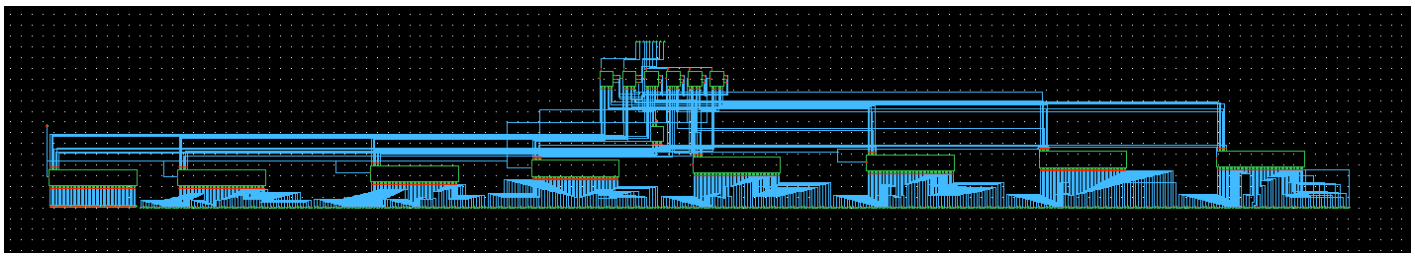


Figure II.3: 512:9 priority encoder

(*): See Appendix for examples of transistor-level diagrams and sizing.

Worst-case Delay Path Diagram:

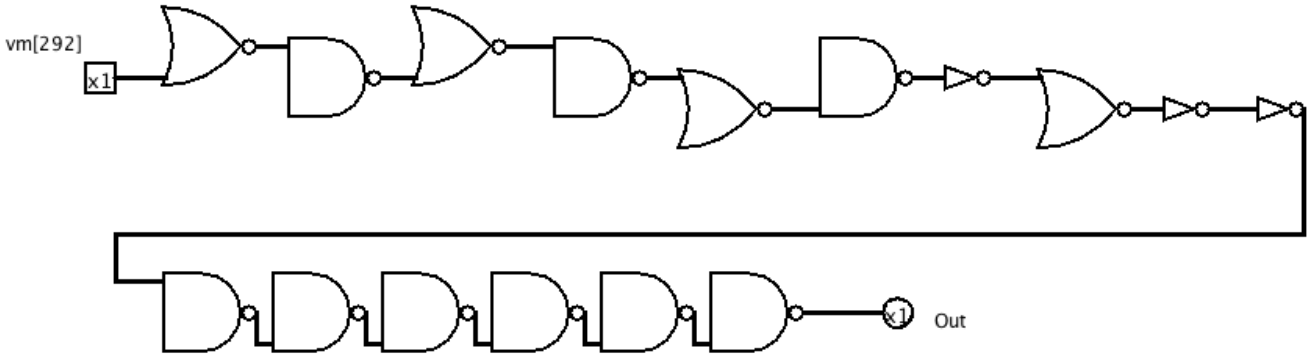


Figure II.4: transition 0->1 of vm [292] causes worst-case delay

Functionality Testing (input pattern under instruction):

t_d = 40 ns
net544 = em[0] = 1 at between 80 - 200ns.
net543 = em[1] = 1 at between 80 - 120ns and 160 – 200ns.
net542 = em [2] = 1 at between 160 – 200ns.
net541 = em [3] = 1 at between 80 – 200ns.
net540 = em [4] = 1 at between 80 – 160ns.
net539 = em [5] = 1 at between 120 – 200ns.
net538 = em [6] = 1 at between 120 – 200ns.
net537 = em [7] = 1 at between 160 – 200ns.
net536 = em [8] = 1 at between 160 – 200ns.
net535 = match = 1 at between 80 – 200ns.
Based on the plot, the *rise and fall time* is below 1ns and thus satisfies our design constraint.

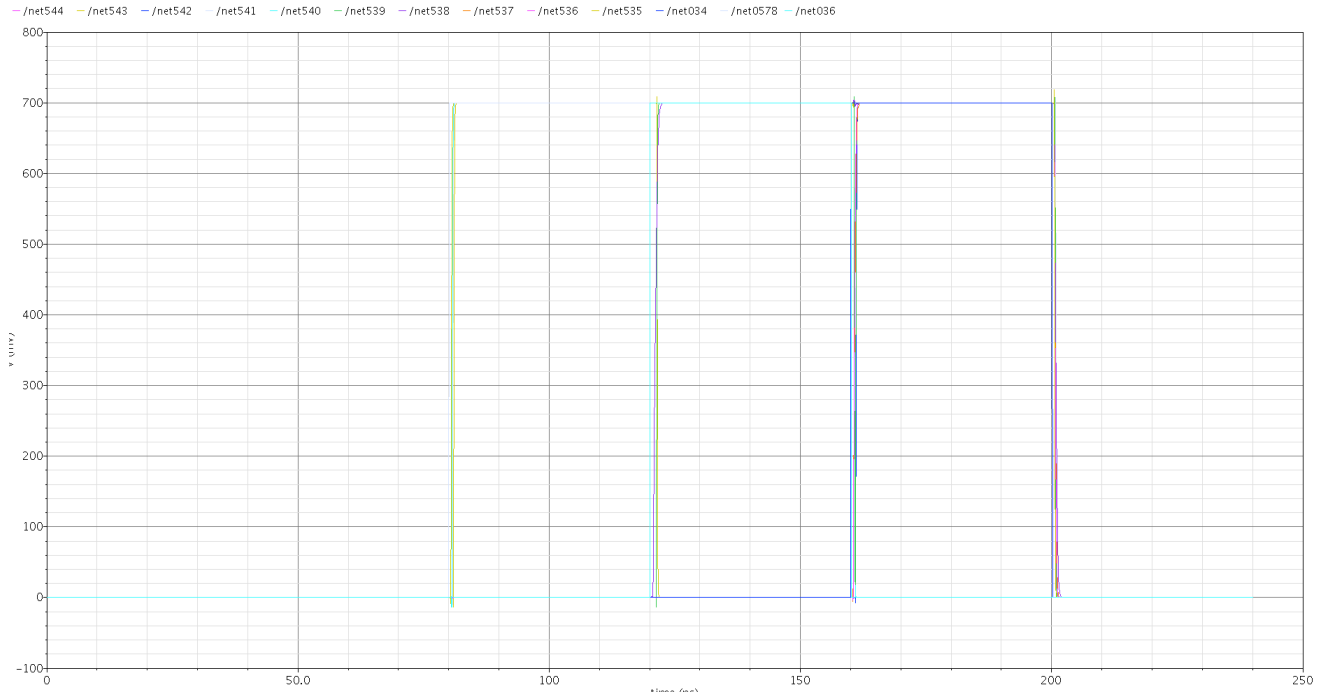


Figure II.5: Plot demonstrating that your design is functionally correct

III. Timing and Energy Simulations – Area Estimation

Noise Margins & VTC:

Let vm[27] sweep from 0 to 0.7V and the rest inputs are grounded. The output voltage of em[0] provided by the VTC plot is shown below.

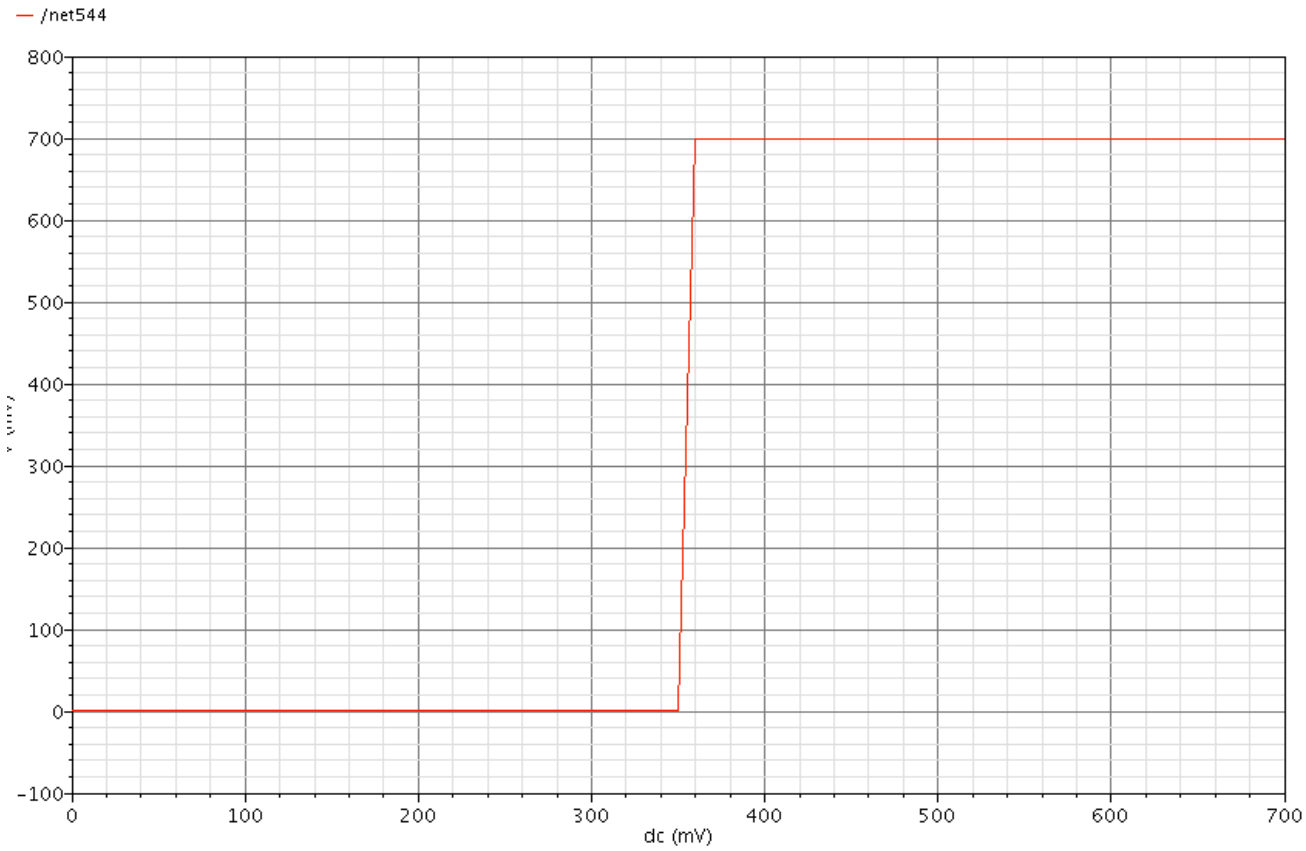


Figure III.1: $V_{OL} \approx 0$ V, $V_{OH} = 699.93$ mV.

Worst-case delay:

By Calculation: (vm[292] to em[5])

$t_{inv} = 3LR_{sq}C_g = 3 * 100nm * (9.43k\ \Omega + 22.32\ k\ \Omega) / 3 * 0.191fF = 6.064ps$

$t_p = \sum(p + LE.f) . t_{inv} = (4 * 4 + 2 * 9 + 3 * (0.982 * 3 + 0.871) + 4 / 3 * (2.855 * 2 + 1.355 + 5 * 1.696) + 2.07 + 1.4 + 1.736) * 6.064ps = 524.8ps$

With NOR4: p = 4, LE = 3; NAND2: p = 2, LE = 4/3; NOT: p = 1, LE = 1;

$f = C_{out} / C_{in} = (C_{g,\,out} + C_{d,\,in}) / C_{g,\,in}$

By Simulation: (vm[292] to em[5])

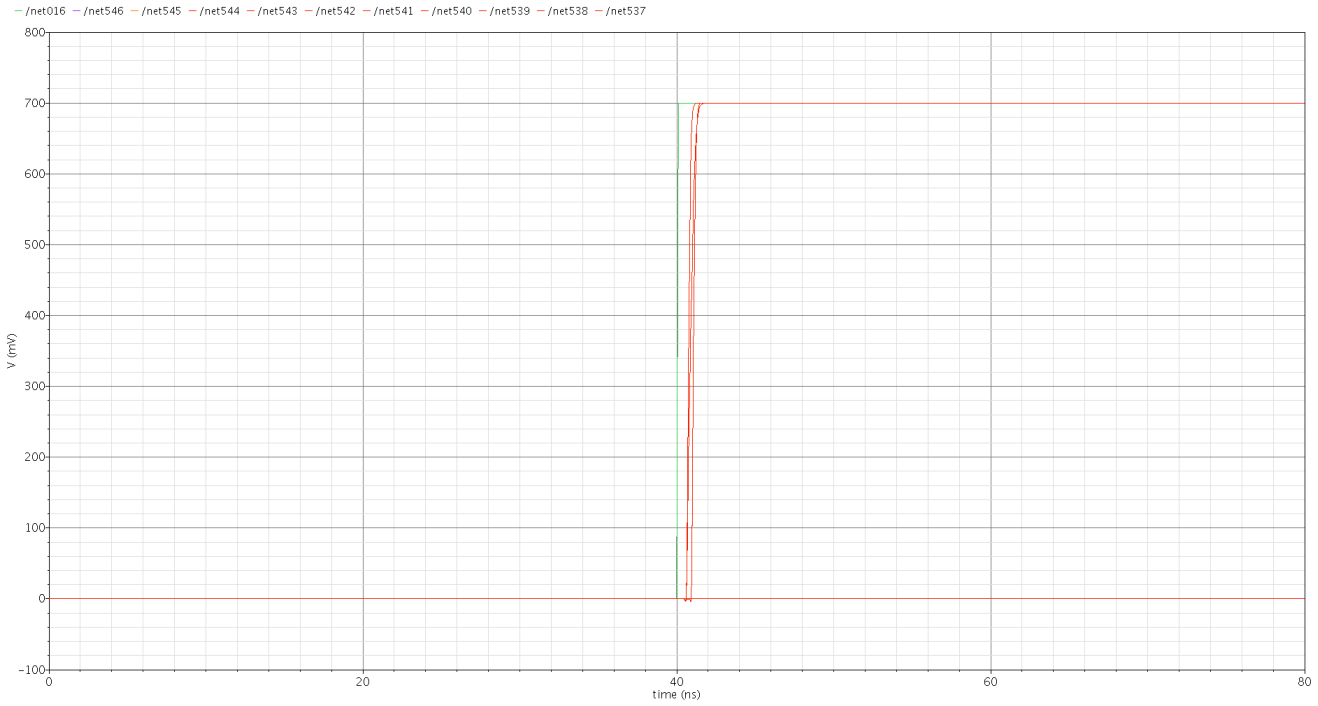


Figure III.2: Simulated worst-case delay t_p= 41.07ns – 40.05ns = 1.02ns

Power Dissipation:

By Calculation:

When all inputs switch from 0 to 1, the sum of capacitors that are going to be charged is:

Assume that the output capacitance of each pin is equivalent to the total gate capacitance of NAND2 gate (C_g = 1.91fF/um, C_d = 0.77 fF/um, W_p = 240 nm, W_n = 120 nm, L = 100 nm).

For the output pin $C_{out} = 12\ C_{g,\ NOT} = 12 * 1.91 * 0.12um * 3 = 8.25$ fF

For priority encoder 8:3 (NAND2, NOT, OR2, OR4):

$C_{L,\ 1} = C_{NAND2,\ g+NAND2,\ d} + C_{NAND2,\ g+NOT,\ d} + C_{NAND2,\ g+NAND2,\ d} + C_{NAND2,\ g\ +\ OR2,\ d} + C_{NAND2,\ g+OR4,\ d}$

$= 1.91 * 0.12um * 4 + 0.77 * 0.12um * 6 + 1.91 * 0.12um * 4 + 0.77 * 0.12um * 3$

$+ 1.91 * 0.12um * 4 + 0.77 * 0.12um * 6 + 1.91 * 0.12um * 4 + 0.77 * 0.12um * 9$

$= 6.162$ fF

For mux 8:1 (11 NAND2):

$C_{L,\ 2} = C_{NAND2,\ g+NAND2,\ d} * 11 = 11 * 1.4712 = 16.1832$ fF

For priority encoder 64:6 (9x priority encoders 8:3, 3x mux 8:1):

$C_{L,\ 3} = 9C_{L,\ 1} + 3C_{L,\ 2} = 9 * 6.162 + 3 * 16.1832 = 104.01$ fF

For priority encoder 512:9 (8x priority encoders 64:6, 1x priority encoder 8:3, 6x mux 8:1, 10x C_{out}):

$C_L = 8C_{L,\ 3} + C_{L,\ 1} + 6C_{L,\ 2} + 10 * C_{out} = 8 * 104.01 + 6.162 + 6 * 16.1832 + 10 * 8.25 = 1017.82$ fF

Energy consumption for the given input pattern (512 pins from 0 to 1):

$E = C_L * V_{DD}^2 = 1017.82 * 0.7^2 = 498.7$ fJ

By Simulation:

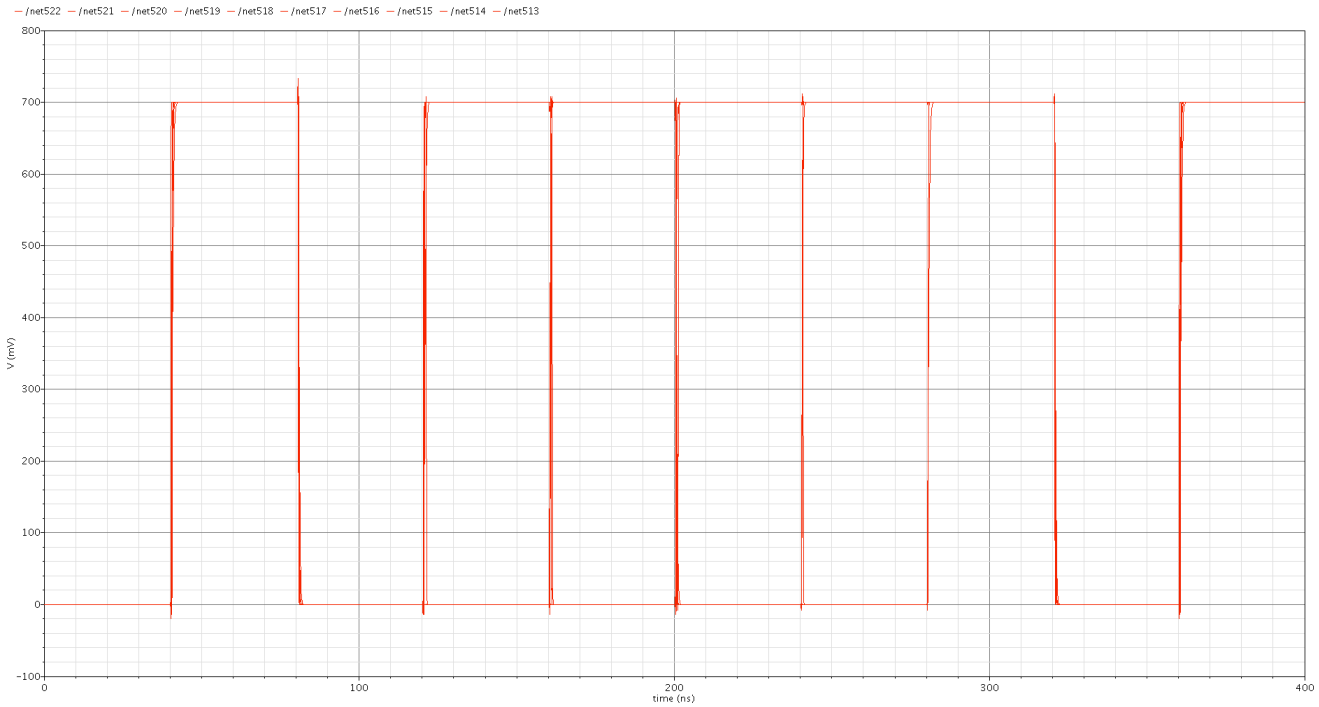


Figure III.3: Transient plot of 10 outputs for power

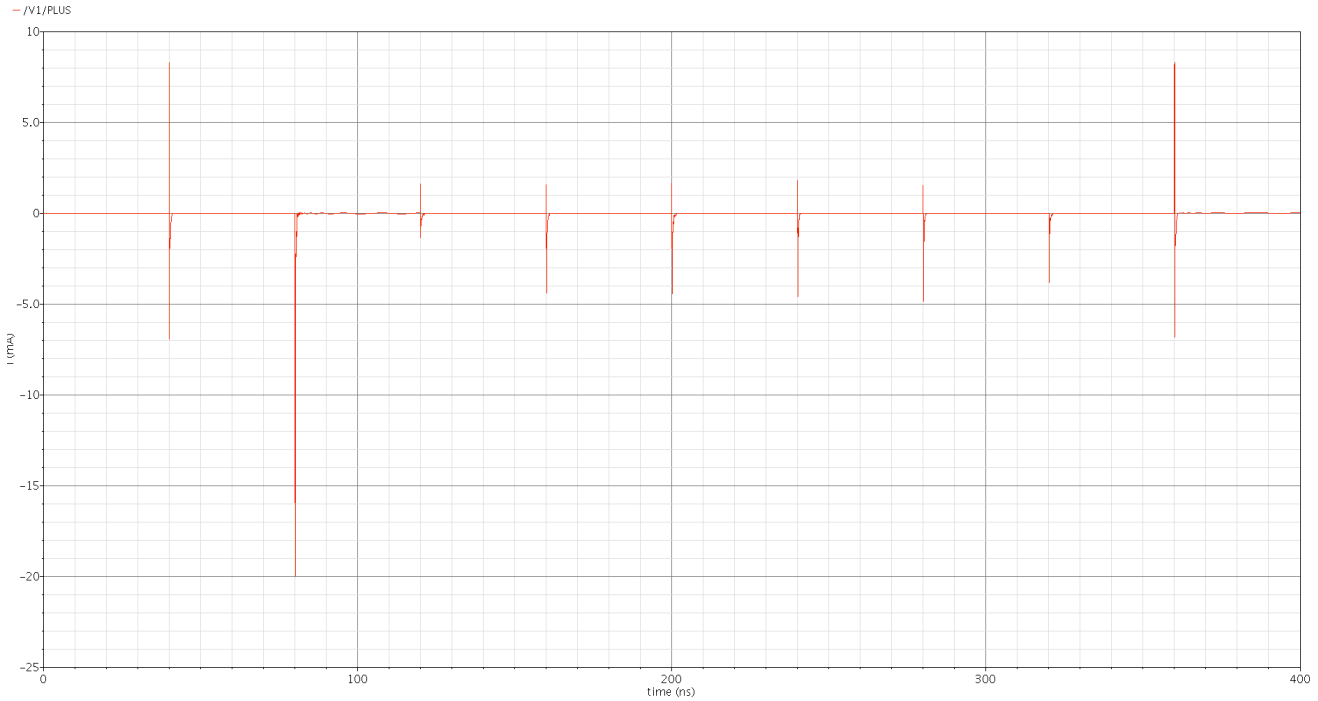


Figure III.4: Current drawn from voltage supply

Max current at 40ns is approximately 8.27 mA => $P = I_{DD} * V_{DD} = 8.27 * 0.7 = 4.96$ mW

Estimated energy consumption: $E = I_{DD} * V_{DD} * t = 8.27 * 0.7 * 60ps = 347.34$ fJ

Area Estimation:

H = 511 * 3um + 0.6um = 1533.6um
W_{NOR2} = 0.96um, W_{NAND2} = 0.48um, W_{NOR4} = 3.84um, W_{NOT} = 0.24um.
Priority encoder 8:3: $W_{8:3} = (W_{NOT} + W_{NOR4}) * 2 = (0.24 + 3.84) * 2 = 8.16$um
Mux 8:1: $W_{8:1} = 6*W_{NAND2} = 2.88$um
Priority encoder 64:6: $W_{64:6} = W_{8:3} * 2 + W_{8:1} = 8.16 * 2 + 2.88 = 19.2$um
Priority encoder 512:9: $W_{512:9} = W_{64:6} + W_{8:3} + W_{8:1} = 19.2 + 8.16 + 2.88 = 30.24$um
Total Area = 1533.6 * 30.24 = 46,376 um^2

APPENDIX

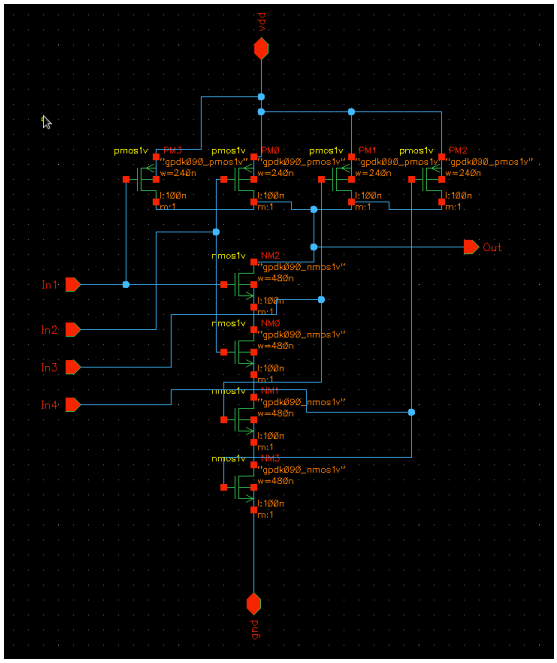


Figure A.1: NAND4 transistor level (W_P=960nm,W_N=120nm)

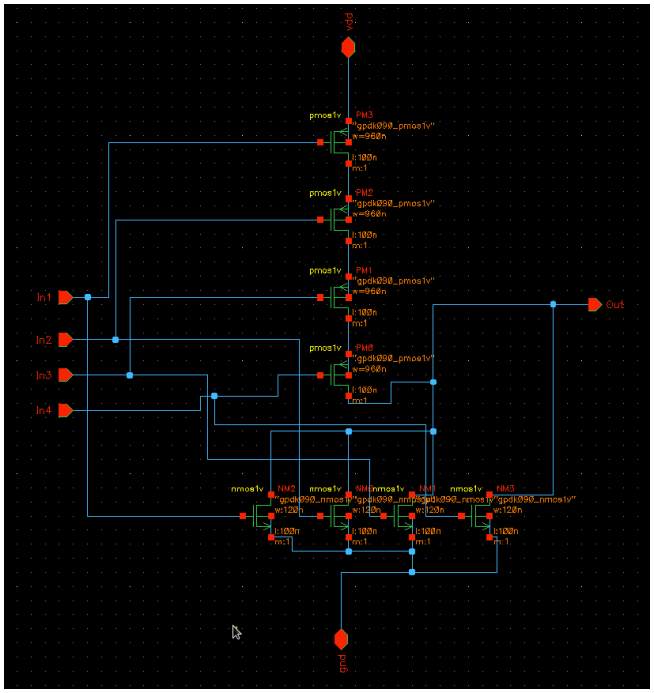


Figure A.2: NOR4 transistor level (W_P=240nm,W_N=480nm)