out_port

in_port

port_id

EXWB

A

64-Byte
Scratchpad

DI   DO

EXWB

[9:0]

+1

alu_operation

idu_operand_selection

[7:0]

[7:4]

PC

ROM

IR

YA   Y

Register
File

XA   X

WD

WA

[11:8]

IDEX

B   ci

ALU

A   co

zero

carry

EXWB

Next
Address
Logic

Data
Forward
Control

reg_source

reg_x_address

reg_y_address

reg_dst_address

conditional_match

call, return

+1
-1
0

Add

SP

Condition
match
logic

stack write enable

IDEX

Stack

+2

IFID

zero

carry

Note: Interrupt handling
logic not shown

RojoBlaze pipelined CPU
Register Block Diagram
with Data Forwarding Logic
John Lynch OGI/OHSU
23 Dec 2005