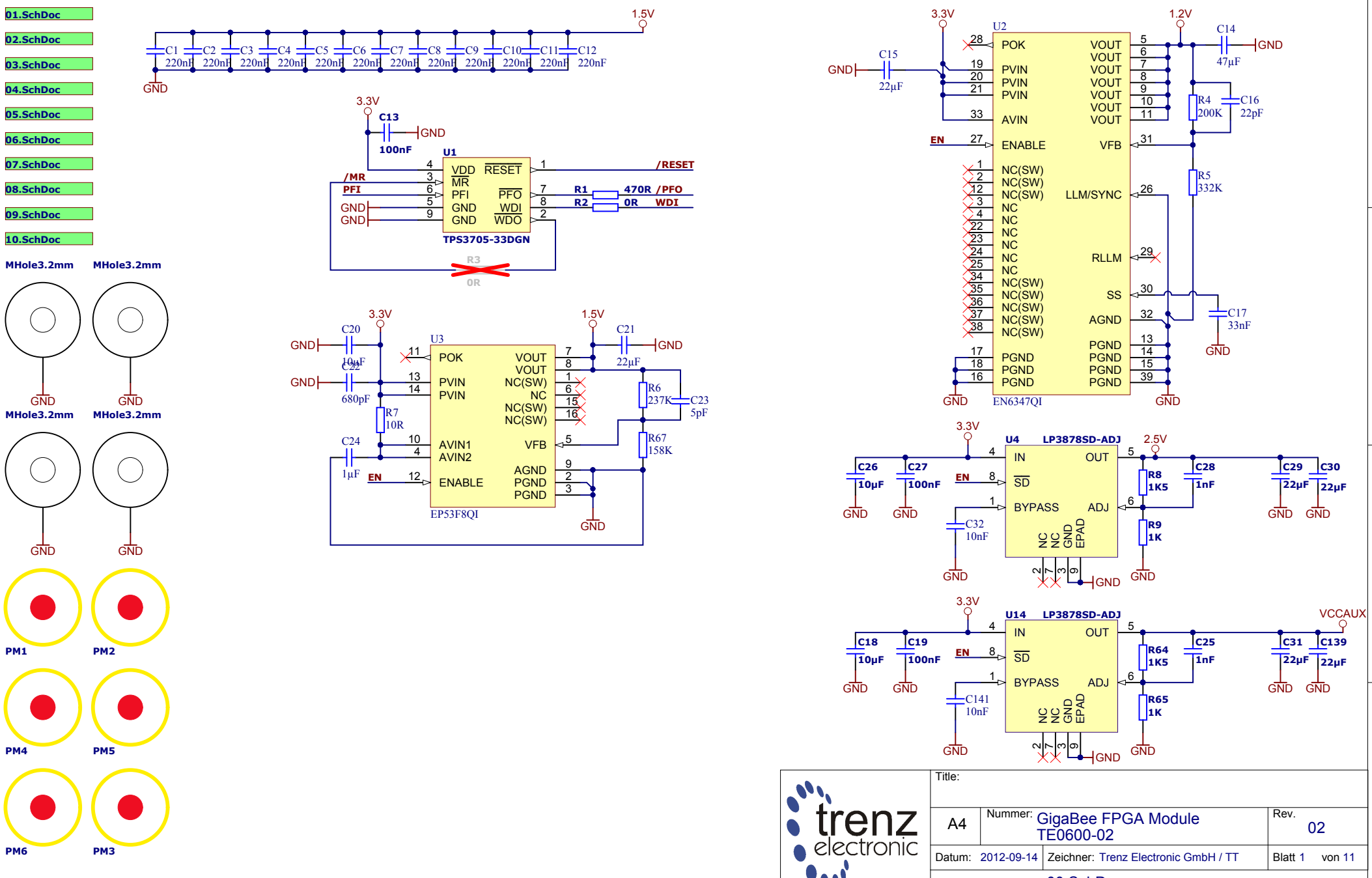
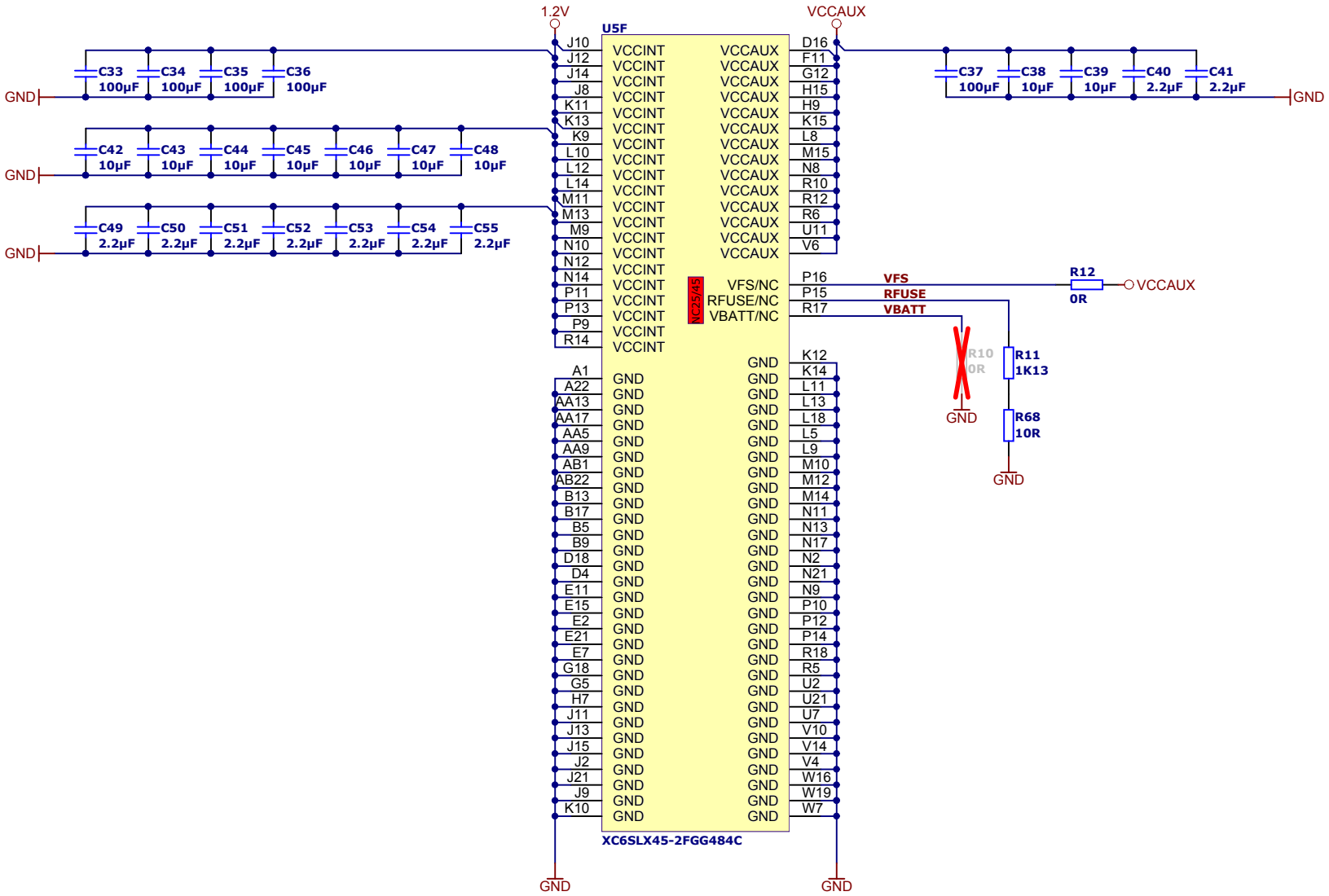
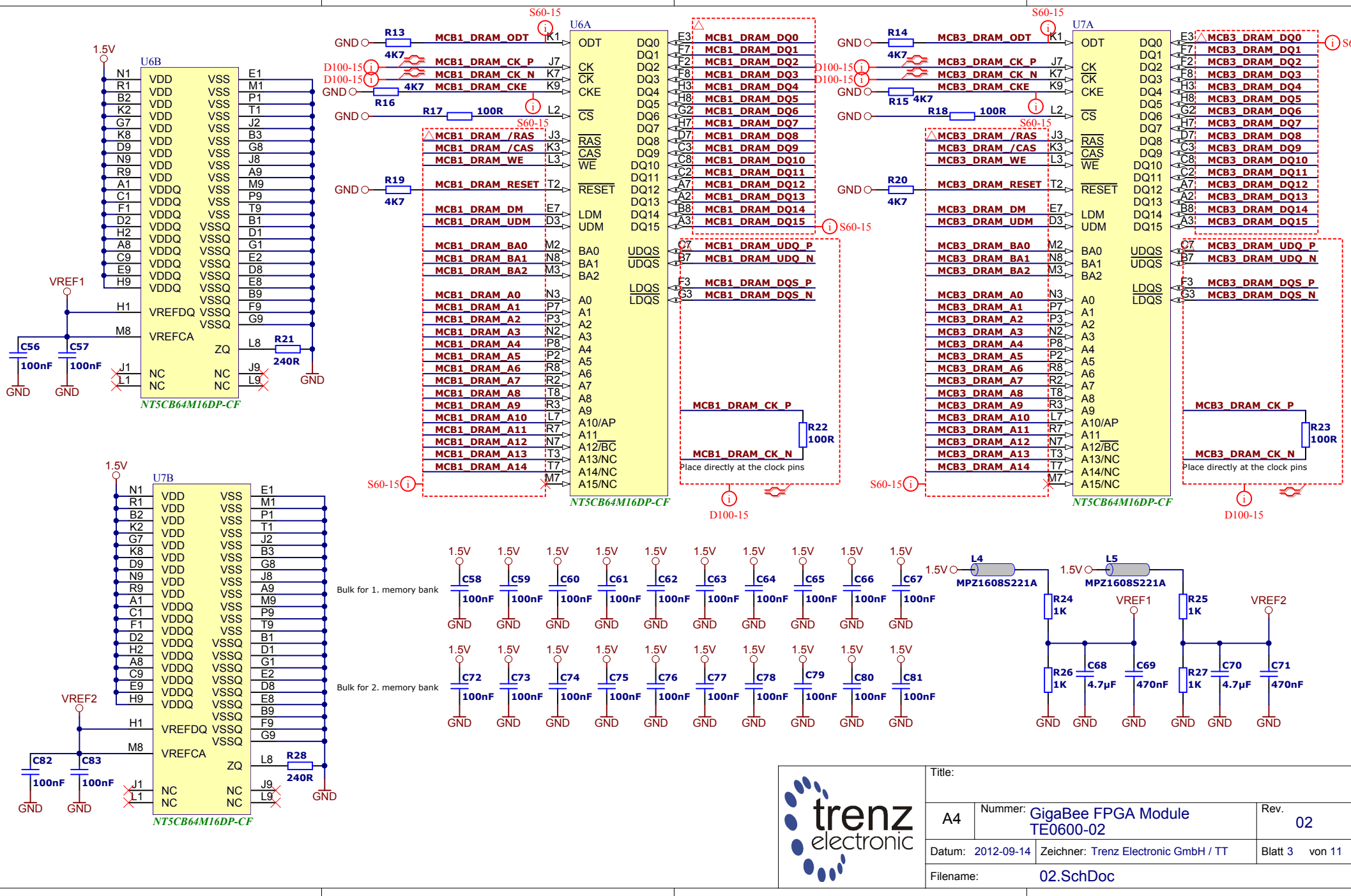

01.SchDoc
02.SchDoc
03.SchDoc
04.SchDoc
05.SchDoc
06.SchDoc
07.SchDoc
08.SchDoc
09.SchDoc
10.SchDoc
MHole3.2mm
MHole3.2mm
MHole3.2mm
MHole3.2mm
PM1
PM2
PM4
PM5
PM6
PM3
GND
1.5V
C1 220nF
C2 220nF
C3 220nF
C4 220nF
C5 220nF
C6 220nF
C7 220nF
C8 220nF
C9 220nF
C10 220nF
C11 220nF
C12 220nF
3.3V
C13
100nF
U1
TPS3705-33DGN
VDD
MR
PFI
GND
GND
RESET
PFO
WDI
WDO
/MR
PFI
/RESET
/PFO
WDI
R1 470R
R2 0R
R3 0R
U3
EP53F8QI
POK
PVIN
PVIN
AVIN1
AVIN2
ENABLE
VOUT
VOUT
NC(SW)
NC
NC(SW)
NC(SW)
VFB
AGND
PGND
PGND
C20 10µF
C22 680pF
C24 1µF
C21 22µF
R7 10R
R6 237K
C23 5pF
R67 158K
EN
U2
EN6347QI
C15 22µF
C14 47µF
R4 200K
C16 22pF
R5 332K
C17 33nF
3.3V
1.2V
POK
PVIN
PVIN
PVIN
AVIN
ENABLE
NC(SW)
NC
NC
NC
NC
NC
NC(SW)
NC(SW)
NC(SW)
NC(SW)
PGND
PGND
PGND
VOUT
LLM/SYNC
RLLM
SS
AGND
PGND
VFB
U4
LP3878SD-ADJ
C26 10µF
C27 100nF
C32 10nF
R8 1K5
R9 1K
C28 1nF
C29 22µF
C30 22µF
2.5V
IN
SD
BYPASS
OUT
ADJ
NC
NC
GND
EPAD
U14
LP3878SD-ADJ
C18 10µF
C19 100nF
C141 10nF
R64 1K5
R65 1K
C25 1nF
C31 22µF
C139 22µF
VCCAUX
trenz electronic
Title:
A4
Nummer: GigaBee FPGA Module TE0600-02
Rev. 02
Datum: 2012-09-14
Zeichner: Trenz Electronic GmbH / TT
Blatt 1 von 11
Filename: 00.SchDoc



Title:		
A4	Nummer: GigaBee FPGA Module TE0600-02	Rev. 02
Datum: 2012-09-14	Zeichner: Trenz Electronic GmbH / TT	Blatt 2 von 11
Filename: 01.SchDoc		


U6B
U6A
U7A
U7B
NT5CB64M16DP-CF
1.5V
VREF1
VREF2
GND
S60-15
D100-15
MCB1_DRAM_ODT
MCB1_DRAM_CK_P
MCB1_DRAM_CK_N
MCB1_DRAM_CKE
MCB1_DRAM_/RAS
MCB1_DRAM_/CAS
MCB1_DRAM_WE
MCB1_DRAM_RESET
MCB1_DRAM_DM
MCB1_DRAM_UDM
MCB1_DRAM_DQ0
MCB1_DRAM_DQ1
MCB1_DRAM_DQ2
MCB1_DRAM_DQ3
MCB1_DRAM_DQ4
MCB1_DRAM_DQ5
MCB1_DRAM_DQ6
MCB1_DRAM_DQ7
MCB1_DRAM_DQ8
MCB1_DRAM_DQ9
MCB1_DRAM_DQ10
MCB1_DRAM_DQ11
MCB1_DRAM_DQ12
MCB1_DRAM_DQ13
MCB1_DRAM_DQ14
MCB1_DRAM_DQ15
MCB1_DRAM_UDQ_P
MCB1_DRAM_UDQ_N
MCB1_DRAM_DQS_P
MCB1_DRAM_DQS_N
MCB1_DRAM_BA0
MCB1_DRAM_BA1
MCB1_DRAM_BA2
MCB1_DRAM_A0
MCB1_DRAM_A1
MCB1_DRAM_A2
MCB1_DRAM_A3
MCB1_DRAM_A4
MCB1_DRAM_A5
MCB1_DRAM_A6
MCB1_DRAM_A7
MCB1_DRAM_A8
MCB1_DRAM_A9
MCB1_DRAM_A10
MCB1_DRAM_A11
MCB1_DRAM_A12
MCB1_DRAM_A13
MCB1_DRAM_A14
MCB1_DRAM_CK_P
MCB1_DRAM_CK_N
Place directly at the clock pins
MCB3_DRAM_ODT
MCB3_DRAM_CK_P
MCB3_DRAM_CK_N
MCB3_DRAM_CKE
MCB3_DRAM_/RAS
MCB3_DRAM_/CAS
MCB3_DRAM_WE
MCB3_DRAM_RESET
MCB3_DRAM_DM
MCB3_DRAM_UDM
MCB3_DRAM_DQ0
MCB3_DRAM_DQ1
MCB3_DRAM_DQ2
MCB3_DRAM_DQ3
MCB3_DRAM_DQ4
MCB3_DRAM_DQ5
MCB3_DRAM_DQ6
MCB3_DRAM_DQ7
MCB3_DRAM_DQ8
MCB3_DRAM_DQ9
MCB3_DRAM_DQ10
MCB3_DRAM_DQ11
MCB3_DRAM_DQ12
MCB3_DRAM_DQ13
MCB3_DRAM_DQ14
MCB3_DRAM_DQ15
MCB3_DRAM_UDQ_P
MCB3_DRAM_UDQ_N
MCB3_DRAM_DQS_P
MCB3_DRAM_DQS_N
MCB3_DRAM_BA0
MCB3_DRAM_BA1
MCB3_DRAM_BA2
MCB3_DRAM_A0
MCB3_DRAM_A1
MCB3_DRAM_A2
MCB3_DRAM_A3
MCB3_DRAM_A4
MCB3_DRAM_A5
MCB3_DRAM_A6
MCB3_DRAM_A7
MCB3_DRAM_A8
MCB3_DRAM_A9
MCB3_DRAM_A10
MCB3_DRAM_A11
MCB3_DRAM_A12
MCB3_DRAM_A13
MCB3_DRAM_A14
Bulk for 1. memory bank
Bulk for 2. memory bank
MPZ1608S221A
Title:
A4
Nummer: GigaBee FPGA Module TE0600-02
Rev. 02
Datum: 2012-09-14
Zeichner: Trenz Electronic GmbH / TT
Blatt 3 von 11
Filename: 02.SchDoc
trenz electronic

Trace widths should be 3 to 5 mils.
Trace spacing should be three times the trace width.
Signals must not be routed over splits or voids.
Routing of differential pairs adjacent to noisy signal lines or high-speed switching
devices such as clock chips should be avoided.
The spacing between differential clocks/strobes and other signals on the same PCB
layer should be 20 mil. The 20 mil spacing should be maintained when using
serpentine routing for length matching.
Differential clocks/strobes are to be routed as 100O differential signals. The clock
pairs must be routed on the same PCB layer with no layer changes or hops after the
initial pad to via breakout.
The Data (DQ), Data Mask (DM), and Data Strobe (DQS) signals should receive the highest
priority (that is, routed first), because they are the highest speed DDR signals.
DQ, DM, and DQS signals should be routed in a data group (per byte). Each group
should have similar loading and routing to maintain timing and signal integrity.
The provided spacing should be 20 mil between a data group and any other signals.
DQS signals should be isolated from other signals by 20 mil to avoid crosstalk.
There should be a maximum of ±25 ps electrical delay (±150 mil) between any
DQ/DM and its associated DQS strobe.
A data group should be referenced to a GROUND plane.
DQ bit swapping at the memory interface is permitted to facilitate layout. Swapping
should only be done within a data group.
DQS to DQS_N trace lengths should be matched (±10 mil).
Memory terminations (if external terminations are used) should be placed after the
associated memory component in a fly-by fashion.
For 16-bit DDR devices, the LDQS/LDQS_N and UDQS/UDQS_N trace lengths
should be matched within ±25 ps of the electrical delay (±150 mil).
When the data groups have been routed, the next highest priority is the differential clock
(CK / CK_N). The clock should be routed first because all address and control trace length
matching must be referenced to the differential clock PCB trace length, which might need
to be adjusted as the layout task proceeds.
CK to CK_N trace lengths must be matched (±10 mil).
CK and DQS trace lengths must be matched (±250 mil) to maximize setup and hold margins.
There must be a maximum ±50 ps electrical delay (±300 mil) between any
address/control signals and the associated CK and CK_N differential clock FPGA output.
Address and control signals can be referenced to a POWER plane if a GROUND plane
is not next to this group of signals in the PCB stack-up.
To avoid crosstalk, address and command signals should be kept on a different
routing layer from DQ, DQS, and DM.
Differential clock terminations (if external terminations are used) must be located as
close as possible to the load, after the clock pads of the PCB. PCB trace lengths used in
trace length matching must exclude the CLINE length of the PCB trace from memory
ball to terminating resistor.

Classnames:
S60-15 uses 1.5V or GND plane as reference
D100-15 uses 1.5V or GND plane as reference

S60-25 uses 2.5V or GND plane as reference
D100-25 uses 2.5V or GND plane as reference

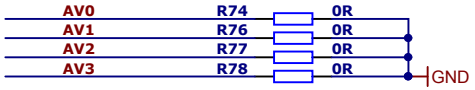
S60-IO uses VCCIO0 or GND plane as reference
D100-IO uses VCCIO0 or GND plane as reference

S60-33 uses 3.3V or GND plane as reference
D100-33 uses 3.3V or GND plane as reference

AV0 = 0 -> commercial AV0 = 1 -> Industrial

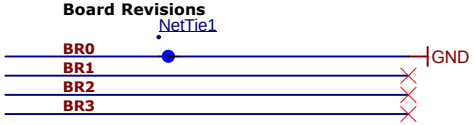
AV3	AV2	AV1	
0	0	0	2 x 128 MBit, speedgrade 2
0	0	1	2 x 128 MBit, speedgrade 3
0	1	0	2 x 512 MBit, speedgrade 3

Assembly Variants



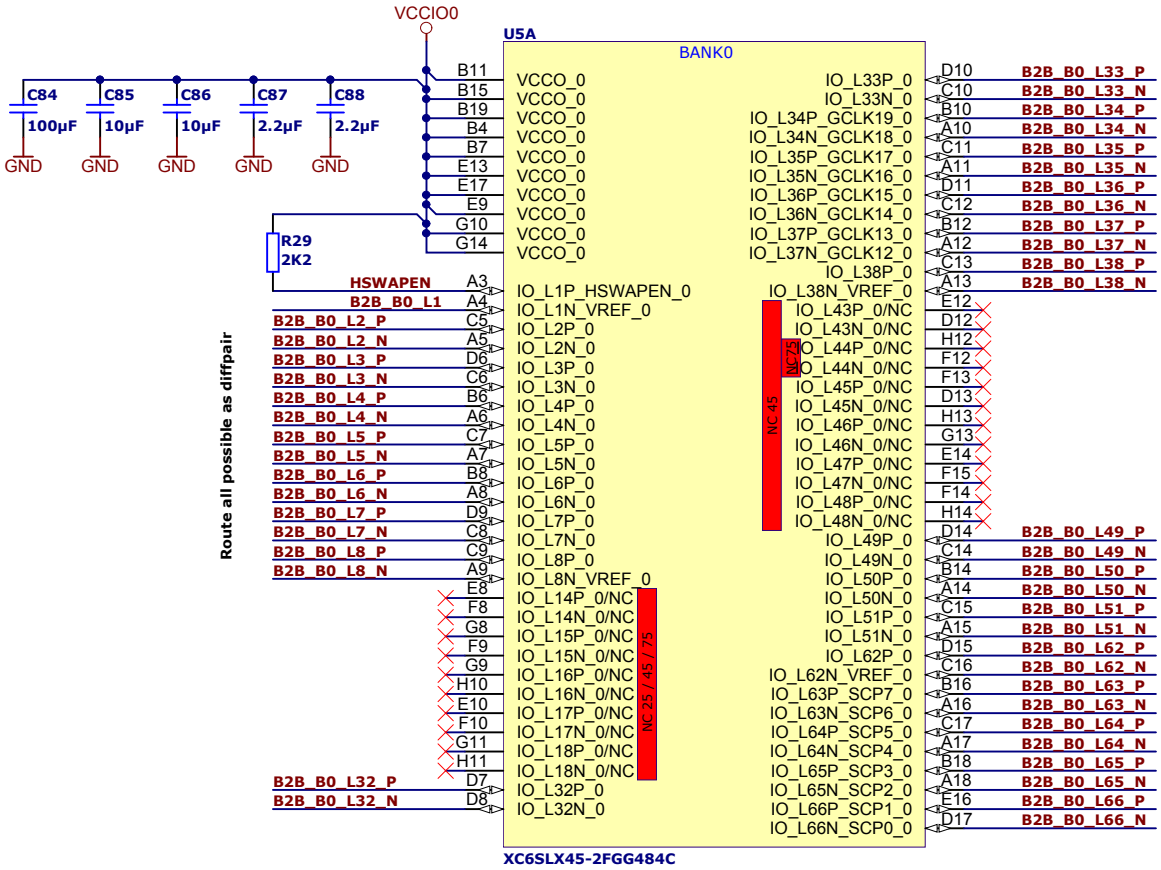
BR3	BR2	BR1	BR0	
1	1	1	1	-01 Initial revision
1	1	1	0	-02

Board Revisions

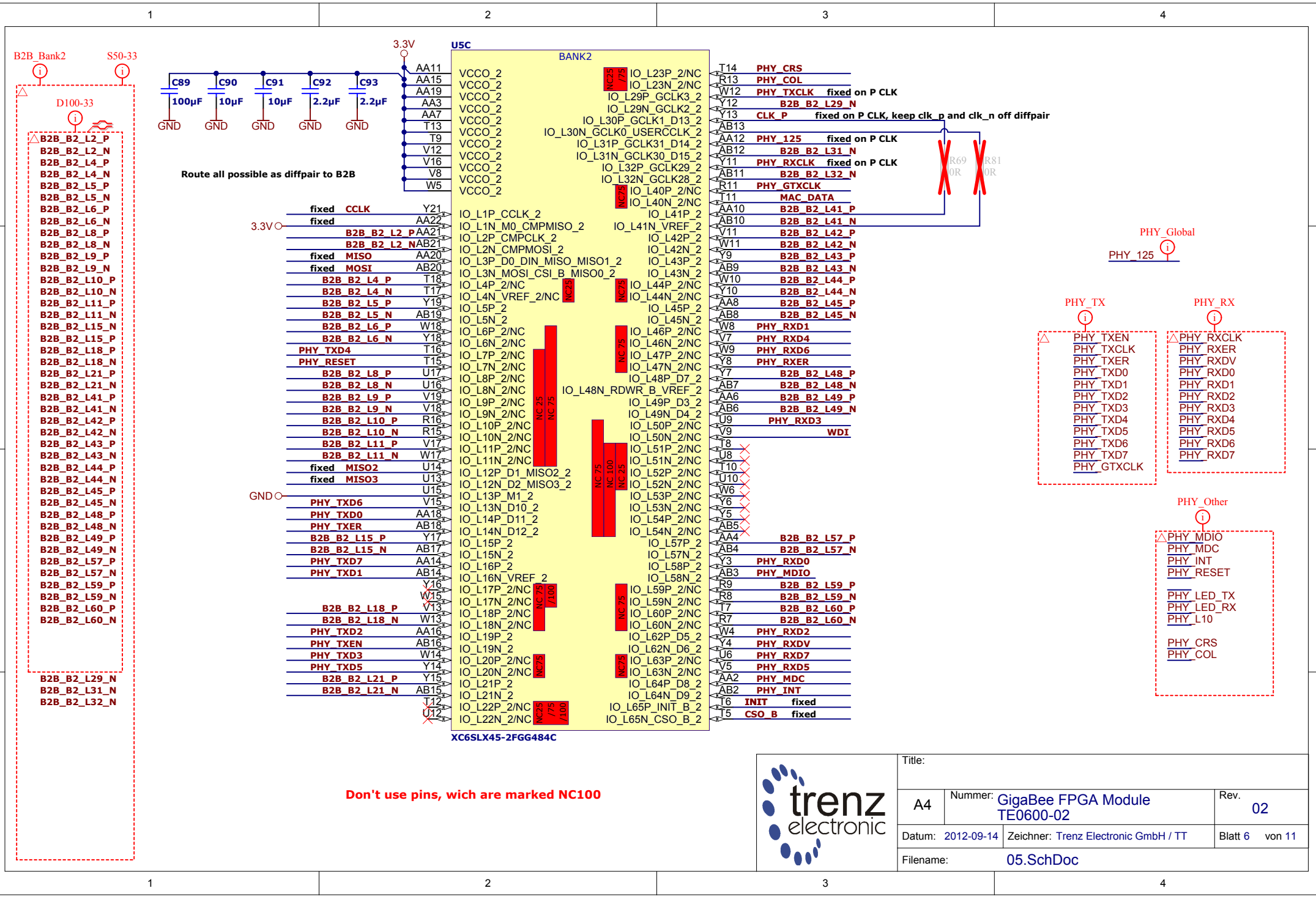


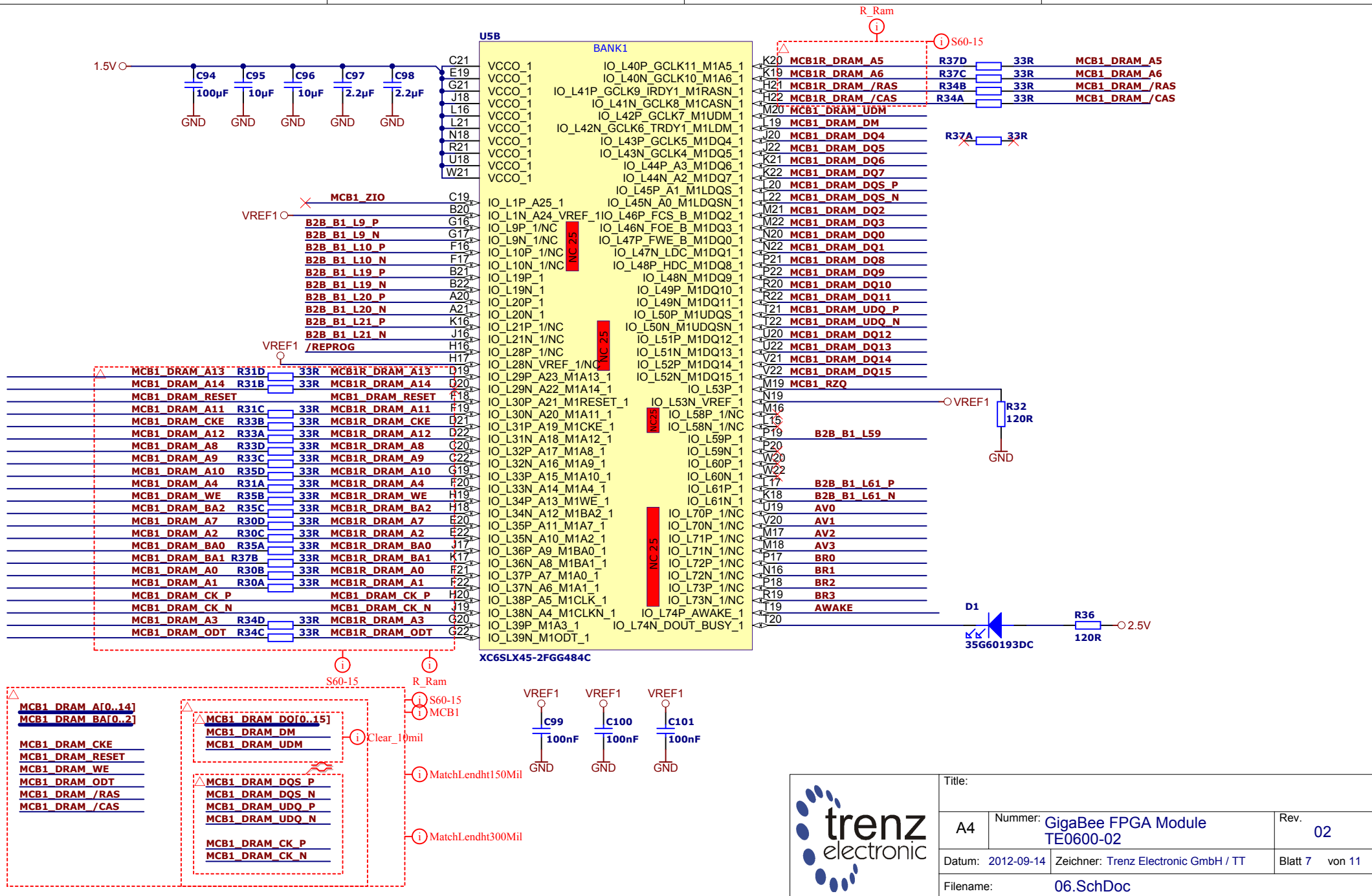
Enable pullups in FPGA

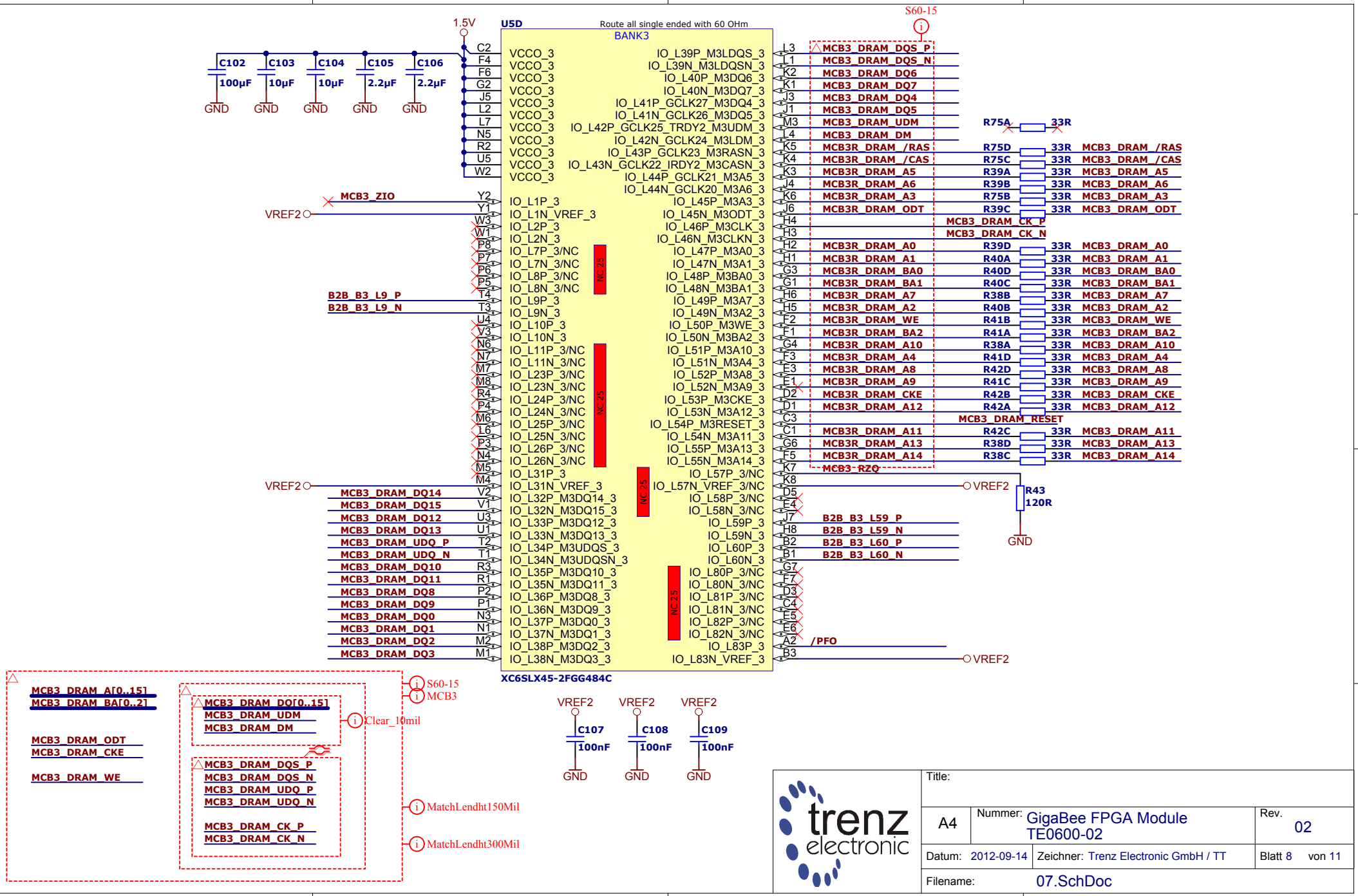
	Title:		
A4	Nummer: GigaBee FPGA Module TE0600-02		Rev. 02
	Datum: 2012-09-14	Zeichner: Trenz Electronic GmbH / TT	Blatt 4 von 11
	Filename: 03.SchDoc		

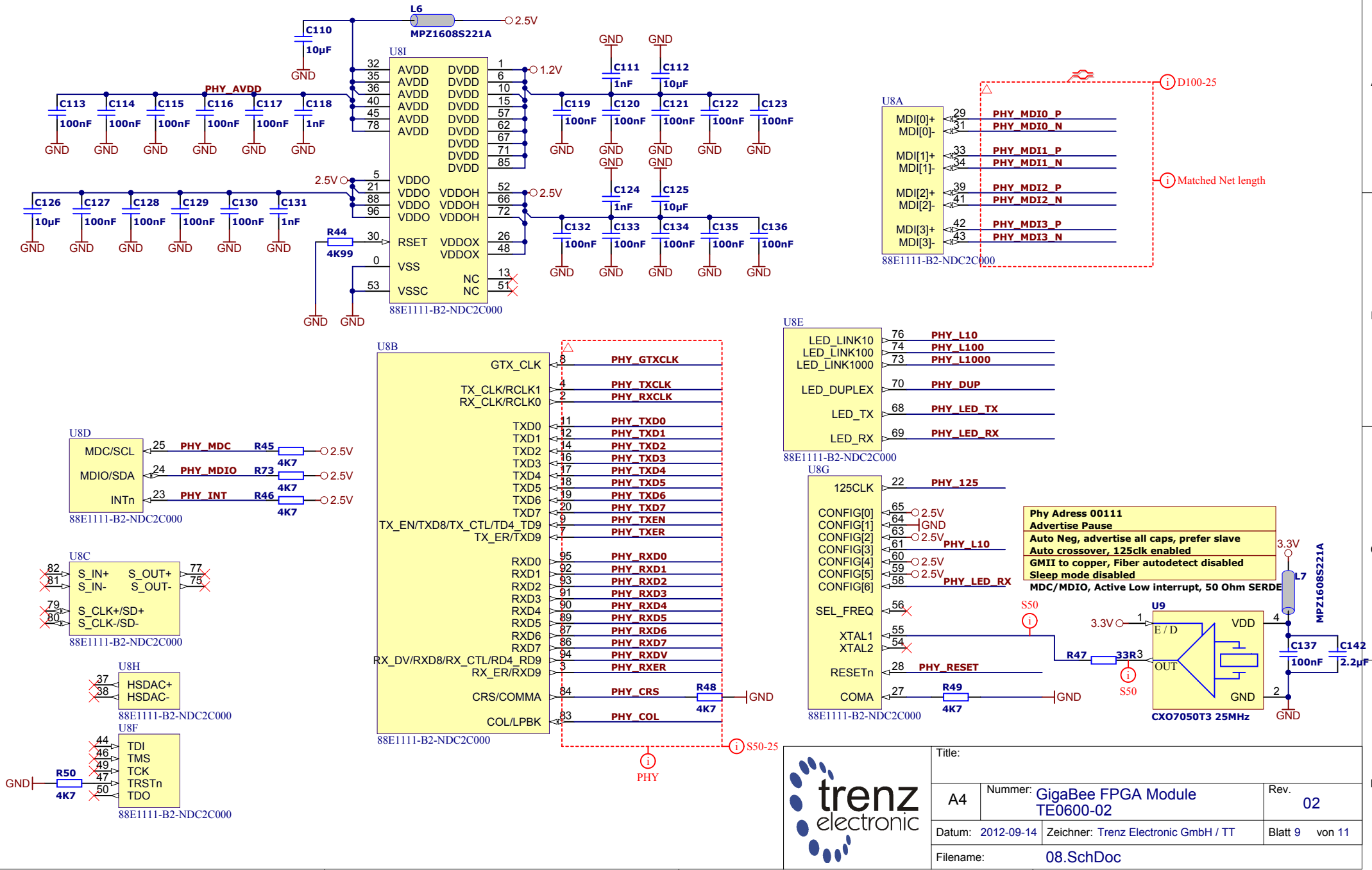


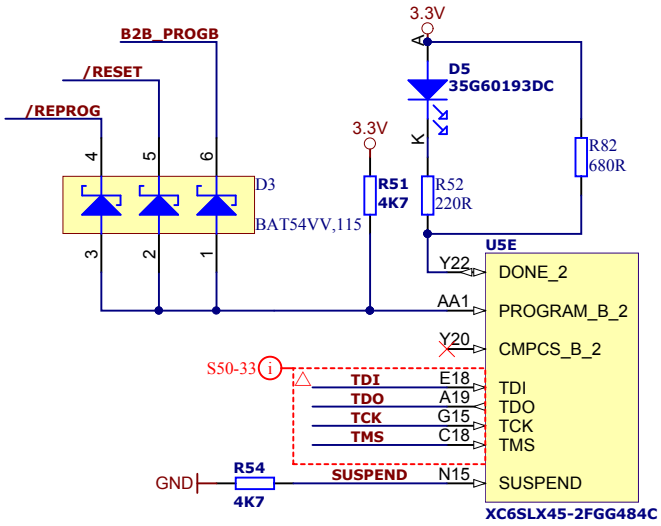
trenz electronic	Title:		
	A4	Nummer: GigaBee FPGA Module TE0600-02	Rev. 02
	Datum: 2012-09-14	Zeichner: Trenz Electronic GmbH / TT	Blatt 5 von 11
	Filename:	04.SchDoc	

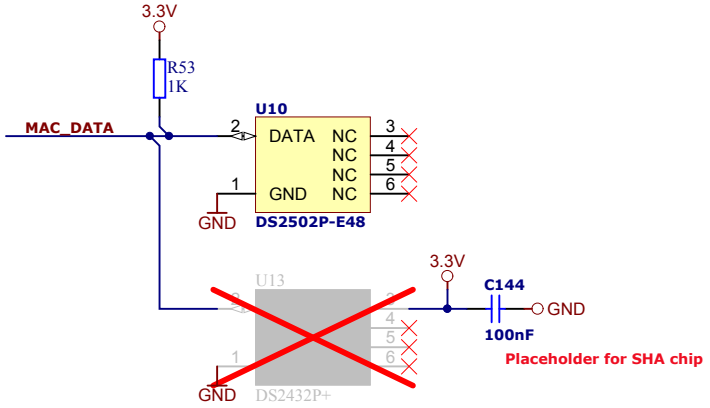

B2B_Bank2
S50-33
D100-33
B2B_B2_L2_P
B2B_B2_L2_N
B2B_B2_L4_P
B2B_B2_L4_N
B2B_B2_L5_P
B2B_B2_L5_N
B2B_B2_L6_P
B2B_B2_L6_N
B2B_B2_L8_P
B2B_B2_L8_N
B2B_B2_L9_P
B2B_B2_L9_N
B2B_B2_L10_P
B2B_B2_L10_N
B2B_B2_L11_P
B2B_B2_L11_N
B2B_B2_L15_N
B2B_B2_L15_P
B2B_B2_L18_P
B2B_B2_L18_N
B2B_B2_L21_P
B2B_B2_L21_N
B2B_B2_L41_P
B2B_B2_L41_N
B2B_B2_L42_P
B2B_B2_L42_N
B2B_B2_L43_P
B2B_B2_L43_N
B2B_B2_L44_P
B2B_B2_L44_N
B2B_B2_L45_P
B2B_B2_L45_N
B2B_B2_L48_P
B2B_B2_L48_N
B2B_B2_L49_P
B2B_B2_L49_N
B2B_B2_L57_P
B2B_B2_L57_N
B2B_B2_L59_P
B2B_B2_L59_N
B2B_B2_L60_P
B2B_B2_L60_N
B2B_B2_L29_N
B2B_B2_L31_N
B2B_B2_L32_N
3.3V
C89 100µF
C90 10µF
C91 10µF
C92 2.2µF
C93 2.2µF
GND
Route all possible as diffpair to B2B
U5C
BANK2
XC6SLX45-2FGG484C
PHY_CRS
PHY_COL
PHY_TXCLK fixed on P CLK
B2B_B2_L29_N
CLK_P fixed on P CLK, keep clk_p and clk_n off diffpair
PHY_125 fixed on P CLK
B2B_B2_L31_N
PHY_RXCLK fixed on P CLK
B2B_B2_L32_N
PHY_GTXCLK
MAC_DATA
B2B_B2_L41_P
B2B_B2_L41_N
B2B_B2_L42_P
B2B_B2_L42_N
B2B_B2_L43_P
B2B_B2_L43_N
B2B_B2_L44_P
B2B_B2_L44_N
B2B_B2_L45_P
B2B_B2_L45_N
PHY_RXD1
PHY_RXD4
PHY_RXD6
PHY_RXER
B2B_B2_L48_P
B2B_B2_L48_N
B2B_B2_L49_P
B2B_B2_L49_N
PHY_RXD3
WDI
B2B_B2_L57_P
B2B_B2_L57_N
PHY_RXD0
PHY_MDIO
B2B_B2_L59_P
B2B_B2_L59_N
B2B_B2_L60_P
B2B_B2_L60_N
PHY_RXD2
PHY_RXDV
PHY_RXD7
PHY_RXD5
PHY_MDC
PHY_INT
INIT fixed
CSO_B fixed
fixed CCLK
fixed MISO
fixed MOSI
PHY_TXD4
PHY_RESET
PHY_TXD6
PHY_TXD0
PHY_TXER
PHY_TXD7
PHY_TXD1
PHY_TXD2
PHY_TXEN
PHY_TXD3
PHY_TXD5
fixed MISO2
fixed MISO3
R69 0R
R81 0R
PHY_Global
PHY_125
PHY_TX
PHY_TXEN
PHY_TXCLK
PHY_TXER
PHY_TXD0
PHY_TXD1
PHY_TXD2
PHY_TXD3
PHY_TXD4
PHY_TXD5
PHY_TXD6
PHY_TXD7
PHY_GTXCLK
PHY_RX
PHY_RXCLK
PHY_RXER
PHY_RXDV
PHY_RXD0
PHY_RXD1
PHY_RXD2
PHY_RXD3
PHY_RXD4
PHY_RXD5
PHY_RXD6
PHY_RXD7
PHY_Other
PHY_MDIO
PHY_MDC
PHY_INT
PHY_RESET
PHY_LED_TX
PHY_LED_RX
PHY_L10
PHY_CRS
PHY_COL
Don't use pins, wich are marked NC100
trenz electronic
Title:
A4
Nummer: GigaBee FPGA Module TE0600-02
Rev. 02
Datum: 2012-09-14
Zeichner: Trenz Electronic GmbH / TT
Blatt 6 von 11
Filename: 05.SchDoc

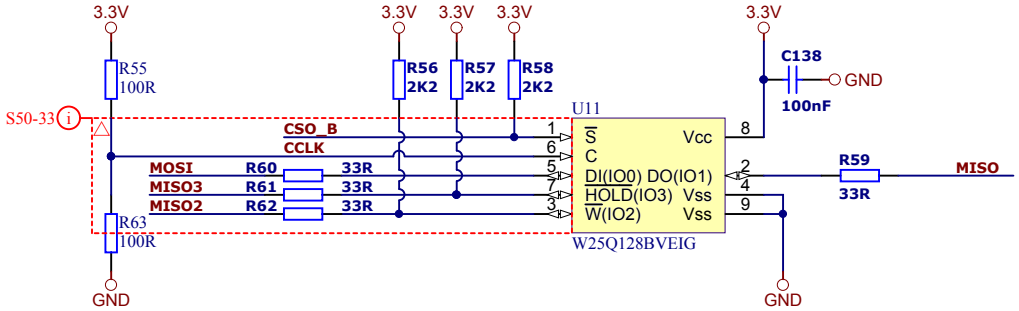

U5B
BANK1
XC6SLX45-2FGG484C
1.5V
C94 100µF
C95 10µF
C96 10µF
C97 2.2µF
C98 2.2µF
GND
VREF1
/REPROG
MCB1_ZIO
R_Ram
S60-15
R37D 33R MCB1_DRAM_A5
R37C 33R MCB1_DRAM_A6
R34B 33R MCB1_DRAM_/RAS
R34A 33R MCB1_DRAM_/CAS
R37A 33R
R32 120R
B2B_B1_L59
B2B_B1_L61_P
B2B_B1_L61_N
AV0
AV1
AV2
AV3
BR0
BR1
BR2
BR3
AWAKE
D1
35G60193DC
R36 120R
2.5V
MCB1_DRAM_A13 R31D 33R MCB1R_DRAM_A13
MCB1_DRAM_A14 R31B 33R MCB1R_DRAM_A14
MCB1_DRAM_RESET
MCB1_DRAM_A11 R31C 33R MCB1R_DRAM_A11
MCB1_DRAM_CKE R33B 33R MCB1R_DRAM_CKE
MCB1_DRAM_A12 R33A 33R MCB1R_DRAM_A12
MCB1_DRAM_A8 R33D 33R MCB1R_DRAM_A8
MCB1_DRAM_A9 R33C 33R MCB1R_DRAM_A9
MCB1_DRAM_A10 R35D 33R MCB1R_DRAM_A10
MCB1_DRAM_A4 R31A 33R MCB1R_DRAM_A4
MCB1_DRAM_WE R35B 33R MCB1R_DRAM_WE
MCB1_DRAM_BA2 R35C 33R MCB1R_DRAM_BA2
MCB1_DRAM_A7 R30D 33R MCB1R_DRAM_A7
MCB1_DRAM_A2 R30C 33R MCB1R_DRAM_A2
MCB1_DRAM_BA0 R35A 33R MCB1R_DRAM_BA0
MCB1_DRAM_BA1 R37B 33R MCB1R_DRAM_BA1
MCB1_DRAM_A0 R30B 33R MCB1R_DRAM_A0
MCB1_DRAM_A1 R30A 33R MCB1R_DRAM_A1
MCB1_DRAM_CK_P
MCB1_DRAM_CK_N
MCB1_DRAM_A3 R34D 33R MCB1R_DRAM_A3
MCB1_DRAM_ODT R34C 33R MCB1R_DRAM_ODT
MCB1_DRAM_A[0..14]
MCB1_DRAM_BA[0..2]
MCB1_DRAM_CKE
MCB1_DRAM_RESET
MCB1_DRAM_WE
MCB1_DRAM_ODT
MCB1_DRAM_/RAS
MCB1_DRAM_/CAS
MCB1_DRAM_DQ[0..15]
MCB1_DRAM_DM
MCB1_DRAM_UDM
Clear_10mil
MCB1_DRAM_DQS_P
MCB1_DRAM_DQS_N
MCB1_DRAM_UDQ_P
MCB1_DRAM_UDQ_N
MCB1_DRAM_CK_P
MCB1_DRAM_CK_N
MatchLendht150Mil
MatchLendht300Mil
MCB1
C99 100nF
C100 100nF
C101 100nF
Title:
A4
Nummer: GigaBee FPGA Module TE0600-02
Rev. 02
Datum: 2012-09-14
Zeichner: Trenz Electronic GmbH / TT
Blatt 7 von 11
Filename: 06.SchDoc
trenz electronic


U5D
BANK3
Route all single ended with 60 OHm
XC6SLX45-2FGG484C
1.5V
C102 100µF
C103 10µF
C104 10µF
C105 2.2µF
C106 2.2µF
C107 100nF
C108 100nF
C109 100nF
GND
VREF2
MCB3_ZIO
B2B_B3_L9_P
B2B_B3_L9_N
S60-15
MCB3
Clear_10mil
MatchLendht150Mil
MatchLendht300Mil
MCB3_DRAM_A[0..15]
MCB3_DRAM_BA[0..2]
MCB3_DRAM_ODT
MCB3_DRAM_CKE
MCB3_DRAM_WE
MCB3_DRAM_DQ[0..15]
MCB3_DRAM_UDM
MCB3_DRAM_DM
MCB3_DRAM_DQS_P
MCB3_DRAM_DQS_N
MCB3_DRAM_UDQ_P
MCB3_DRAM_UDQ_N
MCB3_DRAM_CK_P
MCB3_DRAM_CK_N
MCB3_DRAM_RESET
MCB3_RZQ
/PFO
R43 120R
R75A 33R
R75D 33R MCB3_DRAM_/RAS
R75C 33R MCB3_DRAM_/CAS
R39A 33R MCB3_DRAM_A5
R39B 33R MCB3_DRAM_A6
R75B 33R MCB3_DRAM_A3
R39C 33R MCB3_DRAM_ODT
R39D 33R MCB3_DRAM_A0
R40A 33R MCB3_DRAM_A1
R40D 33R MCB3_DRAM_BA0
R40C 33R MCB3_DRAM_BA1
R38B 33R MCB3_DRAM_A7
R40B 33R MCB3_DRAM_A2
R41B 33R MCB3_DRAM_WE
R41A 33R MCB3_DRAM_BA2
R38A 33R MCB3_DRAM_A10
R41D 33R MCB3_DRAM_A4
R42D 33R MCB3_DRAM_A8
R41C 33R MCB3_DRAM_A9
R42B 33R MCB3_DRAM_CKE
R42A 33R MCB3_DRAM_A12
R42C 33R MCB3_DRAM_A11
R38D 33R MCB3_DRAM_A13
R38C 33R MCB3_DRAM_A14
NC 25
Title:
A4
Nummer: GigaBee FPGA Module TE0600-02
Rev. 02
Datum: 2012-09-14
Zeichner: Trenz Electronic GmbH / TT
Blatt 8 von 11
Filename: 07.SchDoc
trenz electronic

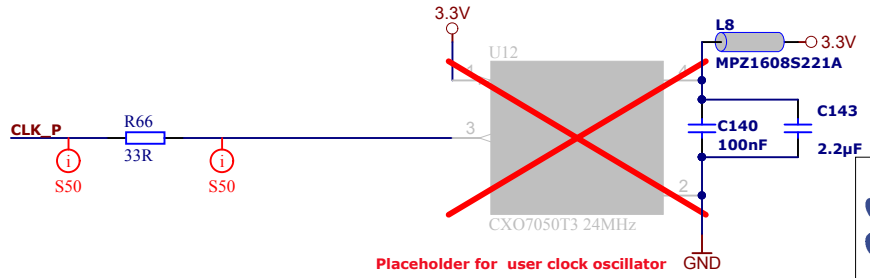

L6
MPZ1608S221A
2.5V
C110
10µF
U8I
PHY_AVDD
C113 C114 C115 C116 C117 C118
100nF 100nF 100nF 100nF 100nF 1nF
AVDD
DVDD
1.2V
C111 C112
1nF 10µF
C119 C120 C121 C122 C123
100nF 100nF 100nF 100nF 100nF
C124 C125
1nF 10µF
C126 C127 C128 C129 C130 C131
10µF 100nF 100nF 100nF 100nF 1nF
VDDO
VDDOH
RSET
VDDOX
VSS
NC
VSSC
R44
4K99
C132 C133 C134 C135 C136
100nF 100nF 100nF 100nF 100nF
88E1111-B2-NDC2C000
U8A
MDI[0]+
MDI[0]-
MDI[1]+
MDI[1]-
MDI[2]+
MDI[2]-
MDI[3]+
MDI[3]-
PHY_MDI0_P
PHY_MDI0_N
PHY_MDI1_P
PHY_MDI1_N
PHY_MDI2_P
PHY_MDI2_N
PHY_MDI3_P
PHY_MDI3_N
D100-25
Matched Net length
U8B
GTX_CLK
TX_CLK/RCLK1
RX_CLK/RCLK0
TXD0
TXD1
TXD2
TXD3
TXD4
TXD5
TXD6
TXD7
TX_EN/TXD8/TX_CTL/TD4_TD9
TX_ER/TXD9
RXD0
RXD1
RXD2
RXD3
RXD4
RXD5
RXD6
RXD7
RX_DV/RXD8/RX_CTL/RD4_RD9
RX_ER/RXD9
CRS/COMMA
COL/LPBK
PHY_GTXCLK
PHY_TXCLK
PHY_RXCLK
PHY_TXD0
PHY_TXD1
PHY_TXD2
PHY_TXD3
PHY_TXD4
PHY_TXD5
PHY_TXD6
PHY_TXD7
PHY_TXEN
PHY_TXER
PHY_RXD0
PHY_RXD1
PHY_RXD2
PHY_RXD3
PHY_RXD4
PHY_RXD5
PHY_RXD6
PHY_RXD7
PHY_RXDV
PHY_RXER
PHY_CRS
PHY_COL
R48
4K7
S50-25
PHY
U8E
LED_LINK10
LED_LINK100
LED_LINK1000
LED_DUPLEX
LED_TX
LED_RX
PHY_L10
PHY_L100
PHY_L1000
PHY_DUP
PHY_LED_TX
PHY_LED_RX
U8G
125CLK
CONFIG[0]
CONFIG[1]
CONFIG[2]
CONFIG[3]
CONFIG[4]
CONFIG[5]
CONFIG[6]
SEL_FREQ
XTAL1
XTAL2
RESETn
COMA
PHY_125
PHY_RESET
R49
4K7
R47
33R3
S50
Phy Adress 00111
Advertise Pause
Auto Neg, advertise all caps, prefer slave
Auto crossover, 125clk enabled
GMII to copper, Fiber autodetect disabled
Sleep mode disabled
MDC/MDIO, Active Low interrupt, 50 Ohm SERDE
U9
3.3V
E / D
VDD
OUT
GND
CXO7050T3 25MHz
L7
MPZ1608S221A
C137
100nF
C142
2.2µF
U8D
MDC/SCL
MDIO/SDA
INTn
PHY_MDC
PHY_MDIO
PHY_INT
R45
R73
R46
4K7
U8C
S_IN+
S_IN-
S_OUT+
S_OUT-
S_CLK+/SD+
S_CLK-/SD-
U8H
HSDAC+
HSDAC-
U8F
TDI
TMS
TCK
TRSTn
TDO
R50
4K7
GND
88E1111-B2-NDC2C000
trenz electronic
Title:
A4
Nummer: GigaBee FPGA Module TE0600-02
Rev. 02
Datum: 2012-09-14
Zeichner: Trenz Electronic GmbH / TT
Blatt 9 von 11
Filename: 08.SchDoc



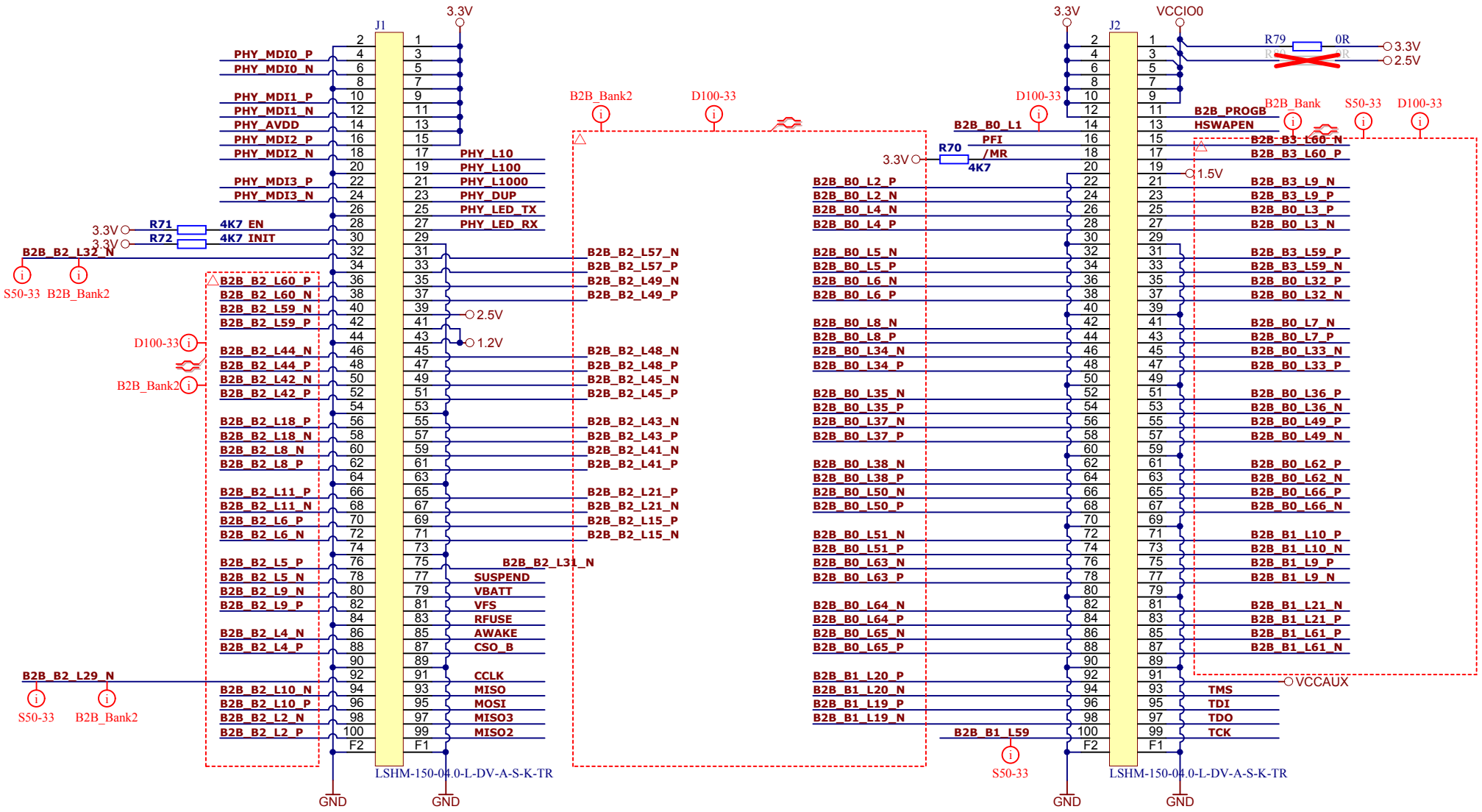




Put cclk termination close to the input pin



Title:		
A4	Nummer: GigaBee FPGA Module TE0600-02	Rev. 02
Datum: 2012-09-14	Zeichner: Trenz Electronic GmbH / TT	Blatt 10 von 11
Filename:	09.SchDoc	



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A4	Nummer: GigaBee FPGA Module TE0600-02		Rev. 02
Datum: 2012-09-14	Zeichner: Trenz Electronic GmbH / TT		Blatt 11 von 11
Filename: 10.SchDoc			