

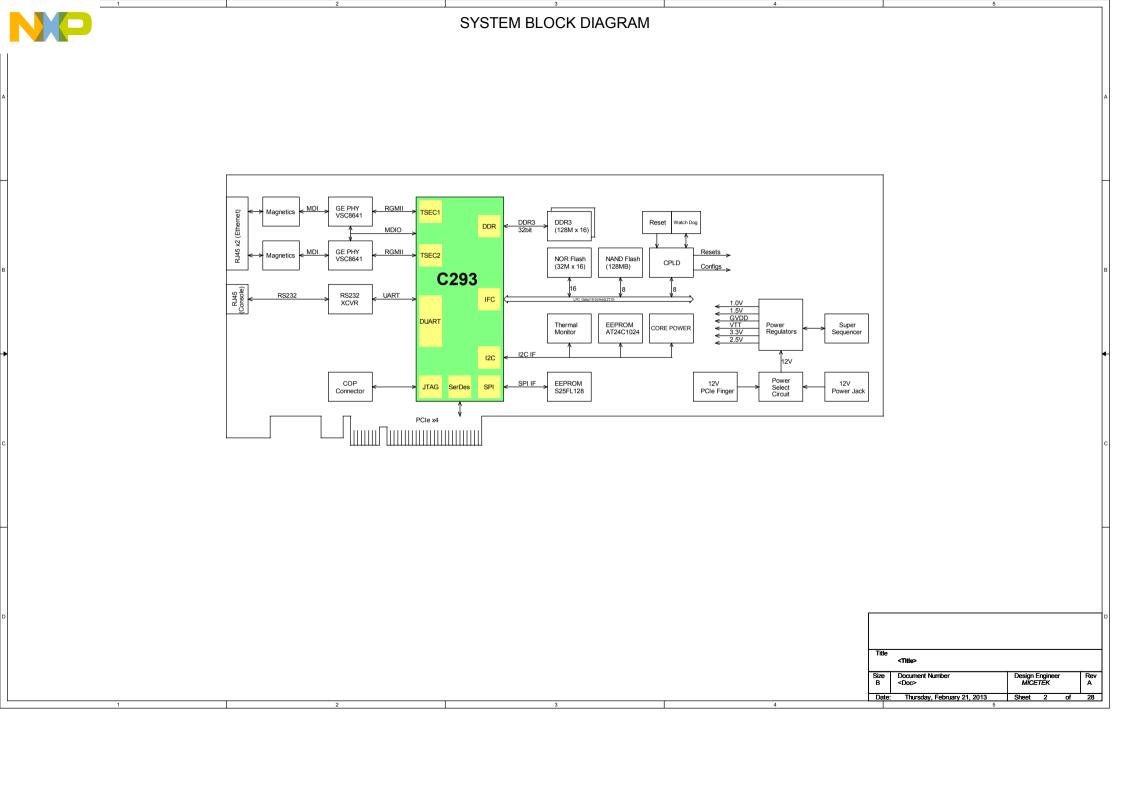
## C290PCle-RDB

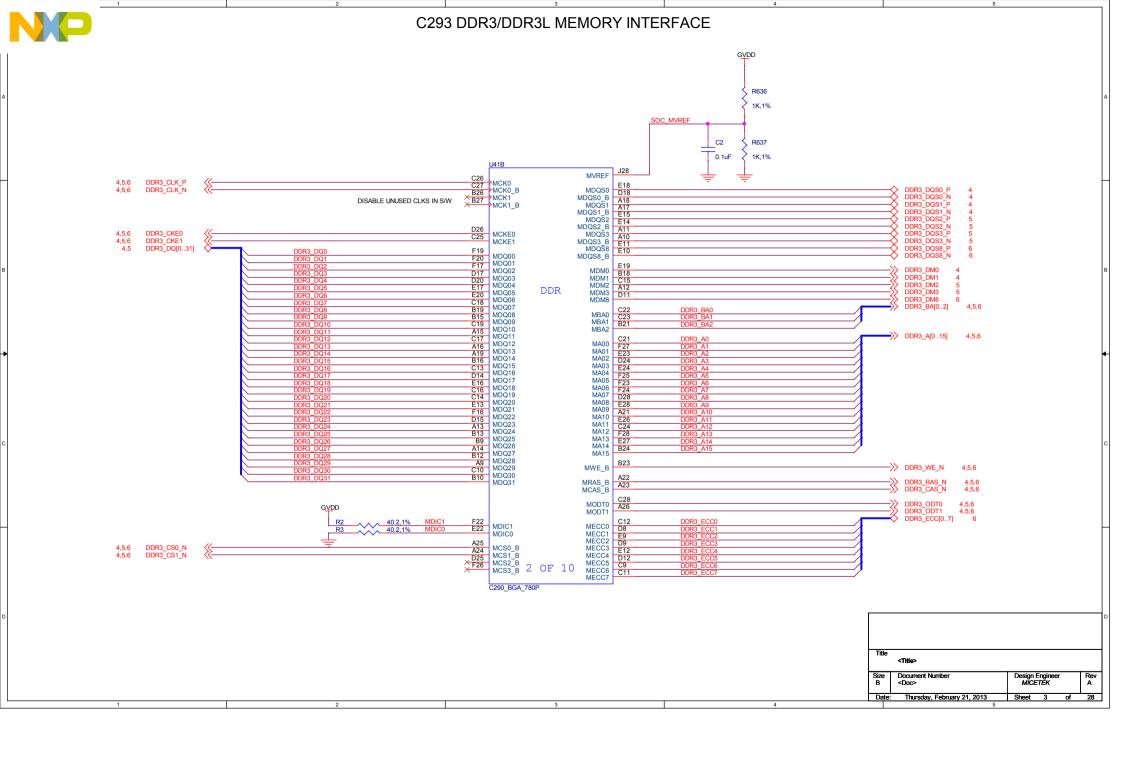
Page	e Description
1	SCHEMATIC PAGE LISTING
2	SYSTEM BLOCK DIAGRAM
3	C293 DDR3/DDR3L MEMORY INTERFACE
4	DDR3/DDR3L MEMORY CHIP 1
5	DDR3/DDR3L MEMORY CHIP 2
6	DDR3/DDR3L MEMORY ECC CHIP
7	C293 IFC INTERFACE
8	NOR FLASH and NAND FLASH MEMORY
9	C293 SERDES and TSEC 1&2 INTERFACE
10	PCI EXPRESS X4 INTERFACE
11	10/100/1000 ETHERNET PHY (PORT 1)
12	10/100/1000 ETHERNET MAGNETICS and RJ45 CONNECTOR (PORT 1)
13	10/100/1000 ETHERNET PHY (PORT 2)
14	10/100/1000 ETHERNET MAGNETICS and RJ45 CONNECTOR (PORT 2)
15	C293 MISC
16	DUART INTERFACE
17	I2C&SPI DEVICE, RESET and WATCHDOG
18	C293 POWER-ON STRAPPINGs
19	C293 POWER SUPPLY
20	C293 POWER SUPPLY (cont.)
21	C293 GROUND
22	CPLD
23	SYSTEM CLOCK GENERATORS
24	C293 CORE POWER CONVERTOR
25	SYSTEM POWER CONVERTORs
26	SYSTEM POWER INPUT
27	SYSTEM POWER ON SEQUENCING
28	MECHANICALs

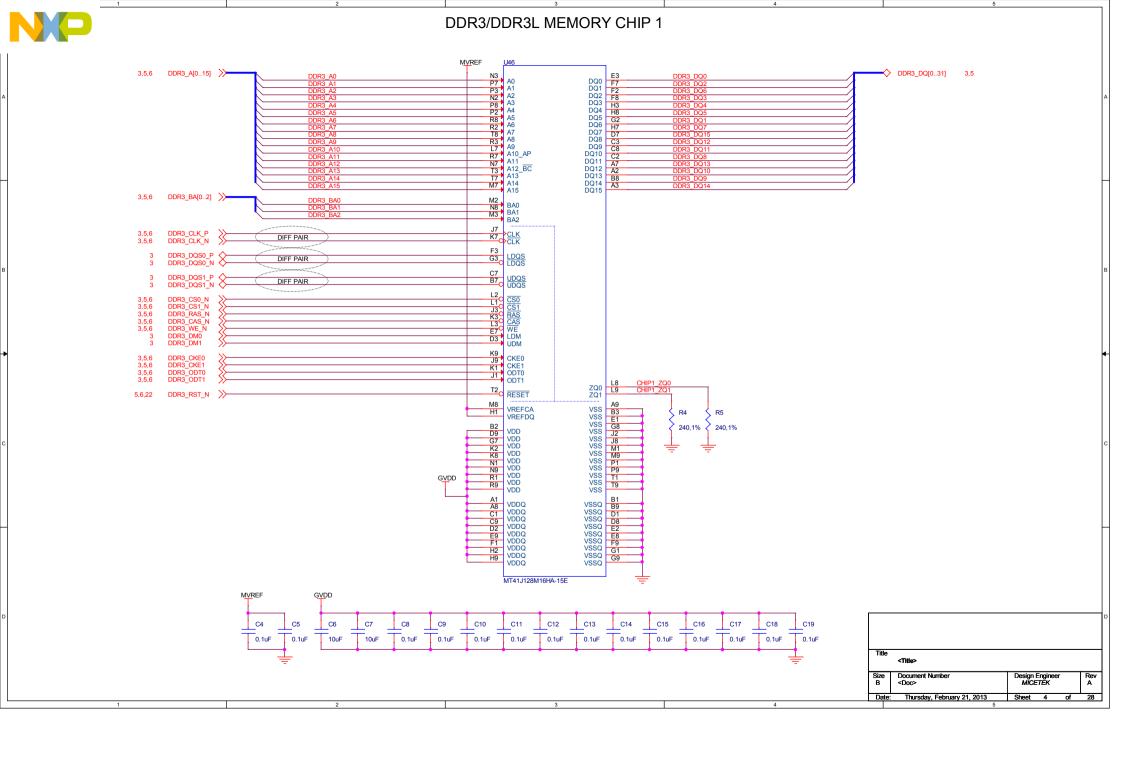
Version Control							
Version	Date	Modifications					
V0.1	2012/09	First release of Schematics					
V0.2	2012/10	update C293 symbol, change GE phy to VSC8641, add I2C boot EEPROM					
V0.3	2012/10	update POR strappings					
V0.4	2012/10	Change DDR3 to 3 x16 chips.     Add FBANK_SEL2 to NOR Flash, change NOR Flash MPN to S29GL512P11TFI0.     Add pull-up resistor to PIN10 of NAND Flash.     Add pull-up resistor to TSEC1_GTX_CLK for cfg_60x in P1010 interposer.     Correct net name errors of "GE2_CMODEx".     Remove UART1 signals and RJ45 connector.     Change POR-ON strappings with connect to switchs and CPLD.     Connect MGN signal to CPLD and switch to change VCORE voltage.     Change heatsink to S06QZZ0B.	Page 4-6 Page 8 Page 8 Page 8 Page 13 Page 15/16 Page 18/22 Page 24 Page 28				
V0.5	2012/11	Swap DDR3 data bus order for layout.     Change switch pull-up pull-down resistors to same side.     Add sw_cfg_rom_loc[0:3] from switch to CPLD.	Page 4/5/6 Page 18 Page 18/22				
V0.6	2012/11	Swap CPLD pins for layout.     Reduce power decoupling caps of C293.	Page 22 Page 20				
V0.7	2012/11	Generate SOC MVREF use voltage divider.     Delete 4.7pF cap on DDR3 clock pair.     Delete optional pull down resistor for TMP_DETECT_B.	Page 3 Page 3 Page 15				
V0.8	2012/11	Add a 0603 cap to 1V0_CB.     Add several caps acrossing plane splits.	Page 20 Page 28				
V0.9	2012/12	Add a 1000pF cap between ZL_VSEN_P and ZL_VSEN_N.     Change U34 to SOT23-5 footprint and connect NC pin to GND.	Page 24 Page 25				
V1.0	2013/02	update BOM					
V1.1	2013/02	1. Change NAND Flash R/B to CPLD, then CPLD to C293 R/B0 and R/B1.     2. Add a 0.01uF cap to PEX_RST_N.     3. Change panel LED to single color.	Page 7/8/22 Page 10 Page 22				
V2.0	2013/08	Add 6pin ATX 6pin power connector, remove PTC and common mode chock	Page 25				
V2.1	2013/10	Add notes for serdes power and nand flash stuff R248, R275, R299,					

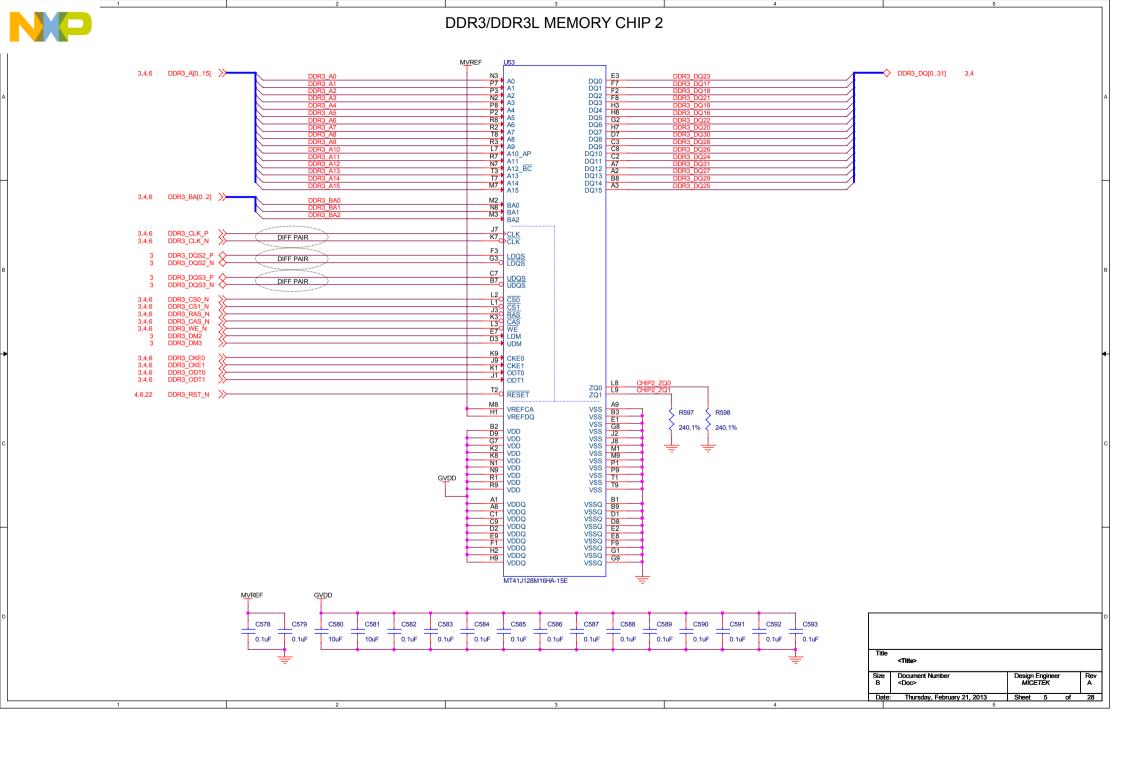
All information is subject to change without notice. No warranty, expressed or applied, is made as to the accuracy of the information contained herein. This schematic is provided for reference purposes only. Contact your Freescale representative to obtain the latest information on this product.

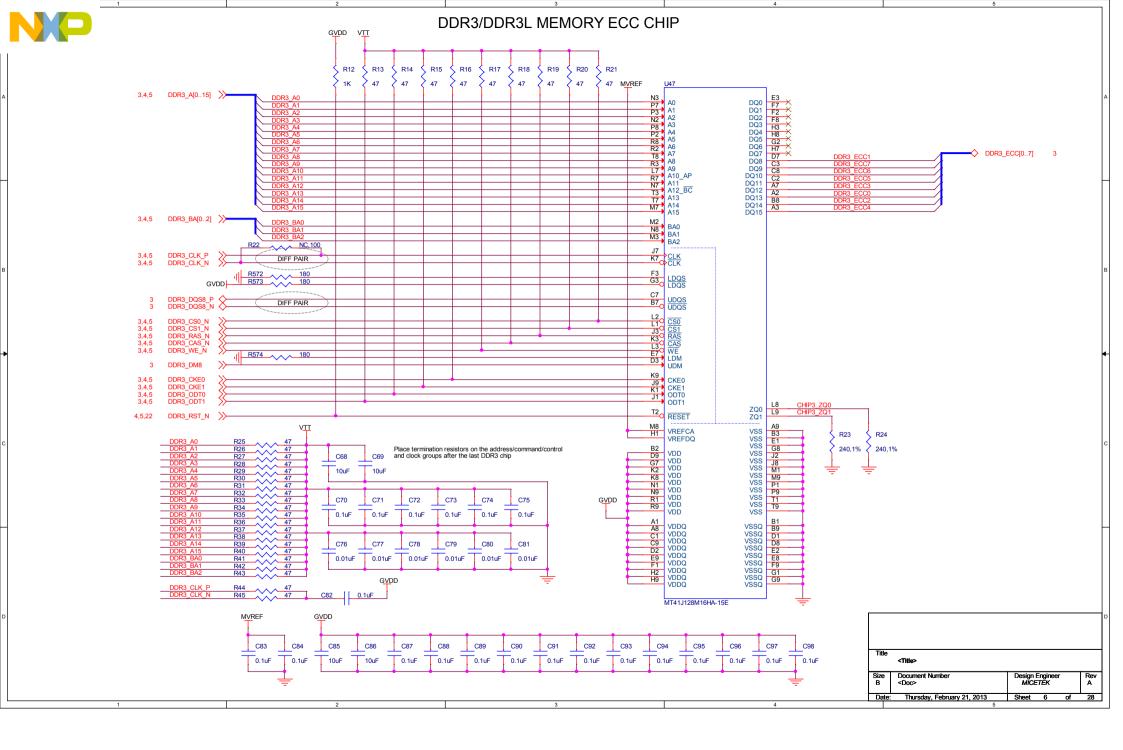
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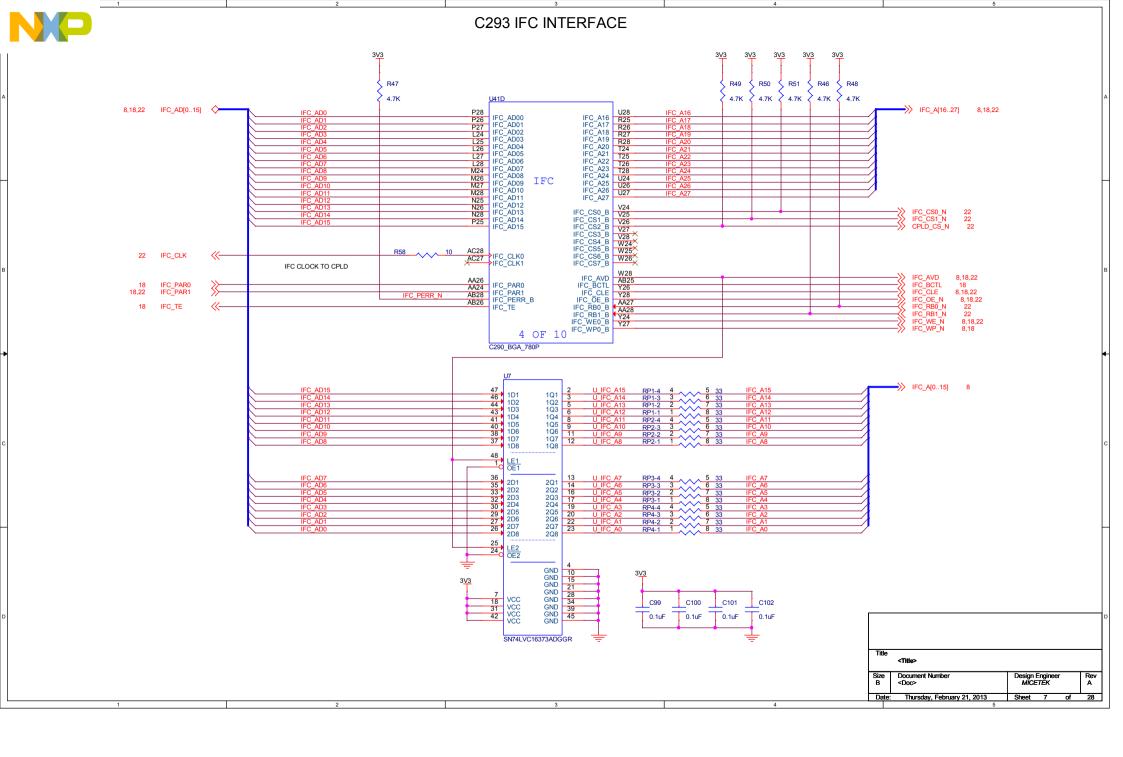


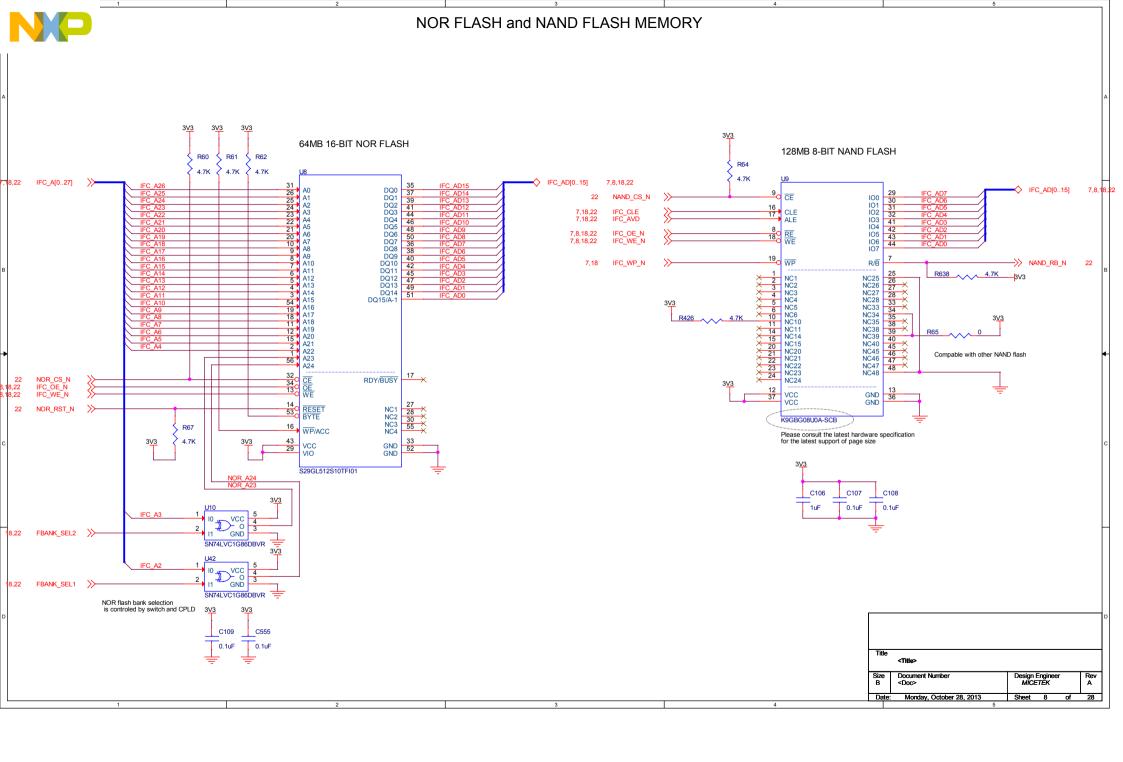


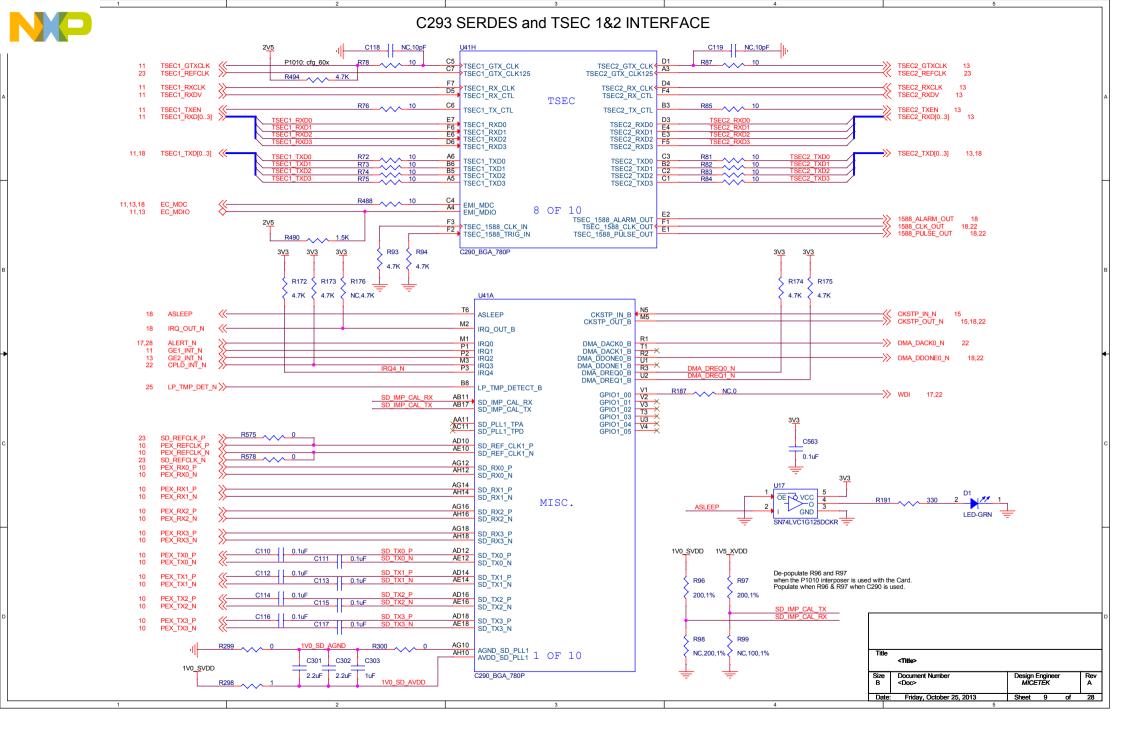


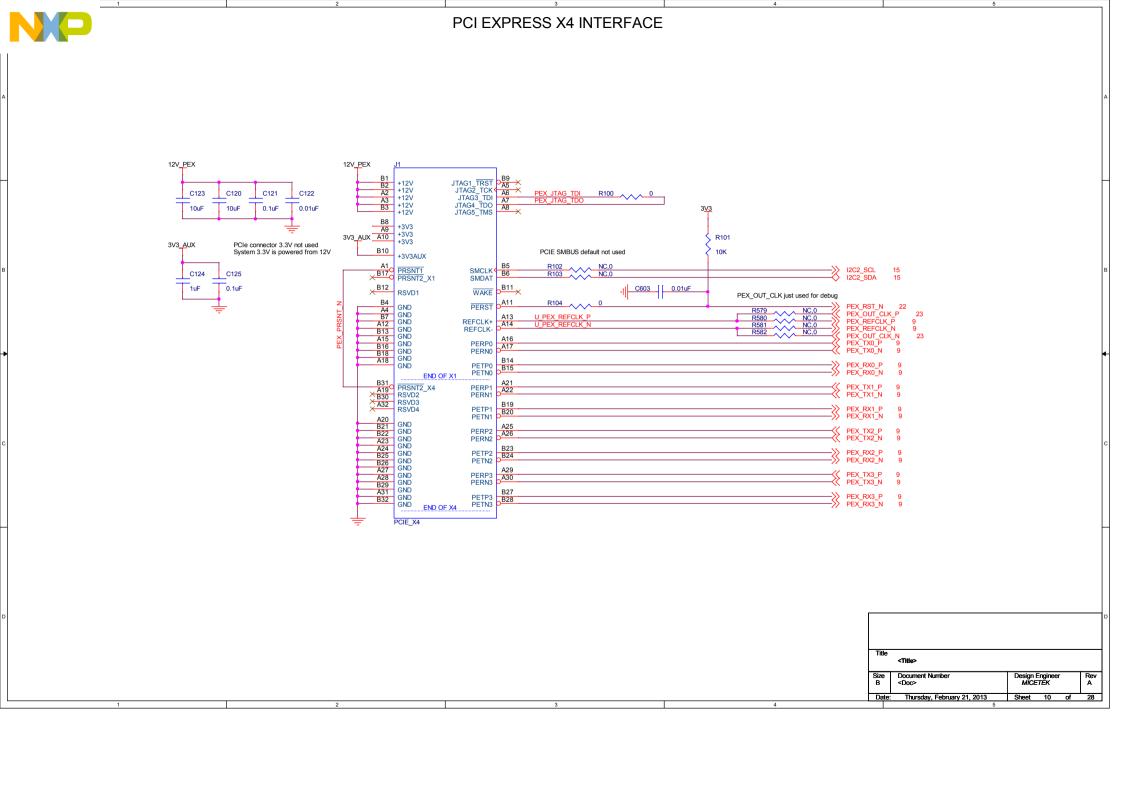


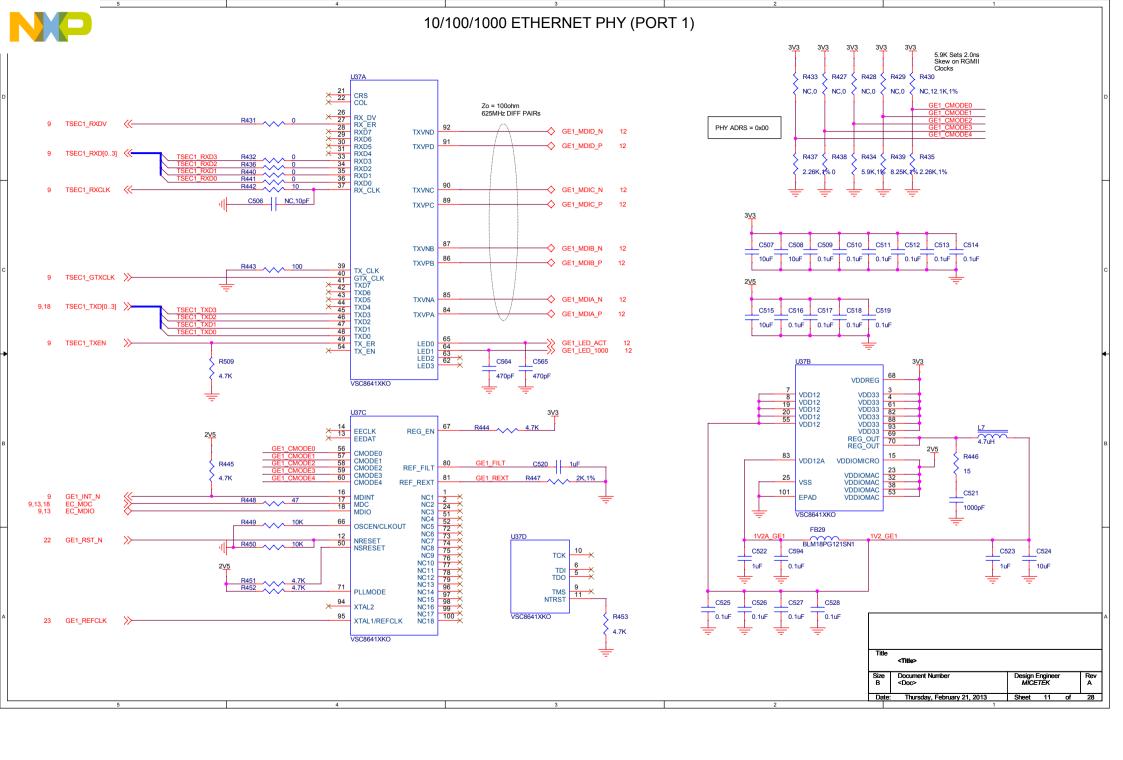


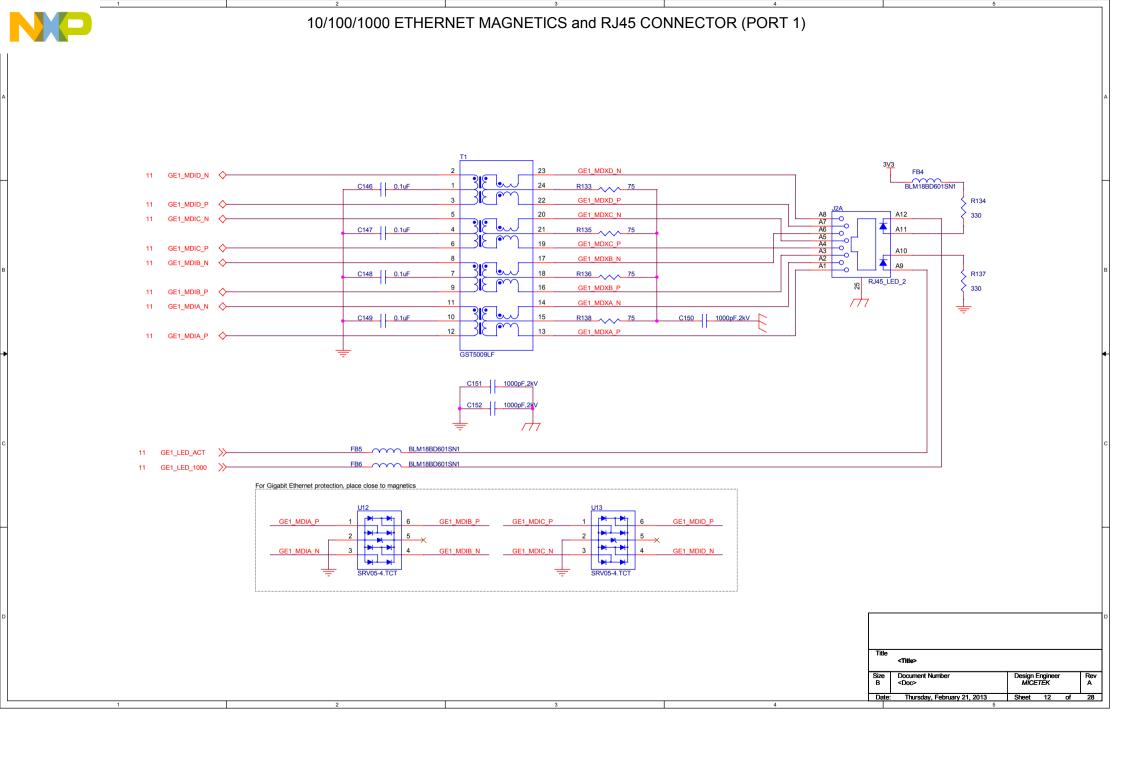


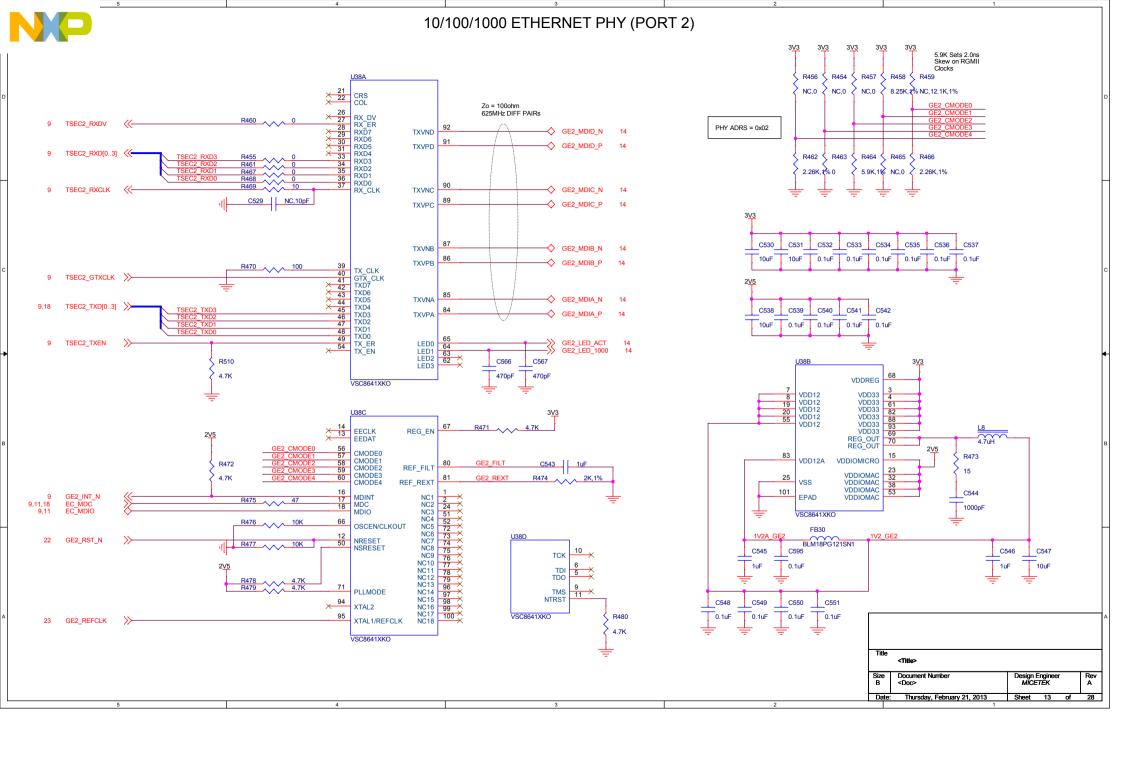


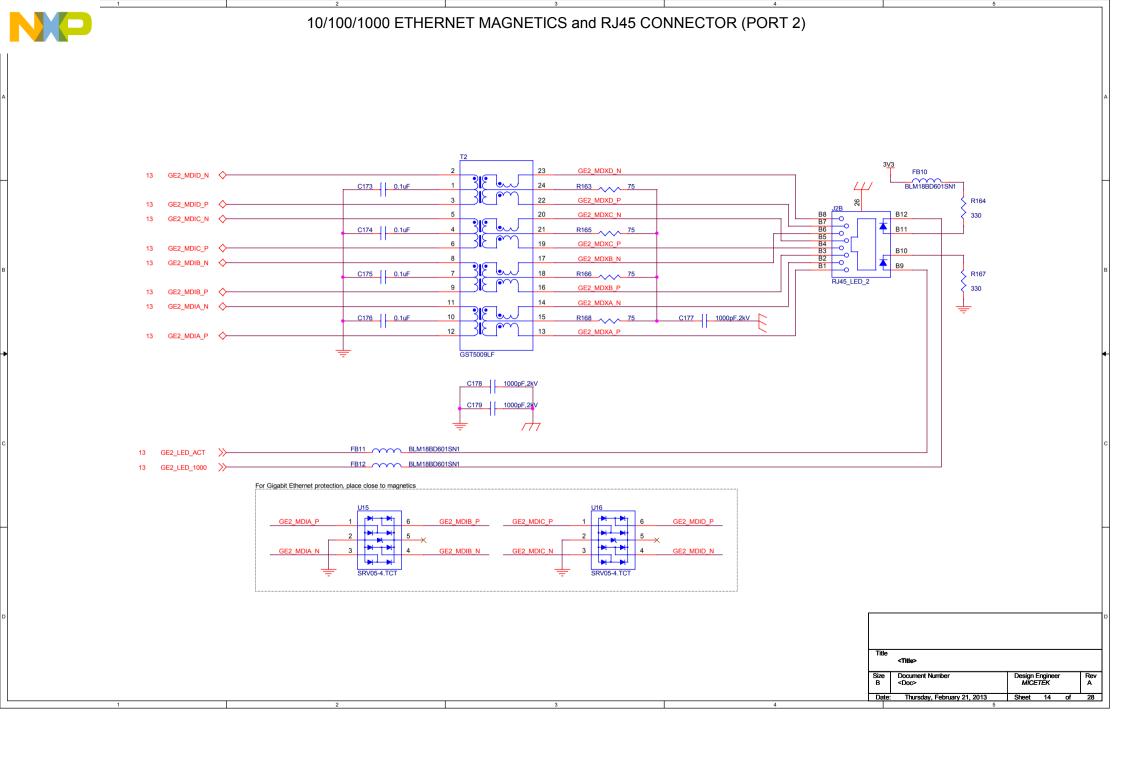


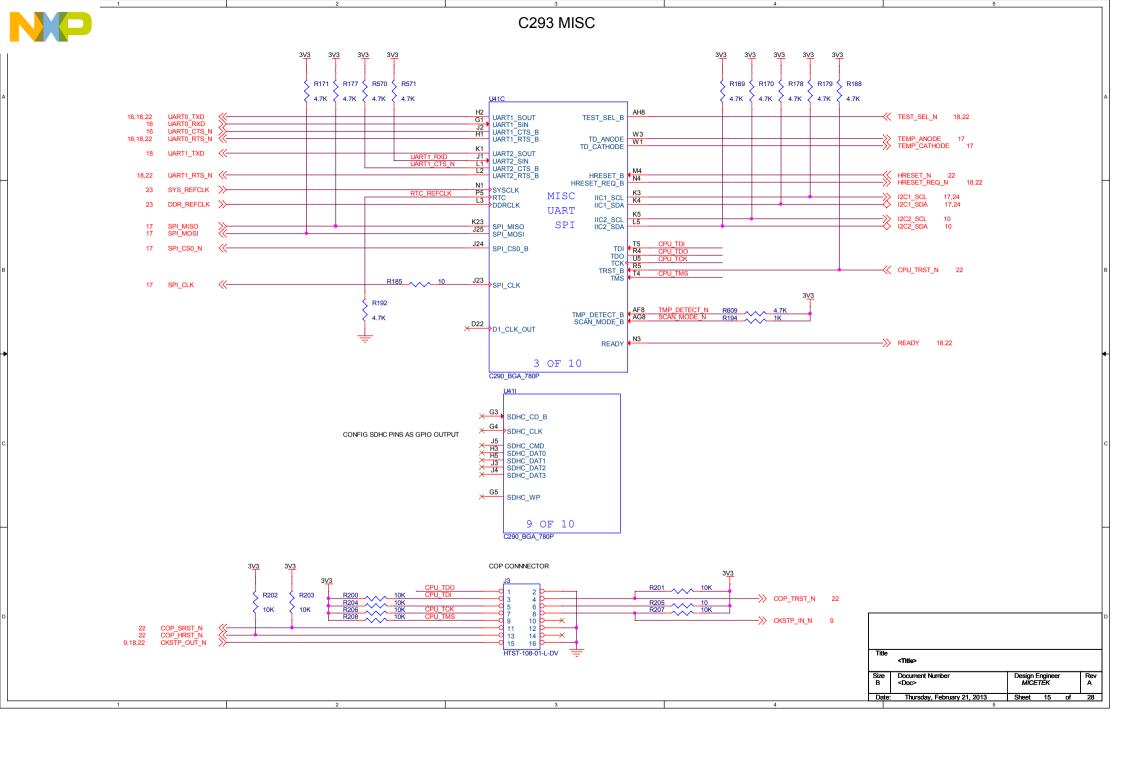


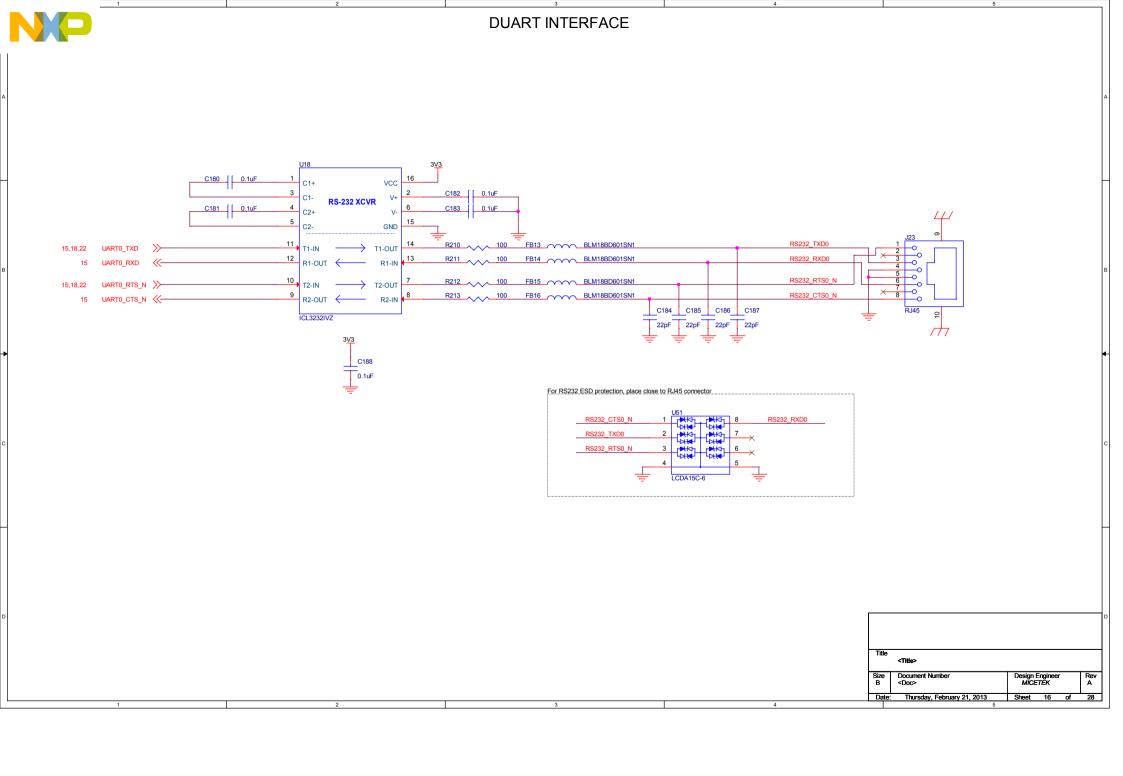


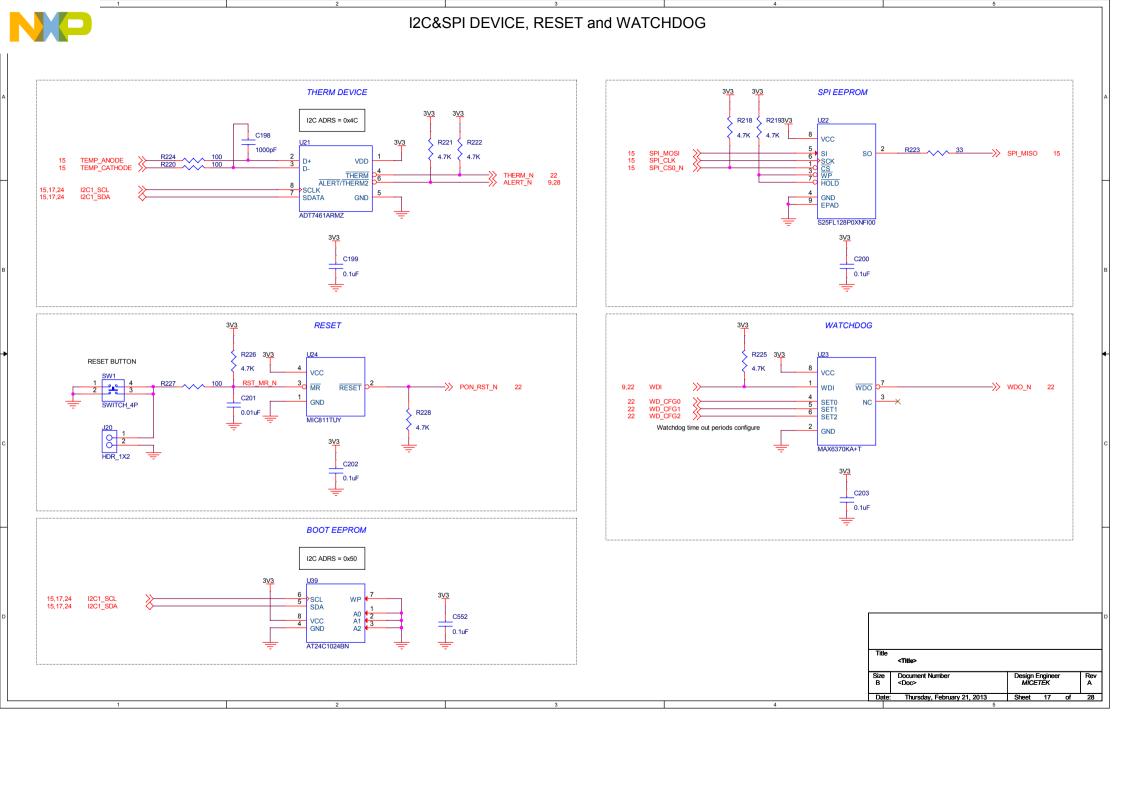


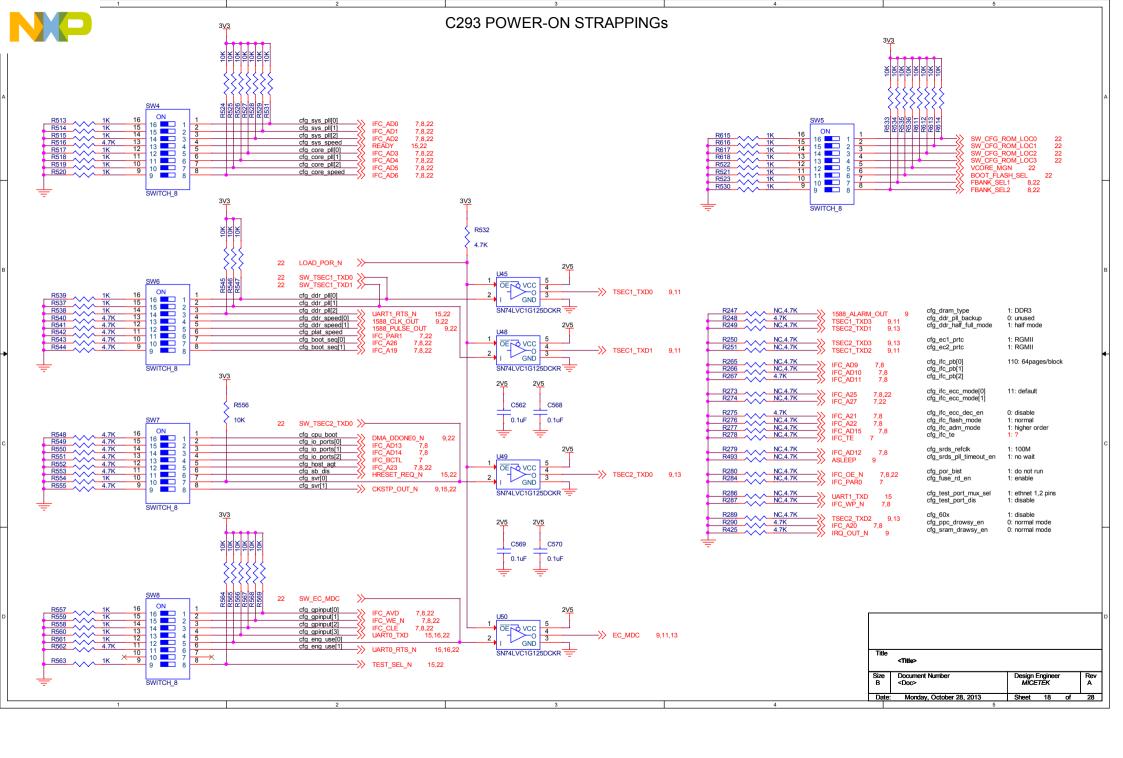


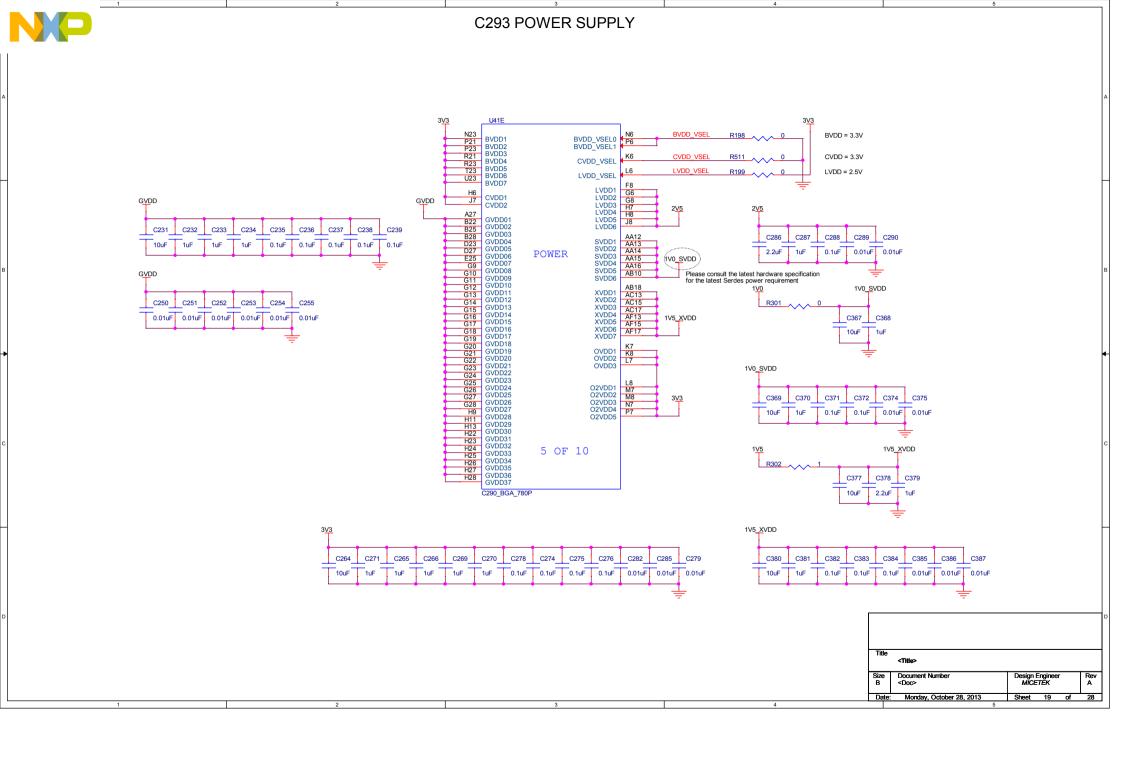


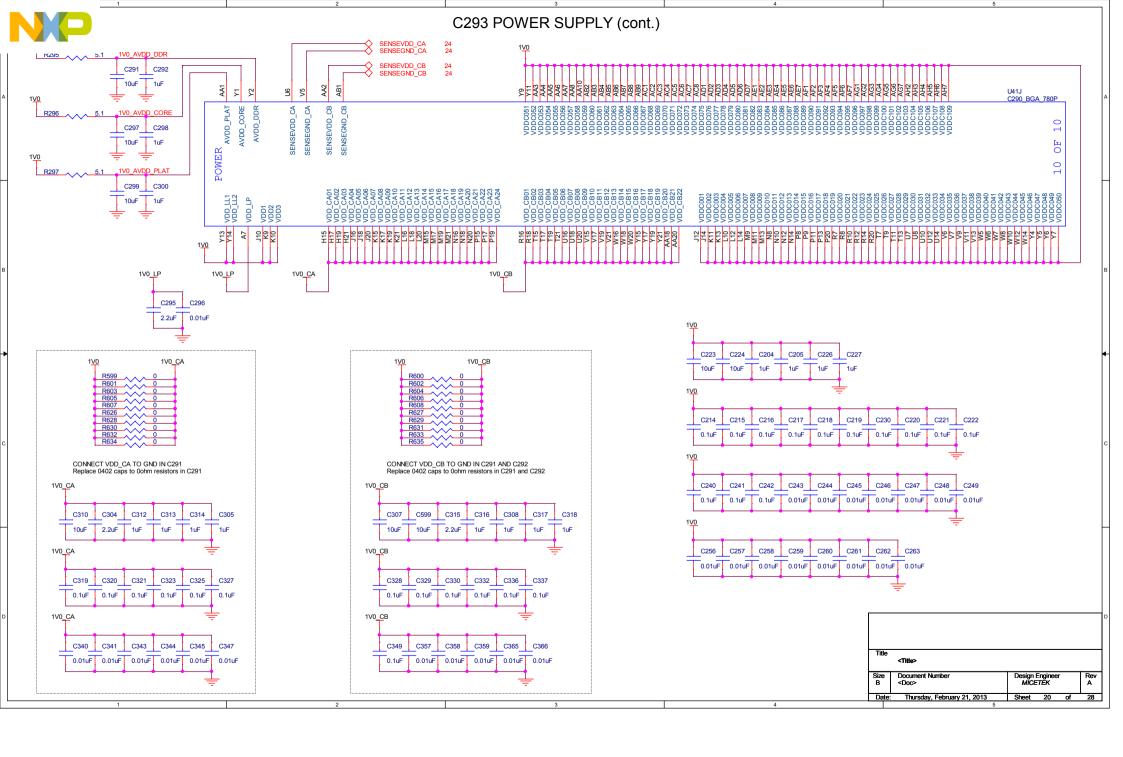


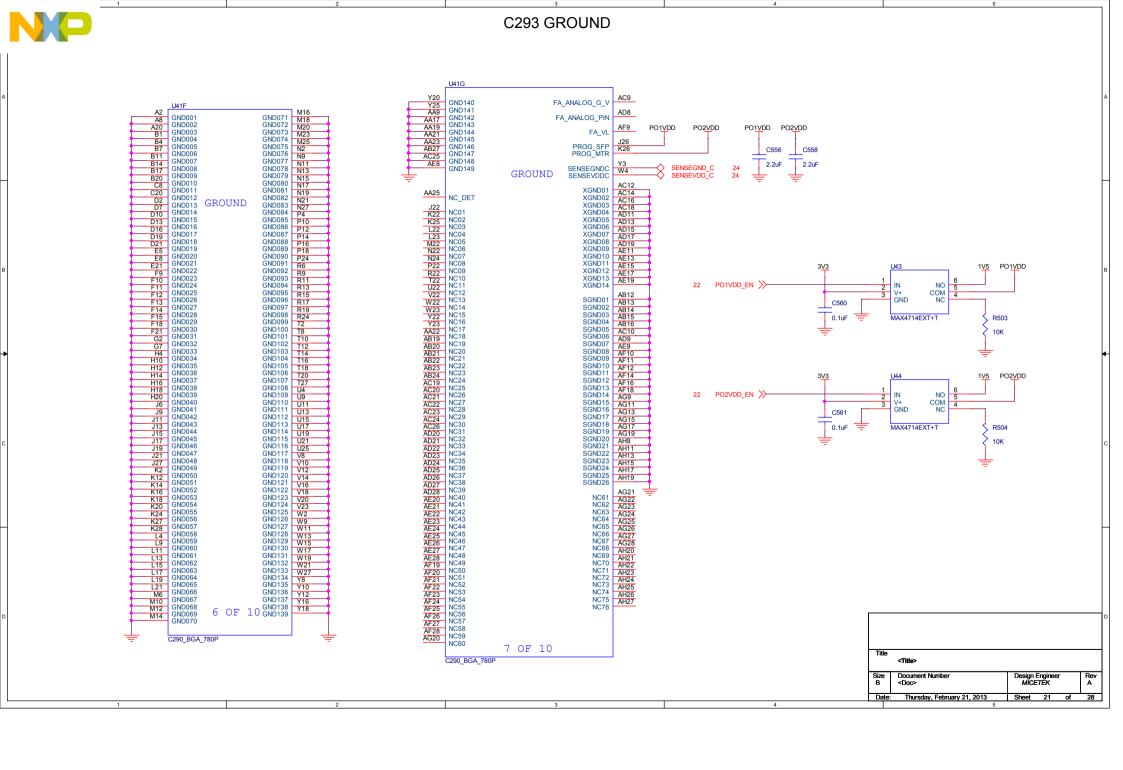












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EXT\_PWR\_DET
THERM\_N
FAN\_PWM IO-002 IO-052 IO-053 7,8,18 cfg rom loc[2] IO-002 IO-003 IFC A24 7.8 IO-053 cfg\_boot\_seq[0] 7,8,18 7,18 7,8,18 10-005 10-055 CPLD\_INT\_N PO1VDD\_EN 10-006 IO-056 A27 cfa svs pll[0] 21 21 10 057 \_\_\_\_ 10-007 cfg sys pll[1] 7,8,18 PO2VDD EN 10-008 IO-058 15 IO-008 16 IO-015 17 IO-016 18 IO-017 19 IO-018 20 IO-020 21 IO-020 26 IO-021 27 IO-026 28 IO-027 29 IO-028 cfg sys pll[2] IFC 10-061 66 7,8,18 7,8,18 7,8,18 7,8,18 18 18 24 LOAD\_POR\_N VCORE\_MGN cfa core pll( 10-066 AD3 cfa core pll[1] PS\_1V0\_MGN IFC AD4 10-067 10-068 69 cfg core pll[2] IFC AD5 7,8,18 7,8,18 cfg core speed 10-069 cfa rom loc[0] IFC\_AD7 CPLD CS N 7,8 IO-070 IO-071 IO-072 73 IO-073 74 IFC OE N 7.8.18 cfg\_gpinput[1] IFC WE N 7,8,18 NAND\_RB\_N IFC\_RB0\_N IFC\_RB1\_N 10-074 8 29 IO-028 30 IO-029 33 IO-030 34 IO-033 35 IO-034 36 IO-035 37 IO-037 IO-075 76 IO-076 77 10-070 IO-078 81 IO-081 BOOT\_FLASH\_SEL IFC CSO N 10-082 IO 89 IO 97 R305 33 IO 100 R306 33 IO 77 37 IO-036 38 IO-037 39 IO-038 40 IO-039 IO-083 84 BOOT FLASH SELECT NOR\_CS\_N NAND\_CS\_N FBANK\_SEL1 IO-084 84 PANEL LED IO-085 86 10 43 41 10-040 IO-086 87 8.18 42 IO-041 47 IO-042 48 IO-047 49 IO-048 10-041 10-087 IO-088 89 R304 \_\_\_\_ IO-089 31/3 PON\_RST\_N PEX\_RST\_N 10-090 LED\_PM\_1 C388 22pF IO-030 IO-091 92 10-049 50 IO-050 IO-092 cfg\_sb\_dis HRESET\_REQ\_N
CPU\_TRST\_N
HRESET\_N 19 15,18 IO-051 IO-095 IO-095 IO-096 IO-097 IO-097 15 RESET 10-098 99 NOR\_RST\_N DDR3 RESET N 3V3 10-099 100 GE1 RST N IO-100 IO-001 GE2\_RST\_N 13 C389 IO/DEV\_OE 0.1uF COP TRST N IO/DEV\_CLRn COP CONN. COP SRST N 12 14 IO/GCLK0 62 IO/GCLK1 CPLD\_REFCLK 3<u>V3</u> IFC\_CLK 64 IO/GCLK2 3V3 R312 \_\_\_\_\_0  $\begin{array}{c|c}
NC & VCC & \frac{5}{4} \\
& 0 & 3
\end{array}$ WDI 9 17 →>> DDR3\_RST\_N R313 4.7K R314 4.7K R315 4.7K 23 22 TDI TMS WDO\_N 17 25 CPLD TDO WATCHDOG DDR3 RESET N TDO WD\_CFG0 17 GND WD\_CFG1 WD\_CFG2 NC,74LVC1G07DCKR TCK R316\_\_\_\_\_ 13 63 VCCINT **GNDINT** 65 cfg sys speed cfg ddr pll[0] READY 15,18 SW\_TSEC1\_TXD0 SW\_TSEC1\_TXD1 VCCINT GNDINT 18 cfg\_ddr\_pll[1] VCCIO1 CPLD JTAG CONNECTOR cfg\_ddr\_pll[2 VCCIO1 GNDIO 32 GNDIO 46 UART1\_RTS\_N IFC\_AD8 7 45 cfg rom loc[1 VCCIO1 cfg\_rom\_loc[3] DMA\_DACK0\_N 1588 CLK OUT **GNDIO** GNDIO 60 GNDIO 79 cfg ddr speed[ VCCIO2 9,18 cfg ddr speed[1] VCCIO2 GNDIO 1588\_PULSE\_OUT 93 cfg plat speed VCCIO2 GNDIO IFC\_PAR1 7,18 IFC A19 7,8,18 cfa boot seaf1 ×-CPLD\_TDI cfg cpu boot DMA\_DDONE0\_N 10 FPM240T100C5N POR STRAPPING cfg\_svr[0] SW\_TSEC2\_TXD0 TSM-105-01-S-DV cfg\_svr[1] CKSTP\_OUT\_N IFC\_AVD 7,8,18 IFC\_CLE 7,8,18 9,15,18 cfa apinput(0 7818 3V3 cfg\_gpinput[2] cfg\_gpinput[3] UARTO\_TXD SW\_EC\_MDC UARTO\_RTS\_N 15,16,18 cfg\_eng\_use[0 cfg\_eng\_use[1 18 15,16,1/ C390 C391 C392 C393 C394 C395 C396 C397 SW\_CFG\_ROM\_LOC0 SW\_CFG\_ROM\_LOC1 1uF 1uF 0.1uF 0.1uF 0.1uF 0.1uF 0.1uF 0.1uF SW\_CFG\_ROM\_LOC2 SW\_CFG\_ROM\_LOC3 Title <Title> Size Document Number Design Engineer MICETEK Rev A В <Doc> Date: Friday, February 22, 2013 Sheet 22 of 28

