



C290PCle-RDB

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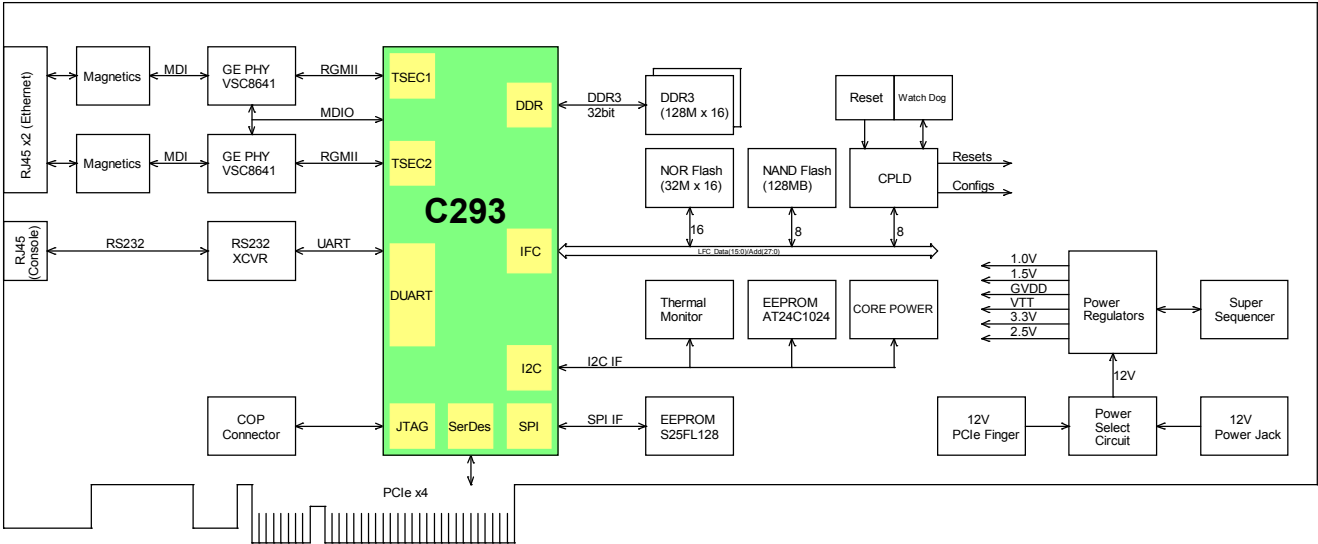
Version Control		
Version	Date	Modifications
V0.1	2012/09	First release of Schematics
V0.2	2012/10	update C293 symbol, change GE phy to VSC8641, add I2C boot EEPROM
V0.3	2012/10	update POR strappings
V0.4	2012/10	1. Change DDR3 to 3 x16 chips. Page 4-6 2. Add FBANK_SEL2 to NOR Flash, change NOR Flash MPN to S29GL512P11TF10. Page 8 3. Add pull-up resistor to PIN10 of NAND Flash. Page 8 4. Add pull-up resistor to TSEC1_GTX_CLK for cfg_60x in P1010 interposer. Page 8 5. Correct net name errors of "GE2_CM0DEX". Page 13 6. Remove UART1 signals and RJ45 connector. Page 15/16 7. Change POR-ON strappings with connect to switches and CPLD. Page 18/22 8. Connect MGN signal to CPLD and switch to change VCORE voltage. Page 24 9. Change heatsink to S06QZZ0B. Page 28
V0.5	2012/11	1. Swap DDR3 data bus order for layout. Page 4/5/6 2. Change switch pull-up pull-down resistors to same side. Page 18 3. Add sw_cfg_rom_loc[0:3] from switch to CPLD. Page 18/22
V0.6	2012/11	1. Swap CPLD pins for layout. Page 22 2. Reduce power decoupling caps of C293. Page 20
V0.7	2012/11	1. Generate SOC MVREF use voltage divider. Page 3 2. Delete 4.7pF cap on DDR3 clock pair. Page 3 3. Delete optional pull down resistor for TMP_DETECT_B. Page 15
V0.8	2012/11	1. Add a 0603 cap to 1V0_CB. Page 20 2. Add several caps acrossing plane splits. Page 28
V0.9	2012/12	1. Add a 1000pF cap between ZL_VSEN_P and ZL_VSEN_N. Page 24 2. Change U34 to SOT23-5 footprint and connect NC pin to GND. Page 25
V1.0	2013/02	update BOM
V1.1	2013/02	1. Change NAND Flash R/B to CPLD, then CPLD to C293 R/B0 and R/B1. Page 7/8/22 2. Add a 0.01uF cap to PEX_RST_N. Page 10 3. Change panel LED to single color. Page 22
V2.0	2013/08	Add 6pin ATX 6pin power connector, remove PTC and common mode chock Page 25
V2.1	2013/10	Add notes for serdes power and nand flash stuff R248, R275, R299,

All information is subject to change without notice.  
No warranty, expressed or applied, is made as to the accuracy of the information contained herein. This schematic is provided for reference purposes only.  
Contact your Freescale representative to obtain the latest information on this product.

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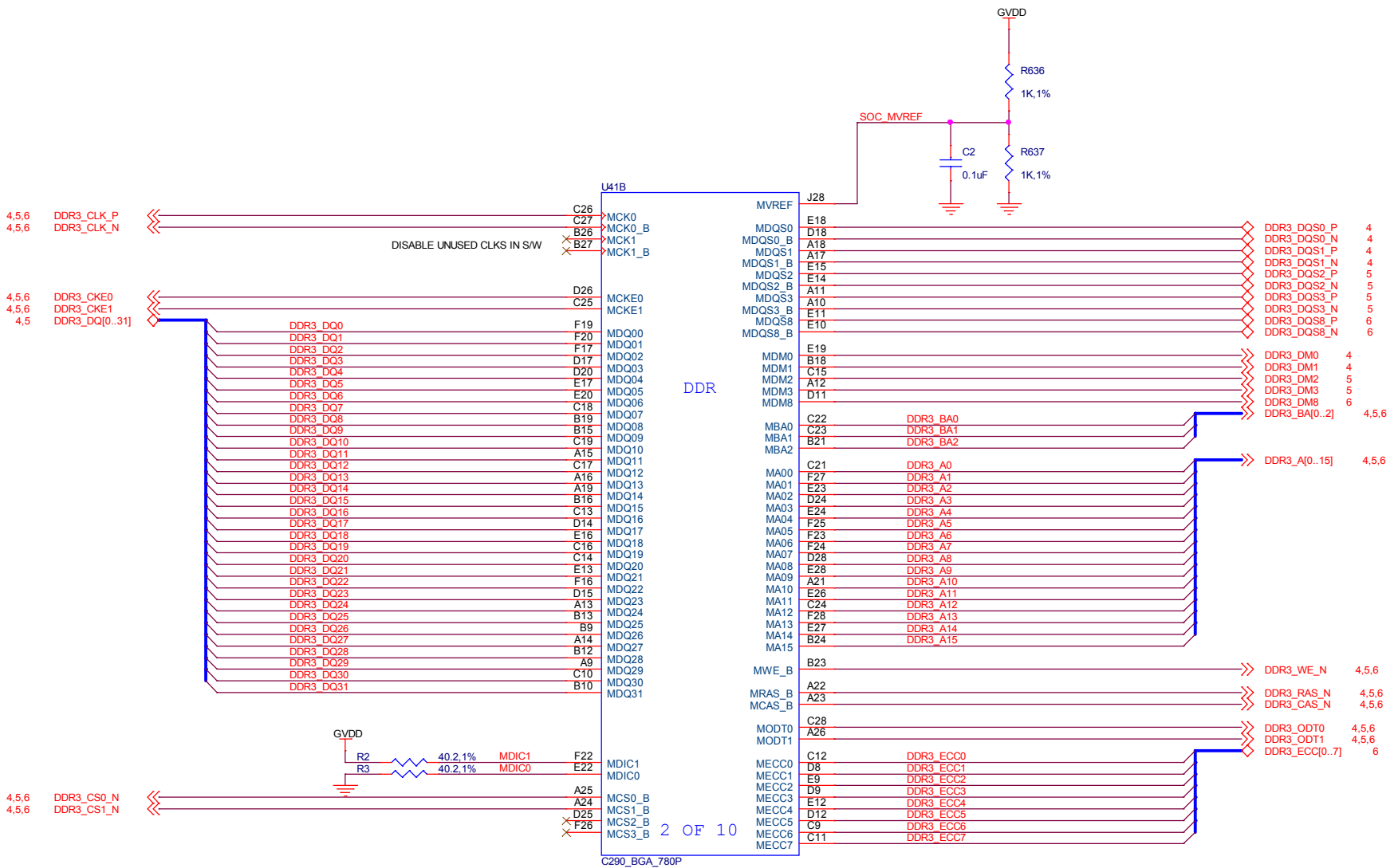
SYSTEM BLOCK DIAGRAM



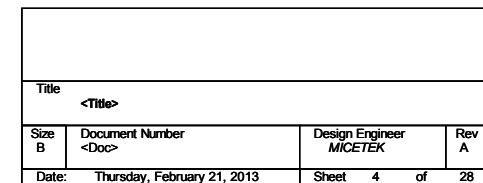
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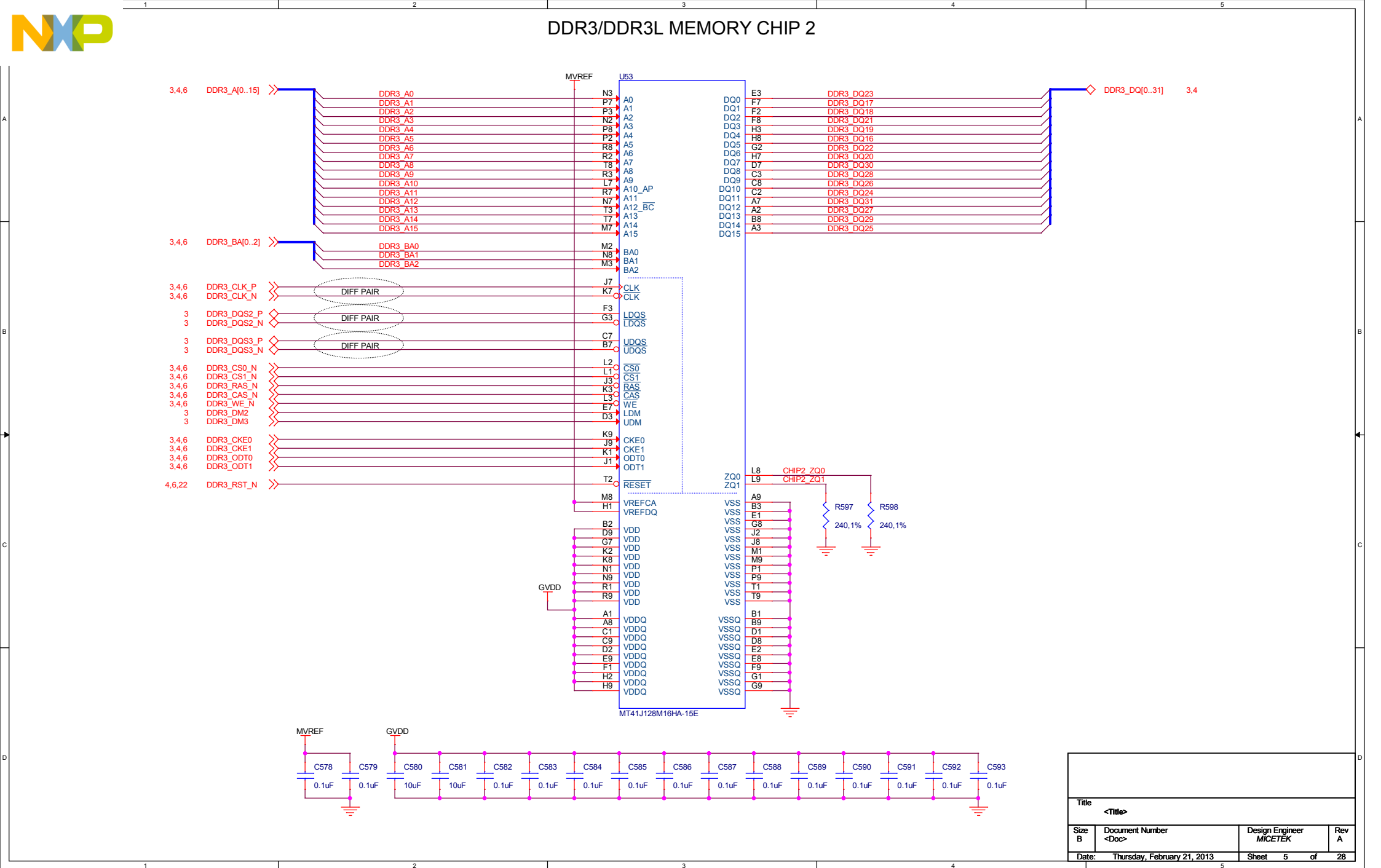


C293 DDR3/DDR3L MEMORY INTERFACE



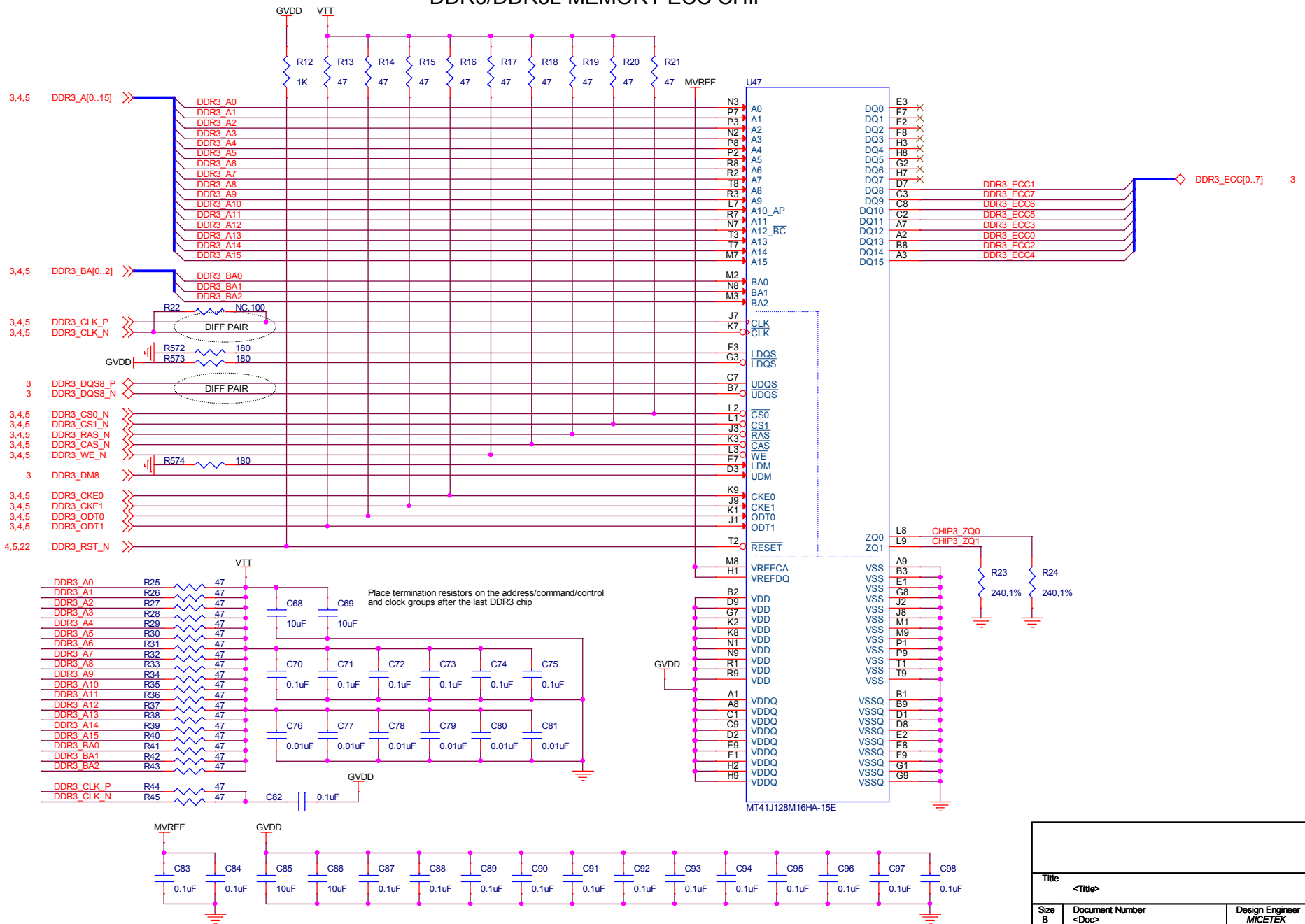
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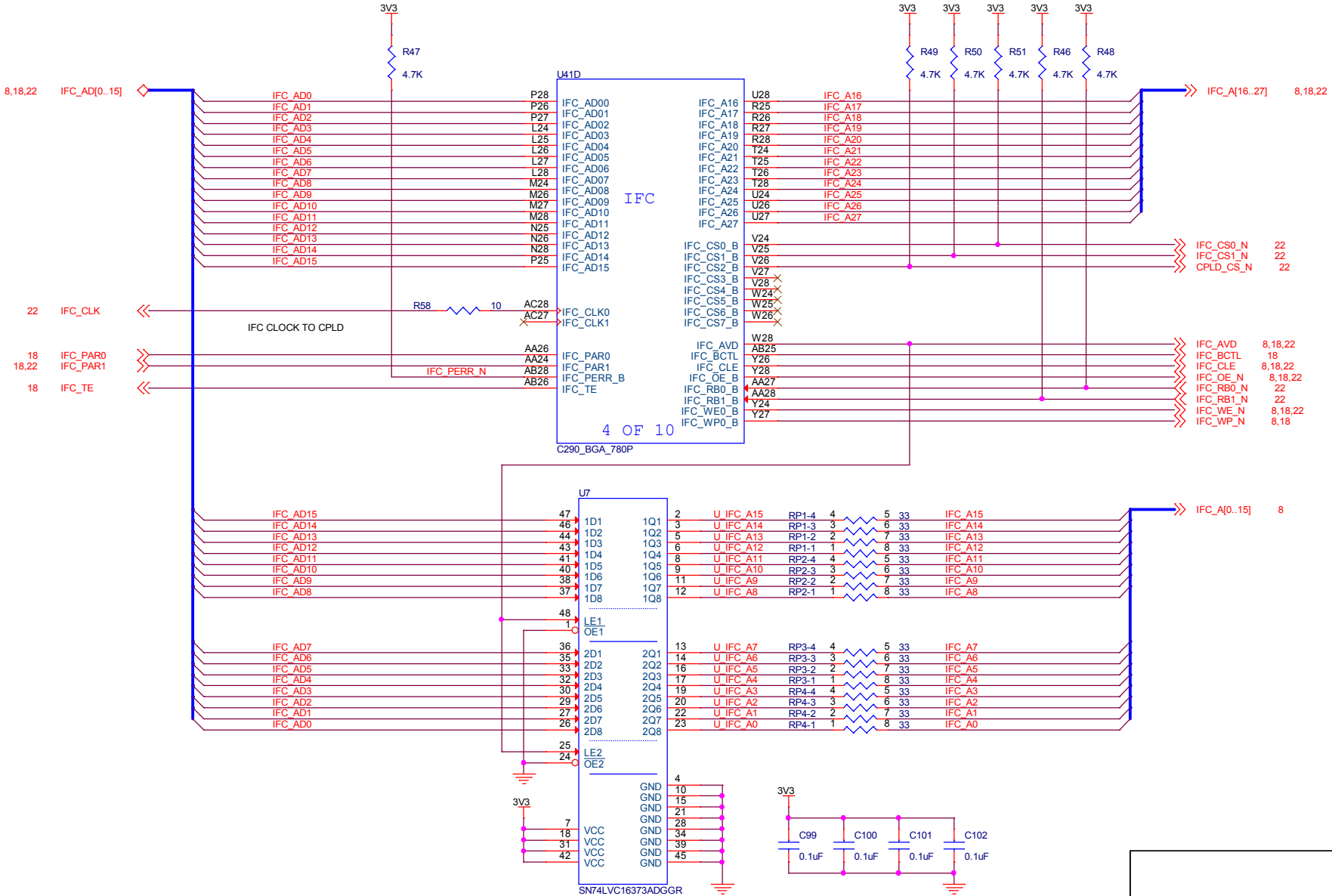


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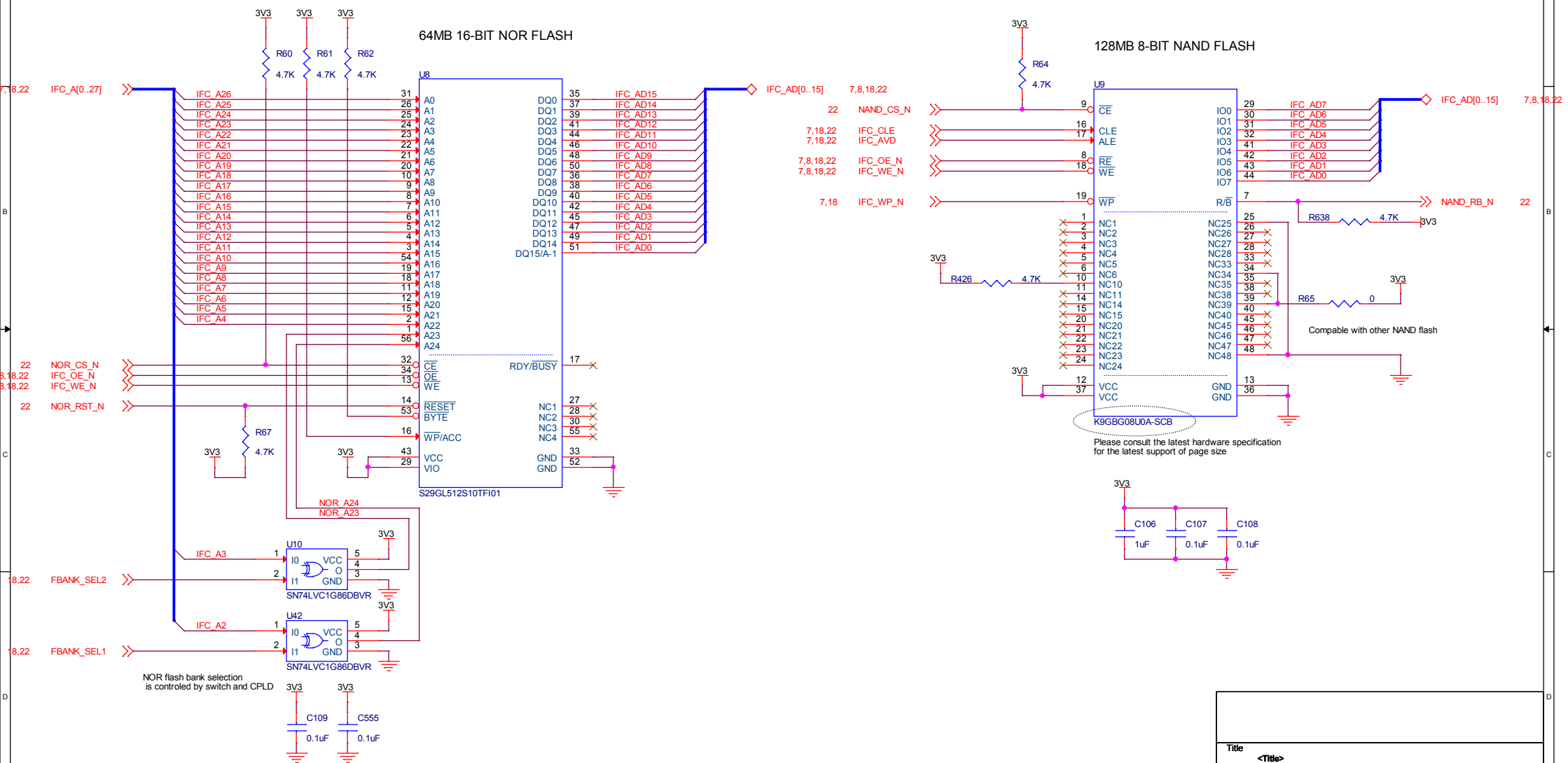




C293 IFC INTERFACE



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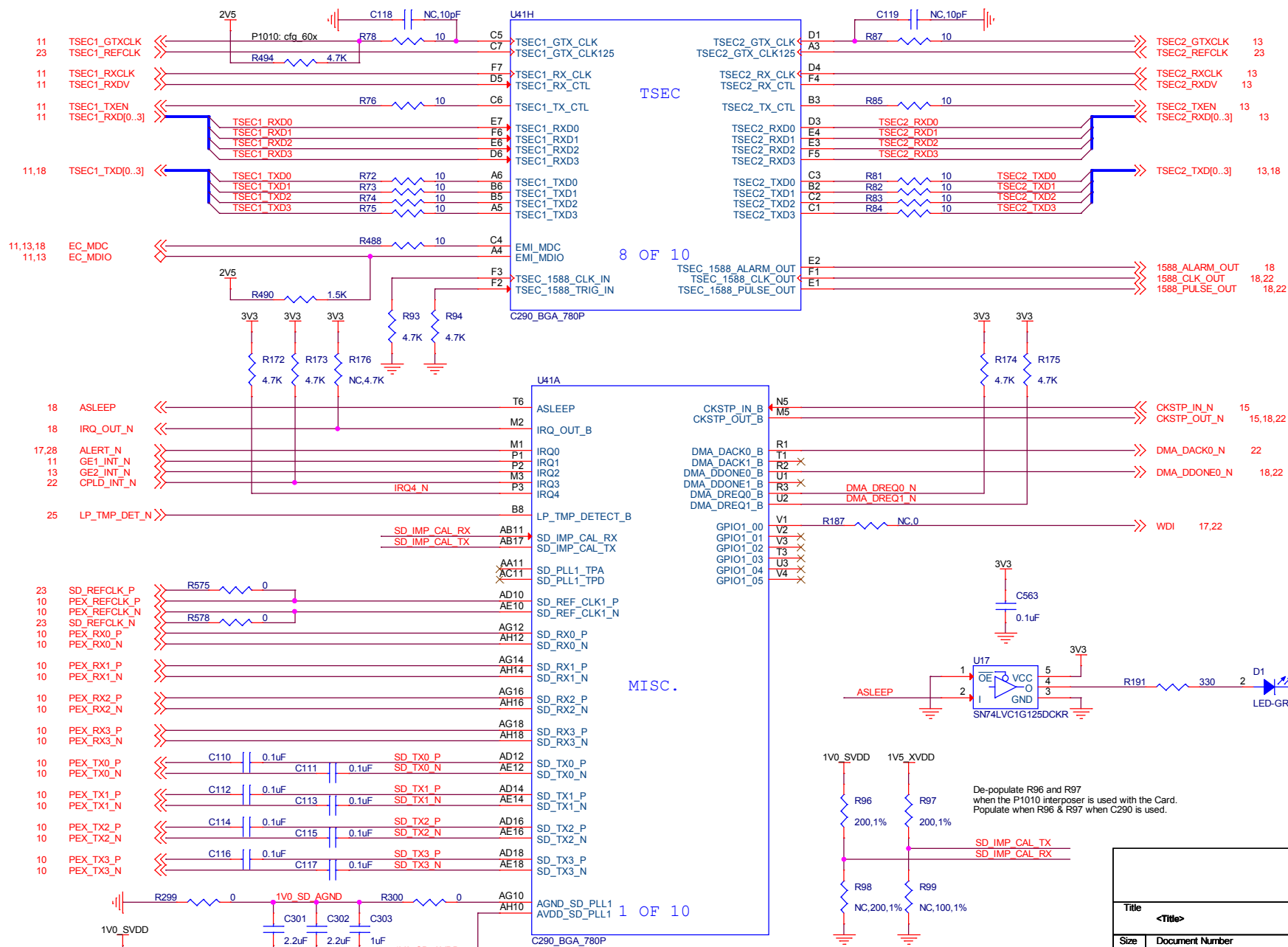


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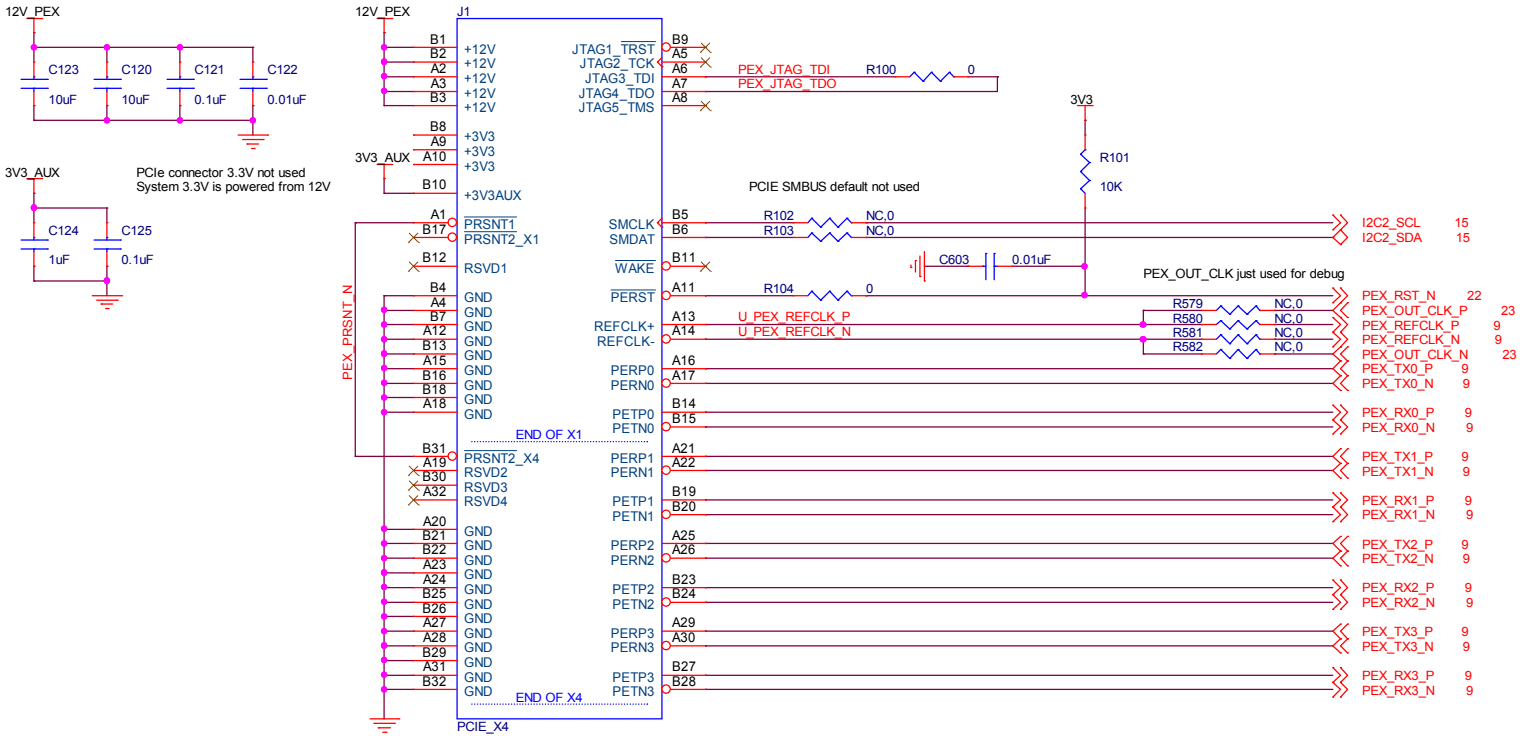


# C293 SERDES and TSEC 1&2 INTERFACE

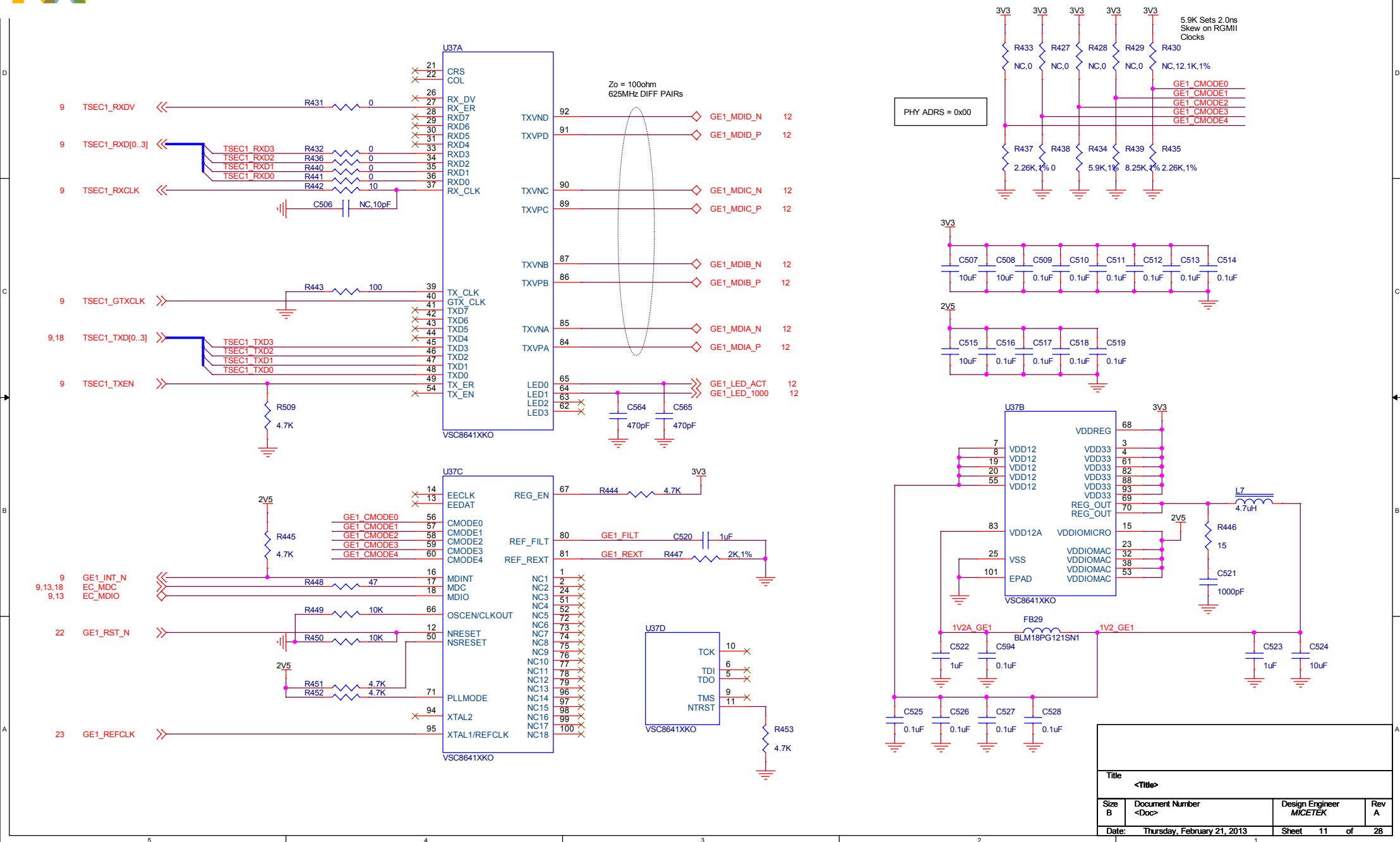


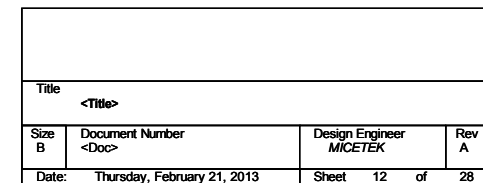


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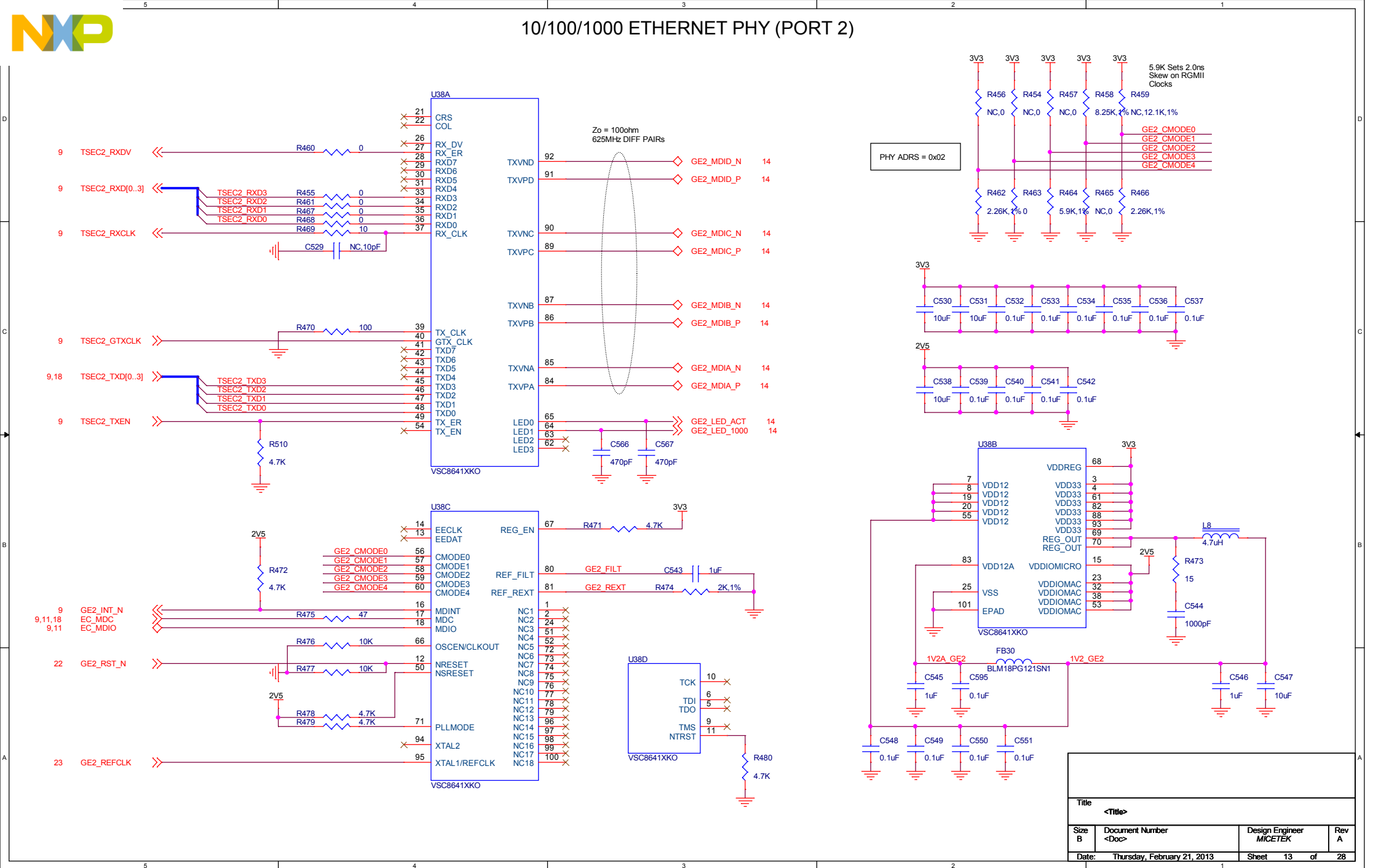
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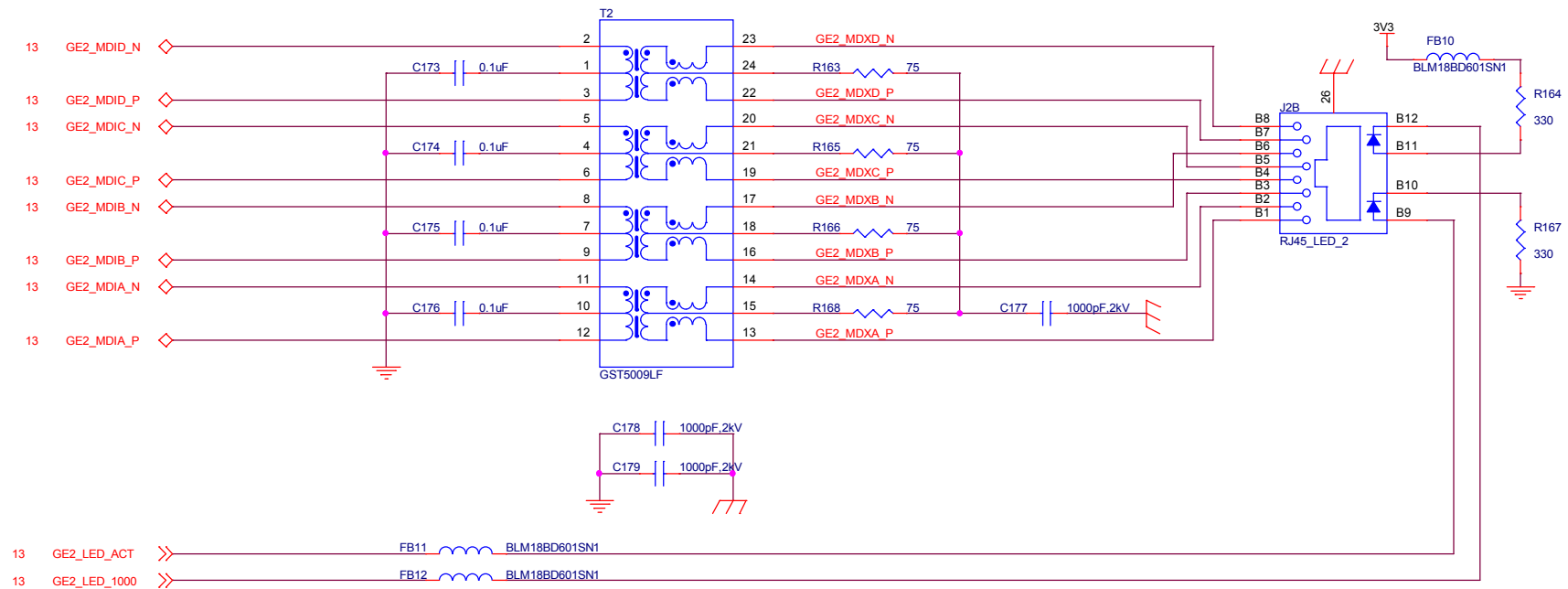




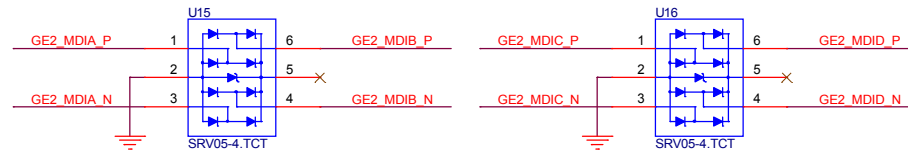


10/100/1000 ETHERNET PHY (PORT 2)





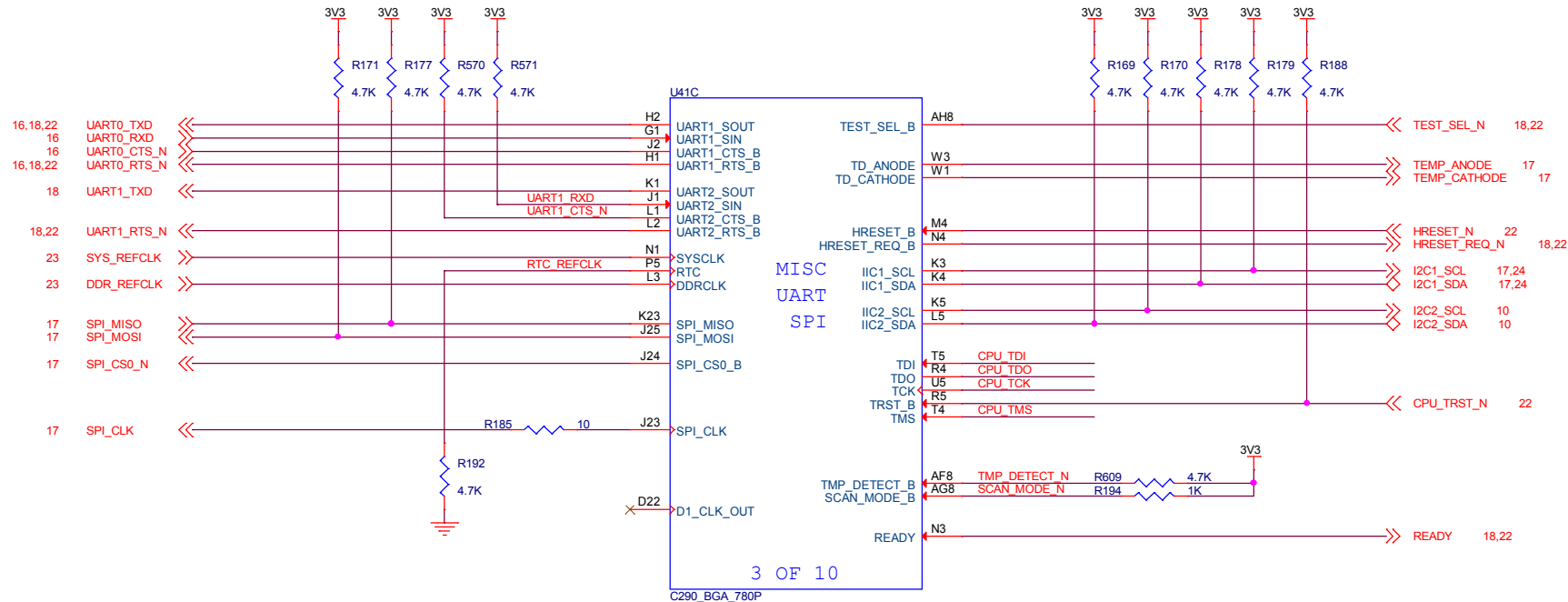
For Gigabit Ethernet protection, place close to magnetics



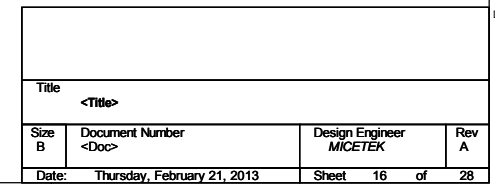
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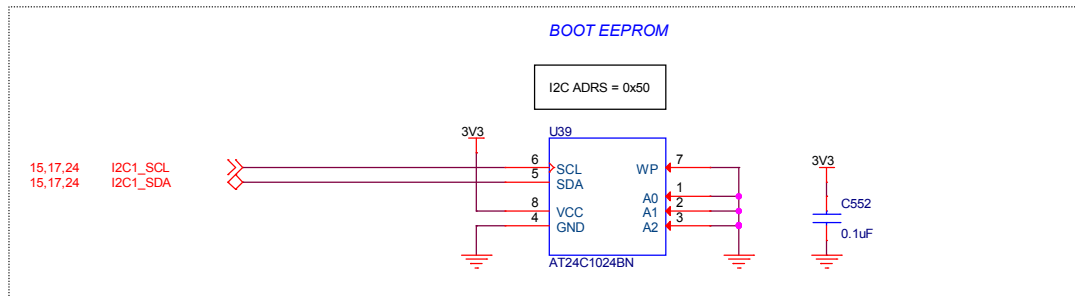
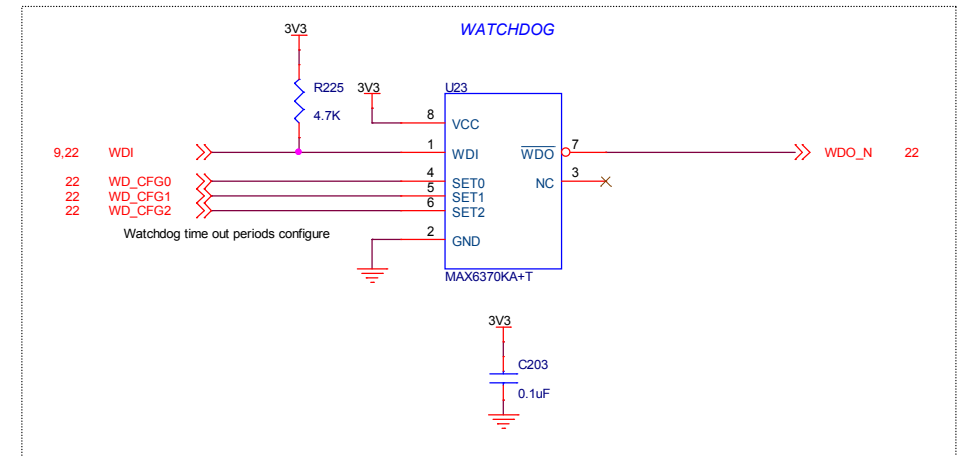
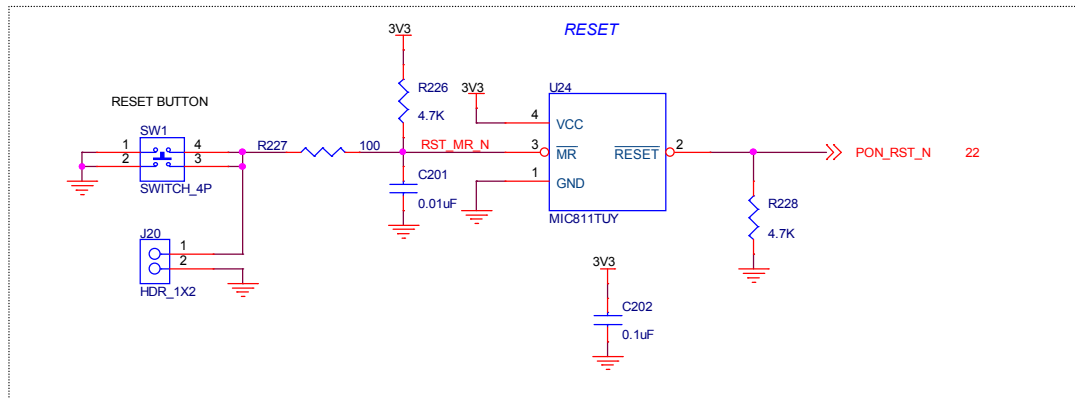
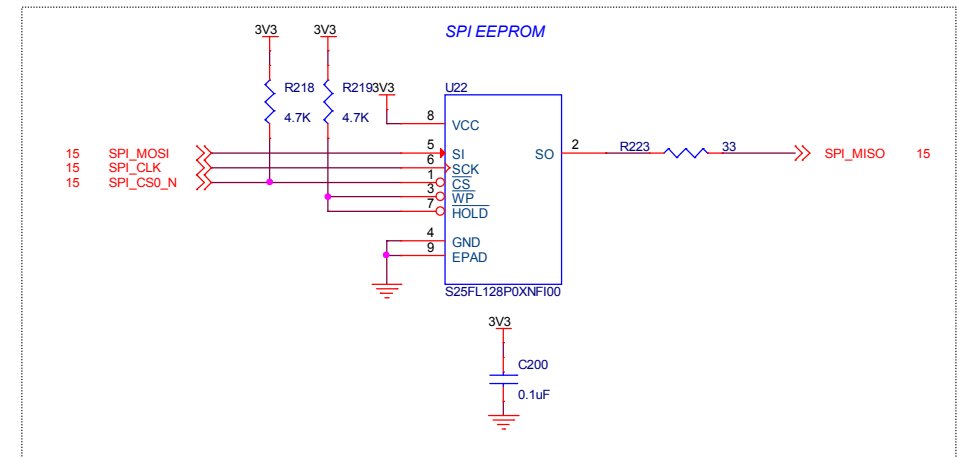
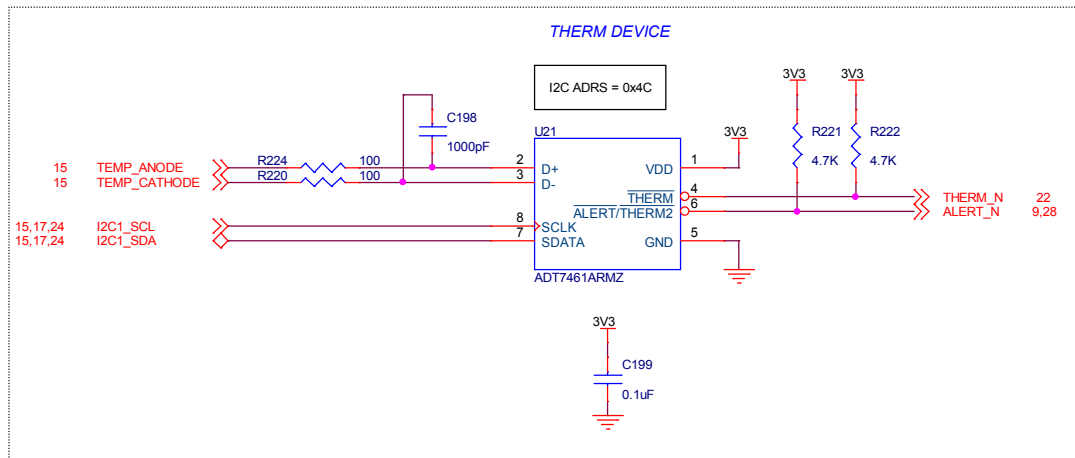
C293 MISC



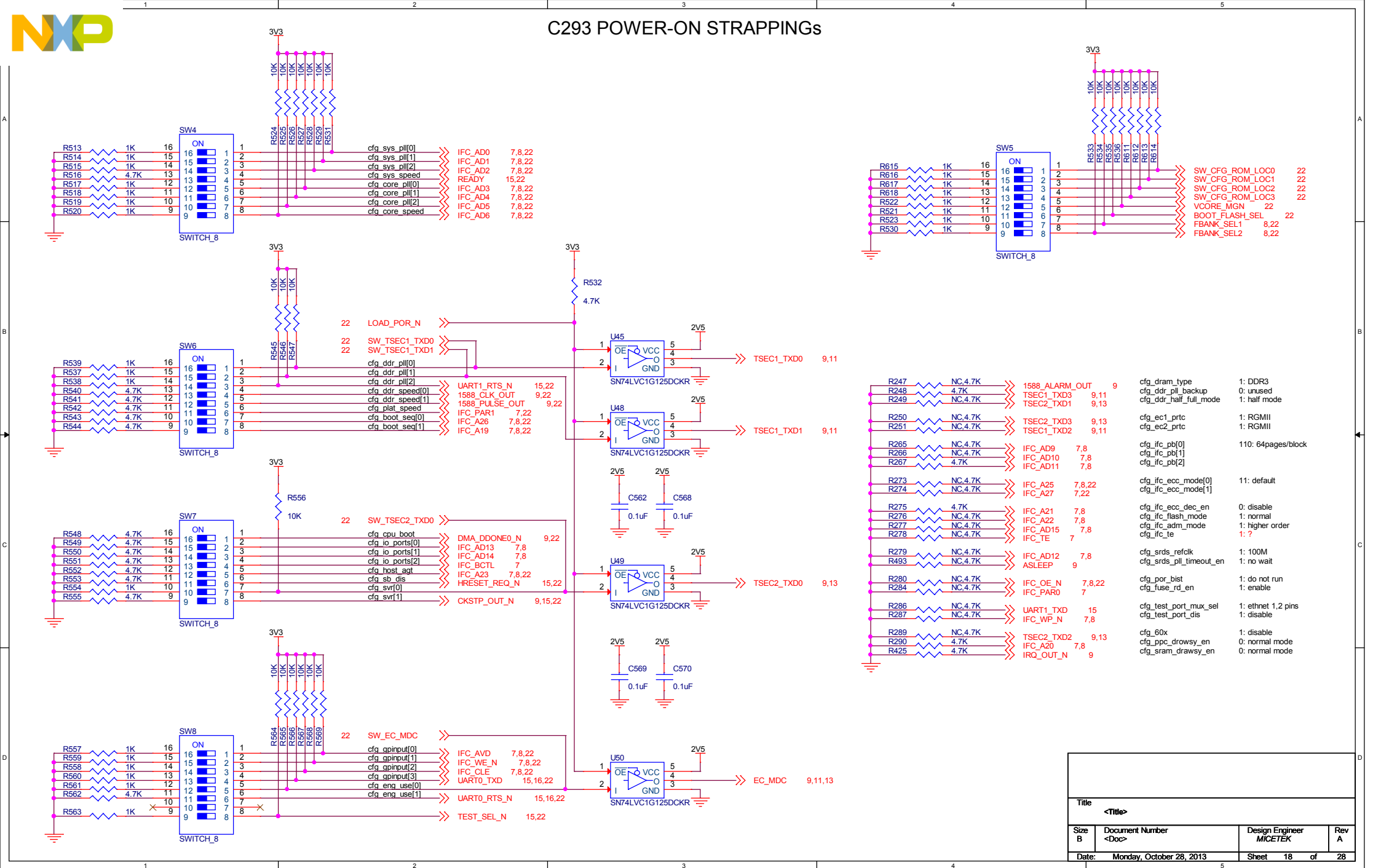
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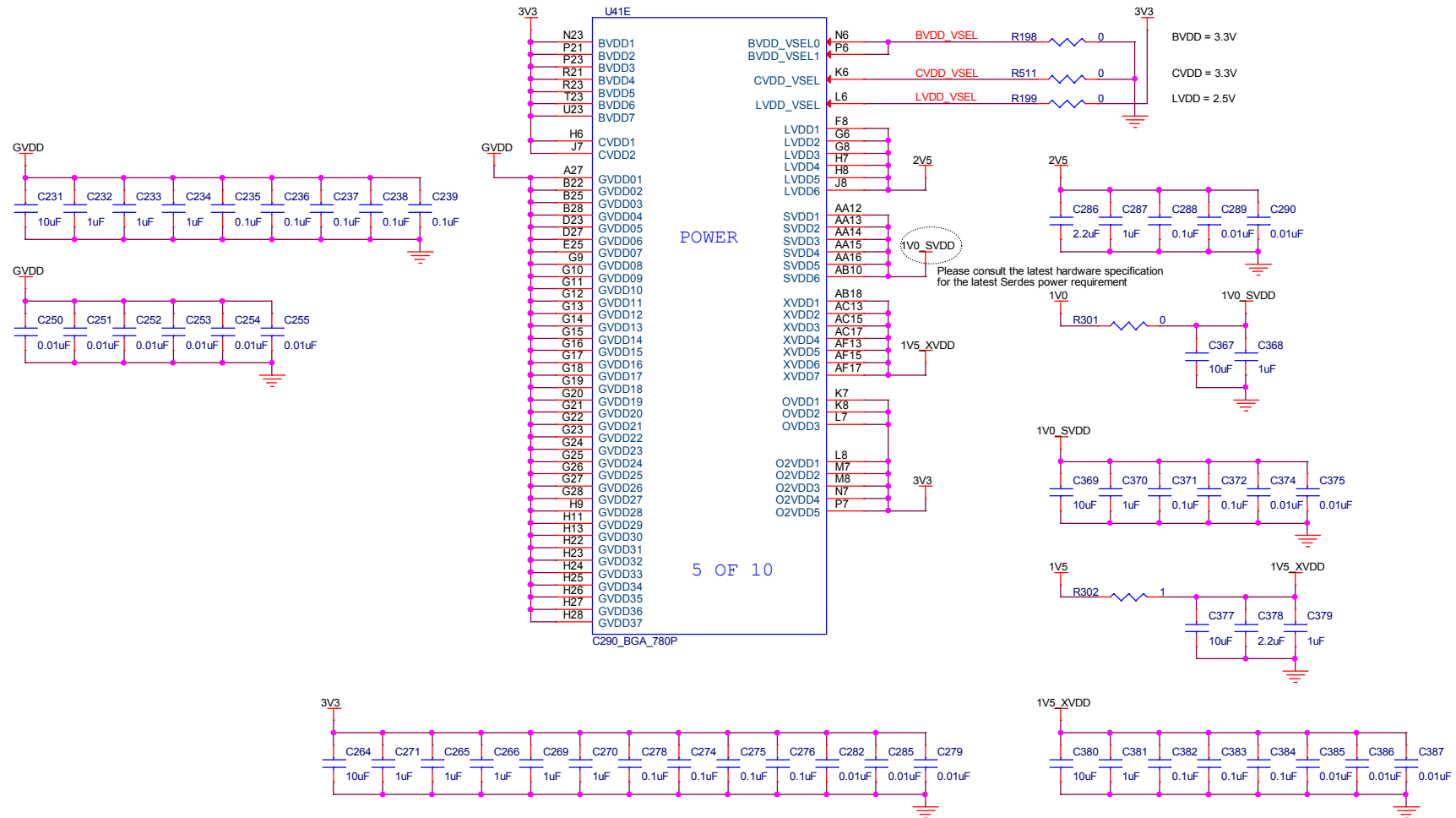


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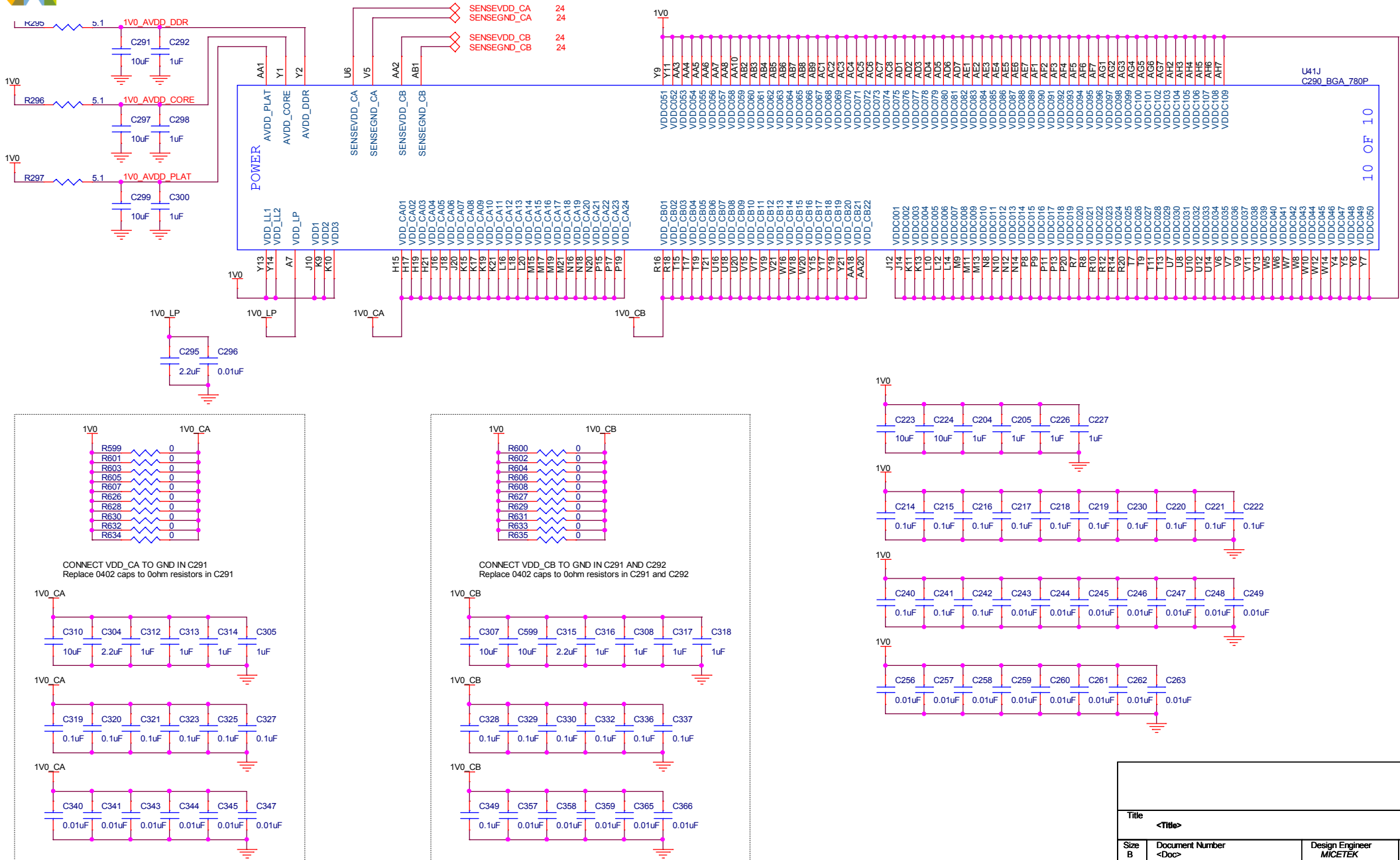
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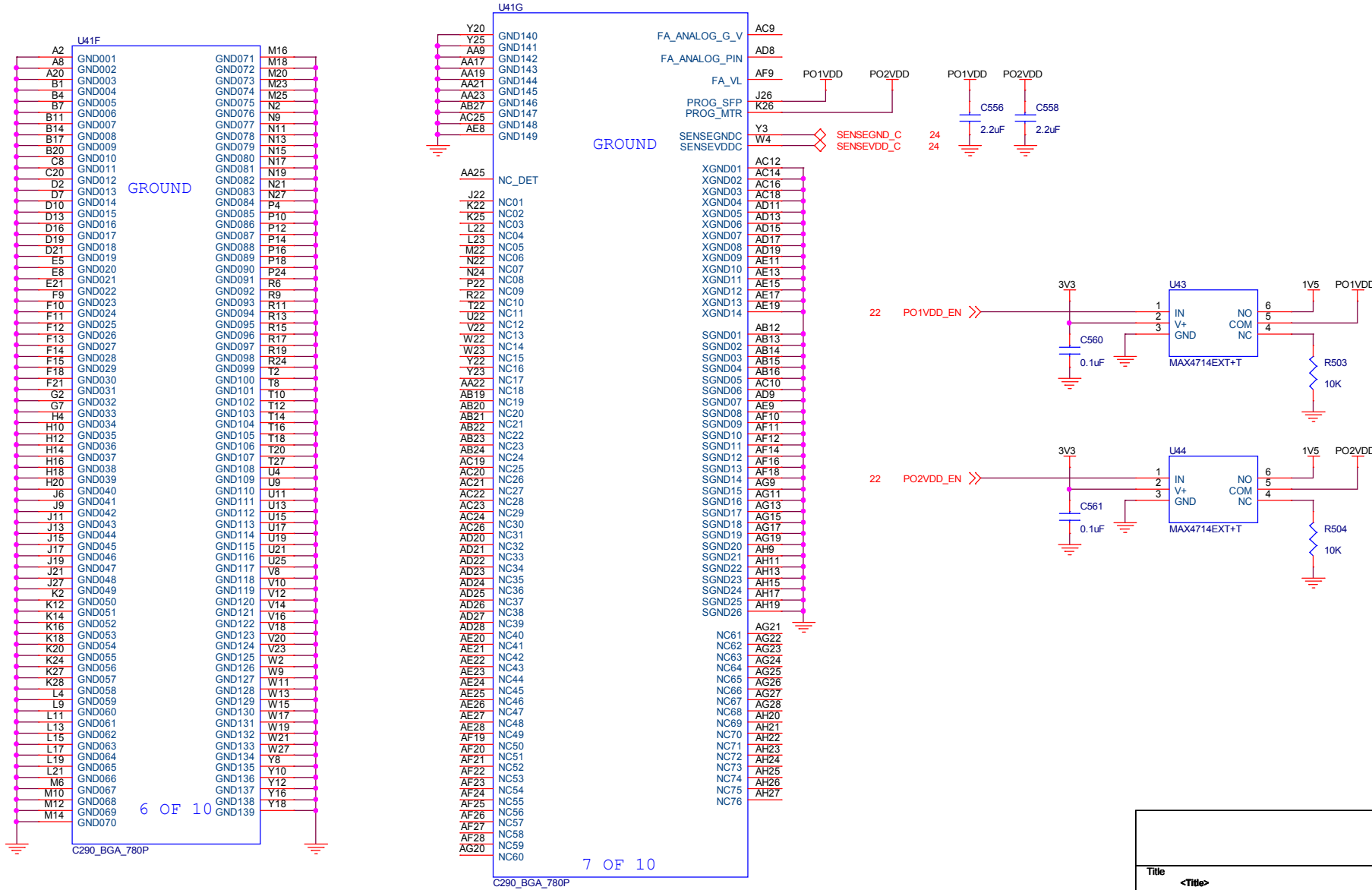
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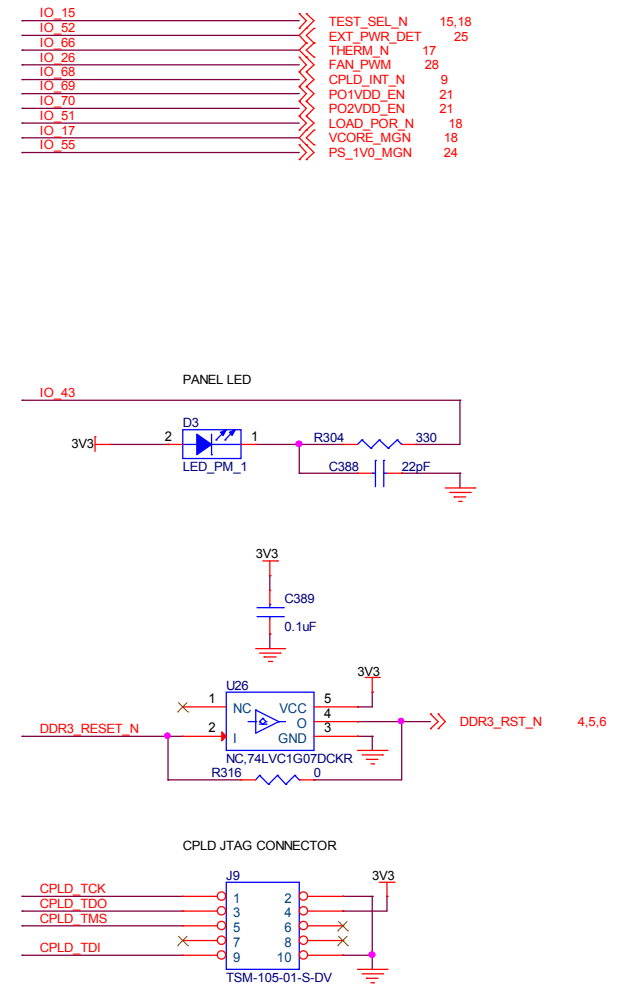
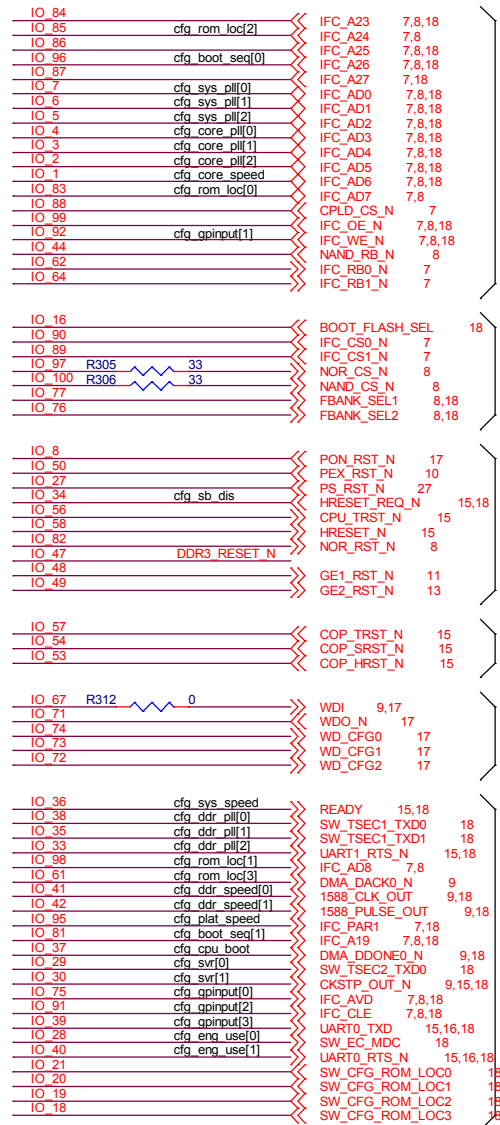
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C293 GROUND



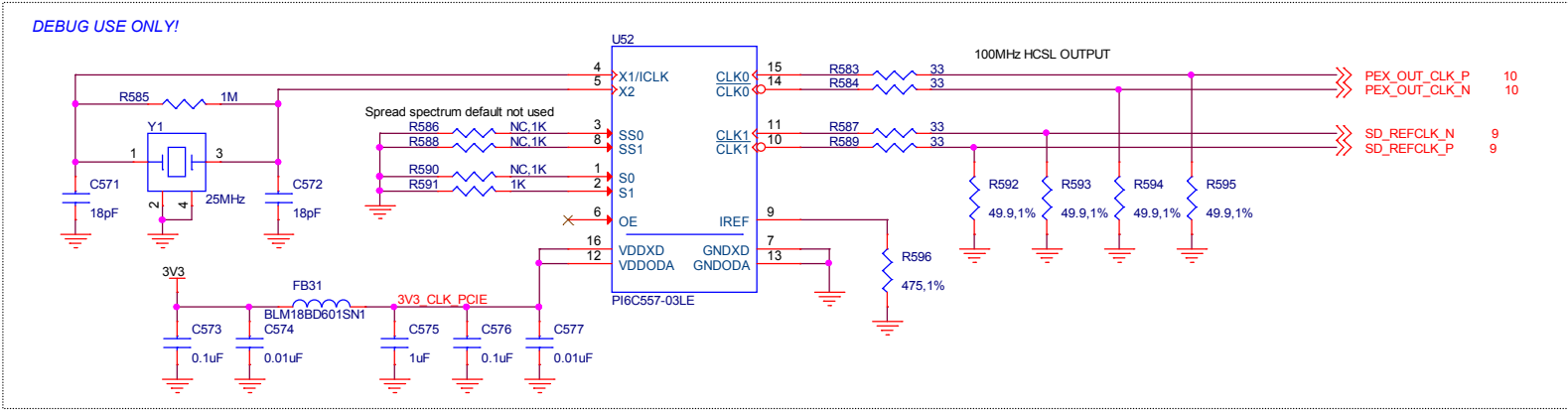
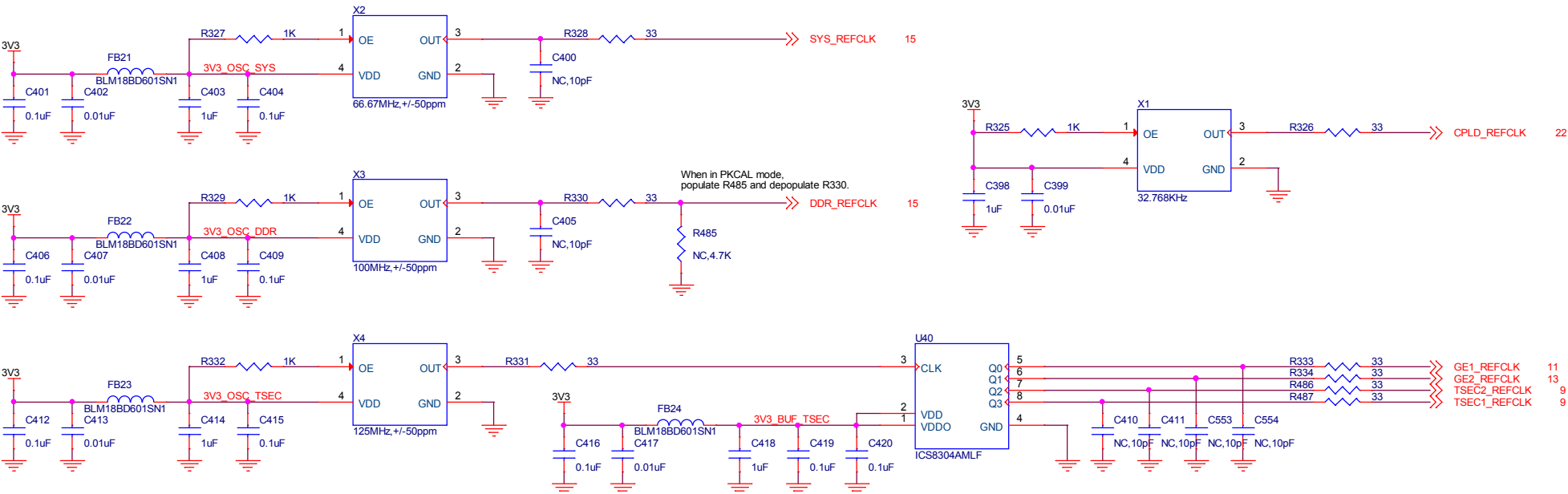
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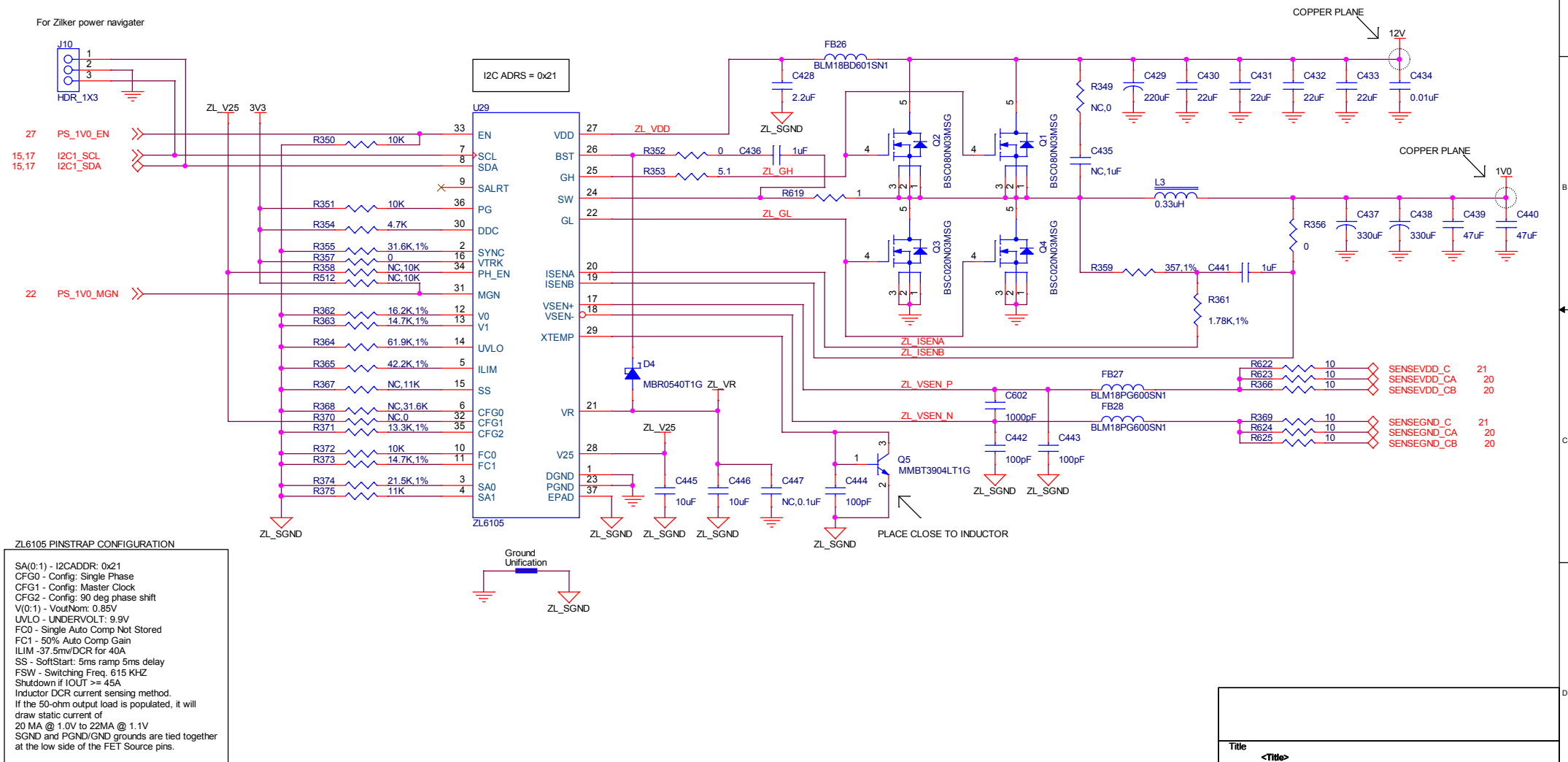
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SYSTEM CLOCK GENERATORS

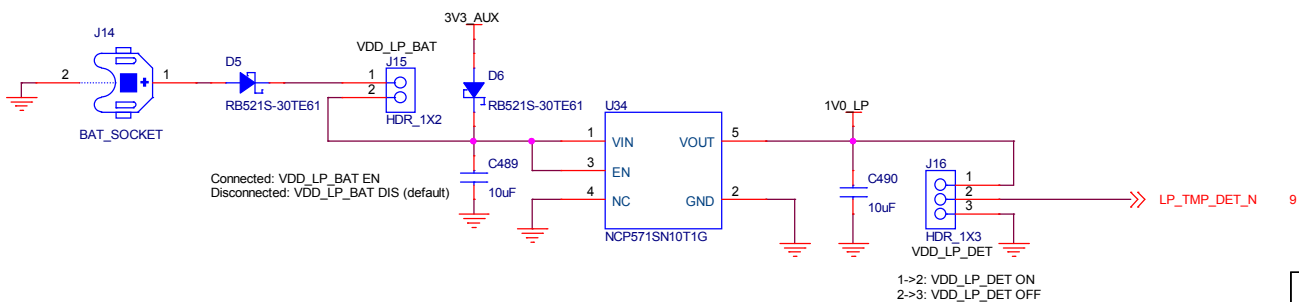


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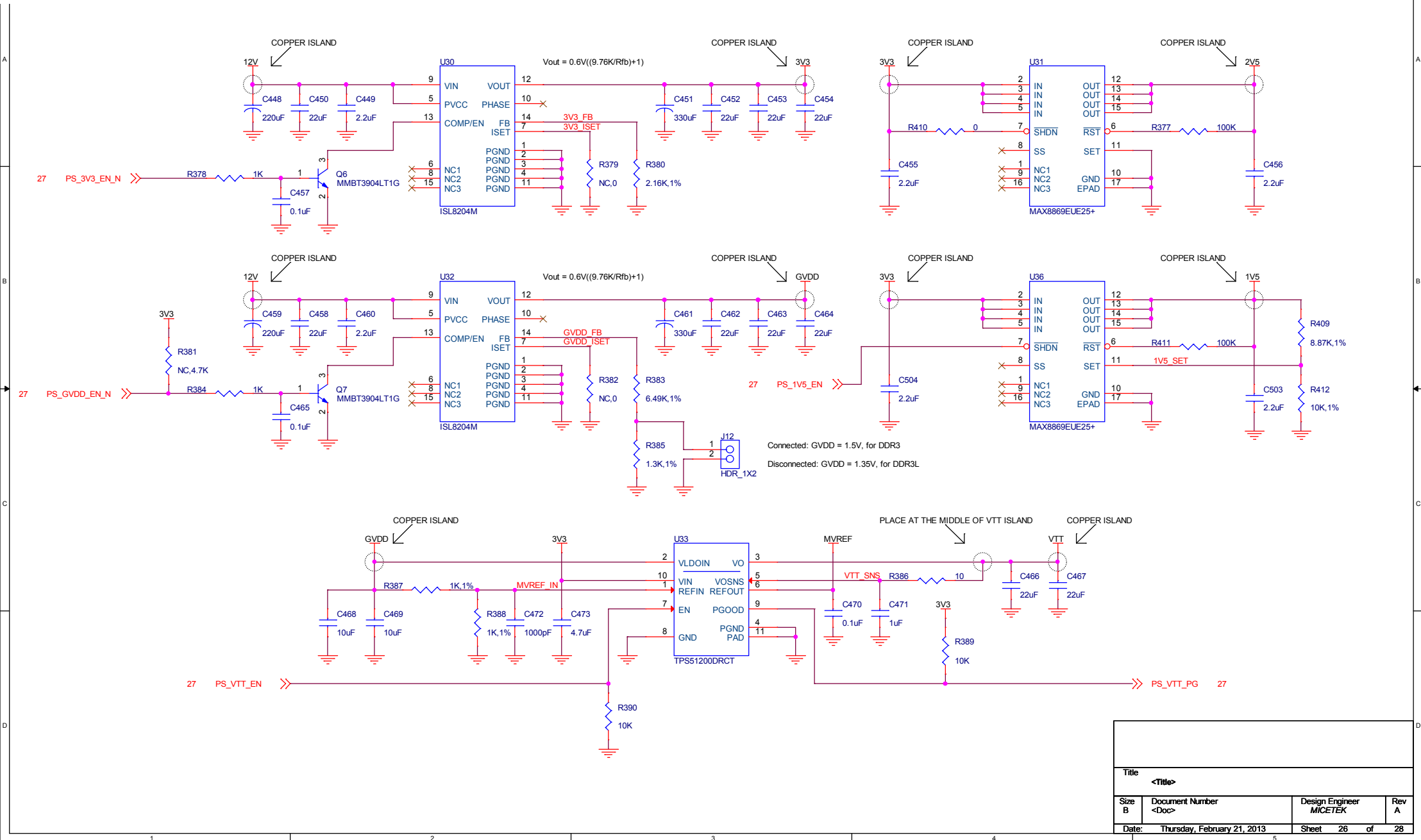


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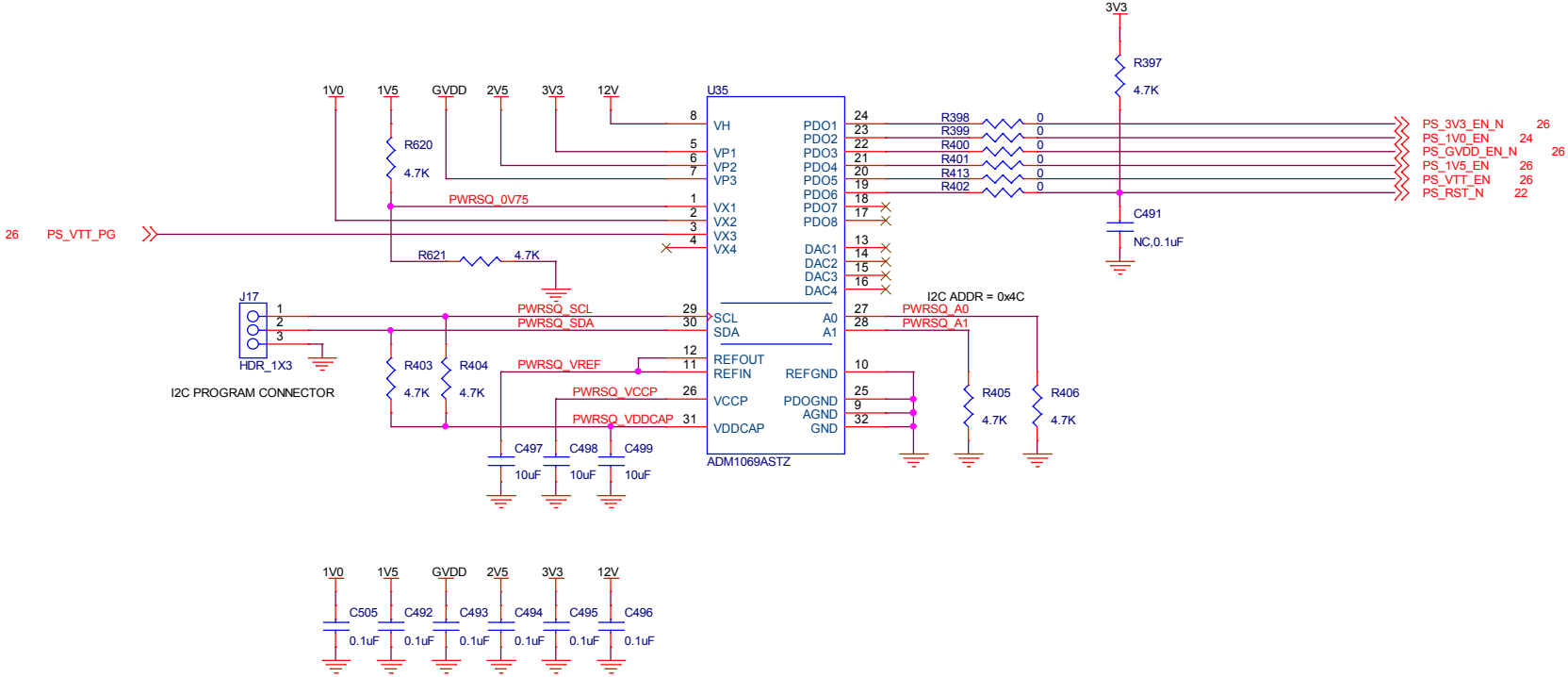
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SYSTEM POWER ON SEQUENCING



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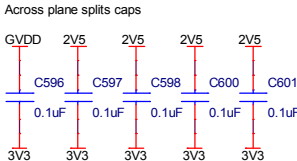
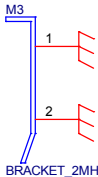
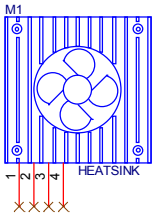


MECHANICALs

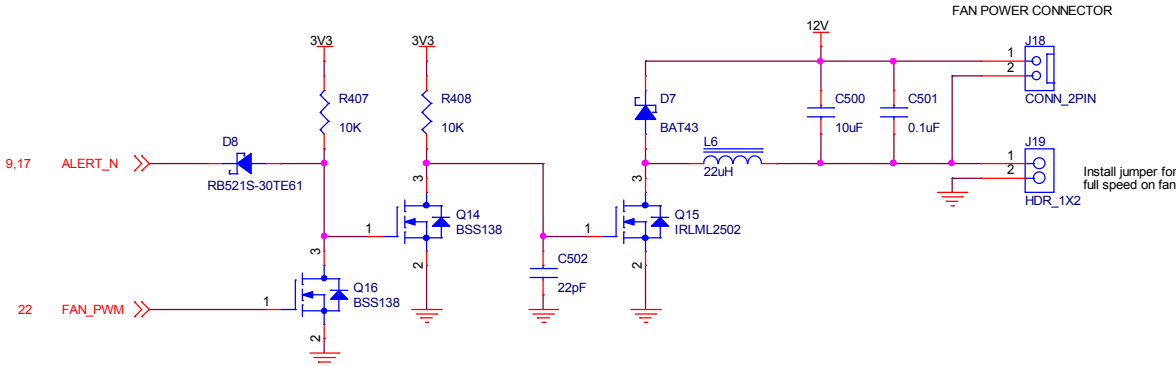
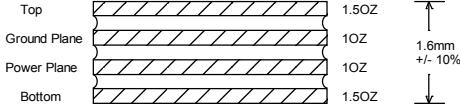
Fiducial Marks



Mouting Holes



Layer Detail



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