Artix®-7 FPGAs

XILINX

			Artix®-7 FPGAs Optimized for Lowest Cost and Lowest Power Applications (1.0V, 0.95V, 0.9V)					
	Part Number		XC7A15T	XC7A35T	XC7A50T	XC7A75T	XC7A100T	XC7A200T
Logic Resources	Logic Cells		16,640	33,280	52,160	75,520	101,440	215,360
	Slices		2,600	5,200	8,150	11,800	15,850	33,650
	CLB Flip-Flops		20,800	41,600	65,200	94,400	126,800	269,200
Memory Resources	Maximum Distributed RAM (Kb)		200	400	600	892	1,188	2,888
	Block RAM/FIFO w/ ECC (36 Kb each)		25	50	75	105	135	365
	Total Block RAM (Kb)		900	1,800	2,700	3,780	4,860	13,140
Clock Resources	CMTs (1 MMCM + 1 PLL)		5	5	5	6	6	10
I/O Resources	Maximum Single-Ended I/O		250	250	250	300	300	500
	Maximum Differential I/O Pairs		120	120	120	144	144	240
Embedded Hard IP Resources	DSP Slices		45	90	120	180	240	740
	PCIe® Gen2[1]		1	1	1	1	1	1
	Analog Mixed Signal (AMS) / XADC		1	1	1	1	1	1
	Configuration AES / HMAC Blocks		1	1	1	1	1	1
	GTP Transceivers (6.6 Gb/s Max Rate)[2]		4	4	4	8	8	16
Speed Grades		Commercial	-1, -2	-1, -2	-1, -2	-1, -2	-1, -2	-1, -2
		Extended	-2L, -3	-2L, -3	-2L, -3	-2L, -3	-2L, -3	-2L, -3
		Industrial	-1, -2, -1L	-1, -2, -1L	-1, -2, -1L	-1, -2, -1L	-1, -2, -1L	-1, -2, -1L
	Package[3], [4]	Dimensions (mm)	**Available User I/O**: 3.3V SelectIO™ HR I/O (GTP Transceivers)					
	CPG236	10 x 10	106 (2)	106 (2)	106 (2)			
	CSG324	15 x 15	210 (0)	210 (0)	210 (0)	210 (0)	210 (0)	
	CSG325	15 x 15	150 (4)	150 (4)	150 (4)			
	FTG256	17 x 17	170 (0)	170 (0)	170 (0)	170 (0)	170 (0)	
	SBG484 / SBV484	19 x 19						285 (4)
Footprint Compatible	FGG484	23 x 23	250 (4)	250 (4)	250 (4)	285 (4)	285 (4)	
	FBG484 / FBV484	23 x 23						285 (4)
Footprint Compatible	FGG676	27 x 27				300 (8)	300 (8)	
	FBG676 / FBV676	27 x 27						400 (8)
	FFG1156 / FFV1156	35 x 35						500 (16)

XMP086 (v4.7)

CPG: 0.5 mm Wire-bond chip-scale; **CSG**: 0.8 mm Wire-bond chip-scale; **FTG**: 1.0 mm Wire-bond fine-pitch; **SBG / SBV**: 0.8 mm Lidless flip-chip; **FGG**: 1.0 mm Wire-bond fine-pitch; **FBG / FBV** 1.0 mm Lidless flip-chip; **FFG / FFV**: 1.0 mm Flip-chip fine-pitch

Notes:
1. Supports PCI Express Base 2.1 specification at Gen1 and Gen2 data rates.
2. Represents the maximum number of transceivers available. Note that the majority of devices are available without transceivers. See the Package section of this table for details.
3. Leaded package option available for all packages. See DS180, *7 Series FPGAs Overview* for details.
4. Device migration is available within the Artix-7 family for like packages but is not supported between other 7 series families.