



# Freescal Technology Forum

Collaboration. Innovation. Inspiration.

July 2009

## DDR3 Design Considerations for PCB Applications

AN111

Jon Burnett



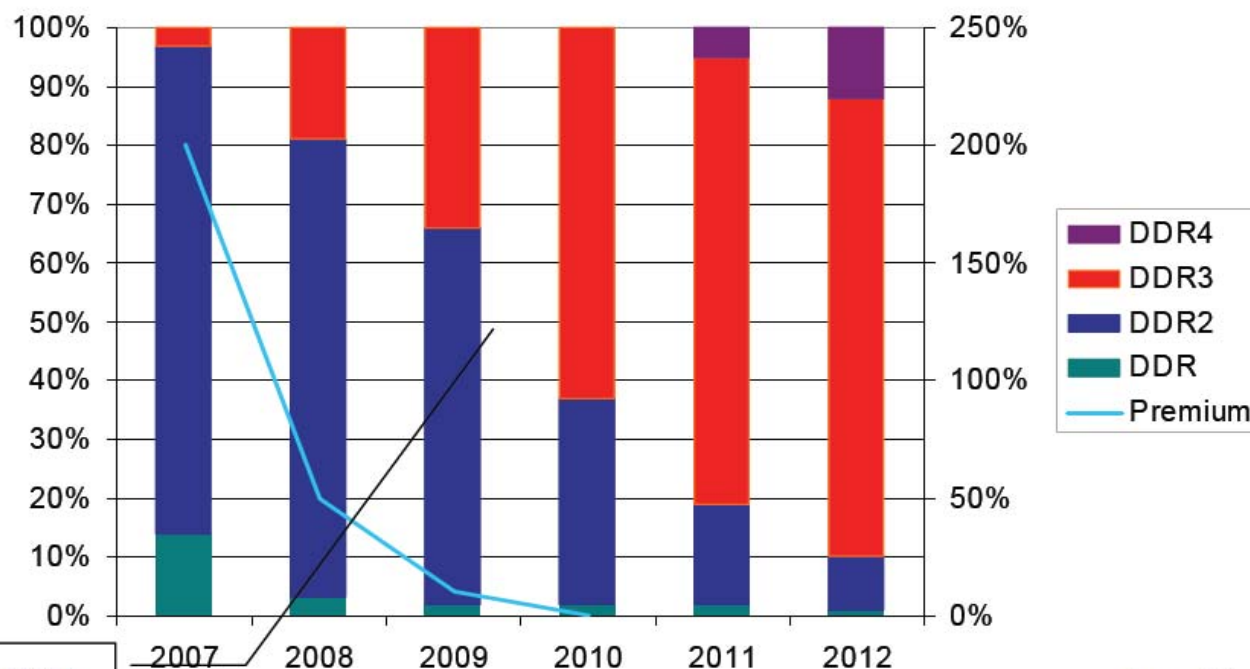
- ▶ Customers are beginning to inquire and / or expect DDR3 support on their new product offerings, especially as the price cross-over point nears.
- ▶ The first device with DDR3 support was 8572.
- ▶ The first development system with DDR3 will be P2020.
- ▶ As such, more and more FSL products are supporting DDR3 moving forward.
- ▶ In this session we will look at key distinctions between DDR3 vs. DDR1 & DDR2, with key emphasis placed on elements that are important to hardware / board design engineers.

- ▶ DDR3 SDRAM Attributes.
- ▶ DDR Controller Highlights.
- ▶ DDR3 Signaling.
- ▶ DDR3 Routing Methodology.
- ▶ Memory Pins, New Features.
- ▶ PCB Design Pitfalls.

- ▶ Supported by all major memory vendors



# Cross-over Point



Source: Micron Marketing

DDR2 to DDR3 Crossover

	2007	2008	2009	2010
DDR	14%	3%	2%	1%
DDR2	83%	78%	64%	33%
DDR3	3%	19%	34%	60%

# DDR SDRAM Highlights and Comparison

Feature/Category	DDR1	DDR2	DDR3
Package	TSOP	BGA only	BGA only
Densities	128Mb -1Gb	256Mb - 4Gb	512Mb -8Gb
Voltage	2.5V Core 2.5V I/O	1.8V Core 1.8V I/O	1.5V Core 1.5V I/O
I/O Signaling	SSTL_2	SSTL_18	SSTL_15
Internal Memory Banks	4	4 to 8	8
Data Rate	200-400 Mbps	400–800 Mbps	800–1600 Mbps
Termination	Motherboard termination to $V_{TT}$ for all signals	On-die termination for data group. $V_{TT}$ termination for address, command, and control	On-die termination for data group. $V_{TT}$ termination for address, command, and control
Data Strokes	Single Ended	Differential or single	Differential

# DDR SDRAM Highlights and Comparison (cont.)

Feature/Category	DDR1	DDR2	DDR3
Burst Length	BL= 2, 4, 8 (2-bit prefetch)	BL= 4, 8 (4-bit prefetch)	BL= 8 (Burst chop 4) (8-bit prefetch)
CL/tRCD/tRP	15 ns each	15 ns each	12 ns each
Master Reset	No	No	Yes
ODT (On-die termination)	No	Yes	Yes
Driver Calibration	No	Off-Chip (OCD)	On-Chip with ZQ pin (ZQ cal)
Write Leveling	No	No	Yes

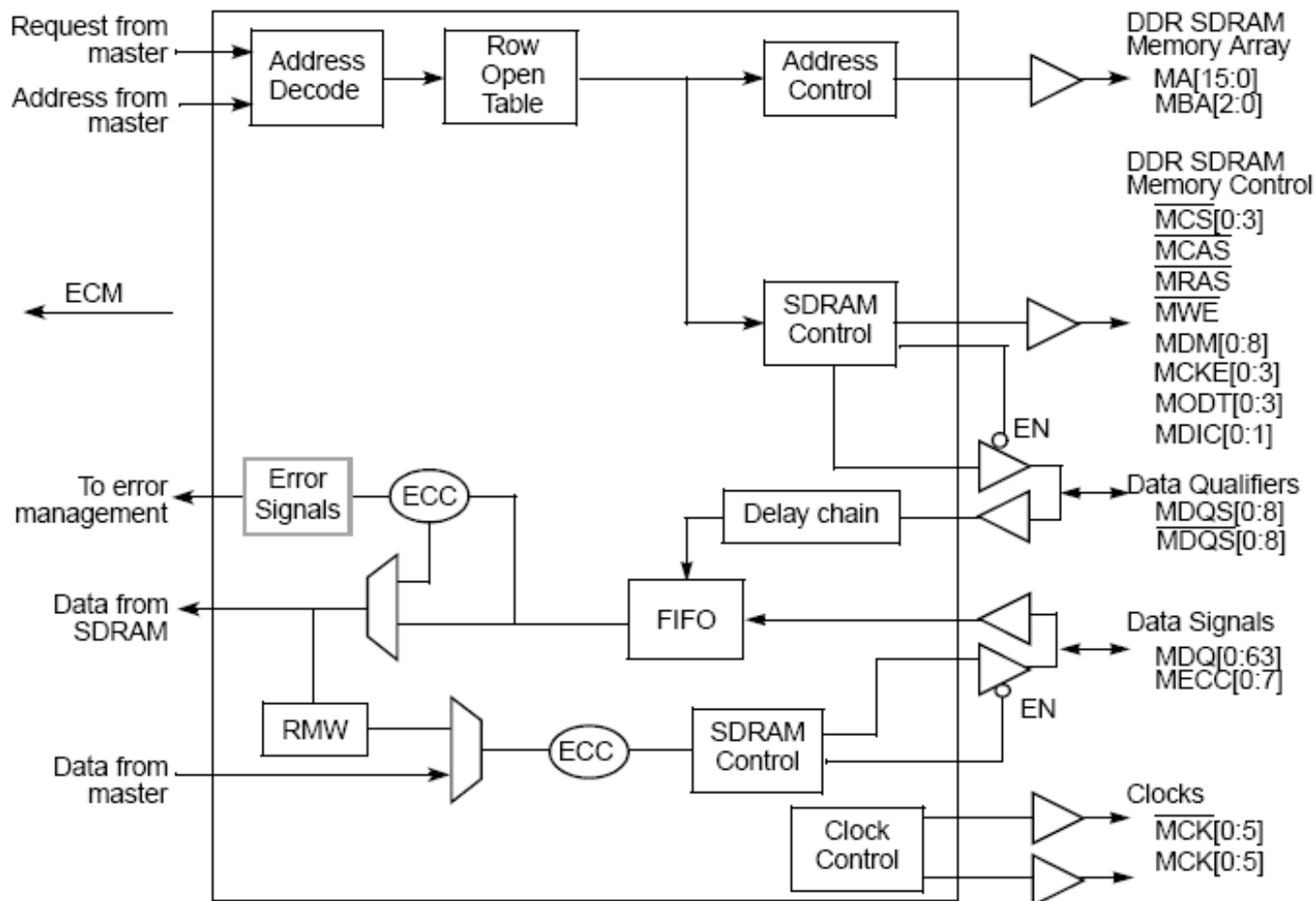
# Typical Freescale DDR2/3 Controller Highlights

- ▶ **Interface speed**
  - DDR2 - up to 800 MHz
  - DDR3 - up to 800 MHz today (MPC8572, MPC8526)
    - Evaluating higher speeds 1066 MHz and up to 1600 MHz
- ▶ **Support Interface width**
  - 64/72-bit data bus – high end product
  - 32/40-bit data bus – low end products
  - 16/24-bit data bus – low end products
- ▶ **Discrete, unbuffered, and registered DIMM support**
  - Memory device densities from 64Mb – through 8Gb
  - Up to four chip selects supported
  - Support for x8/x16 DDR devices – x4 devices are not supported
- ▶ **Full ECC (Error Correction Code) support**
  - Single error correction/detection, double error detection
  - Error injection for software development
- ▶ **Self refresh support**



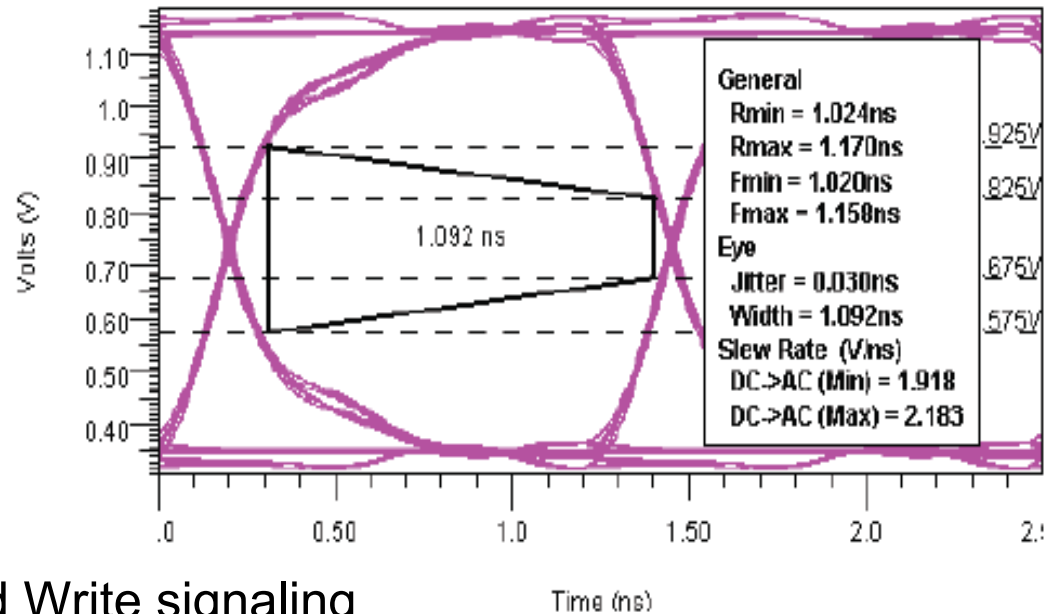
- ▶ Read-Modify-Write support for Atomic Inc, Dec, Set, Clear, and sub-double word writes
- ▶ All timing parameters are under SW control
- ▶ Automatic Data Initialization (easy ECC support)
- ▶ Differential data strobes
- ▶ Dedicated Open Row Table for each sub-bank
  - Up to 32 simultaneous open rows with 4 chip selects
- ▶ Up to six diff clock pairs
  - Eliminates the need for any external clock PLLs
- ▶ ODT support (both internally and externally)
- ▶ On-chip ZQ driver calibration
- ▶ SSTL-1.8, and SSTL-1.5 compatible IOs

# Memory Controller Block Diagram

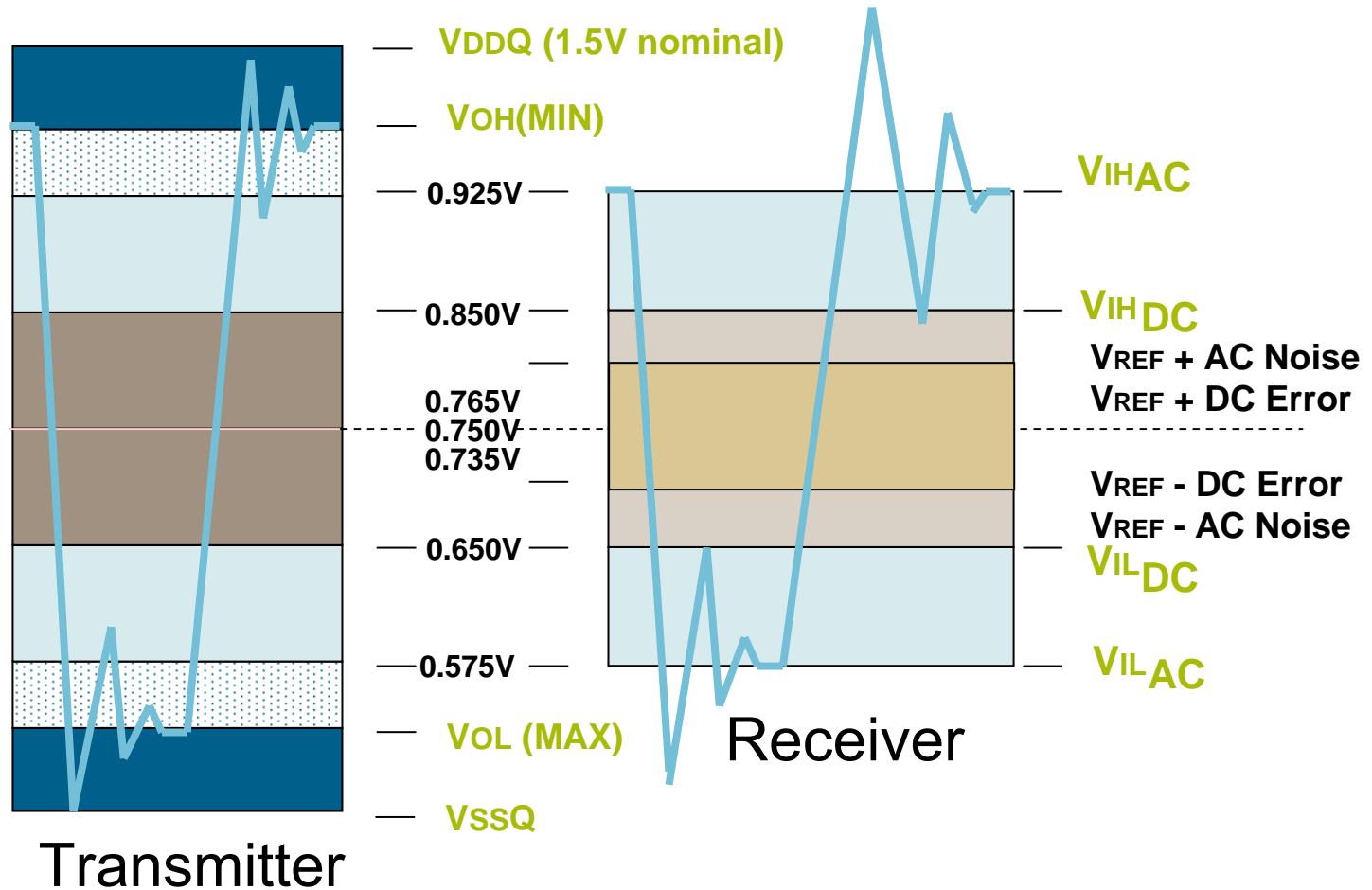


# Key DDR3 Memory Improvements and Additions

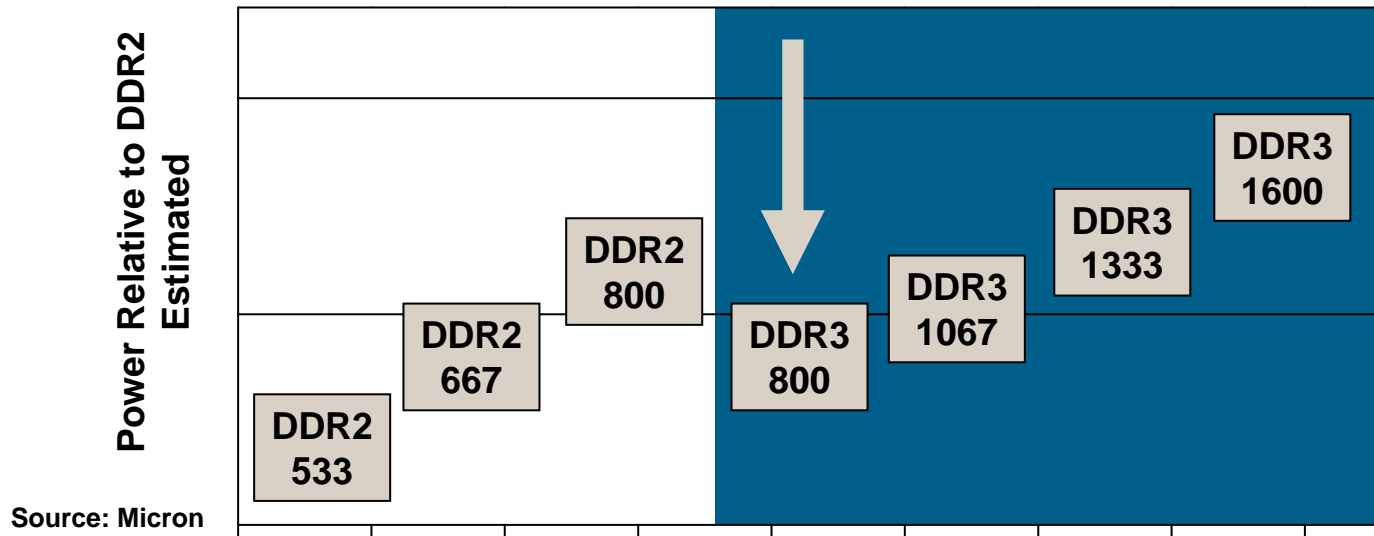
- ▶ Lower signaling standard
- ▶ Reduced power
- ▶ Improved device pinout
- ▶ Fly-by architecture
- ▶ Write Leveling
- ▶ Dynamic ODT for improved Write signaling
- ▶ Driver calibration
- ▶ Device Reset
- ▶ DIMM address mirroring



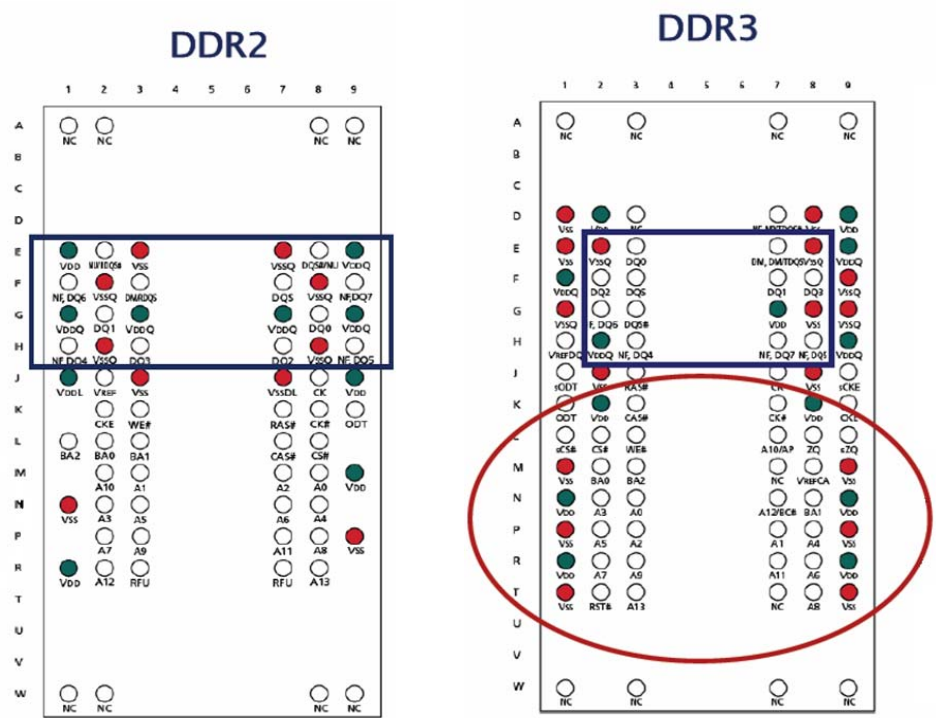
# DDR3 Signaling – Example SSTL-1.5



- ▶ Supply voltage reduced from 1.8V to 1.5V
  - ~ 30% power reduction (Micron claim)
  - ~ 25% is JEDEC's official claim
    - Compared to DDR2 at same frequency bin
- ▶ Lower I/O buffer power
  - 34 ohm driver vs. 18 ohm driver at memory device
- ▶ Improved bandwidth per Watt

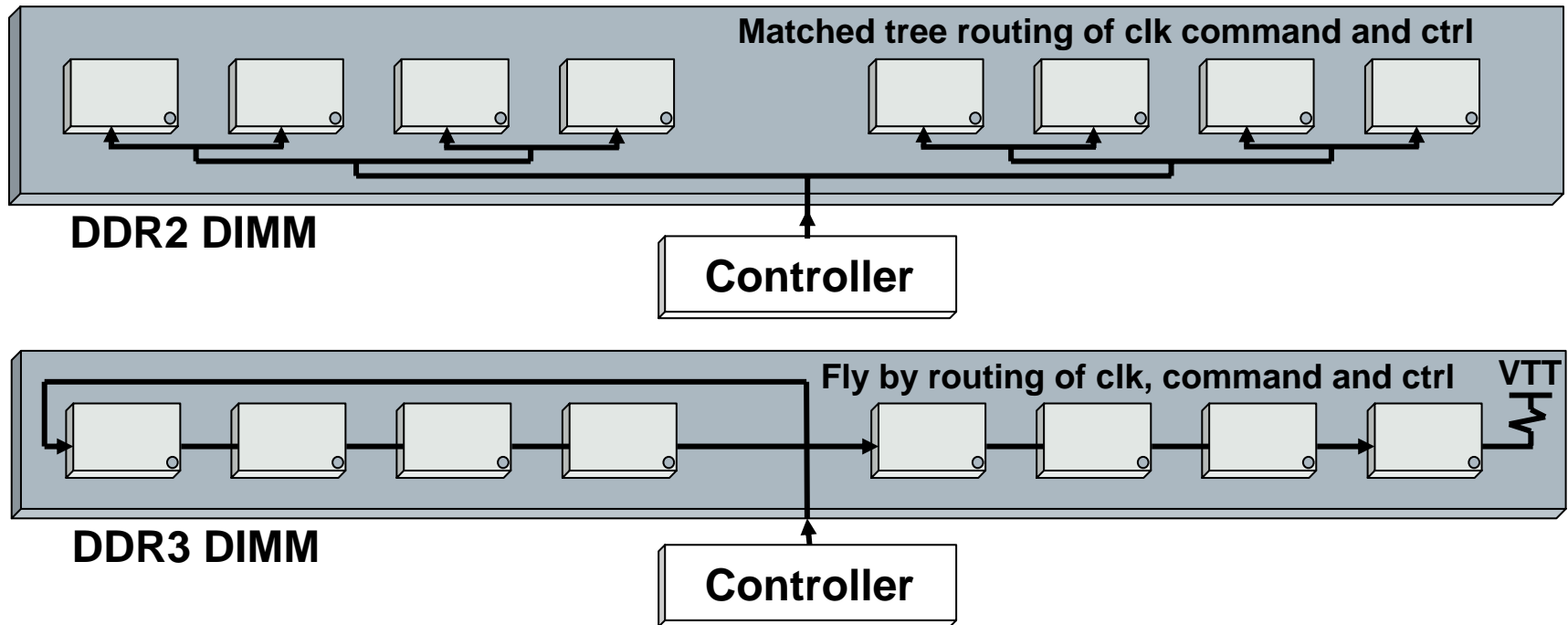


- ▶ Improved power delivery
  - More power and ground balls
- ▶ Improved signal quality
  - Better power & ground distribution
  - And better signal referencing
- ▶ Fully populated ball grid
  - Stronger reliability
- ▶ Improved pin placement
  - Less pin skew
  - Tighter timing leaving chip

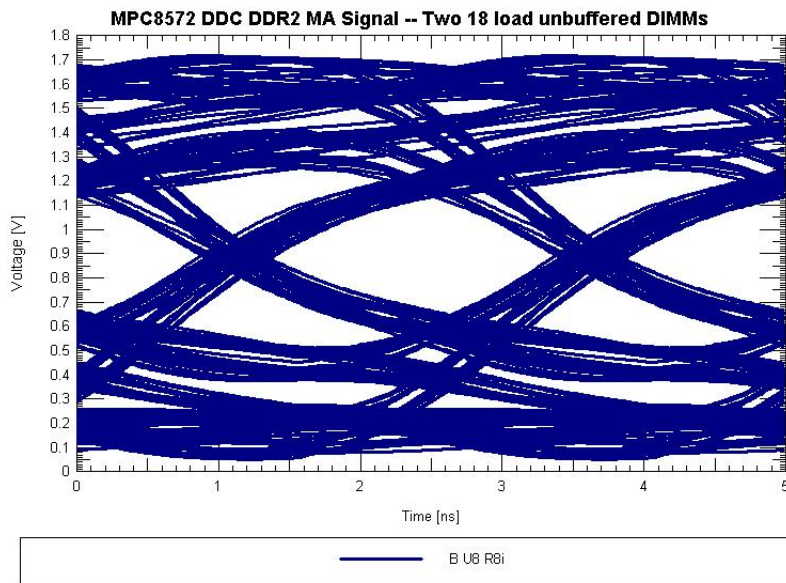


## ► Introduction of “Fly-by” architecture

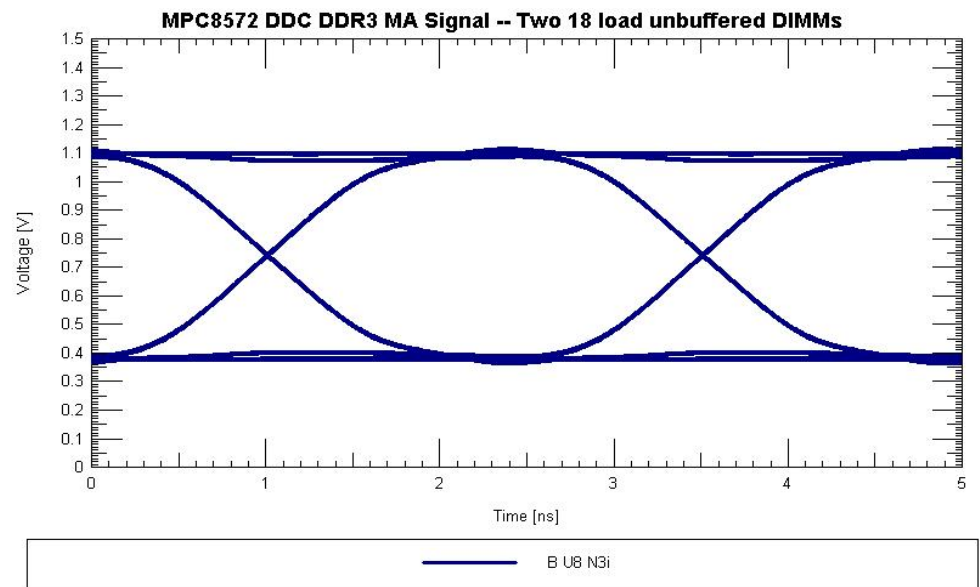
- Address, command, control & clocks
- Improved signal integrity...enabling higher speeds
- On module termination



## DDR2 Matched tree routing

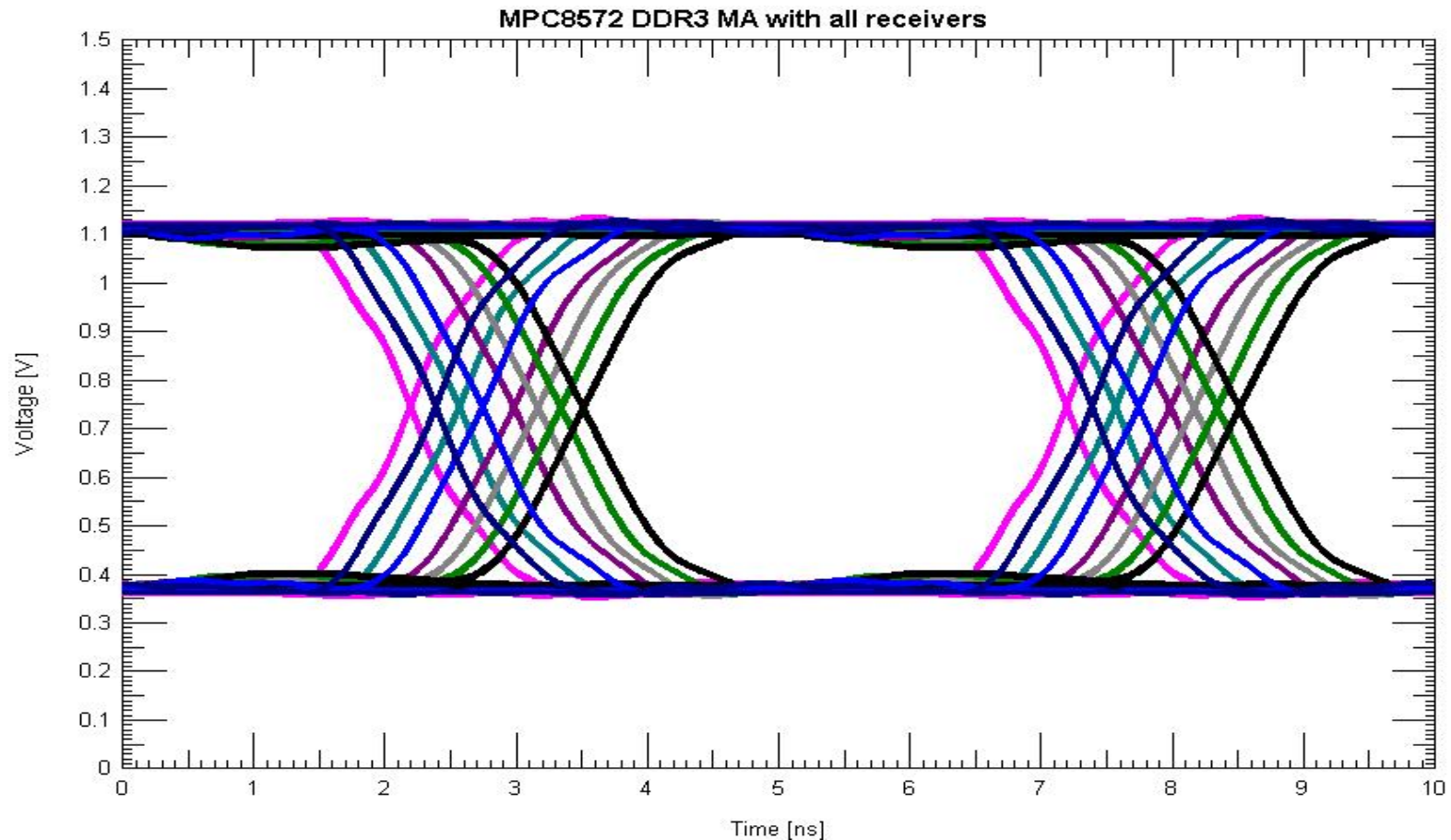


## DDR3 Fly by routing





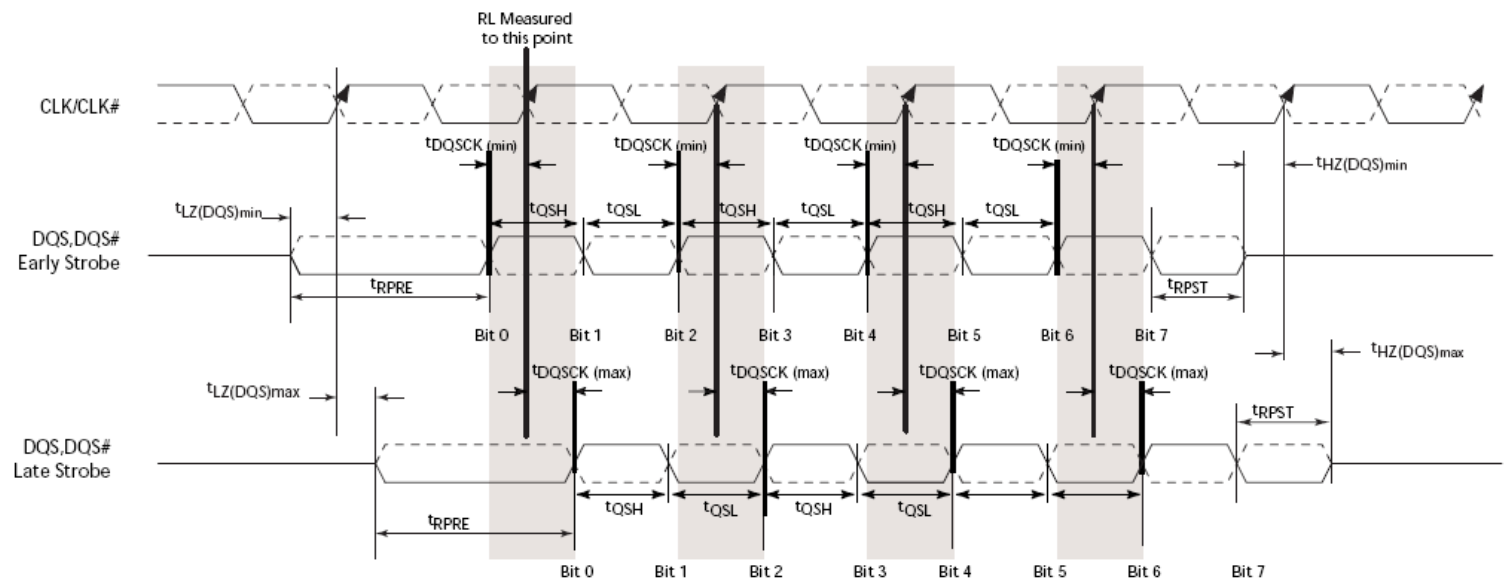
# Fly By Skew Across All receivers



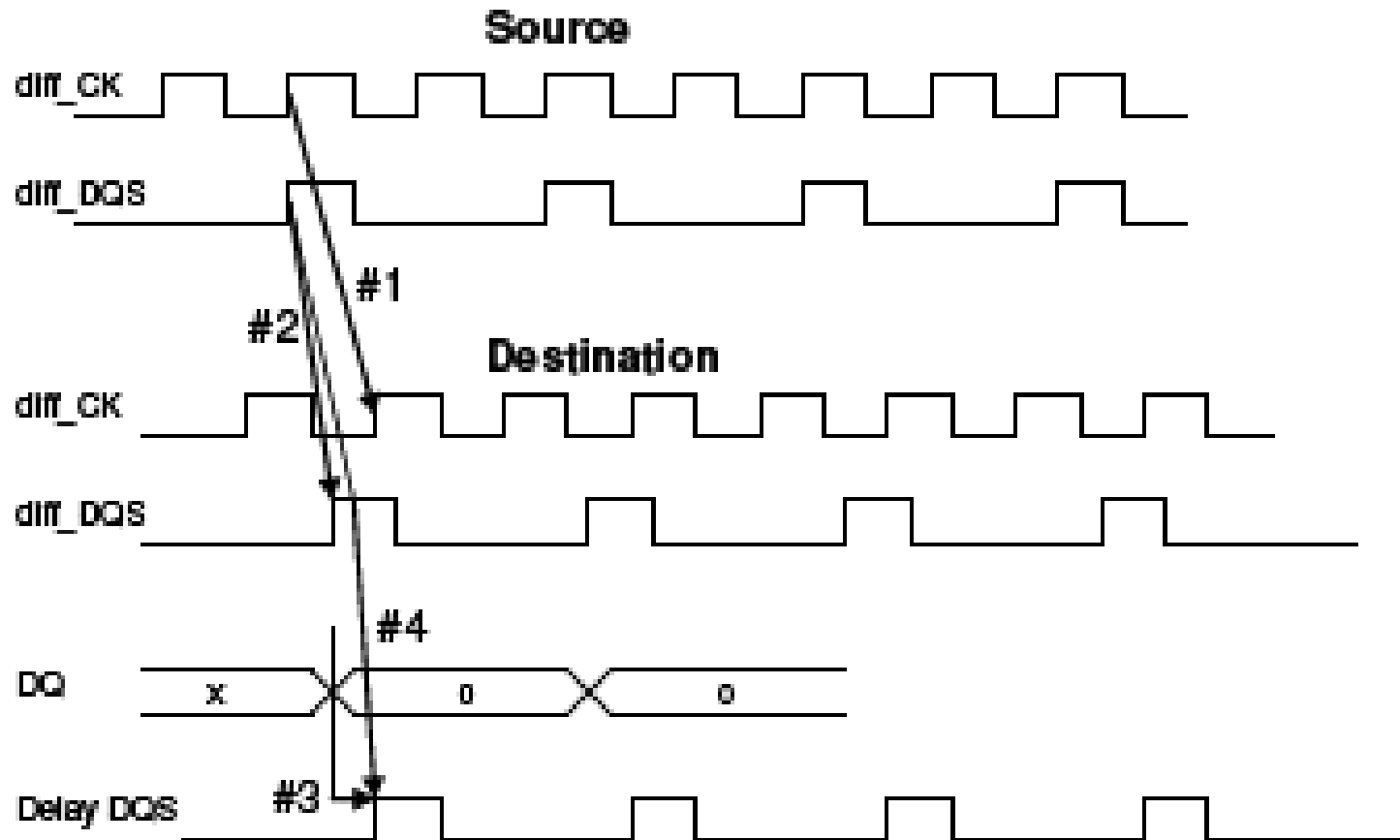
**This illustrates the skew created by DDR3 fly by routing**

# The need for write-leveling....

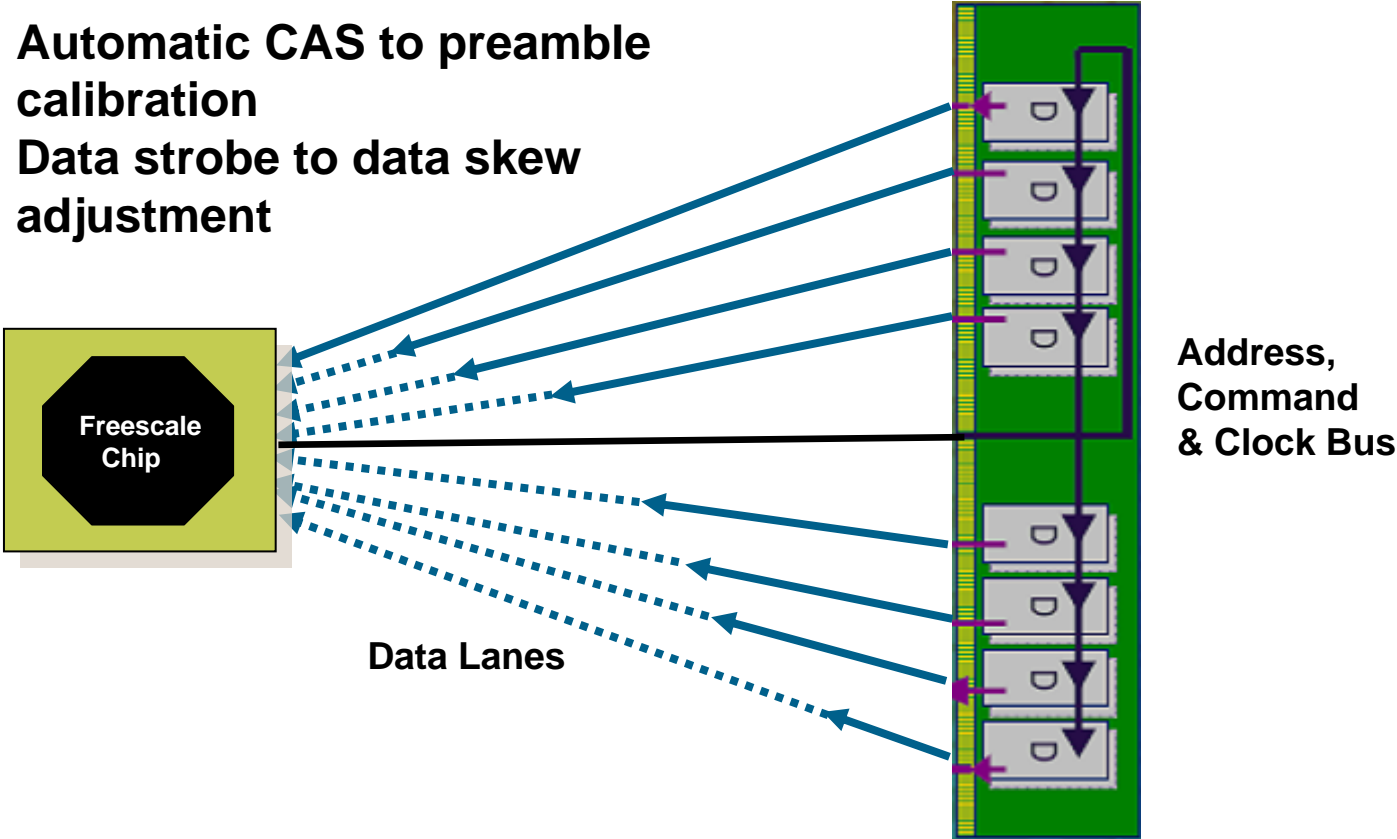
- ▶ tDQSS requirement:
  - DQS/DQS# rising edge to CK/CK# rising edge
  - Clock to Strobe should be within a certain range for proper write operation to DDR3 SDRAMs
- ▶ tDQSS spec:  $\pm 0.25 \cdot t_{ck}$



# Write-Leveling... How it works



- Automatic CAS to preamble calibration
- Data strobe to data skew adjustment



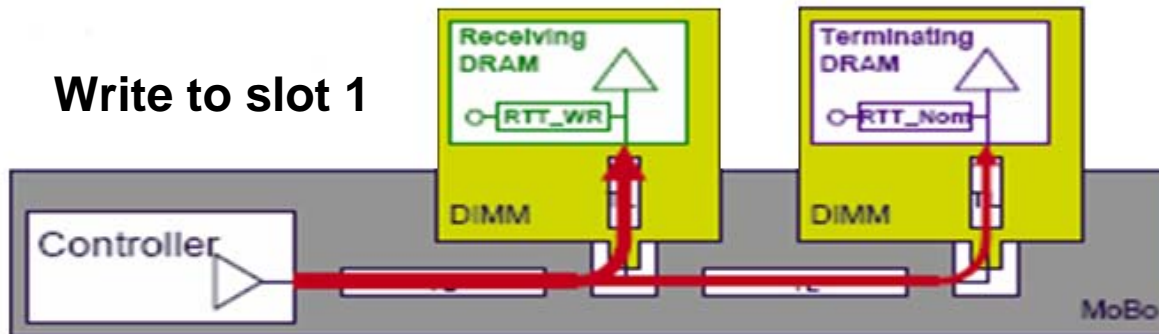
Instead of JEDEC’s MPR method, Freescale controllers use a proprietary method of read adjust method which will work with DDR2 and DDR3. This provides comparable performance to JEDEC’s DDR3 MPR method

# Dynamic ODT – System Motivation

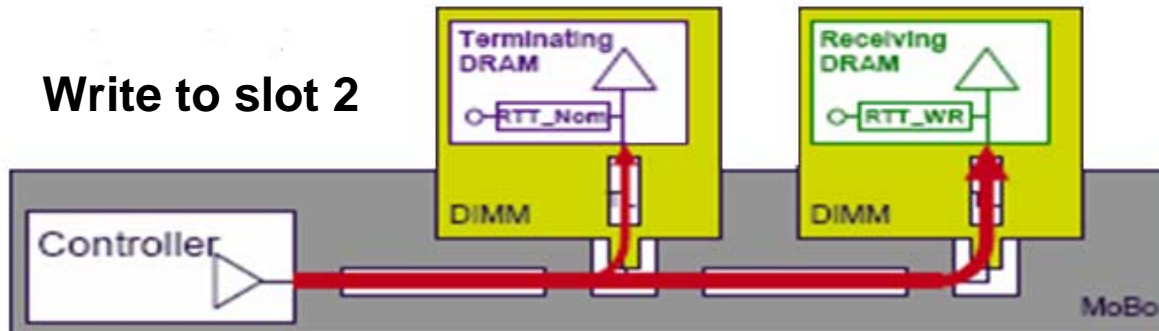
## Example of termination scheme in application

Transaction	Slot 1	Slot 2
Write to Slot 1	$RTT_{WR} = 120 \Omega$	$RTT_{Nom} = 20 \Omega$
Write to Slot 2	$RTT_{Nom} = 20 \Omega$	$RTT_{WR} = 120 \Omega$

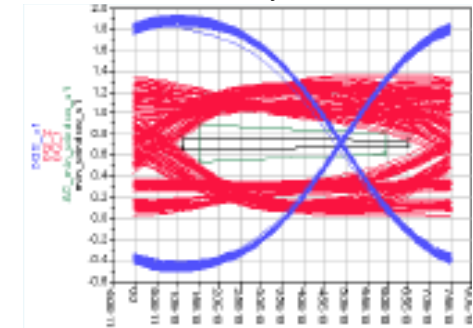
### Write to slot 1



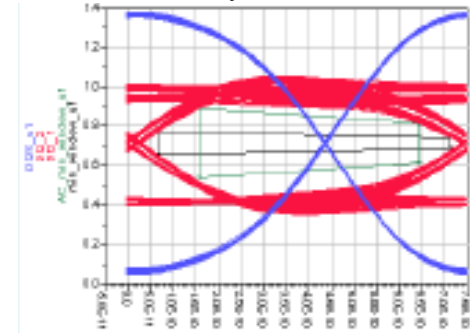
### Write to slot 2



Without Dynamic ODT



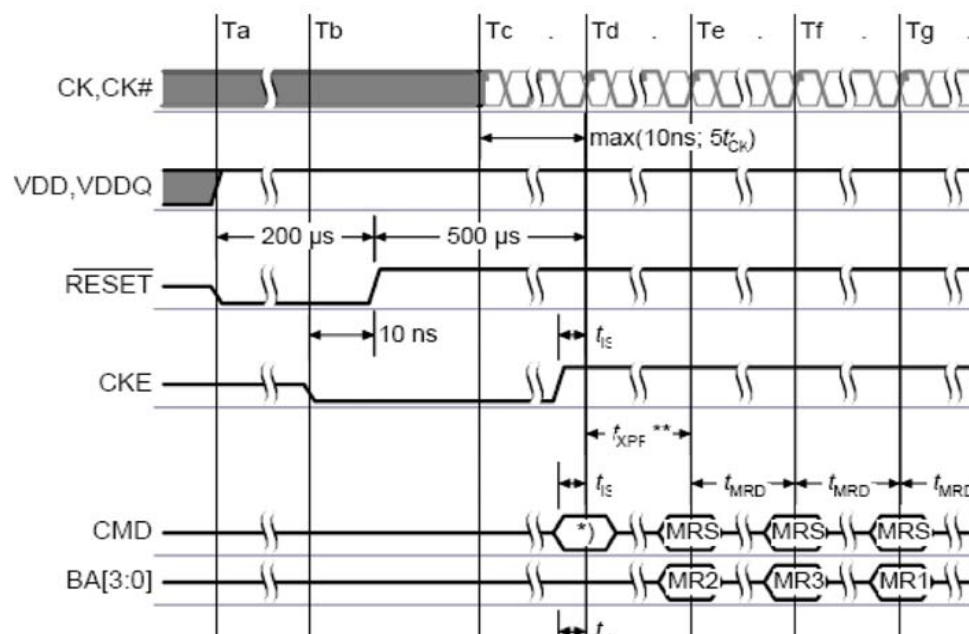
With Dynamic ODT



Significant improvement of write signal integrity with DDR3 dynamic ODT

## ► Introduction of an asynchronous RESET# pin

- Prevent Illegal commands and/or unwanted states
  - Cold reset
  - Warm reset
- Known initialization
  - Resets all state information
  - No power-down required
  - Destructive to data contents



- ▶ VREF broken into separate banks (..at the DDR3 memories)
  - VREFCA
    - Used for the command / address signals
    - Decoupled to VDD plane
  - VREFDQ
    - Used for the data signals
    - Decoupled to VDD plane
- ▶ Key premise – Noise reduction and coupling between the groups

**At the DDR3 controller the same source driving VREFDQ to the memories would drive the controller VREF pin.**

# NEW DDR3 pins – ZQ Calibration Pin

- ▶ The RZQ resistor is connected between the DDR3 memory and ground
  - Value = 240 Ohm +/- 1%
  - Permits driver and ODT calibration over process, voltage, and temperatures
- ▶ Easier and more accepted than DDR2's (optional) OCD method.
- ▶ Our controllers support both ZQ calibration commands
  - ZQCL – used during initialization (..takes longer)
  - ZQCS – used during normal operation (...periodic and takes less time)

**Table 9-26. DDR\_ZQ\_CNTL Field Descriptions**

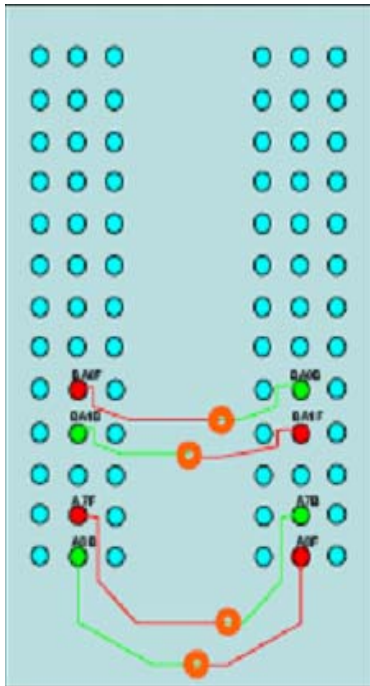
Bits	Name	Description
0	ZQ_EN	<p>ZQ Calibration Enable. This bit determines if ZQ calibrating will be used. This bit should only be set if DDR3 memory is used (DDR_SDRAM_CFG[SDRAM_TYPE] = 3'b111).</p> <p>0 ZQ Calibration will not be used.</p> <p>1 ZQ Calibration will be used. A ZQCL command will be issued by the DDR controller after POR and anytime the DDR controller is exiting self refresh. A ZQCS command will be issued every 32 refresh sequences to account for VT variations.</p>



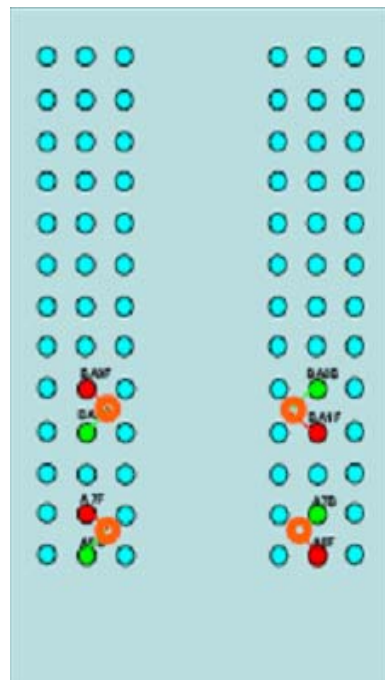
# Freescal Controller Driver Calibration

- ▶ Our Freescale controller also does driver calibration
  - Enabled by software
  - Occurs automatically during initialization after MEM\_EN is set
  
- ▶ MDIC precision resistors are used at our controller
  - Value = 40 Ohms 1% tolerance

- The DDR3 IP fully supports address mirroring



**Non-Mirrored**

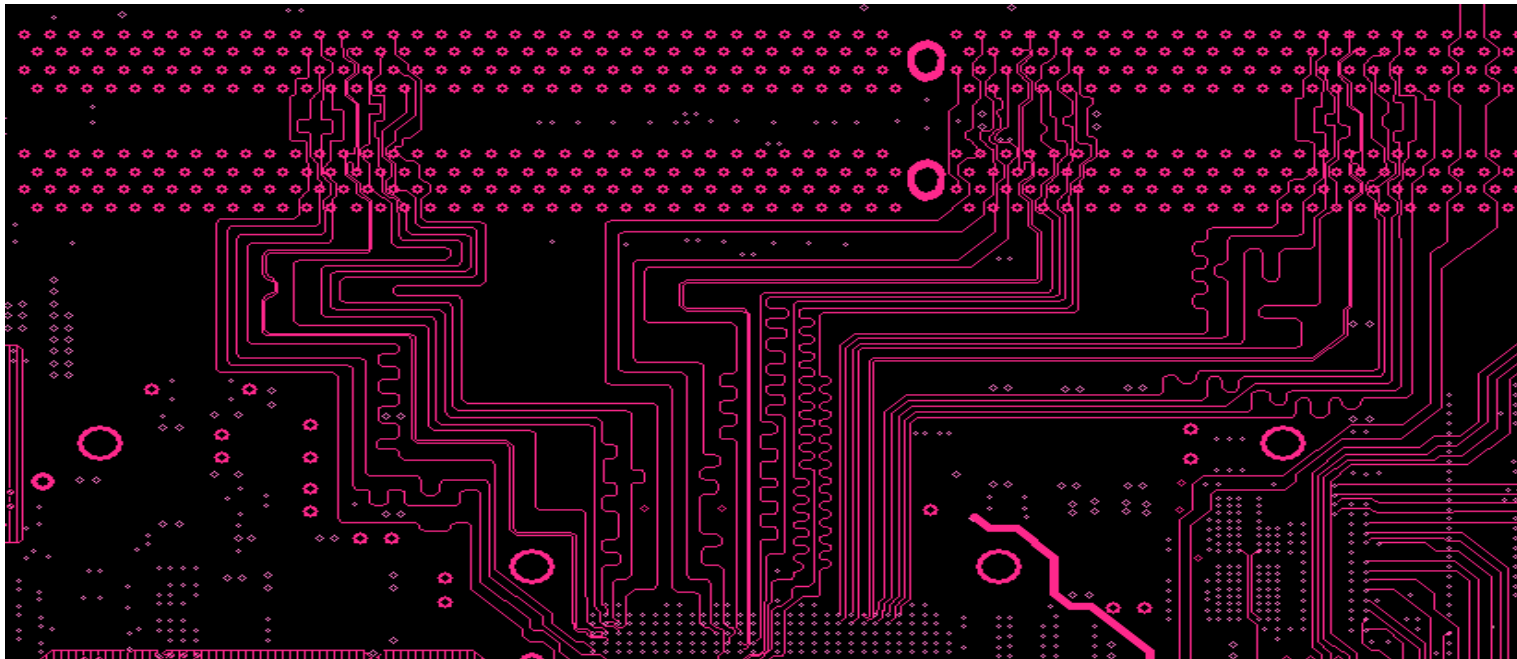


**Mirrored**

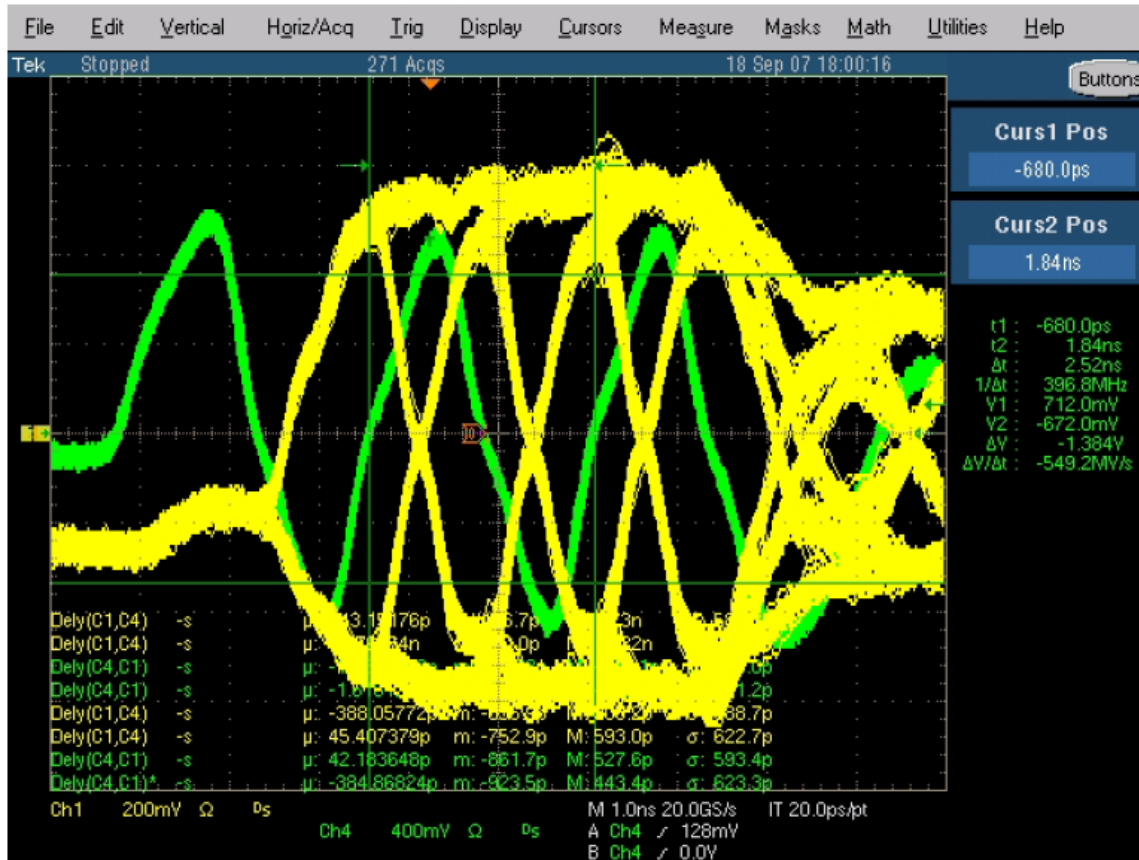
Edge Connector Signal	SDRAM Pin, Standard	SDRAM Pin, Mirrored
A0	A0	A0
A1	A1	A1
A2	A2	A2
A3	A3	A4
A4	A4	A3
A5	A5	A6
A6	A6	A5
A7	A7	A8
A8	A8	A7
A9	A9	A9
...	...	...
A15	A15	A15
BA0	BA0	BA1
BA1	BA1	BA0
BA2	BA2	BA2

- ▶ TDQS/TDQS# New pin on x8 DDR3 devices
  - Not present on x4 or x16 devices
  - Allows combinations of x4/x8 devices in the same system.
  
- ▶ We don't support TDQS/TDQS#
  - We do not support x4 devices... so this function is not supported

## ► Byte lane routing example



## 120 Ohm / Half Driver / 1 DIMM



Good margins across  
all data beats

Required  
Tsu = 95 ps  
Th = 170 ps

Measured Setup (Average)	646 ps	443 ps	440 ps	452 ps
Measured Hold (Average)	427 ps	405 ps	432 ps	850 ps

# Common Design Pitfalls

- ▶ Pitfall 1 Noisy Vref: Care must be taken to isolate Vref
- ▶ Pitfall 2 Weak Vref: Insure adequate current for Vref
- ▶ Pitfall 3 Ref Plane: Insure excellent reference plane for all DDR signals
- ▶ Pitfall 4 Data Tuning: Data bits within 10 mil, Byte lanes within 0.5"
- ▶ Pitfall 5 Proper Termination: Discrete implementations require term.
- ▶ Pitfall 6 POR Config: Insure correct DDR (2/3) is set for controller
- ▶ Pitfall 7 Expandability: Hook up unused address lines
- ▶ Pitfall 8 Incorrect Topology: Insure use of JEDEC routing topologies
- ▶ Pitfall 9 Separate VDDQ/VDDIO : VDDQ and VDDIO are common on DDR DIMM Modules, not on controller.

# Design Pitfalls Summary (Continued)

- ▶ Pitfall 10 Slew Rate: Must account for de-rated slew rate for system timing (See JEDEC Table)
- ▶ Pitfall 11 Testability: Insure there is test and measurement access to DDR signals
- ▶ Some other noteworthy pitfalls
  - Not using ECC
    - Highly Recommended for first prototypes. De-pop for production
  - Missing pull-up on MAPAR\_ERR (registered DIMMs) and MAPAR\_OUT



# Design Pitfalls

## Backup Slides

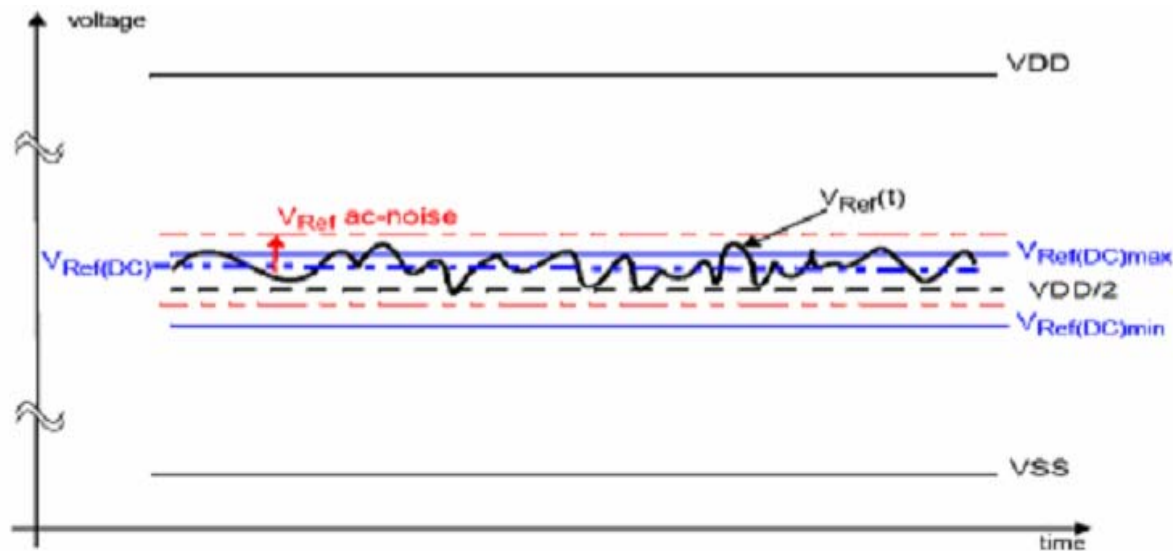
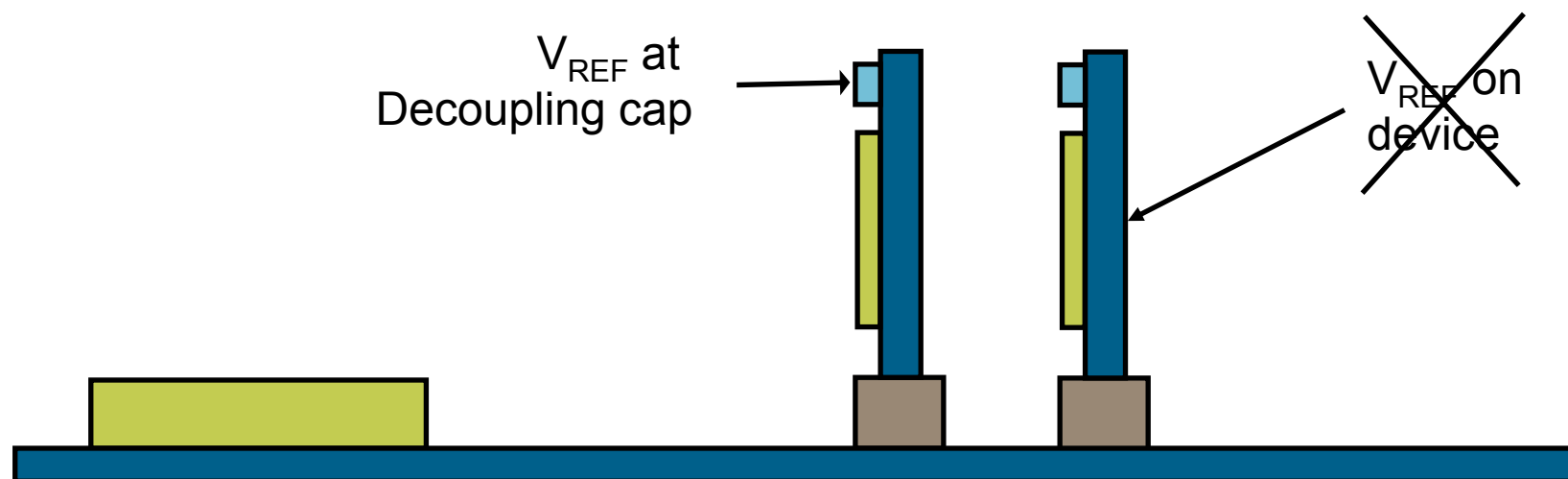


Figure 80 — Illustration of  $V_{Ref(DC)}$  tolerance and  $V_{Ref}$  ac-noise limits

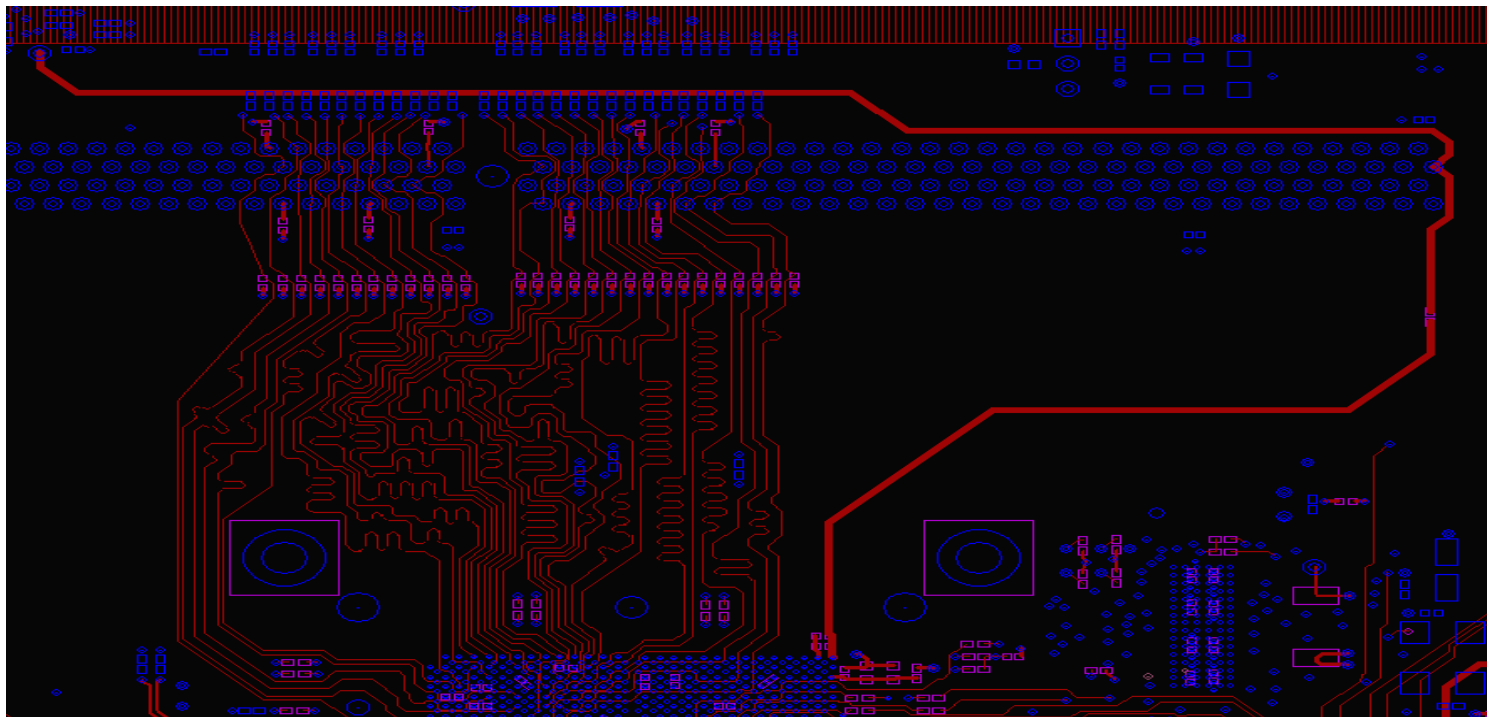
- $V_{Ref}(t)$  may temporarily deviate from  $V_{Ref}(DC)$  by no more than  $\pm 1\% VDD$
- $V_{Ref}(DC)$  is the linear average of  $V_{Ref}(t)$  over a very long period of time (e.g. 1 sec)

- ▶ **Measuring at device will likely give greater than 50 mV peak-to-peak**
  - Result of coupled noise from DDR device
- ▶  **$V_{REF}$  system noise should be measured at capacitor nearest the memory device**



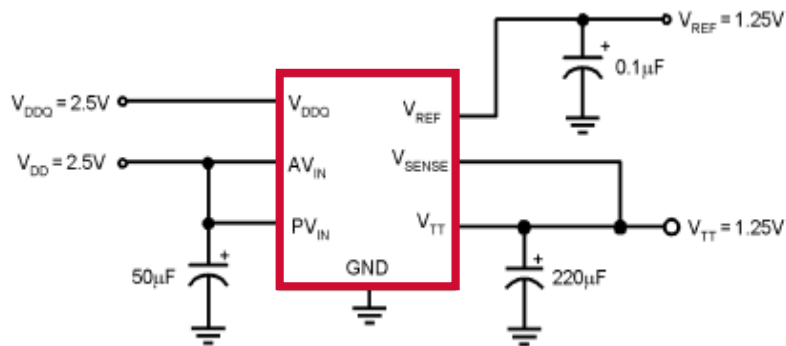
# Pitfall 1 – Protecting VREF

$V_{REF}$		
18.	Has $V_{REF}$ been routed with a wide trace? (Minimum of 20–25 mil recommended.)	
19.	Has $V_{REF}$ been isolated from noisy aggressors? In addition, maintain at least a 20–25 mil clearance from $V_{REF}$ to other traces. If possible, isolate $V_{REF}$ with adjacent ground traces.	
20.	Has $V_{REF}$ been proper decoupled? Specifically, decouple the source and each destination pin with 0.1uF caps.	



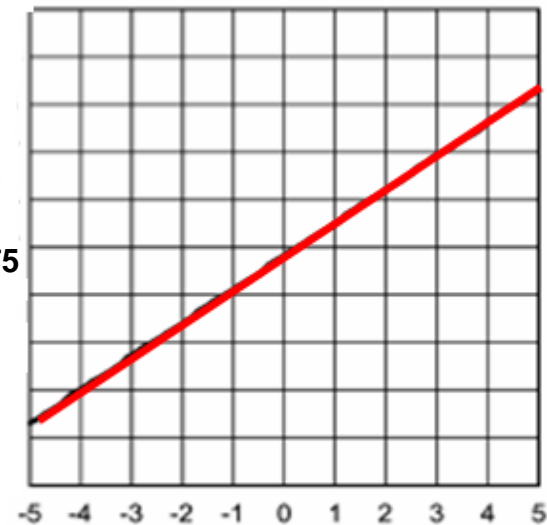
## Pitfall 2 – Wimpy $V_{REF}$ source

- ▶  $V_{REF}$  current consumption is typically 1.5-2.0 mA
- ▶ For most DDR regulators.... this is easily handled



$V_{REF}$  vs.  $I_{REF}$

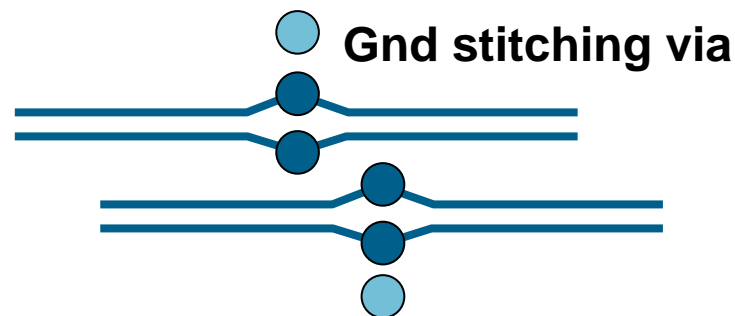
$V_{REF}$  (V)



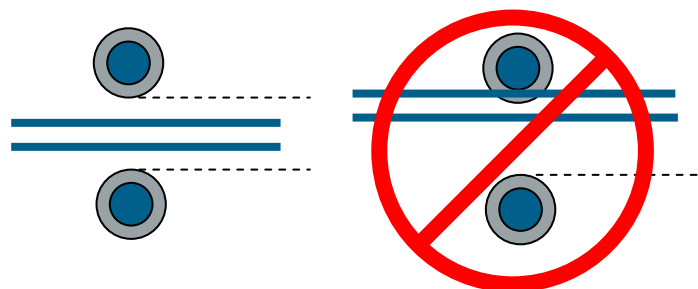
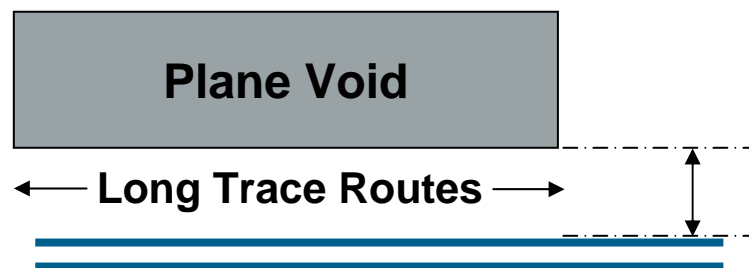
$I_{REF}$  (uA)

# Pitfall 3 – Reference Plane discontinuities

- ▶ Contiguous reference plane
  - GND – Data
  - Pwr - Address / Cmd
- ▶ Use stitching vias if switching layers

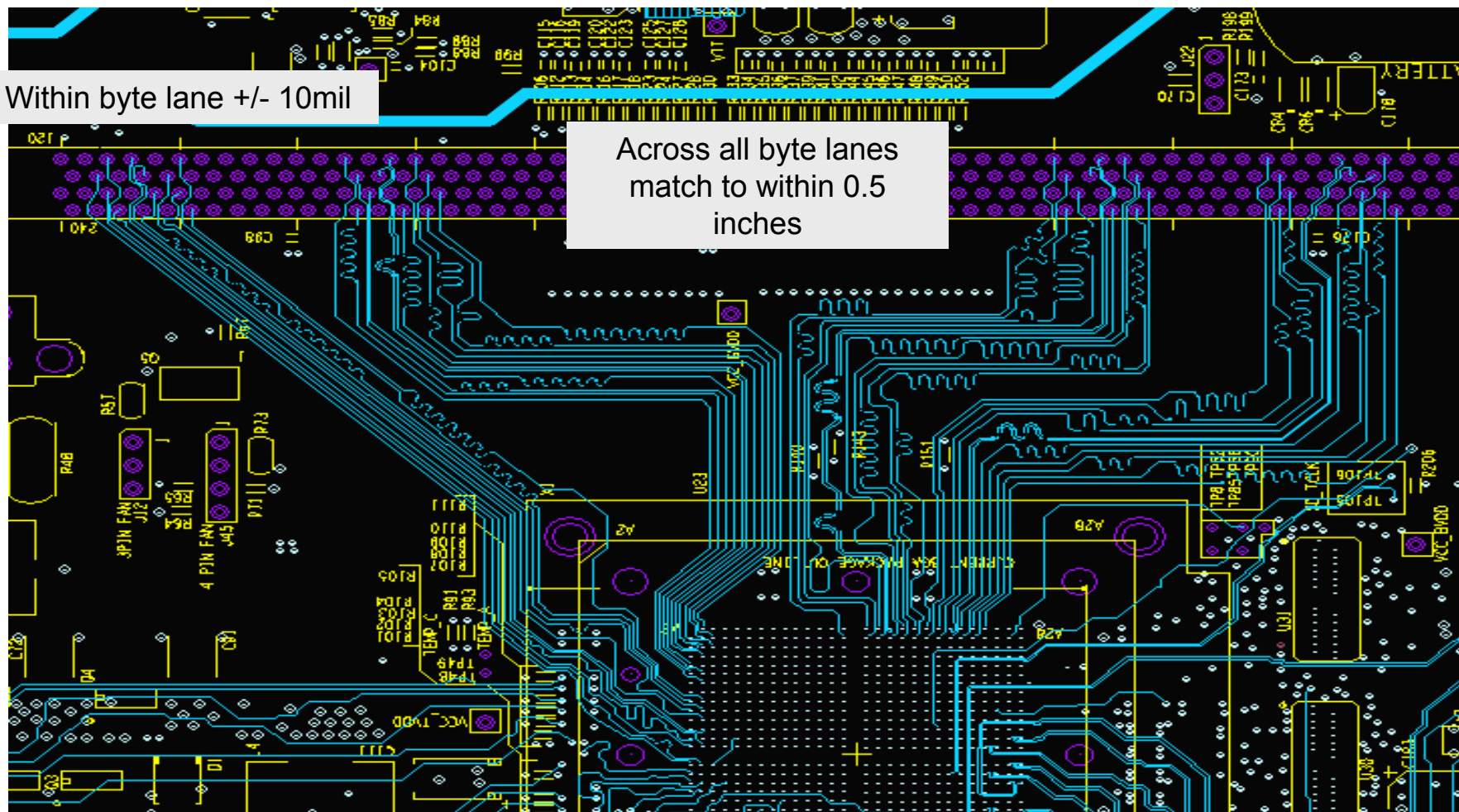


- ▶ Keep away from plane voids
- ▶ Avoid crossing plane splits
- ▶ Avoid trace over anti-pad



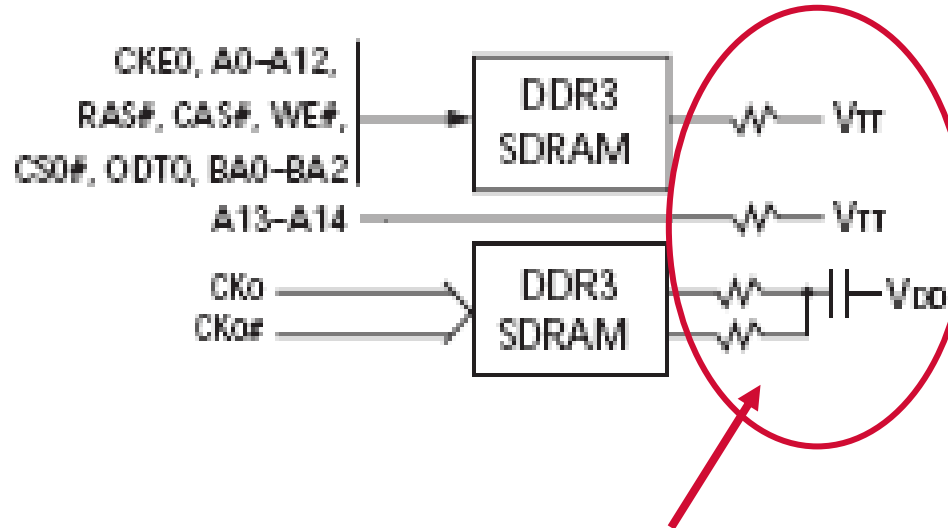
Within byte lane +/- 10mil

Across all byte lanes  
match to within 0.5  
inches



# Pitfall 5 – Forgetting Termination

Command, address, control, and clock line terminations



**Still needed for soldered-down implementations.**

**DIMM modules have the termination on the module.**



# Pitfall 6 – POR config selection

Table 4-18. DDR DRAM Type

Functional Signal	Reset Configuration Name	Value (Binary)	Meaning
TSEC2_TXD[1]  Default (1)	cfg_dram_type	0	DDR2 1.8V, CKE low at reset
		1	DDR3 1.5V, CKE low at reset (default)

**Above example assumes 8572. Other devices may utilize a different functional pin for the POR setting**

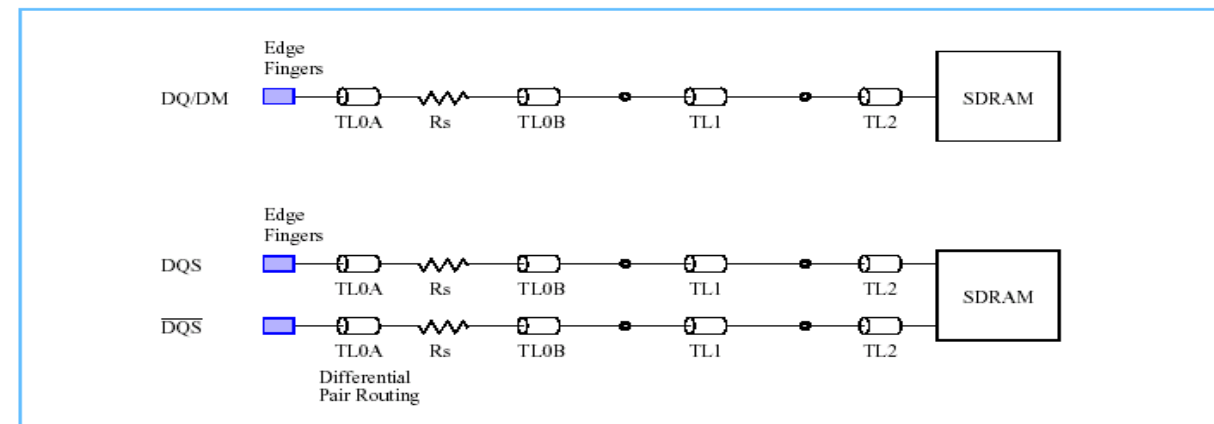
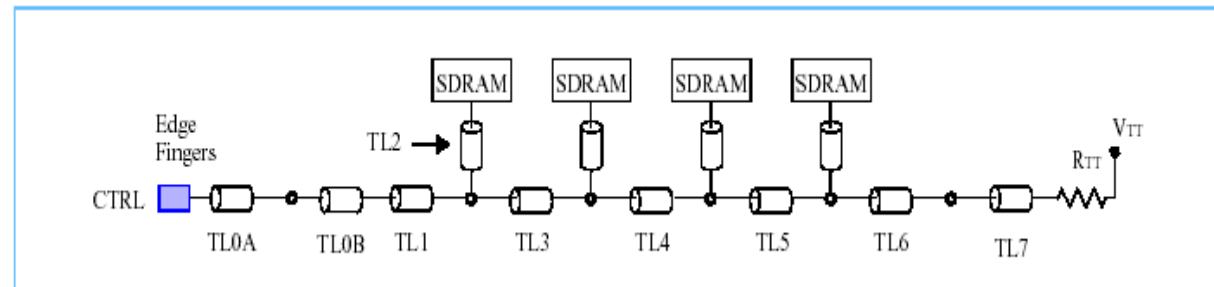
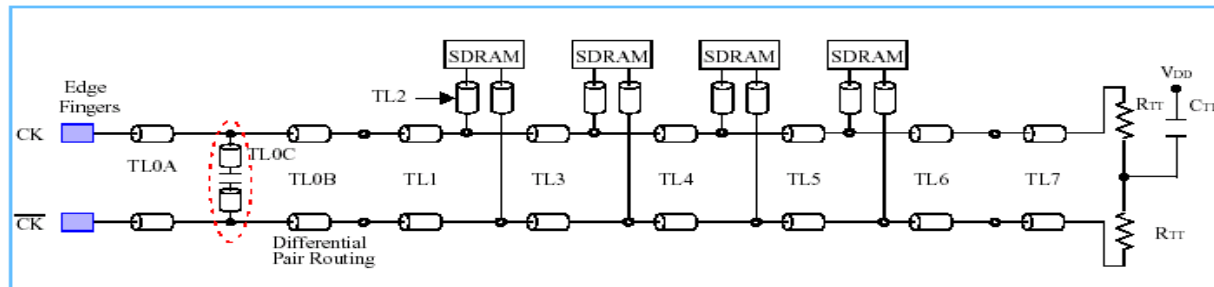
## Pitfall 7 – Expandability

Signal Name	Pin Nomenclature	Signal Type	Function
A13	NC	No connection to internal die. Okay to run trace to PCB pad.	Used on x4/x8 512 Mb and 1 Gb devices and all configurations of the 2 Gb or 4Gb.
A14	NC	No connection to internal die. Okay to run trace to PCB pad.	Used on x4/x8 2 Gb devices and all 4 Gb configurations.
A15	NC	No connection to internal die. Okay to run trace to PCB pad.	Used on 4 Gb (x4/x8).
BA2	NC	No connection to internal die. Okay to run trace to PCB pad.	Used on all configurations of the 1 Gb, 2 Gb, and 4 Gb.

### Rule of thumb:

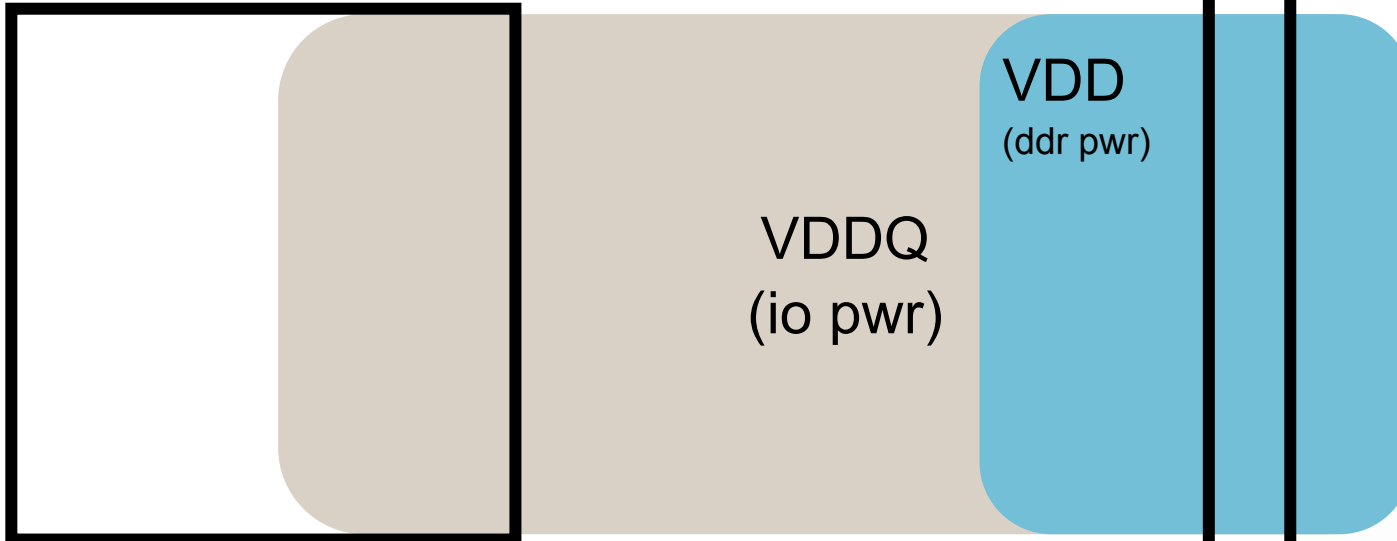
For DDR3 - Every address (A0-A15), and all three bank address (BA0-BA2) line from our controllers should be connected to the memory subsystem.

# Pitfall 8 – Not using proven JEDEC topologies



# Pitfall 9 – Separate VDDQ/VDDIO

PowerQUICC®  
Controller



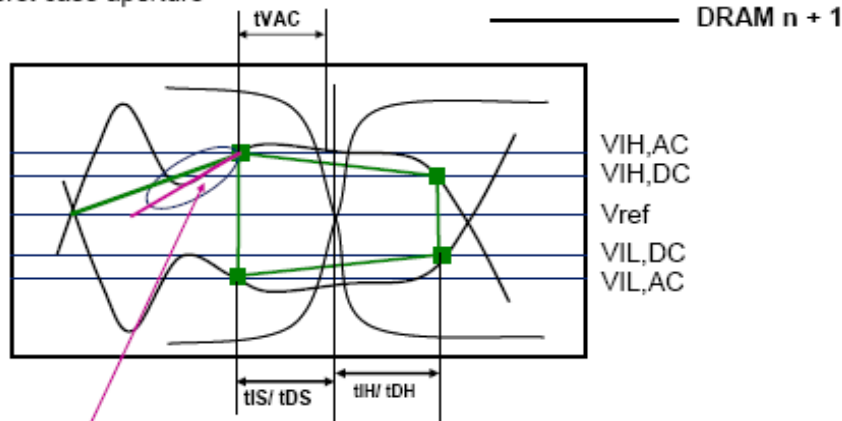
Separate planes are not  
viable with standard  
JEDEC DIMM memory  
modules



VDDQ & VDDIO are same  
plane on the modules

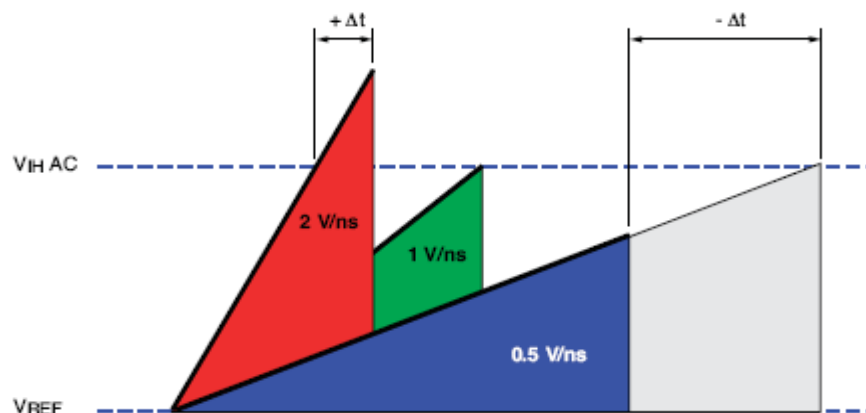
# Pitfall 10– Slew Rate De-rating (setup & hold)

Worst case aperture



**Tangent line slew rate for de-rating**

Correct valid eye time wrt to voltage margin



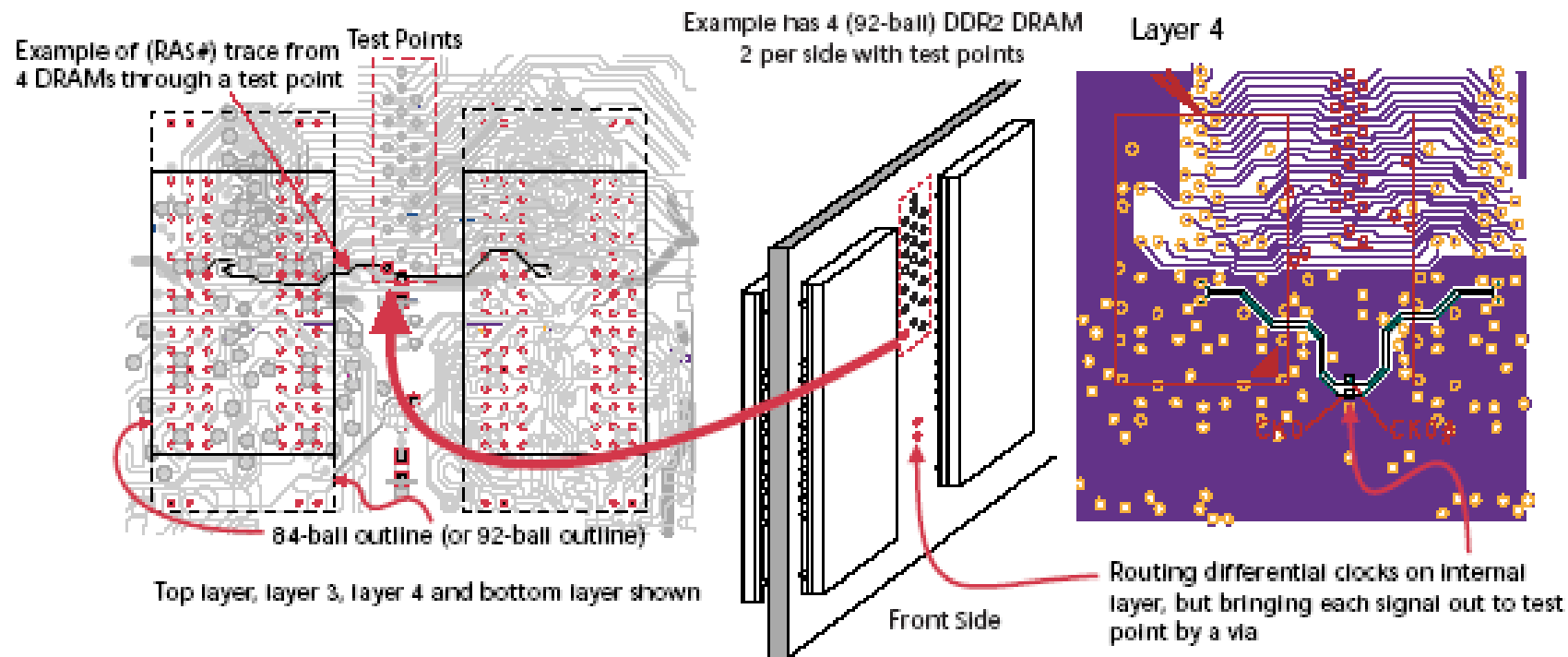
Source: Xcell Journal

Table 47 — Derating values for DDR2-667, DDR2-800

		$\Delta t_{IS}$ and $\Delta t_{IH}$ Derating Values for DDR2-667, DDR2-800						Units	Notes
		CK,CK Differential Slew Rate							
		2.0 V/ns		1.5 V/ns		1.0 V/ns			
$\Delta t_{IS}$	$\Delta t_{IH}$	$\Delta t_{IS}$	$\Delta t_{IH}$	$\Delta t_{IS}$	$\Delta t_{IH}$				
Command/Address Slew rate (V/ns)	4.0	+150	+94	+180	+124	+210	+154	ps	1
	3.5	+143	+89	+173	+119	+203	+149	ps	1
	3.0	+133	+83	+163	+113	+193	+143	ps	1
	2.5	+120	+75	+150	+105	+180	+135	ps	1
	2.0	+100	+45	+130	+75	+160	+105	ps	1
	1.5	+67	+21	+97	+51	+127	+81	ps	1
	1.0	0	0	+30	+30	+60	+60	ps	1
	0.9	-5	-14	+25	+16	+55	+46	ps	1
	0.8	-13	-31	+17	-1	+47	+29	ps	1
	0.7	-22	-54	+8	-24	+38	+6	ps	1
	0.6	-34	-83	-4	-53	+26	-23	ps	1
	0.5	-60	-125	-30	-95	0	-65	ps	1
	0.4	-100	-188	-70	-158	-40	-128	ps	1
	0.3	-168	-292	-138	-262	-108	-232	ps	1
	0.25	-200	-375	-170	-345	-140	-315	ps	1
	0.2	-325	-500	-295	-470	-265	-440	ps	1
	0.15	-517	-708	-487	-678	-457	-648	ps	1
	0.1	-1000	-1125	-970	-1095	-940	-1065	ps	1

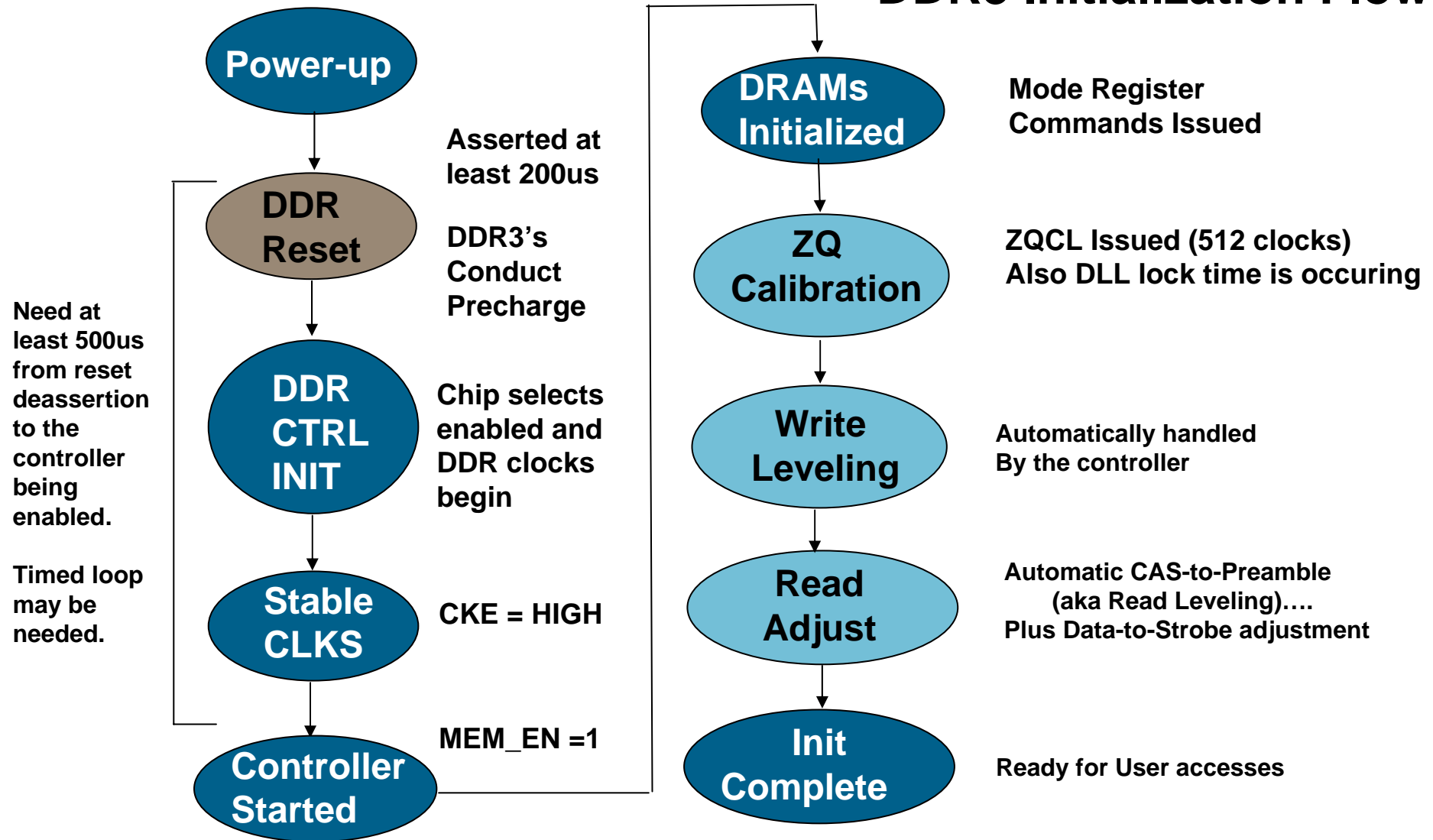
Source: JEDEC 79-2C

# Pitfall 11 – No debug or testability on BGA devices



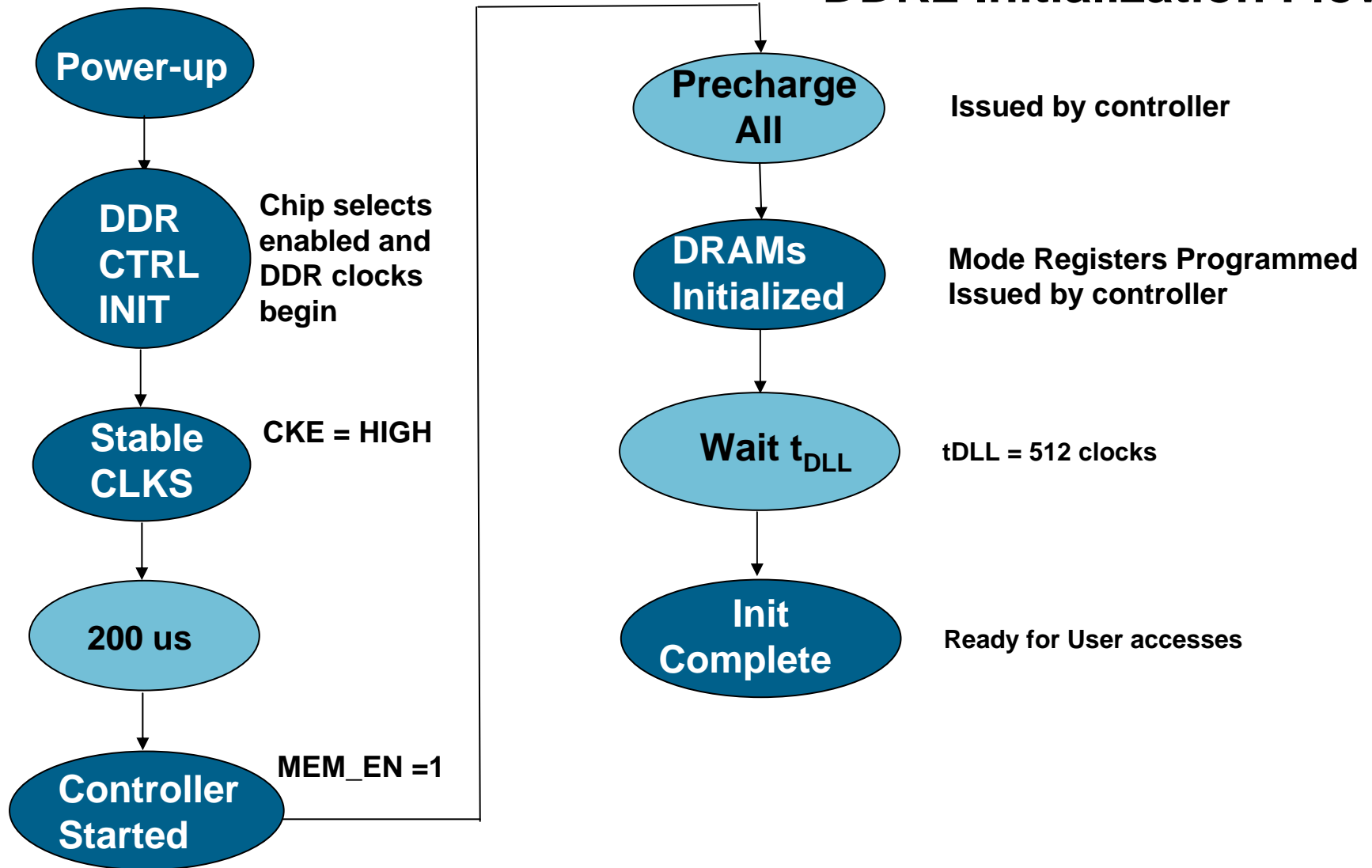
# Power up and Initialization Sequence Backup Slides

# DDR3 Initialization Flow



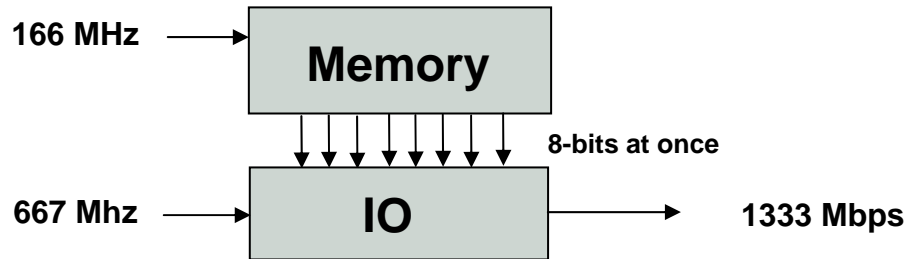


# DDR2 Initialization Flow

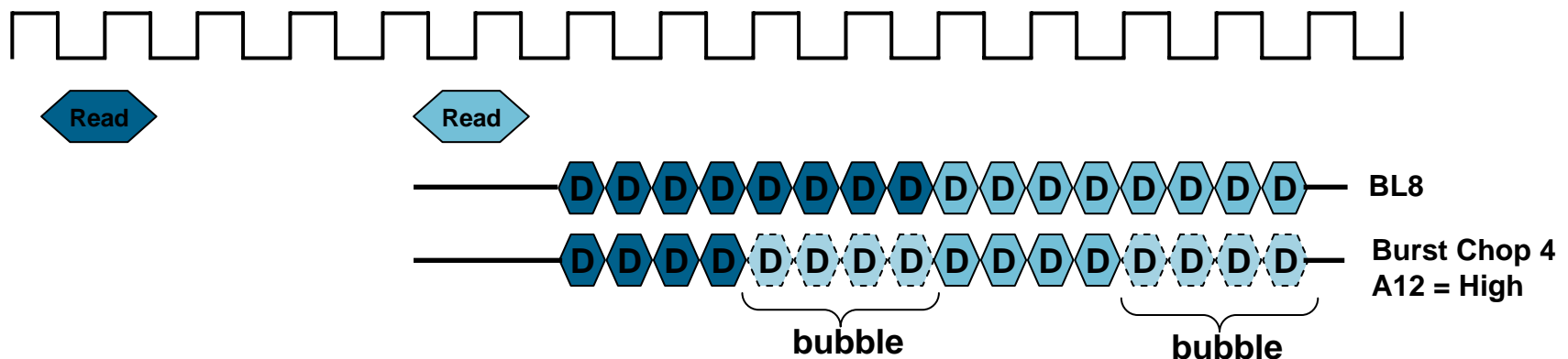


## ► Burst Length control (BC4/8 on the fly)

- 8-bit pre-fetch is standard for DDR3 memories
- Thus, burst length of 8 is default



## ► DDR3's also support 'pseudo BL4' using burst chip

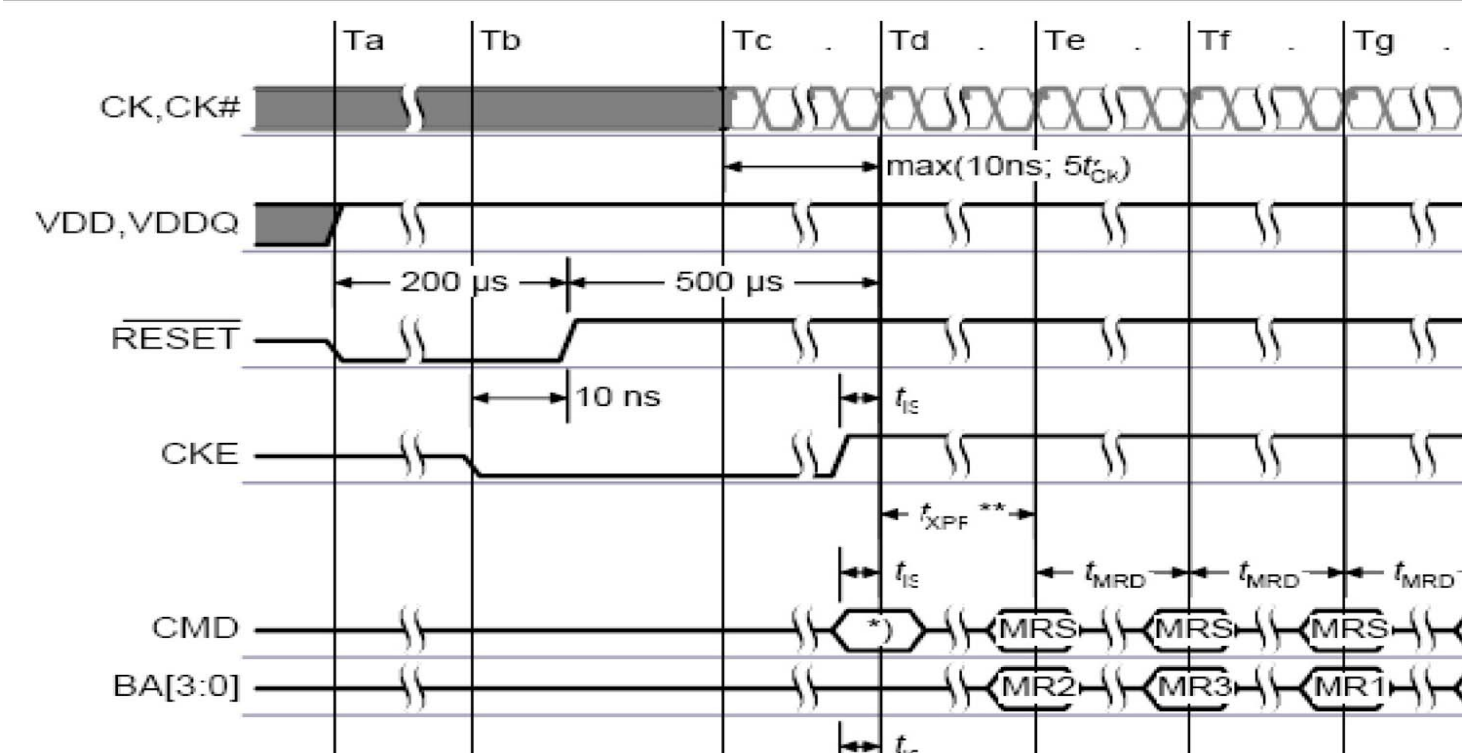


- ▶ DDR3 memories have two power pins defined.
  - Same voltage level of 1.5V nominal
  - Separate pins help reduce power supply noise/interruption
  - VDD – Core Power
  - VDDQ – IO Power
  
- ▶ Therefore, there will be 2 different cases:
  - Case 1 – two separate sources
  - Case 2 – Single voltage source for both rails

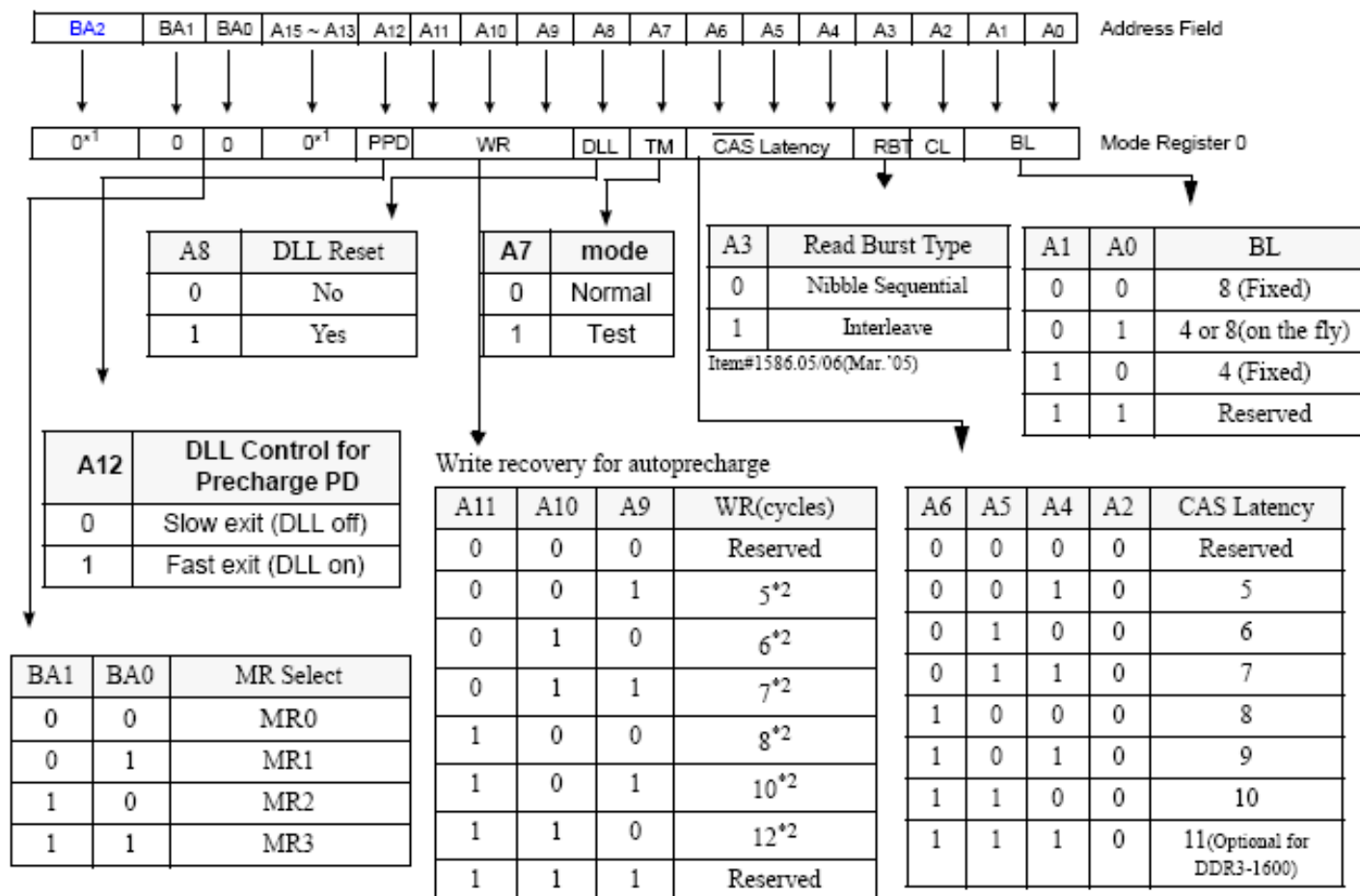
- ▶ The following should be applied whether a single voltage source or a separate voltage sources are used:
  - Apply Power:
    - RESET# is recommended to be maintained below  $0.2V \times VDD$  (min 200us) and all other inputs may be undefined
  - The voltage ramp time between 300mV to VDDmin must be no greater than 200ms
    - $VDD > VDDQ$ ,  $VDD - VDDQ < 0.3V$
  - The voltage levels on all other pins should not exceed VDD/VDDQ or be below VSS/VSSQ

- ▶ Starting with DDR3, a reset function is supported
  - All devices have a dedicated RESET# pin, operating at CMOS levels
  - Low pass filter incorporated – prevents accidental glitches
  - Voltage level of the pin should be carefully maintained to prevent loss of data
  
- ▶ Reset should be done after the power supply voltage level(s) are properly up and stabilized
  
- ▶ Reset can also be issued whenever “Warm-booting” is needed.
  
- ▶ Destructive to data contents, therefore memories will need to be re-initialized

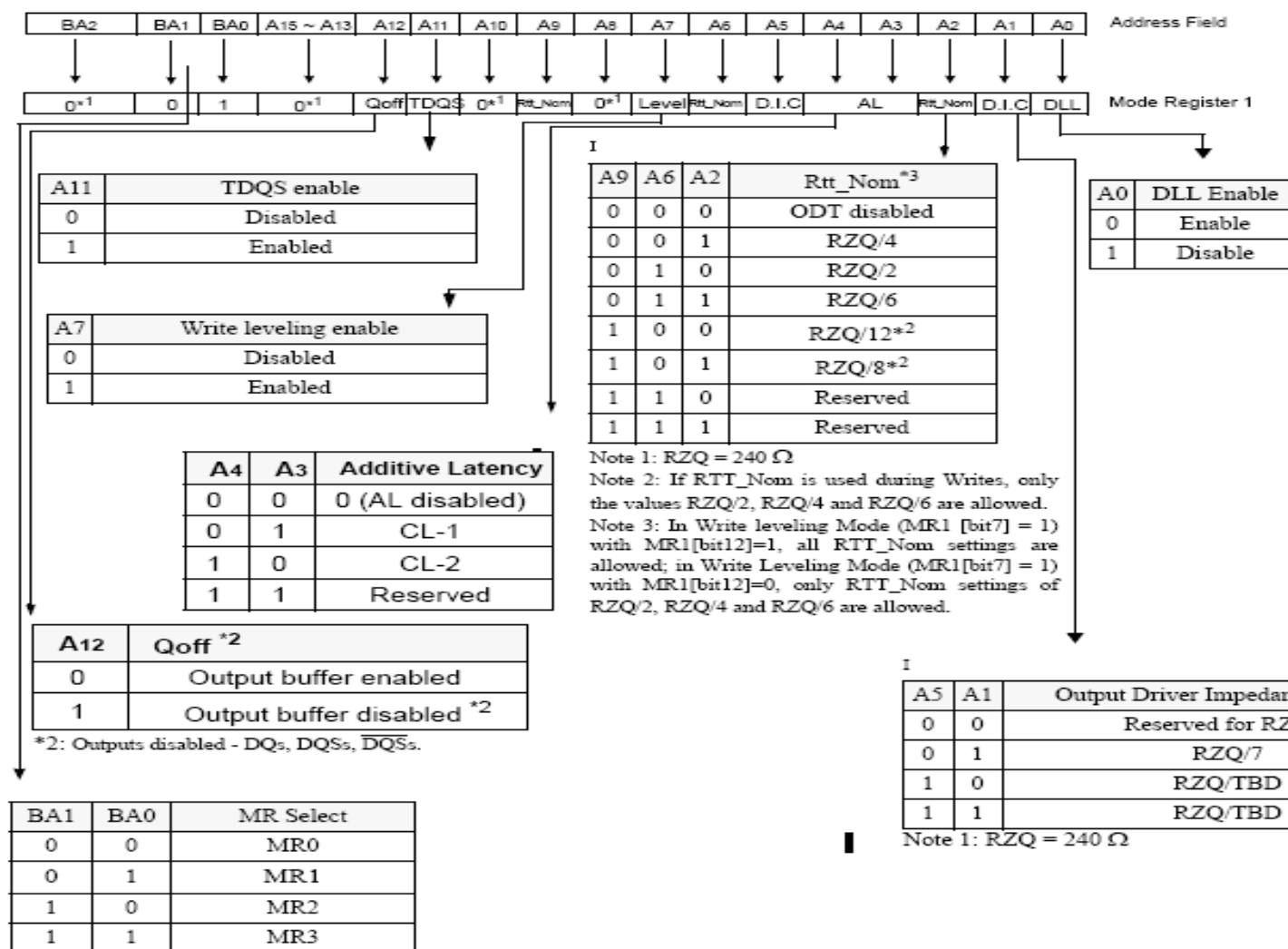
- ▶ Clocks are started as soon as a chip select is enabled.
  - Controller will ensure that the appropriate clock to CKE relationship is met

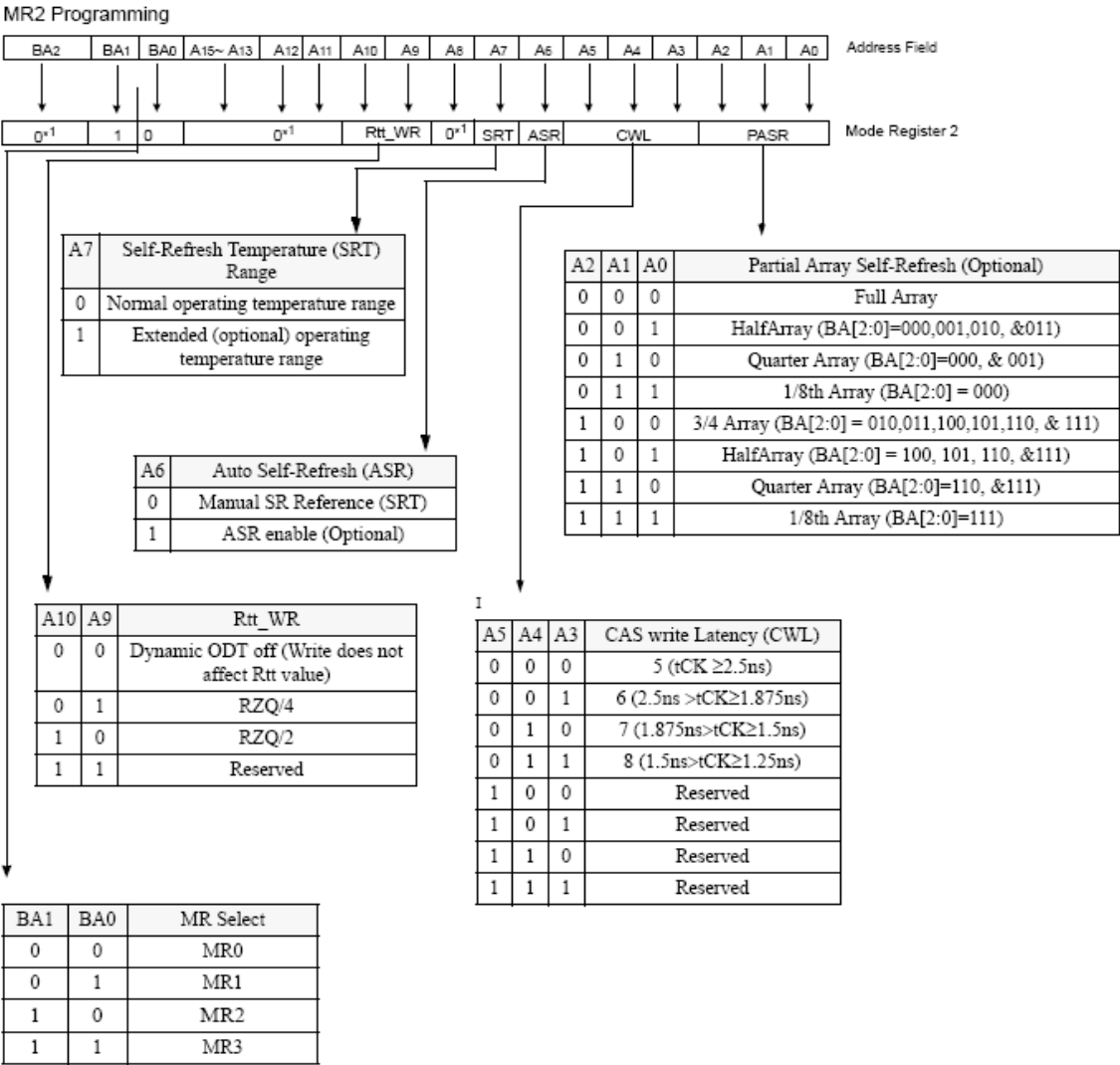


- ▶ Once clocks are stabilized, the next step should be to set the Mode Register.
  - Mode Registers set the operational mode of the DDR3 DRAMs
  - Order of programming
    - MR2 -> MR3 -> MR1 -> MR0
  
- ▶ Several new features for DDR3, such as
  - MR0 : Burst length control (BC4/8 on the fly)
  - MR1 : Write leveling enable
  - MR2 : RTT\_WR, CWL, ASR









- ▶ DDR3 SDRAMS require a ZQ resistor (240ohm +/- 1%) external to the device.
  - Used as a reference for driver and ODT calibration
  - Allows both to remain stable – independent of thermal variation during operation
  
- ▶ Therefore, the last step in the initialization process is ZQ\_long calibration sequence – after which the DDR3 memories are now ready for normal operation

